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Advanced calibration and measurement techniques for (sub)millimeter wave devices characterization

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Advanced calibration and measurement techniques for (sub)millimeter wave devices characterization

Advanced calibration and measurement techniques for (sub)millimeter wave devices characterization

Dissertation

for the purpose of obtaining the degree of doctor
at Delft University of Technology
by the authority of the Rector Magnificus, Prof.dr.ir. T.H.J.J. van der Hagen,
chair of the Board for Doctorates
to be defended publicly on
Monday 25 November 2019 at 12:30 o'clock

by

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Keywords: millimeter wave, sub-THz, on-wafer, calibration, VNA, small-signal, large-signal, characterization, wafer probes, transmission lines, CPW, EM simulation, de-embedding, load-pull, power control, instrumentation …

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To Valeria, Elisa and Poppy,
the (sometimes literal) reasons I get out of bed every morning

To Marco Di Rosa,
a better friend than I could have ever been

A Nonna Elena

Contents

1

Introduction

Homo Sapiens Sapiens is the only extant human (sub)species [1], and arguably the most "impactful" animal species in the world. The impact of human kind can be measured by the influence humans have on the ecosystem they live in (the Earth), which is not comparable to any other single animal species in the Earth's history. In time, the reasons why humans grew to "shape" the world have been much discussed. As a matter of fact, humans are not the biggest [2] nor the strongest [3] living animals, while other species have been found to have similar intelligence [4] and complex social structures [5]. Many studies relate the human success to the ability of standing, or manufacturing and employing tools (although similar skills can be found also in orangutan and chimpanzees [6]), but probably the most important skill that distinguishes humans from any other animal is their capability to *communicate*. It is true that several animals are capable of complex communication and language (Bottlenose Dolphins can call each other by name [7], while Elephants can even communicate using seismic signals [8]), but humans are the only ones capable of transmitting information through both *space* (communication can be achieved even on very long distances) and *time* (the knowledge acquired can be preserved during time, transmitted and increased during generations). In this respect it can be stated that the human world-conquer campaign started when written language was invented. Until then, although information could be transmitted orally, its preservation during time was subject to alteration. With the invention of writing, the knowledge acquired by humans had the possibility to be *stored* for long time and possibly *transported* to very far regions, allowing the accumulation and the *dissemination* of knowledge, leading to a faster species advancement. During centuries, the capability of efficiently transporting information also determined the influence and the technology advancement of a civilization. It is not by chance that the first advanced postal service (the *cursus publicus*) was established under Augustus Caesar, the first Roman emperor [9]. Also, the invention of *printing* is considered one of the cornerstones that characterizes the passage from the *Middle Age* to the more technologically advanced *Renaissance*, due to the novel capability

(a) (b)

Figure 1.1: a) Bottlenose dolphins rely on (ultra)sound production to communicate, hunt and navigate, and they have been found to be able to call other individuals by name [7]. b) African Elephants can use complex communication mechanism, including using seismic waves to signal position and danger [8].

to promptly reproduce written information in mass production, enormously augmenting its dissemination. Until modern history, however, information could only be transmitted in *deferred* time: the information was first produced and written, and then eventually transported with processes that could take long times depending on the means of transport. Only with the invention of *telecommunication*, starting in the early 19th century, information could be transmitted in *real* time. Telecommunication allowed the technological leap that characterized the last two centuries, and every technical step from then on has been supported by a newer and more effective way of communicating. It first was telegraph and phone, which still required *physical* connection between the communication points (by cable), basically allowing only one-to-one connection. Then, radio and television were invented, *wireless* technologies creating the possibility of transmitting information from one to many. Later in the 20th century, internet gave the possibility to individuals to *independently* access a high volume of information from their home, and the introduction of cellular phone allowed people to communicate from any position in the world. The era of smartphones, the era we currently live in, is characterized by an enormous availability of information, to basically anybody, everywhere in the world. It is reasonable at this point to start wondering what will be the next telecommunication step, and how to enable it. In the last decade, the fast development of electronic devices, in conjunction with computer science and artificial intelligence (AI) has fostered the development of new applications that promise to revolutionize everyday life, from business to entertainment. From big data analytics and augmented reality used to support industry, to 3D media and virtual reality for video gaming, these emerging applications are, day by day, changing the way telecommunication systems are used. However, in a world in which the *portability* is the key requirement for each device, the real challenge is to make these applications *sustainable* for the mobile network infrastructure. As a matter of fact, such *bandwidth*

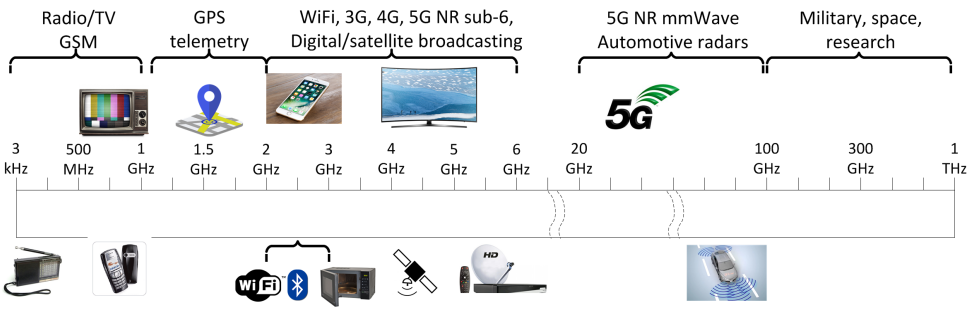


Figure 1.2: This table depicts the spectrum occupation by most of the RF/microwave consumer application. Almost all current commercial wireless application employ frequencies lower than 6 GHz, while millimeter waves are at the moment mostly dedicated to military and space application.

demanding applications need reliable and efficient connectivity, where any high latency or data corruption would just be not sustainable, determining the failure of the application. To really bring these applications to the end users, new communication paradigms will need to be introduced, with an increasing occupation of an already crowded radio spectrum. The congestion of the RF and microwave spectrum risks to be the real bottleneck for the development of new applications. Most of wireless applications work at frequencies lower than 6 GHz (see, Figure 1.2), and communication channels are typically bandwidth limited, while most of the bandwidth slots are already allocated by local and global regulations, limiting the space for the introduction of new applications and systems. On top of that, data intensive applications would need large bandwidth allocation and sufficient guard space to avoid interference. For these reasons, the attention is moving towards the exploitation of the underutilized millimeter wave and sub-millimeter wave portion of the spectrum (30 GHz to 1 THz), where the high carrier frequency and low spectrum congestion would guarantee large bandwidth availability, enabling the needed ultra-high data rate communication capability. In this respect, also the discussion about the next generation of mobile broadband technology (5G) is moving towards considering millimeter wave frequencies as possible candidates for future application deployments, with frequencies between 30 GHz and 87 GHz raising interest in the research community, with some already being assigned for testing [10].

1.1. Challenges related to millimeter wave applications

Developing applications and shifting wireless telecommunication to millimeter wave frequencies is, unfortunately, not a trivial task. The shortcomings are first of all physical, as propagation of electromagnetic waves at higher frequency is more prone to suffer from atmospheric conditions. Atmospheric gases interact with electromagnetic waves, in specific sub-bands, blocking long distance signal propagation (see, Figure 1.3a). Moreover, phenomena such as high humidity and rain tend to increase propagation losses in the mm-wave range. This means that outdoor trans-

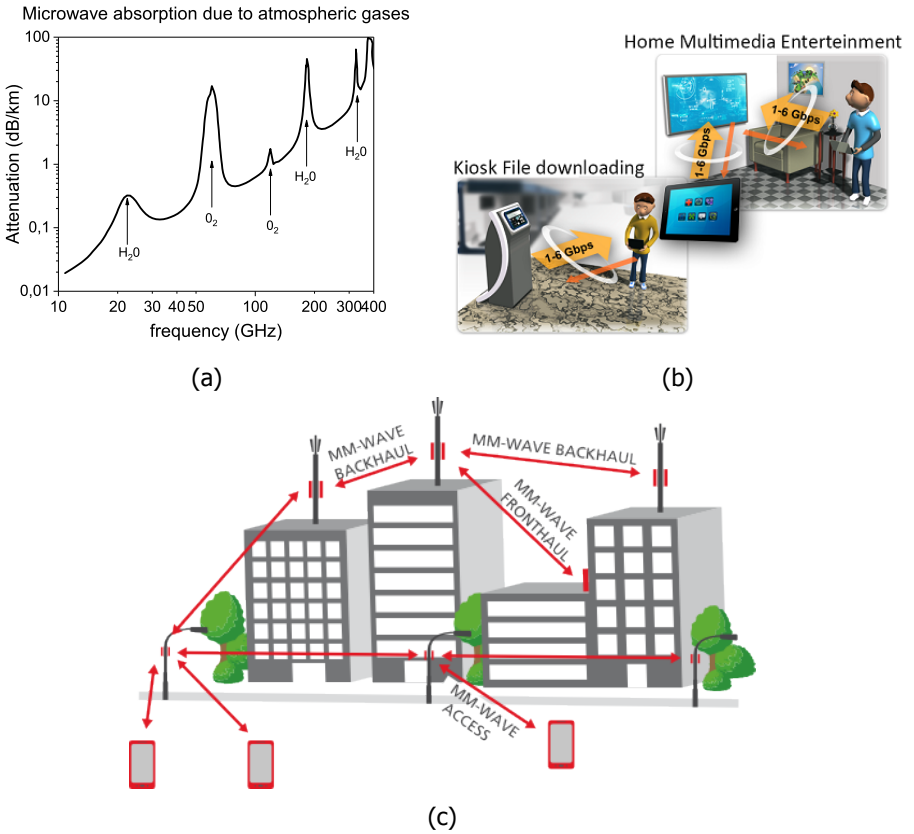


Figure 1.3: a) Absorption of microwave radiation from the atmosphere, highlighting the oxygen and water attenuation peaks. b) In-door application for millimiter wave frequencies include close-range media distribution and kiosks for mobile syncronization of large data. c) Open-space application for mm-wave frequencies require clear line-of-sight between the communicating devices, requiring dense networks of base stations and access points.

missions would be strongly affected by weather conditions, which cannot be controlled if not barely predicted with relatively short notice time. For these reasons, millimeter wave wireless technologies are mainly intended either for outer space applications (satellite-to-satellite applications, space imaging), where the electromagnetic propagation is not affected by the atmospheric conditions, or for short range applications, like automotive radar, security imaging, indoor media sharing (for home/in-flight entertainment, or for office networks), virtual reality or data sharing kiosks (see, Figure 1.3b), so that the electromagnetic propagation would not be compromised by the high attenuation related to atmospheric dispersion. The use of mm-wave frequencies for cellular communication is also being considered [11] (see,Figure 1.3c). The way this kind of application is conceived, however, requires clean line-of-sight between communicating devices, and it is constrained

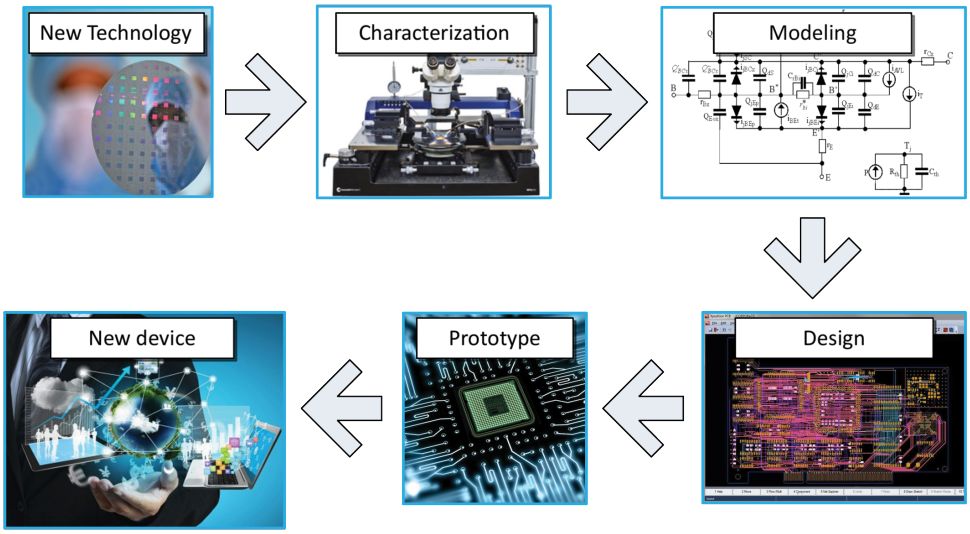


Figure 1.4: Development flow for (telecommunication) electronic devices based on semiconductor technologies.

by the use of high-density small cells in order to neglect the effects of high atmospheric attenuation.

While the physical constraints define the space of applicability for millimeter wave wireless technologies, the development of any commercial application needs to be supported by a proper technological advancement. In this respect, the continuous improvement in performances of integrated/semiconductor devices, in terms of speed of operation, space occupation and power consumption is fostering the implementation of the first commercial millimeter wave systems [12]. Technology, however, is still not mature enough to open the possibility for consumer applications in the (mobile) telecommunication market for millimeter waves. When considering mobile applications, electronic devices need to be developed to guarantee some main requirements:

- As mobile systems rely on limited power supply (i.e., batteries), the power consumed by the electronic circuitry should be limited;
- The quality of the signals transmitted (and received) should be sufficient to guarantee a reliable communication;
- The system should guarantee high reliability (durability) and resilience to adapt to different communication conditions.

As current state-of-the-art technology still presents limitations in meeting those requirements for millimeter wave communications, the further development of new devices is necessary [13]. The development flow characterizing the realization of a commercial application is composed of several steps, the most important of which

are summarized in Figure 1.4. First step is represented by the definition of the device fabrication technology, which is the set of chemical/mechanical processes and rules used to fabricate electronic devices on wafers of semiconductor materials. The semiconductor industry is characterized by a continuous innovation in the fabrication technology, involving improvements in the material composition, as well as in the geometrical feature sizes. These directly impact on the electrical performances of the individual devices that are embedded in the semiconductor material (the *front-end-of-line* or *FEOL*) and on the interconnection between the devices (*back-end-of-line* or *BEOL*). The development of a new fabrication technology brings, as a consequence, a new generation of electronic devices, both active (i.e., capable of actively control/amplify electrical signals, like *transistors*) and passive (i.e., *transmission lines*, *capacitors*, *inductors*, etc.) which need, first of all, to be characterized. Using accurate data from measurements, the device characteristics can be used for the development of compact models, to be used for the prediction of the device performances in different working conditions. The use of models allows combining different devices to design complex circuitry, where the overall performances can be predicted with extensive use of circuit simulators. The design is finally used for the realization of a prototype circuit, manufactured in the target production technology, and when the prototype is successfully tested it can be then turned into a final product to be introduced to the market. If the performances of the prototype do not comply with the specifications, the development cycle needs to restart from one of the intermediate steps. Each cycle can have several months of duration, and be characterized by costs that can sum up to several millions of Euro. It is therefore essential from both an engineering and economic point of view to optimize the device development cycle. An important condition for the reduction of time-to-market and development costs of new devices is the availability of **accurate** and **reliable** characterization processes, capable of measuring the characteristics of the devices under test (DUTs) directly in the environment in which they are manufactured (i.e., **on-wafer**) and in the frequency range in which they are supposed to be employed. While for RF and microwave frequencies many solutions already exist and are widely available on the market, when it comes to higher frequencies (i.e., higher than 60 GHz) the availability of measurement equipment reduces, and the existing instrumentation presents lower performances in respect to the microwave counterpart. It becomes of primary importance, for the fostering of millimeter wave applications, to work towards the development of novel characterization strategies, allowing to achieve accurate measurements of on-wafer millimeter wave devices.

1.2. Thesis objectives

This thesis concentrates on the analysis of some of the major challenges related to the characterization of (sub)mm-wave devices, especially regarding on-wafer measurements, and proposes a series of possible solutions and novel approaches. The analysis is first dedicated to the *calibration* of on-wafer test-benches, which is the set of processes required to correct all the errors introduced into the measurements by the characterization equipment. The main bottlenecks of conventional calibration

approaches at millimeter waves are first identified, and a novel simulation-based approach for the characterization of on-wafer calibration artifacts is proposed, with a focus on transmission lines. Then, we introduce a novel transmission line structure, the *capacitively loaded inverted coplanar waveguide (CL-ICPW)*, dedicated to the implementation of direct calibration on silicon back-end-of-line (BEOL), which allows moving the measurement plane directly at the intrinsic (FEOL) device plane. The focus of the thesis will then shift towards the implementation of accurate instrumentation and test-benches. First, we describe the use of a mixed-signal active load pull architecture for the characterization of millimeter wave devices in the frequency range between 50 GHz and 65 GHz, including the design of the dedicated waveguide-based test-bench and its optimization for low- and high-power devices. Then we introduce a novel approach for the measurement and the control of power during small and large signal characterization of millimeter wave devices, which allows using conventional measurement instrumentation (Vector network analyzers, millimeter wave extenders, power meters) to achieve refined power control and vector corrected power measurement with unprecedented speed. This method also opens the possibility to develop active load-pull approaches for frequencies up to 1 THz, as will be introduced by the end of this dissertation.

1.3. Thesis outline

This dissertation is structured as follows.

In Chapter 2, a general overview of the conventional calibration approaches for microwave (on-wafer) measurements is provided, in order to highlight the limitations of these methods when the measurement frequency is increased towards the millimeter wave range.

In Chapter 3, an analysis on the sources of error in millimeter wave measurement test-benches for on-wafer measurement is performed. First, the attention is posed on probe-tip calibrations, and the error associated with the common practice of transferring the calibration error terms from an off-wafer calibration substrate to an on-wafer environment in which the device under test (DUT) is embedded, are analyzed. Then, the chapter will highlight the importance of performing the calibration using test-structures already embedded in the DUT environment (i.e., on-wafer), proposing a novel approach for extracting the characteristic impedance of transmission lines employed for thru-reflect-line (TRL) calibration, which is the most important parameter to be known during calibration whilst the more difficult to properly extract by means of measurements.

Chapter 4 introduces the use of capacitively loaded inverted CPWs (CL-ICPW) in test fixtures for (sub)mm-wave device de-embedding. These transmission lines allow implementing a distributed TRL de-embedding of the fixture, opening the possibility for *direct* calibration up to the DUT reference planes, without the need of additional de-embedding procedures.

Chapter 5 describes the implementation of a waveguide-based mixed-signal active load-pull test-bench, working in the WR-15 waveguide bandwidth, and its use for the large-signal characterization of millimiter wave devices and circuits.

In Chapter 6, a methodology is described for the accurate measurement and

control in conventional (sub)mm-wave small- and large-signal test-benches, and a novel approach for load-pull measurements at frequencies higher than 75 GHz is proposed.

Finally, Chapter 7 will be used to draw some conclusions and make some recommendation for future developments and use of the present work.

2

Conventional high frequency calibration and measurements

The characterization of high frequency electronic devices relies on the quantification of diverse device properties by means of measurements performed on a device-under-test (the *DUT*) at the target operating frequency and, in case an active device is considered, under different operating conditions. The kind of parameters that need to be measured also depends on the application in which the DUT has to be employed. For devices that need to be used in telecommunication applications, for example, it can be important to quantify the capability of properly reproducing an analog signal, without loss of information. This capability is typically linked to the *linearity* of the device. A linear device is capable of reproducing a replica (in frequency and phase) of an input signal, without introducing any *distortion*[1]. The linearity of active devices (like transistors, or amplifiers) can be typically guaranteed by providing low-power signals to the device, and then measuring its response. In this sense, an active device is defined to operate in its linear region when its DC characteristics (i.e., its biasing conditions) are not influenced by the RF signal applied. For this reason, *linear* measurements of active devices are also commonly addressed as *small-signal* measurements. On the other end, to verify

Parts of this chapter have been published in Improved RSOL planar calibration via EM modelling and reduced spread resistive layers (2015) [14], On the definition of reference planes in probe-level calibrations (2016) [15] and Fused Silica based RSOL calibration substrate for improved probe-level calibration accuracy (2016) [16].

[1] Note that the maximum level of distortion discriminating linear from non-linear operation is typically set through standard definitions using various metrics, like *intermodulation distortion*, *error vector modulation*, *spectral regrowth*, etc.. Discussion of these metrics is out of the scope of this dissertation.

the device linear performances, it might be needed to drive it with larger input power levels. In this case the power provided to the input of the device needs to be increased so that it can influence its DC characteristic, and in this case is said to be in *large-signal* operation. This kind of operation typically introduces non-linearity effects in the device RF behavior, that need to be measured (large-signal measurements). The complete characterization of active devices always requires both small- and large-signal measurements even for millimeter and sub-millimeter frequencies. This chapter will be mostly dedicated to the most common measurement system employed for high frequency small signal measurements, the vector network analyzer (VNA). First part of this chapter will be dedicated to a general description of the VNA. Then, important part of the analysis of the measurement systems is dedicated to the errors introduced by the equipment, and the *calibration* strategies that are needed for correcting them. A more specific analysis of the use of VNAs at millimeter waves and beyond will be presented in Chapter 6. The last part of this chapter will be dedicated to the use of VNA setups for the measurement of on-wafer devices, and the related calibration strategies. Special attention is dedicated to the ambiguities in the selection of the calibration reference plane during planar measurements, and on how to choose the appropriate calibration approach depending on the frequency of operation.

2.1. The Vector Network Analyzer

The *Scattering matrix* is widely used to describe the electrical behavior of linear devices [17]. The S-parameter of an N-port network, where each port *i* is terminated to a specific reference impedance Z_{0i} are defined as:

$$\begin{pmatrix} b_1 \\ \vdots \\ b_n \end{pmatrix} = \begin{bmatrix} S_{11} & \cdots & S_{1n} \\ \vdots & \ddots & \vdots \\ S_{n1} & \cdots & S_{nn} \end{bmatrix} \cdot \begin{pmatrix} a_1 \\ \vdots \\ a_n \end{pmatrix} \tag{2.1}$$

Where a_i is the *incident* wave at a specific port i, while b_i is the *reflected* wave at a specific port i. It is important to notice how the S-parameters, and the incident and reflected waves, are reported in literature with different formalism, which sometimes lead to slightly different definitions and properties of other related parameters [18, 19]. In Equation (2.1) and in general in this dissertation, the pseudo-waves formalism is used, based on the one presented in [19], and described in detail in Appendix A. In the case of RF/microwave devices, S-parameters can be employed to compute relevant figures of merit like *small-signa gain*, *insertion loss*, *reflection coefficient* or *amplifier stability*. The measurement of the (frequency dependent) S-parameters of a DUT is commonly performed by means of a vector network analyzer (VNA) [20]. A VNA can be used for measurements of DUTs with one or multiple ports, and is capable of frequency sweeping (from kHz to 1.1 THz, employing different hardware setups) and power control at each test port. In this section, we present a general overview of the principle of operation of VNAs, discussing the limitations associated to this kind of equipment when measuring at (sub)mm-waves.

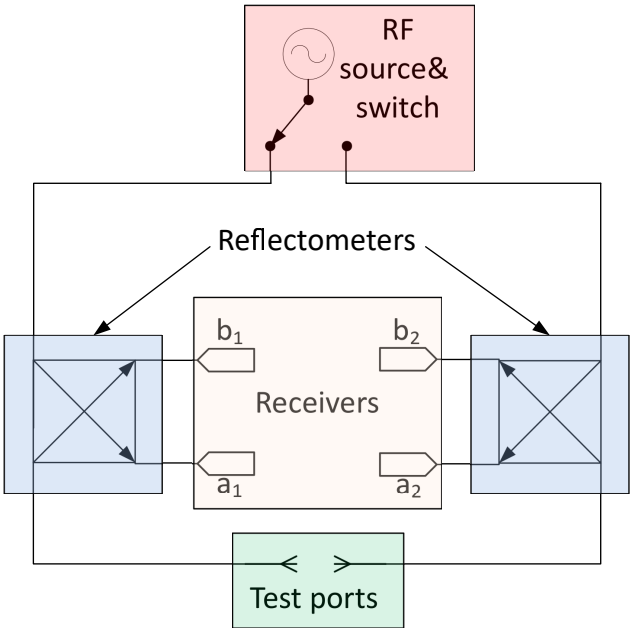


Figure 2.1: General system schematic of a VNA, including the main four stages.

In general, it is possible to schematize a VNA as composed of four main stages (see, Figure 2.1 for two-port example):

1. *The signal generation stage*, where an RF signal is generated, at an appropriate frequency and power level, for each test port.
2. *The reflectometer stage*, where replicas of the *incident* and *reflected* waves are sampled, for each test port. The sampled waves are typically acquired by means of intermediate frequency receivers;
3. *The test ports*, representing the connection point between the VNA and the DUT ports;

From this simple schematic, several variations are possible in terms of number of test ports, number of sources and receivers, add-ons for advanced measurements, etc..

Signal generation

The measurement of the S-parameters is based on the capability to provide an appropriate stimulus, at a given frequency of operation, and to measure the corresponding response of the device. The signal provided to the DUT is typically sinusoidal, but more advanced measurements may require more complex signal generation (pulsed, multi-tone, modulated, etc..). The generation of sinusoidal, frequency swept signals is typically performed by means of synthesizers, where a

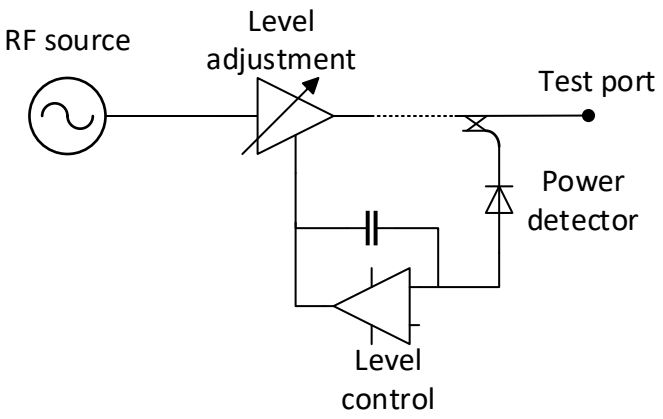


Figure 2.2: Simplified schematic of an ALC loop in VNAs.

phase locked VCO is employed to provide a swept frequency response in a certain, limited, frequency range [21]. In order to guarantee broadband frequency generation, multi-path configurations are typically used, where frequency multiplication, division and mixing allow using a single VCO for multi-octaves frequency coverage [22]. An important aspect to be taken into account during generation is the power control: having a leveled and controllable power delivered at the test-port is generally desirable when measuring active devices, where the DUT's operation (small signal or large signal) needs to be characterized versus the stimulus level (see, also Chap. 6). In VNAs, the power control is achieved by means of the *automatic loop control* (ALC). The ALC system is conceptually simple: the power at the test-port is monitored by means of a detector, while a negative feedback loop is used to control a level adjustment unit (a variable gain amplifier or a variable attenuator) allowing proper power leveling, as shown in Figure 2.2.

Reflectometers

Following the definition of S-parameters [18], the measurement of such quantities is based on the capability of sampling, at each DUT port *i*, the incident wave a_i and the reflected wave b_i. This task is typically performed by means of *reflectometers*. A reflectometer is, at its essence, a 4-port linear device, conventionally schematized as in Figure 2.3. Supposing that the VNA source is connected to port 1 of the reflectometer, while port *i* of the DUT is connected to port 2 of the reflectometer, this device allows to have at the coupled ports 3 and 4 quantities proportional to the scattered waves a_i and b_i, respectively. Different kinds of directional devices can be used to realize a reflectometer, like *directional couplers*, *directional bridges* or splitter based components (i.e., *1 + Gamma reflectometers*)[22]. Regardless of the implementation, reflectometers are typically characterized by some fundamental parameters, such as the *mainline loss* L (attenuation of the a_i wave), the *coupling* C

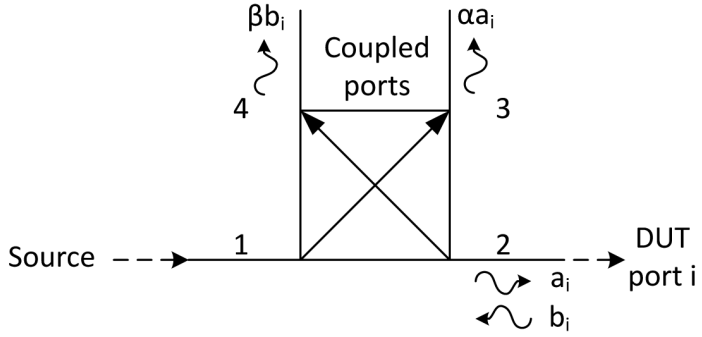
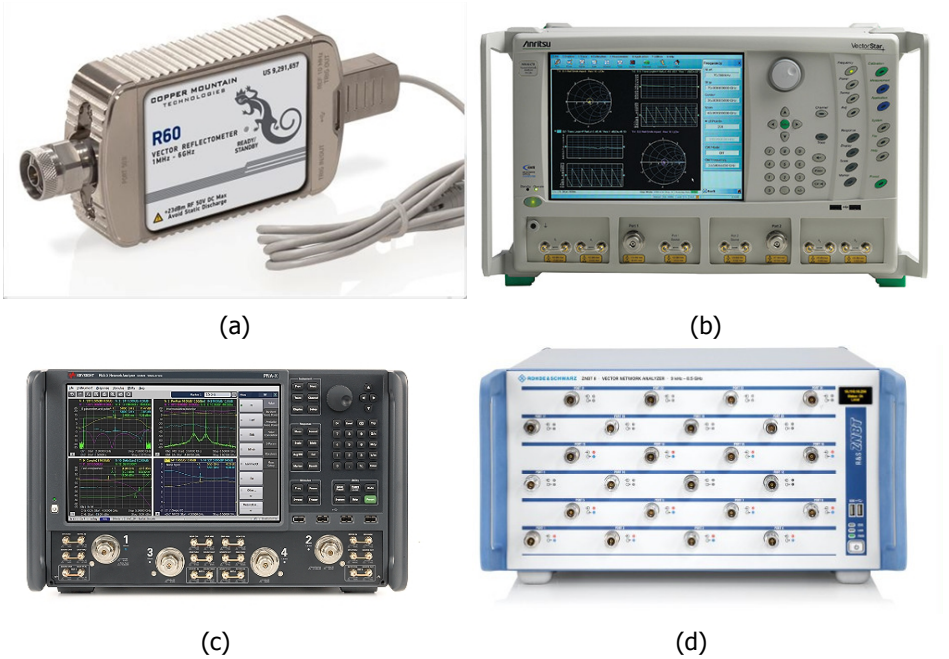


Figure 2.3: Generalized schematic of a reflectometer.

(attenuation of the coupled wave), the *directivity* D (ability to separate the coupled a_i wave from the b_i wave) and the *isolation* I (power coupling between the input port and the isolated port, i.e., leakage from input to b wave and from output to a, which is linked to directivity and coupling as D = I + C dB). Ideally, for a perfect signal separation (and S-parameter measurement) the losses should always be negligible, the directivity infinite, and the coupling equal between the ports. In this case, the coupled waves would be directly proportional to the scattered waves (αa and βb), and their ratio could be directly linked to the S-parameter of the DUT. In practice, the inevitable non-idealities make the coupled waves always affected by frequency dependent errors. Calibration procedures allow, in principle, to correct for these errors, irrespectively of the quality of the reflectometer parameters (also called *raw performances*), and how they deviate from ideality. In reality, however, good raw performances have strong impact on the *stability* of the calibration [21]. The implications of this on millimeter wave measurements will be further discussed in Chapter 5.

Test ports

The test ports of a VNA represent the interface between the instrument and the DUT. In principle, a VNA can have one or multiple test ports, while the most common configurations for modern commercial VNAs are 2-ports and 4-ports. Some examples of VNAs with different numbers of test ports are displayed in Figure 2.4. The primary VNA test-ports are constituted by coaxial rugged connectors, which are typically present in the instrument front panel or in an external test set. However, being not always possible to connect a DUT directly at the front panel ports of a VNA, the typical configuration involves the use of coaxial cables to connect the instrument to the DUT ports. In this case, the *extended* test ports are considered to be the coaxial connectors interfacing with the DUT, see Figure 2.5. In principle, the VNA test ports can be seen as the plane at which the S-parameters measurement actually takes place. In practice, the actual measurement plane in a VNA is at the



(a) (b)

(c) (d)

Figure 2.4: Examples of VNA configurations with different number of test ports. a) Copper Mountain Technologies R60, a 1-port VNA operating from 1 MHz to 6 GHz. b) Anritsu VectorStar, 2-port VNA operating from 70 kHz to 70 GHz. c) Keysight PNAX, 4-port VNA operating from 10 MHz to 67 GHz. d) Rohde&Schwartz ZNBT8, 24-port VNA operating from 9 kHz to 8.5 GHz.

receivers, where the physical quantities (i.e., the scattered waves) are effectively acquired. For this reason, VNAs need procedures that allow relating the acquired quantities to the S-parameters at the test ports, or more specifically to the measurement reference planes. These procedures go under the name of *calibration techniques*, and will be discussed further in this chapter.

2.2. VNA Calibration

When using the VNA to perform the characterization of a DUT, the goal of the measurement is to obtain the physical characteristics (i.e., the S-parameters) of the device at a user defined reference plane (i.e., the extended test ports in Figure 2.5). It is necessary to model all the system imperfections present between the instrument's primary test ports and the measurement reference planes. This is typically done by defining a fictitious network incorporating the system's errors. The process of defining, quantifying and mathematically correcting this error network, in order to set the measurement reference planes, is called VNA calibration. In general, two big groups of errors can be identified: *systematic* and *random* errors. While random sources of errors (i.e., noise, repeatibility, etc..) can only be described by means of qualitative/statistic figure of merit, systematic errors (like

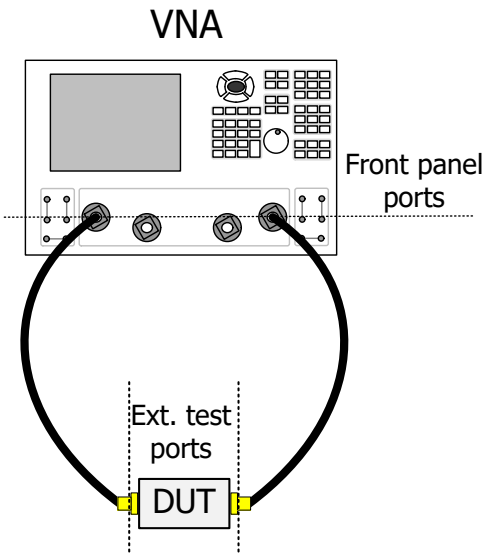


Figure 2.5: Example of test port extension from VNA front panel to the DUT measurement plane, by means of coaxial cables.

losses, directivity, source match, load match, etc..) generally allow a proper quantification, and therefore can be corrected by means of calibration. For a complete review of the systematic contribution to error in a VNA, the reader is invited to read [23]. When the error network is subtracted from the measurement results, it is possible to obtain a *corrected* measurement representing the most accurate estimate of the actual S-parameter of the DUT.

The way a certain calibration procedure is performed depends, on a first instance, on the way the error network is modeled. As a matter of fact, diverse error models exist, which lead to different calibration methods. For the specific case of two-port VNAs, two main error models are typically employed for calibration, the *12-terms* and the *8-terms*.

12-terms error model

The 12-terms error model is the most widely used, while it was developed for older, less advanced VNA architectures, that were based on the use of only three receivers [22]. In this case a clear differentiation between the forward (power is applied at port 1) and reverse (power is applied at port 2) measurement directions is needed. As a matter of fact, this model describes the two measurement phases with two separate error sets (called the forward and reverse error *adapters*), which can be conveniently represented by means of flow graphs, as shown in Figure 2.6. The model includes a total of 12 independent *unkwnown* terms, describing the overall systematic errors in the VNA, and that need to be quantified in order to correct the measurements. The terms e_{30} and e'_{03} are associated to cross talk errors, and can typically be directly measured using S_{21} and S_{12} obtained when terminating port 1

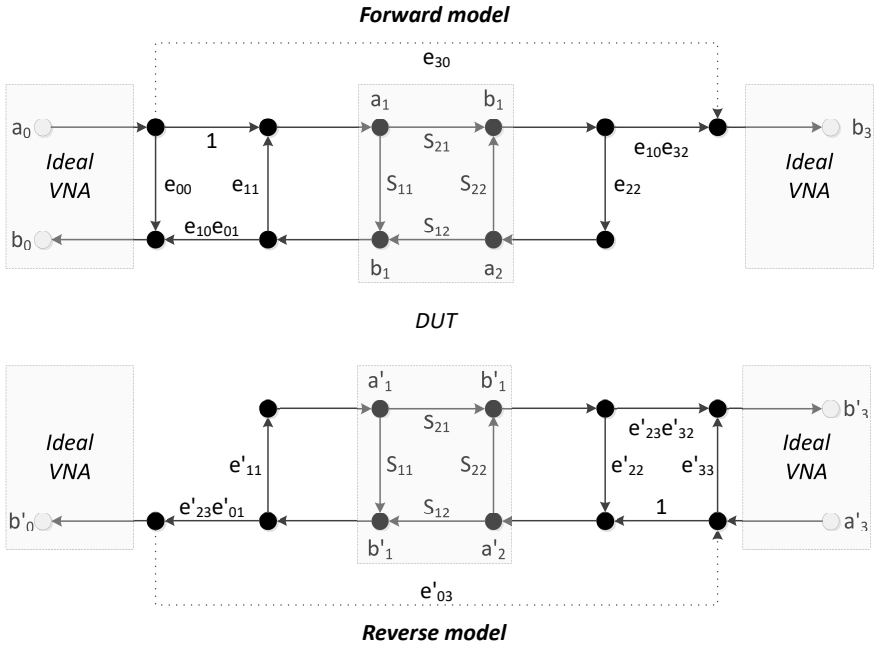


Figure 2.6: Flow graph representation of the 12-terms error model of a generic VNA

and port 2, reducing the number of unknowns to 10. For the other terms, for the forward mode, a typical calibration procedure would require to:

1. Measure three independent one-port DUT with known reflection coefficient (*calibration standards*) to evaluate e_{00}, e_{11} and $e_{10}e_{01}$ (also called one-port calibration).

2. Connect ports 1 and 2 together to obtain e_{22} and $e_{10}e_{32}$.

The same procedure can be applied also to the reverse mode, to obtain all the required error terms [23]. The calibration standards employed during step 1 can be ideally of any kind, as long as their reflection coefficient is known for all the frequencies of interest. In practice, it is preferable, to avoid undetermined expressions in the equations and to maximize the dynamic range of the VNA, to use calibration standard with calibration coefficients as different as possible from each other. Also in step 2, a transmission line can be used in place of a direct interconnection between port 1 and port 2, as long as its S-parameters are known in advance. The most commonly employed calibration method based on the 12-terms error model, which is also the most widely used calibration for coaxial applications, is the Short-Open-Load-Thru (SOLT) calibration, in which a short, an open and a matched termination ($\Gamma_L \simeq 0$) are used as the three independent standards, and a direct connection (thru) is used for the second calibration step. Peculiarity of the SOLT is that the S parameters of the calibration standards needs to be fully

and accurately known, for all the frequencies of interest, in order to apply the correction algorithm. This means that the standards need to be pre-characterized (using a reference calibration or alternative measurements methods), modelled (using behavioral representation of the standard) or simulated to acquire the required information. For this reason, SOLT calibration tends to be less accurate than other techniques requiring smaller knowledge of the standards (like thru-reflect-line and line-reflect-match), especially in conditions where the S-parameters of the calibration artifacts are more complex to predict, like in the case of on-wafer measurments.

8-terms error model

When separate receivers are used for all the scattered waves, then the separation between forward and reverse model can be avoided. In this case, the 12-terms error model can be substituted by equivalent error models, featuring a lower number of error terms, without any loss in accuracy [24]. First, let's assume that the cross-talk leakage is neglectable (or it can be determined in a separated calibration procedure). Then, let's consider the switch to be perfect, and the load match to be insensitive of the switching from forward to reverse mode of the VNA. The latter assumption can only be considered valid when using four separate receivers for the scattered waves, as this allows to mathematically correct for the switch error through the so-called *switch term correction* procedure [24]. In this case, it is possible to use a different error model comprising only 8 error terms, like the one depicted in Section 2.2. The 8 terms error model basically consists in two independent error adapters, one between port 1 and the input of the DUT (*error adapter X*) and one between port 2 and the output of the device (*error adapter Y*). Being the error boxes and the DUT in a cascade configuration, it is convenient to mathematically represent the problem using cascade matrix. If T_M is the cascade matrix of the measurement, then [25]:

$$\mathbf{T}_M = \mathbf{T}_X \cdot \mathbf{T}_{DUT} \cdot \bar{\mathbf{T}}_Y \tag{2.2}$$

where $\bar{T}$ represents the transpose version of a matrix T. In this case, the goal of the calibration procedure will be to determine the matrices T_X and T_Y, representing the cascade matrices of the error adapters X and Y, respectively. Once these are quantified, the measurement can be error corrected by simply inverting the equation, as:

$$\mathbf{T}_{DUT} = \mathbf{T}_X^{-1} \cdot \mathbf{T}_M \cdot \bar{\mathbf{T}}_Y^{-1} \tag{2.3}$$

Please notice that, for measurements of S-parameters (i.e., ratios of scattered waves) the independent terms are actually seven and not eight, as the name of the model would suggest. For this reason, a total of 7 independent readings is needed for the mathematical solution of the problem, and it can be demonstrated that this can be achieved by measuring at least *three* two-port calibration standards [26], while it is not necessary to know all the S-parameters of these standards. It is important to stress that both the 12-term and the 8-term error models describe *exactly* the same system and the same errors. Thus, in the assumption of having a VNA with four independent receivers, the two models are interchangeable. It is

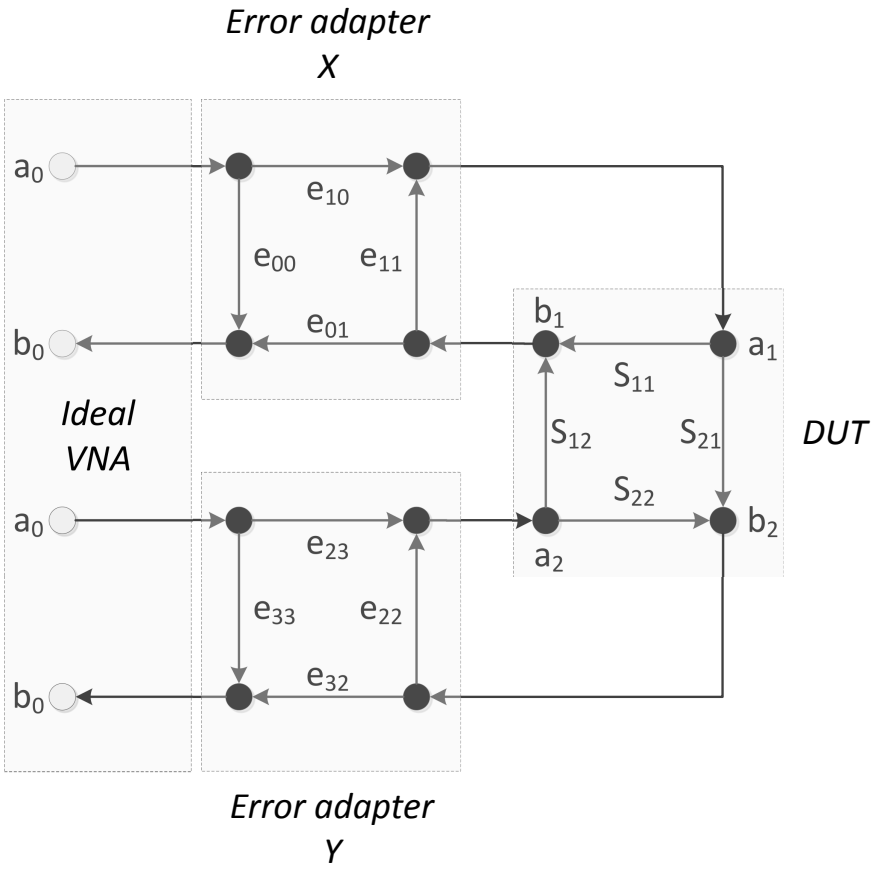


Figure 2.7: Flow graph representation of the 8-terms error model of a generic VNA

indeed possible to transform the 8-term error model in a 10-term error model [24], and the 10-term to 12-term by also including the cross-talk leakage.

The most commonly used calibration procedures for 8-terms error model are:

- Short-Open-Load-Reciprocal (RSOL) [27]
- Line-Reflect-Match (LRM) [28]
- Thru-Relfect-Line (TRL) or Line-Reflect-Line (LRL) [29]

Ultimately, the goal of any of the abovementioned calibration methods, irrespectively of the error model and the implementation, is to:

1. Define the reference impedance of the measurements, which will determine the domain of definition of the S-parameters;
2. Define the position of measurement reference plane, i.e., the position of the ”extended” test-ports of the VNA.

Table 2.1: Relation between reference impedance and reference plane location with the specific calibration standards of SOLT, RSOL, TRL and LRM methods

	SOLT	**RSOL**	**TRL**	**LRM**
Reference impedance Z_{ref}	Z_{ref} std definitions	Z_{ref} lumped std definitions	Z_{ref} line std	Z_{ref} load std
Reference plane location	lumped std	lumped std	Center of the thru std	Center of the thru std

While, in principle, the abovementioned calibration procedures are equivalent in terms of accuracy, the way these objectives are pursued, and the residual uncertainties, are in practice strongly dependent on the choice of the standards, i.e., the manufacturing quality as well as the accuracy of the standard models. For each calibration method, it is possible to define how the reference impedance of the measurement Z_{ref} and the position of the reference plane are estimated, based on the available calibration standards. Table 2.1 exemplifies how reference impedance and reference planes are estimated for the four mentioned calibrations (SOLT, RSOL, TRL and LRM). It is in general suggested to employ calibration strategies in which the standards related to Z_{ref} and reference planes are more easily manufactured and modeled. This mostly depends on the application, on the measurement frequency and on the environment in which the measurements need to be performed. The final part of this chapter will be used to draw some guidelines for the choice of the calibration strategy to be used for on-wafer calibration, depending on frequency and application.

2.3. Planar Measurements

Test and measurement instrumentation for RF and microwave measurements, as in the case of the VNA, is generally designed to perform measurements on coaxial devices, i.e., devices which interface to the outer world through coaxial connectors. As a matter of fact, as can be seen also in Figure 2.4, VNA test-ports are always coaxial. In case of mm-wave extenders, which will be better discussed in Chapter 6, test-ports are instead realized with waveguide flanges, using a waveguide interface according to the specific extender bandwidth. On the other end, electronic devices and circuits are primarily realized on *planar* environments, i.e., on wafers realized using semiconductive materials. While it can be interesting to characterize devices after being packaged and properly connectorized, their performances in the native planar environment must be also measured, especially when model extraction and validation is required. This implies the need to *shift* the position of the instrument test port from coaxial (or waveguide) to planar. This interface transformation is typically obtained by using wafer-probes. Wafer probes provide the proper transition to convert the waves traveling in a coaxial (or waveguide section) into a planar field distribution, often in the ground-signal-ground (GSG) configuration. Examples of different commercially available probes are depicted in Figure 2.8a. The transition

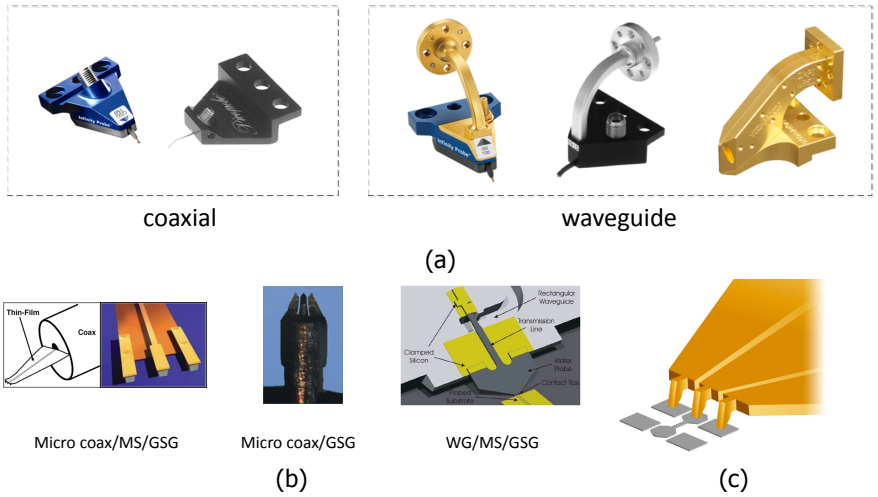


Figure 2.8: a) Examples of commercially available wafer probes for microwave and millimeter wave applications. b) Different approaches for probe tip realization, with microcoaxial to microstrip to GSG transition (left), direct microcoaxial to GSG transition (center) and waveguide to microstrip to GSG transition (right). c) 3D representation of a GSG probe landing on probe pads

from the test-port connector (coaxial or waveguide) to the GSG planar environment can be implemented in several ways, depending on the vendors and the application, as shown in Figure 2.8b. The final interconnection between the probe and the planar environment is achieved by physical contact between the probe tips and the *probe pads*. These landing structures, typically circular or rectangular, are realized using soft metals (gold or aluminum) to allow proper low-ohmic connection without damaging the probe tips (see, Figure 2.8c). While in *connectorized* measurements the uncertainty sources of calibration standards and of reference plane position have been accurately studied and identified, the planar measurements present additional challenges and lack of comparable traceability.

2.3.1. Calibration challenges in planar measurements

Calibration techniques for on-wafer measurements typically consist of a probe-level calibration performed on a low-loss substrate (i.e., alumina or fused silica) [30]. This probe-level calibration is then transferred to the environment where the DUT is embedded in and often, to increase the measurement accuracy, this calibration is augmented with a on-wafer calibration. This allows moving the reference plane as close as possible to the DUT, by de-embedding the parasitics associated to the contact pads and the device-access vias [31]. However, planar measurements present an un-shielded (from an electromagnetic stand point) transition from the instrumentation test port (i.e., the probe) to the DUT, and this allows for uncertainty in the definition of the calibration reference plane. The non-shielded nature of the transition results in a kind of ”distributed” interaction between the probe and the DUT: the transition cannot be placed at an exact reference plane (for example, at

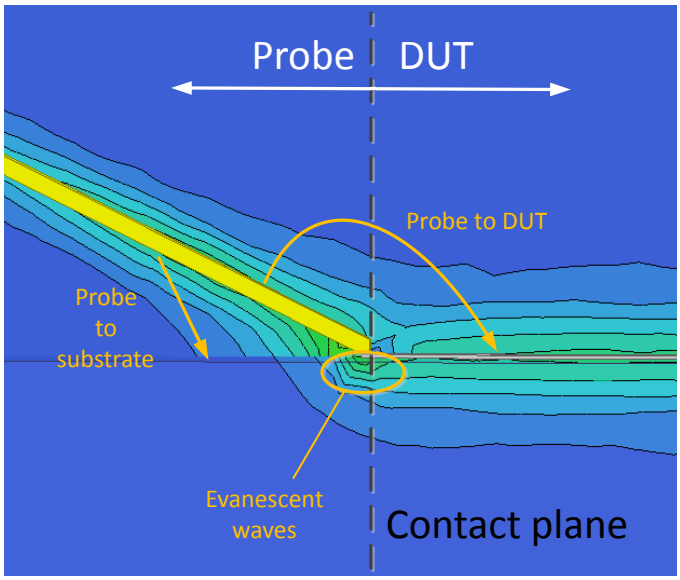


Figure 2.9: Electromagnetic simulation of a probe-to-pad transition, highlighting different coupling mechanism associated to the non-shielded nature of the transition

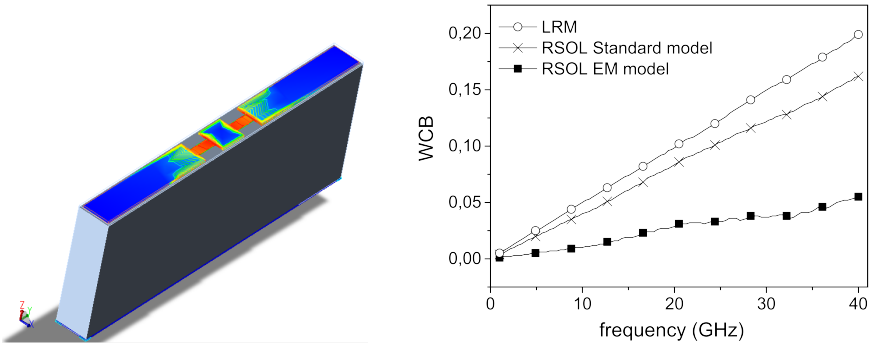
the contact point between the probe tip and the pads) because the probes inevitably interacts electromagnetically with the surroundings, i.e., with the substrate in which the DUT is embedded, the space surrounding the DUT, and the DUT itself through distributed electromagnetic coupling. Also, the abrupt transition from the tips to the pads is keen to excite evanescent, non propagating electromagnetic modes in the surroundings of the contact point, which contributes to making the reference plane not well-defined. The aforementioned effects can be better explained by visualizing the field distribution at the probe-to-pad transition, as done by means of electromagnetic simulations in Figure 2.9. For these reasons the calibration technique, as well as the environment in which the calibration is performed, are very sensitive choices and strongly depend on the application, the frequency range and the required accuracy.

2.3.2. On the definition of the reference planes in probe-level calibration

The standard modelling

Traditionally, calibration techniques requiring little standards knowledge (e.g., TRL, LRL, LRM) have been considered the most accurate, especially in combination with planar applications, mostly due to the challenges related to obtain a full and accurate pre- characterization of planar standards, like matched loads. Nevertheless, when moving to on-wafer environments and requiring a broad-band frequency range of the calibration, the usability of TRL is limited. As a matter of fact, TRL is limited in frequency by the insertion length of the line standard (i.e., the length of

the line in excess to the thru standard), which needs to be electrically shorter than 180 degrees in the whole measurement frequency range [29], so that a single-line calibration kit can never cover more than an 8:1 (frequency span - start frequency) bandwidth. For this reason, techniques featuring multiple lines have been developed to cover wider frequency bandwidths, like the multi-line TRL [32]. But a large number of lines can be impractical in case of on-wafer measurements, because of the conspicuous space occupation and the large required probe movements, due to the different lines lengths. More space efficient calibration procedures, such as the LRM [28], suffer from a simplified purely non-reactive model of the load in its original definition. Imposing partial or full knowledge of some standards allows to extract or incorporate a reactive behavior in the match load, as done in the LRRM [30] and LRM+ [33]. Nevertheless, as the TRL also the LRM technique sets the calibration reference plane in the middle of the (non-zero) coplanar thru line, thus requiring an accurate model of the thru to shift the reference plane back to the probe tips, as it would be required in case calibration is performed on an independent calibration substrate before being transferred to the targeted DUT wafer. It has been demonstrated that, when coupled with accurate standard models, the reciprocal SOL (RSOL) using an unknown thru [27] can provide accuracy levels comparable to those of the TRL technique [34, 35] directly setting the reference plane at the probe tips. Unfortunately, probe and calibration substrate manufacturers typically provide only purely reactive models of the calibration standards. In the past, this was mostly due to the required compatibility with old firmware analyzers, while modern analyzers allow full frequency dependent definition of calibration standards, also in the form of S-parameters. In contrast to this trend, in [34] accurate frequency dependent models were acquired employing a measurement procedure, thus requiring an accurate reference calibration to be performed. These models were then used for the calibration standards, achieving improved accuracy in the calibration. This technique still requires a reference calibration for the pre-characterization of the standards, which then shifts the problem of the residual errors to the accuracy of the reference calibration employed. If one wants to make the definition of the standards independent of any previous calibration, one solution could be the use of EM simulation for their modelling [14]. To make an example, in [14] the calibration standards from a commercially available Cascade Microtech ISS model 101-190C were simulated in order to realize a frequency dependent data-base model, in the form of S-parameters. For the simulation, the transverse and vertical dimensions of the standard were first measured using a Dektak 8 profilometer with a few nanometer of vertical resolution together with an optical analysis with a reference scale. Using these parameters, a model of each standard was realized using a 2.5D full-wave EM environment (i.e., Keysight Momentum), see Figure 2.10a. The standards were simulated by using lumped internal ports to mimic the configuration of a GSG probe, in the frequency range from 10 MHz to 40 GHz. Three different calibrations were performed: a RSOL calibration using the simulated standard models, a RSOL calibration realized using standard lumped models (provided by the manufacturer), and an LRM calibration realized on the same calibration kit. A unique set of raw data of the standards was employed to derive the error-terms of the three different



(a) (b)

Figure 2.10: a) 3D model of match load after Momentum simulation, indicating field intensity over the conductor and resistive layer surfaces. b) Worst case error bound representing the comparison of the three considered calibrations when measuring a 450 µm line. Simulation data of the line are used as reference.

calibrations, in order to guarantee consistency and exclude sources of error due to different probe placement among the calibrations. A raw measurement of a 450 µm line present on the same calibration substrate was used to compare the data obtained applying the three set of error terms mentioned above and compute a worst case error bound (WCB) using the method of [36], as:

$$WCB = max\left|S'_{ij} - S_{ij}\right| \tag{2.4}$$

Were S' represents the S-parameters of the verification DUT obtained using the chosen calibration, and S represents the reference value of the S-parameters of the verification DUT. In this case, the EM simulation of the 450 µm line was used as reference data. The error bound is shown in Figure 2.10b, showing how the EM-based RSOL outperforms both the RSOL calibration based on standard definition and the LRM calibration. The error improvement can be associated to a better accuracy of the standard definitions, as the errors related to probe misplacement and contact have been minimized, or at least made homogeneous for all the calibrations, by using the same set of raw data for the error computation.

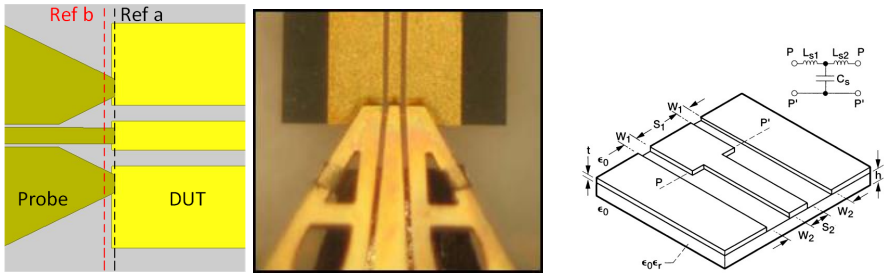
On the placement of the reference planes

For connectorized measurements, the sources of uncertainty related to calibration standards and reference planes have been accurately identified and modelled in literature, and the reader can refer to [37] for further information. For unconnectorized measurements, like in the case of planar measurement, the interface between system and DUT (including the calibration standard) makes things more complicated. If properly realized, calibration procedures like the TRL allow setting the calibration reference plane at the center of the transmission line employed as the thru standard, so that the reference planes are accurately placed far from the

probe-to-DUT transition. On the other end, when the calibration is performed on a "general" impedance substrate, and needs to be transferred to the environment where the DUT is embedded, a less rigorous process takes place. In this case, it would be not consistent to place the calibration reference plane at the center of the thru standard, as this plane would not be present in the final DUT measurement. It is necessary to have an unequivocally defined reference plane, which could be consistently transferred from the primary calibration to the DUT measurement. In case of TRL calibration, the reference plane can be translated back from the center of the thru to the probe tips, based on the knowledge of the propagation constant, and the length of the line [36]. This process is based on the assumption of pure TEM propagation in the considered line. This assumption can be easily violated in close proximity to the probe-tips, as the imperfect probe-to-pad transition (from the electromagnetic standpoint) allows for the presence of non-propagating EM modes, which would affect the accuracy of the reference plane translation. It would be preferable to have a calibration approach which non-ambiguously defines the calibration reference plane directly at the probe-tips, without the need of secondary plane translation. In this respect, RSOL calibration can come in handy. In this case (as well as SOLT) the reference plane is placed where the one-port standards (i.e., short, open and load) are defined, see Table 2.1 (NB, these standards needs to always be defined at the same reference plane). Using this reasoning, if the calibration standards could be defined directly at the probe tip, that would unequivocally define the reference planes. Unfortunately, the way the reference planes are defined for on-wafer calibration procedures presents some challenges. Up-to-date probe-level calibrations are performed using paired substrates and probe set, where the discontinuity caused by the transition (probe-to-line/pad) is entirely embedded in the standard definition, implicitly setting the reference at plane *b* in Figure 2.11a. This results in two effects:

- calibration substrates cannot be used on un-paired probes;
- measured data present offsets when compared to simulated data (which are often the benchmark value in all integrated technologies), since the imperfect probe-to-pad transition is not included in the simulation.

In order to shift the calibration reference plane from plane *b* to *a* (i.e., to the proper probe-to-line transition), it is necessary to embed (most of) the imperfection related to the transition into the error terms, therefore creating a standard definition which is independent of the employed probe. To better understand the problem, let's consider a generic probe-to-line transition, as shown in Figure 2.11b. The various probe types end with a tip providing a contact point in the order of 10-20 μm to easily contact pads and lines having a width of 50 μm. This width step, between the probe tip and the line/pad, can be modelled as a step change in the width of the signal line of a CPW, as shown in Figure 2.11c, from [38]. As can be seen from the inset in Figure 2.11c, this step discontinuity can be modelled, in a first order approximation, as a T-network with a shunt capacitor. In conventional probe-paired calibration kit definitions, this capacitance is removed (becoming of negative sign) and embedded in the standard definition, as can be seen from Table 2.2. By



(a) (b) (c)

Figure 2.11: a) Schematic top-view of a probe-to-line transition for a GSG connection. Line a (dashed black) and b (dashed red) define two possible positions for the calibration reference plane. b) Probe-to-line transition for a |Z| probe on a CPW transmission line. c) Equivalent model for a step change in signal line width for a CPW transmission line, as derived from [38]

Table 2.2: Standard definition for the Cascade Microtech ISS model 101-190C

ACP/ FPC	C-Open fF (on substrate)	C-Open fF (in air)	L-Short pH	L-Term pH	**Infinity**	C-Open fF (on substrate)	C-Open fF (in air)	L-Short pH	L-Term pH
GSG 100	3.5	-9.3	2.4	-3.5	GSG 100	3.6	-6.5	3.3	-0.4
GSG 125	3.5	-9.5	3.6	-2.6	GSG 125	3.6	-6.6	5.7	1.6

contrast, when the standards are defined using EM models, their definition becomes independent of the probe construction (a part from the probe-pitch, which is to be still taken into account during calibration) and the reference plane is directly placed at the probe-to-pad touchpoint. To validate this statement, a comparison was performed by using a Cascade Microtech ISS 101-190C as calibration substrate [39]. For this, probe-paired standard models are provided by the manufacturer, as reported in Table 2.2, for two probe types, ACP/FPC and Infinity, and different probe pitches. No model is instead provided for un-paired probes. For the same calibration kit, models were realized using EM simulations and measurements of the standards dimension as described in previous subsection, for the same probe-pitch dimensions. In order to compare the two different standard models, we considered two different set of probes with the same probe pitch, i.e., 100 µm. In particular, one set of Cascade Microtech Infinity i40 and one set of Cascade Microtech 40 GHz |Z| probes have been employed. Two calibration kits from the same ISS model 101-190C substrate have been considered, and on each one raw measurements of all the calibration standards have been performed with both sets of probes, in the frequency range from 1 GHz to 40 GHz, using a semi-automated probe-station to reduce errors related to probe misplacement. Afterwards, the raw data have been used to derive the error set for RSOL calibration, using the manufacturer provided standard definition for the Infinity, and EM derived standard models for both Infinity and |Z| probes, obtaining a total of six different error sets. All the data acquisition, generation of the calibration terms, and data correction was performed

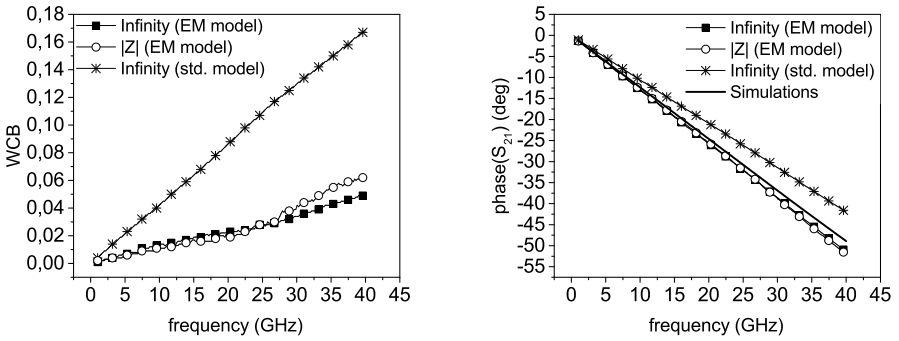


Figure 2.12: a)Worst case error bound defined by the two different sets of probes, employing EM derived calibration standard model for Infinity (full squares) and |Z| probes (empty circles) and the standard probe-paired model for the Infinity (stars) probes, when calibrating using a Cascade Microtech ISS 101-190C. Calibrations have been performed on two different calibration kits on the same substrate, and verified on four different lines. The WCB is computed using simulation data of the verification line as reference. b) Phase response of the 450 µm line, after calibration for different probe types, compared to the phase response obtained using EM simulations.

using Cascade Microetch Wincal XE ver. 4.5. Raw measurements of two 220 µm lines and two 450 µm lines, on the same calibration substrate, have been performed, and the six error sets mentioned above have been applied. In order to compare the different probe-tips calibrations, the method of [36] has been employed, using simulation data of the two verification lines as reference, and defining the worst case error bound (here referred as WCB) as in Equation (3.3). The results of the comparison, that was carried out in [15] are shown in Figure 2.12a. The comparison highlights how, when EM models for the calibration standards are employed (see, Figure 2.12a, full squares for Infinity, empty circles for |Z|), different probes provide similar values for the error bounds, making the calibration in principle insensitive of the probe type. Furthermore, when probe-paired standard definitions are employed (see, Figure 2.12a, star symbols), the resulting error bound is up to two times higher than the error associated to any EM model based calibration, irrespectively of the probe. Note that in this analysis the higher error bound is not to be interpreted as a worse calibration, but as a wrong association of the reference plane, when compared with a clearly defined plane in the simulation environment. This result can also be highlighted by comparing the phase response of the 450 µm line of the two different probes employing the EM models (see, Figure 2.12b, full squares for Infinity, empty circles for |Z|), showing an high agreement with the simulated data (see, Figure 2.12b, solid line), and the result using the probe dependent model provided by the manufacturer (see, Figure 2.12b, star symbols).

On the manufacturing of planar calibration standards

In the previous two subsections it has been shown how, with the aid of electro-magnetic simulations, it is possible to improve the accuracy of RSOL calibration by

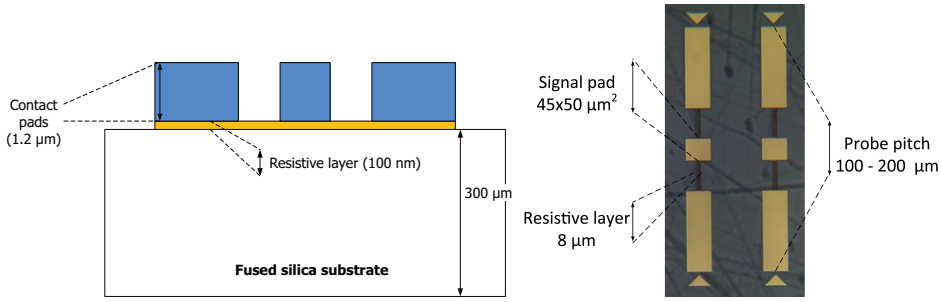


Figure 2.13: a) Schematic cross section of the 50 Ω resistors fabricated on the proposed fused silica substrate; b) Load standard artifact realized using the proposed technology.

providing a more physical model of the calibration standard, and defining unequivocally the reference plane of the calibration. One thing is still missing in this analysis, and is to study how the manufacturing of the standard can affect the accuracy of the model, hence the accuracy of the calibration. For RSOL (as well as for LRM calibration), the variation of the *load* performances, both in terms of DC resistance and electromagnetic behavior, constitute one of the biggest sources of uncertainty [14, 35]. As discussed in previous sections, in commercially available calibration kits, the load standard is typically defined by means of a purely inductive model. In this, while the DC resistance is very well controlled by means of laser trimming [39], the purely inductive model results to be inaccurate since the large capacitive loading provided by the contacting metal stripes is neglected. At the same time, the laser trimming procedure, while keeping the resistance value highly repeatable, poses a limit in the EM modeling of the load standard, since the geometrical modifications generated during the trimming procedure are not predictable. The only way to avoid laser trimming is to use a fabrication process that could allow very precise control of the geometrical properties (width/thickness) of the resistive layer. In this framework, a lithographic process like the one proposed in [14], featuring a layer thickness variation in the order of 1% across a single 2x2 cm^2 and horizontal accuracy in the order of parts of nanometer, can represent a good candidate for the manufacturing of a precision RSOL calibration substrate. Figure 2.13a shows a simplified schematic cross section of a calibration load manufactured in the proposed technology. The resistive layer with controlled thickness is first deposited, then patterned by means of lithography. The contact pads are then deposited on top of the resistive layers, in order to guarantee a good ohmic contact between the low resistivity material of the pad (aluminum) and the high resistivity material used for the resistance. For the other standards (short, open and thru) the same manufacturing process is used, with the low resistivity material always deposited on top of the high resistivity layer. Figure 2.13b shows one of the load artifact realized on the proposed technology. All the designed structures feature a 45x50 μm^2 signal pad, and a geometry which can allocate probe pitches in the range 100-200 µm. In order to create the models of the calibration standards, the same kind of EM simulation pro-

cedure as in Section 2.3.2 has been developed. For each calibration standard, the material properties and geometrical characteristics (width and length) have been defined as provided by the manufacturer. The resistive layer thickness value has been extracted by means of DC measurements, using the width, length and resistivity as constants. At the end of the procedure, a probe-pitch dependent model is extracted for this new calibration kit. Once the calibration kit is manufactured and properly modeled, the performances can be evaluated by means of comparison. In order to do that, measurements have been performed in the frequency range from 10 MHz to 50 GHz, employing a set of Cascade Microtech Infinity i50 probes with 125 µm pitch, using Cascade Microtech Wincal XE ver. 4.5 for the data acquisition and calibration computation. First a RSOL calibration has been performed by using the new calibration kit in combination with the model realized with EM simulations, and the error terms have been saved. Then another RSOL calibration has been conducted on a Cascade Microtech ISS model 101-190C, using manufacturer definitions for the standards. Finally, a unique set of raw measurements has been conducted on different DUTs: a set of different loads manufactured with the fused silica technology described in this section (0.35 Ω, 0.45 Ω, 41 Ω, 4500 Ω, 6800 Ω), two CPW lines realized on fused silica (726 µm, 1422 µm), a verification line from the ISS substrate (1800 µm) and a CPW line realized on SiGe BiCMOS 130 nm technology (600 µm). The two different calibrations have been then applied to each one of the raw measurements. In order to compare the performance of the calibration, the method of [36] has been employed, using simulation data as reference, and defining two different worst case error bounds for the transmission lines and for the loads:

$$WCB_{Line} = max\left|S_{ij,n}^{w} - S_{ij,n}^{Ref_w}\right| \tag{2.5}$$

$$WCB_{Load} = max\left|S_{ii,n}^{k} - S_{ii,n}^{Ref_k}\right| \tag{2.6}$$

Where S^{Ref} is the S-parameter associated to the reference data, with *k* associated to the load standards and *w* associated to the line standards, $S^{k}_{ij,n}$ is the *nth* s-parameter measured with $n \in [1,2]$ being the considered error set, and $i,j \in [1,2]$. The results of this comparison are two synthetic figures of merit, comprehensive of all the performed measurements, summarizing the error committed by employing a specific calibration technique, and are shown in Figure 2.14. When measuring transmission lines (see, Figure 2.14a, full squares for fused silica calibration, asterisks for ISS calibration), where the sources of error are dominated by the probe displacement on the transmission lines that are not accounted for by the simulations, both errors tend to increase with frequency. However, fused silica based calibration performs better than ISS in the entire frequency range, with an error 2,5 times smaller at 50 GHz. When the one-port measurements are considered, probe displacement error has very small impact on the calibration accuracy [14]. In this case, the error will be mainly determined by the accuracy of the standard definition. As shown in Figure 2.14b, while the error associated to the calibration on fused silica is approximately constant versus frequency, the error associated to the conventional ISS calibration is frequency dependent and always higher than the

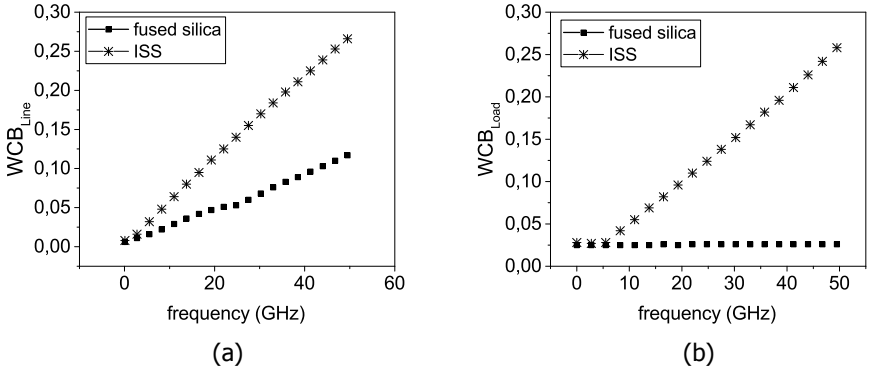


Figure 2.14: Worst case error bound for a) measurements of transmission line and b) measurements of one-port loads, obtained by using fused silica calibration (full squares) and ISS calibration (asterisks).

error resulting from measuring with the method proposed in this paper, with a discrepancy that can reach one order of magnitude at 50 GHz. Additional insight can be obtained by considering the impedences of the loads as measured with the two calibrations, as shown in Figure 2.15. To exemplify the problem, we focus on the measurements of a very low impedance load, featuring a DC resistance of 0.35 Ω (see, Figure 2.15, red curves) and a very high impedance load, with a DC resistance of 4500 Ω (see, Figure 2.15, black curves). For the real part of the impedance, both calibrations give results close to simulations (see, Figure 2.15a). However, when the imaginary part of the impedance is considered, the ISS calibration is only valid at very low frequencies, while it fails to predict the correct values as the frequency increases (see, Figure 2.15b). Particularly interesting is the measurement of the very high impedance load, where the ISS calibration shows a positive value for the imaginary part of the impedance, totally neglecting the mainly capacitive behavior of the DUT, which instead is accounted for by the fused silica calibration. This behavior can be easily associated to the inaccurate inductive model of the ISS load, as also described in [14].

2.4. Conclusions

Conventional microwave characterization of electronic devices is generally, at least in part, performed using vector network analyzers (VNAs). In this chapter, the general features and architectures of commercially available VNAs have been discussed. Then, the focus of the chapter has been moved towards the calibration of the VNA. In particular, special attention has been dedicated to planar measurements. When measurements are performed on-wafer (i.e., on planar environments) additional challenges are present due to the imperfect electromagnetic transition offered by the probe-to-pad connection, requiring dedicated calibration approaches to minimize the residual errors of the corrected measurements. At the end of this chapter, a set of guidelines has been shown to improve the accuracy of on-wafer calibration.

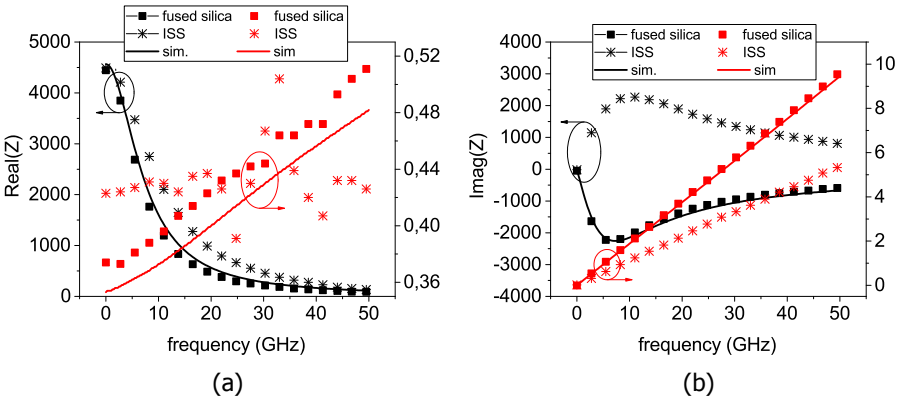


Figure 2.15: a) Real and b) Imaginary part of the impedance extracted from the measurements of a 4500 Ω (black curves and symbols) and a 0.35 Ω (red curves and symbols) obtained by using fused silica calibration (full squares) and ISS calibration (asterisks) as compared to simulations (solid lines).

First, a technique based on the EM modelling of calibration standards has been presented, allowing to include all the physical properties of the calibration standards in the modelling, in contrast with conventional modelling which is typically limited to simplified lumped models. Then, the same modelling techniques have been used to unequivocally define the calibration planes in planar measurement, by placing them exactly at the probe-tip contact point with the calibration standard. Finally, an implementation of a planar calibration kit has been shown, realized using low-impurity fused silica as substrate, and photolitographic techniques for the metalization. The proposed implementation allows for high repeatability of the calibration standards, especially of the load, in order to avoid laser trimming for the resistance definition. In the next chapters, the challenges related to millimeter-wave planar measurements will be discussed in details, and solutions for accuracy improvement will be presented.

3

Advanced (sub)mm-wave planar calibration

Chapter 2 has reviewed the concepts of planar calibration. As described, calibration algorithms are based on (partially) known devices (i.e., SOLT/SOLR/LRM) or employ distributed concepts (TLR and multi-line TRL). The accuracy of the calibration is directly dependent on the accuracy with which the standards are known. Traditionally, calibration techniques requiring little standards knowledge (e.g., TRL, LRL, LRM) have been considered the most accurate, with TRL reaching metrology institute precision, by only requiring the information of the characteristic impedance of the line [29]. In this chapter the focus will be placed only on TRL-based calibration techniques due to their best compatibility with (planar) millimeter and sub-millimeter wave characterization [40]. First, challenges and potential solutions associated with first-tier calibrations performed on a low-loss substrate will be analyzed, then the design flow for the realization of calibration kits integrated in the back-end-of-line of silicon based technologies will be discussed, focusing on the procedures required to correctly extract the characteristic impedance of the transmission lines. In this framework a novel, simulation based method for the accurate extraction of characteristic impedance will be proposed.

3.1. Probe-tip planar calibration

Probe-tips or first-tier off-wafer calibration are terms typically referred to the use of commercial impedance standard substrates (ISS) to define the reference planes of the measurement. These substrates are fabricated on low-loss, well characterized, dielectric materials (i.e., alumina, silicide or fused silica) to calibrate coplanar probe measurement setups, setting the calibration reference plane at the edge of the probe-tips. For this procedure, the most commonly employed material is alumina due to the well characterized material properties and the relative simplicity in manufacturing accurate calibration standards.

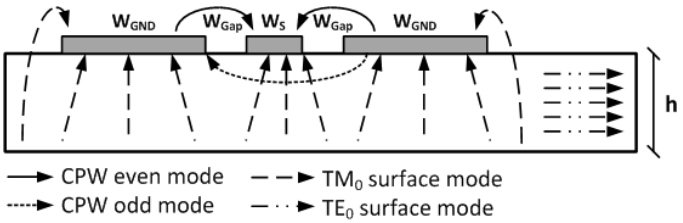


Figure 3.1: Cross section of a CPW with finite ground planes, and sketches of the E field distributions of the first propagating modes supported.

3.1.1. Multimode propagation in calibration standards

In association with the G-S-G nature of the probing pads (see, Section 2.3), transmission lines used for calibration purposes are typically coplanar waveguides (CPWs). Conventional calibration techniques are based on single mode propagation inside the transmission lines employed during the procedure. While this is automatically ensured in purely TEM propagating structures (i.e., coaxial), CPWs (as well as microstrips) may support multiple propagation modes. The different propagating modes supported by a CPW are qualitatively sketched in Figure 3.1. The CPW mode characterized by opposite direction of the fields across the slots, represents the intended propagation mode and is often referred to as *CPW differential mode* or *CPW even mode*. The CPW mode characterized by in-phase direction of the field across the slots represents an unwanted radiating mode and is often referred to as *CPW common mode* or *CPW odd mode*. The TM_n and TE_n modes are surface waves propagating along the grounded dielectric slab, their cut off frequencies are functions of the height and dielectric constant of the substrate [18]. Overall, the propagation of unwanted modes has two main effects on the (measurement of) a CPW line: an increase of the measured transmission line losses (i.e., $|S_{21}|$), due to the energy that is transferred to the unwanted modes and is not detected in the single-mode measurement process, and the generation of ripples on the transmission parameter (i.e., S_{21}) of the CPW. The ripples are the results of interference (constructive or destructive depending on the frequency) between the unwanted modes, reflected by discontinuities (i.e., dielectric constant changes), and the intended CPW mode. When considering a planar TRL calibration, at least two transmission lines are conventionally used, namely:

- The *thru* standard, implemented as a CPW with a physical length in the order of 200-400 μm, which defines the reference planes of the calibration at its center;
- The *line* standard, implemented as a CPW providing an insertion phase (in respect to the thru line) of 90° at the center of the calibration band.

In this section, the impact of multimode propagation on (TRL) calibration accuracy will be analyzed. The analysis presented is based on numerical 3D simulations, and has been also described in [41].

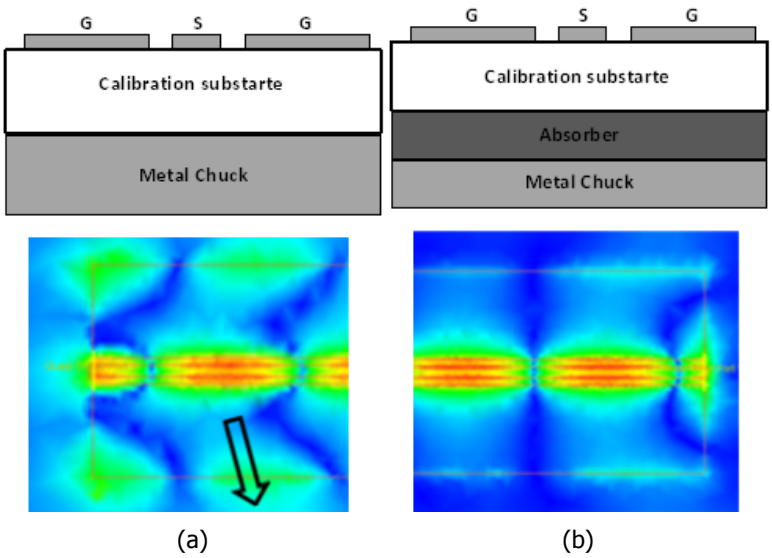


Figure 3.2: a) Cross section of CPW placed: on metal chuck, b) on absorber. Electrical field below the CPW metal plates for case: c) no absorber, d) with absorbing boundary conditions in the 3D FEM simulation, both fields computed at 110 GHz.

Parallel plate waveguide mode

During the calibration procedure, the substrate is typically directly placed over a metallic wafer chuck, creating effectively a grounded coplanar waveguide (GCPW) structure , as shown in Figure 3.2a. This structure supports, in addition to the modes shown in Figure 3.1, also a parallel plate waveguide (PPW) mode. This occurs since the top (ground planes of the CPW) and bottom (chuck) metals are not directly contacted, thus a different potential can exist and propagate along the structure. The PPW mode can be visualized in a 3D EM simulation by plotting the E field intensity below the metal surface. To reduce the PPW mode propagation, an interposed ferromagnetic substrate is conventionally used between the calibration substrate and the metal chuck. The ferromagnetic material "absorbs" the propagating PPW mode, due to the high losses presented to EM waves. Figure 3.2b shows the reduction of the PPW mode when simulating over the absorber structure.

Effects related to surface wave modes

The overall loss behavior of the CPW structure, including the surface waves, can be analyzed using the 3D simulation environment shown Figure 3.3a. A point voltage source with a source impedance of 50 Ohm is applied between the bridge and the CPW, to provide a discontinuity similar to a wafer probe. In the 3D simulation environment, the boundary conditions were set to absorbing, thus providing perfect match condition to all the unwanted modes within the structure. The extension of the substrate, and the air gap between the substrate and the simulation boundaries (sub and GAP in Figure 3.3a, respectively), are used as parameters for the

simulation, in order to mimick the effect of different position of the CPW line across a limited calibration substrate. Figure 3.3b compares the insertion loss of CPW structures realized in alumina when the substrate is enlarged and different air gaps (*GAP*) are applied between the substrate boundary and the radiation boundary of the box. The condition with no air gap (i.e., GAP = 0 μm) and no substrate extension (i.e., sub = 0 μm) can be considered an ideal case, in which all the energy generated by the unwonted modes is absorbed by the radiation boundaries of the simulation, so that no reflection happens. The simulation result for this situation is shown in Figure 3.3b, triangle symbols. When the air gap is applied, multiple reflections of the unwanted modes occur within the structure, generating an interference pattern (dependent on the distance to the discontinuity) along the trace, as can be seen by the shift of minima and maxima points when the *sub* parameter is changed (Figure 3.3b, cross and x symbols). The simulation does not include conductive or dielectric losses, thus the reduction in $|S_{21}|$ shown in Figure 3.3b can only be attributed to energy dissipated in the other modes supported by the structure. Based on the simulation results we can expect that, when considering real structures on alumina substrate, the lines closer to the edge of the calibration substrate will exhibit a stronger ripple caused by interference with the surface wave mode. In Figure 3.3c measurement results are shown related to structures with different distance to the substrate edge (i.e., placed at the center and at the N-W edge) for the alumina substrate. As can be seen in the figure, the structures at the edge of the substrate exhibit a clear interference pattern, as predicted by the simulation analysis.

Suppressing multimode-propagation by employing electrically thin substrates

In order to investigate the problem of multi-mode propagation in CPW lines, it is convenient to make some initial assumption. Considering only surface modes, it is possible to assume they are only weakly dependent on the width of the line and the dimension of the gap (W_S and W_{Gap} in Figure 3.1). If those dependencies are neglected, we can approximate the surface waves supported by a CPW as equivalent to the surface waves supported by a grounded dielectric slab. In this case, the cutoff frequencies of the surface modes only depend upon the substrate thickness h and the substrate material, characterized by its dielectric coefficient ϵ_r and, as shown in [18], are set by :

$$TM_n : f_c = \frac{n \cdot c}{2 \cdot h \cdot \sqrt{\epsilon_r - 1}} \tag{3.1}$$

$$TE_n : f_c = \frac{(2 \cdot n - 1) \cdot c}{4 \cdot h \cdot \sqrt{\epsilon_r - 1}} \tag{3.2}$$

Where n is the mode order, and h is the substrate thickness. Equations (3.1) and (3.2) show that employing lower ε_r substrates shifts the occurrence of the TM_1 and TE_1 modes to higher frequencies. Also, reducing ε_r allows employing a smaller gap dimension for a given signal width, to obtain the same characteristic impedance, reducing the amount of energy radiated by the CPW common mode [42]. For these

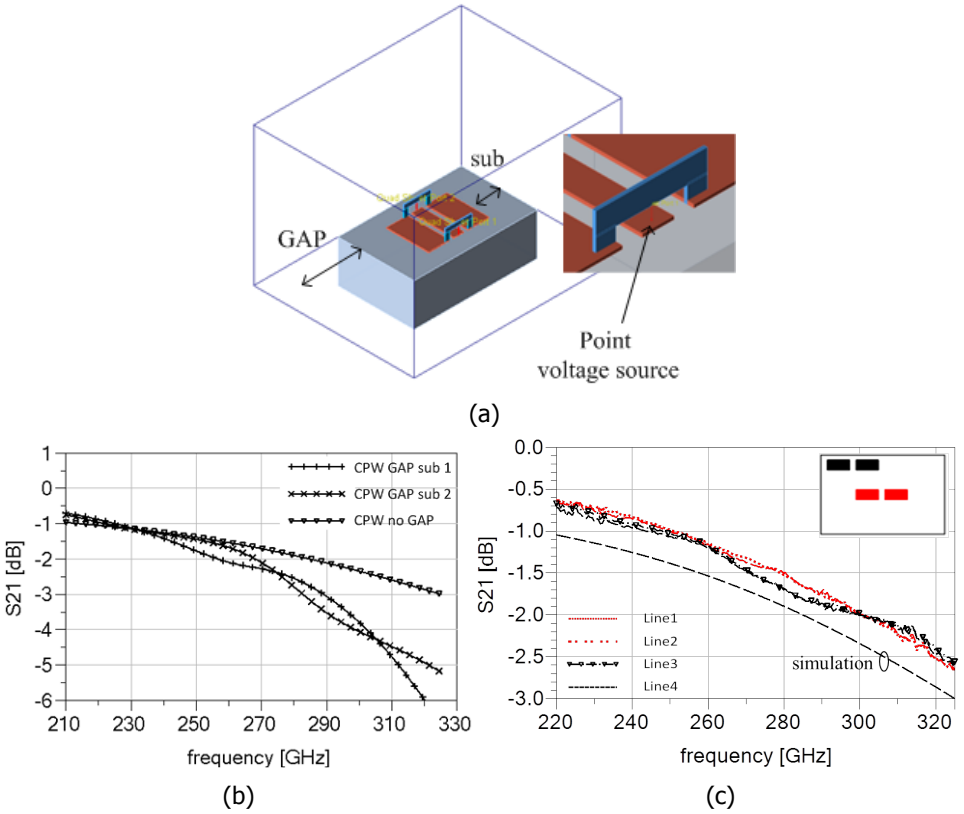


Figure 3.3: a) 3D model for the EM simulation of a CPW on alumina substrate, showing the parametrized quantities (GAP and sub) and the position of the stimulus. b) Simulated S_{21} of CPW on alumina substrate for various cases: CPW no GAP sub=0 µm GAP=0 µm, CPW GAP sub1 sub=320 µm GAP=500 µm, CPW GAP sub2 sub=420 µm GAP=500 µm; c) measurement of different (four) thru lines on alumina substrate in different location of the calibration substrate. Locations (i.e., two middle and two center) identified in the inset on top right.

reasons fused silica (ε_r = *3.7*) can be considered as a better candidate to integrate CPWs to perform TRL calibration in the (sub)mm-wave bands, as compared to alumina (ε_r = *9.9*). The same simulation analysis performed for the alumina case in Figure 3.3b was carried out for the fused silica substrate, see Figure 3.4a. As can be seen by the plot, a considerably lower amount of energy is transferred to other modes. Moreover the lower dielectric constant of the substrate provides lower discontinuities when terminated with air, showing close to no-variation when performing a simulation varying the dimension of the parameters *sub* and *GAP* as shown in Figure 3.4a. The measured results are then compared with the simulation showing a very good agreement in WR3 band, as shown in Figure 3.4b, confirming also the low loss achieved by the CPW realized on fused silica. Please note that the small deviations between measurement and simulation in Figure 3.4b in

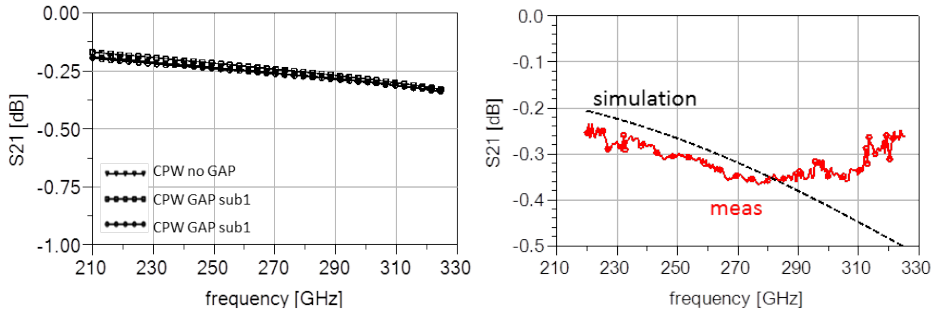


Figure 3.4: a) Simulated S_{21} of CPW on fused silica substrate for various cases: sub = 0 µm GAP = 0 µm (CPW no GAP), sub = 320 µm GAP = 500 µm (CPW GAP sub1), sub = 420 µm GAP = 500 µm (CPW GAP sub2); b) measurement of a thru lines on fused silica substrate.

the upper side of the bandwidth (maximum deviation in the order of 0.2 dB at 325 GHz) might be mostly attributed to the decreased dynamic range (due to decreased available power and increased losses) at the edge of the WR-3 setup employed for the measurements.

3.1.2. Calibration transfer

In the previous section the usage of electrically thin substrates (i.e., fused silica) was introduced to overcome the limitations exhibited by commercially available calibration devices operating in the mm-wave bands. While using such substrates improves the calibration quality, measurement accuracy will also depend on the error introduced by *transferring* the calibration to the environment where the DUT is embedded. It is often the case that the DUT is embedded in a different host medium compared to the calibration, i.e., Si, SiO_2, $GaAs$ or other substrate materials. When the measurement is performed on the new host medium, a different probe to substrate interaction will occur, which would not be corrected for by the calibration. This will introduce a residual error that would be a function of the difference in permittivity between the two substrate materials (i.e., calibration and measurement).

Error box model

When performing S-parameter measurements with the use of a VNA, the measurement can be schematized as in Figure 3.5a, where a two port DUT is embedded between two unknown two-port boxes A and B, called error boxes (i.e., using an 8 error term notation, see Section 2.2). Let us consider, for reason of simplicity, the input and output error box equal and only related to the wafer probe tips. We can then schematize the chain of probes and DUT as in Figure 3.5b. When a calibration is performed, the *P* matrix representing the probe tips is computed and can be removed from the measurements by proper de-embedding (i.e., multiplying the cascade of the probes and the DUT with the inverse of the *P* matrix at the input, and

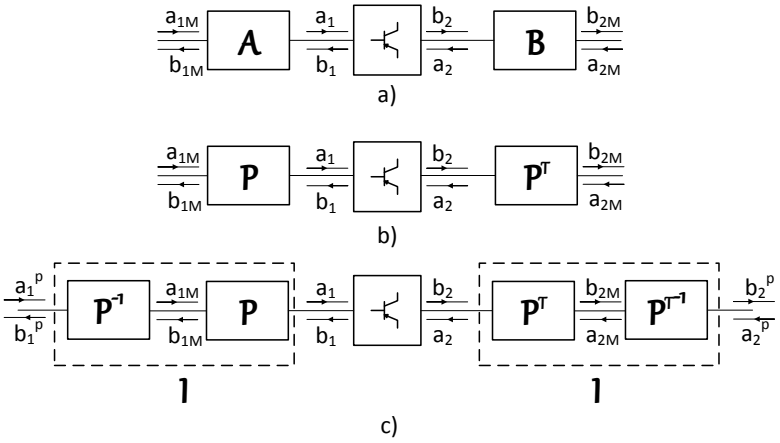


Figure 3.5: Cascade model of systematic errors in VNA. a) General error box model; b) Error model considering probe tips only, where *P* represents the transmission terms for the probe tips; c) Schematic representation of the de-embedding of the probes, where the *P* matrix is evaluated during the calibration procedure and then corrected.

the inverse of *P* transposed at the output). The matrix resulting from the product of *P* (or P^T) for its inverse is an identity, thus the calibration process allows perfectly correcting for the errors introduced by the wafer probes (see, Figure 3.5c). When the measurement is performed on a different substrate, in respect to the calibration substrate, the error box associated to the probe tips will change, as the transition from the probe tips to the landing pads is changed, resulting in a new box P_1, as shown in Figure 3.6a. In a first order approximation, the calibration transfer effect, associated to the change in the error box, can be seen as a capacitive coupling between the probe tip and the substrate, as presented in [43] and schematized in Figure 3.6b and Figure 3.7a. When applying the calibration to the measurements with the same procedure as shown in Figure 3.5c (i.e., applying the inverse of *P* or P^T), the presence of the shunt admittance prevents the cancellation of the matrix *P* with its inverse. The cascade of *P*, *Y* and P^{-1} constitutes now a new (residual) systematic error which can be represented with the Σ error box (see, Figure 3.6c). This residual error can be associated to the process of transferring the calibration from one substrate to another. The magnitude of the residual error will be dependent on the value of the admittance *Y*, thus on the difference in the dielectric coefficient between the calibration and the DUT substrate.

Error evaluation and minimization

3D electromagnetic simulators and circuit simulators can be used to study the effect of calibration transfer on probe tips. In order to do that, first a 3D model of a microstrip GSG wafer probe has to be developed. The model only includes the probe tip, which features a 200 µm long microstrip on a 25 µm thick alumina membrane, with a GSG termination and 35 µm high terminal pins. The probe tip has been designed to be matched to 50 ohm, and a front view particular of the model

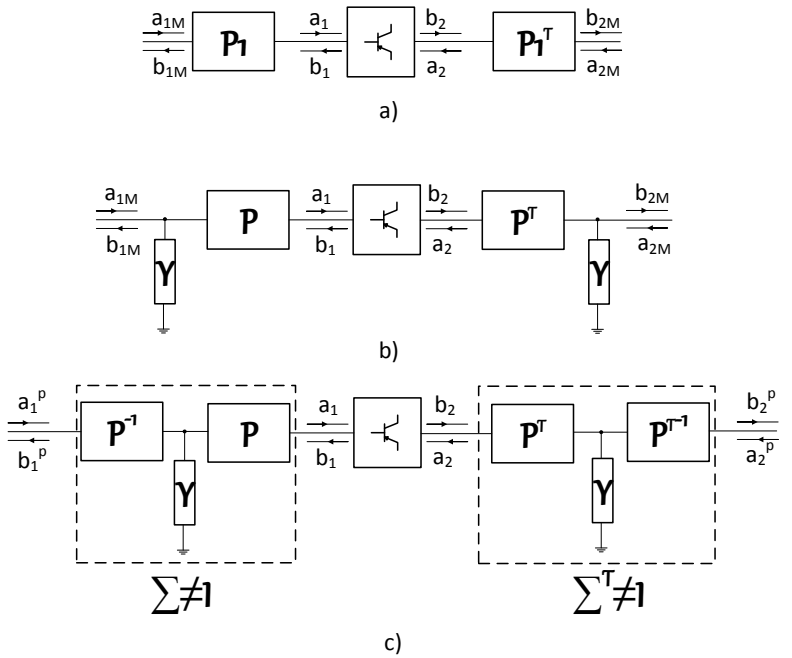


Figure 3.6: Cascade model of systematic errors including the effect of calibration transfer. a) General model in which the errors associated to the probe tips vary in respect to the calibration substrate, resulting in a P_1 error box. b) Modeling of the calibration transfer effect as shunt admittance. c) Schematic representation of probe de-embedding. The shunt admittance doesn't allow the cancelation of the probe terms, generating a residual error box *Σ*.

is visible in Figure 3.7b. The probe tip model was employed in 3D simulations in order to perform, with numerical data, a full TRL calibration on different substrates. Three different carrier materials have been employed: alumina (ε_r=9.6), fused silica (ε_r=3.78) and a BiCMOS SiGe back-end-of-line (ε_r=4.1). All the calibration standards (thru – short – line) have been simulated with the probe tips in the frequency range from 75 GHz to 110 GHz, and no probe misplacement was considered. An additional 600 µm long line was simulated in the SiGe BEOL as verification DUT. Simulations of the 3D models have been performed using Ansoft HFSS. These data have been used to perform the TRL correction procedure in Keysight ADS environment, in order to correct for the errors introduced by the probe tips. Finally, the three corrections have been applied to the verification line on SiGe BEOL. The "corrected" S-parameters of the SiGe line, using the calibration on BiCMOS SiGe BEOL, have then been used as the reference for the benchmark. In order to compare the three different correction implementations, the method of [36] has been employed, like in Section 2.3.2, defining the error as:

$$WCB = max\left|S'_{ij} - S_{ij}\right| \tag{3.3}$$

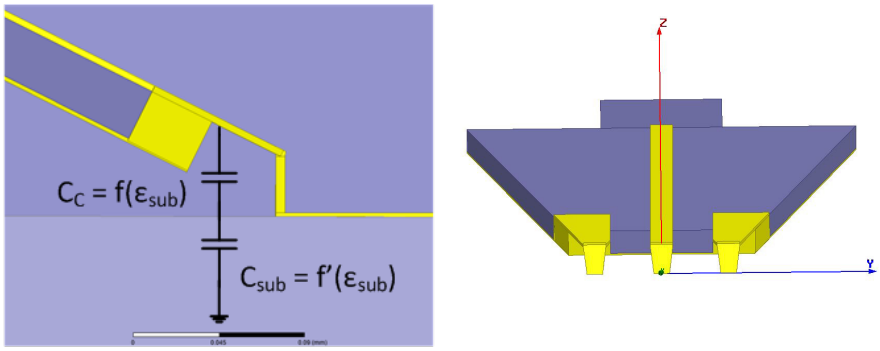


Figure 3.7: a) Schematic representation of the coupling between the probe tip and the DUT through the substrate as a capacitance. b) Front view of HFSS model of the microstrip GSG probe employed in the simulation.

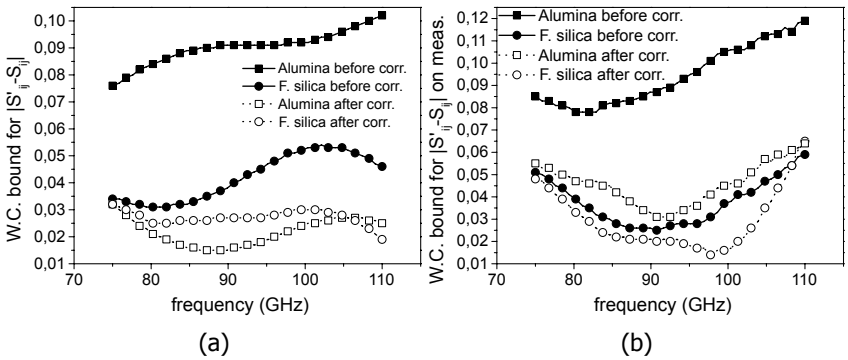


Figure 3.8: Worst case error bound for calibration transfer from fused silica and alumina to SiGe BEOL in the frequency range from 75 to 110 GHz, before correction (full symbols, solid lines) and after correction (empty symbols and dotted lines). a) simulation and b) measurement data.

Where S' is the s-matrix associated to the reference correction (in our case, the SiGe BEOL calibration) while S is referred to the target calibration (on alumina or fused silica) and $i,j \in [1,2]$. The results of this comparison are shown in Figure 3.8a, where the error is plotted towards frequency for both substrates (full symbols and solid lines). It can be noticed how the error due to transfer from alumina, with a maximum value of 0.1 (in magnitude) in the frequency range, is higher than the error obtained when the correction is transferred from fused silica, which is lower than 0.055 in the entire band. This can be related to the proximity of the dielectric constant of fused silica to that of the SiGe BEOL when compared to alumina.

In order to remove the error due to calibration transfer, we employ the procedure described in Figure 3.9:

- a shunt capacitance is introduced in the Keysight ADS environment at the

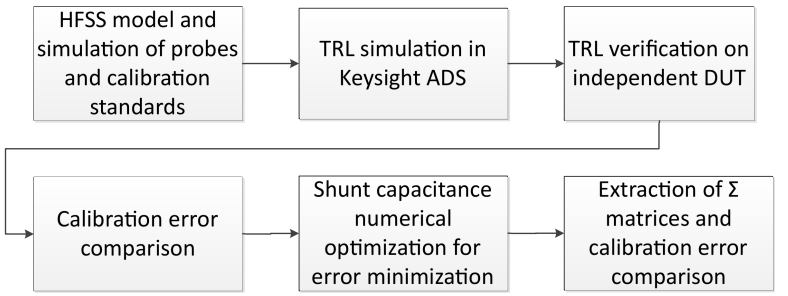


Figure 3.9: Error quantification and minimization procedure

input of the probe tips when simulating the SiGe BEOL verification line,

- a numerical optimizer is employed in Keysight ADS to minimize across the frequency band the error associated to the calibration on alumina and fused silica, by finding the optimized value of the shunt capacitance;
- when the capacitance is found the Σ matrices are generated for both substrates and a second de-embedding process (i.e., after the TRL calibration) is applied to remove the residual error for both substrates.

The results (see, Figure 3.8a) show that a correction capacitance of 0.94 fF for the fused silica calibration and 2.01 fF for the alumina allow a reduction of the maximum error in the entire considered frequency range in the order of 35% and 65%, respectively. As expected, being the correction capacitance a result of the field coupled from the unshielded transition to the substrate, its value is larger for the larger $\Delta\varepsilon$ case, i.e., alumina.

The residual error after Σ correction can be ascribed to the simplified capacitive effect. This optimization technique was benchmarked in a practical situation, similar to the one modeled in simulation. In an experiment, Cascade Microtech Infinity i110 probes with 100 µm pitch were used, which are similar in the construction principle to the ones modelled in Figure 3.7b. With these probes three different TRL calibrations were performed:

- one on a commercial ISS alumina substrate;
- one on a fused silica based calibration substrate;
- one on a calibration kit manufactured on IHP SiGe 130-nm BiCMOS technology BEOL.

The three calibrations have been used to measure the same artifact realized on the BiCMOS BEOL, a 600 µm long CPW line. The comparison between the three calibrations has been performed by means of Equation (3.3), using the BiCMOS calibration as reference. Figure 3.8b shows the results, in terms of worst case error bound, for the calibration comparison before any optimization is applied (full symbols and solid lines). Also in this case a higher error, in the entire frequency range, can be

highlighted for the TRL calibration performed on alumina in respect to fused silica substrate. Since the S-parameters at the input of the probe tips are not accessible, in order to extract the Σ matrices, the P matrix was extracted employing simulation data for the probe tips, while the values of the shunt capacitances have been tuned in order to minimize the error for the calibration on alumina and fused silica, respectively. The results obtained after the application of the correction are showcased in Figure 3.8b (empty symbols, dotted lines), where the maximum value for the error associated to the calibration of alumina decreased from 0.12 to 0.06, and an improvement is noticeable in the entire bandwidth. However, as in simulation, a reduced improvement compared to the alumina case is obtained for the fused silica, where the error associated to the difference in substrate coupling due to calibration transfer is small due to the similarity of permittivity between the fused silica and the silicon dioxide present in the back-end-of-line of the process.

This study shows how the calibration accuracy depends on the difference in permittivity between the calibration and the DUT substrates, resulting in higher residual errors when calibration transfer is performed among materials with bigger dielectric dissimilarity. Improvements are possible using the proposed optimization approach if EM models of the probes are available.

3.2. Direct on-silicon calibration

To totally remove the errors arising from the process of calibration transfer, it would be suggestible for the calibration kit to be directly implemented in the same environment of the DUT. Due to the objective difficulty, especially at higher frequencies, in manufacturing an accurate and predictable resistor in a commercial silicon technology, (multiline)-TRL calibration represents the standard employed technique. TRL does not require resistors to define the measurement normalization impedance, which is instead set by the characteristic impedance of the lines used during the calibration. Thus, the accurate (frequency dependent) determination of the calibration lines characteristic impedance becomes a key requirement to allow the correct re-normalization of TRL-calibrated S-parameter measurements.

3.2.1. Measurement based methods for characteristic impedance extraction of transmission lines

When transmission lines are fabricated over well-characterized homogenous materials and both radiation losses and surface waves can be neglected (i.e., at lower mm-wave frequencies) the line characteristic impedance can be derived by means of quasi static approaches, typically based on conformal mapping [44, 45]. When the structure geometry and the host substrate become more complex (i.e., silicon integrated grounded CPW), these approaches become less accurate. To overcome these limitations, various techniques have been developed to experimentally determine the characteristic impedance of these lines [46–52].

The Eisenstadt method

One of the simplest and most widely used methods for the computation of Z_0 of transmission lines is based on the direct measurement of the line's S-parameters,

and was introduced in [46]. The approach behind the technique is rather simple. If we consider the ABCD matrix of an homogeneous, generally lossy, transmission line, with an arbitrary characteristic impedance Z_0, this can be represented as:

$$\mathbf{ABCD} = \begin{bmatrix} cosh\gamma l & Z_0 sinh\gamma l \\ \frac{sinh\gamma l}{Z_0} & cosh\gamma l \end{bmatrix} \tag{3.4}$$

If the S-parameters of the transmission line are measured, in a measurement system with reference impedance Z_{sys}, it is always possible to transform the S-parameters in ABCD parameters with:

$$\begin{aligned} A &= \frac{(1 + S_{11} - S_{22} - \Delta S\ )}{2S_{21}} \\ B &= \frac{(1 + S_{11} + S_{22} + \Delta S\ )\, Z_0}{2S_{21}} \\ C &= \frac{(1 - S_{11} - S_{22} + \Delta S\ )}{2S_{21} Z_0} \\ D &= \frac{(1 - S_{11} + S_{22} - \Delta S\ )}{2S_{21}} \\ \Delta S &= S_{11}S_{22} - S_{21}S_{12} \end{aligned} \tag{3.5}$$

Combining Equation (3.4) and Equation (3.5) it is possible to obtain:

$$Z_0 = Z_{sys} \cdot \sqrt{\frac{\left(1 + S_{11}^2\right) - S_{21}^2}{\left(1 - S_{11}^2\right) - S_{21}^2}} \tag{3.6}$$

Equation (3.6) is derived equating the scattering parameters of the measured line to that of the model of a generally un-matched and lossy transmission line section. For this reason, Equation (3.6) is only applicable when measuring uniform lines, and the line is described by means of a single and unequivocal set of characteristic impedance and propagation constant. In this perspective, the presence of any input/output fixtures, as well as non-ideal probe-to-pad transitions and contact-pad capacitances, would provoke an error in the computation of the characteristic impedance. Moreover, the equation provides a discontinuity at half wavelength, as better described in [49], where an approach based on residuals shows the divergence of Equation (3.6) when the electrical length of the line approaches 90 degrees. All the aforementioned considerations make the expression in Equation (3.6) only an estimate of the characteristic impedance of the line.

Methods based on the knowledge of the propagation constant

The method proposed in [47] allows the extraction of the characteristic impedance from the propagation constant measured during the TRL calibration, and an estimate of the capacitance per unit length of the line. This method is based on the fact that, for a general transmission line, the capacitance per unit length *C*, the inductance per unit length *L*, the resistance per unit length *R* and the conductance

per unit length *G* can be related to the characteristic impedance Z_0 and propagation constant γ by means of:

$$\frac{\gamma}{Z_0} = j\omega C + G \tag{3.7}$$

$$\gamma \cdot Z_0 = j\omega L + R \tag{3.8}$$

The *RLCG* parameters are typically unknown. However, assuming low conductive losses in the substrate ($G \ll \omega C$) and the capacitance per unit length as approximated by its DC value C_0, then Equation (3.7) simplifies into:

$$\frac{\gamma}{Z_c} = j\omega C_0 \tag{3.9}$$

where Z_c is an estimate of the characteristic impedance Z_0 in the aforementioned assumptions. In this condition, Z_c can be estimated as far as the values of the propagation constant and the DC capacitance per unit length are available. Concerning the propagation constant, this can be obtained as a by-product of the TRL calibration, and directly computed during the procedure without any additional step [29]. Diverse approaches exist for the estimation of the capacitance per unit length [47, 50].

In [47] the estimate of the capacitance per unit length is obtained from the dc-resistance and the knowledge of the length of the line. This approach often leads to large inaccuracies, due to contact repeatability, when considering silicon technologies with aluminum pads. Also in [50] an estimate of the capacitance per unit length of the line is computed from the reflection coefficient of a small resistive load, in the assumption that the load is real, constant and equal to its dc resistance, conditions very difficult to reproduce in complex technologies, as the frequency increases. This approach is strongly limited by its assumptions to low loss substrates and simple geometries. As a matter of fact, the approximation made when assuming the capacitance per unit length as equal to it's DC-value assumes low loss substrates, weak transverse currents in the conductors and constant value versus frequency, assumptions often violated at very high frequencies and when employing lossy substrates. To overcome these problems, in [52] a new method is proposed, where the capacitance per unit length has been computed by means of conformal mapping. In this case, the computation of the DC-capacitance has been done by only considering the *in-vacuo* capacitance of a CPW realized on a $LiNbO_3$, using a dedicated numerical conformal mapping extraction, based on Schwarz-Christoffel technique, instead of conventional elliptic-integral based extraction. This technique has shown accurate extraction up to 40 GHz for the case of a CPW on a single-crystal dielectric substrate.

The "Calibration comparison" method

The above mentioned problems were overcome in the calibration comparison method for Z0 extraction proposed in [49, 50]. As the name suggests, the calibration comparison method is a technique originally formulated to allow the comparison between any two calibration techniques. The procedure typically begins by calibrating the VNA with a benchmark calibration *B*. Then, using the benchmark calibration as

reference, a second calibration *C* is performed. If a DUT is measured using each calibration, the cascade matrix *T* of such device can be described as:

$$T \approx T_B = X_C \cdot T_C \cdot W_C^T \tag{3.10}$$

where T_B in Equation (3.10) is the cascade matrix associated to the benchmark calibration *B*, T_C is the cascade matrix of the DUT measured with calibration *C*, and X_C - W_C are error box matrices describing the difference between calibration *C* and the benchmark calibration. If we assume that the two calibrations have the same reference plane, for example the probe tips, the matrices X_C - W_C can be seen as a simple impedance transformation between the two calibrations. Considering X_C:

$$X_C = \frac{1}{\sqrt{1-\Gamma_C^2}} \cdot \begin{bmatrix} 1 & \Gamma_C \\ \Gamma_C & 1 \end{bmatrix} \tag{3.11}$$

$$\Gamma_C = \frac{Z_B - Z_C}{Z_B + Z_C} \tag{3.12}$$

where Γ_C is an impedance transformer, Z_B and Z_C are the characteristic impedances of calibration *B* and *C*, respectively. A similar formulation can be performed for matrix W_C. Solving Equation (3.11) for Γ_C brings:

$$\Gamma_C = \sqrt{\frac{X_{C11} \cdot X_{C22} - 1}{X_{C11} \cdot X_{C22}}} = \sqrt{\frac{X_{C21} \cdot X_{C12}}{1 + X_{C21} \cdot X_{C12}}} \tag{3.13}$$

If calibration *B* has a well known characteristic impedance, then Equation (3.13) and Equation (3.12) allow defining the reference impedance of calibration *C*. However, if calibration *C* is a (multiline)TRL calibration realized using uniform transmission lines (i.e., with no pads and complex pad-to-line transitions) then the calibration reference impedance extracted using Equation (3.13) and Equation (3.12) is exactly equal to the characteristic impedance Z_0 of the line(s) employed for the calibration *C*. In this respect, the calibration comparison method constitutes a method for measuring the characteristic impedance of transmission lines used for (multiline)TRL calibration. The aforementioned procedure, proposed in [47], doesn't account for any shunt capacitance at the input/output of the transmission lines. However, large shunt capacitances may be present when employing conventional contact pads for wafer probing. Also, shunt capacitance can always be associated to the coupling between the wafer probe and the surroundings, if not properly corrected during calibration (see, Section 3.1).

In [51] the calibration comparison method was improved by using a lumped model to describe the probe to line transition, making the calibration comparison also insensitive to large shunt capacitances. In particular, in the formulation of [51], the calibration comparison method accounts for a discontinuity in the transition from contact pads to line, which can be modeled as a shunt admittance (Y) with a capacitive susceptance, representing the contact pad, and an impedance transformer, as shown in Figure 3.10. In this case, Equation (3.11) transforms into:

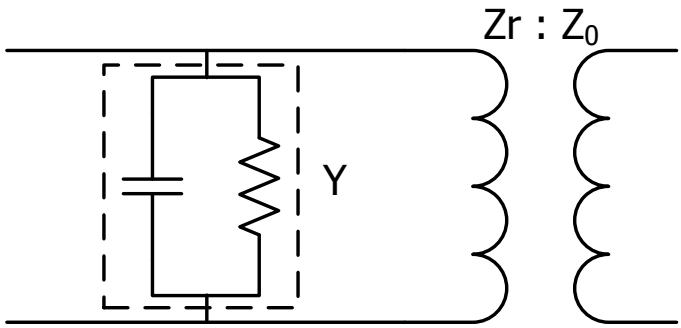
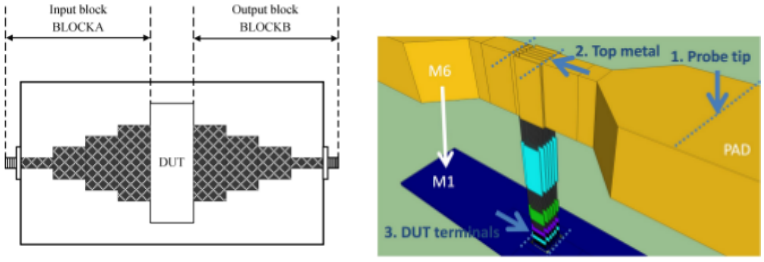


Figure 3.10: Equivalent circuit model for the pad to line transition as employed in [51]



(a) (b)

Figure 3.11: a) Test fixture for high power transistor characterization taken from [54], b) zoom in of the vias interconnection for a commercial SiGe technology modeled in a 3D EM environment, taken from [55].

$$X_C = \frac{1}{\sqrt{1-\Gamma_C^2}} \cdot \begin{bmatrix} 1 & \Gamma_C \\ \Gamma_C & 1 \end{bmatrix} + \frac{Y \cdot Z_r}{2} \cdot \begin{bmatrix} -1 & -1 \\ 1 & 1 \end{bmatrix} \tag{3.14}$$

Using proper manipulation, Equation (3.14) leads to an alternative estimate of the characteristic impedance, defining the impedance transformer Γ as:

$$\Gamma_C = \sqrt{\frac{(X_{C21} + X_{C12})^2}{4 + (X_{C21} + X_{C12})^2}} \tag{3.15}$$

and, by means of Equation (3.12), Z_0 can be computed also when large shunt capacitances are present.

The method of [51] loses accuracy when a series inductance or in general a non-lumped transformation is present between the shunt admittance Y and the impedance transformer. These situations can occur when an inductive pad to line transition is considered, as described in [53], or when the TRL kit is embedded in a more complex fixture where impedance tapers (see, Figure 3.11a) or complex vias interconnects are employed (see, Figure 3.11b).

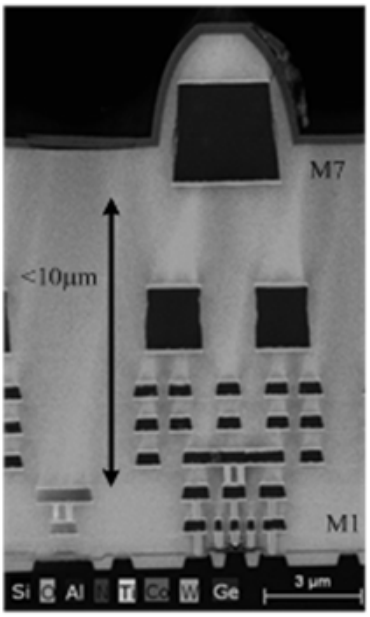


Figure 3.12: TEM image of the BEOL of the IHP SG13G2 130 nm SiGe BiCMOS technology.

When considering a commercial integrated technology BEOL, see Figure 3.12, the maximum distance between the signal (i.e., top metal line) and the ground (i.e., meshed M1 and M2) line of a micro-strip of a CPWG is usually limited to 10 µm. This technology restriction translates to the requirement of having narrow line widths in the fixture embedding the DUT, to achieve inductive line sections and characteristic impedances comparable with the measurement system impedance [56]. The resulting step change (from pad to line) in the width of the coplanar line connecting the DUT can be modeled as a series reactance and can be placed at the plane of the line discontinuity [38]. To make an example of how the error arising from the presence of a series reactance propagates on the extraction of the characteristic impedance using the method of [51], we applied the calibration comparison method to a set of CPW lines, presenting a varying step in the pad-to-line width, using the Keysight ADS simulation environment. The step discontinuity was computed using the model proposed in [38]. The probe pad is considered as a square pad with a 50 x 50 μm^2 area, and is included in the model using a shunt capacitance (simple parallel plate capacitance computation) of 18 fF, as shown in Figure 3.13a, while the line section is varied from a width of 7.5 µm (W of Figure 3.13a) to the size of the pad (i.e., no discontinuity). The parametrized (in width) line section is included in the simulation using the analytical model for the coplanar waveguide available in ADS, based on conformal mapping. All the lines use the same (lossless) substrate model (i.e., ADS CPWSUB) employing the values as used in [38], with a substrate thickness of 350 µm and a dielectric constant ε_r = 12.9. The set of lines was simulated using a reference impedance of 50 Ω and the TRL equations applied

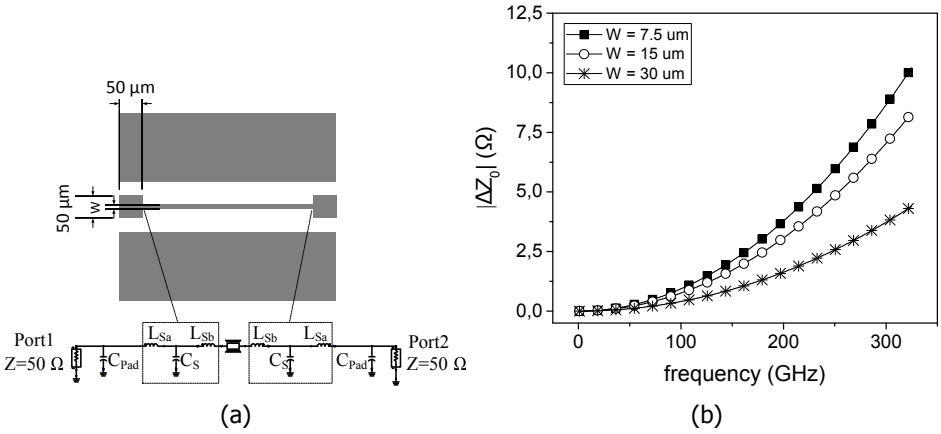


Figure 3.13: a) CPW line used for calibration comparison simulation with ε_r = 12.9, substrate thickness 350 µm and fixed ground distance equal to 150 µm. Top: Layout thru, with dimensions; bottom: simulation setup for the thru employing a single shunt capacitance for modeling the pad, and the lumped model introduced in [38] for the pad-to-line transition. b) Difference between the actual characteristic impedance and the one computed applying [51] to the transmission lines modeled in Figure 3.13a, for different values of line width *W*. The discrepancy increases with the increase of the width step between the pad and the line.

in order to extract the characteristic impedance of the central line section using the method of [51] (Figure 3.13a). The results shown in Figure 3.13b demonstrate how the computation of the characteristic impedance obtained using the calibration comparison method diverges from the correct characteristic impedance value in the presence of a large step discontinuity. The discrepancy reduces with the reduction of step discontinuity, becoming negligible for uniform lines or lower frequencies (where the inductive contribution is also negligible). Thus, it can be stated that the calibration comparison method proves to lose in accuracy when applied to non-uniform structures, i.e., when inductive pad-to-line transitions are present.

3.2.2. Z_0 extraction using EM simulations

Previous subsection has shown how each one of the currently employed measurement based extraction techniques for characteristic impedance presents critical limitations when it comes to characterize transmission lines employed for TRL calibration, and manufactured in silicon technology for mm-wave applications. In this section we describe a characteristic impedance extraction procedure based on 3D electro-magnetic (EM) simulations. The proposed method is developed to reach comparable accuracy to the calibration comparison method of [51], without requiring the extra calibration step, and overcomes its limitation in case of inductive pads-to-line transitions.

The procedure is quite simple in its approach. First, a 3D model of the considered transmission line should be created, taking into account both geometry and material properties. Then, the modeled line is simulated and the S-parameters extracted. Finally, Equation (3.6) is used to compute the characteristic impedance, that can

be eventually used during the TRL calibration for proper re-normalization, using the formalism described in Appendix A. It is self evident that, to use Equation (3.6) while avoiding its limitations described in Section 3.2.1, proper care has to be taken in the stimulus definition.

Design of an on-wafer calibration kit

In order to better understand the procedure, together with its advantages and drawbacks, we will consider a case study. For this purpose, we designed and fabricated a TRL calibration kit using the BEOL of the IHP 130 nm SiGe BiCMOS process, see Figure 3.12. Uniform CPWG lines have been considered to allow direct comparison with probe-level calibrations (i.e., transferred) and with the calibration comparison method, thus removing the error arising from width discontinuities between lines and pads, as also described in Section 3.2.1. The fabricated chip microphotograph of the TRL kit is shown in Figure 3.14 (i.e., thru, reflect and line, respectively a, b and c). The lines are implemented as grounded CPW, to reduce losses in the (semi) conductive substrate. All the structures employ aluminium pads, i.e., signal pad 30x50 µm2 and larger grounds pads to allow different probe pitch to be used on the same structure (i.e., 75 µm and 100 µm). The thru line is a 200 µm long uniform coplanar waveguide (Figure 3.14a). The calibration kit reflects are realized by two symmetric offset shorts (Figure 3.14b), with an offset equal to half the thru length. This minimizes the distance between the centre of the thru and the location of the short, allowing to fix the sign of the square root solution in the TRL calibration [29] (i.e., +/- open/short) for the entire calibration band. Three transmission lines with lengths of 360, 450 and 680 µm are fabricated to allow single line TRL calibration in the WR3, WR5 and WR10 waveguide bands, respectively. The lines have been designed for their insertion length (i.e., the length in excess of the *thru*) to be electrically 90° at the center of the associated waveguide bandwidth. Finally a 600 µm long CPWG is used for calibration verification.

The first two metal layers of the BEOL (Figure 3.12) have been used to realize a meshed ground plane satisfying the metal density rules. The bottom ground plane is electrically connected to the coplanar ground planes using interleaved meshed metal on all layers and employing the maximum via density allowed. The CPW line is 30 µm wide and 3 µm thick with a 10 µm gap (Figure 3.14d). The silicon dioxide acting as a dielectric has a relative permittivity of ca. 4.1, almost homogeneously among the entire structure, allowing simple simulation geometry.

Defining the simulation setup

The structures were simulated using three different 3D electro-magnetic simulators, Keysight EMPro, Ansoft HFSS and CST Studio Suite, to check for simulation discrepancies. In the model, the meshed ground planes have been simplified considering a continuous metal connection, both vertically and horizontally. This simplification provides good approximation of the electrical response of the structure, being the openings in the metal mesh much smaller than the wavelength (maximum aperture is in the order of 2.5x2.5 μm^2), and the openings interleaved among different metal levels. The excitation to the CPW lines is provided by means of waveguide (modal) ports. When using this type of ports, the simulator first solves a two-dimensional

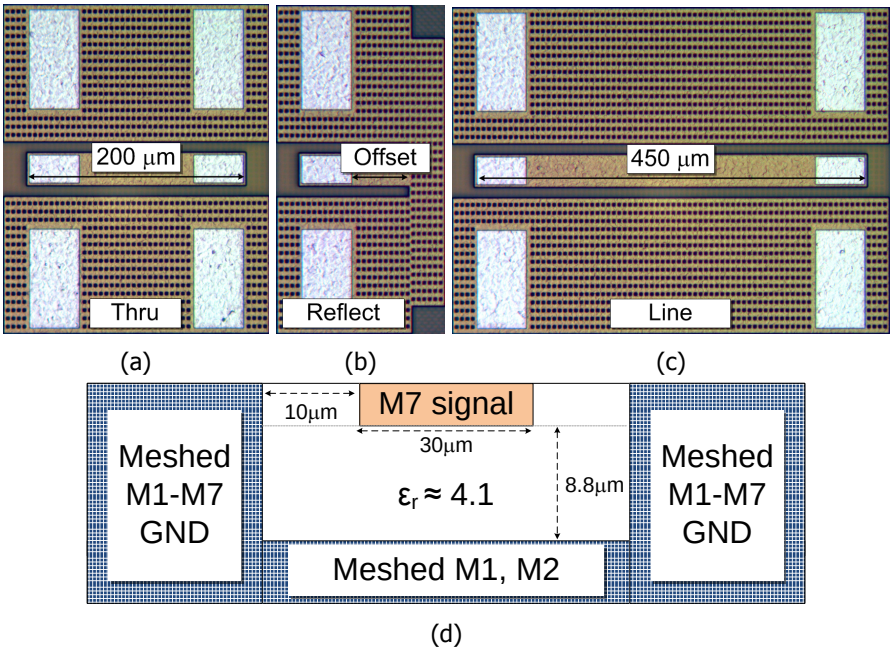


Figure 3.14: CPW calibration artefact realized on IHP SiGe 130 nm BiCMOS technology. (a) Microphotograph of the thru line, (b) of the reflect standard and (c) of the transmission line employed for the WR05 calibration kit. (d) Cross section sketch of the CPW line.

eigenvalue problem to find the waveguide modes of this port and then matches the fields on the port to the propagation mode pattern, and computes the generalized (i.e., mode matched) scattering parameters. In all the simulators, the port dimensions are designed using the rules of thumb described in [57], ensuring ideally no fields at port boundaries, as also depicted in Figure 3.15 for two simulator examples. The use of lumped ports was not taken into account in this work, due to the additional parasitics effect introduced that would affect the computation of the characteristic impedance.

Absorbing/radiation boundaries are then imposed at the lateral and top faces of the simulation box. The box is defined horizontally by the dimensions (length/width) of the simulated structure, and vertically by the wavelength (λ/4 at minimum simulation frequency). The bottom face of the simulation box is defined as a perfect electric conductor, simulating the presence of a metallic chuck underneath the structure, as it is the case during measurements. The absorbing boundaries simulate an unperturbed propagation of the EM waves through this boundary. In this respect, the interference with other structures on the wafer is not taken into account in the simulation. Material parameters and lateral dimension are chosen according to the nominal technology values.

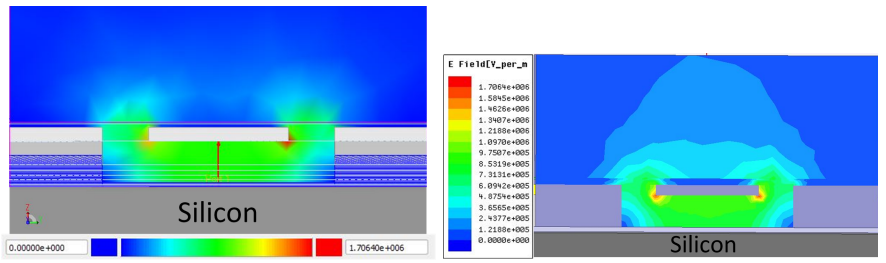


Figure 3.15: Field distribution on waveguide ports at 300 GHz when exciting the structures described in this section, for a) Keysight EMPro and b) Ansoft HFSS.

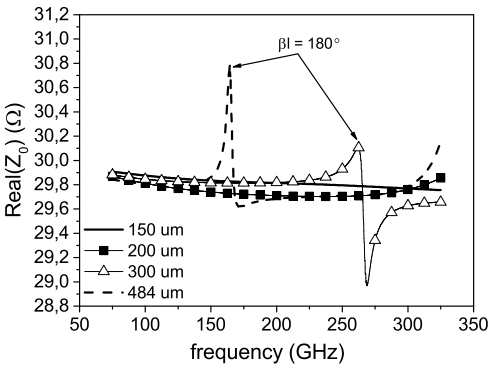


Figure 3.16: Comparison of the real part of the characteristic impedance for the considered structures computed using Equation (3.6) on simulated S-parameters of lines with different lengths, 150 µm, 200 µm, 300 µm and 484 µm versus frequency.

Extracting the characteristic impedance

The scattering parameters calculated during simulation are re-normalized to a given system value (i.e., 50 Ω) and used in Equation (3.6) to compute the line characteristic impedance. The use of waveguide ports during the simulations allows the minimization of the discontinuities between the simulation port and the line. It is important to note that these discontinuities, as shown in [50], contribute to the error in the estimate of Z0, which is maximum as the line lengths approaches half a wavelength. When the half a wavelength condition is reached ($tan(\beta l) = 0$) within the calibration band, large errors in the Z0 estimate will occur. When the half a wavelength condition is kept outside the required frequency band, the differences of Z0 estimate between lines (i.e., 200 µm and 150 µm) are smaller than 0.3% (see, Figure 3.16).

Similar errors can be seen in the estimate of the imaginary part of Z0 versus the electrical length of the line. Note that the simulation environment allows using line lengths below the minimum advised in experimental characterization (i.e., 150

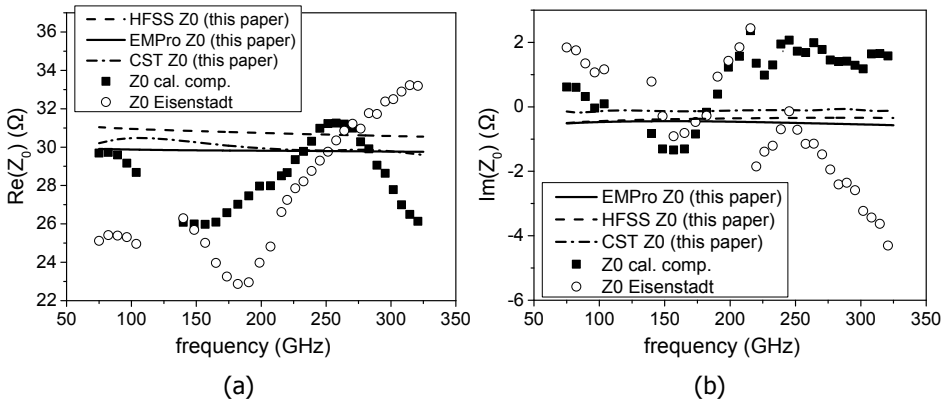


Figure 3.17: Real part (a) and imaginary part (b) of characteristic impedance for the line shown in Figure 3.14a, computed by the simulation approach described in this section (solid lines EMPro, dashed lines HFSS, dashed-dot lines CST), measured with the method of [46] (empty circles) and measured with the method of [51] (filled squares).

μm), limited by the probe to probe cross-talk, thus allowing an accurate estimate of Z_0 in the entire (sub)mm-wave band. A 150 μm line has been used to extract the characteristic impedance in this work. To benchmark the proposed EM extraction approach, the characteristic impedance of the line shown in Figure 3.14a was also extracted, from measured data, with the Eisenstadt and calibration comparison method. For both experimental extraction procedures a probe-level (TRL) calibration performed on a fused silica substrate was employed as a first-tier calibration.

In Figure 3.17 the characteristic impedance computed with the three methods are compared. As can be seen by the plot, Eisenstadt, as predicted from [50], is hampered by the discontinuities due to the probe to pad transition. The impedance extracted using the calibration comparison presents some fluctuations which can be attributed to the inductive nature of the probe to pad transition (i.e., step in transmission line width). Moreover, both mentioned techniques suffer from the errors arising from the calibration transfer from the fused silica substrate.

It is interesting to notice from Figure 3.17 how simulations performed with different tools produce slightly different values for the characteristic impedance. As a matter of fact, the three computations differ up to a maximum of 1 Ω for the real part and 0.1 Ω for the imaginary part, for the same structure, when applying similar settings in terms of meshing and solving methods. This can be considered as an intrinsic uncertainty of the proposed method, since different simulation tools would not converge to exactly equal results. However the discrepancy between the simulators is still much smaller than the fluctuations in the characteristic impedance computed with the Eisenstadt and calibration comparison methods. For the rest of the section, for ease of display, only the simulations obtained with Keysight EMPro will be employed.

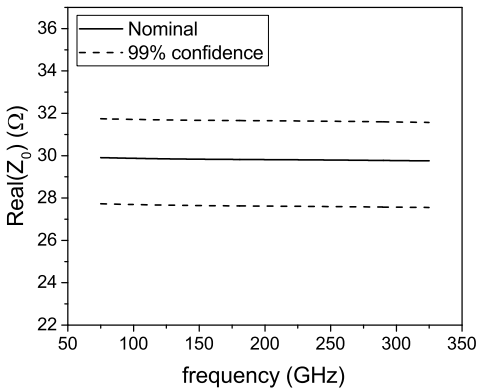


Figure 3.18: Characteristic impedance variation associated to technology tolerances for the transmission lines described in this section, using the same scale of Figure 3.17a.

Simulation uncertainties

The accuracy of simulation based methods (both analytical as well as numerical), relies totally on the accuracy of the model, that is on the completeness of dominant phenomenon description and uncertainty/variation on the material parameters. Modern numerical simulation tools are capable of including all the electromagnetic effects and parameters associated to transmission line propagation. In respect to the main parameters that can influence the characteristic impedance, those are: the line width variations, the interlayer dielectric thickness spread and the dielectric coefficient uncertainty. In order to investigate the impact of these parameters on the characteristic impedance extraction, simulations have been performed using data provided in the IHP 130 nm SiGe BiCMOS process specifications manual.

Results are shown in Figure 3.18, where the variations associated to line width have been neglected, being the tolerance in the order of 300 nm (i.e., 1%). The variations on Z_0 are dominated by the dielectric thickness and dielectric constant uncertainty. Using the process variation reported in the manual, the 99% confidence interval results in a range of ±7% in respect to the nominal case, see Figure 3.18.

Comparison with state of the art methods

In order to validate the method proposed in the previous subsections, we compared different calibration substrates and strategies applied to the measurement of a CPW line. The line is embedded in the technology described in Figure 3.12 and the measurements are carried out for three different waveguide bands, i.e., WR-10 (75-110 GHz), WR-5 (140-220 GHz) and WR-3 (220-325 GHz), using simulation data of the reference line for verification.

The measurements have been carried out on a precision semi-automatic probestation in order to have constant contact force and minimize the probe landing misplacement among the measurements of different structures (see, Figure 3.19).

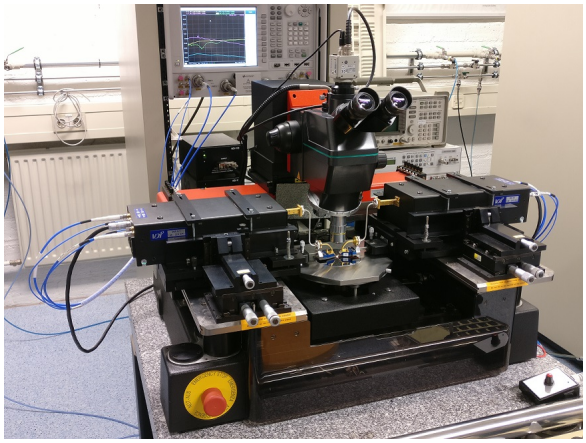


Figure 3.19: Measurement setup employed for the comparison of probe tip calibrations in the WR-5 waveguide bandwidth.

Three different calibration kits have been employed, an ISS LRM calkit on alumina substrate (i.e., W-band 104-783), a TRL calkit designed on fused silica as described in [41] and the TRL calkit on SiGe BiCMOS BEOL shown in Figure 3.12. In order to allow a proper comparison, the calibration planes of the on-wafer (i.e., BiCMOS) calibration have been shifted back to the probe-tips using the propagation constant computed by the TRL algorithm. For the BiCMOS calkit, two cases are considered, one in which the characteristic impedance is extracted with the calibration comparison method, where a probe tip calibration on fused silica is considered as reference, and one in which the characteristic impedance is computed a priori with EM simulations. In order to compare the different calibrations, the method of [36] has been employed, defining a worst case error bound metric as:

$$WCB\,(f) = max\left|S'_{i,j}(f) - S_{i,j}(f)\right| \tag{3.16}$$

Where S' is the reference scattering matrix of the verification line (i.e., 3D simulated S-parameters), S(f) is the frequency dependent scattering matrix resulting from the investigated calibrations (i.e., LRM on alumina, TRL on fused silica and TRL on BiCMOS) and i,j∈[1,2]. This metric defines the upper bound of the deviation of the S-parameters measured by one calibration and the reference S-parameters computed using EM simulations. The measurement data used to compute the error bound of Figure 3.20 are based on the same raw data of the verification line, thus removing any measurement variation of the verification artifact from the error propagation mechanisms. To these raw data the respective calibration algorithm (with the previously computed error terms) were applied. In addition, both the methods indicated as TRL on silicon in Figure 3.20, use also the same raw measurement in the calibration procedure (i.e., extraction of error terms), thus confining their difference only to the characteristic impedance values versus frequency, computed with the two different methods. TRL on fused silica performed sensibly better than

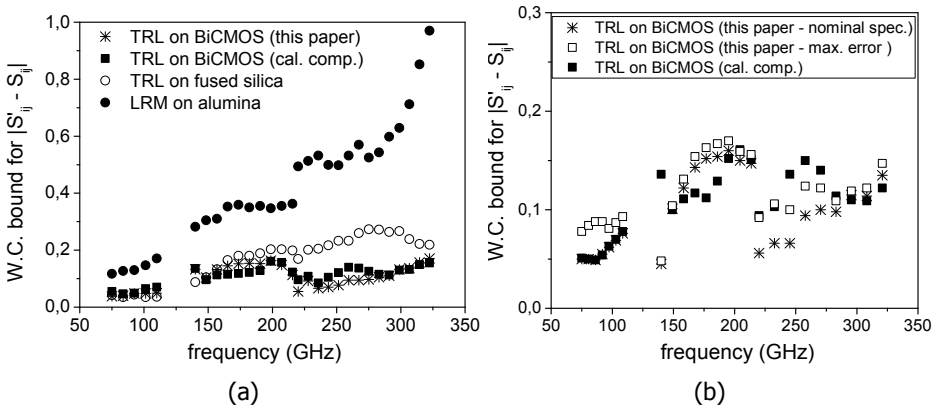


Figure 3.20: a) Comparison of probe-tips corrected measurements of a verification line manufactured on the SiGe BEOL in the frequency range 75-325 GHz for different calibrations. b) Detail of calibration comparison, with error associated to technology tolerance in the Z0 extraction (empty squares).

the LRM on alumina (see, Figure 3.20, empty circles) with the value of the error bound always lower than 0.25 in the entire frequency band. Also in this case the deviation from simulation increases with frequency, as the effect of the delta capacitance associated to the calibration transfer becomes more relevant. The calibration performed on SiGe technology is the one that presents smaller deviation from the reference data, with a WCB<0.17 in the entire frequency band for both characteristic impedance extraction method considered, i.e., the proposed EM-based method (Figure 3.20, asterisks) and the calibration comparison method (Figure 3.20, filled squares). The two BiCMOS calibrations show good agreement with the reference data and track each other well, demonstrating how even discrepancies in the Z0 extraction up to 10% (3 Ω), for both real and imaginary part, result in S-parameter errors smaller than the other sources of error associated to the calibration (e.g., asymmetric probe misplacement, contact resistance fluctuations, contact force repeatability). For the same reason, errors on simulation associated to process tolerances, as described before, have a very small impact on the overall error, as shown in Figure 3.20b, especially at higher frequencies where other sources of error tend to dominate. It is important to mention that repeated measurements over different devices on the BiCMOS calibration kit in the highest frequency band (i.e., WR-3) show a measurement repeatability defined by a maximum standard deviation σ = 0.033. This value is always below the minimum value of the UB metric shown in Figure 3.20, which is in the order of 0.05.

Application to CPWs with inductive transitions

When considering lines with more complex transitions, the calibration comparison provides lower accuracy due to the unaccounted series reactance as explained in Section 3.2.1. In order to demonstrate the improvement provided by the proposed method, we consider a TRL de-embedding kit manufactured on NXP QubiC4XI 0.25 µm BiCMOS SiGe, employing non uniform lines. The structures composing this de-

embedding kit present large GSG landing pads, with 50 µm diameter. The signal pad is directly connected to a micro strip having a width of 10.5 µm, creating an inductive series transition between the landing pads and the line. The TRL kit features a 162 µm thru, a pair of short standards and a line of additional 662 µm length (see, Figure 3.21a). This BiCMOS kit has been used to perform a TRL calibration in

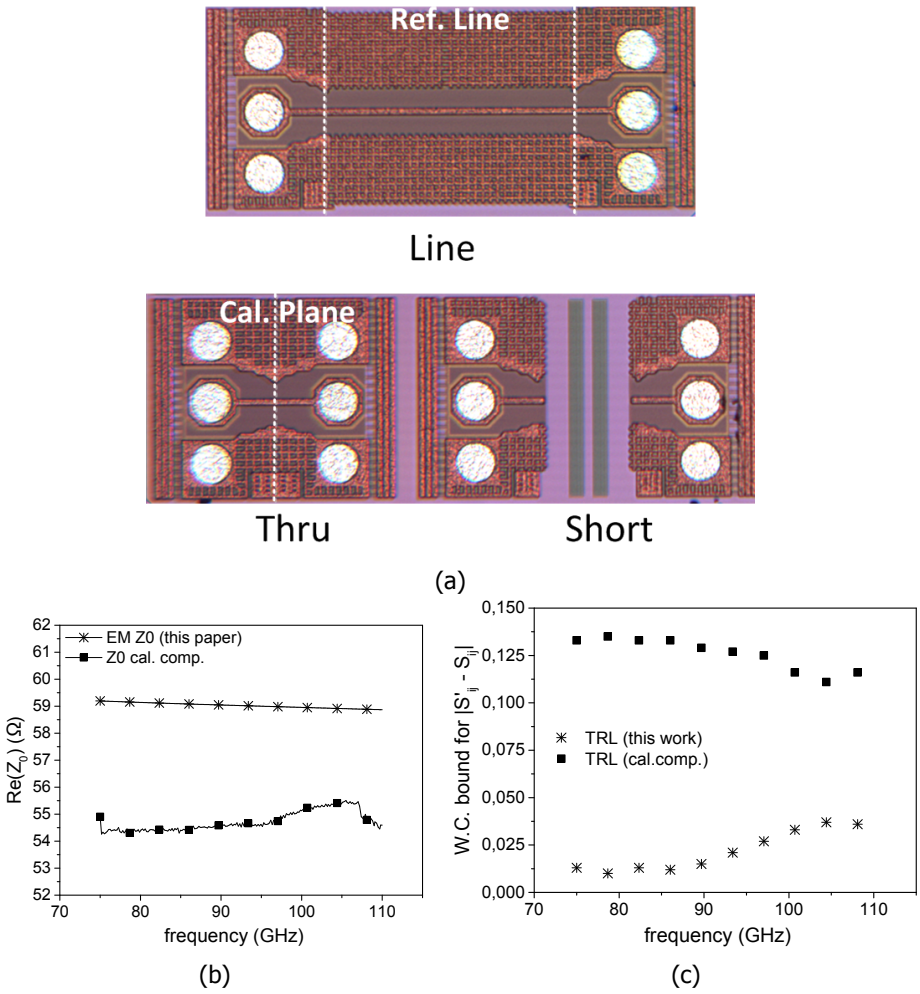


Figure 3.21: a) TRL de-embedding kit manufactured on NXP QubiC4XI 0.25 µm BiCMOS SiGe. b) Real part of the characteristic impedance for the Qubic4XI intrinsic transmission line extracted with the simulation method described in this section (solid line - asterisks) and the calibration comparison method (solid line – full squares). c) Comparison of TRL calibrations performed on the calkit shown in Figure 3.14 when employing the characteristic impedance extracted with the calibration comparison method of (full squares) and the simulation based method extracted in this work (asterisks)

the frequency range from 75 GHz to 110 GHz, where the employed characteristic impedance has been extracted using EM simulations of the intrinsic transmission line

and compared with the Z_0 computed using the calibration comparison method of [51]. Figure 3.21b shows the real part of the characteristic impedance computed with both methods. The characteristic impedance computed with the calibration comparison method shows deviations from simulation (up to 5 Ω for the real part) and a lower value, consistent with the presence of an inductance in series with the pad, as described in [53]. These deviations directly affect the measurements, as shown in Figure 3.21c, where the upper bound of the error as defined in Equation (3.16) is displayed for both considered methods, using the EM simulated data as the reference values. The results show how the errors in the characteristic impedance extraction, when using the calibration comparison technique, are dominating all other sources of error, resulting in a upper bound up to one order of magnitude higher than the one achieved using the proposed method.

3.3. Conclusions

Calibration for on-wafer measurements can present peculiar challenges when a (sub)mm-wave characterization is required. The conventional approach of transferring the calibration from a low loss substrate to the measurement environment risks to degrade the measurement accuracy for two main reasons: on one end, the propagation of unwanted modes in CPW lines (typically used on planar calibration) may violate the single-mode propagation condition in TRL calibration, degrading performances. On the other end, the difference in probe-to-substrate capacitance arising from the calibration transfer process is not corrected for by conventional two-tier calibrations. The impact on both problems can be minimized with one single solution: the use of insulator materials with lower dielectric constant (i.e., fused silica), shifting the cutoff frequency of unwanted propagating modes to higher frequencies, and minimizing the delta capacitance due to the limited difference in dielectric constant between fused silica and silicon BEOL. Nonetheless, the only radical solution to eliminate the errors due to calibration transfer is to reduce the calibration to one single-tier procedure, using calkits manufactured in the same environment as the one of the final DUT. For TRL calkits realized on silicon technology, the main challenge lies in the extraction of the characteristic impedance of the employed lines, needed for the proper re-normalization of the measurement reference impedance. Conventional measurement-based methods are generally inadequate for lines realized on lossy, stratified materials, when measuring at (sub)mm-wave frequencies and when inductive probe-to-line transitions are present. The EM-based extraction method presented in this chapter allows solving the abovementioned problems, by eliminating the simplifications and discontinuities at the basis of the failure of conventional methods. The proposed method has been benchmarked towards the state of the art (i.e., the calibration comparison method) on uniform transmission lines, where inductive probe-to-line effects are minimized due to the geometry, and proved to outperform the calibration comparison method when inductive transitions are instead present.

4

Capacitively loaded inverted CPWS for distributed calibration and de-embedding

While in Chapter 3 the benefits of performing VNA calibration directly on the final DUT environment have been discussed, after calibration the measurement reference plane might be still not placed at the DUT reference plane. This is especially the case when attempting to characterize transistors for model extraction or validation. In this case, the DUT needs to be embedded in special *test fixtures* to allow the proper interconnection. A general simplified interface to the active device from the coplanar (GSG) interface provided by the probe tip is sketched in Figure 4.1. Test fixtures might have complex geometries and extend on different metal layers, as the DUT terminals are typically set by technology at lower metals (i.e., metal 1 or metal 2). The parasitics associated to these additional structures will therefore be included in the measurement, introducing an error on the DUT characterization that need to be corrected (*de-embedded*). Classical measurement procedures consist, after a probe-tips calibration, of an on-wafer de-embedding, which allows to quantify and properly remove the parasitics associated to the test-fixture, effectively moving the reference plane as close as possible to the DUT. With the increased maximum oscillation frequency of modern technologies (deriving from reduced device geometries), these fixture parasitics tend to dominate the ones of the intrinsic device, placing more emphasis on the de-embedding process [59]. In this chapter, the use of capacitively loaded inverted CPWs (CL-ICPW) in test fixtures for

Parts of this chapter have been published in Capacitively Loaded Inverted CPWs for Distributed TRL Based De-Embedding at (sub)mm-Waves (2017) [58].

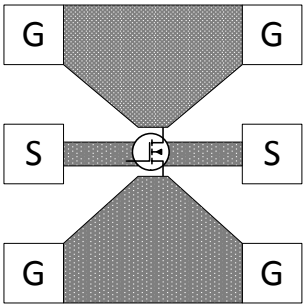


Figure 4.1: Generalized sketch of a ground-signal-ground test fixture for transistor characterization.

(sub)mm-wave device de-embedding is introduced. These transmission lines allow implementing a distributed TRL de-embedding of the fixture, opening the possibility for *direct* calibration up to the DUT reference planes, without the need of additional de-embedding procedures.

4.1. Direct DUT-plane calibration

De-embedding procedures are conventionally based on lumped approximations of the test-fixture parasitics. The lumped components are quantified by means of different dummy structures measurements(i.e., pad, open, short, etc.) [60–62]. With the increase of the model extraction/validation frequency, the single shunt-series parasitic approximation of the fixture model (assumed by the open-short de-embedding), together with the ideal nature of the open and short conditions becomes less accurate [63].

To mitigate this effect, various approaches presented in literature increase the number of measurement dummies and/or elements in the fixture model [63, 64]. But bandwidth limitation of any finite elements lumped model is still conflicting with the needs of state-of-the-art high speed technologies, i.e., capability to extract/validate models in the higher frequency range. For this reason, a fully distributed technique, providing no intrinsic upper frequency limitation and capable of providing a direct calibration at the device reference plane, with a limited number of structures would provide the optimal solution for device model extraction/validation in the (sub)mm-wave region. From this perspective, the use of a thru-reflect-line (TRL) [29] de-embedding procedure would be the preferable choice, due to the high accuracy and limited knowledge of the standards required by this technique. Several papers have been reported in which TRL is employed for device characterization at mm-wave [65–67], where the calibration/ de-embedding transmission lines have been realized on the top metal layer of the technology back-end-of-line (BEOL). This allows to achieve high quality transmission lines (thick metal and $Z_0 \cong$ 50 Ω), at the expense of a larger physical separation from the intrinsic DUT, thus requiring an extra step (often based on lumped approximation) to remove the access structures to the device. The realization of a direct calibration/de-embedding

process, removing all parasitics up to the intrinsic device ports, employing TRL distributed technique, would need to address the following challenges:

1. transmission lines realized on *M1* would be exposed to the lossy and poorly controlled substrate, degrading the propagation characteristics of the line;

2. the characteristic impedance of the M1 lines would be difficult to quantify using state-of-the-art-techniques, like the calibration comparison method [51], or methods based on the knowledge of the propagation constant [47]. In the first case, the inductive pad-to-line transitions between the access and the TRL lines are not accounted for by the model [53] and might lead to big errors at mm-wave frequencies [68]. In the second, the assumptions associated to the line, where C_0 is approximated to the dc-capacitance scaled for the length, with low loss substrates (i.e., $G_0 \cong 0$), weak transverse currents in the conductors, and no dispersion in the material permittivity [48], [49], might be easily violated in case of high frequency and dispersive materials.

To address the aforementioned challenges, we designed a TRL calibration/ de-embedding kit, employing transmission lines realized on M1 with high capacitive loading (per unit length) to confine the field in the dielectric layers of the BEOL, thus minimizing the interaction with the dispersive substrate. The characteristic impedance of the capacitively loaded inverted CPWs (CL-ICPW) is computed by means of EM simulations, as described in Chapter 3, overcoming the challenges of extracting the characteristic impedance of lines with no direct access.

4.2. CL-ICPW concept

When considering CMOS/BiCMOS technologies, classical CPW topologies suffer from significant losses already at microwave frequencies (1-2 dB/mm at 10 GHz) [69]. A typical approach to reduce these losses is to shield the conductive substrate by means of a meshed metal ground plane, thus realizing a grounded CPW [70]. If the goal, is to design CPWs in the lowest metal layer (i.e., M1 in Figure 4.3), then no metal to realize the shield is available, thus leaving the transmission line exposed to the lossy substrate. In this case, the energy flowing along the line will be partitioned based on the permittivity of the two surrounding media, i.e. silicon (ε_{Si} = 11.9) and SiO_2 (ε_{SiO_2} = 4). The higher permittivity medium will store proportionally more energy, thus leading to increased energy flowing in the lossy substrate ($\varepsilon_{Si} > \varepsilon_{SiO_2}$). To invert this behavior, the storage capacity of the oxide, quantified by the capacitance per unit length, needs to be increased. This result can be achieved when a short distance between the signal line and the ground plane of the CPWG is employed. Nevertheless, this approach results in very narrow line widths (i.e., large conduction losses) when impedance range close to the system impedance are targeted. Alternatively, the silicon dioxide dielectric constant can be artificially increased. This can be achieved by inserting floating metal planes in the host dielectric, in close proximity to the signal line. By doing so, the propagating field is "pulled" towards the shield into the dielectric, thus reducing its penetration into the substrate, minimizing the losses generated by silicon. However, additional

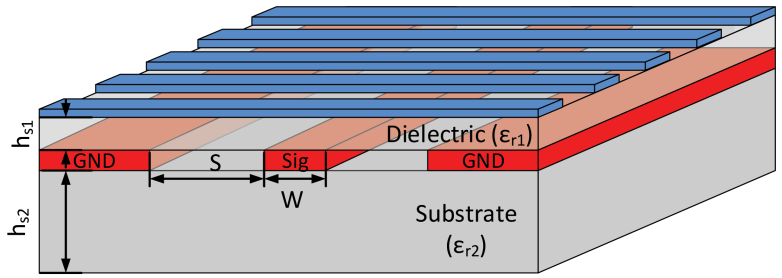


Figure 4.2: Simplified sketch of a CL-ICPW section. The transmission line consists of a CPW realized over the lossy substrate, characterized by a dielectric constant ε_{r_2}, and is capacitively loaded by means of floating bars separated by a dielectric layer, with dielectric constant ε_{r_1}.

4

conductive losses could arise, due to eddy currents in the shield together with a reduced inductance per unit length which is generated by the opposite magnetic field forced by the return current. To minimize these effects, the shield can be realized with (thin) floating bars, orthogonal to the signal propagation, as in slow-wave CPWs (SW-CPW) [71]. The floating bars represent a capacitive load which can be defined by the designer. A so made device, constituted by a transmission line on a lossy substrate, with a capacitive load realized by means of floating metal bars in a surrounding low-loss dielectric, is defined as capacitively loaded inverse CPW (CL-ICPW). A simplified cross section of a CL-ICPW is sketched in Figure 4.2, where the thin oxide layer between the CPW and substrate has been omitted to simplify the drawing. The dimensions of the CL-ICPW vary from few tenths of a micron in the vertical separation to decade of microns in the lateral dimension (i.e., line and gaps) requiring large CPU resources and computation time when an extensive electromagnetic analysis is needed for design purposes. For this reason, it helps to develop a simplified mathematical model for the CL-ICPW based on conformal mapping, to support preliminary line sizing and design. Using the CPW analysis of [71] detailed in Appendix B, the effective dielectric coefficient of the CL-ICPW, ε_{eff} can be computed, as:

$$\varepsilon_{eff} = \frac{C_{tot}}{C_{air}} = \frac{\varepsilon_{r_2} + 1}{2} + \varepsilon_{BOOST} \tag{4.1}$$

$$\varepsilon_{BOOST} = \frac{\varepsilon_{r_1} \cdot W}{4 \cdot h_{s_1}} \cdot \frac{K\left(k_0'\right)}{K\left(k_0\right)} \tag{4.2}$$

Where all the variables are extensively introduced in Appendix B. The first contribution in Equation (4.1) is the effective dielectric coefficient associated to a conventional CPW above a substrate with dielectric ε_{r_2} (i.e., no top dielectric ε_{r_1} and floating shield). ε_{BOOST} represents the increase in the effective dielectric coefficient due to the capacitive load alone. Starting from the knowledge of C_{Tot} and ε_{eff}, it is also possible to derive the phase velocity v and the characteristic impedance Z_0 of

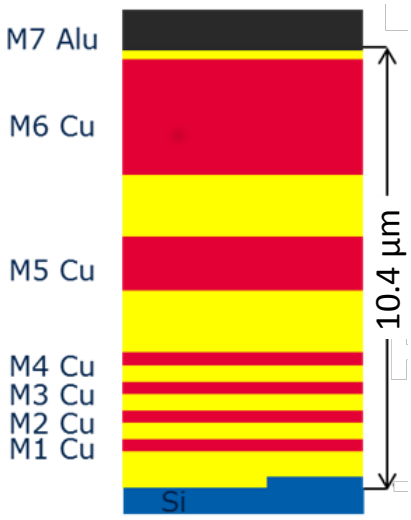


Figure 4.3: Sketched image of the BEOL of the Infineon B11HFC technology.

the transmission line, as:

$$v = \frac{c}{\sqrt{\varepsilon_{eff}}} \tag{4.3}$$

$$Z_0 = \frac{1}{C_{tot} \cdot v} \tag{4.4}$$

Note that ε_{r_1}, ε_{r_2} are fixed by the technology, thus ε_{eff}, v and Z_0 can only be influenced by varying the geometrical dimensions S, W and h_{S_1}. The TRL calibration/de-embedding kit based on the CL-ICPW developed in this work was fabricated in the BEOL of Infineon's 130 nm SiGe BiCMOS technology B11HFC, shown in Figure 4.3, providing 250 GHz/380 GHz f_T/f_{max} npn transistors and six copper metallization layers with a 2.9 µm thick upper metal. In this implementation, the minimum h_{S_1} value is determined by the distance between M1 and M2 which is in the range of few hundreds of nm, while the maximum value (i.e., M7) is in the order of 10 µm. To analyze the performance of the specified technology, three different positions have been considered for the floating shield, for a fixed CPW geometry with W = 5 µm and S = 10 µm, using M2 (h_s = 0.34 µm), M3 (h_s = 1.07 µm) and M4 (h_s = 1.80 µm). Using these specifications, 3D models of the CL-ICPW lines have been simulated with Keysight EMPro using waveguide ports in the frequency range between 220 and 325 GHz. First, the S-parameters computed during simulations have been employed to extract the ε_{eff} and Z_0 of the lines. Then, the extracted parameters are compared with the analytic model.

Figure 4.4a and Figure 4.4b show the dependence of ε_{eff} and Z_0 on the height of the floating shield h_{S_1}. The continuous lines represent the values computed by Equation (4.1) and Equation (4.3), considering a silicon substrate (ε_{r_2} = 11.9) and

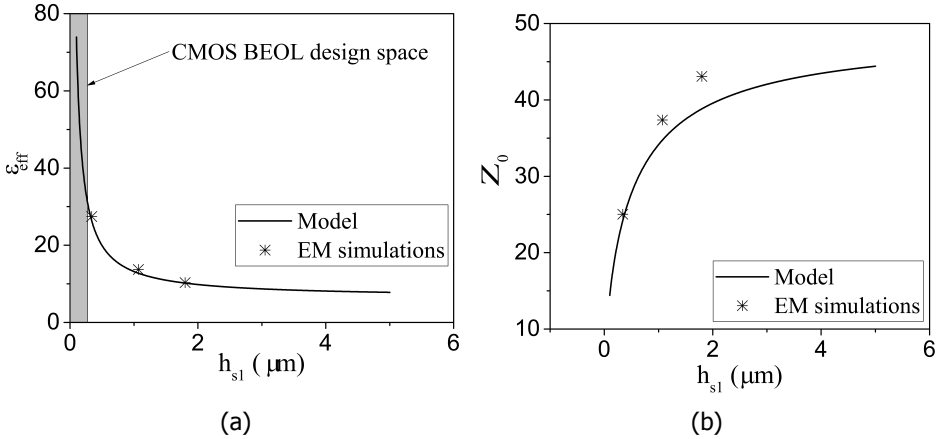


Figure 4.4: Effective permittivity (a) and characteristic impedance (b), plotted versus the height of the floating shield for the CL-ICPW lines considering a silicon substrate (ε_{r_2} = 11.9) and silicon dioxide as dielectric (ε_{r_1} = 4.1), and assuming W = 5 μm and S = 10 μm. The value is computed using the proposed model (solid line) and extracted by means of electromagnetic simulations of the lines as described in Section 4.3 (symbols) at 300 GHz. The grey area in (a) highlights the values of effective permittivity that can be achieved when employing CMOS technology, where the h_{S_1} dimensions, when employing M2 for the floating shield, can be very small (i.e., <300 nm).

silicon dioxide as dielectric (ε_{r_1} = 4.1) with W=5 μm and S=10 μm, while the symbols are 3D EM simulations for the same lines, using the fixed layers position supported by the technology (cf. Figure 4.3). The close agreement between EM simulations and the proposed model provide a first order validation of the proposed approach. A small degree of divergence is visible with increasing h_{s_1} due to the fact that the condition S»h_{s_1}, applied in the model, loses validity when h_{s_1} becomes greater than a tenth of S. The aforementioned electrical parameters of the line have been derived in the hypothesis of lossless material. For consistency with the analytical model, also the EM simulations have been performed assuming no losses in the employed media (i.e., perfect conductor, lossless dielectric, lossless substrate). However, such a CL-ICPW is intended to be used in a situation in which material 1 has low losses (i.e., silicon dioxide), while material 2 presents a finite conductivity (i.e., silicon substrate). The dielectric losses α associated to the substrate can be taken into account as:

$$\alpha = AR \cdot 8.66 \cdot \frac{Z_0}{10\rho} \cdot \frac{K(k)}{K\left(k'\right)} \tag{4.5}$$

Where:

$$AR = \frac{\varepsilon_{r_2} + 1}{2 \cdot \varepsilon_{eff}} \tag{4.6}$$

Equation (4.5) is derived by [72] and modified in order to take account that the field propagating in the substrate is just a portion of the total field by means

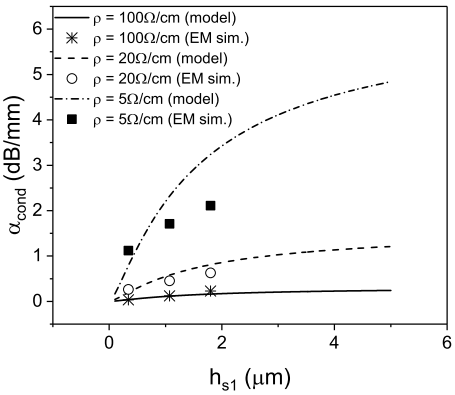


Figure 4.5: Conductive losses in the substrate plotted versus the height of the floating shield for the CL-ICPW lines considering a silicon substrate (ε_{r_2} = 11.9) and silicon dioxide as dielectric (ε_{r_1} = 4.1), and assuming W = 5 μm and S = 10 μm. The value is computed using the proposed model (solid line) and extracted by means of electromagnetic simulations of the lines as described in Section 4.3 (symbols) at 300 GHz.

of AR, which is the ratio between the effective ε_r of the CPW in silicon, and the total effective permittivity of the complete structure. In Figure 4.5 the values of α_G versus the height of the floating shield are displayed for different values of substrate resistivity in the range from 5 Ω/cm to 100 Ω/cm for the same CL-ICPW described in Figure 4.4a and Figure 4.4b. The lines are generated using the proposed model sweeping the height of the dielectric layer, while the symbols are the result of 3D EM simulations using the same W and S as in the model and for three discrete h_{s_1}, fixed by the metal stack in the chosen technology. As shown by the figure, the losses (α_G) decrease, as expected, with increasing substrate resistivity, but also with the proximity of the shield. This proximity of the shield results in an increased capacitively load, confining the field in the dielectric which can be evaluated by the reduced AR. When considering CL-ICPW on low resistivity substrates with the increase of the height of the floating shield, the discrepancies between the model and EM simulations increase, which can be explained with increased energy running in the high permittivity (electrically thick) layer giving rise to other loss mechanism not accounted for by the first order model proposed (i.e., surface waves). Note that in these EM simulations, only the losses associated with the substrate have been introduced, while conductors and dielectric layers have still been considered as ideal.

4.2.1. CL-ICPW as a transmission line

To this point, CL-ICPW structures have been described by means of (quasi-static) transmission lines theory. It is worth now to make a step back to make some considerations on the behavior of these structures, first to prove that they indeed can be represented as transmission lines and also to justify the choice of such a

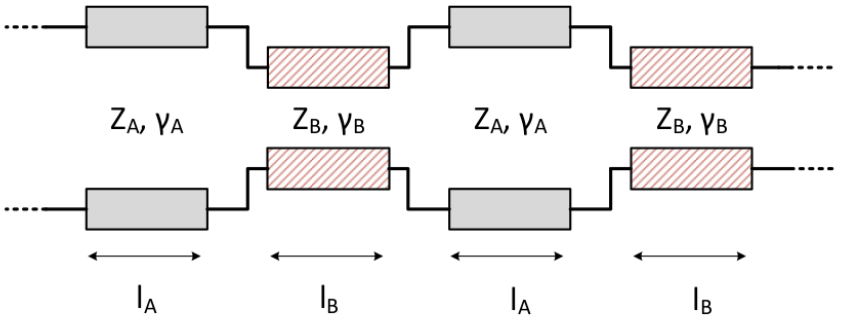


Figure 4.6: Schematic representation of a slow-wave transmission line as an artificial periodical transmission line, defined as the repetition of two separated sections of transmission lines characterized by different characteristic impedance Z_A and Z_B, and propagation constant Γ_A and Γ_B

topology for the purpose of calibration (or de-embedding) standards. Being the CL-ICPW a periodical structure, we can stipulate that two conditions need to apply in order to consider it a well-behaved transmission line: first, the structure needs to support guided propagation at the frequencies of interest and second, the number of repetitions in the periodical structure of the CL-ICPW needs to be sufficiently high.

Bragg frequency

Owing to its design, a CL-ICPW can be seen as a periodical artificial transmission line structure. As such, its fundamental propagation mode is characterized by a first propagation bandwidth, followed by a stop-band which onset is defined by a specific *Bragg frequency*, or cut-off frequency [73]. At Bragg frequency propagation stops as the propagation constant and the characteristic impedance become purely imaginary. The Bragg frequency can be identified as the frequencies at which the propagation constant B of the line intercepts the first Brillouin zone [74], defined such as $\mathrm{B} = \frac{\pi}{l}$ [75], where l is the length of the periodic section of the structure. To find the Bragg frequency for the considered structure let's assume, for simplicity, the CL-ICPW as equivalent to a slow-wave transmission line. As reported in [71], a slow-wave type of transmission line can be analysed as a sequence of repeated structures A and B, with different characteristic impedance and propagation constant, as schematized in Figure 4.6. Applying the same principle to the CL-ICPW, we can consider structure A as a section with length l_A = 2 µm corresponding to one floating bar, and B a section with length l_B = 2 µm corresponding to a region without floating bar (we will see in Section 4.3 how these will be the chosen dimension for the implemented structure). The propagation constant (and, in turn, the dispersion plot of the line) can be extracted by using Floquet spatial harmonic expansion, as described in [71]:

$$cos(\beta l) = \frac{(1+K)^2}{4K} cos(\beta_A l_A + \beta_B l_B) - \frac{(1-K)^2}{4K} cos(\beta_A l_A + \beta_B l_B) \qquad (4.7)$$

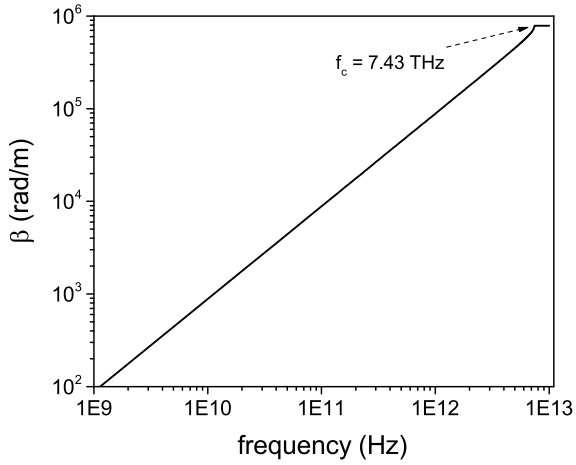


Figure 4.7: Dispersion diagram for the CL-ICPW structure realized using Equation (4.7).

Where $l = l_A + l_B = 4\mu m$ and $K = \frac{Z_A}{Z_B}$, and we only considered the real part β of the propagation constant γ. When numerically solving Equation (4.7) for β (see, Figure 4.7), we can find the frequency f_c, at which $= \frac{\pi}{l} = 7.8540 * 10^5 rad/m$, which for the considered structure results to be $f_c = 7.43THz$. From Figure 4.7, it is possible to notice how the cut-off frequency f_c can be highlighted as the frequency at which B deviates from linearity before becoming undefined, as also suggested in [71]. A generalized rule of thumb suggests that an artificial periodical transmission line is well behaved an none (weakly) dispersive for frequencies lower than $\frac{f_c}{2}$, which in this case would be around 3.7 THz.

Repetition number in periodic structures

Using Equation (4.3), it is possible to analytically extract the propagation constant of the CL-ICPW as $\beta = 2\pi\nu$. Once β is computed, the electrical length (versus frequency) of the transmission line can be extracted. Considering a single element of the periodical structure as defined above, i.e., 4 μm, the electrical length at 220 GHz (which, in the rest of this chapter, will be the minimum frequency of operation) is 3.77°. In order for a section of line to be considered sufficiently long to be a transmission line, a common rule of thumb is to have an electrical length of at least a quarter wavelength (i.e., 90°). In the considered case, this would require circa 24 repetitions, obtaining a 96 μm long transmission line. For this reason the minimum length for a CL-ICPW to be used in the considered technology is set to 100 μm.

The CL-ICPW topology

It could be argued that other configurations, based on microstrip lines (MSs) rather than CPWs, could be preferred for the realization of inversed structures for low metal level propagation. In order to justify the choice of a CPW based topology, we

will make use of a comparison. The choice of a specific transmission line topology (i.e., CPW, MS or ICL-CPW) for the purpose of TRL calibration/de-embedding, is the result of a trade-off between characteristic impedance (that needs to be close to the system impedance), losses (typically dominated by the conductors) and dispersion in the wave propagation (i.e., leakage of energy from the fundamental propagating modes to other propagating modes). The first point to be addressed is to define the range of characteristic impedance that can be used for a line to obtain an accurate TRL calibration. In general, TRL lines are usually designed for 50 Ω characteristic impedance, in order to guarantee high sensitivity of the VNA. It is possible to roughly define the range of impedances that allows little reduction of sensitivity as in between 30 Ω and 70 Ω [76]. Other than the sensitivity of the instrument, TRL calibration can also suffer a loss on sensitivity when the raw values of the reflection coefficient measured during the calibration procedure do not provide a sufficient difference between the reflect (often a short) and the transmission line. So, if the line is extremely mismatched (i.e., the characteristic impedance differs strongly from 50 Ω) the TRL calibration might have lower accuracy. On the other end, when considering on-wafer technologies (i.e., silicon), due to the large capacitive loading presented by the thin BEOL, the characteristic impedance of transmission lines is typically low, with also small margin of variation with geometry, due to the strong design rule constraints. Considering this trade-off, we can define a target characteristic impedance for this analysis approximately equal to 35 Ω. In order to perform the analysis, we will compare four different structures, in which the geometry has been optimized to comply with the target characteristic impedance (see, Figure 4.8):

- A CL-ICPW, as described in Section 4.2 and realized in the BEOL represented in Figure 4.3, with dimensions W = 5 µm, S = 10 µm, and floating shield placed at M3 (i.e., h_{s1} = 1.07 µm), labeled as Ref. CL-ICPW in Figure 4.8a .
- A microstrip line with signal conductor placed at M1, W = 18 µm,and ground placed at M7 (h_{s1} = 9.6 µm), labeled as MS1 in Figure 4.8b.
- A microstrip line with signal conductor placed at M1, W = 10 µm, and ground placed at M5 (h_{s1} = 3.7 µm), labeled as MS2 in Figure 4.8c.
- A microstrip line with signal conductor placed at M1, W = 2.5 µm, ground placed at M3 (h_{s1} = 1.07 µm), labeled as MS3 in Figure 4.8d.

Once the transmission lines are realized, they can be modeled into a 3D simulator and then properties like characteristic impedance and losses can be extracted. The real and imaginary part, versus frequency, of the characteristic impedance are displayed, for all structures, in Figure 4.9. The comparison shows that the ref. CL-ICPW and the MS3 line present none or weak frequency dependence for the characteristic impedance versus frequency, while MS1 and MS2 show much higher dispersivity.

In this respect, it is important to note that, in the considered simulations, no dissipation mechanism is included (i.e., perfect conductors and lossless dielectrics/

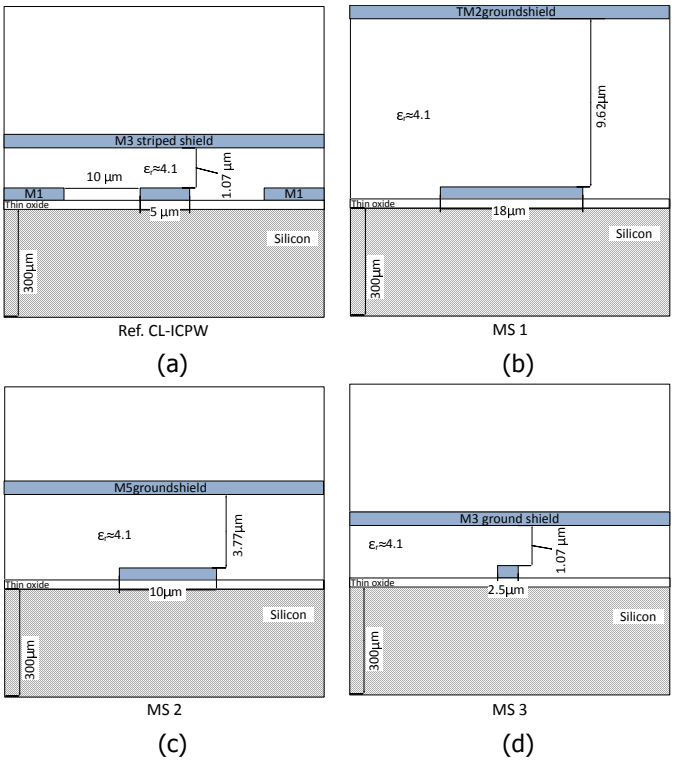
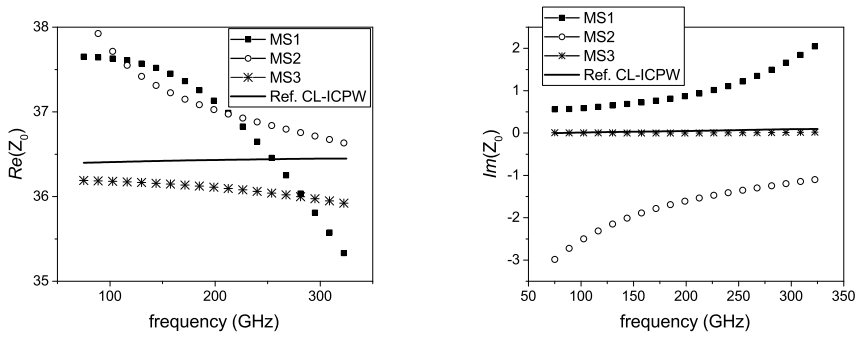


Figure 4.8: Different shielded transmission line topologies realized in the Infineon BEOL, designed for a target characteristic impedance Z_0 ≈35 Ω. a) CL-ICPW. b) Microstrip shielded at M7. c) Microstrip shielded at M5. d) Microstrip shielded at M3.

substrates are employed), thus indicating the presence of non-TEM mode propagating in MS1 and MS2. This behavior can be associated with different mechanisms. The strong asimmetry and the non-homogeneity of the substrate can trigger the onset of higher order modes at relatively low frequency. On top of that, the high "electrical thickness" of the silicon (i.e., high dielectric costant - ε_r = 11.9 - combined with relatively high thickness - 300 µm) allows supporting several waveguide modes inside the silicon. In the case of MS3, instead, the close proximity of the ground shield allows the propagation of a basically single microstrip mode, confining most of the propagating energy in the low dispersive BEOL, at least until the considered maximum frequency (i.e., 325 GHz) so that the line is non-dispersive in the considered frequency range, as it is also the case for the ref. CL-ICPW. Considering that TRL calibration relies on non-dispersive propagation inside the employed transmission line, MS1 and MS2 are not good topology for the desired purposes, and are then discarded from this analysis. At this point, it is interesting to include the ohmic losses. When targeting a specific value of characteristic impedance, and other conditions remain the same (thickness of the conductor, thickness of the substrate, h_{s1}) a microstrip presents a signal width always smaller than a CPW (in this



(a) (b)

Figure 4.9: Real part (a) and imaginary part (b) of the characteristic impedance for the structures used for the comparison between microstrip and CL-ICPW implementation, extracted by means of electromagnetic simulation on 100 µm long lines.

case, W_{MS3} = 2.5 µm, while $W_{CL\text{-}ICPW}$ = 5 µm). This gives rise to higher ohmic losses for MS3, as also confirmed by electromagnetic simulations (see, Figure 4.10). As displayed in the plot, the losses associated to the conductors for MS3 are roughly double in respect to the ref. CL-ICPW. Considering that the losses due to the conductivity of the substrate are comparable for the two structures (α_{sub} ≈1.5 dB/mm for ρ= 5 Ωcm), and that the dielectric losses in the BEOL are negligible for both structures (α_{diel} ≈0.1 dB/mm at 325 GHz), the ohmic losses represent the main contribution to power loss, therefore justifying the choice of a CL-ICPW as compared to a microstrip based topology for the purposes of TRL calibration.

4.3. Design of calibration/de-embedding kit

The general schematic for one of the structures of the calibration/de-embedding kit is shown in Figure 4.11. It features three main sections: an input stage (pad plus launch line) represented by section *a* and realized in M7; a transition from M7 to M1 (section *b*) composed by all metal layers and interconnecting vias, and the final DUT stage, realized on M1 using CL-ICPWs, that can feature a transmission line (thru or line for the TRL de-embedding kit) or an offset short (section *c*).

For ease of characterization, in the input stage the central conductor of the launch line has been designed with a constant width of 30 µm which is equal to the width of the signal probe pad, and a 15 µm gap guaranteeing a characteristic impedance of 35 Ω which is close to the one presented from the CL-ICPW. Figure 4.12a shows a schematic of the cross section of Figure 4.11, section (a), where M3 is used as ground shield in order to isolate the CPW from the lossy substrate. The transition from the top metal center conductor of the CPW to the M1 center conductor of the CL-ICPW is realized using a gradual, inverse pyramidal shape, in order to connect the large top metal conductor (i.e., 30 µm width) with the small center conductor of the CL-ICPW, minimizing the dimension of the transition while keeping

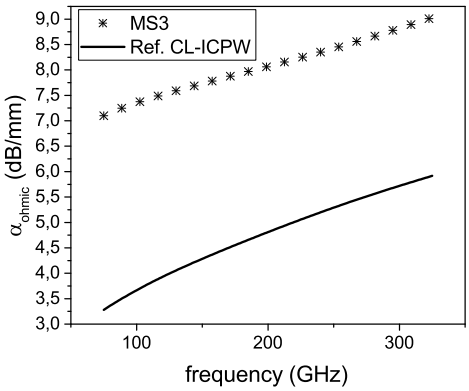


Figure 4.10: Attenuation due to ohmic losses in the transmission line for ref. CL-ICPW (solid line) and MS3 (symbols).

the ground reference at the same metal level (i.e., M3) as shown in Figure 4.12b.

For the DUT stage, M3 is chosen as the metal layer for the floating shield. This choice allows reducing the losses (up to 60% considering the model as displayed in Figure 4.5) while guaranteeing a Z_0 of 34 Ω that, as described in [76] is enough to guarantee good accuracy when measuring in a conventional VNA-based setup. The shield is realized with 2 µm wide metal strips and a fill factor of 50% in order to respect the design rules. The cross section of the final design for the CL-ICPW is shown in Figure 4.12c, where a second level of shield has been used at M4 to reduce the losses associated to field dispersion due to the low fill factor used in the floating shield, and an additional one at the top metal for further shielding. The calibration/de-embedding kit operating in the frequency range from 220 GHz to 325 GHz is shown in Figure 4.13, and employs 130 µm long launch lines. The thru standard is realized by means of a 150 µm CL-ICPW, and it is designed to embed the final device in its center reference plane. The de-embedding kit reflects are realized by means of two symmetric offset shorts, with an offset equal to half the thru length. Furthermore, a longer line with an additional 80 µm length for the CL-ICPW, in respect to the thru, is realized as the line standard. Finally, a test structure consisting of a 310 µm long CL-ICPW has been realized for verification. Once the structure has been properly designed, EM simulations can be performed. Since the only information needed for the TRL calibration/de-embedding procedure is the characteristic impedance of the transmission line in the DUT stage (see, Figure 4.11 section c), which in our case is the CL-ICPW, this is the only part of the de-embedding structure which needs to be simulated. The CL-ICPW has been simulated using Keysight EMPro and excited using waveguide (modal) ports, designed to ensure that no field is present at the port boundaries. As also reported in Section 3.2.2, lumped ports are not considered in this kind of analysis, due to the additional parasitics that they may introduce. Absorbing/radiation boundaries are imposed at lateral and top faces

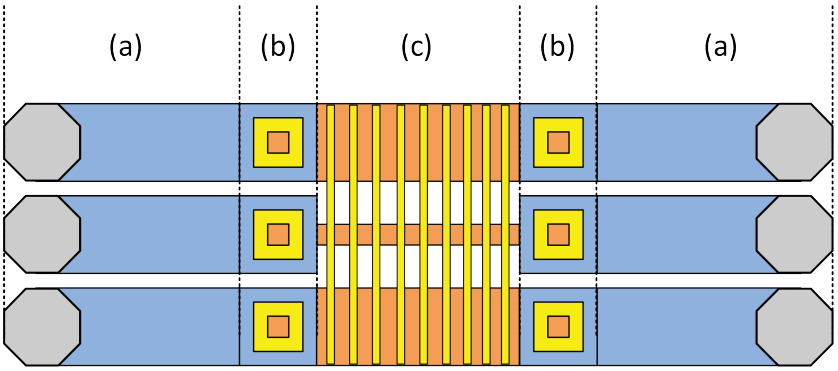


Figure 4.11: Simplified schematic top-view of a generic test-structure realized with CL-ICPW. a) Input section, b) M7-M1 vertical transition and c) DUT stage.

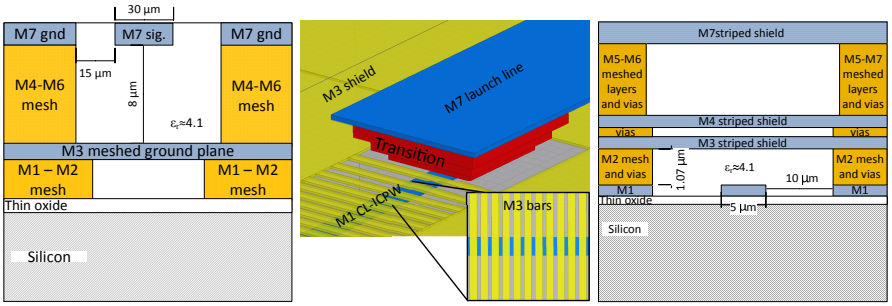


Figure 4.12: (a) Schematic cross section of the input stage used for the test structures.(b) 3D model of the vertical transition connecting the central conductor of the input stage in M7 to the CL-ICPW central conductor in M1.(c) Cross section of the CL-ICPW realized in the Infineon B11HFC technology to be used in the TRL de-embedding kit. The design features additional shielding levels to reduce the losses.

of the simulation box, which is defined horizontally by the dimensions of the simulated structure (length/width), vertically by the wavelength (λ/4 air gap at minimum simulation frequency surrounding the structure). The bottom face of the simulation box is defined as a perfect electric conductor. Material parameters and lateral dimension are set according to the nominal technology values. The S-parameters computed during simulation are re-normalized to the system impedance (i.e., 50 Ω) and used to compute the characteristic impedance.

4.4. TRL Calibration/de-embedding

The proposed set of structures can provide a direct calibration using the TRL algorithm. To benchmark the accuracy of the direct calibration at M1 level, we employ two techniques to extract the required characteristic impedance of the CL-ICPW

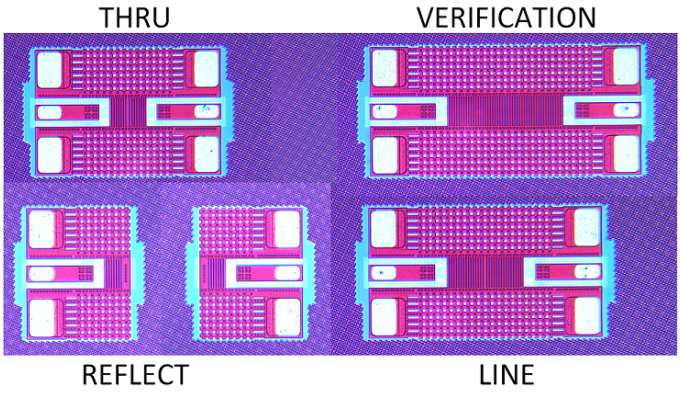


Figure 4.13: Micrograph of the de-embedding kit on Infineon B11HFC technology.

line, i.e. the calibration comparison method of [51] and the simulation based Z_0 extraction of [68], both introduced in Section 3.2.2. The measurements have been carried out on a precision semi-automatic probe-station to guarantee constant contact force and to minimize the probe landing misplacement among the measurements of different structures. First, a probe tip calibration has been performed using a TRL cal-kit designed on fused silica, and this calibration has been used as reference for the calibration comparison method. Then, the thru, reflect and line of the proposed de-embedding kit have been measured to perform both a direct TRL calibration (i.e., performing raw measurements of the standards) and a TRL de-embedding (using the probe tip calibration as reference). Figure 4.14 shows the characteristic impedance of the CL-ICPW as computed with EM simulations (squares) and using the calibration comparison method (circles). The plot highlights a strong frequency dependence of the Z_0 (for both real and imaginary part) when the calibration comparison method is employed, which can be attributed to the inductive transition between the pads and the CL-ICPW that is not accounted for by the method [53]. When considering the Z_0 of the intrinsic line, extraction using the EM method yields stable characteristic impedance, with small frequency dependence, validating the approach of the capacitive loading described in Section 4.2. The presented line is optimized for the WR03 frequency band (i.e., 220 GHz to 325 GHz). When a broader calibration band is targeted, more lines should be realized and a multi-line TRL calibration should be employed. The structures shown in Figure 4.13 can be either employed for direct calibration at the DUT plane, or for a second-tier calibration (de-embedding), following a first-tier probe-tip calibration performed on a separate substrate, to move the measurement reference plane from the probe-tips to the DUT reference plane. Although, in principle, the two procedures are equally adequate to obtain accurate measurements, the use of a direct DUT plane calibration may allow a reduction in the overall residual error. In order to compare the performances of direct and two-tier calibration procedures, the raw measurements of the thru, reflect and line standards have been used for both

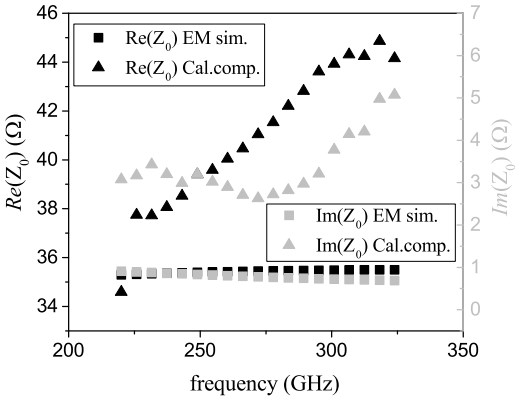


Figure 4.14: Real (left axes, black symbols) and imaginary (rigth axes, grey symbols) part of the characteristic impedance of the CL-ICPW realized in Section 4.3, as computed with EM simulations (squares) and using the calibration comparison method (triangles).

cases, where in the two-tier calibration the fused silica substrate has been used for the first-tier probe-tip calibration. In both cases, the characteristic impedance extracted using EM simulation has been used for the proper re-normalization of the S-parameters. Then, the method of [36] has been employed, defining the UB as in Equation 3.16. Figure 4.15 shows the results of the measurement comparison, where the upper bound of the error is plotted towards frequency for both direct calibration (asterisks) and de-embedding (filled squares). The plot shows a lower value for the error associated to the direct calibration (lower than 0.05 in the entire considered bandwidth) when compared to the de-embedding procedure. The reason for this is the error associated to the calibration transfer [43], as well as the possible errors propagating from the first tier calibration on fused silica (i.e., probe displacement, probe coupling, Z_0 uncertainty, etc.). It is important to mention that repeated measurements, characterized by 50 subsequent landings on a test DUT (transmission line) from the same calibration kit, in the same frequency range and employing the same setup, show a contact repeatability defined by a maximum standard deviation $\sigma = 0.06$. In the same frequency range, the system drift is always lower than 0.02 during at least 3 hours of repeated measurements.

4.5. Measurements of intrinsic devices on SiGe Technology

To demonstrate the proposed calibration/de-embedding method in its final application, measurements of a heterojunction bipolar transistor (HBT) featuring two emitter fingers with 5 µm length and 220 nm width were performed. The device was embedded into the test fixture employing CL-ICPW in common-emitter (CE) configuration directly at the calibration reference planes (i.e., at the center of the

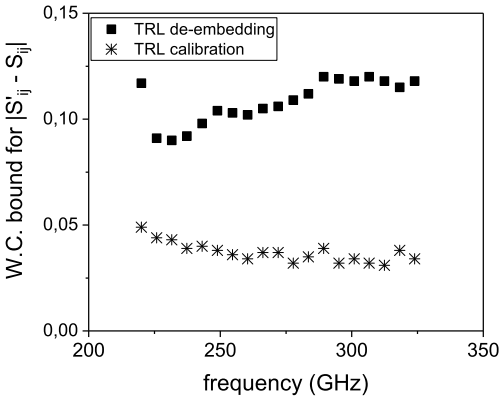


Figure 4.15: Comparison of the de-embedded measurement of the verification line manufactured on the Infineon B11HFC BEOL, in the frequency range 220-325 GHz.

thru line described in Section 4.3, shown in Figure 4.16. To guarantee proper connection between the CL-ICPW test and the structure modeled in the process design kit (PDK) (i.e., employing a p-type guard ring around the active device, with ground contacts connected to metal level 1) a small bridge at metal 2 (see, Figure 4.16b) was added. After calibration, EM simulations of these lines are used to de-embed them from the measurements. The device S-parameters have been measured using the direct calibration technique described in Section 4.4, in the frequency range from 220 to 325 GHz, using fixed bias conditions ensuring close to peak f_T, i.e., V_{CE} = 1.5 V and V_{BE} = 0.91 V. All S-parameters are referred to the system reference impedance, i.e., 50 Ω. The measurement results are compared to the S-parameters obtained by using the HICUM level 2 model of the device. Figure 4.17a shows the comparison of the magnitude in dB for all the S-parameters of the considered transistor. The measured values for S_{11} and S_{21} well fit the model prediction, with discrepancies in the order of 0.2 dB, while S_{22} shows a bigger error, with a maximum value in the order of 1.1 dB in the entire frequency range. The S_{12} parameter shows the biggest relative error in magnitude, due to its small absolute value. Discrepancies between measurements and model are more significant when considering the phase information (see, Figure 4.17b) where they can reach 40 degrees for S_{12}. The S-parameter measurement can be employed to compute the unilateral gain, as shown in Figure 4.18. The deviations between measured and modeled unilateral gain, in the displayed frequency range, correspond to those observed in the S-parameters and may partially be explained by missing substrate coupling and inaccurate parasitic capacitances in the model. It is important to note that no cross-talk correction has been applied to these measurements, while increased measurement accuracy could be reached when applying the technique as in [77]. This comparison shows the importance of accurate transistor parameter extraction for applications at very high frequencies. Nevertheless, the trend of the modeled

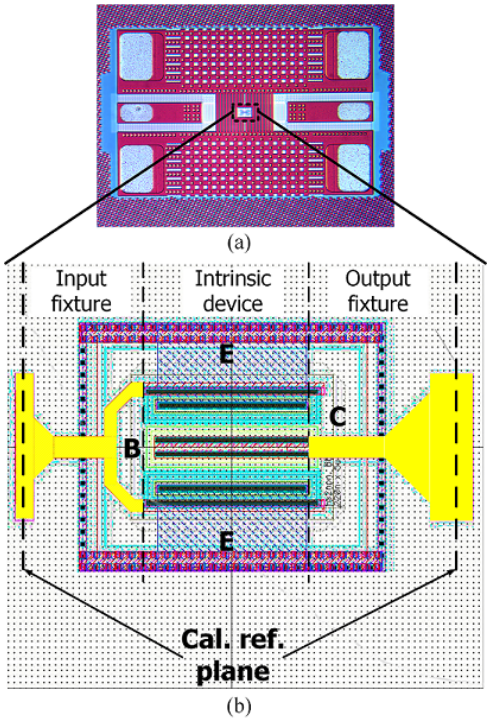


Figure 4.16: a) Top view of the transistor integrated into the test-structure. b) Detailed view on the layout for the integrated transistor, highlighting the input and output fixture (in yellow) required to guarantee correct connection to the intrinsic device. The base, collector and emitter contact (B, C and E, respectively) are marked on the layout.

frequency dependence matches that of the measurements. Although further comparison between the proposed method and conventional de-embedding methods is needed, together with a thorough investigation on the small-signal model parameters in the (sub)mm-wave range, Figure 4.17 represent the first promising example of measurements versus model data at frequencies as high as 325 GHz.

4.6. Conclusions

In this chapter, we have presented the capacitively loaded inverted CPW (CL-ICPW) as a novel transmission line design that can be employed for TRL de-embedding in silicon technology BEOL. The peculiar structure of the CL-ICPW allows access to structures embedded in low metal layers (i.e., up to level 1) by confining the electromagnetic field in the upper low-loss dielectric layer, thus avoiding propagation in the dispersive semi-conductive substrate. The characteristic impedance of the line can be extracted by means of EM simulations, overcoming the challenges associated to characteristic impedance measurement in highly inductive fixtures. A de-embedding kit has been manufactured in SiGe BEOL, and used for direct VNA

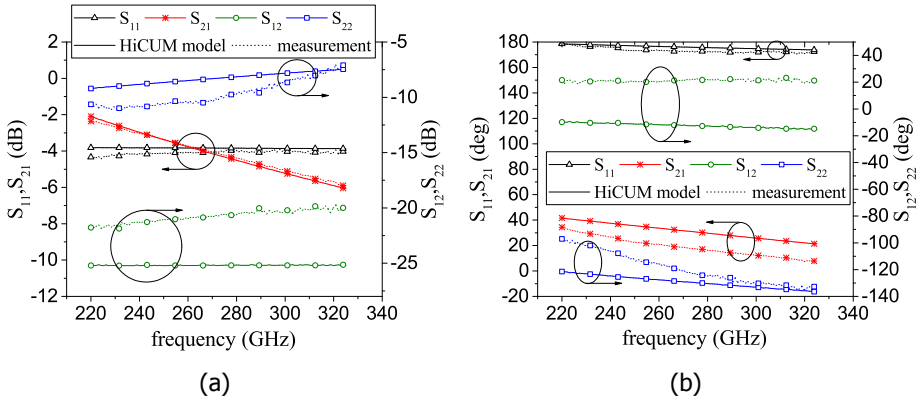


Figure 4.17: S-parameter measurements (dotted lines) versus model of the considered IFX transistor (solid lines) for both a) amplitude (in dB) and b) phase (in degrees).

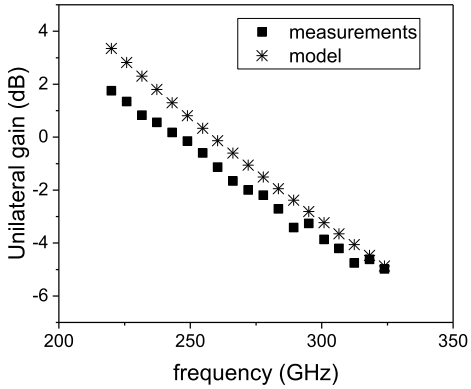


Figure 4.18: Unilateral gain obtained from measurements of the considered device using VCE = 1.5 V and VBE = 0.91V.

calibration, and the accuracy of the calibration has been benchmarked by measuring transmission lines and comparing the measurements with simulation data. This approach allows fixing the calibration reference plane as close as possible to the DUT, avoiding multi-tier process and thus the propagation of systematic errors through subsequent calibration steps. The capability of the proposed calibration approach to perform direct measurement of close-to-intrinsic transistors has been demonstrated, allowing performing device model validation at mm-wave and with a fully-distributed approach.

5

60 GHz mixed signal active load-pull system for millimeter wave devices characterization

The characterization of active devices (i.e., transistors) and circuits (PA) typically requires, on top of accurate small-signal measurements, also the capability to test the DUT for its large signal performance. At microwave frequencies, this is usually done by using *load-pull* measurements. Load-pull is the measurement technique in which the loading conditions offered to a DUT are varied while its large signal characteristics are measured [78]. This is typically accomplished either by employing passive impedance tuners in close proximity to the DUT (*passive* load-pull), or by properly injecting a signal into the output port of the DUT, synthesizing in this way an arbitrary load (*active* load-pull). First section of this chapter will be dedicated to a brief introduction to load-pull techniques, with focus on active implementation. For a thorough review the reader is referred to [21]. Then, the main challenges at mm-wave frequencies will be presented, with an example of the state-of-the-art for millimeter wave active load-pull techniques. The focus of the chapter will then shift to waveguide-based implementation, describing the main advantages in respect to coaxial based implementation at frequencies higher than 50 GHz. Finally, a novel implementation, based on a mixed-signal approach, will be presented, together with a series of examples of practical applications in the field of millimeter wave device and circuit characterization.

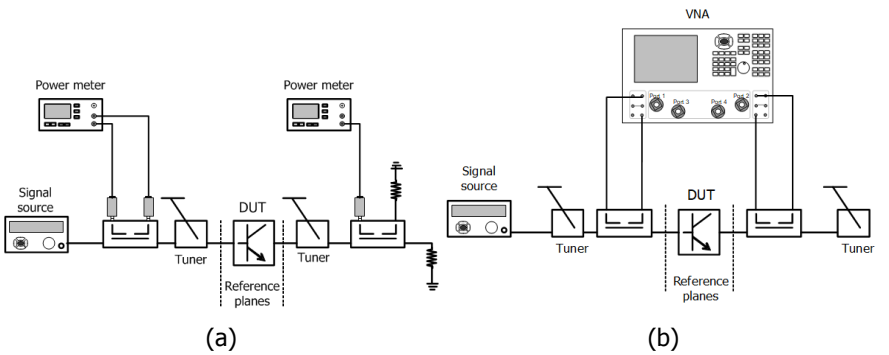


Figure 5.1: a) Conventional schematic implementation of a passive load-pull setup, with the tuners placed in close-proximity to the DUT. b) Real-time implementation of a passive load-pull setup, with a reflectometer placed between the tuner and the DUT.

5.1. Conventional load-pull techniques

Passive load-pull techniques are based on the use of *impedance tuners*, passive devices that can be used to present a predetermined load termination to a DUT. Tuners may differ in their mechanical implementation, but in the most common and essential case they are based on the use of slide-screw tuners, where a reactive probe (*slug*) is used to change the loading conditions by sliding along an airline [79]. Impedance tuners can be manual or automated, and used in different system implementations, at both the input (source-pull) or the output (load-pull) of the DUT. Passive load-pull setup can be divided in two main architectural families: *conventional* (or *non-real-time*) where the tuner is placed as close as possible to the DUT (see, Figure 5.1a), and *real-time*, where a reflectometer is placed between the tuner and the DUT (see, Figure 5.1b). The first implementation has the advantages of minimizing the losses and the electrical distance between the tuner and the DUT, while the latter allows to have the tuner excluded from the calibration path of the system, so that the system can be accurately calibrated and the load-condition presented to the DUT can be directly measured using the reflectometers and a VNA (while, in the conventional case, the tuner needs to be pre-characterized). The main disadvantages related to passive load-pull architectures typically lie in the relatively high time cost associated to the realization of a determined load (due to the inevitable time needed for mechanical tuners to change the value of the presented load) and the constraints on the reflection coefficient magnitude at the load reference plane (mostly limited by the losses in the interconnection between the tuners and the DUT) [21]. These challenges can be both circumvented, if the phase and the amplitude of the wave injected into the DUT output port (i.e., $\boldsymbol{a_2}$) can be arbitrarily controlled to realize the desired load coefficient Γ_L. Being Γ_L the frequency domain ratio between waves (a_2 and b_2), the main condition required to be able to artificially synthesize any chosen load coefficient is that a_2 (which is artificially injected in the DUT output) and b_2 (which is mostly determined by the DUT output) are *coherent* in phase, i.e., they share the same phase reference. If that's not

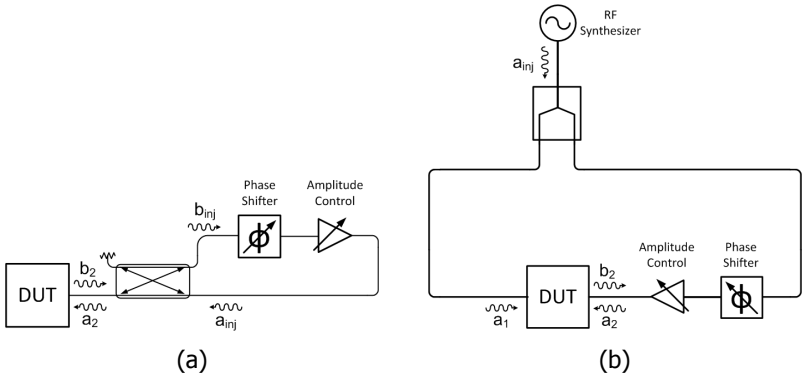


Figure 5.2: a) Simplified schematic representation of the active tuning part of a closed-loop active load-pull; b) simplified schematic representation of the active tuning part of an open-loop active load pull.

the case, the relative phase between a_2 and b_2 would have a contribution which is continuously varying, thus preventing the possibility of predetermining the phase of the ratio Γ_L. In this perspective, two ways exist to guarantee phase coherence between a_2 and b_2:

- a_2 is a (modulated) replica of b_2;
- a_2 shares the same signal source as a_1, assuming that the DUT doesn't introduce any random phase change in the transmitted signal.

The first case defines the main characteristic of a closed-loop active load-pull (see, Figure 5.2a for a schematic representation), the second instead represents the working principle of an open-loop active load-pull (see, Figure 5.2b for a schematic representation). For a complete review of the features and characteristics of the two main implementations of active load-pull, the reader is encouraged to read [21]. To complete and support the rest of this chapter, before analyzing millimeter wave load-pull techniques, one of the most important open load-pull techniques will be described: the mixed-signal active load-pull [80].

5.1.1. Mixed-signal active load-pull

The mixed-signal active load-pull is an open-loop technique first introduced in [80]. The main goal of the technique is to allow flexibility when using the system for the measurement of devices under realistic signal condition, i.e., modulated signals. As a matter of fact, the technique exploits the properties of IQ mixers to couple conventional microwave techniques with low-frequency signal generation and digital data processing. A simplified schematic of a mixed signal active load-pull setup is presented in Figure 5.3. The architecture presents a reflectometric configuration in close proximity to the DUT, where the scattered waves are sampled in a similar way as in a VNA. The waves are then down-converted by means of fundamental mixers to an IF frequency, and then acquired using broadband analog to digital converters

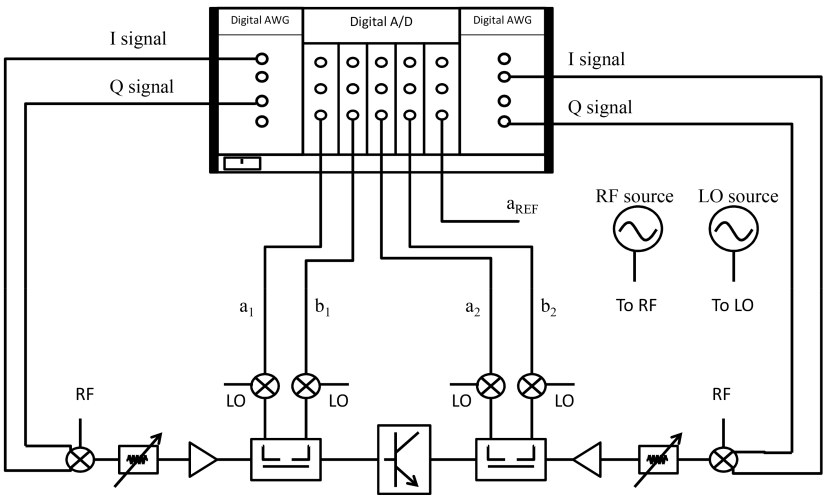


Figure 5.3: Simplified schematic describing the main elements of the architecture of a mixed signal active load-pull setup

(ADC). The acquired waves can then be used in the digital domain for all the required data processing, including calibration. At the input of the reflectometers, at both port 1 and port 2, IQ mixers are present, typically followed by variable attenuators and amplifiers needed to maximize the dynamic range of the system. The IQ mixers share the same LO signal, which is provided by means of a synthesizer. In-phase and quadrature signals are provided to both IQ mixers by means of broadband analog waveform generator (AWG). The IQ signals, can be either DC (in case of single tone measurements) or multitone, depending on the kind of measurement required. In this sense, the IQ mixer provides the *up-conversion* capabilities for waveform generated with the AWG from baseband to the carrier set by the RF synthesizer. In case harmonic measurements are needed, multiple up-conversion paths would be needed, in order to allow the independent load control for each of the harmonics. Harmonic loops are not reported in Figure 5.3 for simplicity. The system is first calibrated using a conventional S-parameter calibration technique (like SOLT, SOLR, LRM, TRL, etc.), then a power calibration is performed.These two steps are followed by a power-offset calibration, which allows to identify the set of I and Q combinations needed to deliver a specified power to the DUT. In case of multi-tone measurements, an additional phase calibration is also needed. When performing load-pull measurements, the system requires an iterative algorithm to allow convergence to the required load condition. In case of multi-tone/modulated signals, the use of ADCs for the acquisition, the digital elaboration of the data, and AWGs for the signal generation, allows to quickly define the loading condition for each tone of interest, and this capability defines the mixed-signal approach.

5.2. Millimeter wave active load-pull

The limitations of passive techniques for load-pull measurements described in Section 5.1, are typically worsened when considering millimeter wave frequencies. As a matter of fact, despite the capability of passive tuners of presenting at their test-port high mismatch condition, the losses associated to the interconnection may compromise the maximum load presented to the DUT. If we consider a simple on wafer system, where the (coaxially connectorized) tuner is connected to the wafer probe by means of a cable, the insertion losses can easily reach 1-2 dB at 60 GHz. Assuming, for example, an ideal value of $\Gamma_L = 1$ at the tuner test port, 1 dB loss would degrade it to 0.8, while a 2 dB loss would provoke a reflection coefficient around 0.63. Things are even more complicated when *real-time* systems are involved, having also the reflectometer between the DUT and the tuner (see, Figure 5.1b). In this case, the losses of the employed couplers would add-up to have an even lower reflection coefficient at the DUT. For these reasons, passive tuner based techniques at millimeter wave typically present maximum loading condition at the DUT in the order of 0.5 - 0.6 in magnitude of Γ [81–85]. Moreover, the "electrical distance" between the tuning element and the DUT would increase with frequency, provoking an error in the definition of the correct phase of the loading condition presented to the DUT during the measurements. On the other end, the implementation of active techniques may present challenges at millimeter waves, mostly due to the scarce availability of components. For closed-loop systems, in particular, electronically controlled phase shifters and narrowband filters are difficult to find and relatively expensive, while in general there is a trade-off for power amplifiers between broadband capabilities, linearity and available power. Few examples of active load-pull systems at mm-wave exist in literature [86, 87]. In [86] an open-loop technique was employed, based on the use of 6-port reflectometers, and a variable attenuator together with a variable phase shifter for the active tuning. As the system does not allow for independent control of the power delivered at the input and the output of the DUT, the intrinsic limitation of the setup is related to the capability of performing power sweeps during measurements. The system of [87] is instead a closed-loop system for the measurement of devices at 94 GHz. In this case, the limitations related to closed-loop systems are circumvented by implementing a down-converted loop for the load-optimization. A simplified schematic of the implementation is depicted in Figure 5.4. The load optimization is performed as follows: the b_2 wave is coupled by the coupler C2 at the output of the DUT and then fed to the fundamental mixer M5. M5 allows for the downconversion of the signal from 94 GHz to 9.6 GHz, by using an independent signal at 84.4 GHz on its LO terminal. The down-converted signal can be then more easily filtered, phase shifted and conditioned to synthesize the desired load condition. The tuning signal is then up-converted again to 94 GHz using mixer M6, and finally filtered and amplified before being provided to the output of the DUT. The measurement is then performed using coupler C1 and C4 for the separation of the scattered waves, and a VNA for the acquisition after proper down-conversion to intermediate frequencies using mixers M1-M4. The closed-loop nature of the system allows for easily sweeping the power at the input of the DUT, while the loading condition remains

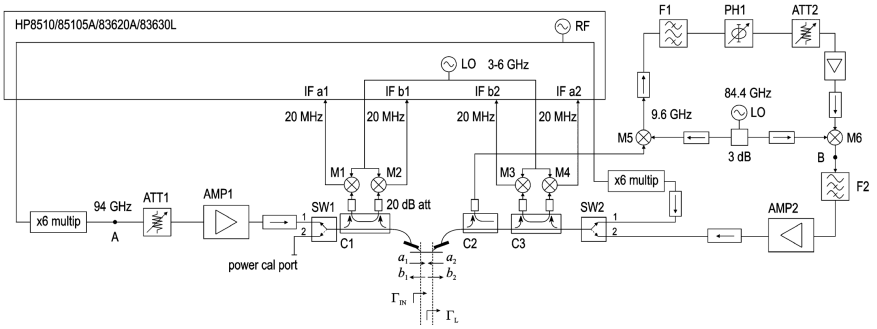


Figure 5.4: Simplified schematic of the closed loop architecture described in [87]

fixed. The system in [87] was only presented for operation at 94 GHz, while broadband capabilities are in principle possible depending on the availability of the loop amplifiers. However, neither the system of [86] or the one of [87] allows, in any case, load-pull under multi-tone conditions. In this chapter the focus is posed on the use of open loop techniques at millimeter waves, specifically mixer-signal active load pull in the WR-15 waveguide bandwidth (50 - 75 GHz). Before describing the architecture and performances of the considered setup, first general considerations on the accuracy and the power capabilities of millimeter wave setups are discussed in Section 5.3, to justify some of the design choices.

5.3. Waveguide based test-set

Conventional mm-wave test benches, both small-signal as well as large-signal, are constrained by the large losses provided by the coaxial interconnections at these frequencies. Large signal setups typically share, at least partially, the same front-end of small-signal setups (i.e., VNA), including reflectometers in proximity of the test-ports. This front-end is commonly referred to as *test-set*, and also in large signal setups an initial calibration is needed to correct for the errors introduced by the test-sets, with basically the same procedures as the one used for VNA measurements. For active load-pull setups, it is important to investigate the impact of the test-set losses on two aspects:

- The accuracy and stability of the calibration
- The capability to provide high reflection conditions to mismatched devices.

In this section three different test-cases will be considered:

Topology 1 *Waveguide test-set*, the entire front-end of the test-bench is realized using rectangular waveguides and a mixed-signal approach is used for the signal generation and acquisition, see Figure 5.5a. Signal distribution for the LO signals needed for the down-conversion of the coupled waves is done by means of coaxial cables at lower frequencies (i.e., 16-22 GHz), while the signal is up-converted by means of a x3 multiplier directly at the LO mixer port.

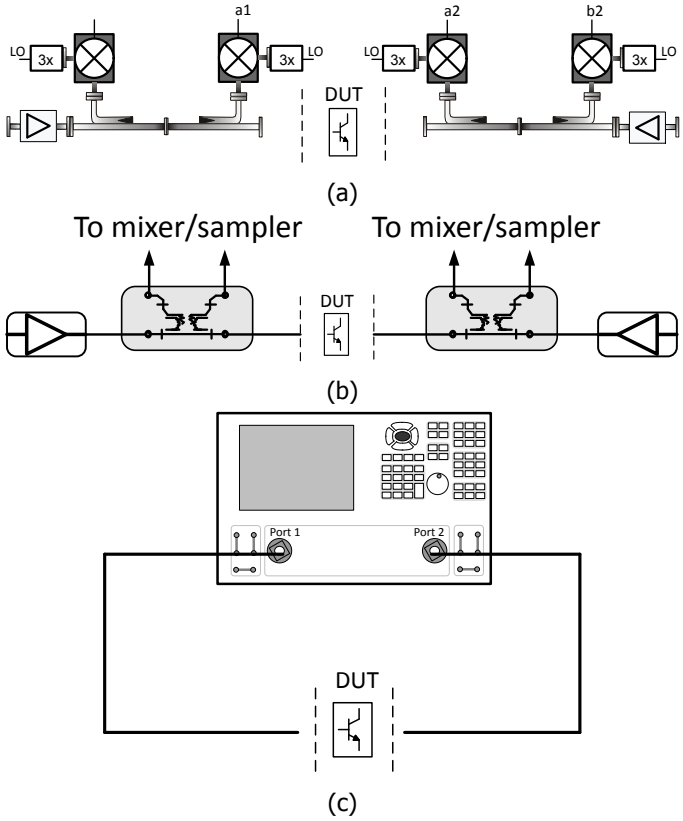


Figure 5.5: Test-benches front end for stability and power driving capability comparisons, a) "waveguide test-set" –this work-, b) "VNA with external test-set", c) "VNA-internal setup".

Topology 2 *VNA with external coaxial test-set*, external amplifiers and coaxial couplers are used in close proximity to the DUT, operating directly at the measurement frequency, see Figure 5.5b.

Topology 3 *VNA-internal setup*, the internal instrument sources and reflectometers are used, see Figure 5.5c.

5.3.1. Measurement stability

In order to properly compare the performances of the different test-sets we need to assess their stability and their power handling. To do that, we consider the nominal performance of the components constituting the test-sets, i.e., coaxial or waveguide cables and couplers, as reported in Table 5.1 for commercially available equipment. These values are used in circuit-level simulation, as shown in Figure 5.6, which represents the input of a virtual 2 port test-set (i.e., topology 1 and 2, in the above list). The schematic can be used to first assess the virtual system

Table 5.1: Waveguide vs. coaxial connectiond and couplers performances

Nominal component performance @60 GHz			
Component	**Insertion loss**	**Directivity**	**VSWR**
Coaxial 1.85 mm	6 dB/m [88]	-	1.26
WR-15	1.4 - 1.7 dB/m [89]	-	1.07
Coaxial coupler	3.2 dB [90]	8 dB	1.9
WG coupler	2 dB [91]	40 dB	1.2

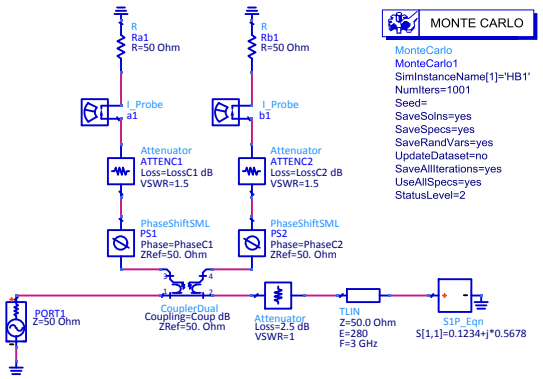


Figure 5.6: Virtual test-set in Agilent ADS for waveguide to coaxial performance comparison.

raw performance, i.e., the error terms associated with the system. This is possible by simulating an ideal SOLT calibration (i.e., with no errors in the definition of the calibration standards). The error terms resulting from this simulation are summarized in Table 5.2. While error terms do not directly impact the measurements (if error terms can be estimated by calibration, they can as well be properly corrected mathematically), they can play a role in the propagation of the system noise to the final measurement. In order to estimate this impact, the evaluated error terms are employed in a Montecarlo simulation. First, the repeatability associated to cable movements is evaluated by experimental VNA measurements. To do that raw reflection coefficient measurements were realized, in a temperature controlled lab environment, using a flexible 1.85 mm cable connected to a matched load, and applying a fixed movement of 5 mm to the cable every 5 minutes (mimicking the cable movements due to probe positioning). Using this setup, 100 repeated measurements were performed in two frequency ranges, 16.6-21.6 GHz (i.e., the frequency range in which cables would be employed in the topology of Figure 5.5a) and 50-65 GHz (i.e., the frequency in which cables would be employed in the topology of Figure 5.5b). The standard deviation (in magnitude and phase) extracted from these measurements represent the mere repeatability error associated to the cables, which in this case was $|\sigma_{LF}|_{\text{dB}} = 0.018$ dB and $\angle\sigma_{LF} = 0.143°$ for the lower

Table 5.2: Simulated calibration error terms for coaxial and waveguide reflectometer front-ends

Topology	ed (dB)	es (dB)	et (dB)
Coaxial	-8	-13.9	-10.75
WG (simulated)	-40	-23.7	-5.5
WG (measured)	-31.4	-27	-4

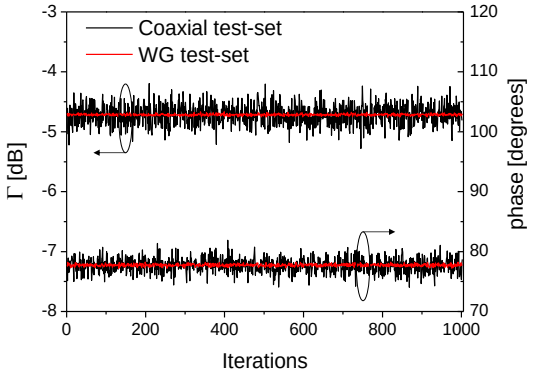


Figure 5.7: Montecarlo simulation of the impact of measurement fluctuations due to the use of coaxial reflectometers front end in amplitude and phase compared to a waveguide based architecture.

frequency range, and $|\sigma_{HF}|_{\text{dB}}$ = 0.08 dB and $\angle\sigma_{HF}$ = 0.57° for the higher frequency range. In order to "propagate" the stability of the cables to the measurement stability, the results of the repeatability measurements were employed in the virtual test-set of Figure 5.6, for the two different topologies, by introducing the cable repeatability as a statistical error and then performing a Montecarlo simulation of the entire test-set. In the simulation, the test-sets are terminated with an arbitrary load, set as $\Gamma_L = 0.1234 + j5678$. This value is estimated, by means of ideal SOL calibration, while the statistical noise on the cables is added, for 1001 independent iterations for each of the considered topologies. Figure 5.7 shows the results of the simulation, which can be summarized with a standard deviation, on the corrected measurement, of 0.174 dB in amplitude and 1.22° in phase for the coaxial configuration, versus 0.015 dB in amplitude and 0.193° in phase when the waveguide configuration is considered, highlighting the improved stability performance that can be achieve using a waveguide test-set. These numbers refer to the errors due only to the reflectometers front-end, all the other independent sources of error are not considered in this analysis. As the uncertainty for a certain loading condition Γ ultimately depends also on the value of Γ, a more system-level analysis would require to propagate the uncertainty to the calibration error terms, as these would be independent of the considered loading condition. Such analysis has not been performed in this dissertation, but has been considered for the further analy-

sis of waveguide based load-pull setup currently in place. The analysis presented in this section represents a qualitative indication of the improvement, in terms of uncertainty, which can be provided by using waveguide based test-sets for active load-pull measurements.

5.3.2. Driving power capability

As can be seen from the data in Table 5.1, a coaxial implementation of the test-set can also be associated to higher losses. Since the saturated power of commercially available instrumentation amplifiers is limited to 22 dBm, these losses directly imply a reduction of the power available at the test-port, i.e., the power associated to the a_2 wave injected into the output of the DUT. This means that the reflection coefficient that can be provided (during active load-pull measurements) to the DUT will be also limited. It is possible to calculate, for a realistic DUT, what would be the maximum loading condition achievable by the three topologies previously considered, by using equation 3.4 from [92]:

$$P_{a2} = P_{b2} \cdot \frac{(1 - |\Gamma_{DUT}|^2)}{(1 - |\Gamma_{SYS}|^2)} \cdot \frac{|Z_{DUT} + Z_0|^2}{|Z_{SYS} + Z_0|^2} \cdot \frac{|Z_L + Z_{SYS}|^2}{|Z_{DUT} + Z_L|^2} \tag{5.1}$$

Where P_{a2} is the injection power at the test port, P_{b2} is the output power of the DUT, Z_{DUT} and Γ_{DUT} are output impedance and reflection coefficient of the DUT, Z_{SYS} and Γ_{SYS} are the impedance and reflection coefficient offered by the system, Z_0 is the renormalization impedance, and Z_L is the targeted load impedance. To perform this comparison, we considered the output impedance and the power provided by a device implemented in a commercially available SiGe technology, i.e., DUT Z_{out} equal to 2.25 Ohm and P_{SAT} 9 dBm, and finally estimated the injection power (Pav from the amplifier) required to achieve a certain loading condition at the DUT reference plane. Figure 5.8 shows that only using an external waveguide test-set a sufficiently high reflection coefficient ($|\Gamma_{L1}| = 0.98$) can be offered to realistic (mismatched) power cells.

5.4. System configuration

The waveguide concept introduced in the previous section can be conveniently coupled with a mixed-signal approach [80]. In Figure 5.9 the simplified schematic of the proposed system is shown. The RF signal, employed for the signal injection, is provided by a low frequency signal generator (up to 20 GHz) followed by a times-four (x4) waveguide multiplier. The RF signal is then split using a waveguide magic tee (see, Figure 5.10a), which provides low insertion loss (i.e. lower than 1 dB at 60 GHz) and high isolation between the two output branches. The use of the multiplier allows to reduce the system overall cost, avoiding the use of mm-wave frequency synthesizers. In both branches (i.e., input and output) an IQ mixer is placed to modulate the injection. After the mixer, an attenuator is employed to optimize the matching with the following power amplifier and increase the dynamic range of the generated signal, by maximizing the voltage swing at the IF ports of the mixer, for a given (mm-wave) power level. At the end of the signal injection

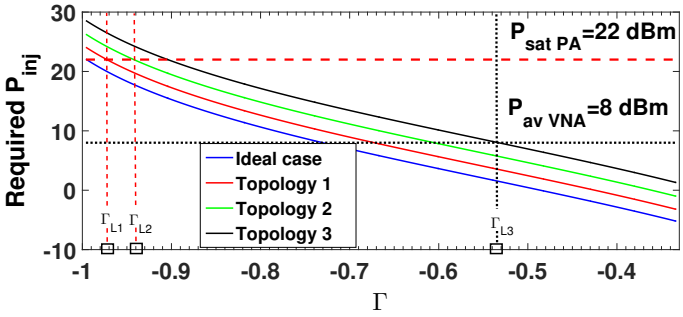


Figure 5.8: Injection power required versus Γ, for a 2.25 Ohm output impedance device with 9 dBm saturated power for the three considered topologies (Red for the WG-based topology #1, green for the topology using VNA and external test-set #2, purple for the topology using the VNA internal test-set #3). The horizontal lines represent the maxmium power available when using a mm-wave instrumentation amplifier (red dash) and the output power from conventional VNAs (black dots). The intersection between the horizontal lines (available power) and the requested injection power, allow to identify what is the maximum achievable mismatched condition using the specified configuration, $\Gamma_{L1} = 0.98$, $\Gamma_{L2} = 0.94$, $\Gamma_{L3} = 0.54$

chain, PAs are employed to guarantee sufficient DUT driving signal and injected signal levels (i.e., 13 dBm input and 22 dBm output). At both the input and the output of the DUT, two bi-directional waveguide couplers (Figures 5.10b and 5.10c) are used as reflectometers, to couple the incident and reflected waves, providing "real-time" measurement capability to the system. The coupled waves are down-converted by means of fundamental mixers. The LO distribution path for the mixers down-conversion is composed by a LO signal generator with a maximum frequency of 26.5 GHz, multiplied by a times-three (x3) waveguide multiplier. Also in this case a lower frequency synthesizer together with the use of multipliers allows to reduce the costs, simplifies the LO distribution path and improves the test-set stability when compared to fundamentally operating coaxial cables, as was shown in Section 5.3. This configuration also avoids the use of mm-wave power splitters and – most importantly – the need of expensive mm-wave PAs. The resulting IF signals are acquired with broadband ADC converters (i.e., 40 MHz). For the IQ generation as well as for the baseband acquisition two NI PXIe-7965R cards with NI 5781 adapter modules, integrating both a 16 bit DAC and a 14 bit ADC, are employed. These cards feature Xilinx Virtex V FPGA modules, making them an extremely flexible tool for both signal generation and acquisition.

5.4.1. Schematic optimization

The signal detection path (coupler-mixer configuration) described in Section 5.4 was at first optimized for small device sizes. However, for increased power levels, this configuration presents down-conversion mixer compression starting from P_{in} of circa -10 dBm as shown in Figure 5.11a. To modify the power handling capability of the system and allow load-pull optimization on power device cells (i.e., higher than 1 mW), attenuators are required on the coupled arms. To avoid the need of costly

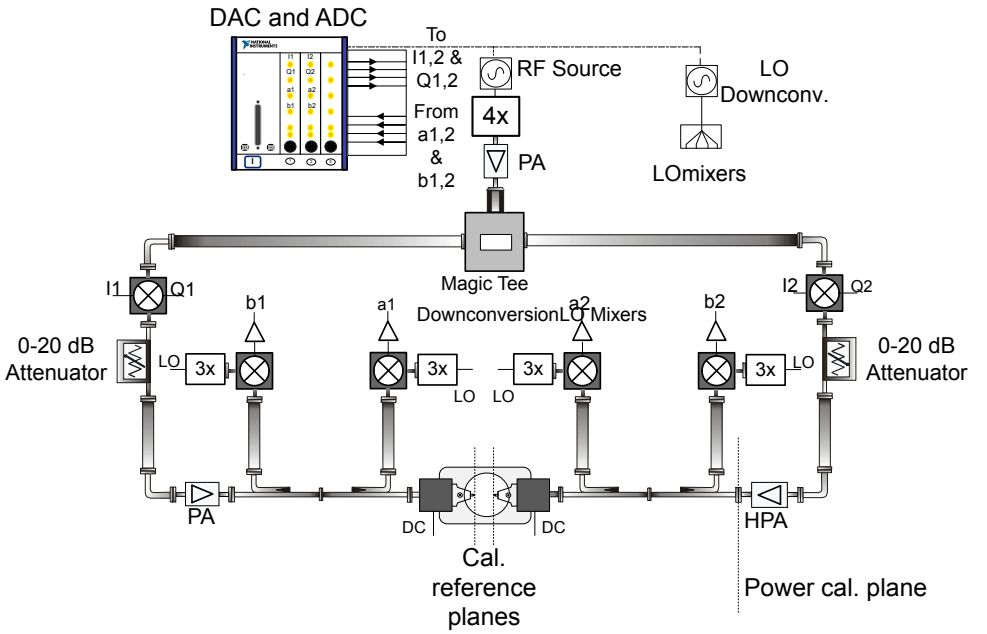
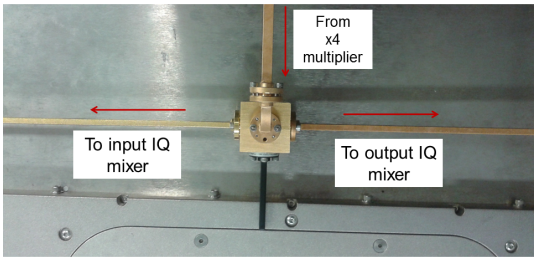


Figure 5.9: Simplified system block diagram of the waveguide based mixed-signal active load-pull.

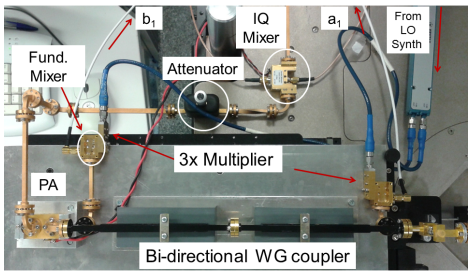
waveguide attenuators, which would also alter the waveguide mechanical setup (due to the extra weight of the component and different size/volume), custom fixed attenuators were implemented by inserting short sections of absorbing material into WR-15 waveguide bends (see, Figure 5.12a). This simple technique allows to achieve full-band attenuators (approx. 17 dB for the attenuators on the input section and approx. 24 dB for the ones on output section, see Figure 5.12b), without mechanically loading the coupler arm. When optimizing the power level at the mixer, the proper system performance (i.e., gain on a calibration thru) is measured up to P_{IN} levels of about 13 dBm (see Figure 5.11b). It is worth noticing that using different attenuators on the coupled arms represents a compromise between dynamic range optimization, speed and calibration stability. As a matter of fact, having balanced reflectometer branches allows maximizing the calibration accuracy, while the proposed unbalancing guarantees the maximum dynamic range at both input and output port. An alternative could be to use the same attenuation on all branches, in this case 24 dB, in order to guarantee linearity at both ports. In this case, to optimize the dynamic range, it would be needed to reduce the IF bandwidth of the detection, affecting the measurement speed.

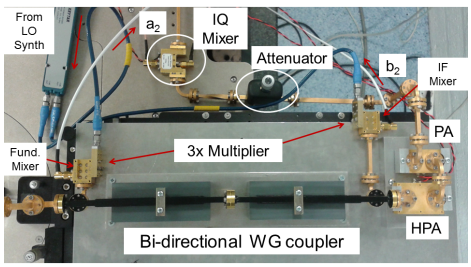
5.5. System operation

The primary purpose of the proposed waveguide mm-wave mixed-signal load-pull system is to perform large signal characterization of mm-wave devices for compact model development and validation, under CW and digitally modulated excitation.



(a)

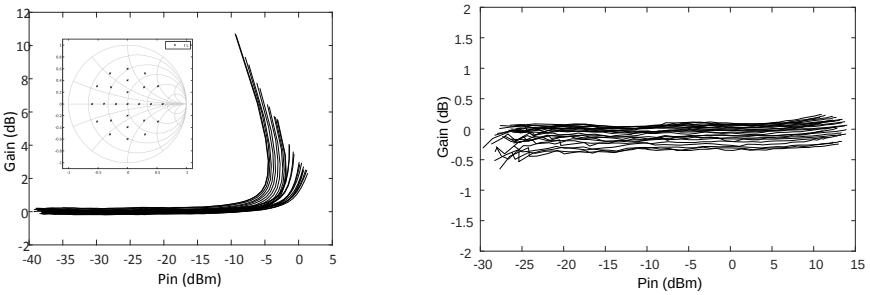




(b) (c)

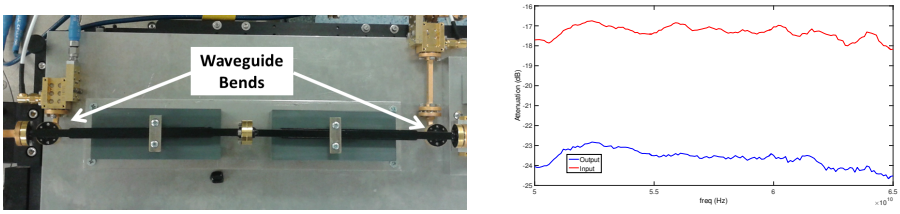
Figure 5.10: Pictures of (a) magic Tee for up-converting RF signal splitting, (b) Input injection signal up-conversion chain and coupled a_1 and b_1 down-conversion chain for the proposed system, and (c) Output injection signal up-conversion chain and coupled a_2 and b_2 down-conversion chain for the proposed system.

The mixed-signal open-loop configuration allows to generate any user-defined reflection coefficient versus frequency (at both the input and output of the device) by controlling the injected signals. The injected waves are obtained by successive iterations, monitoring the frequency dependent required reflection coefficient [80]. The high dynamic range of the generated signal together with the accurate detection of the reflection coefficient presented at the DUT reference plane, obtained with the proposed waveguide test-set, allows achieving accurate load-pull data for compact model validation and development.



(a) (b)

Figure 5.11: Measured values showing the effect of down-conversion mixer compression on the measured gain of a thru standard at 55 GHz (a) with no attenuation on the coupler arms and (b) after the insertion of the attenuators. Inset showing the different loading conditions used for the measurement.



(a) (b)

Figure 5.12: (a) Picture from the output reflectometer of the load-pull setup, with the modified waveguide bends. (b) Measured values of attenuation for custom fixed full-band attenuators realized inserting short sections of absorbing material into the WR-15 waveguide bends.

5.6. System performances

5.6.1. Impedance control

To test the capabilities of the proposed setup of actually controlling the load impedance offered to a DUT, first an impedance control over the entire Smith chart was performed in the operating band of the system (i.e., 50-65 GHz). Figure 5.13a reports the controlled loading conditions (i.e., measured impedances) provided at the calibration reference plane at 60 GHz on a waveguide thru. Another test was performed setting a constant reflection coefficient of -0.95 while providing an input power sweep from 2 to 11 dBm (see, Figure 5.13b). To demonstrate the load impedance control versus power and versus frequency (depending only on the averaging value and the setting on the convergence algorithm), Figure 5.13b shows Γ_L at the calibration reference plane versus the injected power level (frequency fixed at 60 GHz) while Figure 5.13c shows Γ_L versus the operating frequency (power fixed at 10 dBm). Figure 5.13c shows a Γ control versus frequency which is always better than 0.006 for frequencies below 60 GHz, while it increases to 0.04 for frequencies between 60 and 65 GHz. The loss in performance above 60 GHz can be associated to

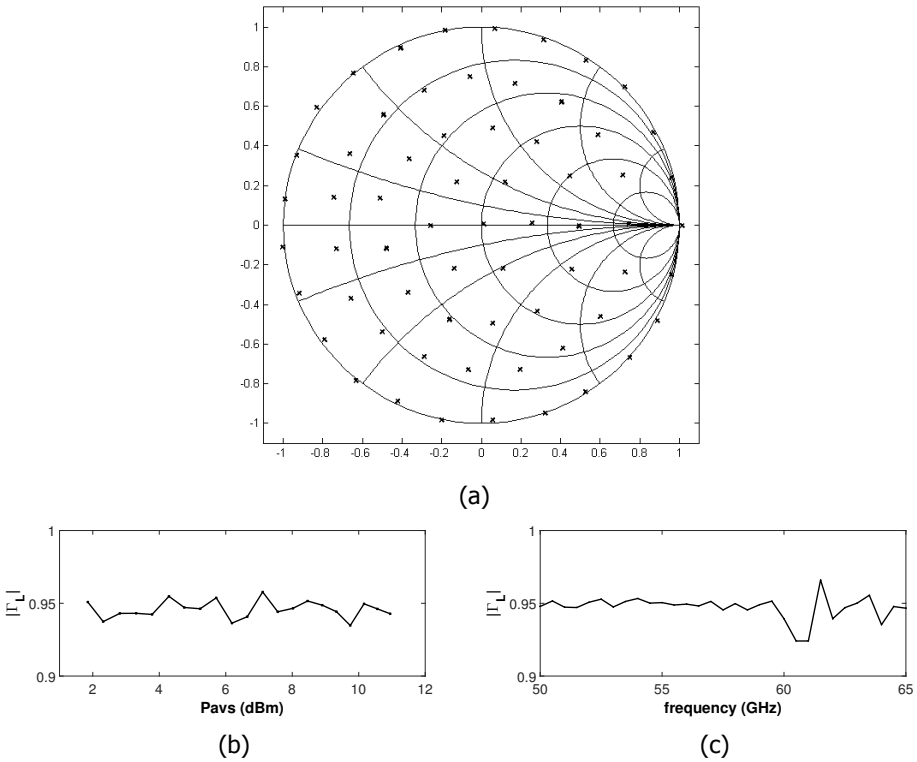


Figure 5.13: Control of impedance value presented to the load, on a thru standard, (a) on the entire Smith Chart at 60 GHz, (b) versus the available power, for a set -0.95 Γ_L value at 60 GHz and (c) versus frequency with a fixed power of 10 dBm.

a non-optimized LO distribution, in which some components are used out-of-spec in part of the bandwidth. This will affect the LO signal, thus the accuracy of the system, when measuring at frequencies from 57 to 65 GHz (i.e., in the LO distribution chain, from 18 to 21.67 GHz).

5.6.2. Stability

The use of waveguide components in the test-set allows to achieve better raw performances when compared with their coaxial counterparts, as was numerically shown in Section 5.3.1. Table 5.2 reports the comparison between the error terms of a general waveguide test-set (simulated data based on component data-sheet values) and actual error terms obtained after calibrating the proposed waveguide based active load-pull setup at 60 GHz. In this section we present experimental data on the stability of the proposed setup. The system was first calibrated, for S-parameters, at the probe tips (i.e., Cascade Infinity waveguide i75 125 GSG) using an impedance standard substrate (ISS) 101-190C from Cascade. Afterwards, an absolute power calibration [93] (performed at the Power cal. plane in Figure 5.9)

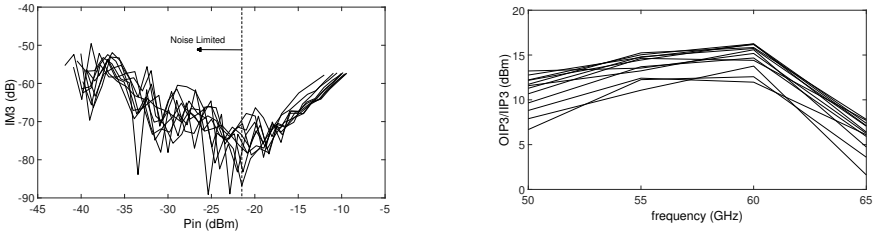
Table 5.3: Measured power gain maximum standard deviation

Frequency (GHz)	50	55	60	65
Standard deviation (rel. - %)	1.47	0.48	0.38	0.92

and power leveling were carried out. A load-pull measurement was performed on a thru standard from the same calibration substrate to evaluate the calibrated power gain. The measurement was performed for 5 different loading conditions (Γ = 0, 0.5, -0.5, 0.5i, -0.5i), at four operating frequencies (50 GHz, 55 GHz, 60 GHz, 65 GHz) over an input power ranging from -10dBm to 10dBm. The standard deviation (STD) of the power Gain on the thru, which provides some information on the stability of the calibration, was obtained, in a temperature controlled lab environment (21°±1° Celsius), repeating the measurements periodically, at each frequency, for 36 hours. For each measured frequency, the maximum of the acquired standard deviation among the different loading conditions is reported in Table 5.3. The analysis reveals an overall maximum standard deviation of 1.47% at 50GHz and an average STD in the entire system bandwidth of 0.48%.

5.6.3. Two tones

The proposed system is also designed to perform two-tones measurements for device linearity characterization. When characterizing the linearity performances of a DUT, it is crucial to achieve a highly linear driving signal. A good rule of thumb for the required drive signal is to aim at an IM_3 level (in dBc) comparable to the system dynamic range, in our case around 60 dB. This value can be obtained by having the driving amplifier operating at large back-off values respect to the OIP_3 (i.e., circa 30 dB). Considering that, as a theoretical rule, the OIP3 of an amplifier is set 9.6 dB higher than the P_{1dB} [94], in the mm-wave bands, due to the limited maximum power of commercially available PAs (i.e., 13 dBm for medium power amplifiers, as used at the input of the proposed system), the back-off requirement translates in largely reduced maximum power available from the source (i.e., circa -10 dBm). In order to minimize the impact of the reduced voltage swing over the (fixed range) ADCs, the two tones measurements are performed in the low-power configuration, i.e., removing the waveguide bend attenuators in the test-set. The limitation of the maximum drive power to -10 dBm imposes the measurement for model verification to be performed on small area transistor cells. The two-tones system linearity performances have been measured using on-wafer thru standards at different frequencies employing a tone spacing of 10 MHz. Measurements at 60 GHz show (see, Figure 5.14a) that for up to -17 dBm of input power the 3rd order intermodulation products are below the system's noise floor and then they start to increase, affecting the performances of the setup. Considering the full operational bandwidth of the designed setup, the worst case performances in terms of OIP3 are obtained at 65 GHz (see, Figure 5.14b), where the OIP3 measured for a -10 dBm input power drops, worst case, to 2 dBm. At this frequency, as well as at 50 GHz, the system linearity is limited by the performance of the input IQ mixer and



(a) (b)

Figure 5.14: Two tones performances of the proposed LP setup, measured on a thru standard at different loading conditions (see, Figure 5.11a. (a) Measured IM3 at 60 GHz for a two-tones signal with 10 MHz tone spacing. (b) Measured OIP3 vs. frequency at -10 dBm input power.

driving amplifier, which are operating at the edge of their specified bands. A better frequency refined analysis would show the problem to be confined around those two frequencies. The linearity performance of the system could be boosted by applying predistortion on the driving signal or by performing source-pull in combination with the load-pull measurement, as was shown for the lower frequency mixed signal load-pull presented in [95].

5.7. Large signal characterization of mm-wave devices using mixed signal active load-pull

The mm-wave mixed signal load-pull system was used to evaluate the large signal performance of different devices and compare these results with the prediction of a bipolar transistor model (i.e., Mextram 504). NXP Semiconductors SiGe HBT technololgy, QUBIC4Xi, providing an f_T/f_{MAX} of 180/200 GHz, was employed. First a single striped emitter transistor (device A) of 0.4x20 μm^2 emitter area was characterized at 60GHz. In Figure 5.15, two different choices for base biasing are presented, showing the possible optimization for maximum PAE (Figure 5.15a, V_{be} = 0.78) obtained when the device is biased in a weak class AB, and a compromise between maximum Gain and maximum PAE (Figure 5.15b, V_{be} = 0.82) with the device biased in a moderate class AB. Figure 5.15 provides also a comparison with the transistor model (embedded with the test-fixture parasitics) in the CAD environment (i.e., Cadence Virtuoso-Spectre). Both plots show good correlation between model and measurements for low power levels, while in both biasing points the model predicts a higher compression point, highlighting the importance of large signal measurements for model verification. A second device, a QUBIC4Xi dotted multi-emitter transistor (device B) of 20x(0.4x1.0) μm^2 was measured from the same wafer. The device has the same emitter area of the transistor reported in Figure 5.15, but a different layout. In Figure 5.16a a constant PAE load-pull contour at 1dB gain compression at 60 GHz is presented. In Figure 5.16b power gain and PAE for a reflection coefficient $\Gamma = 0.632\angle 161°$ are reported, showing a large

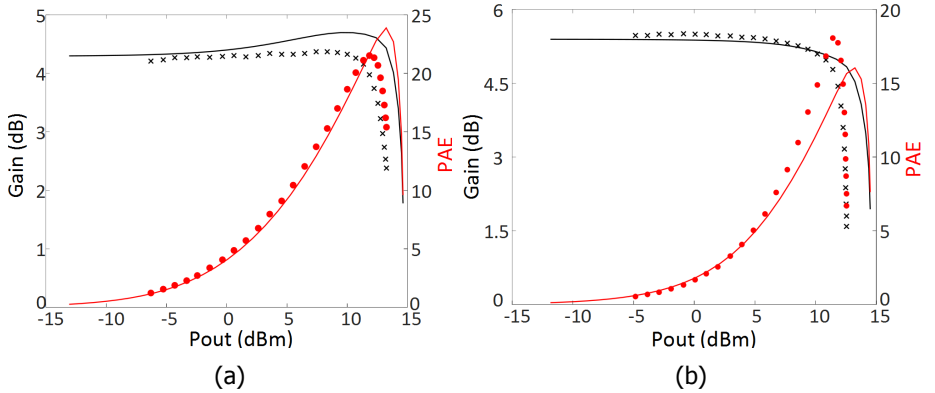


Figure 5.15: Comparison between measured and simulated values of Gain and PAE for device A with a load reflection coefficient of $\Gamma = 0.49\angle 156°$ at 60GHz for base bias a) V_{be} = 0.78 V and b) V_{be} = 0.82 V. Dotted lines refer to measurements, solid lines refer to simulations.

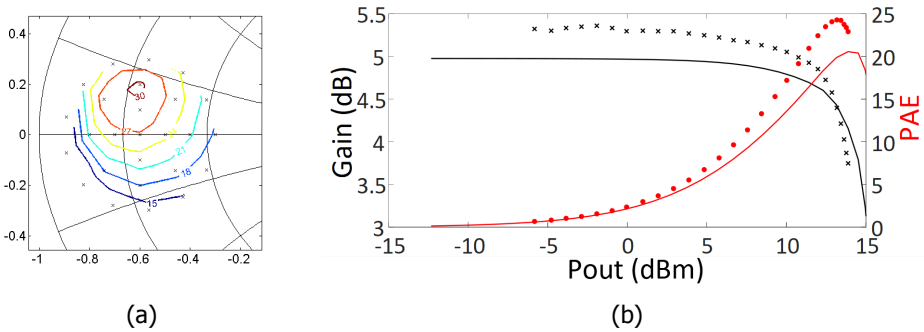


Figure 5.16: a) Constant PAE load-pull contour at 1dB gain compression and b) measured values of Gain and PAE for device B (dotted lines), with a set load reflection coefficient Γ= 0.632 ∠161° at 60GHz for base bias V_{be} = 0.82 V, and comparison with simulated values (solid lines)

improvement for the PAE, reaching a maximum of 24% at 1 dB compression point. These results highlight how large-signal measurements, and in particular load-pull, can be employed to compare different device topologies, in the same technology, for verification purposes. Similar investigations can be done for different topologies of the same device type, i.e., for different values of emitter width. Results obtained for each device can be then employed to perform a performance comparison, in order to analyze the performance of the same device depending on the geometry. An example of this kind of comparison is showcased in Table 5.4, where the performances of device B in terms of PAE and Gain are shown, in terms of maximum values achieved at 60 GHz, towards the emitter width.

Table 5.4: Maximum values of PAE and Gain, versus emitter width of device B, reported with the associate value of Γ_{Load}

W (um)	0.15	0.20	0.25	0.30	0.35	0.40
Maximum PAE	20.28	34.05	33.91	33.91	29.63	24.29
Γ	0.87∠ 152.7°	0.77∠ 153.7°	0.77∠ 153.7°	0.69∠ 154.4°	0.73∠ 162.2°	0.63∠ 161.6°
Maximum Gain (dB)	3.70	5.70	5.85	5.64	5.06	4.51
Γ	0.88∠ 162.1°	0.88∠ 162.1°	0.85∠ 171.3°	0.71∠ 166°	0.70∠ 173.5°	0.61∠ 170.5°

5.8. Large signal characterization of power amplifiers using active load-pull at mm-waves

Load-pull measurements of transistors, like the ones shown in Section 5.7, are typically used to extract and verify the device models, which are then employed during the design of more complex circuitry, like PAs. While the design process of this circuitry relies on models, their behavior still needs to be properly tested and verified. In this context, PAs are typically designed to be matched (at the input and the output), in the specific operation bandwidth, to 50 Ω, in order to properly drive the output (supposed to be at 50 Ω) and, during testing, the contact pad impedance. The pre-matched condition of this kind of ICs would prevent the need of mismatched measurement techniques like load-pull. Also, the higher output power (in respect to the single transistors) that can be achieved by PAs (in the order of 20 dBm for PAs in CMOS technology) would limit the capability of a load-pull system to present highly mismatched conditions at their load. However, some additional considerations need to be done:

- The residual uncertainty of the design phase could cause the output impedance to be (slightly) off the design goal, also considering the unpracticability of a perfect matching in the entire frequency bandwidth of an amplifier;
- At mm-wave, the maximum power delivered from PAs is still limited, and maximizing it is a major design goal. Even small improvements in the P_{SAT} or P_{1dB}, in the order of 1 dB or even just half a decibel, can be considered valuable enough to be worth investigating possible measurement-aided design optimizations.

With the aforementioned preconditions, the use of load-pull techniques for measurements of PAs performances at millimeter-wave frequencies can still come in handy. To make an example of the use of load-pull measurements on matched amplifiers, we used a Class-E/F_2 power amplifier realized in a 40 nm CMOs technology, designed to operate around 60 GHz, which was presented in [96]. Figure 5.17a shows the large signal performances of the considered PA, extracted with a 50 Ω loading condition, at 60 GHz. These results show state of the art performance for this kind of amplifiers. However, looking at the measured S_{22} of the device (i.e., the output impedance), it is possible to notice how, at 60 GHz, the device doesn't present a perfect match, which was intended in the initial design and would allow maximum power transfer at that frequency. It is then worth investigating the performance of the amplifier when applying small mismatch conditions, to see if it is

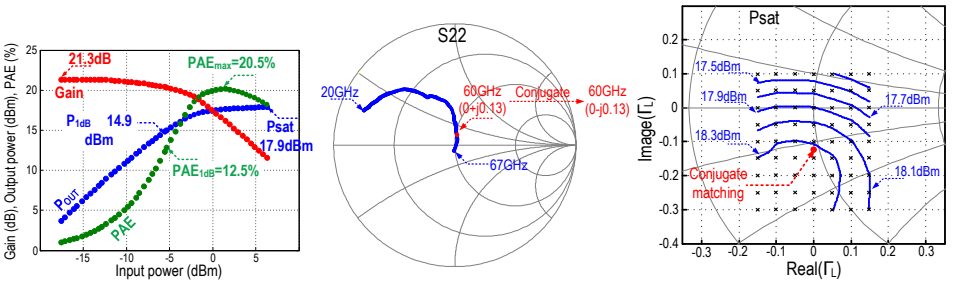


Figure 5.17: Measurement results from the considered class-E/F_2 power amplifier realized in a 40 nm CMOs technology, extracted from [96]. a) Large signal results at 50 Ω loading, at 60 GHz. b) Measurements of S_{22}. c) P_{SAT} countour at 60 GHz.

possible to further improve the performances. In order to do so, load-pull measurements were performed at 60 GHz forcing 63 different loading conditions around the conjugate matching Γ_{Conj} = -j0.13, sweeping the input power from -17 dBm to 7 dBm. Focusing only on the power performances, P_{SAT} improves from 17.9 dBm at 50 Ω to 18.3 dBm at Γ_{Conj}, arriving to 18.4 dBm at Γ = -0.05-j0.2, as shown from the P_{SAT} contour of Figure 5.17c. Similar improvements can be obtained for the power gain and the PAE of the amplifier, highlighting how it can be worth considering the use of load-pull techniques for a fine-tuning of pre-matched PA performances in the mm-wave frequency range.

5.9. Load-Pull aided small signal characterization of millimeter-wave breakout circuits

Systems-on-a-chip (SOC), like transmitters, receivers or radiometers, are typically composed of several different sub-circuits, like PAs, LNAs, detectors, antennas, etc... Design iterations often use, to improve the overall system performance, the characterization of stand-alone circuit blocks, the so called *breakouts*. Breakouts are basically replicas of the circuits blocks that are embedded in the complete systems, which are taken as stand-alone blocks to be properly characterized. In order to perform the characterization, the breakouts typically need some modification in respect to the original circuit block in order to properly interface with the characterization setup (i.e., 50 Ω feeding lines and probe pads). When considering the mm-wave frequency range such modifications can become substantial redesigns, due to great impact of circuit parasitic on the entire circuit, partly nullifying the motivation for circuit breakout in the optimization strategy. As an example consider the second stage of a mm-wave LNA driving a diode detector in its final application, shown in Figure 5.18, where all the back-annotated parasitic components are highlighted in colors. When comparing the in-system LNA and its breakout stand-alone version we notice:

- a different peaking inductor L1, re-optimized to resonate out the pad capaci-

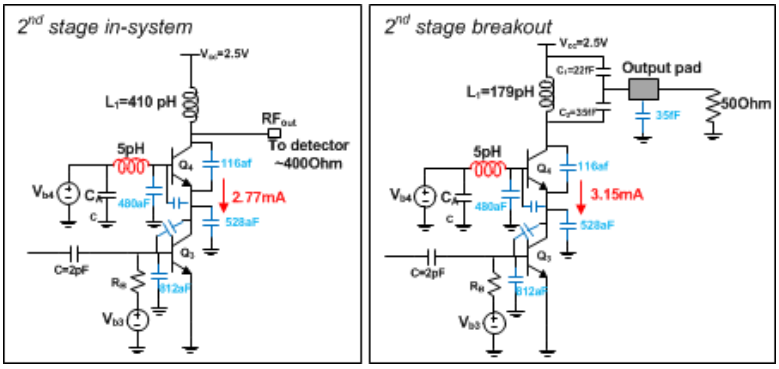


Figure 5.18: Simplified schematic of the 2nd stage of a mm-wave LNA intended to drive a diode-based detector. a) Schematic of the LNA in its final application. b) Schematic of the LNA in the breakout standalone version.

tance present in the stand-alone version,

- a capacitive divider to match the 50 Ω (instrumentation impedance) versus to the ~400 Ω of the in-system value,
- a slightly higher current in the stand alone version to compensate for the extra losses of the added components.

Overall, the circuit breakout represents a different circuit in respect to the original LNA, with even a modified biasing condition. Therefore, measuring the breakout performances would not be equivalent to the characterization of the LNA in its original application.
To overcome the above mentioned limitations, in this section we present a load-pull aided procedure to allow the direct characterization of breakout circuits of more complex integrated systems.

5.9.1. Breakout circuits characterization flow

To describe the breakout characterization flow, a simple two-block integrated system can be employed, as shown in Figure 5.19a. If the goal is to characterize Circuit 1, then a replica of this circuit block needs to be designed, including an appropriate output fixture (probe pads plus feeding line) allowing interfacing the characterization setup (see, Figure 5.19b). To replicate the original operating conditions of Circuit 1, it is ideally needed to provide, at its output, realistic loading conditions, i.e., to ”pull” the load of Circuit 1 to be equal to the input impedance of Circuit 2. However, the presence of the output fixture prevents the direct access to the internal reference plane of Circuit 1. If the output fixture can be properly characterized, the targeted loading conditions, required at Circuit 1 reference plane, can be transformed to an equivalent set of loading conditions at the pad plane, which is directly accessible by the measurement setup. At this point, a load-pull measurement can be performed to properly characterize the standalone component. This

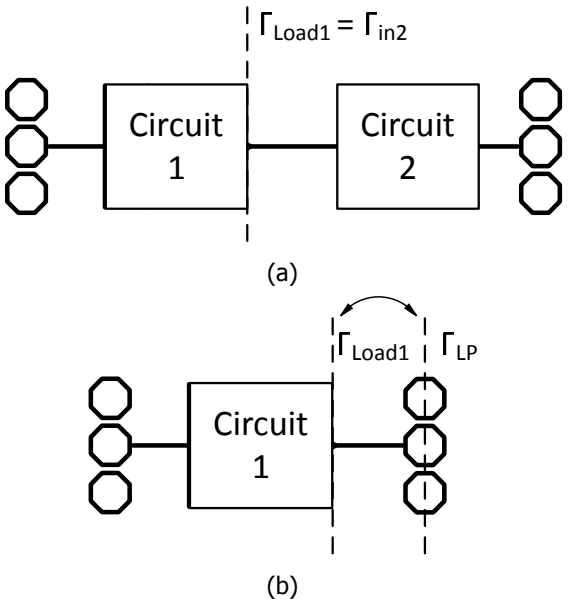


Figure 5.19: Design flow of standalone breakout. a) From the original circuit, the reference plane for the standalone characterization is set. b) An output fixture is applied at the reference plane to allow proper probing, and then the loading conditions required for the characterization are transferred to the probing pad.

procedure is intrinsically scalable to any number of building blocks, and in principle applicable in the same way if different source conditions need to be applied (i.e., using source-pull).

5.9.2. Standalone characterization of a LNA breakout

In order to present a practical example on how the proposed breakout characterization procedure can be applied to mm-wave circuits, we considered a 60 GHz radiometer realized in 0.25 µm BiCMOS technology, and presented in [97] (see, Figure 5.20a). The radiometer is composed of a two-stages LNA driving a square-law detector, without any intermediate matching networks. In order to characterize the LNA, first the reference plane for the breakout is defined. Then the output fixture is designed and added to the layout of the breakout circuit, as depicted in Figure 5.20b. At this point, it is needed to identify the loading conditions at the reference plane of the LNA, and then properly transfer them to the output pads of the breakout. For simplicity, we extracted the input impedance of the square law detector (i.e., the load impedance of the two-stage LNA) from simulations, using the parasitic extraction tool of Cadence Virtuoso. Considering this impedance, an accurate de-embedding of the output fixture is needed to compute the loading conditions at the pads. For this purpose, a TRL de-embedding kit was realized in the same back-end-of-line (BEOL) of the LNA (see, fig. 5.21a). The 'thru' standard of the de-embedding kit is realized by mirroring the layout of the output fixture,

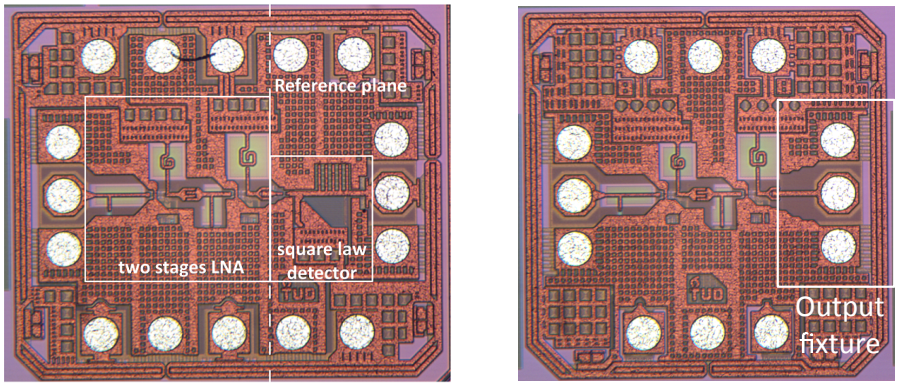


Figure 5.20: Micrograph of a) 60 GHz radiometer realized in 0.25 µm BiCMOS technology, and b) breakout of the two-stages LNA used for the characterization.

and the reference plane of the de-embedding procedure is placed at the center of the thru. This allows properly computing the S parameters of the output fixture as a direct result of the de-embedding procedure. The impedance transformation associated to the loading condition from the reference plane to the pads is shown in Figure 5.21b. At this point the LNA can be characterized. First, a S-parameter measurement is performed (see, Figure 5.22a, empty circles) at the contact pads. This measurement can be used to estimate the gain of the LNA when loaded by the detector, by simply de-embed the fixture and recalculate the S-parameters using the detector load as port-2 reference impedance. This has been done using Keysight ADS and it is reported in Figure 5.22a, full square symbols. If the behavior of the LNA is linear, i.e., the 50 Ω termination offered from the probes at the pad doesn't alter the operation regime of the device, than this estimate of the gain should be equal to the gain extracted by means of load-pull measurements, which is shown in Figure 5.22a, asterisk symbols. The discrepancy between the two shows that the only way to characterize the LNA breakout for its final application is to use load-pull measurements, since its output is not capable to drive the 50 Ω impedance offered by the measurement setup. The breakout measurements can be benchmarked towards the measurements of the complete circuit in which the LNA is integrated in its final application. In the case of the radiometer, the final responsivity can be computed through the knowledge of the LNA gain and the responsivity of the square low detector. For the latter, independent measurements of a detector breakout were not available, therefore simulations had to be used. Figure 5.22b shows the responsivity computed using the LNA gain measured using load-pull and the simulated responsivity of the detector. This result is compared towards simulations and measurements of the considered radiometer, from [97]. Despite a frequency shift of the values which can be mostly attributed to the use of simulations for the detector, absolute values of responsivity well match, in a first order approximation, the data obtained from the measurement of the entire detec-

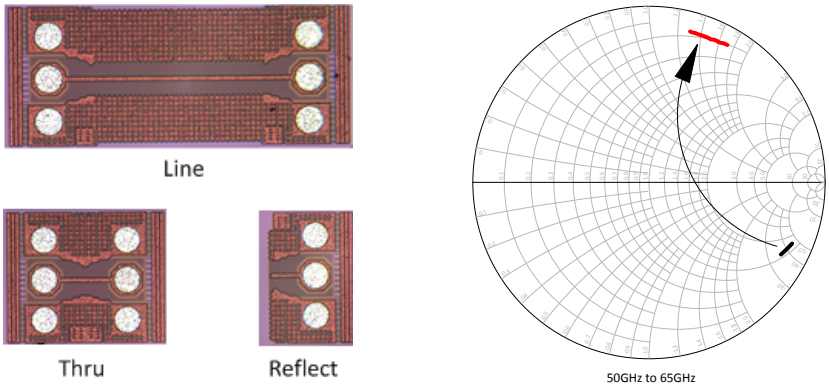


Figure 5.21: a) Micrograph of the de-embedding standards. b) Transformation of the load impedance associated to the input of the detector from the reference plane (black) to the pad plane (red).

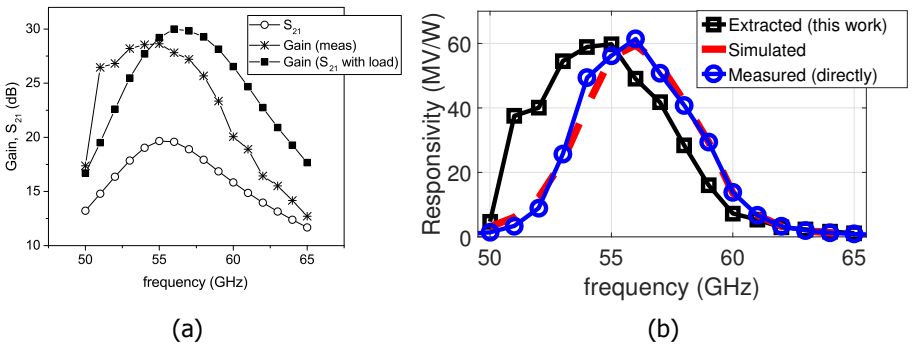


Figure 5.22: a) measured S_{21} (empty circles), small signal gain extracted from the measured S_{21} by artificially applying realistic loading condition (full squares) and the small signal gain measured using load pull at the load impedance computed in Figure 5.21b (asterisks). b) Responsivity of the 60 GHz radiometer of Figure 5.20a, obtained by using the measured gain of the LNA and the simulated responsivity of the square law detector. Data are compared towards simulation data of the same radiometer (dashed red curve) and measurement data of the entire radiometer (blue curve, circles), from [97].

tor (i.e., without breakouts), suggesting that the approach proposed in this section can be useful for complex circuit characterization. Additional test-cases with measurement of multiple breakouts will be needed to investigate the overall limits and advantages of this approach.

5.10. Conclusions

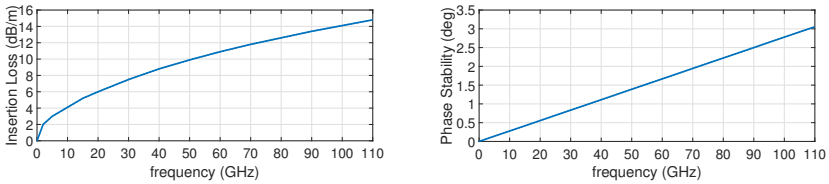
The use of (active) load-pull techniques at millimeter wave frequencies requires special precautions to guarantee the performances in terms of maximum mismatch that can be presented to a DUT, and the stability of the measurements. The use

of waveguide-based test-sets guarantees the maximum exploitation of the driving power capabilities, reducing the losses in the interconnections and the test-set. At the same time, a waveguide-based implementation provides a more stable measurement setup due to the better (raw) performances. In this chapter, a waveguide based mixed-signal active load pull operating in the frequency range from 50 to 65 GHz has been presented. The proposed setup allows the characterization of small devices (transistors), where high mismatch needs to be provided to the device load to determine optimum performances, as well as pre-matched ICs, where low-mismatch analysis can be employed for a secondary tuning and fine-optimization of the performances. Finally, this kind of measurement setup is envisioned to be used in *breakout* characterization. Here, the capability of providing arbitrary mismatch at the DUT reference plane would allow the measurement of realistic breakout circuits, avoiding circuit modifications and additional fixtures that might alter the circuit behavior and regime of operation.

6

VNA based small-signal and large-signal characterization at (sub) millimeter wave frequencies

In the previous chapter, a dedicated setup for large signal measurement in the WR-15 waveguide bandwidth has been described. When the frequency of operation increases, custom design like the one proposed in Chapter 5 may become unfeasible, due to the very high cost of both active and passive components, together with the limited availability of (IQ) mixers and in general medium power PAs. For this reason, there are little conventional large signal measurement setups for frequency higher than 75 GHz, and thus are mostly based upon the use of off-the-shelf equipment, typically frequency multipliers and power meters [98]. This kind of setups presents several limitations in terms of dynamic range, speed and accuracy of the calibration. On the other end, when using VNAs with extender modules for small signal measurements (i.e., S-parameters) there are limitations in the control of the power delivered to the DUT, due to the exclusion of the ALC from the measurement loop. In this chapter we first discuss the working principle of mm-wave VNA measurements, and related challenges. Then, a methodology allowing circumventing classical challenges associated to both small signal and large signal (sub)mm-wave measurements is described, and a novel approach for mismatched measurements (i.e., load-pull) for frequencies higher than 75 GHz is proposed.



(a) (b)

Figure 6.1: a) Insertion losses versus frequency for a TC110 cable used for 110 GHz application, data extrapolated from [100]; b) phase stability versus flexion for a phase stable coaxial cable, data extrapolated from [101]

6.1. Millimeter wave VNA

Most common commercially available test and measurement instruments operate at frequencies below 67 GHz, which can be considered enough to fulfill most part of the test and evaluation purposes. However, with the advent of mm-wave applications, the need for instrumentation operating up to 110 GHz, and beyond to the THz range, is rapidly increasing. All the most important VNA manufacturers provide standalone instrumentation capable of achieving coaxial measurement capabilities up to 67 GHz. As a matter of fact, all modern (broadband) VNAs present coaxial test-ports. The use of coaxial cables has the main advantage of allowing broadband operation starting from DC, as coaxial cables allow pure TEM propagation, while rectangular waveguides (and related flanges) are always limited on the lower side of the bandwidth by their fundamental cutoff frequency. Also, the use of coaxial assembly allows flexibility, in contrast with rigid metallic waveguides. On the downside, insertion losses in coaxial assemblies increase rapidly with frequency, and the increase of losses is even more accentuated for cables dedicated to millimeter wave propagation as for the latter, in order to guarantee single mode propagation at higher frequencies, the outer and inner diameter (OD/ID) of the conductor needs to be reduced, usually to dimensions lower than 1.4 mm [99]. At millimeter wave frequencies, the wavelength also becomes comparable with the lateral dimensions of the coaxial structure (λ ranges from 2.1 mm to 2.5 mm, depending on the dielectric, at 110 GHz). This means that even small modifications to the cable geometry (due to flexure, or other mechanical stress) could provoke large changes in the phase of the propagated signal. Figure 6.1 shows examples of data for insertion loss and phase stability for commercially available coaxial assemblies employed for applications up to 110 GHz. On top of that, and due to the required reduction of the inner conductor diameter, manufacturing adequate coaxial connectors is particularly challenging. To make an example, a 1 mm connector, dedicated to applications up to 110 GHz, presents jack pins with a diameter of 0.250 mm [102], and a tolerance of less than 0.051 mm [99]. Very recently, a new standard for 145 GHz propagation was introduced (0.8 mm connectors [103]), but it is not yet widely supported. Small dimensions and low tolerance also degrade the connector repeatability and the VSWR [102]. The combination of all these performance degradation for coaxially connectorized components and assembly would also have an

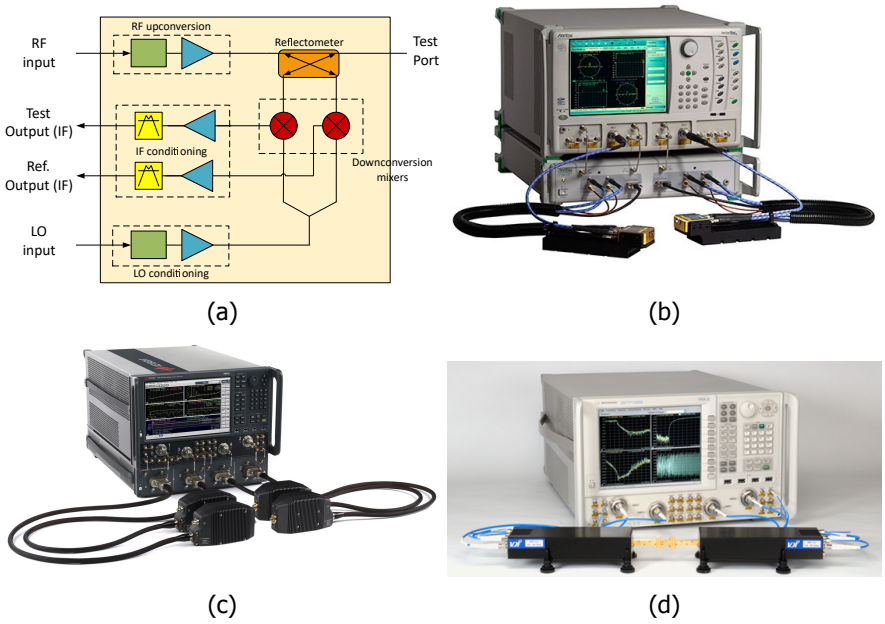


Figure 6.2: a) Simplified schematic of a T/R mm-wave extender module; b) A 2-port Anritsu Vector Star ME7838D broadband VNA, for measurements up to 145 GHz; c) A 4-port Keysight N5291A broadband millimeter-wave network analyzer with PNA series instrumentation, for measurements up to 110 GHz; d) a WR-5 vnax setup, employing mini extender modules from Virginia Diodes.

inevitable impact on the quality of the calibration, as was discussed already in detail in Chapter 5 of this dissertation. Overall, the aforementioned considerations make the realization of a standalone broadband VNA for frequencies higher than 67 GHz less practical. The most commonly adopted solution for mm-wave measurements is to ”extend” the frequency capabilities of the VNA by means of dedicated *frequency extender modules*. These are mainly trasmitter-receiver modules (T/R) allowing to increase the frequency of operation by means of multiplication, and to properly separate the mm-wave signals by means of a reflectometer and a dedicated down-convertion architecture. A simplified schematic of a T/R extender module is shown in Figure 6.2a. At present, extender based solution exist for broadband operation for measurements up to 145 GHz [104] (with a new approach for measurement up to 220 GHz recently announced), where coaxial standards still exist. For higher frequency of operation, extenders typically feature waveguide devices and sections, and their test-ports are usually realized by means of waveguide flanges. For this reason, mm-wave extenders are offered in frequency-banded solutions, being the operation frequency limited on the lower end by the fundamental cut-off frequency of the waveguide, and on the upper end by the onset of the second propagation mode in the waveguide (TE_{20}). The extenders are typically interfaced with the VNA by means of a millimeter wave test-set controller, providing appropriate signal rout-

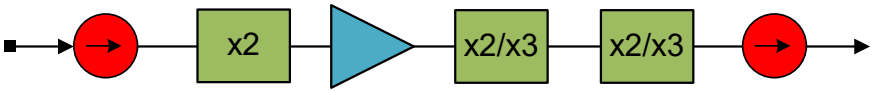


Figure 6.3: Block diagram of generic frequency up-conversion chain in millimeter wave extender

Table 6.1: VNA extenders typical specifications

Waveguide Band	WR15	WR12	WR10	WR8.0	WR6.5	WR5.1	WR4.3	WR3.4	WR2.8	WR2.2	WR1.5	WR1.0
Frequency range (GHz)	50-75	60-90	75-110	90-140	110-170	140-220	170-260	220-325	260-400	325-500	500-750	750-1100
Test port power (dBm, typ.)	10	10	10	6	6	-1	-2	-6	-10	-15	-25	-35
RF multiplication (typ.)	4	6	6	8	12	12	-	18	-	30	-	-

ing and conditioning. Modern multi-port and multi-source VNAs also allow direct connection between the VNA test-ports and the extenders.

6.1.1. Frequency extension

Millimeter wave extenders use, as input, the signals provided from the VNA, which are generated at a lower frequency in respect to the measurement frequency (RF input and LO input, usually in the range 8 - 20 GHz, although extenders accepting higher frequencies up to 40 GHz exist). The modules provide *readouts* of the scattered waves, sampled by the reflectometer, at itermediate frequency (IF, typically between 5 MHz and 500 MHz), so that these signals can be promptly acquired by the VNA receivers (Test and Reference channels). In order to do that, the extender needs to multiply the frequency of the input signal (for the RF and LO input) and to provide some sort of frequency down-conversion for the signals that need to be measured. The mm-wave signals are generated by multiplying lower frequency signals provided by the VNA source. This is achieved by means of multipliers (active or Schottky diode based). These devices can also be used in combination, as chains of multipliers are typically needed to obtain higher frequencies. A generalized block diagram of a frequency up-conversion chain employed in millimeter wave extenders can be seen in Figure 6.3. The VNA generator is used as a driver to a multiplier, typically with a lower multiplication order (x2). the signal is then amplified and used to drive a second passive multiplier, usually a doubler or a tripler. To reach higher frequency, additional multipliers can be used in the chain, possibly combined with intermediate amplification stages to obtain optimum power level to drive the following stage. Depending on the input signal and multiplication stages, frequency up-converters can cover frequencies from 50 GHz to 1.1 THz, with different banded modules (see, Table 6.1). After up-conversion, the signal is provided to the DUT through a bi-directional coupler. The coupled signals are at the same frequency of the measurement, and the down-conversion to IF can be performed by means of fundamental or sub-harmonic mixing [105]. In the first case, being $f_{IF} = f_{RF} - f_{LO}$, the frequency of the signal provided to the local oscillator terminal of the mixer (LO), needs to be first up-converted, using an up-conversion chain similar to the one in Figure 6.3. In case sub-harmonic mixers are used, the LO signal provided

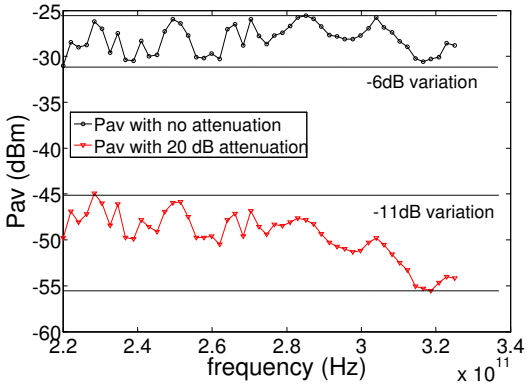


Figure 6.4: Output power versus frequency of a mm-wave extender module in the WR-03 range, at different value of external attenuation.

from the VNA can be directly used for the mixing, or a lower up-conversion can be used, being in this case $f_{IF} = f_{RF} - Mf_{LO}$, with M being the specific harmonic used by the sub-harmonic mixer. Using a sub-harmonic solution allows for a simpler down-conversion stage, reducing cost and complexity.

6.2. Mm-wave test-benches shortcomings

When considering measurements at mm-wave and submm-wave, one of the limitations is the measurement dynamic range reduction. As frequency increases the power available decreases while the noise floor, which is set by the measurement instruments, remains ideally constant, bringing to a reduction of the dynamic range. In standard VNA configurations, the dynamic range is kept constant versus frequency by using the amplitude level control (ALC) (see, Chapter 2). When mm-wave VNA extenders need to be used, the ALC is implicitly excluded from the measurement loop. Due to the absence of an ALC within the extenders, and the non-linear nature of the internal components, the power available from the source can significantly vary within the waveguide band. An example is shown in Figure 6.4, where the power at the output of a commercially available WR-03 VNA extender is displayed, versus frequency, when the nominal (fixed) power is provided at the input RF port of the module (black curve). In the example, the power fluctuation is in the order of 6 dB, but can reach values higher than 10 dB depending on the bandwidth and the manufacturer of the extender. While the absolute value of the output power can be modified coarsely by means of optional embedded manual attenuators (see, Figure 6.4, red curve), the fluctuation cannot be corrected. When measuring active devices (i.e., power amplifiers), this lack of control on the power delivered to the DUT can have different implications on the measurement accuracy.

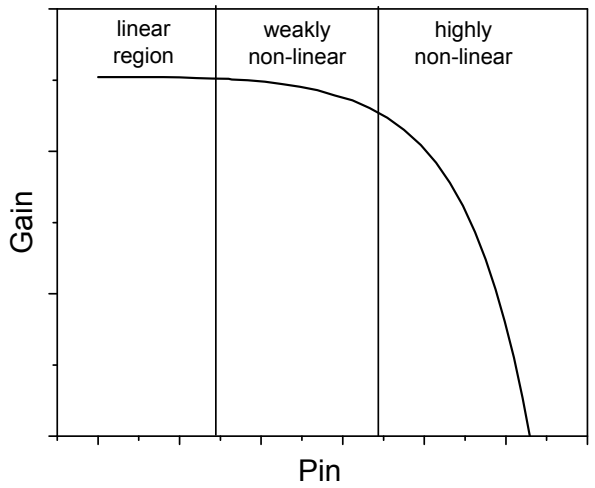


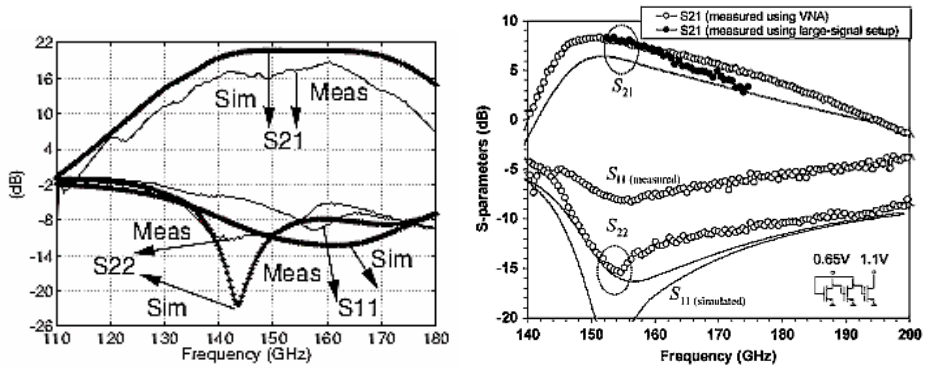
Figure 6.5: Generalized Gain vs. P_{in} characteristic, at fixed frequency, of an active device

6.2.1. Small signal measurements

The small-signal characterization of power amplifiers, aims to look at input matching, reverse isolation and the small-signal gain of the DUT. When performing these measurements, the device drive level needs to ensure the small signal operation. If we consider the simple example of Figure 6.5, at every frequency a power amplifier (in the example, a class A) can be driven into three main operation region. The absolute linearity is only guaranteed when the input power is sufficiently low, while increasing the driving would bring the device first in weakly and then in highly non linear region, where the change in input power would be related to a sensitive change in gain. When the amplifier is composed by several stages, which is often the case at mm-wave frequencies due to the limited gain per stage, the compression mechanism of the gain curve can be very diverse, mostly depending on the area ratios of the stages. When the absolute power level of the drive signal is unknown, and it is not advisable to strongly reduce the driving power (i.e., using waveguide attenuators) not to incur in noisy measurement traces, there is a clear risk of measuring in the weakly non-linear region (Figure 6.5). When this occurs, the S_{21} parameter is actually modulated by the non-constant drive level (versus frequency) and the non-linear device input-output characteristic. This can result in non-physical fluctuations in the measured S-parameter. Examples of this kind of error can be observed in Figure 6.6a, where the measured S_{21} of a power amplifier operating between 135 GHz and 170 GHz [106] presents un-physical fluctuations in magnitude, that are most likely associated to a incorrect DUT drive due to the lack of input power control.

6.2.2. Large signal measurements

In order to characterize the key parameters of PAs (i.e., P_{1dB} and PAE), large-signal setup as shown in Figure 6.7 are typically employed. In this kind of setup, the



(a) (b)

Figure 6.6: a) Small-signal model-hardware correlation of the PA from [106], comparing simulation (black symbols) to measurements (solid lines) b) measured (circles) and simulated (solid lines) S-parameters of the three-stage 150 GHz amplifier, measured with VNA and large-signal setup, from [107].

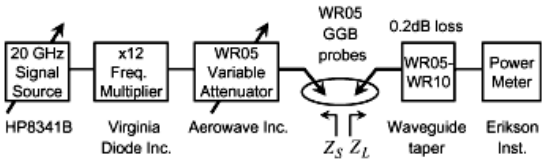


Figure 6.7: G-band large-signal measurement setup (153 GHz to 173 GHz), from [107].

device drive is realized by properly using frequency multipliers and variable gain attenuators, to allow the coarse control of the input power, while the response of the DUT is simply measured by means of power meters. The scalar nature of such setups only allows for a response type of calibration, thus neglecting losses arising from mismatches in the setup. This simplification can easily result into measurement errors, as depicted in Figure 6.6b, where the transducer gain measurement of a CMOS power amplifier, realised at small signal drive using the large-signal setup of Figure 6.7, is compared with the S-parameter measurements of the same device using conventional VNA setup (thus, using proper vector correction) [107]. In this case, the measured transducer gain, which should be equal to the S_{21} of a device when in small-signal region, actually diverges from the measurements of S_{21} when the device's mismatch (i.e., S_{11}) increases, and the error is associated to the lack of vector correction in the large-signal setup. It is important to note that all the components shown in Figure 6.7 are already part of a VNA with frequency extenders, with the only exception that stand-alone frequency multipliers could generate few dBs more of power due to the absence of the directional coupler.

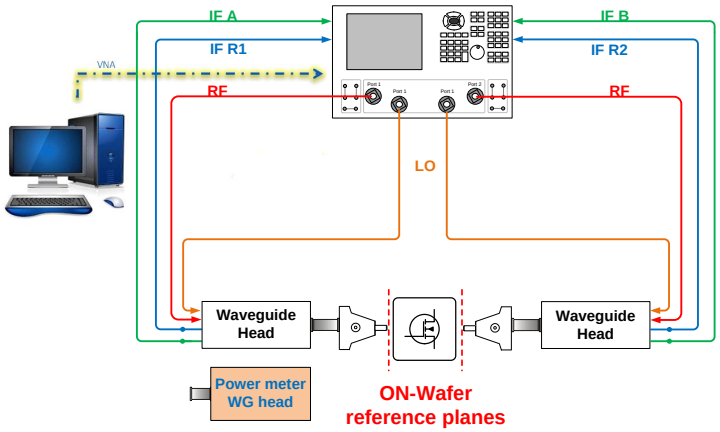


Figure 6.8: Simplified schematic for the proposed measurement setup.

6.3. Power control for s-parameters and large signal characterization at (sub)-mmwave

The challenges reported in Section 6.2 can be circumvented by including proper power control in a conventional VNA setup for mm-wave measurements, mimicking the ALC mechanism with a dedicated software control when the actual hardware device is out of the measurement loop. For this purpose, a hardware and calibration procedure has been presented in [108] to achieve a frequency scalable method for absolute power control in small signal and large signal measurements. The presented method, based on a software based loop, allows refined control of the power presented at the DUT in the entire frequency band covered by the VNA extender. In this section, the architecture and working principle of the method are explained in detail.

6.3.1. System Architecture

Figure 6.8 shows the schematic representation of the proposed test-bench. In this setup, the test-set is equipped with two VNA extender modules, allowing full two-port calibrated s-parameters. Currently, modules for different waveguide bandwidths are commercially available, covering an overall frequency range from 50 GHz to 1.1 THz, and the designed setup is suitable for all the possible waveguide bandwidths. The generation of the RF and LO signals providing the feed to the mm-wave extenders is performed using the internal sources of the VNA, when using a two-source analyzer, or by adding an external, low phase-noise, synthesizer when the VNA only has one single power source. The acquisition of the coupled waves is performed using the VNA receivers. The values of the scattered waves are then sampled and sent to an external controlling PC, where all the computation is performed. In addition to the previous components, not shown in the schematic,

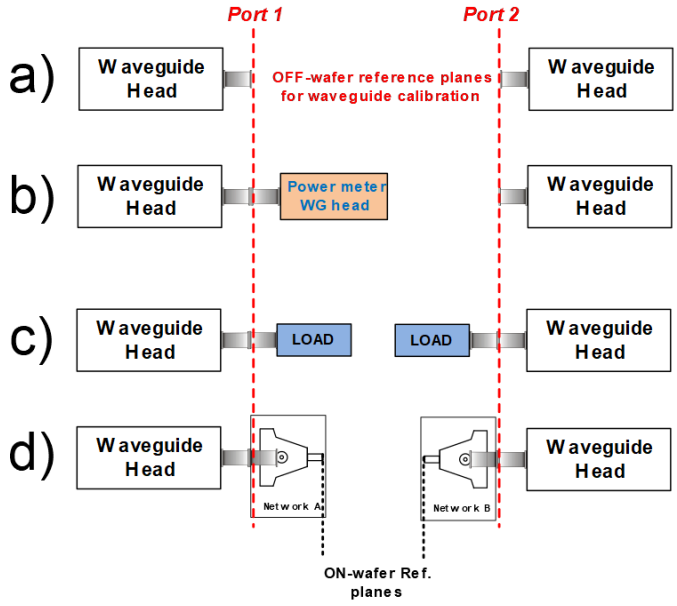


Figure 6.9: Modular schematization of the four calibration steps needed in the proposed setup. a) First a two-port calibration is performed at the waveguide ports; b) then a power calibration is done by connecting the power meter at Port 1; c) after the power calibration, power leveling is performed by doing measurements on matched standards; d) finally wafer probes are included in the setup and de-embedded with a second-tier calibration.

a power meter is needed to perform the absolute power calibration, as it will be discussed in following sections. In this setup a calorimeter based power meter has been used, allowing power measurement from 75 GHz to 1.1 THz. Finally, for on-wafer DUT measurements, wafer probes need to be used.

6.3.2. Calibration method

In order to properly control the power, the knowledge of the absolute power at the reference port, together with the chain gain/losses of the mm-wave extender modules are required. Once these parameters are known, the software aided-solution could mimic the behavior of a closed-loop control system. The proposed calibration procedure that allows the refined power control at the input of the DUT requires four steps, synthetically reported in Figure 6.9. First, a conventional off-wafer two-port calibration (i.e., TRL [29] or LRM [28]) is performed at the mm-wave modules waveguide sections (Figure 6.9a). Then a power calibration, as described in [93], is performed at the waveguide port in order to have a complete knowledge of the absolute power at the output of the module. The power calibration is done by connecting the power meter at the port 1 calibration reference plane, as set from the off-wafer calibration (see, Figure 6.9b). After the power measurement is

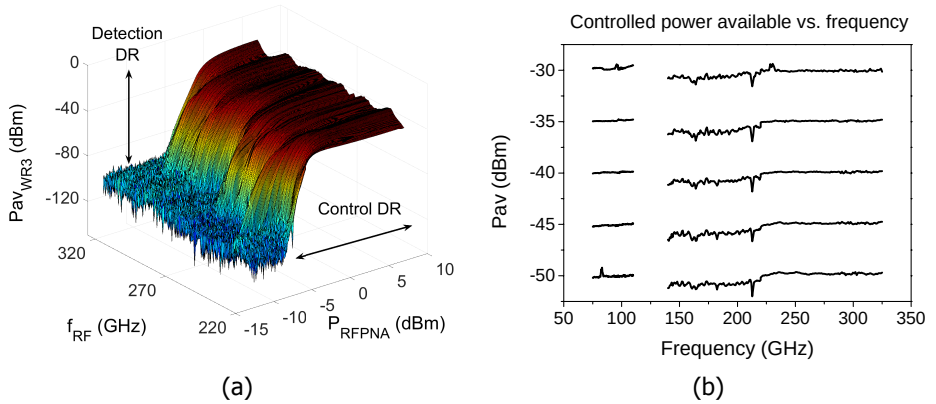


Figure 6.10: a) Power leveling results for Port1 of the proposed setup, in the WR-3 waveguide band. The plot depicts the value of the output power at the port of the extender module as a function of the source power provided by the VNA and the frequency. b) Power available at Port1 of the proposed setup versus frequency in the WR-10, WR-5 and WR-3 waveguide bands, after power leveling. The plot shows the measured output power for different values of power set from the user, versus frequency.

performed, a link between absolute power and the waves measured at the VNA receiver is created by means of an additional error term $|I_{10}|$ [93]. The power calibration can be conveniently applied also to the second port, by properly using the information collected on the thru standard during the initial two-ports calibration. Once the power at the waveguide reference planes can be correctly measured, a last OFF-wafer step must be performed in order to characterize the relation between the RF source power, set in the VNA, and the power available at waveguide Port-1 and Port-2. This step is the so-called "power leveling". During power leveling, a large number of frequency sweeps is performed, varying the VNA RF source power level while measuring the related output power at the waveguide port and the reflection coefficient Γ at both Port-1 and Port-2, which are connected to a 50 Ω termination (see, Figure 6.9c). Hence, the power available at the same reference planes, at each frequency, can be computed as:

$$P_{av_{Port1,2}} = \frac{P_{in_{Port1,2}}}{1 - \left|\Gamma_{Port1,2}\right|^2} \tag{6.1}$$

The result, as depicted in Figure 6.10a for the case of measurements in the WR-3 waveguide band, is a look-up table, showing the power available at the specified port as a function of both the source power provided by the VNA, P_{RF}, and the frequency. Once the power leveling is performed, the look-up-table can be pre-loaded in the system to compute, for each frequency of interest, the source power level that must be set in the PNA in order to have the desired power available at Port-1 and Port-2, also during frequency sweeps, with no overhead time in respect of a conventional measurement. In order to move the calibration reference plane to the probe tips, a further calibration step is needed, consisting in the de-embedding of the wafer probes (see, Figure 6.9d). This de-embedding procedure can be per-

formed on calibration substrates for probe-tip calibration (i.e., alumina, fused silica or silicon BEOL), using standard two-port de-embedding procedures.

6.4. System performances

6.4.1. Power control

After the setup is properly calibrated and the power leveling is performed, it is possible to accurately control the power at the output of the extenders, or at the probe tips if an on-wafer configuration is selected. In Figure 6.10b values of power available at the waveguide ports of the mm-wave extenders is shown for the three considered frequency ranges after the power leveling is applied. The accuracy in power control depends on the frequency range and on the hardware implementation of the up-conversion chain, which depends on the manufacturer. For the considered configuration, the largest spread in control level is obtained in the WR-5 frequency range, where the power control can only be set with a ±0.75 dB error. Note, that the read out in the absolute power provides an accurate value independent of the uncertainty in the set power.

6.4.2. Stability

In order to showcase the performance of the proposed setup in terms of measurement stability, repeated measurements have been performed in a limited time period over the different waveguide bands, and the results have been used to extract the stability of the measurements in terms of standard deviation, versus frequency. First, 100 consecutive measurements have been performed in the entire frequency range. Then, another measurement has been performed after 10 minutes, in which the system has been turned off. In Figure 6.11a the variation of the mean value of the available power, normalized to the available power at thermal regime, is shown versus time. For all the considered waveguide bands, the result highlights an RC time constant behavior, which can be associated to a thermal transient. The average available power varies from an initial value, measured when the system is in a "cold state", to a regime value when the thermal transient is completed. When the RF and LO signals are switched off for a sufficiently long time period, the system returns to its initial state. As shown in fig. 6.11a, the characteristics of the thermal transient, in terms of time constant and power variation, are strongly dependent on the considered module, being frequency and manufacturer dependent. This thermal transient has to be taken into account when defining the stability of the measurement setup. In fact, the measurement repeatability strongly depends on the region of the transient in which the specific measurement is performed. In order to define the impact of the thermal drift on the stability performances, first the standard deviation versus frequency has been extracted from the 100 repeated measurements shown in Figure 6.11a. Then the same procedure has been performed only considering measurements obtained at the thermal regime. The results are showcased in Figure 6.11b, where the stability boundaries defined using the two different standard deviations are sketched for the WR-5 waveguide band. This plot shows a drastic improvement in terms of stability when performing mea-

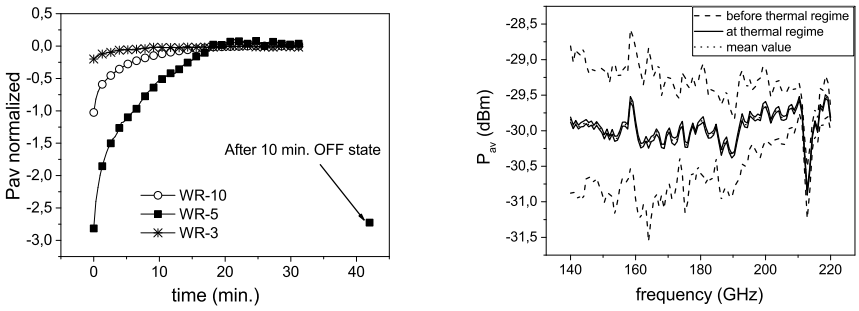


Figure 6.11: a) Average available power, normalized to the regime value, measured at port-1 of the designed setup, for WR-10, WR5 and WR-3 waveguide bands, for the same power set from the user equal to -30 dBm, over 100 consecutive measurements. b) Stability of the power control in the WR-5 waveguide band. The dashed lines represent the stability boundaries defined using the standard deviation extracted from the 100 measurements considered in Figure 6.11a. The solid lines define the stability boundaries using the standard deviation extracted from measurements when thermal stability is reached.

6

surements at thermal regime, with the average value of standard deviation varying from 2 dB to 0.03 dB.

6.5. Power controlled measurements of mm-wave power amplifiers

To demonstrate the capability of the VNA based power controlled setup, a following work described in [98] the measurements of a multi-stage power amplifier in the frequency range from 130 to 180 GHz using the measurement technique described in last section. In this experiment two VDI WR5 VNAX extender modules were employed for the measurements, and a VDI Erickson PM5 power meter, was employed for the power calibration. First, the DUT was measured, for a defined bias level, using the classic mm-wave VNA setup (i.e., without power control). Then, measurements were performed at a fixed, controlled power level of Pav,in = -30 dBm. Finally, power sweeps in the range from -43 dBm to -12 dBm, at different frequencies, have been employed to realize large-signal measurement of the device. Figure 6.12a shows the measured available power from port 1 of the WR5 extender in the conventional operation mode, i.e., no power level, (asterisks) and for power controlled measurements (filled squares). Figure 6.12b shows the measurement results for the S21 of the considered amplifier in the entire frequency range. Measurements highlight a strong discrepancy between the two methods in the frequency range from 130 to 157 GHz (see, Figure 6.12b), where the difference in terms of S21 reaches 10 dB at 140 GHz. This discrepancy depends on the fact that the non-controlled power level at the input of the device in the frequency range between 130 and 160 GHz, is not sufficiently low to ensure linear operation for the

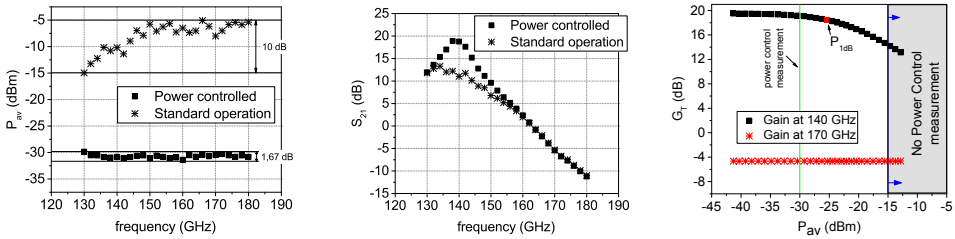


Figure 6.12: a) Power available versus frequency at port 1 of the system employed in [98] for standard operation (asterisks) and using power control (squares). b) S_{21} of the considered PA measured in standard system operation (asterisks) and with -30 dB controlled Pav (squares). c) Transducer gain for the considered device, measured with power sweeps at 140 GHz (filled squares) and 170 GHz (red asterisks)

DUT, as exemplified in Figure 6.12c where the transducer gain of the DUT is shown for both 140 GHz (black filled squares) and 170 GHz (red asterisks).

6.6. Frequency scalable active tuner for (sub)mm-wave active load-pull

As shown in the previous section, using a 3 step calibration and the aid of external computation, allows performing large signal measurements at (sub)mm-wave frequencies, by employing off-the-shelf equipment designed for small signal measurements, i.e., the same equipment which is commonly used for simple, non-power controlled, S-parameter measurements. The large signal capabilities of the setup, however, are limited, and only matched measurements can be performed, since the load (or source) impedance presented to the DUT cannot be changed in respect to the system intrinsic reference impedance. If one wants to perform more advanced measurements (i.e., load-pull), the hardware setup needs some improvement. In this perspective, let's analyze what would be the conditions that would allow the use of the setup for load pull measurements. First and necessary condition, is to have some sort of impedance tuners, i.e., a device able to change the impedance condition at the output of the DUT. As shown in the previous chapter, at very high frequencies, active tuning is preferable to passive tuning, mostly due to the higher losses. An active tuner changes the impedance condition by properly injecting a defined signal into the DUT terminal and, in order to tune the impedance, this signal needs to be controllable both in phase and in amplitude. If we take into account the system described in the previous sections, it is evident that while it is possible to modulate the power injected into the DUT, no control is available on the phase. To incorporate phase control into the signal injection, the use of a phase shifter into the injection path would be needed. The intuitive solution, supposing to have freedom in the hardware design, would be to put the phase shifter right before the reflectometer, allowing performing the phase modulation directly on the multi-

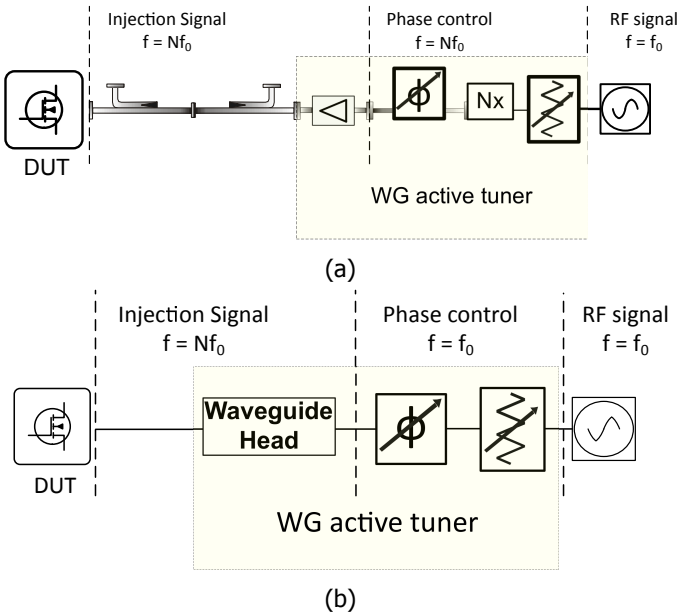


Figure 6.13: Two possible schematic configuration for an active tuner at (sub)mm-wave. a) The phase modulation is performed at the measurement frequency, after frequency multiplication. b) Both phase and amplitude modulation are performed at lower frequency in respect to the measurements, before any frequency multiplication stage.

plied signal (see, Figure 6.13a). This would imply the modification of the mm-wave extender, employing a mm-wave phase modulator. While from the measurement point of view this would be the most suitable option, the very high cost of such a component together with the complexity of an hardware modification inside a mm-wave extender make this solution not viable. On the other end, if the phase shifter is placed *before* the mm-wave extender (see, Figure 6.13b), the phase modulation would be performed on the RF-signal *before* the multiplication, thus at a lower frequency in respect to the measurement one. The latter solution allows more flexibility and lower cost, since lower frequency components can be used for the phase shifter, while the waveguide extender would not be modified. Before choosing the right phisical implementation, it is worth analyzing how the phase modulation can impact on a frequency multiplied signal.

6.6.1. Phase modulation on a frequency multiplied signal

Let's consider a generic sinusoidal signal V_{RF} generated by the VNA, with a frequency f_0 and generic initial phase ϕ_0:

$$V_{RF}(f_0) = cos(2\pi f_0 + \phi_0) \tag{6.2}$$

When this signal is fed to a non-linear component, armonics are generated based on the Fourier series:

$$V_{RF}(kf_0) = \sum_{k=-\infty}^{\infty} c_k e^{ik(2\pi f + \phi_0)} \tag{6.3}$$

if the non linear component is a multiplier with a factor k = N, then the output of interest is the N-th armonic:

$$V_{RF}(Nf_0) = c_N cos[N(2\pi f_0 + \phi_0)] = c_N cos(2\pi N f_0 + N\phi_0) \tag{6.4}$$

Let's now consider a generic phase shifter, introducing a phase change *M* to any signal fed into its input. If we consider the situation of Figure 6.13a, where the phase shifter is placed after the frequency multiplication, then based on eq. (6.4) the output will be:

$$V'_{RF}(Nf_0) = M\{c_N cos[N(2\pi f_0 + \phi_0)]\} = c_N cos(2\pi N f_0 + N\phi_0 + M) \tag{6.5}$$

Viceversa, when considering the situation of Figure 6.13b, the multiplication is performed on a signal on which the modulation is already applied, thus:

$$V''_{RF}(Nf_0) = c_N cos[N(2\pi f_0 + \phi_0 + M)] = c_N cos(2\pi N f_0 + N\phi_0 + MN) \tag{6.6}$$

Equation (6.5) and eq. (6.6) allow highlighting the operational difference between Figure 6.13a and Figure 6.13b: while in the first option the modulation is applied directly to the injection signal, in the latter the modulation would be altered by the frequency multiplication, and this will have to be taken into account when operating the active tuner for load-pull purposes.

6.6.2. The active tuner

The two implementations proposed in Figure 6.13 both represent active tuners to be employed in an open loop active load-pull, as it is implied by the absence of a physical feedback (closed loop). Once the topology of Figure 6.13b is chosen for the active tuner, due to the lower hardware complexity, the actual implementation needs to be defined. The choice of the waveguide head is defined by the specific frequency range, and for simplicity we assume it to be fixed. For the modulating part (amplitude and phase modulation) appropriate components need to be chosen. As explained in Section 6.3, the amplitude (power) modulation of the injection signal can be obtained directly from the RF source of the VNA, while the power control capability is achieved by means of proper calibration steps. However, since the RF source of the VNA needs to be shared between the two instrument ports (Port 1 and Port 2) to guarantee signal phase coherence, using the same source for the power modulation would not allow the two ports to be used independently. If we want the power modulation to be independent between the two ports, another solution should be used. The use of IQ modulators, as done for the mixed signal active load pull of Chapter 5, would in this case come in handy, allowing both power and phase modulation for each port, independently. The main difference in respect to the mixed signal active load pull is that, in this case, the signal modulation is performed at a different frequency in respect to the measurement frequency.

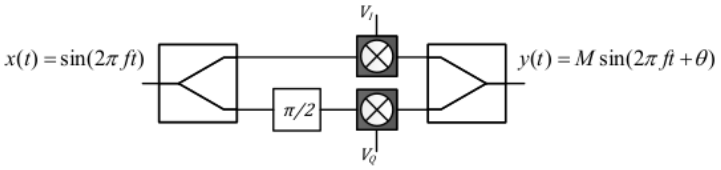


Figure 6.14: Schematic representation of an IQ mixer.

6.6.3. IQ modulation and load pull in a frequency multiplied loop

In order to better understand the following sections, it is worth to make a small recall on IQ modulation. Let's suppose to have a sinusoidal signal $x(t) = sin(2\pi ft)$ and to feed it to an ideal IQ mixer, like the one schematized in Figure 6.14. Now, let's also suppose that the phase and quadrature signals are two DC voltages V_I and V_Q. The output signal *y*(t) will be a modulated version of *y*(t) as:

$$y\,(t) = M * sin(2\pi ft + \theta) \tag{6.7}$$

Where:

$$M = \sqrt{V_I^2 + V_Q^2} \tag{6.8}$$

$$\theta = arctan\left(\frac{V_Q}{V_I}\right) \tag{6.9}$$

At each frequency f, the signal *y*(t) can be also conveniently described as a phasor ***Y***:

$$\mathbf{Y} = Me^{j\Theta} \tag{6.10}$$

The considered IQ mixer can be used, in principle, to perform active tuning at the output of a DUT, as it is done in mixed signal active load pull [80]. So let's consider the simple situation depicted in Figure 6.15a, where a general DUT with an output signal *z*(t) is considered. Let's now assume *z*(t) to be sinusoidal, $z\,(t) = A * sin\,(2\pi ft + \phi_0)$ at the same frequency of *x*(t) and phase coherent with it. The load reflection coefficient Γ_L generated by the active tuner can be described as $\Gamma_L = \frac{y(t)}{z(t)}$, and considering phasorial representation:

$$\Gamma_L = \frac{\mathbf{Y}}{\mathbf{Z}} = \frac{M}{A} * e^{j(\Theta - \phi_0)} \tag{6.11}$$

Considering *A* and ϕ_0 to be constant at a given frequency, ideally any loading condition can be obtained by properly choosing V_I and V_Q. Let's now consider the case in which the IQ mixer is followed by a frequency multiplier, and the measurement is performed at frequency Nf_0 like in Figure 6.15b. In this case, *x*(t) is transformed, by frequency multiplication, in *w*(t):

$$w\,(t) = M * sin(2\pi Nft + N\Theta) \tag{6.12}$$

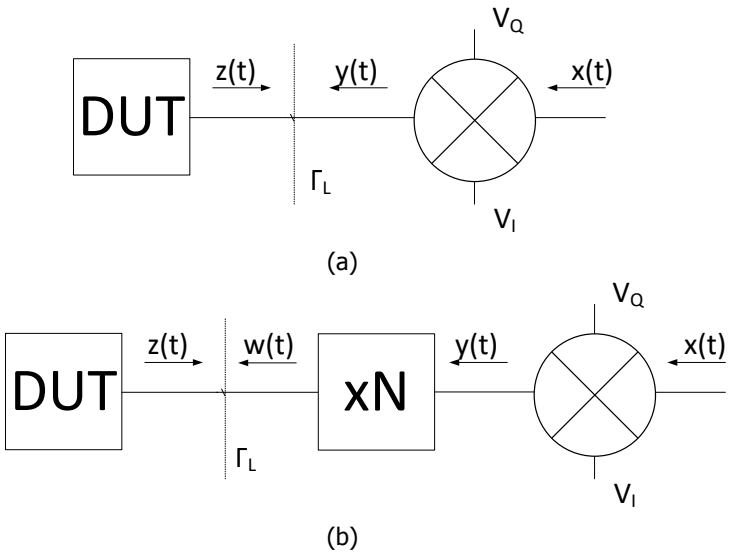


Figure 6.15: Exemplification of the use of IQ mixer based active tuners for load pull measurements. a) A simple IQ mixer is used for the active tuning. b) A frequency multiplication is performed after the IQ mixer.

So that the loading condition presented by the active tuner will become:

$$\Gamma_L = \frac{\mathbf{W}}{\mathbf{Z}} = \frac{M}{A} * e^{j(N\Theta - \phi_0)} \tag{6.13}$$

If we want to graphically describe the problem, we can make use of the charts in Figure 6.16. Using the IQ mixer as a active tuner allows projecting the vector **Y** in the I-Q space (see, Figure 6.16a), into a reflection coefficient in the complex Γspace (i.e., the Smith chart, Figure 6.16b), where the phase and the amplitude of the reflection coefficient only depend on V_I and V_Q. When using a multiplier the same kind of projection is still possible, but the phase of the reflection coefficient will scale with a multiple N of the phase Θ (see, Figure 6.16c). This would mean, for example, that if V_I and V_Q are used to describe a circumference in the I-Q space, the reflection coefficient of the load at the DUT will describe N circumferences in the Smith chart. The analysis performed in this section assumes the use of ideal IQ mixers, and simplifies the behavior of the mm-wave module as an ideal multiplier. In practice, IQ mixers will be limited in performance in a certain range of power and values of V_I and V_Q. Also, the multipliers present into the mm-wave module, will in general introduce an additional phase shift to the signal, while also affect the amplitude due to the conversion loss. Even further, due to the non linear nature of the frequency multiplier, and the generation of several harmonics other than the desired ones, the effect of the multiplication on the phase of the signal will not always be exactly equal to N. Nonetheless, the generality of this analysis allows it to be valid.

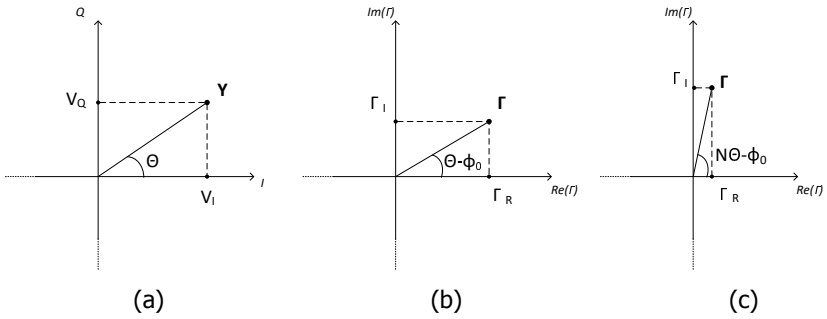


Figure 6.16: Graphic representation of the effect of IQ modulation on active tuning. a) Representation of the vector ***Y*** described by the IQ modulator in the IQ polar space. b) Representation on the complex Γspace of the reflection coefficient synthesized at the output of the DUT in Figure 6.15a. c) Representation on the complex Γspace of the reflection coefficient synthesized at the output of the DUT in Figure 6.15b.

6.6.4. The test bench

Considering the tuner implementation described in Section 6.6.2, we can now define the structure of a test bench for load-pull characterization, for which a schematic representation is shown in Figure 6.17. In this case, ideally two active tuners are employed, one for each port of the DUT. Due to the employment of IQ mixers in the active tuners, digital to analog converters (DAC) need to be used to generate the in phase and quadrature signals (Is and Qs). Since, in the proposed setup, the IQ mixers are only employed for amplitude and phase modulation of a single tone signal, the I and Q signals are generated at DC. In order to allow fast frequency sweep, at least during calibration, an handshaking loop is implemented between the ADC and the VNA, allowing to quickly change the values of I and Q provided to the tuners, as the measurement frequency changes. The two active tuners share the same RF input signal, which is generated at port 1 of the VNA and then split using a power divider. The RF sharing is essential for maintaining the phase coherence between the two injection signals, as explained in [80]. The RF signal is generated at a constant power, defined by the specifications of the employed IQ mixers. For the rest, the setup is substantially identical to the one shown in Figure 6.8 for power control, including the use of an external computing unit.

6.6.5. Preliminary results

While the realization of a complete scalable (sub)mm-wave load pull setup goes beyond the scope of this dissertation, preliminary work has been done to prove the capability of the approach to actually perform active tuning by means of IQ mixer and mm-wave head module. In order to do that, a simplified version of the setup in Figure 6.17 has been used, where the active tuner was only placed at Port 2, while at P1 a simple mm-wave extender module was employed, fed with an RF signal with fixed power. First, a 1 port calibration at port 1 was performed. Then, Port 1 was directly connected to Port 2 at the waveguide reference plane, forming a flush thru connection (see, Figure 6.18). In this way, Port 1 can be conveniently used to

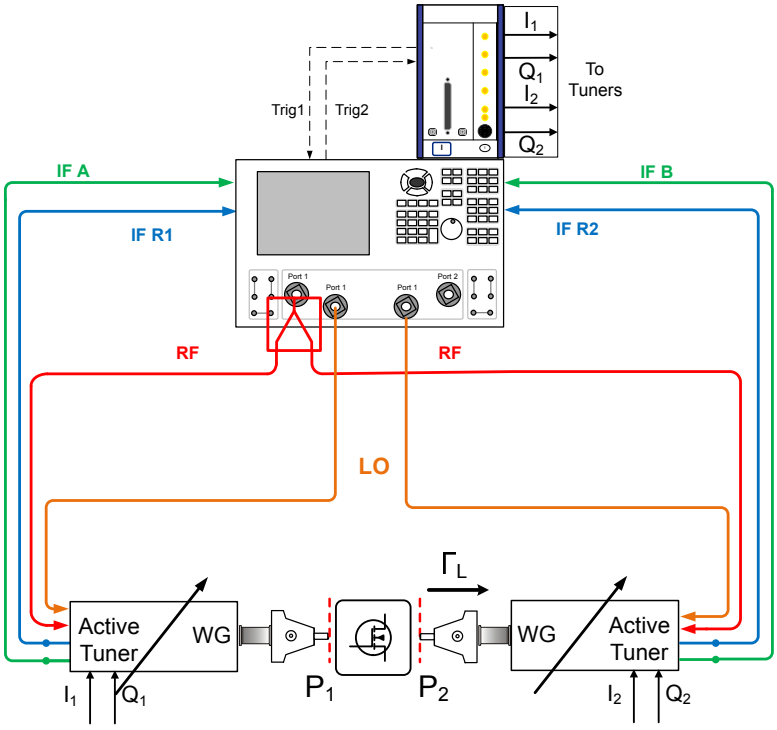


Figure 6.17: Schematic representation of the active load-pull test-bench setup described in Section 6.6.4

actually measure the reflection coefficient presented at its reference plane, which is nothing else than the load synthesized by means of the active tuner at Port2. The first experiment simply consisted in arbitrarily modulate the IQ mixer, by varying the module of the IQ vector ($M = \sqrt{V_I^2 + V_Q^2}$) between 0 and 1, and for every module varying the phase of the vector $\phi = arctan(V_Q/V_I)$ between 0 and $2\pi/N$, where *N* is the multiplication factor associated to the specific waveguide head in use. This multiple "arcs" realized in the V_I - V_Q polar space are then translated, by means of modulation and then frequency multiplication, in complete circumferences in the Smith chart, as described in Section 6.6.3. The results of this analysis are reported in Figure 6.19 for three different frequencies, one for each analyzed frequency bandwidth. All three report the reflection coefficient offered from the active tuner seen from port 1. While these measurements cannot prove that the active tuner can be valuable for load pull measurements of realistic devices, they do validate the concept of using an IQ mixer with conventional mm-wave extender modules to obtain active injection at (sub)mm-wave frequencies.

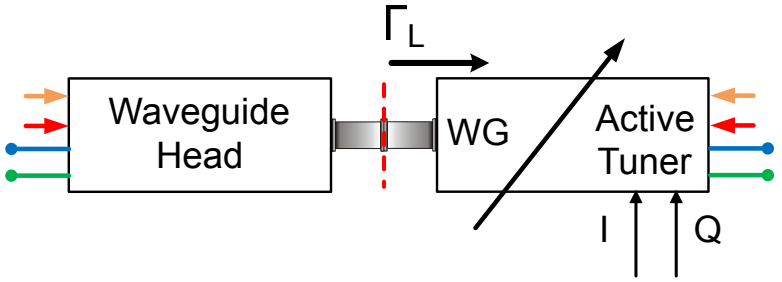


Figure 6.18: Schematic representation of the DUT section of the test-bench employed for the experiments of Section 6.6.5

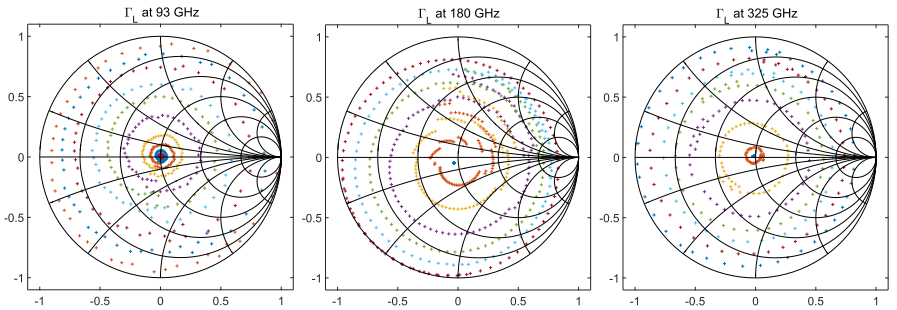


Figure 6.19: Reflection coefficients presented at the output of the active tuner for various V_I-V_Q combination, at different frequencies. a) 93 GHz. b) 180 GHz. c) 325 GHz

6.7. Conclusions

In this chapter a novel method to achieve power control for S-parameters and large signal characterization for mm-wave and sub-mm-wave devices has been presented. The method aims to obtain a refined control of the power available at the DUT, in order to provide constant and controlled power during frequency sweep, thus obtaining a controlled dynamic range versus frequency. Measurement results have been shown highlight the power level control capabilities at the mm-wave extender ports in the WR-10, WR-5 and WR-3 waveguide bandwidths. A study has also been performed in order to showcase the stability performances of the proposed setup and their dependence on the system thermal state. The power controlled measurement setup finds one application in the small-signal characterization of ICs (amplifiers) and transistors, when the standard measurement approach doesn't guarantee the enforcing of small-signal drive for the DUT. With some modifications, the proposed setup can be used for single tone load-pull measurements. In this chapter, the concept of realizing an active tuner by means of millimeter wave extenders and IQ mixers has been described, and preliminary results show the capability of the tuner to actually change the load conditions at the output of a generic DUT.

7

Conclusions

The goal of this dissertation is to provide a set of guidelines for the successful and accurate characterization of (sub)millimeter wave devices. The limits of current measurement approaches have been first thoroughly analyzed, then strategies for calibration, small and large signal measurements have been presented. The results of the work described in this thesis are summarized in Section 7.1, then suggestions for future work are provided in Section 7.2

7.1. Outcome of the thesis

7.1.1. Calibration

The first part of this thesis, relates to the realization of accurate calibration strategies and structures, to improve the quality of on-wafer measurements at extremely high frequencies, i.e., for frequencies higher than 75 GHz. In order to do that, the problem of planar calibration has been approached on three different aspects. First of all, the probe tip calibration of VNA-based measurement setups has been analyzed, as typically performed by using an off-wafer (enclosed in a different environment as the final DUT) calibration substrate. The errors arising by the use of calibration-transfer techniques have been discussed and, to a certain extent, quantified. By using the acquired information, the conclusion reached in this thesis is that it is best practice to realize calibration substrates by using dielectric materials which are electrically thin (i.e., with a low dielectric coefficient), in order to minimize the effect of multi-mode propagation. Also, in case the DUT is realized in silicon technology,it is best to use materials presenting a dielectric coefficient as close as possible to the one of silicon back-end-of-line (typically SiO_2, with $\varepsilon_r \simeq 4.1$), allowing to minimize the effect of spurious capacitances associated to calibration transfer. The best candidate for the manufacturing of calibration substrates has been identified, in this dissertation, to be *fused silica*. As a matter of fact fused silica presents a dielectric constant ($\varepsilon_r \simeq 3.69$) which is sensibly lower than the one of alumina ($\varepsilon_r \simeq 9.1$), conventionally used as standard material for calibration substrates, and

it is also close to the dielectric constant of silicon BEOL. Fused silica presents the advantage of being offered in thin wafers (thickness as low as 200 μm), allowing further increasing the cutoff frequency for surface-modes, and it is prone to be used in conventional photolitographic processes, guaranteeing high manufacturing precision.

The preferable approach for probe-tip calibration, however, would be to use calibration standards manufactured in the same environment as the final DUT, i.e., in case of silicon technology, to embed the calibration standards into silicon BEOL. In this case, all the challenges related to calibration transfer are automatically eliminated. On top of that, the relatively low dielectric constant of silicon BEOL, together with the reduced thickness (typically in the order of 10 μm), prevent the onset of higher order modes for all the frequencies of interest. The challenge, in this case, is in the accurate knowledge of the electromagnetic properties of the calibration standards, as embedded in a stratified media and with low manufacturing predictability. Even when calibration approaches requiring little knowledge of the standards are considered, like the thru-reflect-line calibration (TRL), at least the characteristic impedance of the employed transmission lines needs to be accurately known. A thorough analysis of the conventional approaches reveals that, for (sub)millimeter wave frequencies, and when lossy and stratified materials are employed, none of the measurement-based characteristic impedance extraction methods guarantees an adequate accuracy, mostly because of their inability to take into account (the always present) inductive transitions between the measurement plane and the transmission line. In Section 3.2.2 a characteristic impedance extraction method, based on electromagnetic simulations, has been proposed. This method allows avoiding any possible inductive transition as it only considers the (uniform) transmission line used for calibration, while all the material properties (including all the sources of loss) and electromagnetic phenomena taking place in the calibration structure are taken into account. When benchmarked towards the state-of-the-art measurement-based method (*calibration comparison method*), the proposed method provides comparable results when measuring homogeneous (i.e., with no geometrical discontinuity) transmission lines, while outperforming the conventional method when inductive fixtures are employed between the contact pads and the transmission lines.

To complete the study of on-wafer measurements at (sub)mm-waves, also the de-embedding of on-wafer fixtures has been taken into account. In order to do that, in Chapter 4 of this dissertation, a novel transmission line, called *capacitively loaded inverted CPW (CL-ICPW)*, has been introduced. This kind of structure allows realizing transmission lines for TRL calibration directly at the desired low metal level (M1 or M2), setting the calibration reference plane at the intrinsic DUT ports. The proposed lines' architecture is based on a slow-wave kind of approach where a capacitive load, created by means of a slotted metal plane, is placed at a metal level higher than the one of the transmission line, which is exposed to the substrate. The capacitive load allows confining the propagating field in the weakly dispersive BEOL, while reducing the propagation in the lossy substrate. If properly designed, this transmission line is well behaved and can be used for direct TRL calibration at M1,

as its characteristic impedance can be extracted by the EM-based method described in Section 3.2.2, without having to perform multi-step calibration/de-embedding procedures. When used to measure SiGe transistors at the intrinsic plane and benchmarked towards the existing model, the proposed low-metal calibration kit provides realistic results, showing the possibility for the use of this approach in model extraction and validation applications.

7.1.2. Small and large signal measurements

The second part of the dissertation has been dedicated to the analysis and development of state-of-the-art measurement approaches for small signal and large signal measurements at millimeter and sub-millimeter wave frequencies. First, a waveguide based mixed-signal active load pull system, operating in the frequency range between 50 and 65 GHz, has been presented. The proposed setup expands the scope of an existing load-pull approach (the mixed-signal active load-pull [80]) to higher frequencies, where the implementation of active load pull setups presents challenges related to high losses, low dynamic range and low measurement stability. The waveguide-based architecture, when compared with solutions based on coaxial-based test-sets, provides higher stability and lower losses. The proposed solution has been proved to be effective for small device (i.e., transistors) model validation. Also, the same implementation has been used for the testing of pre-matched millimeter wave ICs, demonstrating how also in this case a secondary (refined-)tuning and optimization of the performances can become crucial to allow the maximization of the output power, at frequencies where the available power is still limited. Finally, an alternative use of this setup has been proposed for breakout characterization, where the load-pull capabilities can be used to characterize realistic breakout circuits, without the need of on-board modifications which could provide non-realistic circuit behaviors.

While the mixed signal active load pull is a peculiar measurement technique requiring a customized hardware setup, in Chapter 6 the attention has been shifted towards exploiting the existing and commercially available measurement setup, i.e., VNAs and frequency extenders for millimeter wave, and expand their capabilities for better accuracy and power measurements. The most compelling challenge when performing small (and large) signal characterization using VNA extenders is the inability to properly control the power, as the internal ALC of the VNA is excluded from the measurement loop. In Chapter 6 a method for achieving power levelled S-parameter measurement has been presented, requiring the use of conventional hardware setup (VNA and extenders) and a power meter for power calibration. The proposed method requires a specific calibration procedures allowing to properly control, set and measure the power at the measurement plane, while maintaining the vector calibration. The capability to measure power allows also performing large signal measurements, as quantities like power gain and efficiency can be directly measured. At the end of the dissertation, the possibility to expand the capabilities of the setup to achieve load-pull measurement at millimeter wave has also been presented. The proposed method involves the use of IQ modulation at lower frequencies (i.e., before the frequency up-conversion provided by the millimeter wave

extenders) to obtain load-pull capabilities at the measurement test-port. Preliminary results show how the proposed technique is actually capable of providing any possible load condition at the measurement test port, when tested on passive devices (i.e., waveguide sections), finally opening the possibility to active load-pull measurements at any frequencies covered by millimeter wave extenders.

7.2. Future work

While this work wants to provide general guidelines for achieving accurate millimeter wave measurements, many aspects for both calibration and measurement architectures need to be further explored.

7.2.1. Cross-talk correction during on-wafer calibration

VNA measurements can be affected by errors arising from coupling between the measurement ports. These errors are typically taken into account from conventional error models (i.e., 12 terms error model) with a single isolation term, which becomes insufficient when on wafer measurements are considered [109]. For this reason, more general error models, like the 16-terms [110, 111], have been introduced to improve the cross-talk correction. Different studies have been realized, to show how the 16-terms error model can lead to calibration improvement both with lumped based calibration approaches [31] or TRL calibration [109]. The effect of cross-talk on on-wafer calibration depends on different parameters, like calibration artifact geometry (access line length, distance between artifacts, distance between probe-pads) or type, probe pitch, substrate (material and thickness) and frequency. In theory, if all these parameters (or the related effects) could be kept constant, during calibration and measurements, the cross-talk effect could be estimated (and corrected for) quite accurately by means of the 16-terms model. When considering (multiline)-TRL calibration procedures, the estimate and correction of the cross-talk error becomes particularly cumbersome, as the distance between the probe tips cannot be kept constant during the procedure, due to the inherent requirements for transmission lines with different lengths. On top of that, also when measuring different DUTs, even if assuming these to be embedded in the same substrate as the calibration kit, the distance between the probe-tips can vary significantly depending on the DUT geometry. It would be essential, for a proper correction of the crosstalk error, to establish a distance-dependent cross-talk model. While the work of [109] tried to give a first order estimate of the distance dependency of the cross-talk model, all the measurements were realized by using a TRL calibration as reference, which would be inherently affected by a distance-dependent cross-talk error, and the correction was never scaled to the DUT length. Future investigations will need to more thoroughly address the problem of the distance dependency in cross-talk correction, by providing solutions allowing to properly scale the cross-talk error to the DUT length, in order to give an accurate correction irrespectively of the geometry.

7.2.2. Comparing CL-ICPW to conventional de-embedding

The use of the CL-ICPW lines for direct calibration at low metal levels has been proved, in Chapter 4, to be effective when characterizing transistors. However, no real comparison between direct TRL calibration with CL-ICPW and more conventional de-embedding techniques for transistor characterization (short-open, short-open-thru, SOLT, split-line, etc.) has been realized so far. While all techniques are expected to perform similarly at lower frequencies, due to the lower impact of the distributed effects when the wavelength is high enough, it is also expected to see deviation in accuracy for the different techniques as the frequency increases. The individuation of the frequency limitations, and the quantification of the actual improvements provided by the use of CL-ICPWs versus frequency, would give more insight into the scope of the application of this new geometry, allowing to identify a set of guidelines for effective characterization (and modeling) of transistors at millimeter and sub-millimeter wave frequencies.

7.2.3. Expanding the use of active load-pull at millimeter waves

Active load-pull is conventionally considered a technique exclusively used to measure highly mismatched devices, in order to characterize non-linear devices for their response in realistic loading conditions. In Chapter 5 alternative uses of active load-pull have been proposed, when a mixed-signal active load-pull setup has been used to characterize pre-matched ICs, in order to perform a sort of "second-tuning". Also, it has been envisioned the use of active load-pull for breakout characterization of linear devices. These *alternative* uses of active load-pull techniques need to be further investigated and validated by means of measurements on several, different DUTs, in order to better understand the real usefulness and the limitations of the proposed approaches. Especially for the use in breakout characterization, countless applications can be envisioned where multiple stages of complex ICs need to be separately characterized. While the approach proposed in this dissertation appears to be promising, it will need to be tested in realistic situations and different applications to finally prove its effectiveness.

7.2.4. Automatic active load-pull at sub-millimeter wave frequencies

As at the end of Chapter 6 the possibility to realize active tuning at mm-Wave by using multiplied modulation has been presented, no real load-pull measurement has been shown in this dissertation. In order to turn the active tuner concept into a complete active load-pull system, few steps need to be achieved. First, the full characterization of the transfer function of the active tuner is needed. As a matter of fact, being composed by non-linear components (IQ mixer, frequency multiplier), the relation between I and Q signals and the load impedance that can be synthesized by the tuner can become quite complex. A complete knowledge of this behavior would allow implementing a robust convergence algorithm, which is the next step towards the exploitation of the load-pull capabilities. Due to the open-loop nature of the proposed architecture, and the complex response of the active tuner, the

choice of the convergence algorithm, and its implementation, would have to be thorough, taking care of achieving both robustness (i.e., the capability to always converge to the desired load impedance, with the requested accuracy) and speed. Finally, the possibility for hardware modifications to the mm-wave heads for best performances will have to be investigated. Mm-wave extenders are designed for use in linear measurements (i.e., S-parameters) and, in order to achieve best performances for large-signal (and high DUT power) some adaptation will be needed, like increasing available power at DUT load (using additional power amplifiers and pre-matching tuners), avoid compression of down-conversion mixer (using high-coupling reflectometers, or introducing attenuation in the coupled arms), minimizing the injection of spurious signals from LO feed-through and multiplier harmonics. Some of these aspect have being already approached, and are still being improved by the ELCA group in TU Delft and Vertigo Technologies, which with MMW STUDIO LP is proposing the first scalable load-pull solution for millimeter and sub-millimeter wave measurements on the market.

A

Wave formalism, characteristic impedance and impedance transformation

A.1. Travelling modes and travelling waves

When considering a general waveguide section, assumed uniform and supporting electromagnetic fields propagating on a generic axe z, defined by a propagation constant γ, the solution to the source-free Maxwell equations allows to define the existence of a *forward* and a *backward* traveling modes, which linear combination allows to describe the total electric field E and magnetif field H in a single mode, so that their transverse components result to be:

$$\mathbf{E_t} = c_+ e^{-\gamma z}\mathbf{e_t} + c_- e^{+\gamma z}\mathbf{e_t} \equiv \frac{v(z)}{v_0}\mathbf{e_t} \tag{A.1}$$

$$\mathbf{H_t} = c_+ e^{-\gamma z}\mathbf{h_t} - c_- e^{+\gamma z}\mathbf{h_t} \equiv \frac{i(z)}{i_0}\mathbf{h_t} \tag{A.2}$$

where e_t and h_t are the transverse components normalized electric and magnetic field, respectively. v and i are called *waveguide voltage* and *waveguide current*, while v_0 and i_0 are normalization constants, allowing v and i to have units of voltage and current, respectively. v, i, v_0 and i_0 are defined so that the complex power p crossing a given transfer plane may be defined as:

$$p = vi^* \tag{A.3}$$

and, for consistency:

$$p_0 = v_0 i_0^* \tag{A.4}$$

It is then possible to define the forward-mode characteristic impedance by using:

$$Z_0 \equiv \frac{v_0}{i_0} = \frac{|v_0|^2}{p_0^*} = \frac{p_0}{|i_0|^2} \tag{A.5}$$

By normalizing the forward and backward modes of Equations (A.1) and (A.2), it is possible to define the forward and backwards traveling waves as:

$$a_0 = \sqrt{Re(p_0)}c_+ e^{-\gamma z} = \frac{\sqrt{Re(p_0)}}{2v_0}(v + iZ_0) \tag{A.6}$$

and

$$b_0 = \sqrt{Re(p_0)}c_+ e^{+\gamma z} = \frac{\sqrt{Re(p_0)}}{2v_0}(v - iZ_0) \tag{A.7}$$

This definition allows to define the reflection coefficient Γ_0 at a certain section z of the waveguide as:

$$\Gamma_0(z) \equiv \frac{b_0(z)}{a_0(z)} \tag{A.8}$$

and the real power as:

$$P(z) = |a_0|^2 - |b_0|^2 + 2Im(a_0 b_0^*)\frac{Im(Z_0)}{Re(Z_0)} \equiv |a_0|^2\left[1 - |\Gamma_0|^2 - 2Im(\Gamma_0)\frac{Im(Z_0)}{Re(Z_0)}\right] \tag{A.9}$$

A.2. Pseudo-Waves

Due to the complexity of the definition of the travelling waves, it is sometimes convenient to use an alternative mathematical artifact. Considering an arbitrary impedance Z_{ref} such as $Re(Z_{ref}) > 0$, the *pseudo-waves* a and b can be defined as:

$$a \equiv \left[\frac{|v_0|}{v_0}\frac{\sqrt{(Re(Z_{ref}))}}{2|Z_{ref}|}\right](v + iZ_{ref}) \tag{A.10}$$

$$b \equiv \left[\frac{|v_0|}{v_0}\frac{\sqrt{(Re(Z_{ref}))}}{2|Z_{ref}|}\right](v - iZ_{ref}) \tag{A.11}$$

Using these definitions, the pseudo-reflection coefficient Γ is defined as:

$$\Gamma(z) \equiv \frac{b(z)}{a(z)} \tag{A.12}$$

And the real power becomes:

$$P = |a|^2 - |b|^2 + 2Im(ab^*)\frac{Im(Z_{ref})}{Re(Z_{ref})} \equiv |a|^2\left[1 - |\Gamma|^2 - 2Im(\Gamma)\frac{Im(Z_{ref})}{Re(Z_{ref})}\right] \tag{A.13}$$

It is possible to demonstrate that traveling waves and pseudo-waves are equivalent when the reference impedance is equal to the characteristic impedance of the waveguide, i.e., $a(Z_0) = a_0$ and $b(Z_0) = b_0$. In this sense, the pseudo-waves add a level of arbitrariness in the use of the reference impedance, which may become handy in particular cases, such as when using lossy transmission lines with complex Z_0.

A.3. S-matrix, Z-matrix, cascade matrix

Let's consider a linear N-port circuit, on which each port is connected to an uniform, semi-infinite waveguide, and let's suppose that a reference plane exists in each waveguide where monomodal propagation insists. For every port i, it is possible to arbitrarily choose a reference impedance Z_{ref}^i, allowing the definition of the pseudo waves $a_i(Z_{ref}^i)$ and $b_i(Z_{ref}^i)$. For convention, the direction of the forward wave a_i can be chosen to be towards the port junction, and in this case a_i is also called *incident* wave, while b_i can be addressed as *reflected* wave. The incident and reflected pseudo-waves, at every port, are linearly related to each other through the so called pseudo-scattering matrix **S**, defined so that its elements S_{ij} satisfy the relation:

$$\begin{pmatrix} b_1 \\ \vdots \\ b_n \end{pmatrix} = \begin{bmatrix} S_{11} & \cdots & S_{1n} \\ \vdots & \ddots & \vdots \\ S_{n1} & \cdots & S_{nn} \end{bmatrix} \cdot \begin{pmatrix} a_1 \\ \vdots \\ a_n \end{pmatrix} \tag{A.14}$$

where n is the number of ports, or vectorially:

$$\mathbf{b} = \mathbf{Sa} \tag{A.15}$$

Equation Equation (A.15) implies that also the vectors related to voltages and amplitude **v** and **i** are linearly related, through the impedance matrix **Z** so that:

$$\mathbf{v} = \mathbf{Zi} \tag{A.16}$$

Please notice that, when $Z_{ref}^i = Z_0^i$, then $\mathbf{S} = \mathbf{S_0}$, where $\mathbf{S_0}$ is the (true) scattering matrix, defined in a similar fashion as Equation (A.15) but using the traveling waves. In this dissertation, for simplicity, we always refer to the pseudo-scattering matrix as just scattering matrix, and to the pseudo-scattering parameters as just scattering parameters or S-parameters.

Another type of linear relationship betwees pseudo-waves is represented by the cascade matrix **T**. In the example of a 2-port linear network with $S_{21} \neq 0$, where the reference impedance at port 1 and port 2 are, respectively, Z_{ref}^i and Z_{ref}^j, then:

$$\begin{bmatrix} b_1(Z_{ref}^i) \\ a_1(Z_{ref}^i) \end{bmatrix} = \mathbf{T^{ij}} \begin{bmatrix} a_2(Z_{ref}^j) \\ b_2(Z_{ref}^j) \end{bmatrix} \tag{A.17}$$

Conversion between scattering matrix and cascade matrix is possible using:

$$\mathbf{R} = \frac{1}{S_{12}} \begin{bmatrix} S_{12}S_{21} - S_{11}S_{22} & S_{11} \\ -S_{22} & 1 \end{bmatrix} \tag{A.18}$$

A

and

$$\mathbf{S} = \frac{1}{R_{22}} \begin{bmatrix} R_{12} & R_{11}R_{22} - R_{12}R_{21} \\ 1 & -R_{21} \end{bmatrix} \tag{A.19}$$

The cascade matrix is particularly convenient when considering cascades of networks, as the cascade matrix of two series-connected 2-port networks is equal to the product of the two cascade matrices, as long as the connecting ports are composed of identical waveguides, with identical reference impedance.

A.3.1. Impedance renormalization

Considering two sets of pseudo waves, described by the same v and i but different reference impedances Z_{ref}^{n} and Z_{ref}^{m}, the two sets are related by the linear relationship:

$$\begin{bmatrix} a(Z_{ref}^{n}) \\ b(Z_{ref}^{n}) \end{bmatrix} = \mathbf{Q}^{nm} \begin{bmatrix} a(Z_{ref}^{m}) \\ b(Z_{ref}^{m}) \end{bmatrix} \tag{A.20}$$

Where $\mathbf{Q^{nm}}$ is described by:

$$\mathbf{Q}^{nm} \equiv \frac{1}{2Z_{ref}^{m}} \left| \frac{Z_{ref}^{m}}{Z_{ref}^{n}} \right| \sqrt{\frac{Re(Z_{ref}^{n})}{Re(Z_{ref}^{m})}} \begin{bmatrix} Z_{ref}^{m} + Z_{ref}^{n} & Z_{ref}^{m} - Z_{ref}^{n} \\ Z_{ref}^{m} - Z_{ref}^{n} & Z_{ref}^{m} + Z_{ref}^{n} \end{bmatrix} \tag{A.21}$$

or

$$\mathbf{Q}^{nm} \equiv \sqrt{\frac{1 - j\frac{Im(Z_{ref}^{m})}{Re(Z_{ref}^{m})}}{1 - j\frac{Im(Z_{ref}^{n})}{Re(Z_{ref}^{n})}}} \frac{1}{\sqrt{1 - \Gamma_{nm}^{2}}} \begin{bmatrix} 1 & \Gamma_{nm} \\ \Gamma_{nm}^{2} & 1 \end{bmatrix} \tag{A.22}$$

Where:

$$\Gamma_{nm} = \frac{Z_{ref}^{m} - Z_{ref}^{n}}{Z_{ref}^{m} + Z_{ref}^{n}} \tag{A.23}$$

Equations (A.20) to (A.22) represent the exact expressions of a *complex* impedance transform. A special case of impedance transformation, is when a waveguide is terminated on a load, characterized by an impedance Z_{load}. In this case, the reflection coefficient at the reference plane of the termination can be computed as:

$$\Gamma(Z_{ref}) = \frac{Z_{load} - Z_{ref}}{Z_{load} + Z_{ref}} \tag{A.24}$$

When 2-ports networks are considered, the simplest way of computing the impedance transformation of the scattering matrix is to first compute the related cascade matrix, then transform the impedance for the cascade matrix, then transform back to scattering matrix. In this case, supposing we have port 1 with a reference impedance Z_{ref}^{n} and port 2 with a reference impedance Z_{ref}^{m}, and that we want to transform the cascade matrix T^{nm} to a reference impedance Z_{ref}^{p} at port 1 and a reference impedance Z_{ref}^{q} at port 2, the resulting cascade matrix T^{pq} will be:

$$\mathbf{T^{pq}} = \mathbf{Q^{pn}T^{nm}Q^{mq}} \tag{A.25}$$

Where **Q** is defined as in Equation (A.22). In the common case where the two-ports use identical reference impedances, and are transformed to other two identical reference impedances, then:

$$\mathbf{T^{pp}} = \mathbf{Q^{pn}T^{nn}Q^{np}} = \frac{1}{1-\Gamma_{pn}^2}\begin{bmatrix} 1 & \Gamma_{pn} \\ \Gamma_{pn} & 1 \end{bmatrix}\mathbf{T^{nn}}\begin{bmatrix} 1 & -\Gamma_{pn} \\ -\Gamma_{pn} & 1 \end{bmatrix} \tag{A.26}$$

A.4. Power Waves

A popular mathematical artifact, often employed as alternative to the pseudo waves, is represented by the *power waves*, sometimes referred as *Kurokawa waves* [112]. These waves are generically defined at a port i of a multi-port network, with port impedance (or port number) $\hat{Z}$, with $Re(\hat{Z}) > 0$. In this case the power waves are defined as:

$$\hat{a}(\hat{Z}) \equiv \frac{v + i\hat{Z}}{2\sqrt{Re(\hat{Z})}} \tag{A.27}$$

$$\hat{b}(\hat{Z}) \equiv \frac{v - i\hat{Z}^*}{2\sqrt{Re(\hat{Z})}} \tag{A.28}$$

Please note that the power waves reduce to the pseudo-waves *only* when $\hat{Z}$ is real and $Z_{ref} = \hat{Z}$. The power waves are designed in order to always satisfy the simple power equation:

$$p = |\hat{a}|^2 - \left|\hat{b}\right|^2 \tag{A.29}$$

The relation of Equation (A.29) is only valid for pseudo waves when Z_{ref} is real. Power-wave scattering parameters and reflection coefficient can be computed in a similar fashion as the pseudo-wave counter parts. For example:

$$\hat{\Gamma}(\hat{Z}) \equiv \frac{\hat{b}(\hat{Z})}{\hat{a}(\hat{Z})} = \frac{v - i\hat{Z}^*}{v + i\hat{Z}} = \frac{Z_{load} - \hat{Z}^*}{Z_{load} + \hat{Z}} \tag{A.30}$$

Where the last equivalence is true when there is a termination to a specific load Z_{load}. Equation (A.30) is not equivalent to Equation (A.24) when a complex port impedance is used. This can be understood with a simple example. Let's consider the reflection coefficient of a short circuit ($v = 0$). For pseudo-waves $\Gamma(Z_{ref}) = -1$ regardless of the reference impedance. For power waves, instead:

$$v = 0 \Rightarrow \hat{\Gamma}(\hat{Z}) = \frac{-\hat{Z}^*}{\hat{Z}} \tag{A.31}$$

Which is equal to -1 only when $Im(\hat{Z}) = 0$. This example shows how the use of power-waves may bring less intuitive results when applied to situations in which complex reference impedances are employed. This is one of the reasons why pseudo-waves are generally considered as the most convenient and general formalism to describe linear networks. For a more in-dept description of the use of travelling-, pseudo- and power-waves, and the related implications, the reader is encouraged to read [19].

B

CPW analysis by means of conformal mapping

When considering a conventional CPW (air and substrate of permittivity ε_{r2}), i.e., ε_{r1} from Figure 4.2, the total capacitance per unit length associated to this CPW can be described from [71] as:

$$C_{CPW} = C_2 + C_{air} \tag{B.1}$$

$$C_2 = 2\varepsilon_0 (\varepsilon_{r2} - 1) \cdot \frac{K\left(k_0^{'}\right)}{K(k_0)} \tag{B.2}$$

$$C_{air} = 4\varepsilon_0 \cdot \frac{K\left(k_0^{'}\right)}{K(k_0)} \tag{B.3}$$

Where C_2 is the capacitance associated to the medium with dielectric constant ε_{r2}, C_{air} is the capacitance associated to the CPW when all the space is filled with air, K is the elliptic integral of the first kind, $k_0 = \frac{S}{S+2W}$ and $k_0^{'} = \sqrt{1-k_0^2}$. If we now consider this line as loaded, capacitively, by a shield, then the total capacitance associated to this CL-ICPW will be:

$$C_{Tot} = C_{CPW} + C_1 \tag{B.4}$$

Where C_1 is the capacitance associated to the floating shield. In the assumption that the thickness of the substrate h_{S2} is very large and that $S \gg h_{S1}$, then C_1 can be approximated as [113]:

$$C_1 \cong \frac{\varepsilon_0 \varepsilon_{r1} W}{h_{s1}} \tag{B.5}$$

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Summary

As the number of wireless applications increases every year, overcrowding the RF/microwave spectrum, research community and industry are gradually starting to dedicate more attention to the less exploited (sub)millimeter wave spectrum, spanning from 30 GHz to 1 THz. While the high frequency and large available bandwidth of the latter promises very fast communication and the space for countless new applications, the development of new devices working at high frequency is hampered by a series of challenges affecting both technology development and implementation. One of the bottlenecks in new technology development is the availability of accurate and reliable measurement techniques, to support the design and the model validation of both passive and active devices working at (sub)millimeter wave frequencies. As a matter of fact, the test and measurement market dedicated to sub-THz applications has presented small developments in the last decades, with the core instrumentation and measurement techniques still based on the same principles dedicated to lower frequency applications. This thesis is dedicated to the development of calibration and measurement techniques for the characterization of (sub)millimeter wave devices, allowing to bridge the gap between the current available measurement instrumentation and the new needs in the sub-THz range. This is done by mainly addressing two aspects: the development of advanced techniques and artifacts for the characterization of electronic devices in their native environment (i.e., on-wafer), and the implementation of measurement techniques allowing to characterize the small- and large-signal behavior of devices and circuits at (sub)millimeter wave, while overcoming the instrument-related challenges present at those frequencies. **Chapter 2** is dedicated to a description of conventional measurement instrumentation for microwave devices (mainly based on the Vector Network Analyzer, or VNA), and the challenges related to the instrument calibration, especially when on-wafer measurements are needed. As a matter of fact, calibration is a fundamental procedure, preceeding the device measurements, and necessary to correct for all the environmental and statistic errors which are introduced when the instrument is connected to the device under test (DUT). The non-shielded nature of the interconnection between the instrument and the on-wafer DUT, which is typically realized in his final part using wafer probes, increases complexity in the error correction. On-wafer calibration becomes even more challenging when frequencies increase towards the millimeter wave and sub-THz ranges, as effects like multi-mode propagation and errors related to calibration transfer between substrates become dominant. This is addressed in **Chapter 3**, where two points of view are employed to try to improve measurement accuracy. First, it is shown how, by accurately choosing the substrate material employed for the realization of the calibration kit, errors related to multimode-propagation and calibration transfer can be minimized. Both errors may be almost completely can-

celed when the calibration kit is realized directly in the environment where the DUT is embedded, which is typically semiconductor back-end-of-line (BEOL). In the second part of Chapter 3, a novel technique is proposed to design and characterize transmission lines used for the realization of thru-reflect-line (TRL) calibration kits in silicon BEOL. One main purpose of on-wafer calibration is to bring the measurement reference plane as close as possible to the DUT, in order to correct for all the errors related to the interconnection and providing measurement results as close as possible to the actual device behavior. As, typically, semiconductor based DUTs (like transistors) are embedded into the BEOL using special and complex fixtures, the problem remains on how to also exclude these fixture from the measurements, after the system is already calibrated. This is typically done by employing correction techniques called de-embedding, which in a similar fashion to calibration techniques allow to estimate the effects of the fixtures, and computationally exclude them from the measurements. While conventional de-embedding techniques start to lose accuracy when the frequencies become higher than 40 GHz, it would be preferrable to be able to directly calibrate the measurement system to bring the measurement reference plane directly at the intrinsic DUT plane, thus correcting for the fixture in the same step of the rest of the calibration. **Chapter 4** introduces the design of a special transmission line, the capacitively loaded inverted coplanar waveguide (or CL-ICPW), that can be built in the lower levels of the BEOL, allowing direct access to the intrinsic DUT plane. The functioning of the transmission line is based on an additional capacitive load, which allows to confine the propagating field in the low-dispersive oxide of the BEOL, reducing the losses into the dispersive silicon of the substrate. This feature allows the CL-ICPW to be well-behaved, so that it can be used for the realization of TRL calibration kits, placing the reference plane as close as possible to the intrinsic DUT.

The second part of this dissertation is dedicated to the realization of large-signal measurement setups, dedicated to the characterization of active devices (mainly, transistors and power amplifiers) at frequencies higher than 50 GHz. Most of the main large-signal techniques are based on measuring the devices performances while varying the incident power, while sometimes changing the loading condition presented to the device when this is driven in non-linear operation (load-pull). **Chapter 5** describes the implementation of a dedicated active load pull setup for measurements in the frequency range from 50 GHz to 65 GHz. In order to optimize the power performances of the system, the setup is completely realized using rectangular waveguides to exploit the low losses in respect to coaxial systems. The implementation of the system is based on the existing mixed-signal active load-pull, developed in TU Delft and commercialized by Anteverta-MW at lower frequencies (i.e., up to 40 GHz). This sort of system can be used for characterization of transistors as well as circuits. A novel use of the active load-pull system is dedicated to the characterization of circuit breakouts, in order to avoid circuit modifications that might alter the actual behavior and polarization of active devices, while providing the necessary realistic termination using active load-pull techniques.

When measurements at frequencies higher than 70 GHz are needed, conventional VNAs cannot be used as they are limited in performance by their (coaxial) connec-

torization. The conventional method to circumvent these limitations is to *extend* the frequency range of the VNA by employing waveguide banded millimeter wave extender modules. These modules are based on frequency multiplication to up-convert the signal coming from the VNA to a desired frequency bandwidth, and they typically include dedicated reflectometers and down-convertion mixers in order to sample the *incident* and *reflected* waves at high frequency, and then convert them to lower frequencies to allow acquisition with the VNA. The main problem of employing these waveguide extenders is that they exclude the capability of controlling the power delivered to the DUT during conventional VNA operation. **Chapter 6** focuses on a novel method, based on a computer-aided characterization of the non-linear behavior of the extender modules, to ultimately be able to control the power delivered to the DUT by modulating the power generated, at lower frequencies, by the VNA. Using a dedicated calibration procedure, the system is capable to control and measure the power at the test-port, so that the correct power driving can be guaranteed during small-signal measurements, and power sweeps can be employed to perform large-signal power measurements, like measurements of gain-compression. The system can be expanded, with the aid of dedicated hardware (IQ mixers and digital-to-analog converters), and an iterative research software, to realize active load-pull measurements at millimeter wave frequencies. The capabilities of the system to control and measure the power, as well as the main capability of modulating the amplitude and the phase of the signals at the system testport, have been demonstrated in this thesis in the frequency range from 75 GHz to 325 GHz, while the system is in principle scalable to any frequency range in which waveguide based millimeter wave extenders are provided.

List of Publications

Journal Papers

F. A. Mubarak, R. Romano, **L. Galatro**, V. Mascolo, G. Rietveld, M. Spirito, "Noise Behavior and Implementation of Interferometer-Based Broadband VNA", *IEEE Trans. Microwave Theory and Tech.*, vol. 67, no. 1, pp. 249-260, Jan. 2019.

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C. De Martino, E. S. Malotaux, **L. Galatro**, M. Spirito, "Direct mm-Wave On-Wafer Power Calibration Employing CMOS as a Transfer Device," in *Proc. 91st ARFTG Microwave Measurement Conference,* Philadelphia, PA, Jun. 2018.

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Curriculum Vitæ

Luca Galatro was born in Salerno, Italy, on the 2nd of May 1986. He received his B.Sc. and M.Sc. (both *cum laude*) in electrical engineering from "Università degli studi di Napoli Federico II", Naples, Italy, in 2009 and 2012, respectively.
In 2012 he joined the Electronic Research Laboratory group (ELCA) of Delft University of Technology, The Netherlands, where he carried out his Ph.D. research on the development of advanced on-wafer calibration and de-embedding techniques for sub-THz VNA-based measurement systems, as well as the implementation of dedicated small-signal and large-signal instrumentation and measurement techniques for the characterization of sub-THz electronic devices.
In 2017 he co-founded and was appointed CEO of Vertigo Technologies B.V., a spin-off of Delft University of Technologies specialized in the development of software and hardware add-ons for VNA-based measurement system, dedicated to the characterization of high-frequency devices and organic materials.