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Challenges of High-Resolution Electron Detection ASICs for SEM Microscopy

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***Abstract*— This paper presents a thorough investigation and evaluation of readout Application-Specific Integrated Circuits (ASICs) tailored for Backscattered Electron (BSE) detection in electron microscopy. The study explores the architecture, operational principles, and performance assessment of integrating and electron counting systems utilized for signal processing in BSE detection. Evaluation of the count rate capability of the readout ASICs is undertaken under diverse conditions, considering variables such as BSE energy, discriminator threshold levels, and preamplifier characteristics. Detailed methodologies for experimental qualification, including test setups, trigger mechanisms, and count rate capability assessments, are outlined to ensure precise evaluation of the ASIC performance. The novel readout ASICs are compared by assessing their maximum output count rate capabilities. Furthermore, we propose strategies to enhance the output count rate by preventing preamplifier saturation, providing insights into the challenges and methods for achieving high-flux rate BSE detection. Experimental verifications validate the effectiveness of the proposed strategies and assessment methodologies in achieving high detection accuracy.**

Keywords—backscattered Electron detection, readout channel, count rate capability, preamplifier saturation, signal shaping block, power-efficient, high time resolution

I. INTRODUCTION

Imaging techniques constitute an essential part of scientific research, facilitating the examination of specimens across different scales and domains. From macroscopic observations of organisms to the subatomic visualization of particles, imaging serves as a cornerstone in elucidating the complexities of natural phenomena. In today's research landscape, there is a growing demand for imaging methods that offer both rapid acquisition and high resolution, allowing scientists to investigate dynamic processes with unprecedented detail. Optical microscopy, the cornerstone of biological and materials science, has long served as the primary imaging modality, providing insights into the intricate structures of cells, tissues, and materials. However, the limitations of optical microscopy in resolving features below the diffraction limit spurred the development of electron microscopy, ushering in a new era of nanoscale imaging. With its finely focused electron beams, electron microscopy offers exceptional resolution and contrast, making it indispensable in fields such as materials science, nanotechnology, and structural biology [1], [2], [3], [4], [5].

Scanning plays a pivotal role in both optical and electron microscopy, albeit with distinct methodologies. In optical microscopy, scanning is not typically employed in image acquisition; rather, the entire field of view is captured in a single exposure, leading to relatively fast imaging speeds. However, in techniques such as confocal microscopy, scanning is utilized to acquire optical sections at different depths within the specimen to make a three-dimensional image. In confocal microscopy, the scanning speed is generally limited by mechanical constraints and the need for precise alignment, resulting in moderate acquisition rates. On the other hand, electron microscopy relies heavily on scanning to capture images of specimen surfaces. The electron beam is systematically scanned across the specimen in a raster pattern, point by point, using electromagnetic coils or scanning mirrors. As the beam scans each point, signals such as secondary electrons or backscattered electrons are detected by the sensor array and assembled into a two-dimensional image. This scanning process allows for the acquisition of high-resolution images with exceptional detail, but it inherently requires more time compared to optical microscopy due to the need to scan each point individually. However, advancements in electron microscopy technology, such as the development of faster scanning mechanisms, multibeam techniques, and improved control algorithms, have significantly enhanced scanning speeds in recent years [2], [5], [6].

With the above-mentioned advancements, electron microscopy emerges as a pivotal technology, offering unprecedented resolution and detail at the nanometer scale. Within electron microscopy, scanning electron microscopy (SEM) occupies a prominent position, renowned for its versatility in revealing surface morphology and structure. This review paper focuses specifically on scanning electron microscopy, with a particular emphasis on the design and optimization of the electron detector readout Application-Specific Integrated Circuit (ASIC). Section II presents the types of commonly used detectors and their configurations, while also addressing the challenges associated with the scanning process and electron detection. Section III provides an overview of the data acquisition chain and the signal processing requirements, followed by a review of readout ASICs designed for single electron detection. Section IV explores the measurement test setup and the test algorithms utilized for the experimental characterization of the readout ASICs. In Section V, the paper concludes with a summary of the topics presented.

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II. Scanning Electron Microscopy

The detectors used in optical and electron microscopy differ significantly, reflecting the differences like the signals being detected. In optical microscopy, detectors such as charge-coupled devices (CCDs) or complementary metal-oxide-semiconductor (CMOS) sensors are commonly used. These detectors are sensitive to visible and/or infrared light, and convert photons into electrical signals, allowing for the capture of high-resolution images with excellent sensitivity. In electron microscopy, detectors such as scintillator-photomultiplier tube (PMT) detectors or scintillator-CCD detectors are employed. These detectors convert signals generated by electron interactions with the specimen into light, which is then detected and converted into electrical signals [6], [7]. In recent years, semiconductor junction-based detectors have emerged as an alternative to traditional scintillator-based detectors in electron microscopy. These detectors utilize semiconductor materials such as silicon or gallium arsenide to directly detect electrons and convert their energy into electrical signals. Semiconductor junction-based detectors offer several advantages over scintillator-based detectors, including higher spatial resolution, faster response times, and lower noise levels [8]. Additionally, they are capable of detecting a wider range of electron energies, making them suitable for a variety of electron microscopy applications. The superior performance of semiconductor junction-based detectors has made them increasingly popular in electron microscopy, paving the way for advancements in imaging technology.

In electron microscopy, backscattered electron (BSE) detection plays a crucial role in providing compositional and topographical information about specimens. One of the key factors influencing imaging quality and scanning speed in electron microscopy is the scanning current intensity and the size of the electron beam spot. The scanning current intensity determines the number of electrons per unit time that interact with the specimen surface, affecting the signal strength and image contrast. Higher scanning current intensities can result in faster imaging speeds but may also lead to increased specimen damage and reduced imaging resolution. Prolonged exposure to high-energy electrons can also degrade the performance of semiconductor detectors over time, leading to reduced sensitivity and increased noise levels. On the other hand, smaller beam spot sizes provide higher spatial resolution and sharper images but may require longer scanning times to cover the entire imaging area. The fast scanning requires very short sampling periods, which, together with the weak secondary current, results in just a few electrons landing on the detector surface per each sampling period [9], [10]. Every backscattered electron impinging on the PIN detector surface creates electron-hole pairs in the detector depletion region as a result of the impact ionization. These electron-hole pairs are separated and directed toward the detector plates by the applied electric field. The detector is followed by a readout ASIC where the energy level and the arrival time of the BSEs can be characterized and registered for image formation.

The electrons reaching the detector may disperse across its surface, resulting in a considerably larger beam spot on the detector surface compared to that on the specimen surface. Configuring the detector surface size becomes crucial to accommodate this broadened beam spot adequately. However, a larger detector area inherently brings about a higher dark current and its accompanying shot noise [11]. Additionally, the noise from the readout ASIC, which depends on the detector parasitic capacitance, scales proportionally with the detector area. Consequently, detectors with larger surfaces yield a lower signal-to-noise ratio (SNR) in the readout ASIC, thus compromising imaging quality. Alternatively, the detector can be partitioned into multiple sensing pixels, each sized to ensure receipt of no more than one electron during each scanning step, leading to a single-electron detection mode of operation [9], [12]. In this mode, individual pulse processing circuits accompany each pixel of the detector, enabling the recording of the arrival time of every BSE with a time resolution defined by the scanning clock frequency.

There are two approaches for BSE detection in electron microscopy. The first approach is the *hybrid pixel detector* whereby each of the pixels in a two-dimensional matrix of a semiconductor detector is connected to its own pulse processing circuit in a readout ASIC. In this setup, the pixel pitch of the detector corresponds to the pitch of the readout channels in the ASIC. Typically, a fine-pitch flip-chip direct physical interconnection method is employed to establish the connection between the detector pixels and the readout ASIC. In contrast, the second approach utilizes a dedicated ASIC to read out the detector pixels, where the pitch of the detector pixel does not necessarily align with the dimensions of the readout channel. In this configuration, the connection between the detector pixels and the ASIC is achieved using an interposer or through the metal traces on a printed circuit board (PCB). This approach allows for flexibility in the design and layout of the detector array and the readout circuitry, enabling optimization for specific imaging requirements and performance metrics [13], [14].

III. Readout ASICs for Signal Processing

The signal processing architectures for BSE detection can be broadly classified into *integrating systems* and *electron counting systems*. In integrating systems, the signal deposited in the detector by incoming electrons is integrated over a given exposure time period. This integral signal processing, as depicted in Fig. 1 (center plot), results in the loss of information contained in the energy of individual electrons. Each electron contributes to the total signal with a weighting factor proportional to its energy, with higher-energy electrons contributing more significantly. However, noise sources such as dark current are also included in the integral, limiting the SNR and dynamic range of the system. Nevertheless, integrating systems excel at processing electron events that arrive close in time without degrading functionality, achieving a linear response even at high fluxes [14], [15], [16].

In contrast, electron counting systems adopt a readout architecture where the signal of each individual electron is processed separately. Typically, this architecture (Fig. 2) comprises a preamplifier to interface the detector, a gain/filter stage to properly shape the signal for the application of interest, and a digitizer stage (including a set of discriminators and counters). When an electron deposits a signal in the detector, a pulse develops at the amplifier output, its amplitude proportional to the detected charge. Discriminators compare this amplitude with various high-resolution thresholds, incrementing a counter associated with an energy bin if the detected electron energy falls within that bin. This approach allows for the acquisition of SEM images

where different sections of the incoming spectrum are sampled simultaneously [15].

The operation of a readout channel in an electron counting system is illustrated in Fig. 1 (bottom plot). However, one limitation of electron counting systems, as demonstrated in Fig. 1 (electron events 4 and 5), is the necessity of a minimum time interval between two consecutive electrons to prevent their signals from overlapping, which could distort the measurement of the total number of detected electrons and their energies. Due to the stochastic nature of electron arrival times, there exists a probability that two electrons deposit their energy in the detector very closely in time, resulting in the overlap of their signals in the processing chain. This phenomenon, known as pileup, occurs particularly at high flux rates and leads to distortion in pulse amplitude measurements and subsequent loss of counts, also referred to as dead time losses. Analytical models have been proposed to estimate dead time losses, with the paralyzable and nonparalyzable detector modes being commonly used in the literature [14].

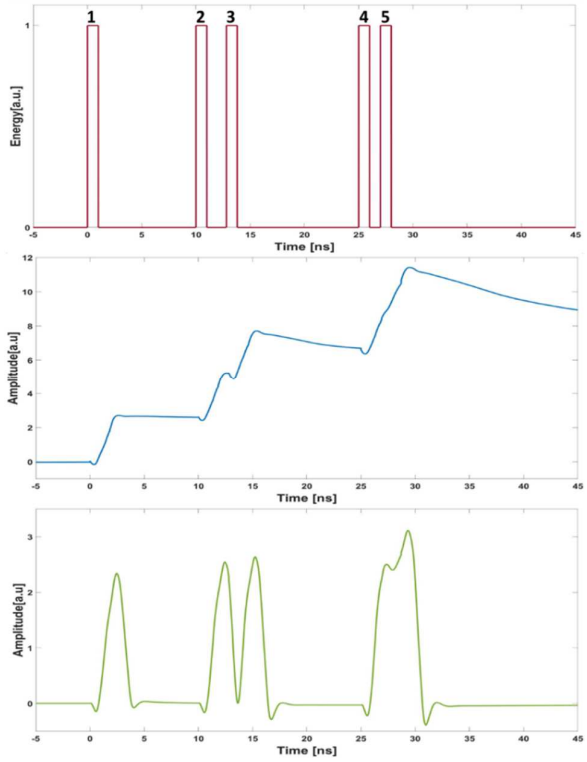

Fig. 1. Illustration of the operation of energy integrating (central plot) and electron counting (bottom plot). The top plot illustrates the moment electrons hit the detector surface. Electrons 4 and 5 suffer from pileup in the electron counting operation.

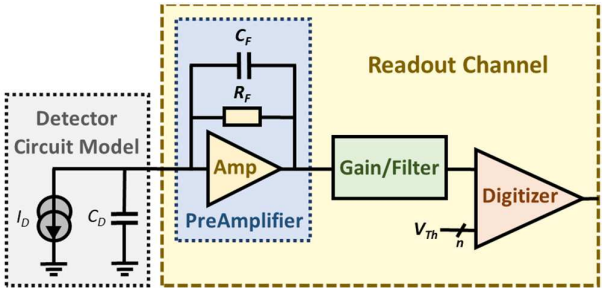

Fig. 2. Simplified block diagram of the readout channel.

In BSE detection ASICs, the objective is to count the total number of BSEs impinging the entire detector area (encompassing all pixels) within a specific time frame defined by the scanning algorithm. Achieving this goal entails each readout channel indicating the arrival of a BSE by generating a logical state '1' through the digitizer within the designated time frame. Subsequently, the number of BSEs per scanning step is determined by tallying the number of readout channels generating a logical state '1'.

In electron counting systems, a signal is attributed to an electron only if it exceeds a threshold set above the intrinsic system noise. However, while the threshold ensures full electronics noise rejection (when a sufficient threshold-to-noise ratio is secured), it may also result in a loss of detection efficiency (missed counts), with the loss increasing as the threshold level rises. Nevertheless, the system exhibits perfect linear behavior across its entire dynamic range, provided the counter capacity is sufficient and pulse pileup is avoided.

One of the significant challenges encountered by state-of-the-art readout ASICs is the precise registration of weak and high flux rate charge signals emitted by detectors. This challenge arises due to the need to detect a series of subtle electrons with an exceptionally low error rate and high time resolution, typically in the nanosecond range. Overcoming this hurdle requires implementing a high-bandwidth, low-noise readout channel with moderate power consumption to mitigate thermal heating and bias drift across the entire system [9]. The error rate is a crucial performance metric in charge signal detection, which can be compromised by either noise or inter-symbol interference (ISI). ISI, in this context, refers to the accumulation of signals at the output of a low-bandwidth stage [17]. The intricate interplay between noise and ISI (as illustrated in Fig. 3) necessitates an optimal bandwidth that strikes a balance in error rates between the two factors [18], [19].

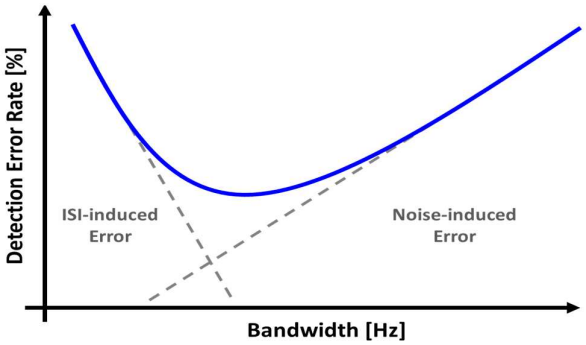

Fig. 3. Conceptual plot of the trade-off between bandwidth, noise, ISI, and the error rate.

Electron microscopy heavily relies on the efficiency and precision of its detector readout electronics, particularly the preamplifier, acting as a critical interface between semiconductor detectors and the interpretation of meaningful data. Among the operational modes of the preamplifier, the Transimpedance Amplifier (TIA) and Charge Sensitive Amplifier (CSA) emerge as prominent choices, each presenting unique advantages and challenges. When comparing TIA and CSA modes for electron microscopy applications, various factors require consideration, including signal characteristics, noise performance, complexity, power consumption, and calibration requirements. The optimal

selection between the two modes depends on the specific needs of the application, necessitating careful evaluation of factors such as dynamic range, sensitivity, and ease of implementation.

Depending on the time constant of the feedback network ($\tau_F = R_F.C_F$), the preamplifier can operate either in charge-sensitive mode ($\tau_F \gg t_p$) or transimpedance mode ($\tau_F \approx t_p$), where t_p represents the peaking time at the preamplifier output. In TIA mode, the preamplifier converts the input current from the semiconductor detectors into voltage signals with rapid transitions. This mode demonstrates high linearity across a wide range of input currents, facilitating accurate signal capture across varying intensities. However, TIA's linear response may result in a restricted dynamic range, while its reduced risk of saturation ensures signal fidelity even under high-intensity conditions. Operating in TIA mode typically entails a wider bandwidth compared to CSA mode, albeit at the expense of higher power consumption and noise levels. This can potentially impact signal quality, especially in low-intensity signal scenarios.

In CSA mode, the preamplifier converts the charge generated by the semiconductor detectors into voltage signals with exceptional sensitivity to charge variations, making it well-suited for precise detection of low-intensity signals. Compared to TIA, CSA configurations often consume less power and exhibit lower noise characteristics due to their relatively limited bandwidth, crucial for enhancing the overall SNR of the system. Additionally, CSA circuits often have more complex designs compared to TIA, requiring careful optimization and calibration to ensure optimal performance. Despite these challenges, CSA mode remains a valuable option for applications where sensitivity to low-intensity signals and efficient power consumption are critical considerations.

In electron counting architectures, preamplifiers are often operated in TIA mode due to their wider bandwidth and faster signal transition speeds, which are crucial for accurately detecting electron events [15]. Following the TIA stage, a discriminator and a counter are typically employed to digitize the detector signal and count the number of BSE, respectively. Conversely, in integrating systems, preamplifiers are commonly operated in CSA mode. In this mode, the preamplifier integrates the charge generated by the detector over a certain period, resulting in a voltage signal proportional to the total charge collected. Subsequently, this voltage signal is processed using either an *n*-bit Analog-to-Digital Converter (ADC) or *n* discriminator circuits. In the case of using discriminator circuits, they compare the charge-proportional voltage signal with a set of threshold levels. These threshold levels are typically generated as global voltage signals distributed to all readout channels. In some configurations, a local Digital-to-Analog Converter (DAC) may be incorporated to adjust or trim the threshold levels for each channel individually [14]. Threshold comparison using multiple discriminator circuits operating in parallel offers a fast digitization scheme. However, this approach can lead to increased power consumption and circuit area within the pixel due to the additional components required for each channel.

To ensure high accuracy in electron detection and signal digitization, the digitizing stage mustn't be triggered by noise or saturation due to offset. Therefore, a low-noise, low-offset, high-resolution discriminator/ADC is essential, which inevitably adds to the power consumption of the digitizing stage. Moreover, for high-flux rate BSEs, to avoid error in detecting the BSEs in the digitizing stage and/or saturation of the preamplifier, the signal after the preamplifier should be retrieved to the baseline through a resetting mechanism [20]. As a potential remedy, adding a gain stage between the preamplifier and discriminator/ADC can alleviate the design constraints of the digitizing stage. However, this solution comes with a trade-off – the additional power consumption of the gain stage and a reduction in SNR [21].

In addition to the previously mentioned architectures, hybrid readout architectures are proposed as a solution to detect low-energy and high-flux rate BSEs with lower power consumption while maintaining the same level of detection accuracy. These architectures involve designing the readout channel with a lower bandwidth than typically required to minimize noise and power consumption, while compensating for this reduction in performance and accuracy with additional circuit complexity [15], [22].

Here, we provide an overview of state-of-the-art hybrid readout architectures tailored for BSE detection, capable of handling a maximum flux rate of up to $400\ \mathrm{MElectrons/s}$. These readout channels are integrated with a segmented PIN detector, where each segment produces charge signals equivalent to $160\ \mathrm{aC}$ (or approximately 1000 electrons) for each impinging BSE. The readout channel is engineered to detect these charge signals with a time resolution of $2.5\ \mathrm{ns}$ at the moment of occurrence, with minimum power consumption [18], [23].

The readout channel architecture proposed in [18] and [24] adopts the double-threshold technique to meet the specified requirements for charge detection. In this approach, the preamplifier operates in TIA mode to generate rapid voltage signals in response to the input charge signals. The TIA is designed with a lower bandwidth than required to limit noise and power consumption. However, this design choice can lead to signal pileup after the TIA if electrons hit the detector segment in consecutive time frames [9]. To address this pileup issue, additional threshold levels (second comparator) are incorporated into the digitizer stage. This additional threshold level compensates for the induced signal pileup, thereby maintaining a lower detection error rate. It is noteworthy that two gain stages exist between the TIA and the digitizer stage to boost the signal level and reduce the digitization errors. Fig. 4 depicts the block diagram of the readout channel with the double-threshold technique architecture.

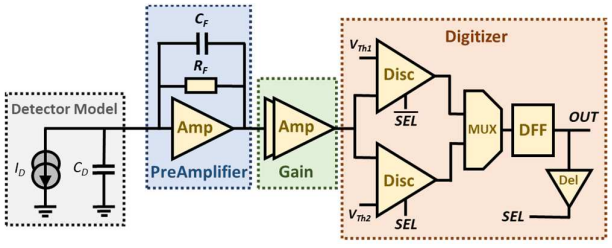

Fig. 4. Block diagram of the double-threshold technique.

At the end of the analog chain, two multiplexed dynamic comparators are employed (Fig. 4) to convert the analog signal into a digital signal and thus realize the double-threshold comparator. Switching between comparators, rather than between two thresholds, offers the advantage of

relaxing the settling time of the comparator and the switched references [25]. Moreover, to minimize power consumption overhead, only one comparator is active at a sampling moment. The comparators are enabled by a selection signal $SEL/\overline{SEL}$, which is a delayed version of the comparator output in the previous clock cycle.

The performance of the proposed architecture was experimentally quantified and presented in [24], revealing a total power consumption of 2.85 mW. For a model of BSEs landing on the detector surface with a Poissonian distribution in the time domain, this readout channel operates with an error rate of 13.56 % in single-threshold mode and 0.384 % in double-threshold mode. While these figures suggest the advantages of leveraging the second threshold level to enhance detection accuracy, this approach falls short of achieving the desired level of accuracy. Despite the TIA being designed with a lower bandwidth, it remained the noisiest and most power-hungry block, serving as the bottleneck of the readout frontend. With the additional gain boosting stages the TIA signal reaches an amplitude of $348\ mV$ with a maximum SNR of 5.6.

Furthermore, the combination of TIA with dynamic comparators introduces second-order effects on detection accuracy, primarily stemming from the stochastic behavior of electrons in the time domain. While the dynamic comparators are triggered by a synchronization master clock, the electrons hit the detector surface randomly with a Poissonian distribution in the time domain. This phenomenon may cause discrimination with a lower SNR, as the clock signal can trigger the dynamic comparators at any other point than the TIA's maximum amplitude point. Consequently, this leads to an increase in the number of lost events and a large detection error rate [19].

Two solutions are proposed to address this issue and enhance the performance of the double-threshold technique. The first involves synchronizing the comparator clock signal with the peak of the TIA voltage signal. However, this solution proves impractical as TIA voltage signals are generated randomly, following the stochastic nature of the input charge signals [24]. The alternative solution involves redesigning the preamplifier to keep the signal amplitude close to the maximum value over a few time frames. This adjustment enables the dynamic comparator to discriminate them with only a negligible drop in SNR during each clock cycle. To accomplish this, the preamplifier should operate in charge-sensitive mode, resulting in decreased integrated noise and power consumption. However, it's crucial to acknowledge that in this scenario, errors induced by ISI become more critical [19].

In hybrid architectures, the conversion of weak and fast charge signals from the detector into voltage signals is facilitated by the integration function of a preamplifier operating in CSA mode. Subsequently, the CSA generates staircase-like voltage signals characterized by fast-rising edges and prolonged falling edges. These characteristics are relative to the duration of the detector charge signal and the rate at which electrons are detected [26]. To minimize power consumption and circuit complexity, the objective is to utilize a single discriminator in the readout channel. However, to ensure accurate digitization of the signal, an intermediate filter stage is necessary between the CSA and the discriminator. This filter stage is tasked with shaping the voltage signal appropriately before it is digitized. By shaping the signal, the filter ensures that only the relevant information, corresponding to the high-frequency components of the signal, is passed on to the discriminator for digitization. This selective filtering helps to optimize the performance of the readout channel while minimizing power consumption and circuit complexity.

In [27] a solution is proposed of a CSA comprising a core amplifier followed by a current conveyor stage known as an ICON Cell in the feedback network, intended to implement a large feedback resistance. The design and experimental qualification of the CSA is presented in [19], [23]. Serving as a crucial component in the readout channel, the CSA converts the detector charge signal into an output voltage signal with a gain of $184\ \mu V/aC$, a SNR of 20.6, and consumes $140\ \mu w$ of power. Remarkably, the CSA can process 6 consecutive charge signals without saturation. The voltage signal after the CSA exhibits a fast-rising edge (< 2.6 ns) thanks to its high loop bandwidth [19] and a long falling tail (> 286 ns) due to its limited bandwidth. While the rising edge of the voltage signal after the CSA carries the desired information (high-frequency contributions), the falling tail and associated offset (low-frequency contributions) can introduce errors in electron detection, particularly at high flux rates. To address this issue, a signal-shaping filter can be introduced between the CSA and the discriminator to selectively pass the useful part of the CSA signal (high-frequency contributions) and suppress the remainder. Achieving the anticipated performance requires implementing a transfer function for the band-pass filter in the frequency domain [28], [29]. Additionally, this transfer function should provide attenuation over the drift of the DC level (offset) at the CSA output to enhance discrimination and, consequently, electron detection accuracy.

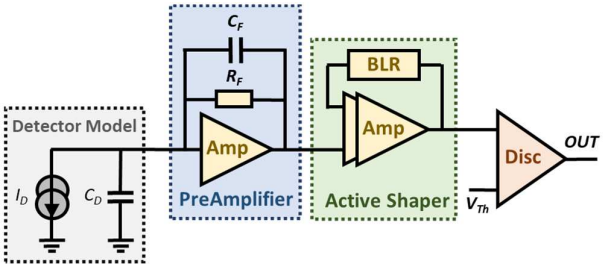

Fig. 5. Block diagram of the readout channel with active shaper.

One potential implementation of the signal shaping filter, known as the *active shaper*, is detailed in [28]. This filter (Fig. 5) operates in closed-loop mode, incorporating a baseline restorer (BLR) loop designed to eliminate the low-frequency contributions of the input signal. The active shaper comprises amplifiers in the forward path and a low-pass network in the feedback branch to achieve the BLR function. The fundamental concept behind the BLR is to monitor the low-frequency contributions of the signal post-amplification in the forward path and subsequently subtract them from the input signal of the signal shaper block [19]. By employing a negative feedback loop, the system continually monitors the voltage at the shaper output node and endeavors to adjust it to an externally applied reference DC level, denoted as V_{ref}. Verified through experimental qualification tests, the active shaper has a SNR of 13.9 and consumes 170 µW of power. It amplifies the high-frequency contributions of the signal after the CSA by a factor of 7 while attenuating its low-frequency contributions (including the offset) by a factor of

24.6 dB, to fit the signal within timeframes of 2.5 ns. The comparator is designed to digitize the signal of the active shaper is presented in [30].

Experimental characterization and qualification of a hybrid readout channel including the CSA, the active shaping filter, and a discriminator, using the test setup presented in Section IV, is reported in [22]. For a model of BSEs landing on the detector surface with a Poissonian distribution in the time domain, this readout channel operates with an error rate of 1.47 ppm (parts per million). The ROIC operates with a total power consumption of 0.37 mW.

This architecture meets the specifications outlined earlier in this section; however, there is always a keen interest in further optimizing the building blocks to achieve better performance. Targeting lower power consumption and reduced circuit complexity, reconfigurations of the CSA, the shaping filter, and the discriminator can be explored. As the CSA is the most critical block in the readout channel, achieving further reduction in its power consumption without compromising electron detection accuracy is challenging, especially considering it is already designed with a lower bandwidth than required to limit noise. Therefore, the focus shifts to optimizing the shaping filter and the discriminator block.

Regarding the performance and expected transfer function of the shaping filter, comparable results can be achieved by implementing the circuit with passive components. In this approach, the active shaper is replaced with a passive high-pass RC filter characterized by negligible power consumption [31]. The negative side of this alternative high-pass RC network is that it loads the CSA output node with a larger capacitor and attenuates the CSA signal amplitude based on the time constant of the RC network. Consequently, the discriminator needs to be upgraded to a more advanced one with lower input-referred noise and offset, as it will operate with input signals with significantly lower amplitudes than those generated by the active shaper. The main challenges with this approach are: the stability of the CSA with an additional capacitive load; the design of a low-noise, low-power, low-offset, fast discriminator.

The readout channel (Fig. 6), comprising the CSA, the passive RC shaping filter, and the low-offset discriminator, is detailed in [31] and validated through post-layout simulations. While leveraging the passive RC shaping filter significantly reduces power consumption in the readout channel, the upgrade of the discriminator results in increased power consumption. The upgraded discriminator utilizes the autozeroing technique for offset attenuation, which is periodically repeated every 90 µs with a duration of 10 ns. The posterior is considered the deadtime of the readout channel, during which it is blind to input charge signals.

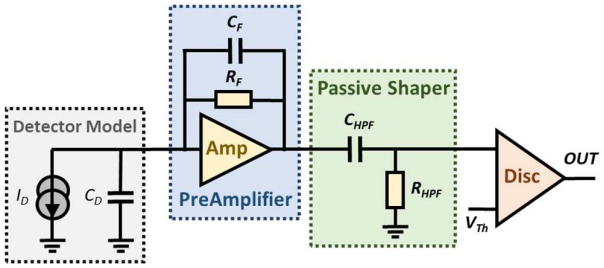

Fig. 6. Block diagram of the readout channel with passive high-pass RC filter.

Post-layout simulation results indicate that this readout channel can detect charge signals with an average detection error rate of 9.3 ppm while consuming 250 µW of power. These figures reveal that the readout channel with the passive RC shaping filter consumes 32 % less power while achieving 25.8 times larger detection error rate compared to the one with the active shaper. Although the overall SNR after the passive RC filter is 15.3 (11 % larger than with the active shaper), the lower accuracy is attributed to the periodic deadtime imposed by the autozeroing technique for offset attenuation in the discriminator block, as well as the signal undershoot issue after the RC network [31]. Nonetheless, in some SEM applications, the scanning principle includes periodic intermediate breaks which can be used for an offset reduction phase. In this particular case, a lower detection error rate, comparable to that of the active-shaper solution, could be obtained.

IV. Test Setup for Experimental Qualification

The core part of the testbench is a chip featuring a matrix of readout channels bonded to the test PCB. Precise evaluation and characterization of the readout channels necessitate a meticulous laboratory setup equipped with specialized instrumentation. The measurement setup includes a voltage supply for powering the test PCB and an oscilloscope for real-time signal monitoring. To maintain signal integrity and minimize noise, the test setup incorporates isolation buffers both on the PCB and within the chip, effectively mitigating peripheral noise injection and preventing loading effects [24]. Additionally, all cables and signal transmission lines are carefully isolated to further minimize noise interference. On the test PCB, multiple power regulation units are strategically positioned to generate various isolated voltage rails required for biasing the chip [22].

A pivotal component of the test setup is the FPGA-based Data Acquisition Board (DAB), essential for programming the chip and evaluating its performance. The DAB facilitates seamless communication with the ROIC through a high-speed low-voltage differential signal (LVDS) interface, ensuring reliable operation free from noise interference [32]. Fig. 7 provides a visual representation of the test setup PCB.

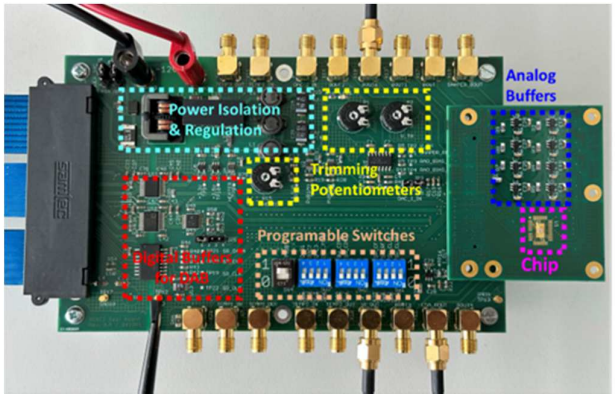

Fig. 7. Test PCB designed for experimental qualification of the chip.

To enhance the testability of the readout channels, additional auxiliary and peripheral blocks are integrated into the chip, as depicted in Fig. 8. These include a detector emulator designed to generate input charge pulses [24], wide-bandwidth voltage buffers aimed at mitigating signal

loading effects during signal monitoring, a power regulator stage for biasing, and a programmable shift register coupled with a set of configuration switches to adapt the operating modes of the readout channels. Control signals from the DAB govern all these auxiliary and peripheral blocks. Further details regarding the implementation and programming of these on-chip auxiliary and peripheral blocks can be found in [22].

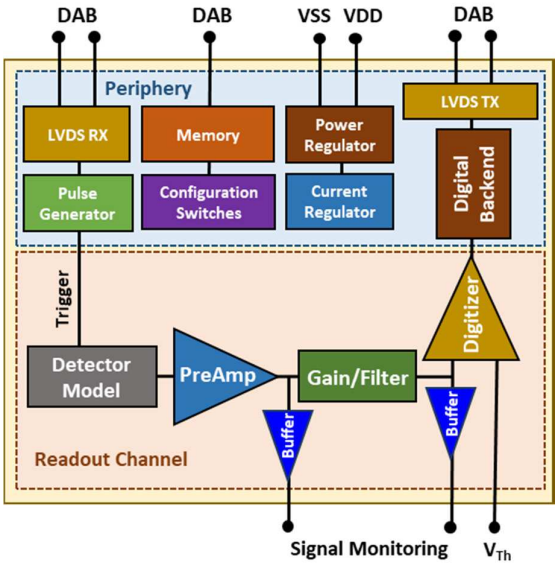

Fig. 8. The on-chip auxiliary and peripheral blocks facilitate the testability of the readout channels.

To assess the operational accuracy of the architectures presented in the previous section, their readout channels are fired by a set of trigger pulses generated by the DAB. To identify and validate the precise moment of triggering the readout channels and consequently, the signal detection, a reference clock generator with tunable frequency is implemented on the DAB. This reference clock frequency sets the timeframes outlining the duration of every scanning step. Each trigger pulse meticulously indicates the status of the detector within that specific time frame, with a logic state of '1' denoting the presence of a particle landing on the detector surface.

During the experimental qualification, the DAB generates the trigger pulses based on digital codes stored in a register labeled the *trigger* register. Concurrently, the DAB collects the digital data generated by the readout channel, assigning them to a register designated as the *data* register. By comparing the logical states in both the trigger and data registers, the detection error rate and operational accuracy of the designed readout channel are evaluated. To ensure consistency and precision in data acquisition, 100 firing cycles are executed, with the outcomes subsequently averaged for thorough analysis. It is notable that, before embarking on the experimental assessment of the detection error rate and operational accuracy, the optimal threshold levels for the discriminators are identified through comparative analysis. Additionally, further assessments are carried out to evaluate the ability of the readout channels to capture consecutive events accurately and mitigate counts attributed to noise [22], [24], [31].

In this series of experimental qualification tests, we focus on assessing the count rate capability of the readout ASICs discussed in the preceding section. The maximum count rates signify the input flux levels at which the output count rate saturates. Once this threshold is exceeded, the count rate cannot be linearized, leading to ambiguous and inconsistent datasets. To evaluate the maximum count rate capability empirically, we configure the trigger register to all logic states of '1', while varying the triggering time frame (trigger frequency) from $1\,\mu s$ ($1\,MHz$) to $1\,ns$ ($1\,GHz$). Fig. 9 illustrates the count rate performance of the readout channels described earlier. The maximum count rate values are indicated in Million counts per second per pixel ($Mcps/pixel$) and Million counts per second per millimeter square ($Mcps/mm^2$). The results highlight that all readout channels exhibit satisfactory performance for input flux rates up to $150\,Mcps$. However, for higher input flux rates, the readout channel featuring the CSA and the active shaper demonstrates a superior output count rate. Table I provides a summary of the performance of the readout channels described earlier.

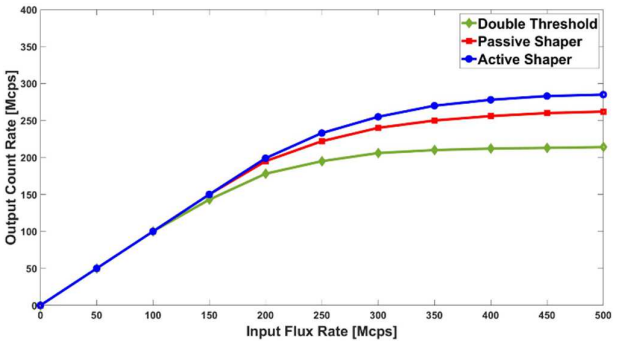

Fig. 9. Count rate performance of the readout channels including: TIA with double threshold discriminator (in green), CSA with passive shaper (in red), and CSA with active shaper (in blue).

TABLE I. PERFORMANCE SUMMARY OF THE PRESENTED READOUT CHANNELS

Readout Channel	Double Threshold	Active Shaper	Passive Shaper
SNR	5.6	13.9	15.3
Power [mW]	2.85	0.37	0.25
Error Rate [ppm]	384	1.47	9.3
Max. Count Rate [Mcps]	214	285	262

It is worth noting that the maximum count rates are strongly influenced by various measurement conditions, such as the energy of the BSE, which determines the amplitude of the detector charge signal and the signals within the readout channel. Additionally, the threshold level of the discriminator plays a significant role in determining the duration of the pulses fed into the counter, thereby affecting the count rate [33]. Moreover, the time constant of the preamplifier and the voltage headroom at its output node are crucial parameters for determining the count rate capability of the readout channel. Every preamplifier, whether operating in TIA or CSA mode, can withstand a certain flux

rate of input charge signals before saturation occurs. Fig. 9 provides a visual representation of the input flux rate limit at which the output count rate enters a plateau region, indicating saturation of the preamplifier stage. To mitigate preamplifier saturation, a reset switch in the feedback network can be activated to discharge the integrating capacitor within the preamplifier. However, this comes with a trade-off in the form of dead time, during which the readout channel is blind to input charge signals. Consequently, the output count rate is also influenced by the resetting period and the associated mechanism.

There are several methods to activate the reset switch in the readout channel. One possible approach involves comparing the signal after the preamplifier with an auxiliary threshold level set close to the saturation limit of the preamplifier output node. When a few BSEs hit the detector consecutively within a short period, the signal after the preamplifier surpasses the auxiliary threshold level, activating the reset switch. Although this method enhances the accuracy of BSE detection, it comes at the cost of additional power consumption and a larger silicon area to implement the auxiliary threshold level. Furthermore, the reset switch is triggered based on the rate of BSEs hitting the detector surface rather than their pattern over time frames. Another approach is to activate the reset switch periodically, irrespective of the pattern of input charge signals. While this method ensures the operation of the preamplifier without saturation for high flux rate BSEs, it periodically renders the readout channel blind to BSEs during the resetting process, potentially leading to a higher detection error rate. A third approach involves activating the reset switch according to the pattern of BSEs landing on the detector surface. By statistically calculating the expected number of BSEs impinging on each detector pixel over consecutive time frames, a logic circuit can be implemented in each readout channel to scan the discriminator output and activate the reset switch accordingly. This method incurs negligible additional power consumption and carries a lower risk of missing BSEs, as it can be optimally tuned based on the pattern of BSEs and the flux rate.

To experimentally assess the impact of different resetting approaches on count rate performance, the DAB triggers the readout channel using a specific code. This code comprises 10^8 Poissonian-distributed logic states of '1', anticipating a maximum of 3 electrons within 4 consecutive time frames of 2.5 ns , equivalent to a maximum flux rate of 400 MElectrons/s. The readout channel under investigation incorporates the CSA, active shaper, and a single discriminator, as this particular configuration has demonstrated superior output count rate performance. Two resetting strategies are implemented for comparison: periodic resetting and pattern-oriented resetting. In the case of periodic resetting, the reset switch is activated every 25 ns, occurring once every 10 time frames. Conversely, for pattern-oriented resetting, the reset switch is activated after every 3 triggers in 3 consecutive time frames. Fig. 10 presents the measured output count rate performance of the readout channel for above mentioned resetting approaches. As depicted, pattern-oriented resetting yields the most favorable outcome in terms of detection accuracy, effectively preventing CSA saturation.

For the above-mentioned resetting approaches and the readout channel featuring the CSA, active shaper, and a single discriminator, Fig. 11 presents the 3-sigma error rate (calculated through $\mathrm{Error}_{3\sigma} = \mu_{\mathrm{error}} + 3 \times \sigma_{\mathrm{error}}$) as a function of threshold level. This visualization provides insight into the influence of resetting methods and threshold levels on readout channel performance and detection error rate. As expected, pattern-oriented resetting demonstrates superior performance, effectively preventing preamplifier saturation under high input flux rates.

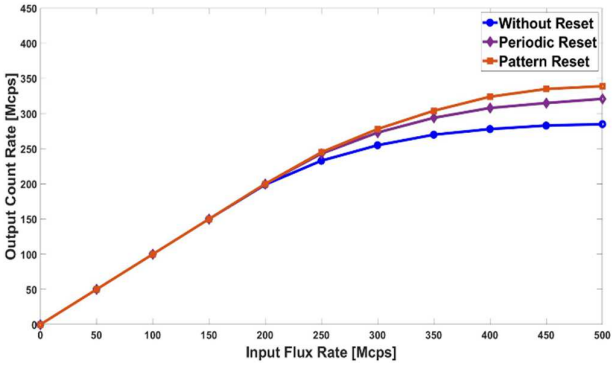

Fig. 10. Count rate performance of the readout channel incorporating the CSA, the active shaper, and one discriminator with the periodical resetting and pattern-oriented resetting.

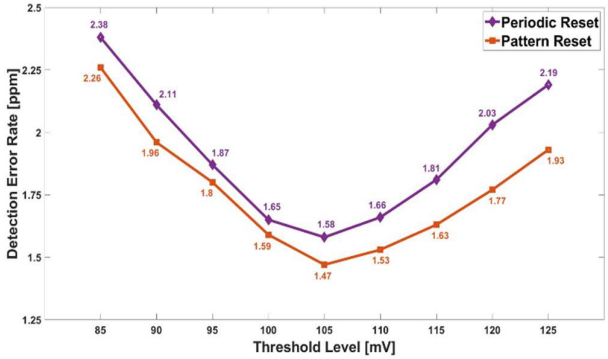

Fig. 11. The 3-sigma error rate as a function of the threshold level for periodical resetting and pattern-oriented resetting

V. Summary and Conclusions

A study of both integrating and electron counting systems is presented, elucidating the architecture, operational principles, and performance characteristics crucial for efficient signal processing in BSE detection. The investigation of the count rate capability of the readout ASICs under varying conditions, including discriminator threshold levels and preamplifier characteristics, provides insights into the operational limits and optimization strategies for enhancing detection accuracy and performance efficiency.

The detailed description of experimental qualification methodologies, encompassing meticulous test setups, trigger mechanisms, and count rate capability assessments, ensures an accurate and reliable evaluation of ASIC performance. The incorporation of specialized instrumentation, such as the Data Acquisition Board (DAB), in the laboratory setup facilitates precise performance evaluation and validation of proposed architectures. Furthermore, the study proposes effective strategies to prevent preamplifier saturation and mitigate challenges associated with high-flux rate BSE detection. Experimental results demonstrate the effectiveness

of the proposed architectures and assessment methodologies in achieving high detection accuracy and performance efficiency in electron microscopy applications.

This paper contributes to advancing the understanding of readout ASICs for BSE detection, offering valuable insights into their design, operation, and performance evaluation, thereby paving the way for enhanced signal processing capabilities and improved detection accuracy in electron microscopy.

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