# High Efficiency
## RF Power Amplifier Architectures

PROEFSCHRIFT

ter verkrijging van de graad van doctor
aan de Technische Universiteit Delft,
op gezag van de Rector Magnificus Prof. ir. K.C.A.M. Luyben,
voorzitter van het College voor Promoties,
in het openbaar te verdedigen op dinsdag 3 juli 2012 om 10.00 uur
door

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ISBN 978-94-6203-071-8

*To my parents*

# Contents

Chapter 1

# Introduction

Although by now wireless communication has a long history, first demonstrated by Nikole Tesla in 1897, it was only until the early 1970s that wireless communication was mainly used for broadcast radio, military or space applications. In 1973 Bell Laboratories presented the idea of cellular networks [1][2](Figure 1.1), which promoted the use of wireless technologies for voice communication among the masses. The most important benefit of their proposal was the efficient reuse of the frequency spectrum by spatial separation of the broadcasting base stations. Namely, the total region covered by the wireless network can be divided into hexagonal cells, each having its own base-stations. In such a cell each base-station is assigned to a number of frequency channels. The same frequency channels are assigned to other base-stations operating in the same region but located in a different cell. The location of these cells is chosen such, that their cross interference is kept at the minimum, by assigning different frequency channels to the neighboring cells. In this way reuse of the frequency spectrum becomes possible, enabling services to a large number of users within a limited frequency band [2].

## 1.1 Mobile Base-Stations

The heart of modern cellular networks is the mobile base-station which is typically situated in the middle of each cell (Figure 1.2) where it handles all the calls made from, to, or in that cell. The current third generation mobile networks (3G), does not only provide voice services, but also high-speed data services like internet, MMS (multi-media messaging service) and video conferencing [3][4][5]. The provision of these high-end services not only requires very sophisticated digital signal processing hardware, but also low noise and highly linear transceivers.
These days there are a large number of mobile service providers, therefore there is continuous competition to reduce cost and increase profit margins. In view of

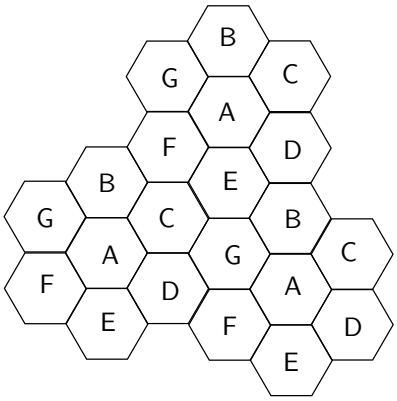


**Figure 1.1:** *Illustration of the cellular frequency reuse network. Cells with same letter use the same set of frequencies*

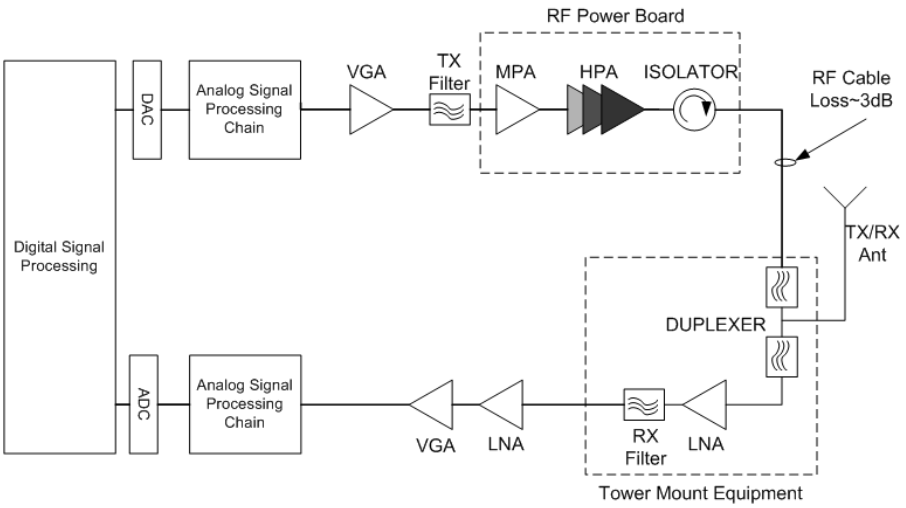


**Figure 1.2:** *Block diagram of a typical high power base-station*

this, in addition to the initial installation costs of a base-station, also the operating costs of the base-station become very important for cellular service providers. Currently, the overall efficiency of a base-station, which relates to the conversion of DC power to the RF power, lies between only 2.5 to 3.0%. A significant portion of this efficiency number is set by the performance of the RF power amplifier(s). However, not only the efficiency of the power amplifier itself is of importance, but also secondary energy expenses needed for the cooling of these amplifiers. Therefore, improved amplifier efficiency yielding reduced cooling requirements, is currently driving the developments in base-station transmitters.
The block diagram of a typical RF front-end of base-station is shown in Figure 1.2, the high power RF power amplifier (HPA) is the last component in the transmitter chain and consumes typically more than 30% of total power of the transmitter chain due to its limited DC to RF conversion efficiency. Moreover, a considerable amount of RF power is lost in the RF cables connecting the RF power amplifier to the antenna, as the RF power amplifier module can not be placed close the antenna for logistic reasons. Additionally if the base-station module has to support more than one standard using different frequencies, currently a separate RF PA will be required as efficient multi-band RF PAs are currently not available. This results not only in an even lower efficiency for the base-station, but also increases its form factor. Therefore currently, base-station manufacturers are now not only focusing on improving the efficiency, but also extending the bandwidth of the broadcast amplifiers.

## 1.2 RF Power Amplifier Efficiency

The efficiency of an RF power amplifier determines how efficiently it converts DC power to broadcast RF output power. There are a number of definitions for the efficiency of RF amplifiers, namely; drain efficiency, power added efficiency (PAE), average efficiency and average power added efficiency. The drain efficiency is given simply by the ratio of the output power to the provided DC power. (1.1). Note that (1.1) gives a generalized definition of the efficiency of the RF PA, which for a given operating class e.g. class-B [6] can be expressed as function of the ratio output RF voltage vs. DC supply voltage (1.2)

$$\eta_{CW} = \frac{P_{RF}}{P_{DC}} \tag{1.1}$$

$$\eta_{CW(AB)} = \frac{\pi}{4}\frac{V_{RF}}{V_{DC}}. \tag{1.2}$$

The drain efficiency does not accurately reflect the actual efficiency, since a part of input power is also fed into the PA as the RF input power. Therefore there is another, also commonly used definition, known as power added efficiency

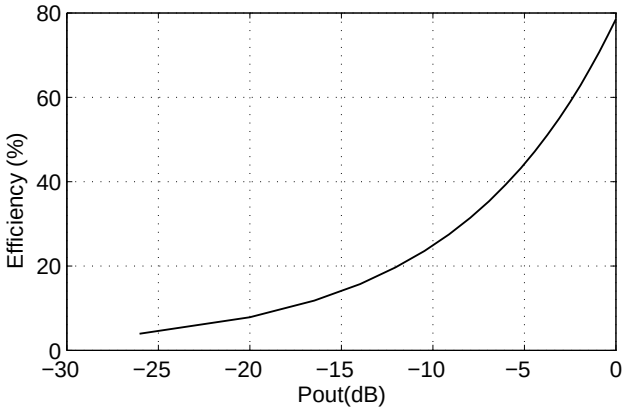


**Figure 1.3:** *Efficiency of a class-B Rf amplifier*

(PAE), which is given by (1.3). The PAE definition takes into account the limited gain of the RF PA along-with its DC to RF efficiency

$$\eta_{CW(PAE)} = \frac{P_{RFout}}{P_{RFin} + P_{DC}}. \tag{1.3}$$

The above to mentioned efficiencies are known as CW (continuous wave) efficiencies, as these correspond to the CW characteristics of the power amplifier. Moreover, the CW efficiency of the RF PA is a strong function of the output RF power as shown in the Fig.1.3 for an ideal class-B amplifier.

The RF PAs used in the mobile base-stations are usually operated with modulated signals that have very high peak-to-average ratios. For the RF PA this means that most of the time it operates at the power levels, which are far less than the peak power levels. The achieved efficiency with these modulated signals is known as the average efficiency, which is given by the ratio of the average output power to the average DC input power. The analytic expression of the average efficiency is quite complex as it not only depends on the efficiency versus power characteristics of the RF PA, but also on the characteristics of the signal to be amplified. An expression based on the probability density function of the modulated signal [7][8] is given by (1.4)

$$\eta_{\text{avg}} = \frac{\int_{V_{\text{n}}=0}^{V_{\text{n}}=1} P_{\text{out}}(V_{\text{n}})\rho(V_n)\mathrm{d}V_{\text{n}}}{\int_{V_{\text{n}}=0}^{V_{\text{n}}=1} \frac{P_{\text{out}}(V_{\text{n}})}{\eta(V_{\text{n}})}\mathrm{d}V_n}. \tag{1.4}$$

Whereas $\rho$ is the probability density function of the signal to be amplified, while $P_{out}$ and $\eta_{CW}$ are the output power and CW efficiency characteristics of

the RF power amplifier. These days the base-station industry is more concerned about the average efficiency of the power amplifier rather than the CW efficiency because this defines their actual DC to RF efficiency. The average efficiency of a simple RF PA, for example class-B, (for signals with a high peak-to-average ratios) is a few times lower than the peak efficiency of this amplifier. For example, current high power LDMOS class-B PAs have a maximum efficiency between 60% to 65%, however, their actual average efficiency for WCDMA signals lies between 20% to 25%. Currently, base-station manufactures are aiming for an average efficiency of $\geq 50\%$ for W-CDMA signals. Since these high average efficiency specs needs to be combined with high requirements on linearity, the design of the RF PA becomes much more complex. These facts led to an intensive research in industry towards efficiency as well as linear PAs.

## 1.3 Efficiency Enhancement Techniques

The average efficiency of the PA can be improved by altering the CW efficiency curve of the PA at the back-off power levels, by using techniques like doherty [9], outphasing [10], dynamic load line, envelope tracking and EER (envelope elimination and restoration). All these techniques increase their efficiency at the back-off power levels by improving the ratio $\frac{V_{RF}}{V_{DC}}$. This can be done either by increasing the RF voltage swing ($V_{RF}$) (doherty, outphasing, dynamic load line amplifier configurations) or by decreasing the DC supply voltage $V_{DC}$ (envelop tracking, envelop elimination and restoration) [11] for the lower power levels. The following section presents an overview of the different techniques and provides the merits and demerits associated with each of them. In these considerations, we will assume class-B operation for the RF amplifier(s).

### 1.3.1 Doherty Power Amplifiers

Doherty power amplification (DPA) [9] is a technique dating back to 1930s and named after its inventor William H. Doherty. He proposed this technique to improve the efficiency of vacuum tube RF power amplifiers used in AM broadcast applications.

This technique has become recently very popular for the base-stations nodes in the wireless networks with the introduction of 2G and 3G mobile networks that rely on complex modulated signals with very high peak-to-average ratios (PAR). The block diagram of a DPA in its most simple form is shown in the Figure 1.4, which contains two PA branches, the top PA is called main or carrier amplifier which operates at all power level, whereas the bottom PA operates only at the peak power levels and therefore is known as the peaking amplifier. The operation of the DPA depends on the active load modulation effect of the peaking amplifier on the main amplifier. This allows for using higher load impedances of the main

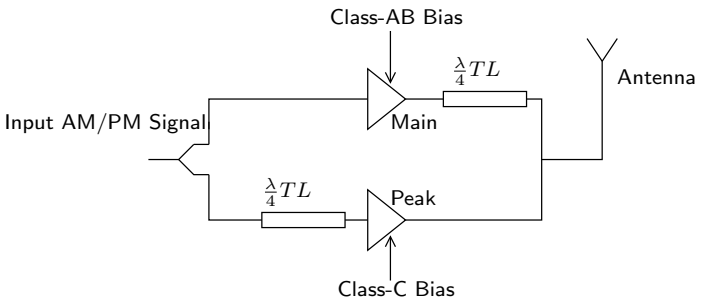


**Figure 1.4:** *Conceptual block diagram of a two-way doherty power amplifier*

amplifier at the back-off power levels, eventually resulting in higher efficiency at those power levels.
The DPA technique is quite popular due to its simplicity, high-efficiency in power back-off and large modulation bandwidth, which makes it a very attractive choice for base-station applications and is currently widely applied in the modern high efficiency base-station transmitters.
However, this increased performance of the DPA comes at the cost of linearity and operational RF bandwidth. The class-C bias of the peaking device exhibits significant amounts of AM-PM distortion, which compromises the linearity of the DPA. Moreover, the complex output power combiner network limits the RF bandwidth of the DPA, which not only hinders its use in multi-band transmitters, but also causes pre-distortion algorithms to fail by introducing memory effects [12][13]. In view of above, DPA applications are limited to RF narrowband operation and are always accompanied by pre-distorters. The current advancement in the DSP technology allows digital pre-distortion hardware to be directly embedded in the transmitter. Therefore research in DPA technology, is currently more focused on achieving higher RF bandwidths [14][15] and increasing the efficiency in power back-off rather than on improving linearity. Earlier DPA work [12] was already focused on improving the efficiency in power-back off. Therefore in this thesis we focus on new DPA topologies (Chapter 5) that can guarantee a 3 to 4 times improvement in the high efficiency bandwidth of the DPA.

### 1.3.2 Outphasing Power Amplifiers

The origin of the outphasing power amplifiers [10][16] also dates back to 1935, but this technique was initially presented to improve the linearity of the RF transmitters rather than their efficiency. The main idea behind this technique is to convert the amplitude modulation (AM) of the input signal to phase-modulation (PM) so that the AM-PM distortions of the PA devices do not affect the linearity of the output signal (see Figure 1.5). This approach has as additional advantage

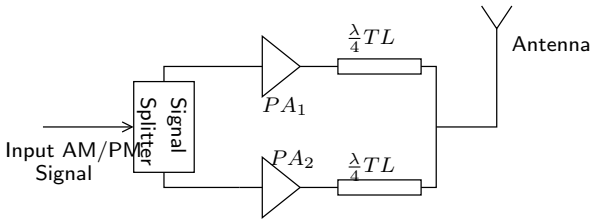


**Figure 1.5:** *Conceptual block diagram of an outphasing PA*

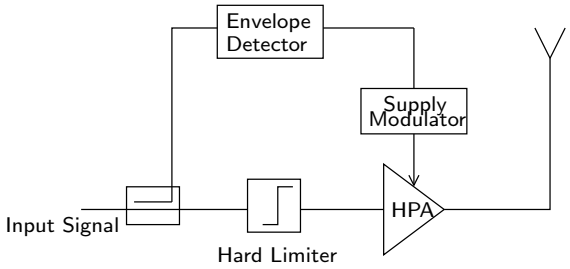


**Figure 1.6:** *Envelope elimination and restoration technique (EER)*

that the PA devices can now always be used in the region where they operate highly efficient, yielding a better average efficiency of the system.
Although the idea behind this technique is quite brilliant as it can guarantee efficiency along-with linearity, practical implementations of this technique are very complex and prone to the non-ideality of the PA devices (details in Chapter 2). Additionally due to the AM-PM conversion in the input power splitter the video bandwidth of the conventional outphasing amplifier is not very high, while its RF bandwidth is limited but slightly better than a conventional Doherty power amplifier.
Due to the above mentioned problems, the outphasing technique has been neglected for some time with almost no application in base-station units. This thesis tries to change that situation, by introducing a new operation class of outphasing amplifier namely mixed-mode outphasing amplifier [16][17] which addresses most of the problems associated with conventional outphasing amplifier implementations. Moreover, the combination of outphasing with class-E amplifiers can provide some additional benefits in the form of efficiency as well as RF bandwidth [18].

### 1.3.3 Supply Modulation

In this efficiency enhancement technique, the DC voltage at the drain is varied with the envelope of the output signal. This improves the ratio of the RF voltage

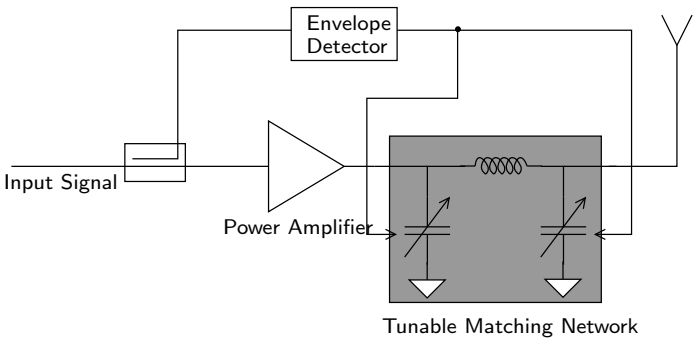


**Figure 1.7:** *Conceptual block diagram of a dynamic load line rf power amplifier*

swing with respect to the DC voltage at the power back-off levels, eventually improving the CW efficiency of the PA at those power levels (Figure 1.6). Currently there are two popular variants of this technique, envelope tracking (ET) [19][20] and envelope elimination and restoration (EER) [11][21]. Conceptually these two techniques are similar, the difference lies in the inclusion of a hard limiter in EER, eliminating the envelop modulation present in the input signal, which is later restored by the supply voltage modulation at the drain /collector of the RF power amplifier. This technique poses problems in dynamic range and linearity [11]. On the other hand the input envelop signal in the ET technique, is not separated, and only the supply voltage of the RF PA is varied with the input signal.
In general, supply modulation techniques are not only capable of providing very high average efficiency [11] but also capable of providing very wide RF bandwidths [21]. Modern base-station transmitters currently employ very wideband complex modulated signals, consequently, the amplification of those signals requires PAs with a large ($\geq$100MHz) video /modulation bandwidth as well as wide RF bandwidth. Although, the EER/ET basestation PA topologies are capable of providing a very wide RF bandwidth, their video bandwidth is limited by the bandwidth of supply voltage modulator. Moreover, the output capacitance of practical PA devices changes drastically with the varying drain supply voltage, which means the output matching network of the PA, can be tuned for maximum performance only at one specific drain voltage and therefore will operate less optimal at other drain voltages unless a smart compromise if found [22]. Due to these problems and their complexity and efficiency overhead imposed by the voltage modulator, these PA's are currently not as popular in the base-station industry as the Doherty PAs.

### 1.3.4 Dynamic Load-Line

The Dynamic Load-Line technique [6][23][24] also relies on load modulation to increase the RF voltage swing at the terminals of the active device at power

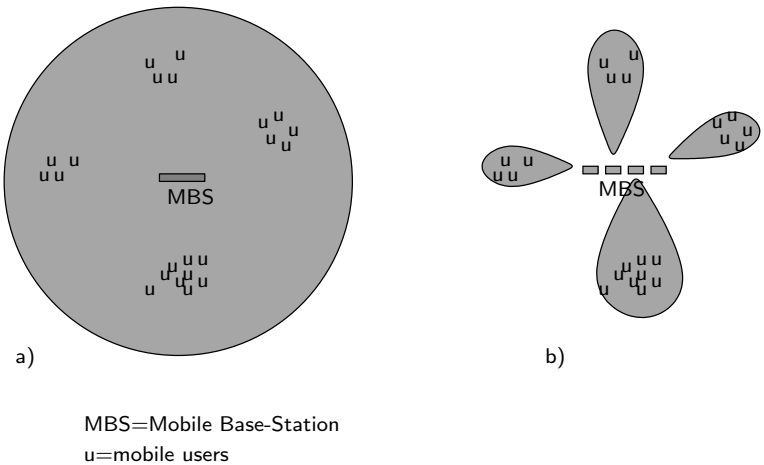


**Figure 1.8:** *Comparison of the omni-directional pattern of a conventional base-station with the pencil beam approach of a future base station unit with improved air link budget utilizing a multi-beam smart antenna*

back-off (see Fig.1.7). But unlike the Doherty and outphasing techniques, it uses passive load modulation, i.e. the properties of the output matching network are varied with the envelop signal by using tunable circuit elements like varactors. This is also a nice technique for improving the efficiency, but the performance of the PA will be constrained by the losses and breakdown properties of the tunable elements used in the adaptive matching network. Therefore due to the limited breakdown properties of currently available varactors, the application of this technique (up till now) is mostly limited to low-power handheld PAs only. However, this situation might change when high-voltage devices become available. Similarly as for the EER and ET approach, also here there are some concerns for the maximum achievable video bandwidth, since the generation of the high control voltages that are typically needed for adaptive matching network is normally also constrained in bandwidth.

## 1.4 Smart Antennas for Base-Stations

So far we have discussed the stand-alone efficiency of power amplifiers in base station units. However, there is also another aspect of RF signal transmission between the base station and mobile handset that needs attention. Current base-stations use omni-directional antennas, which means that they transmit the same power in all directions irrespective of the location of the users, which in itself is very inefficient. It has been proposed recently [25][26][27], to use smart antennas, in order to direct the transmission beam of the antenna to the direction where the

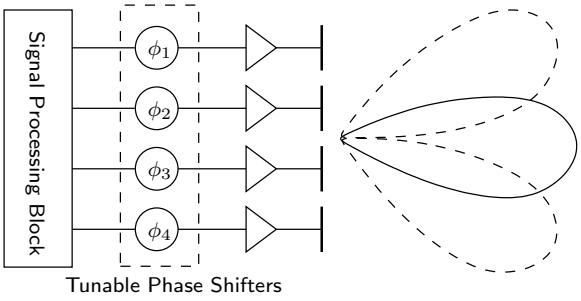


**Figure 1.9:** *Block Diagram of a Phase-Array Antenna*

actual mobile user is located (Fig.1.8). When more users are present, multiple pencil beams can be utilized with the appropriate information. This approach utilizes the antenna gain to improve the link budget, something that in theory allows a strong reduction of the total broadcast power. As such the energy consumption of the full transmitter can be drastically reduced.
These concepts, which are still in research phase, require major changes not only at the software and system level, but also in the mobile transmitters and antennas. One of those changes in the transmitter, is the use of phase-array antennas [28][29], which are typically fed by many small Power Amplifiers. In these antennas arrays, the phase of the output transmit signals is controlled in order to electronically steer the beam of the antenna. To keep the computational overhead limited, these phase changes are typically implemented through the use of analogue phase shifters (Figure 1.9). Note that the location of these phase-shifters in the transmitter imposes very stringent requirements in terms of phase and amplitude linearity, bandwidth, loss and chip area. Therefore, special attention is required in the design of these phase-shifters, and for this purpose one chapter (Chapter 7) is this thesis is totally devoted to the design and of low loss high linearity phase-shifters. Within that chapter some systematic methods for the implementation of these phase-shifters are presented that can yield very loss low as well as linear phase shifters [30].

## 1.5 Thesis Outline

The outline of the thesis is summarized as follows.
Chapter 2, Chapter 3 and Chapter 4 are devoted to the outphasing amplifiers. In which Chapter 2 presents the basic concept of outphasing amplifiers alongwith a complete analysis for modulated signals both for ideal and non-ideal PA devices. The purpose of this chapter is to present the reader with a deep understanding of the outphasing principal, its advantages and its limitations, so that the ideas presented in the later chapters can be well understood.

Chapter 3 extends the outphasing concept by introducing a class-B mode of operation at deep power back-off levels in order to improve their efficiency. The ideas presented in this chapter are followed by experimental verification through designing a prototype of a mixed-mode outphasing amplifier, which is presented at the end of the Chapter 3.
Chapter 4 further extends the outphasing concept by introducing tunable matching networks at the output of the PA devices. By using these networks, the efficiency at deep power back-off conditions can be further improved. A prototype of this adaptive outphasing technique is presented at the end of this chapter.
Chapter 5 is devoted to the RF operating bandwidth of the Doherty power amplifier. After a brief introduction to the Doherty amplifier, this chapter analyses the bandwidth limitations of the Doherty amplifier using the conventional power combiner at the output. After identifying the root cause of the bandwidth limitations of the Doherty amplifier, a Doherty power amplifier with an optimized bandwidth is presented. Next, some techniques are presented which can improve the inherent bandwidth of the DPA by using advanced wide-band power combiners at the output. This technique is also verified through a prototype wide-band DPA which is also presented at the end of this chapter.
The outphasing amplifiers presented in chapters 2 to 4 are optimized for efficiency performance which results in poor linearity performance for such amplifier. Chapter 6 discusses techniques for the digital pre-distortion of the multi-path power amplifiers. The techniques introduced, can in general be applied to all multi-path power amplifiers e.g. digital doherties and mixed-mode outphasing amplifiers. But in this chapter the application of this technique to mixed-mode outphasing amplifiers is presented as show case.
As discussed previously, the efficiency of transmission can be improved either by improving the DC-RF conversion efficiency of rf power amplifier design or improving the antenna efficiency by using smart antenna. Phase-shifter is an integral component in a smart antenna, chapter 7 presents techniques to design very low-loss and very linear phase-shifters which can be used in the implementation of smart antenna systems with improved link budget. The content of this chapter is also supported by some experimental results.
Finally Chapter 8 presents the main conclusions and recommendations for future works.

Chapter 2

# Outphasing Amplifiers

## 2.1 Basic Principle

Outphasing as amplifier enhancement technique (dating back to 1935's [10]) was originally proposed to improve the linearity of microwave transmitters. The main idea behind this technique is to present the PA devices with constant envelop signals such that, their AM-AM and AM-PM distortion properties do not affect the linearity of the output signal [6][31]. This has a positive side effect that the PA devices in this configuration can realize high efficiency operation [6]. In this way, in theory, the outphasing concept enables linear amplification of the input signal with high efficiency using non-linear components, explaining its widely used name; LINC (Linear amplification using Nonlinear Components) [32]. The conceptual block diagram of a conventional outphasing amplifier is shown in Figure 2.1. In this approach the amplitude modulated input signal is converted to two anti-phase

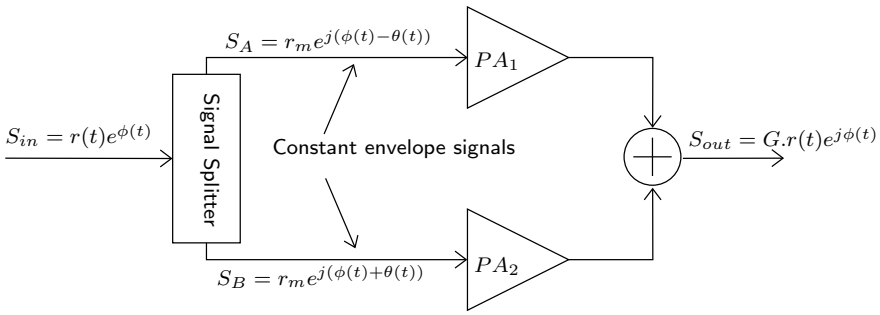


**Figure 2.1:** *Conceptual block diagram of a conventional outphasing amplifier*

phase modulated signals and amplified by two highly efficient, but not necessarily linear power amplifiers. The amplified output signals are then summed by an output power combiner to recover back the amplified replica of original amplitude modulated signal. The operation of the outphasing amplifier can be represented mathematically by (2.1) to (2.4)

$$S_{in} = A(t)\cos(\omega_c t) \tag{2.1}$$

$$S_A = \frac{A_m}{2} cos(\omega_c t + \cos^{-1}(A(t)/A_m) \tag{2.2}$$

$$S_B = \frac{A_m}{2} cos(\omega_c t - \cos^{-1}(A(t)/A_m)) \tag{2.3}$$

$$S_{out} = G.S_A + G.S_B = G.A(t)\cos(\omega_c t) = G.S_{in}. \tag{2.4}$$

$S_{in}$ is the amplitude modulated signal at the input of the outphasing amplifier, $G$ is the gain of the branch amplifiers and $S_A$ and $S_B$ are the input signals to the branch amplifiers. The efficiency and linearity of the outphasing amplifiers are very much dependent on how the output signals are combined together at the output of PA devices. There are two main types of output power combiners, the isolating power combiners (e.g., Wilkinson power combiner) and the non-isolating power combiners like the Chireix power combiner. The properties of these power combiners are explained in detail in the following sections.

### 2.1.1 Isolating Power Combiner

As its name suggests, this power combiner keeps the PA devices in an outphasing transmitter isolated from each other irrespective of the outphasing angle in the system. An outphasing transmitter with a Wilkinson type power combiner is shown in the Figure 2.2. A simple analysis of the circuit shows that the impedance seen by each of the PA devices is always constant irrespective of the outphasing angle, hence the PA devices remain effectively isolated from each other. As a result the linearity of the output signal will be high [31], whereas the related output power delivered to the load is given by (2.5) and the power consumed in the hybrid terminations is given by (2.6)

$$P_{out} = P_m \cos^2(\phi) \tag{2.5}$$

$$P_{losses} = \frac{2V^2 \sin^2(\phi)}{2R_L} \Rightarrow P_m sin^2(\phi). \tag{2.6}$$

Whereas $\phi$ in (2.5) and (2.6) is the outphasing angle, $R_L$ is RF load and $P_m$ is the maximum output power. As one can observe, this high linearity is achieved at the stake of losses in the power combiner. Because once the outphasing angle is increased beyond zero degrees, a voltage difference will appear at the isolating

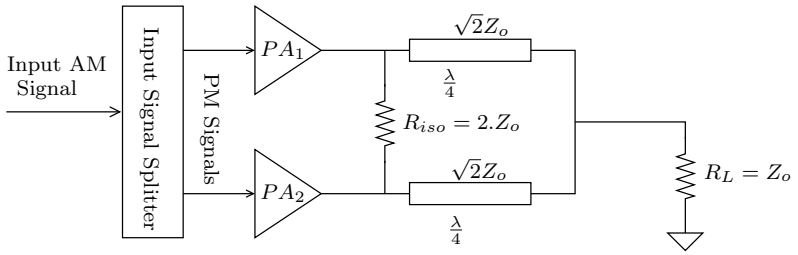


**Figure 2.2:** *Outphasing amplifier with Wilkinson power combiner*

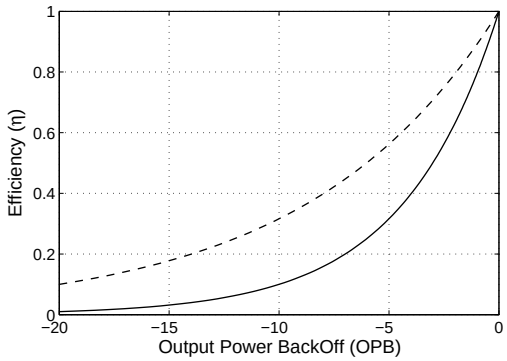


**Figure 2.3:** *Solid Lines show the normalized efficiency of an outphasing transmitter with isolating power combiner, and dotted lines show the normalized efficiency of a class-B transmitter*

resistor $R_{iso}$ causing power loss. Therefore, the resulting CW efficiency of this transmitter implementation drops as the outphasing angle is increased, which is shown in Figure 2.3. The efficiency of the outphasing transmitter drops even more rapidly than a simple class-B amplifier, resulting in low average efficiency for modulated signals, like W-CDMA.

There are a few techniques proposed in the literature [33][34] for improving the average efficiency of the isolating outphasing transmitters but these are not very effective. For example using an outphasing amplifier with a rat race power combiner hybrid and power recycling(Figure 2.4) [33][34]. In this approach the port 4 is isolated only if the input powers to port 1 and port 2 are in-phase, otherwise, power is leaked into port 4 which is dissipated in the 50Ω termination connected at that port. In order to preserve the efficiency of the system in Figure 2.4 a power recycling [33] approached is used, in which the dissipating 50Ω termination is replaced by an impedance matched rectifier, which converts the leaked power at port 4 to DC power and feed it back to the biasing network. On first sight the idea seems to be very elegant, but actual implementations suffer in efficiency due

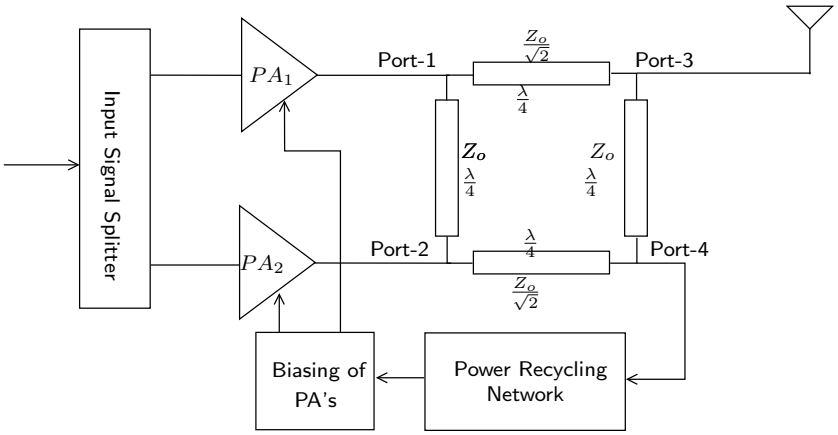


**Figure 2.4:** *Efficiency enhancement of outphasing with power recycling approach*

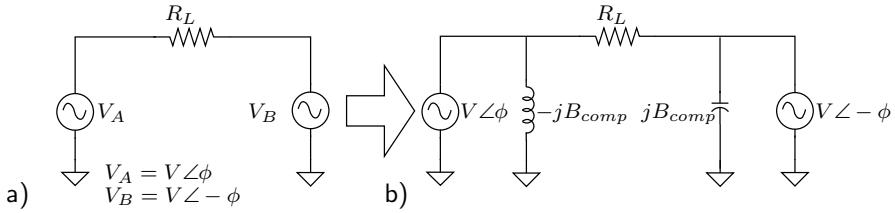


**Figure 2.5:** *The conceptual block diagram of a Chireix transmitter*

to the low conversion efficiency of the recycling network. Moreover, the linearity is also affected because isolation will be degraded due to the non-perfect 50Ω impedance match provided by the recycling network [33].

### 2.1.2 Non-Isolating Power Combiners

Outphasing amplifiers using non-isolating power combiners uses the interaction between the PA devices to enhance the average efficiency of the amplifier system. However doing so will compromise the achievable linearity of the outphasing amplifier [31]. The most well known out of these combiners is the Chireix combiner [10], which is the basis of the advanced multi-mode amplifier presented in the next chapters, therefore a complete analysis of this combiner will be presented in the following sections.

## 2.2 Chireix Transmitter

The Chireix transmitter [10][32] uses a non-isolating power combiner, which in principle can increase the average efficiency of the transmitter. The most simple block diagram of a Chireix transmitter is shown in the Figure 2.5, which consists of a floating load resistor $R_L$ and voltage sources $V_A$ and $V_B$ representing the outputs of two highly efficient branch power amplifiers. The output power delivered to the load $R_L$ in the circuit of the Figure 2.5 depends on the voltage difference over the resistor, which is at its maximum when the voltage sources are perfectly out of phase, and is zero when these are exactly in-phase. Therefore the output power is dependent on the outphasing angle and a simple analysis of the circuit leads to (2.7) for the output power as function of the outphasing angle

$$P_{out} = P_m sin^2(\phi) \tag{2.7}$$

with

$$P_m = 0.5\frac{(2V)^2}{R_L} = \frac{2V^2}{R_L}. \tag{2.8}$$

Where $P_m$ is the maximum output power (2.8) and $\phi$ is the outphasing angle between the voltage sources. In addition to the output power, it is also interesting to analyze the admittance seen by each of the voltage sources. The admittance is modulated due to the interaction between the voltage sources and is given by (2.9). Note that there is an outphasing dependent real and imaginary part, which are both plotted in Figure 2.6, the real part decreases as the outphasing angle is decreased, while the imaginary part show a cosinusoidal behavior

$$Y_{A/B} = \frac{2}{R_L}\sin^2(\phi) \mp j.\frac{1}{R_L}\sin(2\phi). \tag{2.9}$$

The decrease of real part of the admittance is useful for the enhancing the efficiency of the PA devices at back-off power levels, but, due to the presence of reactive susceptance, the efficiency of the PA devices will still not improve in practical situations [7]. To overcome this problem Chireix proposed to tune-out these susceptances by the insertion of two parallel compensating susceptances $B_{comp}$ and $-B_{comp}$, which will result in purely ohmic loading conditions for the PA devices at the two outphasing angles ($\phi_{comp}$ and $\frac{\pi}{2} - \phi_{comp}$), causing the efficiency to peak at these outphasing angles as reflected by the efficiency characteristics of the compensated Chireix transmitter in Figure 2.7.

The circuit of Figure 2.5 provides good support to understand the basic principal of the Chireix transmitter, but the use of a floating load is, in most practical implementations is not desirable. Therefore typically a balun is used to convert the floating load into a single-ended load [6], an action that can easily be implemented by two quarter wave transmission lines resulting in the circuit of Figure 2.8.

The quarter wave transmission lines in the Figure 2.8 convert the output voltages

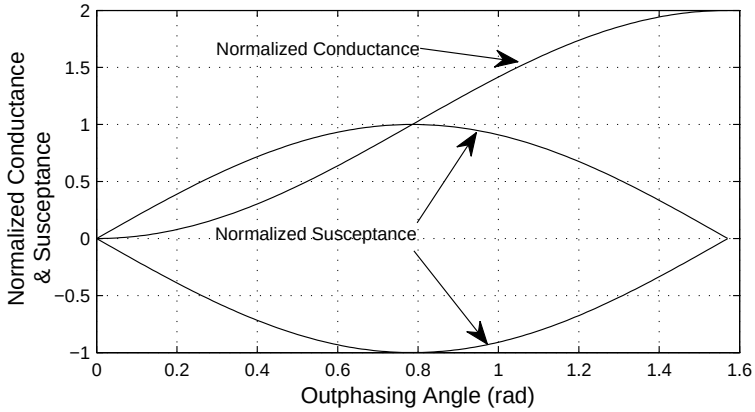


**Figure 2.6:** *Load modulations of the conductance and susceptance in an outphasing transmitter*

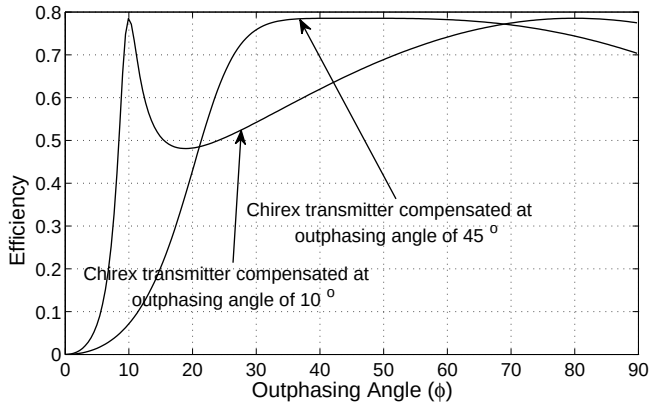


**Figure 2.7:** *CW efficiency vs outphasing angle for Chireix amplifiers using different compensation angles*

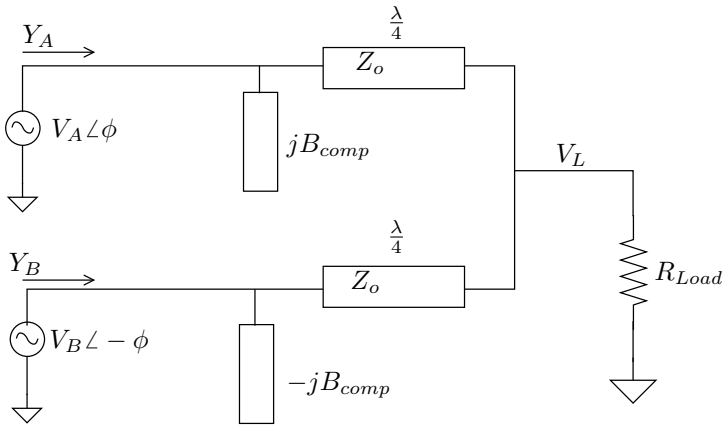


**Figure 2.8:** *Block diagram of Chireix transmitter with transmission line balun*

of the voltage sources to currents, which are added together at the output node and supplied to the single-ended load resistor. The only difference between the circuit with floating load and its transmission line equivalent is a phase change between voltages sources. This has a consequence that while in the original circuit the output power is maximum when the voltage sources are out-of-phase, in this circuit the output power is maximum when the voltage sources are in phase. As such the circuit is a more practical implementation of the Chireix transmitter, which for this reason we will use it in all further analyses. Moreover due to the $\frac{\pi}{2}$ phase shift the equations 2.7 to 2.9 are adjusted to reflect this shift of outphasing angle, resulting in equations (2.10) to (2.12)

$$P_{out} = P_m cos^2(\phi), \tag{2.10}$$

with

$$P_m = \frac{2R_L}{Z_o^2}(V^2), \tag{2.11}$$

Assuming $V_A = V_B = V$ which is the case in a conventional outphasing amplifier,

$$Y_{A/B} = \frac{R_L}{Z_o^2} 2\cos^2(\phi) \mp j.\frac{R_L}{Z_o^2}\sin(2\phi). \tag{2.12}$$

Moreover if the Chireix transmitter is chosen to be compensated at the outphasing angle $\phi_{comp}$, the required parallel susceptances are given by (2.13) and loading conditions of the PA devices is given by (2.14). Additionally, if the PA devices are assumed to be ideal and operating in class-B mode, the efficiency of the transmitter can be normalized to the class-B values as is represented by (2.15)[6]

$$B_{comp} = \frac{R_L}{Z_o^2}\sin(2\phi_{comp}), \tag{2.13}$$

$$Y_{A/B} = \frac{R_L}{Z_o^2}2\cos^2(\phi) \mp j\frac{R_L}{Z_o^2}\sin(2\phi) \pm jB_{comp}. \tag{2.14}$$

$$\eta(\phi, \phi_{comp}) = \frac{\frac{\pi}{4}}{\sqrt{1+\frac{1}{4}(\frac{\sin(2\phi_{comp})-sin(2\phi)}{\cos(\phi)^2})^2}}. \tag{2.15}$$

### 2.2.1 Selection of Compensation Angle

The compensation angle $\phi_{comp}$ determines the shape of efficiency versus output power back-off (PBO) characteristics of the Chireix transmitter, and can be optimized to maximize the average efficiency for a modulated signal [7][8][16]. In that case, the overlap between the power probability density function of modulated signal and efficiency characteristics of the transmitter is at its maximum. A probability density function (PDF) of W-CDMA signal with a particular peak to average ratio $\epsilon$ can be represented by Rayleigh distribution [35]

$$\rho(V_n, \epsilon) = 2V_n\epsilon e^{(-V_n^2\epsilon)}, \tag{2.16}$$

whereas $V_n$ is normalized the output voltage over the load resistor, and for a Chireix transmitter $V_n$ can be defined as $V_n = \sqrt{\frac{P_L}{P_m}} = \cos(\phi)$.

To ease our calculations, the efficiency of the Chireix transmitter can be expressed in form of normalized voltages $V_n$ as given by (2.17) [16]

$$\eta(V_n, \phi_{comp}) = \frac{\frac{\pi}{4}}{\sqrt{1+\frac{1}{4}(\frac{\sin(2\phi_{comp})-2\sqrt{V_n^2-V_n^4}}{V_n^2})^2}}. \tag{2.17}$$

With this notation, the average efficiency of the amplifier can be calculated using (2.16) and (2.17) [7][16].
Consequently,

$$\eta_{\text{avg}}(\phi_{comp}) = \frac{P_{\text{out\_avg}}}{P_{\text{dc\_avg}}} = \frac{\int_{V_n=0}^{V_n=V_m} P_{\text{out}}(V_n)\rho(V_n)\mathrm{d}V_n}{\int_{V_n=0}^{V_n=V_m} \frac{P_{\text{out}}(V_n)}{\eta(V_n,\phi_{comp})}\mathrm{d}V_n}. \tag{2.18}$$

It can be noted from (2.18) that the average efficiency is a function of the compensation angle $\phi_{comp}$. The optimum value of this compensation angle can be obtained analytically by solving (2.19)

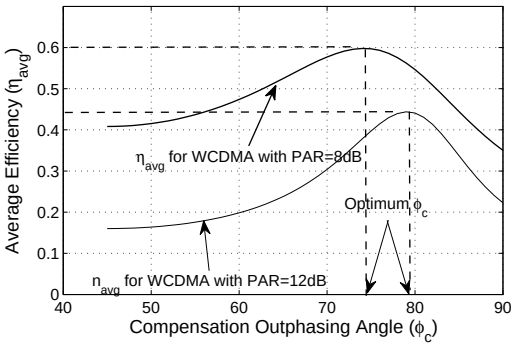


**Figure 2.9:** *$\eta_{avg}$ versus compensation angle $\phi_{comp}$ for W-CDMA signals with a peak-to-average ratio of 8 & 12dB*

$$\frac{\partial \eta_{avg}(\phi_{comp})}{\partial \phi_{comp}} = 0. \tag{2.19}$$

It is also possible to perform this optimization using a graphical approach [7][16], by plotting the average efficiency as a function of compensation angle ($\phi_{comp}$) and locate the optimum value of $\phi_{comp}$ for which the average efficiency is at its maximum. As an example of such optimization, performed on a W-CDMA signal with a peak to average ratio of 8 & 12dB to find the optimum compensation angles (Figure 2.9), which proves to be $74^o$ and $79^o$ respectively. The power probability density function ($V_n^2.\rho(V_n, \epsilon)$) and the optimum efficiency characteristics for 8 and 12dB signals are plotted in the Figure 2.10, showing the maximized overlap between the power probability density and efficiency characteristics of the optimized transmitters. It is also advantageous to study the behavior of the Chireix transmitter with W-CDMA signal with different peak-to-average-ratios (PAR) to find the related maximum average efficiencies. For this purpose, the maximum attainable average efficiencies & optimum compensation angles $\phi_{comp}$ of the amplifier are plotted against the peak to average ratio in Figure 2.11. This result shows that the maximum attainable average efficiency degrade as the peak to average ratio of the W-CDMA signal is increased, and drops below 50% once the peak to average ratio is increased beyond 10dB. This drop in average efficiency gets worse once the non-idealities of the PA devices are taken in account, which will be discussed in the next section.

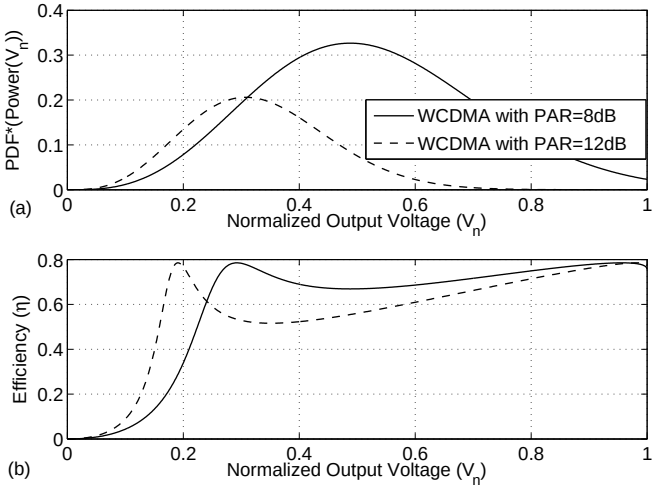


**Figure 2.10:** *a) Power probability distribution (PDF) of the 8dB and 12dB PAR, W-CDMA Signals b) Corresponding optimized efficiency characteristics*

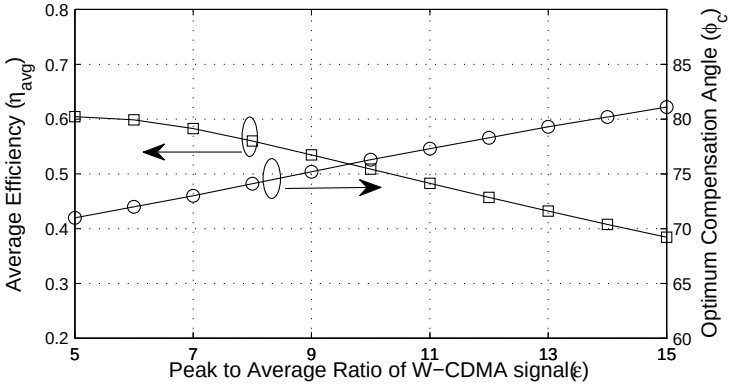


**Figure 2.11:** *Optimum outphasing angles and average efficiencies for W-CDMA signals with different peak-to-average ratio*

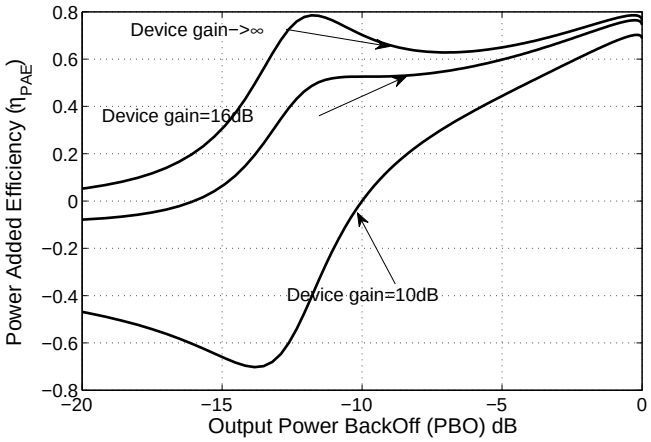


**Figure 2.12:** *Plot of average power added efficiency for different gains of the PA devices*

## 2.3 Chireix Amplifier with Non-ideal Devices

So far we have discussed the performance of the Chireix transmitter with ideal devices, but in this section, an analysis of Chireix amplifier is presented using a more realistic model of active devices. Using this model the constraints of practical devices with their related impact on the average efficiency and average power added efficiency is investigated.

### 2.3.1 Limited Gain of PA devices

The performance of a transmitter is usually judged based on its power-added efficiency (see 2.20), which is a function of the gain of transmitter. In a Chireix or any conventional outphasing transmitter, the input power is kept constant and the output power is backed-off by varying the outphasing angle. This implies that true outphasing transmitters will show a variable gain which is decreasing linearly with output power as described by (2.21).

$$\eta_{PAE} = (\frac{P_{out} - P_{in}}{P_{DC}}) \Rightarrow \eta_{PAE} = \eta(1 - \frac{1}{G}) \tag{2.20}$$

$$G = G_m - P_{back-off} \tag{2.21}$$

Practical PA devices have limited gain ranging from 12∼20dB (at GHz frequencies) [36][37][38].This has a pronounced effect on the CW PAE of Chireix transmitter, which is plotted for 12dB, 16dB and for ideal devices ($gain \longrightarrow \infty$)

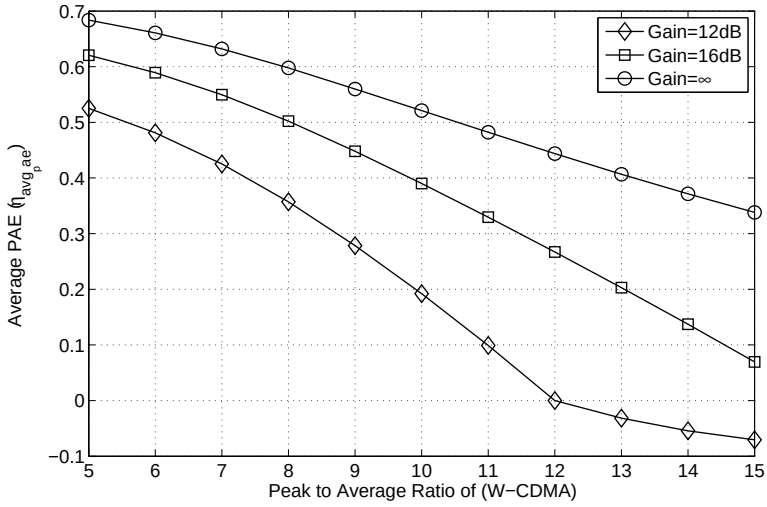


**Figure 2.13:** *Plot of Average Power Added Efficiency with different Gains of the PA devices, while keeping the input power constant*

in Fig 2.12, using (2.20) and (2.21).
As expected the plots show a clear degradation of PAE of the transmitter as the gain of the devices is decreased, and its even become negative after a certain PBO indicating the the transmitter for these power levels has a gain less than 0dB, and is no longer amplifying the input signal.
An even more interesting conclusion can be made if the average power added efficiency of the system is calculated by using (2.20), (2.21), (2.18) and (2.19) for W-CDMA signals with different peak to average ratios, which is plotted in the Figure 2.13. The PAE decreases with the decreasing gain, but beyond a certain peak to average ratio, it becomes negative, which implies that with those particular devices it is no longer possible to amplify W-CDMA signals efficiently with the peak-to-average ratio more than that value. For example for PA devices with 12dB gain, it is not possible to amplify the W-CDMA signals with peak to average ratio more than 12dB, as indicated by the plots of the Figure 2.13.

### 2.3.2 Finite Output Resistance

Practical PA devices have finite output resistance which determines the effectiveness of the load modulation applied to the active device to increase its efficiency [39]. To investigate this limitation quantitatively, consider the simplified schematic of a PA device connected in the Chireix transmitter [16] as shown in the Figure 2.14 while the PA devices are still assumed to behave like perfect voltage

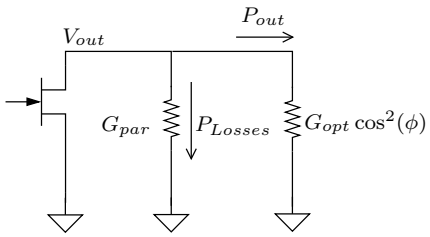


**Figure 2.14:** *Model of the PA devices with parasitic output resistance*

sources, and the reactive loading due to outphasing is neglected for simplicity. Moreover $G_{load}$ in the circuit of Figure 2.14 is the outphasing dependent load conductance, which is given by (2.22)

$$G_{load} = G_{opt}\cos^2(\phi); \tag{2.22}$$

Whereas $G_{opt}$ in (2.22) is the optimum load of the device for maximum performance.

The efficiency of the circuit of the Figure 2.14 depends on the ratio of the parasitic conductance $G_{par}$ and the outphasing dependent load conductance ($G_{load}$) as is given by (2.23)

$$\eta_{dev} = \frac{1}{1+\frac{G_{par}}{G_{load}}} \Rightarrow \frac{V_n^2}{V_n^2+\gamma}, \tag{2.23}$$

whereas $\gamma = \frac{G_{par}}{G_{opt}}$. The results are plotted in Figure 2.15 by using different ratios of parasitic conductance $G_{par}$ and optimum load conductance $G_{opt}$. Efficiency suffers especially at low output power levels, because at those levels $G_{par}$ is bigger than $G_{load}$, hence a significant portion of the useful output power is wasted in the parasitic output conductance.

The efficiency of the Chireix transmitter with the lossy devices can be obtained by multiplying the efficiency of the lossy device with the efficiency of the Chireix transmitter represented by (2.24). This data is plotted in the Figure 2.16, which clearly shows the ineffectiveness of the efficiency enhancement techniques in these conditions.

$$\eta_{lossy} = \eta_{dev}.\eta_{chireix} \tag{2.24}$$

The impact of parasitic loading of the output of the devices can also be studied for modulated signals. Average efficiencies are calculated for W-CDMA signals with difference peak-to-average-ratios and plotted in Figure 2.17. It can be seen

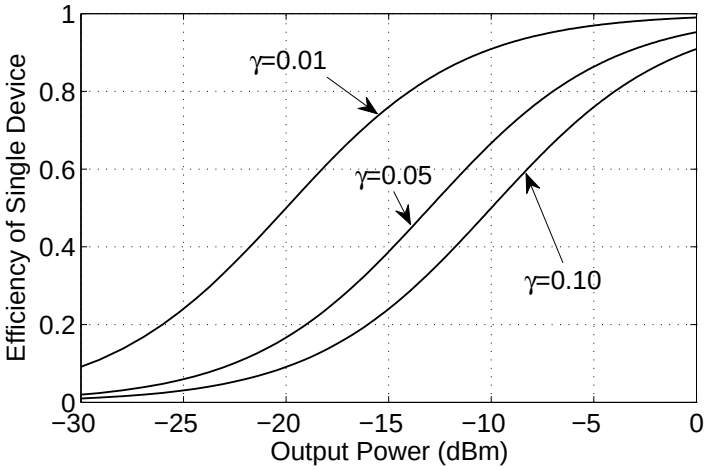


**Figure 2.15:** *Normalized efficiency of the PA devices connected in a Chireix combiner if the reactive loading is neglected*

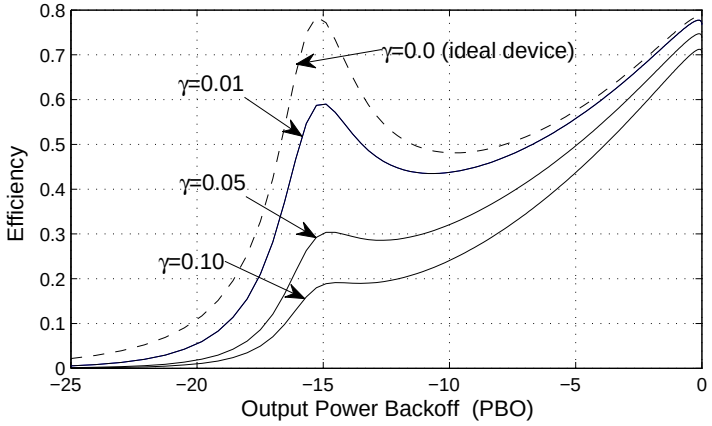


**Figure 2.16:** *Efficiency of the Chireix transmitter for devices with different values of parasitic conductance*

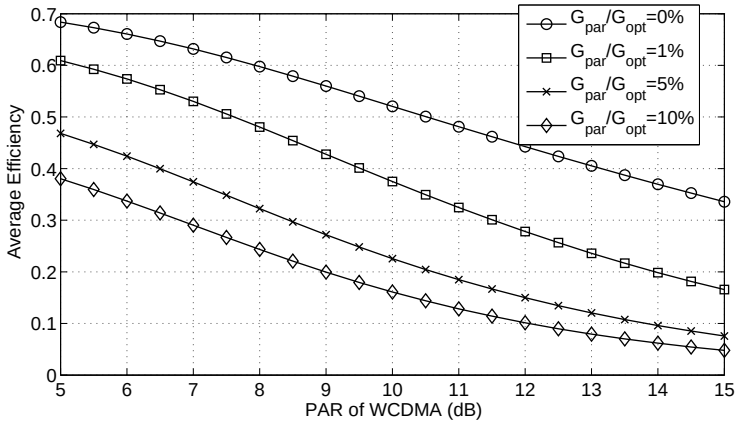


**Figure 2.17:** *Average efficiencies of Chireix transmitter with lossy devices*

clearly from the Figure 2.17 that the maximum achievable average efficiency of the Chireix transmitter for modulated signals degrades drastically as the losses of the PA devices are increased

## 2.4 Conclusions

This chapter provides the analysis for the Chireix outphasing amplifiers for their performance when operated with W-CDMA signals. The optimum outphasing angles and maximum attainable average efficiencies are calculated and discussed. On basis of the results of this chapter we can conclude that the Chireix amplifier can be highly efficient but at the same time, very sensitive to the non-idealities of the devices. Especially, the losses of the PA devices can have a devastating effect on the performance of the overall amplifier. Moreover the limited gain of PA devices will also affect the performance of an outphasing amplifier when operated with W-CDMA signals having a high peak-to-average ratio.

Chapter 3

# Mixed Mode Outphasing Transmitter

## 3.1 Introduction

In chapter 2 we have identified some basic performance constraints by analyzing conventional outphasing amplifiers. Although most of these problems are due to the non-idealities of the PA devices, some of these problems also arise from inherent limitations of the outphasing concept [16]. The most severe problems are,

- Low average efficiency for signals with a high PAR.
- High sensitivity to losses in the PA devices.
- Low dynamic range (due to path mismatches).
- High bandwidth expansion of the modulated input signals.

Due to the above mentioned problems, the outphasing concept is currently not a popular choice for 3G and future 4G base-station transmitters. In this work we aim to change this situation and improve for the constraints, stated above, by introducing a new class of outphasing amplifiers that make use of outphasing as well as class-B operation in deep power back-off. In such an approach, the outphasing action is limited up-to a certain threshold outphasing angle $\phi_{thr}$ which is chosen close to or at the second high efficiency point where the complex loading of the active devices is compensated. Beyond this point the branch amplifiers are operated in class-B mode, by fixing the outphasing angle to $\phi_{thr}$ and using the input power control of the branch amplifiers to back-off the output power. We refer to these amplifiers as mixed-mode amplifiers due their hybrid outphasing / class-B type of operation [16].
Although outphasing and the combination of outphasing and input power control

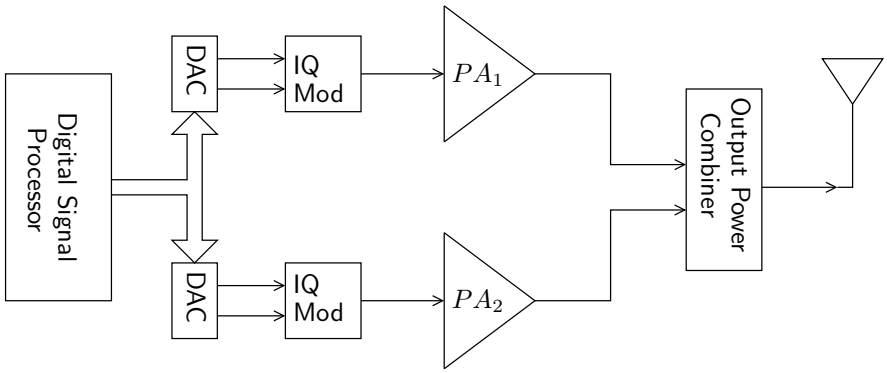


**Figure 3.1:** *Block diagram of a digitally controlled, mixed-mode outphasing transmitter.*

is not new [40][41][42], to the author's best knowledge, a true high-efficiency, high-power outphasing amplifier with a competitive industrial performance was not yet been brought to light. Moreover a clear analysis showing the use of input power control and its impact on different performance parameters e.g., average efficiency, gain and efficiency was also missing.
To fill this gap, this chapter re-analyzes outphasing amplifiers, but now with the option of switching to class-B operation after a certain threshold outphasing angle $\phi_{thr}$. In addition to this, at a later stage the option of using also input power control in the outphasing region will be explored. With this additional feature even higher gain and power-added-efficiency (PAE) can be achieved when dealing with practical devices, a situation that strongly deviates from the idealized case. To verify the proposed techniques, a 90-W reference amplifier is designed with independent input control of the branch amplifiers (Figure 3.1). Consequently, this reference amplifier can be operated in both in mixed-mode, as well as, in pure outphasing mode enabling a clear comparison performance comparison for both operating modes.

## 3.2 Efficiency of the Mixed-Mode Outphasing Amplifier

### 3.2.1 CW Efficiency

The benefit of switching to class-B mode in power back-off can be best understood, if we compare the CW efficiency versus power back-off characteristic of a pure outphasing amplifier with Chireix power combiner with that of a traditional class-B amplifier. For this purpose, we consider Figure 3.2 where the CW efficiencies of the Chireix amplifier and the class-B amplifier are plotted versus their normalized output voltages [43][44]. Note that for a class-B amplifier, the efficiency is always linearly proportional to its normalized output voltage, therefore,

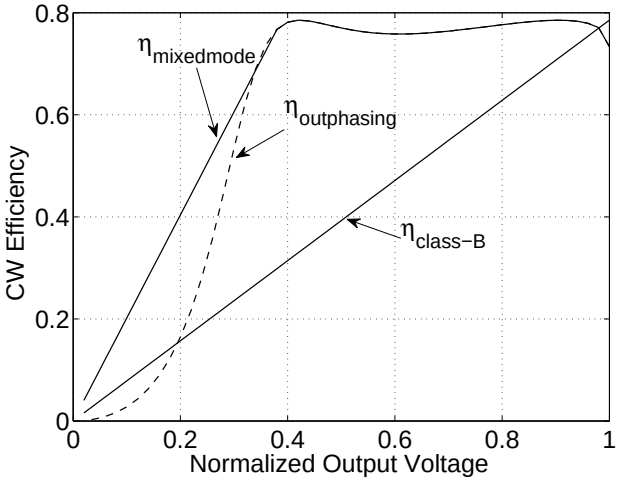


**Figure 3.2:** *CW efficiency in pure outphasing, mixed-mode operation and class-B amplifier operation. Note that the output voltage in this plot is normalized by its maximum value and the compensation angle is equal to* $66^o$

the efficiency degradation with increased power back-off is quite modest.
In contrast, when considering the efficiency of the pure Chireix outphasing amplifier, we also find, besides the desired efficiency peaking in power back-off, a very steep drop in efficiency versus increased back-off power, once the outphasing angle is increased beyond the compensated angle $\phi_{comp}$. This steep efficiency drop can be explained by the fact that, when using the outphasing beyond the compensation angle $\phi_{comp}$, the loading conditions of the active devices become almost entirely reactive, something that is very harmful for the efficiency of the branch amplifiers.
Hence due to this phenomenon, pure outphasing amplifiers have a low CW efficiency when operated beyond their compensation angle $\phi_{comp}$. Therefore, if the input powers and the phases of the amplifier branches can be controlled independently, it is possible for an outphasing amplifier configuration to switch to class-B just after $\phi_{comp}$. Doing so will result in less reactive loading conditions for the active devices at these low output power levels, while one can benefit from the much lower efficiency roll-off of a class-B operated amplifier. The resulting efficiency curve is shown by solid line in Figure 3.2, which shows that CW efficiency of the amplifier indeed improves significantly at these lower output power levels.
The input outphasing angle, input voltage and resulting efficiency (for a time varying input signal r(t)) is given for the mixed-mode outphasing amplifier by the equations (3.1), (3.2) and (3.3)

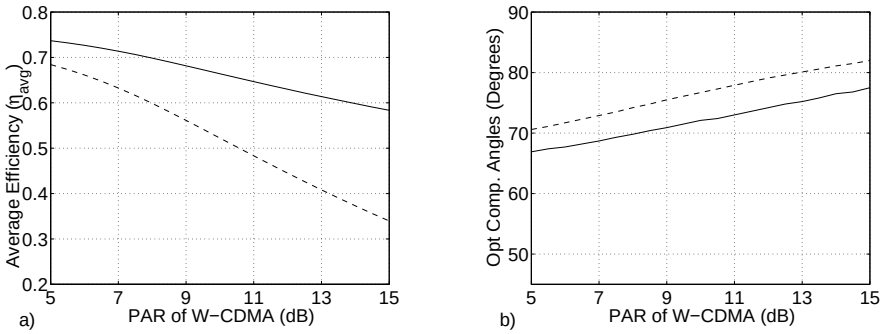


**Figure 3.3:** *a) Average efficiency of Chireix amplifier in mixed-mode operation (solid lines) and for pure-outphasing mode (dashed lines). b) Optimum compensation angles of Chireix amplifier for mixed-mode (solid lines) and for pure-outphasing operation (dashed lines)*

$$\phi_{A/B}(t) = \begin{cases} acos(r(t)) & \text{if } acos(V_{out})) < \phi_{thr} \\ \phi_{thr} & \text{if } acos(V_{out}) \geq \phi_{thr} \end{cases} \tag{3.1}$$

$$V_{in_{A/B}}(t) = \begin{cases} 1 & \text{if } acos(V_{out})) < \phi_{thr} \\ \frac{acos(\phi_{thr})}{V_{out}} & \text{if } acos(V_{out}) \geq \phi_{thr} \end{cases}. \tag{3.2}$$

Whereas the equation for the efficiency of the mixed-mode outphasing amplifier can be written as

$$\eta_{mixedmode} = \begin{cases} \eta_{outphasing} & \text{if } \phi < \phi_{thr} \\ \eta_{outphasing}(\phi_{thr}).\frac{V_{out}}{V_{thr}} & \text{if } \phi \geq \phi_{thr} \end{cases}. \tag{3.3}$$

Note that in $\phi_{thr}$ in (3.1), (3.2) and 3.3 is the threshold outphasing angle, beyond which the mode of operation of the mixed-mode amplifier is changed from outphasing to class-B mode. $V_{out}$ is the normalized output voltage.

### 3.2.2 Average Efficiency for Modulated Signals

The previous section showed that the CW efficiency of the Chireix amplifier indeed improves at lower power levels if class-B mode is used beyond a certain threshold outphasing angle ($\phi_{thr}$). This improvement of CW efficiency should also result in an enhancement of the average efficiency of amplifier especially for modulated signals with high PAR.

The maximum average efficiency for the mixed-mode operation and the corresponding threshold outphasing angles ($\phi_{thr}$) can be calculated by using (3.1) and (3.3) together with the equations for the average efficiency of outphasing amplifiers in Chapter 2. The resulting average efficiencies ($\eta_{avg}$) and optimum threshold

angles ($\phi_{thr}$) are plotted in the Fig 3.3, along-with those for the pure outphasing mode (dotted lines) to allow easy comparison. The plots of Figure 3.3 clearly show that the mixed mode outphasing amplifier out-performs the traditional outphasing amplifier at all values of PAR, while this performance difference increases with the PAR of the W-CDMA signal. For example, for a standard W-CDMA signal (PAR=9.6dB) the improvement in average efficiency of the mixed-mode amplifier over the conventional outphasing case is more than 15%
Another interesting phenomenon which can be observed from Figure 3.3 is that the optimum threshold angle $\phi_{thr}$ for mixed-mode operation is smaller than the optimum compensation angle $\phi_{comp}$ needed for pure out-phasing operation with any given PAR. This effectively results in a reduced load modulation of the PA devices in mixed-mode operation and therefore the mixed-mode amplifier will be less sensitive to the losses of the PA devices.

### 3.2.3 Performance considerations when using lossy PA devices

The previous section showed that mixed-mode outphasing amplifier employs reduced load modulation conditions on the PA devices compared to the situation of using pure outphasing, therefore the efficiency degradation due to the losses of the PA devices should also be lower. In order to quantify this improvement, the average efficiency of the mixed-mode amplifier for a W-CDMA signal is calculated using the same model for the lossy devices as in section 2.3. The results are plotted in Figure 3.4 along-with the average efficiency of the pure outphasing mode amplifier (dotted lines). These results show that, although the maximum attainable average efficiencies of the mixed-mode amplifier degrade due to losses, this degradation is much lower than that of pure outphasing amplifier. For example for a W-CDMA signal with a PAR equal to 9.6dB, the average efficiency of pure outphasing transmitter drops by almost 30% (if the losses of the PA devices are set to 5%), whereas the average efficiency of the mixed-mode transmitter for the W-CDMA signal with same PAR drops only by 10%. Therefore, there is a three-fold efficiency improvement when the losses of the PA devices are considered.
The main cause of this improvement is the ability of the mixed-mode amplifier to reduce the load modulation of the PA devices something, that is essential when dealing with practical devices with losses [16][17]. So, by switching to the class-B mode excessive load modulations on the PA devices are avoided, while at the same time achieving an improved average efficiency. This fact is also reflected in the plots of the Figure 3.5, which show that the optimum threshold outphasing angles $\phi_{thr}$ should decrease as the losses of the PA devices are increased.

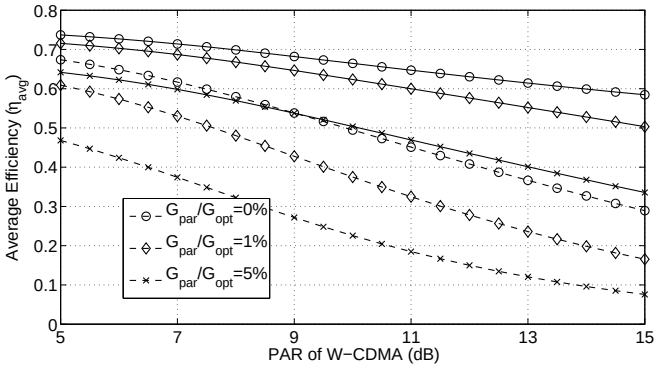


**Figure 3.4:** *Average efficiency of the amplifier for: mixed-mode (solid lines) and pure outphasing mode (dashed lines) for W-CDMA signals*

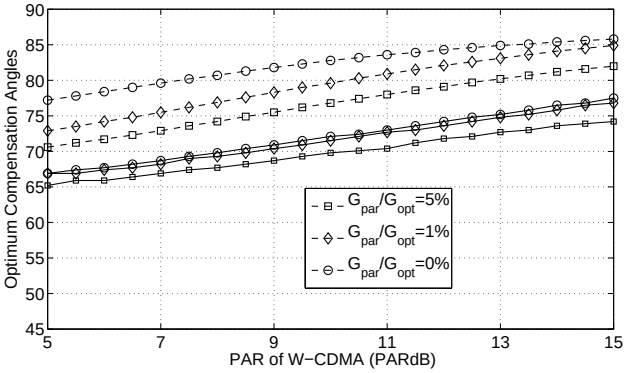


**Figure 3.5:** *Optimum threshold / compensation angle for: mixed-mode (solid lines) and pure outphasing mode (dashed lines) for W-CDMA signals*

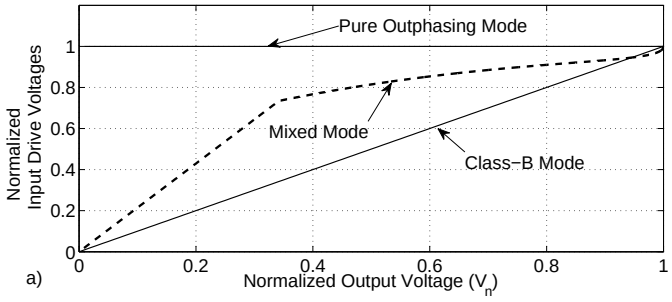


**Figure 3.6:** *Normalized Input drive of branch amplifiers for class-B, pure outphasing, and mixed-mode operation*

## 3.3 Input Signal Generation

In classical outphasing-amplifier implementations, the branch amplifiers are driven by a constant envelope signal such that PA devices are always operated in saturation mode [31], and therefore, closely approximate the behavior of a controlled voltage source. The drawbacks to this approach are the high input power and the low effective gain that will be achieved in power back-off operation due to this constant input amplitude. As a result, the power-added efficiency (PAE) will drop rapidly in power back-off since it has become dependent on the RF input power. To improve the PAE, one can make use of the fact that most PA devices (when designed in class-B mode) act more like a controlled current source rather than an ideal controlled voltage source. Therefore, the input power needed to drive a device into saturation, reduces with the outphasing angle (due to the increased loading with increasing outphasing angle). Consequently, reducing the input power in back-off operation will improve gain, as well as PAE; in additions, it will also avoid excessive overdrive conditions of the active devices that can yield degradation effects.

### 3.3.1 Optimum Input Signals Generation for the Branch Amplifiers

As discussed, unlike in the case of classical outphasing amplifiers, the input signals for the branch amplifiers of the mixed-mode outphasing amplifier contains amplitude modulation as well as phase modulation to improve for the gain and PAE of the system. Consequently for a particular complex modulated test signal $S_{in}$

$$S_{in} = r(t)e^{j\theta(t)} \tag{3.4}$$

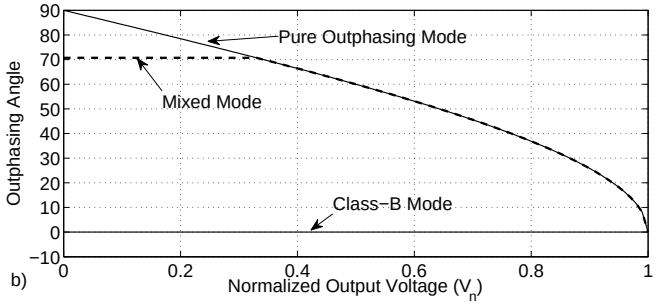


**Figure 3.7:** *Phase difference between the branch amplifiers for class-B, pure outphasing, and mixed-mode operation*

Whereas $\theta(t)$ represents the angle modulation and r(t) represents the phase modulation in the input signal $S_{in}$. The input signals for the branch amplifier A and B can be described as

$$S_{PA_{A,B}} = V_{in}(t)e^{j(\pm\phi(t)+\theta(t))}. \tag{3.5}$$

in which

$$\phi(t) = \begin{cases} acos(r(t)), & \text{if } acos(r(t)) \leq \phi_{thr} \\ \phi_{thr}, & \text{if } acos(r(t)) > \phi_{thr} \end{cases} \tag{3.6}$$

and

$$V_{in}(t) = \begin{cases} p_o r(t) + p_1 r^2(t) + p_2 r^3(t) + p_3 & \text{if } acos(r(t)) \leq \phi_{thr} \\ \frac{r(t)}{cos(\phi_{thr}} & \text{if } acos(r(t)) > \phi_{thr} \end{cases}. \tag{3.7}$$

The coefficients $(p_o, p_1..p_n)$ in (3.7) are used to implement the input-power control in the outphasing regime, and $p_o$ represents the linear term, while the higher order terms $(p_1, .., p_n)$ are needed to keep the branch amplifiers just at the edge of saturation while operating in the outphasing mode. The actual value of the parameters $(p_o, ..., p_n)$ are determined experimentally as follows; first find the optimum efficiency input power curvature by sweeping both the input power and phase offset of the branch amplifier inputs. Then determining the parameters $(p_o, ...p_n)$ to closely approximate this optimum input power curvature using the curve fitting toolbox of MATLAB.
The various input drive conditions for the different modes of operation are illustrated in Figure 3.6 and Figure 3.7 along with the resulting output loading of the active devices given in Figure 3.8. Note that switching to class-B operation

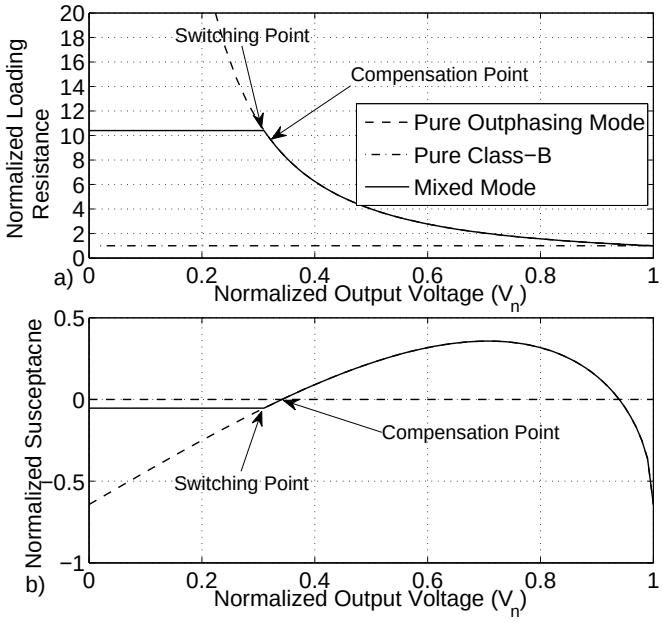


**Figure 3.8:** *Loading conditions of the branch amplifiers for the various modes of operation, a) Real part loading condition b) Reactive part loading condition*

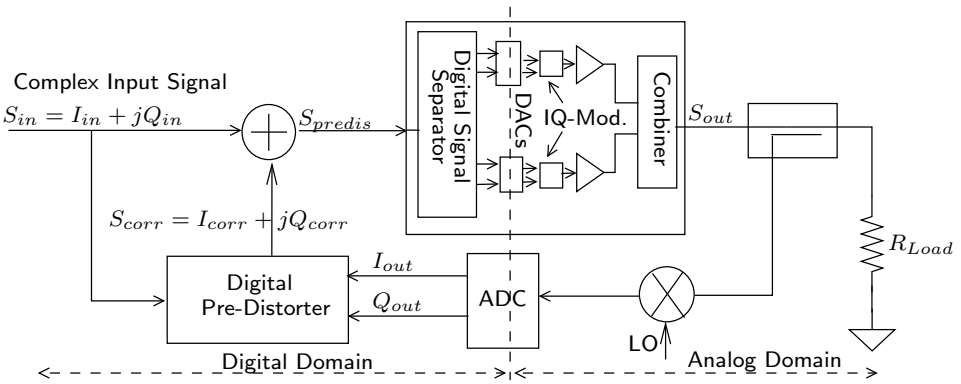


**Figure 3.9:** *Principal block diagram of the memoryless closed-loop DPD*

not only limits the reactive loading in deep power back-off, but also limits the real part of the load to the level defined by the threshold angle (here, almost $10 * R_{opt}$). This will limit the impact of the losses in the output of the devices and the power combining network (see section 3.2.3). Note that the switching is done at the point where the efficiency of the outphasing amplifier starts to drop more rapidly than that of the class-B amplifier, which is slightly different that the point where the outphasing amplifier is entirely compensated for the reactive loading. Doing so yields maximum efficiency at any power level in power back-off operation for the mixed-mode amplifier. However, it must be mentioned that setting $\phi_{thr}$ equal to $\phi_{comp}$ will in practice closely approximate this situation.

### 3.3.2 Digital Pre-distortion (DPD)

Since the modified outphasing amplifier employs input power and phase control and is only optimized for efficiency, its resulting gain characteristic will be non-linear. Consequently, for a fully operational system, DPD will be needed to meet the spectral requirements.
To implement this, we use for the DPD the basic block diagram of Fig 3.9 which makes use of a constellation-mapping based DPD algorithm [45][46]. If each channel of the amplifier is pre-distorted separately, the DPD can be very complex, therefore we assumed that the mixed-mode outphasing amplifier is a single-input, single-output system. This assumption allows the pre-distortion to be applied directly on the input signal $S_{in}$, while the separation for the branch amplifiers is handled in the digital domain by (3.6) and (3.7). The algorithm of pre-distortion, therefore, can be kept very simple, since it only has to compare the amplifier output signal with the original input signal and adjust the error terms in the lookup

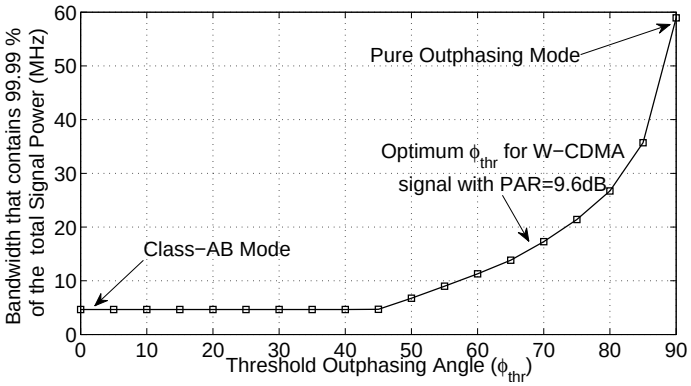


**Figure 3.10:** *Bandwidth expansion of the input signals that drive the branch amplifiers used in the mixed-mode outphasing amplifier as function of the threshold outphasing angle for a W-CDMA 3GPP signal with 9.6-dB PAR*

table to make this match as good as possible. This approach also has some additional advantages like higher dynamic range and less dependency on the path mismatches. We will discuss this DPD approach in chapter 6.

### 3.3.3 Reduction of Modulation Bandwidth Expansion

Another important aspect in the design of the outphasing PA is the modulation bandwidth used for the branch amplifiers which is considered to be notorious for the classical outphasing amplifier [31]. This bandwidth expansion occurs when the original baseband signal is converted to the outphasing signals for the branch amplifier inputs. This modulation bandwidth expansion is mainly caused by the inverse cosine operation in conjunction with associated AM-PM conversion involved in the input-signal processing. Moreover, this phenomenon does not only restrict the modulation bandwidth of the overall transmitter, but also makes the pre-distortion hardware and software more complex and expensive. In addition memory effects in the branch amplifier tend to be more pronounced due to the bandwidth expansion.
In view of this, an additional benefit of the mixed-mode amplifier is its very limited bandwidth expansion compared to the classical outphasing amplifier. This can be concluded by considering two extreme cases, namely $0^o$ and $90^o$ for the outphasing threshold angle $\phi_{thr}$. When the threshold outphasing angle is set to zero, the amplifier operates as a pure class-B amplifier and no bandwidth expansion will be present. On the other hand, if the outphasing angle is set to $90^o$, the amplifier acts like a pure classical outphasing amplifier with related maximum bandwidth expansion (up to a factor approximately 12 for a W-CDMA signal). Therefore, the

bandwidth expansion for the mixed-mode amplifier will lie somewhere between these two extremes. To support the conclusion above, a model for the mixed-mode amplifier was developed in MATLAB and operated with a W-CDMA 3G signal, while using different values for the threshold outphasing angle ($\phi_{thr}$). To estimate the bandwidth expansion of the input signals for the branch amplifiers, the bandwidth is plotted for a W-CDMA signal (PAR=9.6dB, sampling frequency 122.9MHz), where 99.99% of the total signal power is contained. The result is plotted in Figure 3.10 and is in line with the above-mentioned expectations. Consequently, it can be concluded from the Figure 3.10 that for a 9.6-dB PAR W-CDMA signal, a bandwidth expansion factor of only 3.5 can be expected when using the mixed-mode outphasing operation with a threshold angle of $\phi_{thr} = 68^o$.

### 3.3.4 Design of the Mixed-Mode Outphasing Amplifier

To support the previously introduced theory, a W-CDMA base-station amplifier has been designed that makes use of the proposed mixed outphasing / class-B operation. For the active devices in this demonstrator, two 45 W GaN devices have been used, which due their low parasitic output conductance, offer high efficiency even for high-impedance loading conditions. The resulting amplifier provides 90 W peak power (49.5dBm) at a center frequency of 2.14 GHz.

#### Branch Amplifier Cells

The overall efficiency performance of any outphasing amplifier is very much dependent on its branch amplifiers, which must provide high efficiency not only for optimum loading, but also at the maximum load impedances that occur during outphasing (Figure 3.8). Moreover, to guarantee this optimum behavior, the load modulation due to the outphasing should be correctly transferred to the internal drain of the active devices. Therefore, in the design procedure, the disturbing influence of the package and device parasitic elements (e.g., bond wires and output capacitances) must be compensated. In our design, the influence of these parasitic can be considered as a short artificial transmission line with a given characteristic impedance, consequently by adding some additional transmission line length with the same characteristic impedance, the total effective electrical length can be made equal to $180^o$. Note, that for this particular value, the varying load impedance at the output power combiner interface due to outphasing action will be perfectly reproduced at the internal drain terminal of the PA devices. Consequently, the output capacitance of the devices can also be compensated at the end of this $180^o$ (Figure 3.11). Device matching for the real part is incorporated in the design of the output power combiner. Finally, the branch amplifier cells are designed unconditionally stable in order to handle the varying loading conditions due to the outphasing action without any complication.

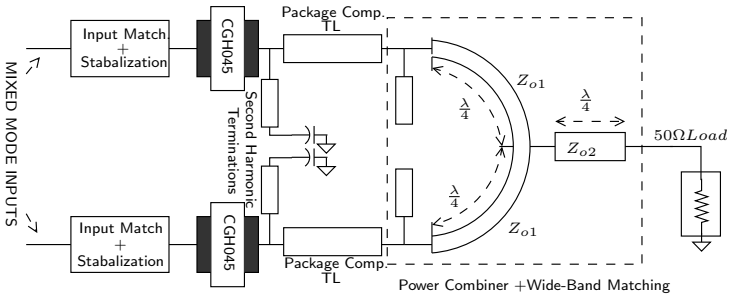


**Figure 3.11:** *Simplified schematic of the mixed-mode amplifier*

### 3.3.5 Power Combiner Design

The Chireix output combiner is also given in the Figure 3.11, it utilizes a conventional two-line microstip power combiner with an additional $\frac{\lambda}{4}$ impedance transformer to implement a two step impedance matching. The low-Q matching results in the desired bandwidth of the overall outphasing amplifier. As a final step, (based on the theory of the previous sections), the optimum Chireix compensation angle was found to be equal to $68^o$ for the desired W-CDMA signal with a 9.6-dB crest factor. The compensation susceptances related to the $68^o$ angle have been combined wit the susceptances needed for compensating the output capacitances of the active devices. The resulting susceptances are added to the power combiner as open stubs. Note that, although on first sight the compensation stubs seem to have the same length, in the actual layout one stub is slightly longer that $\frac{\lambda}{4}$ and the other transmission line is slightly shorter than $\frac{\lambda}{4}$ to implement the desired compensation susceptances.

## 3.4 Experimental Results

The demonstrator amplifier was tested using a mixed-mode measurement setup, which is explained in detail later in chapter 6. In this chapter only the measurement results are given. The amplifier was operated in mixed-mode, as well as, in pure outphasing operation in order to provide clear insight in the performance achievements due to the application of the mixed-mode concept.

### 3.4.1 Single-Tone Characterization

In the previous sections, we have shown that the efficiency of outphasing amplifiers can be improved by optimizing the power and phase of the input signals. For this reason a single-tone characterization is performed to find these optimum input power levels, as well as, the optimum threshold angle $\phi_{thr}$. The optimum

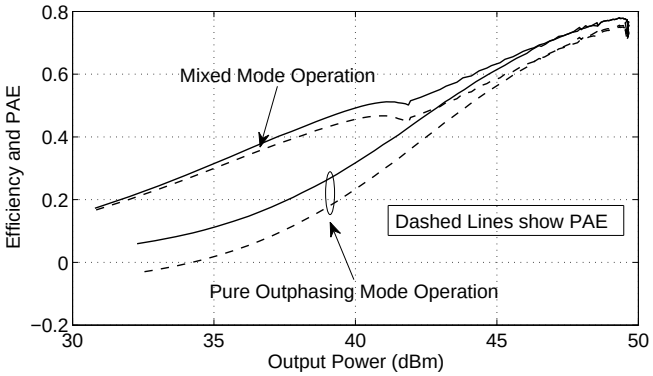


**Figure 3.12:** *Measured CW efficiency and PAE as a function of output power of the 90-W GaN outphasing amplifier when operated in pure outphasing mode, as well as in mixed-mode operation*

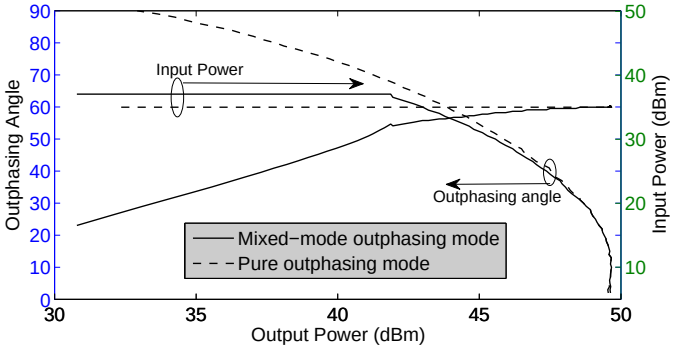


**Figure 3.13:** *Input power drive profiles used for the branch amplifier, in pure outphasing mode, as well as in mixed-mode operation*

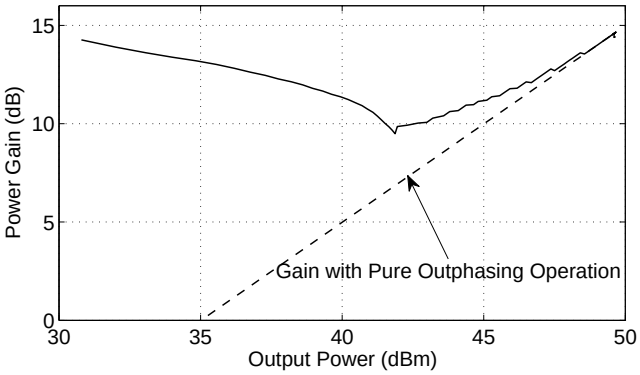


**Figure 3.14:** *Measured transducer power gain of the mixed-mode amplifier and outphasing amplifier as a function of output power*

input power levels with the related phase information are then used to estimated the optimum control parameters of (3.6) and (3.7).
This characterization involves an input power sweep with stepped outphasing angles while measuring the output power and phase of the transmitter. Finally by plotting the maximum achievable efficiency for each output power level, the overall achievable efficiency versus output power can be obtained as shown in Figure 3.12.
The efficiency and PAE of the transmitter are measured and plotted for both mixed-mode, as well as, the pure outphasing mode of operation. Note, that when we operate the amplifier as a pure outphasing transmitter with constant input power, we find the early efficiency roll-off in power back-off operation, as predicted by the theory. The performance improvements for the mixed-mode operated outphasing amplifiers are clearly visible. The input drive conditions used in both case are also shown in Figure 3.13. Note that due to the lower input power in mixed-mode operation, the amplifier branches are driven less in saturation, causing a slightly lower output power. Consequently, the outphasing angle required in mixed-mode operated amplifiers for a given output power back-off (OPB) level will be slightly lower than that of pure outphasing mode, as is reflected by the curves in Figure 3.13.
The transducer power gain of the mixed-mode amplifier is plotted in Figure 3.14. As can be observed from this figure, there are two distinguishable regions of operation (the outphasing and class-B regions). In the outphasing region, the gain reduces with power back-off, whereas after switching to class-B mode the gain starts to increase again since the PA devices are coming out of saturation. Moreover the gain drop in the outphasing region due to the input power control, for mixed-mode operation, is restricted to 4dB at 8-dB OPB, instead of 8dB for

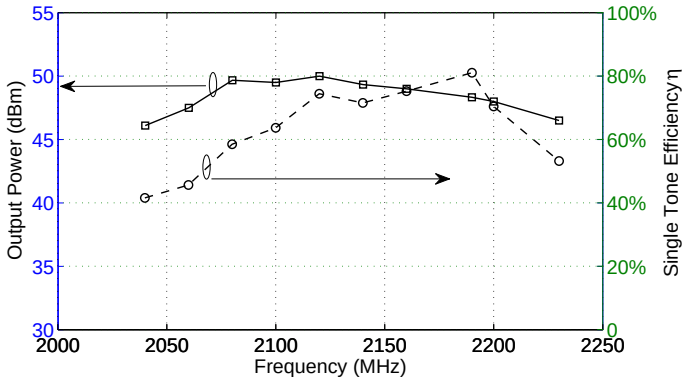


**Figure 3.15:** *Measured maximum output power and efficiency as function of frequency for the 90-W GaN outphasing amplifier*

pure-outphasing operation (3.14). We can therefore conclude from Figure 3.12 and 3.14 that driving class-B operated devices in deep compression is harmful to their gain and PAE. This conclusion does not really change when considering other saturated classes of PAs, e.g., class-E or class-F, where the inherently lower gain of these classes make input power control even more important if the output power is varied over a large range.
The RF bandwidth of the mixed-mode outphasing amplifier has also been investigated. It can be concluded from Figure 3.15 that the amplifier is capable of maintaining an output power of more than 48dBm with high efficiency ($\eta$ =60%) over a bandwidth of 140MHz, which is more than sufficient for most 3G and 4G basestations applications.

### 3.4.2 W-CDMA Characterization

Once the input power control parameters for the mixed-mode outphasing transmitter are computed, the outphasing amplifier has been tested with a W-CDMA signal with 16 dedicated physical channels (16-DPCHs). The resulting W-CDMA signal has a PAR of 9.6dB and bandwidth of 3.84MHz. Figure 3.16 shows the output of the transmitter with a W-CDMA signal with and without DPD (digital pre-distortion). Note that the pre-distortion algorithm applied, does not correct for the memory effects of the amplifier. The resulting measured average power of the pre-distorted output signal is 39.5dBm while meeting the spectral requirements of the 3G W-CDMA standard. The related average efficiency for this 9.6-dB crest factor signal is 50.5%, which is, (to the author′s best knowledge), the highest value published up to date (august 2009) for any outphasing amplifier operated with a W-CDMA signal

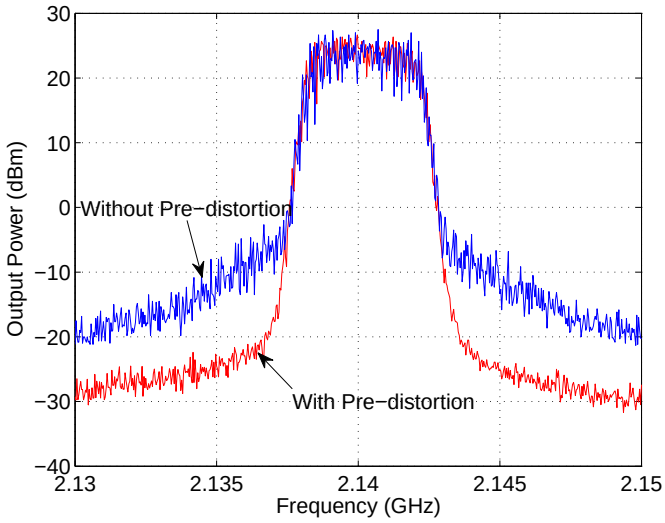


**Figure 3.16:** *Measured maximum output power as function of frequency for the 90-W GaN outphasing amplifier*

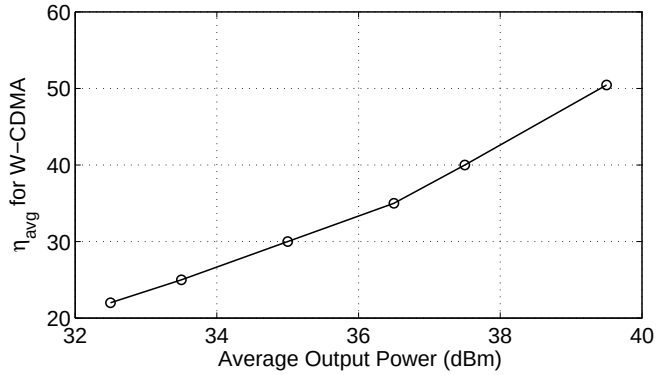


**Figure 3.17:** *Measured average efficiency for a W-CDMA 3G Signal using predistortion as function of reduced average output power*

## 3.5 Conclusions

In this chapter it has been shown that by making use of class-B operation for the deep power back-off conditions, not only the CW efficiency at those power levels can be increased but also extreme loadings conditions of the branch amplifiers (due to the outphasing) can be avoided. This results in a significant improvement in average efficiency of the amplifier when operated with W-CDMA signals. In addition, due to reduced load modulation, the impact of output losses of the branch amplifiers is also lower. These analyses indicate that even with class-B operation of the branch amplifiers, average efficiencies of W-CDMA signals in excess of 50%-60% are feasible, provided that the output losses of the active devices and power combiner can be kept low.

Although all efficiency data in this paper is given for (saturated) class-B operation (in the outphasing regime), these results can be easily renormalized to other (higher efficiency) amplifier classes, enabling even better results.

It has also been shown that the use of mixed-mode operation is effective in limiting the modulation bandwidth expansion of the input signal of the branch amplifiers. This latter fact will reduce the hardware requirements and cost of the digital predistorter. The DPD itself can be kept simple, since memory-less pre-distortion proved to be sufficient to meet the spectral requirements.

All introduced theory is verified using a 90-W peak output power GaN mixed-mode outphasing/class-B operated amplifier. The achieved 50.5% average efficiency for a 9.6-dB crest factor W-CDMA, while meeting all linearity requirements, is to the author's best knowledge, the highest ever reported up to date (August 2009). This combined with its high-efficiency bandwidth, facilitating multi-channel operation, makes the proposed amplifier concept an interesting candidate for 3G and 4G future communications systems.

Chapter 4

# Adaptive Outphasing

## 4.1 Introduction

Although the performance of the conventional outphasing transmitter can be significantly improved by the use of mixed-mode signal splitting techniques [16] (see Chapter 3), the maximum attainable average efficiency, for modulated signals like 3G W-CDMA, are however still much lower than the peak efficiency of the PA devices at their maximum output power ratings. For example, an ideal class-B PA has a peak efficiency of 78.5%, while the maximum attainable average efficiency for mixed-mode outphasing, (assuming class-B operation of the branch amplifiers), is only in the order of 60% for a 12dB PAR W-CDMA signal [16]. This number represents a kind of upper limit of what can be achieved for these transmit signals when using the proposed mixed-mode concept in combination with class-B device operation.
This chapter introduces the possibility of using tunable elements in the Chireix power combiner [17]. Amplifiers based on this principle can provide in theory an average efficiency, which is equal to the peak efficiency of the PA devices at their maximum output power conditions (e.g., 78.5% for class-B PAs).

## 4.2 Theory

The basic theory of the outphasing amplifier has already been presented in detail in Chapter 2. Therefore only the loading of the PA devices is discussed in more detail in the following text.
The conceptual block diagram of the Chireix amplifier is shown in the Figure 4.1, along-with the equivalent loading conditions of the PA devices. In this diagram, the output of the active devices is assumed to behave like a perfect voltage source,

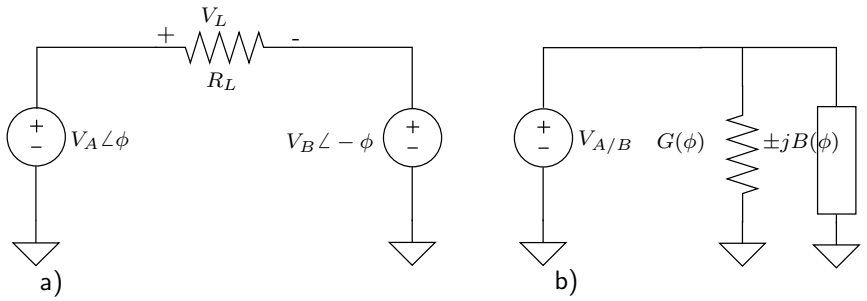


**Figure 4.1:** *a) Basic block diagram of Chireix amplifier, b) Equivalent loading of the PA devices*

something that can be approximated in practice by saturated class-B or class-F operation [47]. Moreover, the varying phase angle between these voltage sources (PA devices) results in the varying output power at the load resistor $R_L$, as well as the outphasing angle dependent load modulation at the terminals of these PA devices [6]. A simple analysis of the circuit of the Figure 4.1 yields (4.1) for the output power and (4.2) for the loading of the PA devices

$$P_{out} = \frac{0.5.V_L^2}{R_L}\sin^2(\phi). \tag{4.1}$$

Whereas $V_L$ is the RF voltage developed across the load resistor $R_L$ and $\phi$ is the outphasing angle between the voltage sources

$$Y_{A/B}(\phi) = \frac{2.sin^2(\phi)}{R_L} \pm j\frac{\sin(2\phi)}{R_L}. \tag{4.2}$$

Rewriting (4.3) in terms of the normalized output voltage $V_n$, yields,

$$Y_{A/B}(V_n) = \frac{2.V_n^2}{R_L} \pm j\frac{2.V_n.\sqrt{1-V_n^2}}{R_L}. \tag{4.3}$$

Where $V_n = \sqrt{\frac{P_{out}}{P_m}} = \sin(\phi)$. $P_m$ is the maximum output power of the amplifier. Note that the PA devices in the Chireix configuration experience opposite load susceptance which is indicated by '$\pm$" in (4.2) and (4.3). The load conductance and the susceptance of the PA devices can be normalized by $\frac{2}{R_L}$ (which is the load conductance under maximum power conditions) for the sake of generality. Note that the value of $R_L$ is chosen such that $\frac{2}{R_L}$ represents the optimum load of the PA devices. The resulting normalized conductance $G_n$ and the normalized suceptances $B_n$ are plotted in Figure 4.2, which shows that the normalized conductance initially starts at '1' and decreases to zero as the normalized output voltage is reduced to zero by changing the outphasing angle between the voltage sources. The efficiency of the Chireix amplifier is dependent on the efficiency of

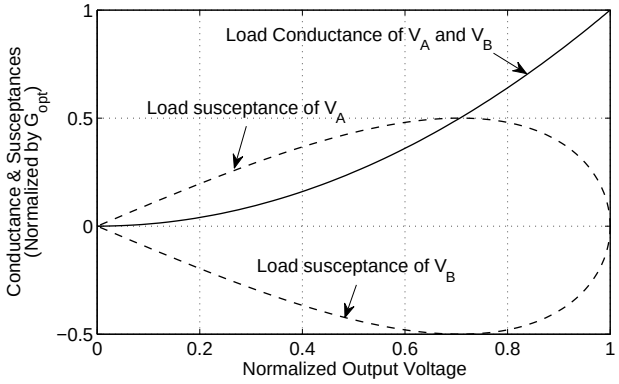


**Figure 4.2:** *Loading conditions of PA devices in an uncompensated Chireix amplifier*

the PA devices, which normally relies on the phase difference between their terminal voltages and currents, e.g., for class-B operation the efficiency of the PA devices is [7] given by (4.4)

$$\eta_B = \frac{\pi}{4}.\frac{V_{out}}{V_{dc}}.\cos(\phi). \tag{4.4}$$

whereas $\phi$ is the phase angle between terminal voltage and current of the PA devices, and $V_{out}$ is the terminal RF voltage and $V_{dc}$ is the drain/collector bias voltage.

In the conventional Chireix configuration, the terminal voltages of the PA devices are fixed and therefore their efficiencies are only a function of $\phi$, which in an uncompensated Chireix amplifier increases with decreasing output voltage, thereby lowering the related CW efficiency [31]. As discussed earlier in this thesis, Chireix proposed to add fixed reactive elements at the terminals of the PA devices in order to improve the efficiency, which tune out the reactive part of their loads at some particular outphasing angles (or at the corresponding normalized output voltages). As a result, pure ohmic conditions exist at these outphasing angles, yielding peaks in the efficiency characteristic (see Figure 4.3). The values of these compensation susceptances are given by (4.5)

$$B_{comp} = \mp j\frac{2\sin(2\phi_{comp})}{R_L}. \tag{4.5}$$

in which $\phi_{comp}$ represents the outphasing angle where the device loading conditions of the devices are purely ohmic. Note that this well known Chireix compensation with a fixed susceptance results in two pronounced efficiency peaks. This is caused due to the fact that the load susceptances for an uncompensated

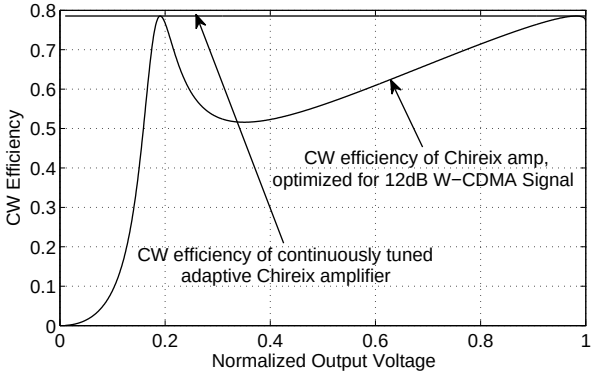


**Figure 4.3:** *CW efficiency of a conventional Chireix amplifier (optimized for a 12 dB PAR W-CDMA signal) and the CW efficiency of an adaptively-compensated adaptive Chireix amplifier*

Chireix amplifier are the function of $\sin(\phi)$, consequently compensation at $\phi_{comp}$ also results automatically in compensation at $(\frac{\pi}{2} - \phi_{comp})$ [6]. The compensation angle $\phi_{comp}$ must be chosen such that the average efficiency of the amplifier for a particular modulated signal is maximized (see (Chapter 2)).
Although the Chireix approach yields a big efficiency improvement over conventional outphasing and traditional class-B amplifiers, it also has its efficiency limitations for signals with high PAR like W-CDMA. The main reason for this degradation is that with fixed reactive elements, the load susceptances can be compensated only at two specific outphasing angles, and hence the CW efficiency of the amplifier is degraded for all other outphasing angles, resulting in a reduced average efficiency for modulated signals.

### 4.2.1 Adaptive Chireix Amplifier

In order to overcome the above mentioned limitations, in this chapter we extend the classical Chireix amplifier concept with adaptive suceptance compensation [16]. In this approach, the fixed compensation succeptances are now replaced by tunable resonators, which in principle can compensate for the undesired imaginary loading conditions that result from the outphasing action at any angle. This results in ohmic loading conditions for all outphasing angles, and consequently, the CW efficiency of the amplifier becomes flat for all outphasing angles or normalized output voltages (Figure 4.3). These improved loading conditions due to the adaptive matching are also plotted in the Figure 4.4.
The flat CW efficiency versus normalized output voltage performance of the adaptive Chireix amplifier does not only result in a higher average efficiency of the amplifier (equal to the maximum efficiency possible for the PA device), but also

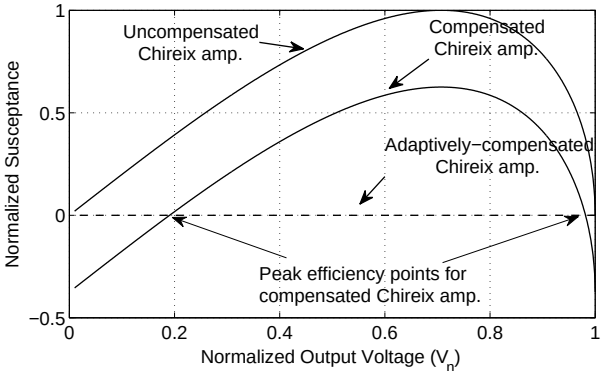


**Figure 4.4:** *Reactive loading for ; an uncompensated Chireix, a compensated Chireix (W-CDMA 12dB) and a adaptively compensated Chireix amplifier*

makes the average efficiency independent of the PAR or modulation of the input signal. This means in practice, that the same amplifier can be used for different kinds of modulated signals making multi-mode operation feasible.
So far in the discussion of the adaptive Chireix amplifier, we have assumed ideal PA devices and ideal tunable components, however, in practical situations their losses will degrade the amplifier performance and the resulting CW efficiency will decrease with the normalized output voltage. To quantify the effect of these losses on the performance of the adaptive Chireix amplifier, we present in the following section an analysis that takes into account the losses of the PA devices and the tunable matching networks.

### 4.2.2 Adaptive Chireix Amplifier Operation with Non-Ideal Devices

Figure 4.5 shows the schematics of an adaptively compensated Chireix amplifier, which contains along-with the standard Chireix power combiner and the PA devices, two tunable matching networks. The reactances of these tunable matching networks are assumed to be controlled by two voltages, which vary with the envelop of the input signal. The losses of the PA devices and the tunable matching networks can be lumped together and represented by a shunt parasitic conductance $G_{par}$ at the terminals of the PA devices as shown in the Figure 4.5. Moreover, if it is assumed that the tunable matching network compensates the imaginary part of the load reactance perfectly, and then the efficiency of the adaptive Chireix amplifier ($\eta_{adpchr}$) is given by (4.6)

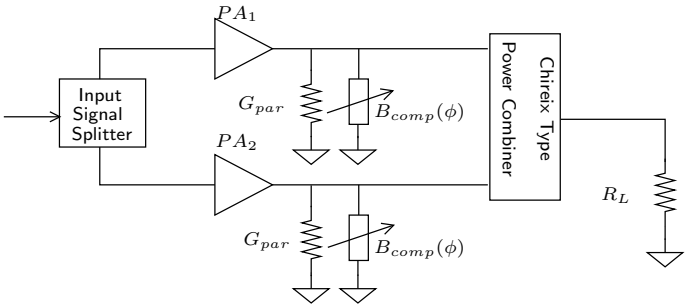


**Figure 4.5:** *Basic schematic of the adaptively tunable Chireix amplifier with losses*

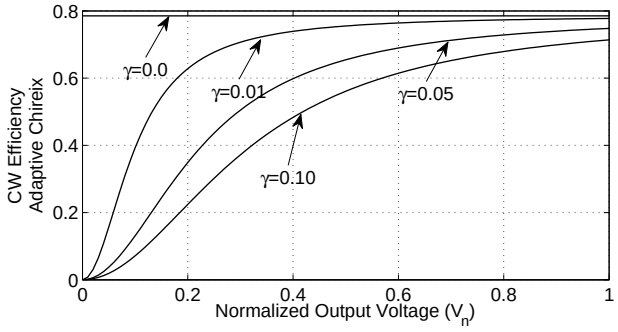


**Figure 4.6:** *CW efficiency of the adaptive Chireix amplifier for different values of the output losses*

$$\eta_{adp\_chr} = \eta_m . \frac{G(V_n)}{(G(V_n) + G_{par})}. \tag{4.6}$$

Whereas $\eta_m$ in (4.6) is the maximum efficiency of the PA devices (i.e., 78.5% for class-B operation) and $G(V_n)$ is the varying output conductance related to the Chireix operation. The efficiency of the adaptive Chireix amplifier can also be expressed as a function of the normalized output voltage ($V_n$) and the ratio of parasitic conductance and optimum load conductance $\gamma = \frac{G_{par}}{G_{opt}}$, by using (4.3) and is given by (4.7)

$$\eta_{adpchr} = \eta_m . \frac{1}{(1 + \frac{\gamma}{V_n^2})}. \tag{4.7}$$

Equation (4.7) shows that in the the efficiency of the adaptive Chireix amplifier decreases with normalized output voltage presence of losses (see Figure 4.6), resulting in degraded efficiency performance at lower power levels. Moreover, the

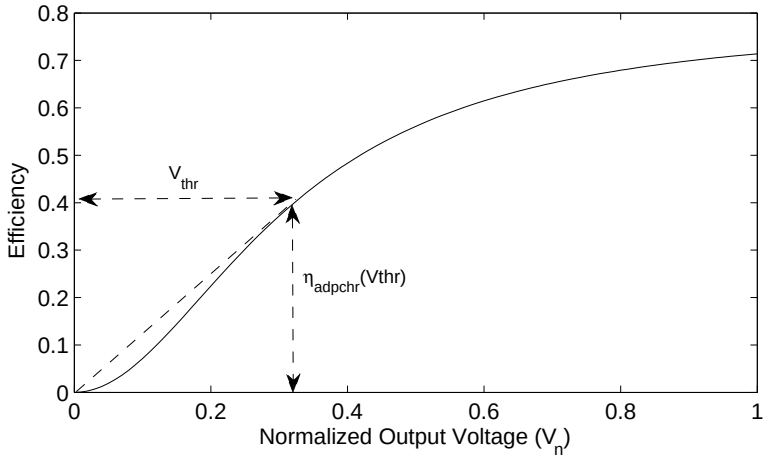


**Figure 4.7:** *CW efficiency of the adaptive Chireix amplifier with switching to class-B mode at lower power levels*

rate of drop in efficiency is not constant and is given by (4.8). It can be observed from the Fig. 4.6, that the efficiency drop is much higher at lower values of $V_n$, therefore it can be beneficial to switch to class-B mode at those power levels (by fixing the outphasing angle and the matching network reactances) in order to take advantage of relatively lower efficiency roll-off of the class-B amplifier [16]. The rate of drop of the efficiency of the adaptive Chireix amplifier can calculated by taking the derivative of (4.7) and is given by the following equation

$$\frac{\partial \eta_{adpchr}}{\partial V_n} = \frac{2\eta_m}{(1+\frac{\gamma}{V_n^2})^2 V_n^3}. \tag{4.8}$$

As the efficiency of a class-B PA drops linearly with normalized output voltage ($V_n$), the efficiency degradation with respect to $V_n$ is constant and is given by the following equation

$$\frac{\partial \eta_B}{\partial V_n} = \frac{\Delta\eta_m - 0}{1-0} = \eta_m = \frac{\pi}{4} \text{for ideal class-B.} \tag{4.9}$$

Once the adaptive Chireix amplifier is switched to class-B region, its rate of efficiency drop also becomes constant. It is equal to the efficiency of the adaptive chireix amplifier at the instant of switching ($\eta_{adpchr}(V_{thr})$) divided by the threshold voltage $V_{thr}$ as shown in the Figure 4.7, and given by the following equation,

$$\frac{\partial \eta_{adpchr}(AB)}{\partial V_n} = \frac{(\eta_{adpchr}(V_{thr}))}{(V_{thr})} = \frac{\eta_m}{V_{thr}.(1+\frac{\gamma}{V_{thr}^2})}. \tag{4.10}$$

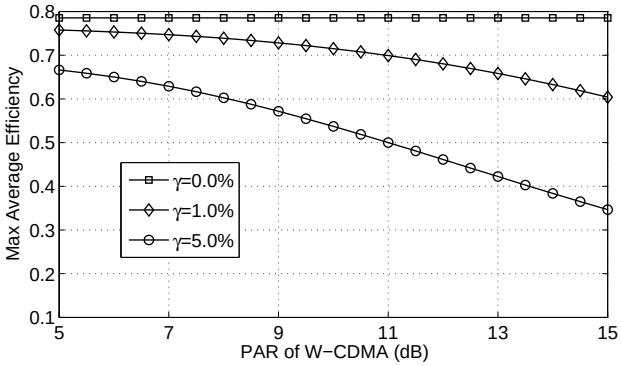


**Figure 4.8:** *Average efficiency of the adaptive Chireix transmitter versus PAR of W-CDMA signal*

The optimum threshold voltage for changing the outphasing operation into class-B operation can be found analytically by expressing (4.10) as function of $V_n$, and then equating (4.8) and solving for $V_n$, resulting in a very simple expression for optimum threshold voltage (4.11)

$$V_{thr}(opt) = \sqrt{\gamma}. \tag{4.11}$$

Finally the CW efficiency of the adaptive Chireix transmitter with class-B switching can be expressed by the following equations, and is plotted in Figure 4.7

$$\eta_{adpchr} = \begin{cases} \eta_m \frac{V_n^2}{V_n^2+\gamma} & V_n \leq V_{thr} \\ \eta_{adpchr}(V_{thr}).\frac{V_n}{V_{thr}} & V_n > V_{thr} \end{cases}. \tag{4.12}$$

Moreover, in order to study the impact of losses on the average efficiency of the adaptive Chireix amplifier, the average efficiency is now plotted versus PAR of W-CDMA signal for different values of losses in Figure 4.8. This figure shows that if the system is lossless, the average efficiency is constant for all signals and is equal to maximum efficiency possible for the PA devices. On the other hand if the losses (of the PA devices and matching networks) are taken into account, the average efficiency decreases and this degradation is more pronounced for signals with high peak to average ratios, since the losses have their biggest impact in deep power back-off operation.

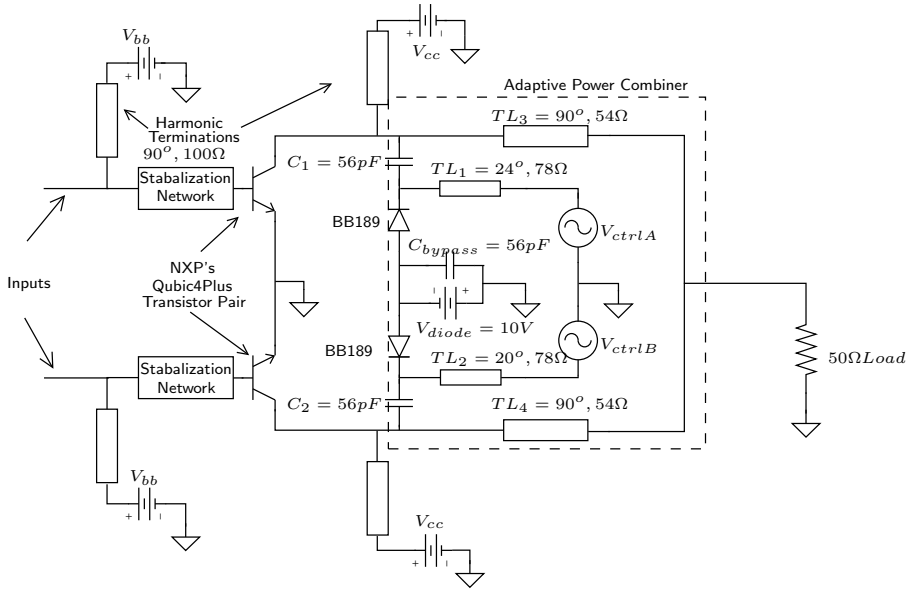


**Figure 4.9:** *Schematic of a 0.5 W adaptive Chireix amplifier*

## 4.3 Adaptive Chireix Amplifier Demonstrator

In order to experimentally verify the ideas presented in this chapter, a prototype adaptive Chireix amplifier has been implemented as a hybrid (see Figure 4.9). It is designed for IS95/WCDMA2K [48] signals, with a design frequency of 870MHz and aimed maximum output power of 27dBm.

### 4.3.1 Power Amplifier Cells

As discussed previously, the efficiency and voltage source like behavior of the PA cells is very important for the efficiency and operation of the Chireix amplifier. Therefore the amplifier cells were designed to operate in saturated class-B mode. Moreover, the amplifier cells are based on a pair of matched NXP QUBiC4P+ transistors, which provide high gain ($> 15dB$) while having a collector efficiency greater than 70%. The amplifiers cells were available as bare dice and are mounted on a PC board that contains all other circuitry for biasing, stabilization and impedance matching.

### 4.3.2 Adaptive Power Combiner

The adaptive power combiner is based on the classical transmission line type Chireix power combiner along-with the tunable resonators for adaptive compen-

sation. These tunable resonators are implemented by a parallel combination of varactor diodes (NXP BB149 varicaps) with inductive transmission lines $TL_1$ and $TL_2$ as shown in the Figure 4.9. The parallel configuration ensures predictable voltage swings on the varicap diodes, which makes it easier to avoid forward bias or breakdown conditions under all RF drive conditions. The arbitrary waveform generator used to control the voltages on the varicap has a range of -5 to +5 volts, whereas the voltage range for varicaps is from 0 to +22V. Therefore, in order to optimally use the proper tuning range of the varicaps, a biasing circuit was added to the resonators, which is formed by the capacitor $C_1$, $C_2$, $C_{bypass}$ and the bias source $V_{diode}$ in the Figure 4.9. The Chireix power combiner itself is made with two transmission lines, $TL_3$ and $TL_4$. Typically the electrical length of these transmission lines is $\frac{\lambda}{4}$ (at the design frequency), but in our design the lengths of these lines are adjusted to compensate for the bond-wire inductances, such that the total electric length from the collector terminals to the load becomes $\frac{\lambda}{4}$ at the desired frequency. This is needed to ensure that the load modulation (generated due to outphasing) is properly transferred to the collector terminals of the active devices. Moreover the characteristic impedance of the transmission lines $TL_3$ & $TL_4$ is chosen in such a way that the 50Ω load transfers to the optimum load of the PA devices. This impedance is given by (4.13), whereas $R_L$ is load of the amplifier (usually 50Ω) and $R_{opt}$ is the optimum loading of the PA devices

$$Z_2 = \sqrt{2R_L R_{opt}}. \tag{4.13}$$

Note that due to the power-combiner design, maximum output power for the amplifier occurs now at zero degree out-phasing angle, while minimum output power occurs at $90^o$ outphasing angle. The proposed network is simple but effective, however, its losses may restrict the average efficiency enhancements which can be achieved using this prototype.

### 4.3.3 Measurement Setup

To experimentally verify the Chireix amplifier with adaptive power combiner, two phase and amplitude controlled input signals along with the modulated bias signals for the varactor diodes are needed. To obtain these signals, we constructed the test setup of Figure 4.10. In this setup, the required RF signals are generated using a four channel arbitrary waveform generator (AWG) and two IQ modulators. The resulting RF signals are pre-amplified in order to obtain sufficient input power for the out-phasing transmitter. An additional high-voltage arbitrary waveform generator is used to generate the control voltages for the varactor diodes. The power and resulting spectrum are monitored by a spectrum analyzer. Moreover, in order to analyze and correct the output modulated signal, the output of the amplifier is also coupled to an IQ de-modulator. The outputs of the IQ demodulator are sampled through high-data rate analog-to-digital converters. Note that this setup, due to the synchronization of the AWGs and coherent up-

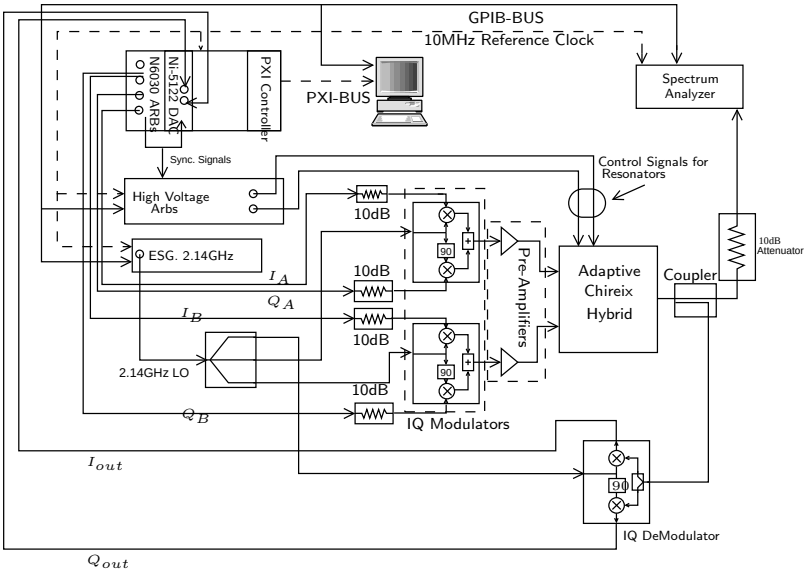


**Figure 4.10:** *Measurement setup for adaptive Chireix amplifier*

conversion, can not only perform static testing, but also facilitates dynamic modulation of the adaptive power combiner with the envelope of a complex modulated signal. Moreover, since the IQ modulators (for up-conversion) and IQ demodulator (for down-conversion) share the same clock, absolute measurements of the output phase are possible. This ia a feature that helps us in selecting the correct diode control voltages for adaptive matching network.

### 4.3.4 Single-Tone Measurements

The main aim of this amplifier is to amplify complex modulated signals like CMDA2K or IS95 signals. However, in order to construct the correct input signals, it is also important to pre-characterize the amplifier to find the optimum values of the diode voltages for the matching network, as well as the optimum threshold outphasing angle $\phi_{thr}$ beyond which class-B operation is used.
For this purpose, the input power, outphasing angles and the diode voltages are varied and the output power, output phase, and the related efficiency are measured. Using this data, the varactor voltages are selected which result in the highest efficiency for each output power level along-with the lowest phase distortion. The resulting CW efficiency performance for different fixed outphasing angles is shown in the Figure 4.11.

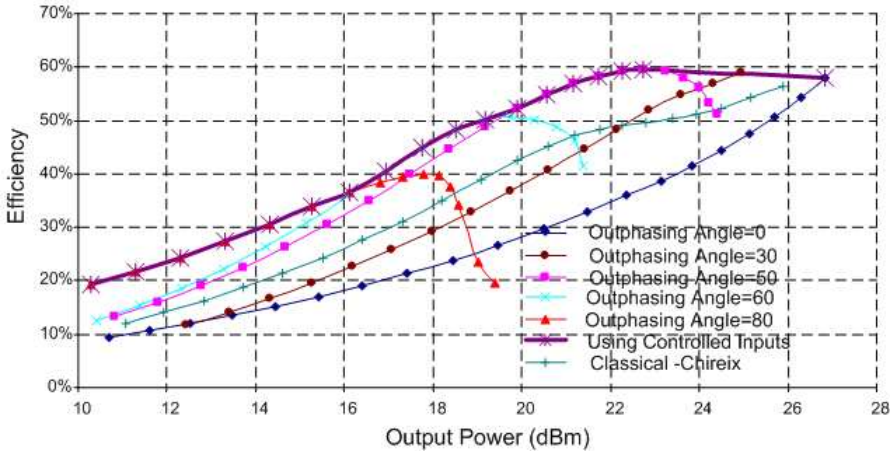


**Figure 4.11:** *Single-tone measurement results for adaptive Chireix amplifier*

### 4.3.5 CDMA2K Measurements

Once the optimum varactor voltages and threshold outphasing angle are known, a lookup table is constructed. The IQ signals for the input of amplifier and the related control signals for the matching network are determined using this table. The measured results for the CDMA2K signal are shown in Figure 4.12. The PAR of this signal is 7dB, the maximum average output power is 20dBm and the corresponding average efficiency is 49.5%.

## 4.4 Conclusions

The previous chapters (Chapter 2 and Chapter 3) showed that there exist a maximum for the average efficiency which can be obtained using the outphasing concept, and that maximum is always below the peak efficiency provided by the PA devices. In this chapter we show that this maximum can be increased if the outphasing concept is combined with an adaptive power combining network. This basically results in an adaptive load modulation amplifier. However, the combination with outphasing provides us with an extra degree of freedom, which helps to keep the adaptive network simple and low-loss. A 0.5 Watt adaptive Chireix amplifier has been realized to verify the proposed concepts of this chapter. This demonstrator shows a fairly flat efficiency performance over 10dB output power back-off range and provides close to 50% efficiency for IS95 signals.

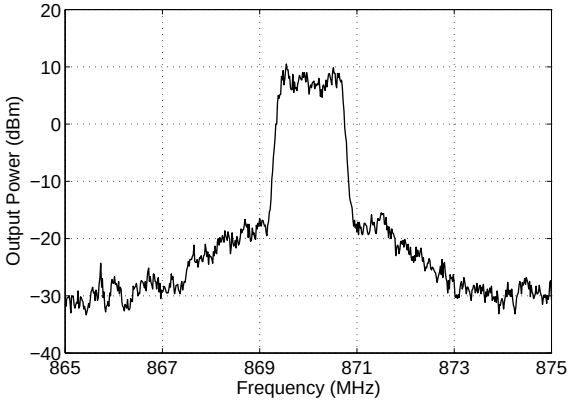


**Figure 4.12:** *Measured CDMA2K Signals, PAR=7dB,* $P_{avg} = 20dBm$*, Efficiency=49.5%*

Chapter 5

# Wide-Band Doherty PA

## 5.1 Introduction

Currently the Doherty power amplifier (DPA) [9] represents the most commonly used high efficiency concept in base station applications. Its popularity results from its high efficiency performance achieved at a low hardware complexity and cost level [12][49]. However, a well known disadvantage of the DPA, is its narrow bandwidth (typically $\leq$10%) [13][50], which complicates its application in multi-band/multi-standard communication systems. Consequently, custom DPA solutions for each individual need in the market have to be developed, raising costs and yielding logistic problems.
To address this limitation, we investigate how the DPA bandwidth for high efficiency operation can be expanded. This chapter is organized as follows; after providing a brief introduction to the Doherty power amplifier, we first discuss the DPA bandwidth restrictions in section 5.2.1. In section 5.3 we evaluate various matching topologies (mainly addressing the wideband compensation of the output capacitance of these devices), connection schemes and Doherty power-combiners that extend the DPA bandwidth. The actual circuit realizations are given in section 5.4, followed by experimental verification in section 5.6. Later in this chapter (section 5.7), improved Doherty power combiners are presented along-with circuit realizations.

## 5.2 Theory of Doherty Power Amplifiers

Doherty power amplifier operation is a well established technique to increase the average efficiency of microwave amplifiers [6]. In this technique the RF amplification is accomplished by using multiple branch amplifiers in parallel. Through smart power combining of the outputs of these branch amplifiers, active load

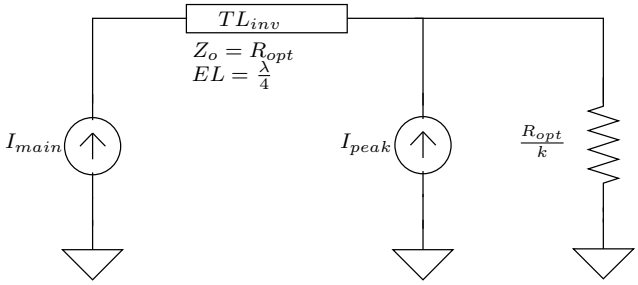


**Figure 5.1:** *Schematic illustrating the basic principle of a two-way DPA.*

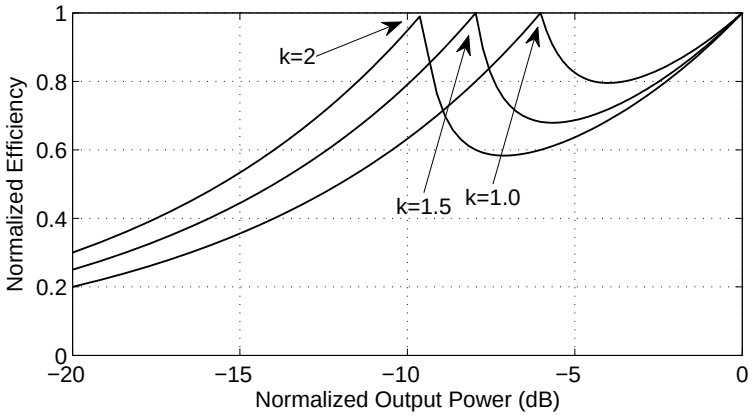


**Figure 5.2:** *Theoretical efficiency characteristics of two-way DPA. The various curves show the performance of two-way DPA for different values of 'k'.*

modulation occurs, which helps to improve the average efficiency of the overall DPA amplifier. Currently, there exist various Doherty power amplifier implementations, e.g., the symmetrical two-way DPA [51], the asymmetrical two-way DPA [49] and the three-way DPA [13]. However in the following sections only the bandwidth performance of the two-way DPA is discussed in detail for reasons of simplicity. The results obtained from this analysis can be easily extended to cover other more complex DPA architectures.

The diagram of a two-way Doherty power amplifier (DPA) in its most elementary form is given in Figure 5.1. Here the main and peak devices are represented by current sources connected by a transmission line impedance inverter, which has an electrical length of $\frac{\lambda}{4}$ at the center frequency of the design. In the DPA, the main device is active at all output power levels, while the peaking device operates only at the peak power levels [6]. Moreover the characteristic impedance of the transmission line $TL_{inv}$ is chosen in such a way that load of the main device (when operating alone) is '$x$'times its optimum load for providing maximum power (i.e., $xR_{opt}$ ). This increased loading results in a higher RF voltage swing at the drain terminal of the main device, and consequently higher efficiency of this device [6]. The RF voltage swing and the efficiency of the main device achieve their maximum value when the output current of the main device reaches ($\frac{1}{x}$) times the current $I_{m,max}$ at full power.

When the RF voltage reaches its maximum (e.g., twice the supply voltages when operated in class-B) the main device gets saturated. As a result, the voltage swing can no longer be increased. Therefore in order to increase the output power, the load of the main device needs to be decreased. This is accomplished by activating the peaking device at the point where the main amplifier reaches its saturation voltage. When the peaking amplifier starts to inject current into the load $R_L$, the effective load of the impedance inverter ($TL_{inv}$) will increase. Consequently, the main device will experience a decreasing load at its drain terminal due to the impedance inversion. As a result, the main device will come out of saturation and will increase its output power by injecting more current into the load. In this way, at these higher power levels, the currents of the main and peaking device(s) are varied such that the main device always remains at the edge of saturation and hence operates at maximum efficiency. When reaching full power the peaking device is injecting ($k = x - 1$) times more power than the main device, while both devices experience their optimum load for output power and maximum efficiency. Due to this previously described operation, the efficiency characteristics of the two-way DPA exhibits two distinct efficiency peaks. Namely, one at full power where both main and peaking devices are operating together, and other one at the back-off power level where the main device is operating alone and reaches its voltage saturation.

The difference between a symmetrical and asymmetrical DPA lies in the ratio of the maximum output power of the peaking amplifier with respect to that of the main amplifier ($k = \frac{P_{peak,max}}{P_{main,max}}$) [12]. This ratio also defines the location of second

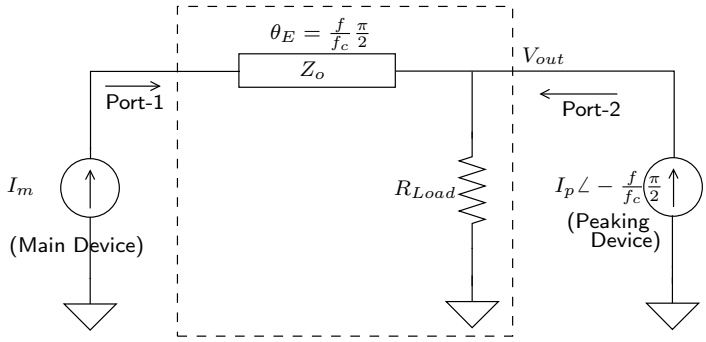


**Figure 5.3:** *Basic schematic of the Doherty power amplifiers used in the bandwidth analysis.*

efficiency peak in the efficiency characteristics of the DPA. In a symmetric DPA the value of $'k'$ is equal to 1, which results in equally sized main and peaking devices and a location of 6dB power back-off level for the second efficiency peak. Whereas, for asymmetric DPA the value of $'k'$ can be chosen higher, e.g. equal to 2. Note that this particular choice would result in a peaking device which is two times bigger than the main device and a 9.6dB power back-off location for the second efficiency peak. The efficiency characteristics of a symmetric and asymmetric two-way DPA are shown in Figure 5.2. In broader sense, the choice of $'k'$ will depend on the characteristics of the signal to be amplified and its value can be optimized in the same way as we have discussed previously in chapter 2. However, in practical situations the most commonly used values of k are 1.0 and 2.0 [49].

### 5.2.1 Bandwidth of the DPA with Ideal Devices

As discussed in the previous section, the operation of the DPA depends on the inversion properties of the impedance inverter transmission line $TL_{inv}$ which, besides being vital for the operation of the DPA, is also the only frequency dependent component in this elementary DPA schematic (Figure 5.1), when implemented using ideal current source like PA devices. Optimum wideband operation of the DPA would require the impedance inverter transmission line to be a perfect impedance inverter over the whole desired frequency band. Without changing the physical properties of the TL, this is not possible [52]. The electrical length of the TL increases linearly with frequency; hence, the TL forming the inverter will impose bandwidth restrictions on the DPA concept. In view of this, the phase relations versus frequency of the input signals, which control the main and peak device current sources, should track perfectly the phase delay provided by the TL impedance inverter at each frequency [16]. In practical situations, the output capacitance of the PA devices proves to play a very decisive role in defining the

maximum bandwidth of the DPA in addition to the impedance inverter, something that we will include later in our analysis.
To evaluate the frequency dependent efficiency behavior of the DPA, we use the simplified schematic of the 2-way DPA with the assumption that the PA devices can be represented by ideal current sources with zero output capacitance. Moreover, the terminal voltages of PA devices (which are vital for efficiency) can be calculated easily if the network enclosed by the dotted rectangle in the Figure 5.3 is represented by the impedance matrix (Z-matrix) [52],

$$\begin{bmatrix} \frac{Z_o(R_L\cos(f_n\frac{\pi}{2})+jZ_o\sin(f_n\frac{\pi}{2})}{Z_o\cos(f_n\frac{\pi}{2})+jR_L\sin(f_n\frac{\pi}{2})} & \frac{Z_oR_L}{Z_o\cos(f_n\frac{\pi}{2})+jR_L\sin(f_n\frac{\pi}{2})} \\ \frac{Z_oR_L}{Z_o\cos(f_n\frac{\pi}{2})+jR_L\sin(f_n\frac{\pi}{2})} & \frac{Z_oR_L\cos(f_n\frac{\pi}{2})}{Z_o\cos(f_n\frac{\pi}{2})+jR_L\sin(f_n\frac{\pi}{2})} \end{bmatrix}. \tag{5.1}$$

Note that in (5.1), $f_n$ is the normalized frequency with respect to the center frequency of the design ($f_n = \frac{f}{f_c}$), $Z_o$ is the characteristic impedance of the TL impedance inverter and $R_L$ is the load impedance. The terminal voltages of the main ($V_m$) and peaking amplifier ($V_p$) are given by

$$V_m = Z_{11}I_m + Z_{12}I_p, \tag{5.2}$$

$$V_{out} = V_p = Z_{21}I_m + Z_{22}I_p. \tag{5.3}$$

$I_m$ and $I_p$ in (5.2) and (5.3) represents the currents of the main and peaking device. Once the terminal voltages are known (by using 5.1 to 5.3), the output power ($P_{out}$) and the efficiency ($\eta_{dpa}$) of the total DPA, (assuming class-B operation for the active devices) can be calculated as,

$$\eta_{dpa} = \frac{P_{out}}{P_{dc}} \rightarrow \frac{\pi}{4}\frac{Re(V_mI_m^*) + Re(V_pI_p^*)}{|V_{m(max)}||I_m| + |V_{p(max)}||I_p|}. \tag{5.4}$$

Note that class-B operation is assumed in (5.4). The resulting efficiency curves are given in the Figure 5.4 for the symmetrical two-way Doherty case.

Note that for ideal devices, that act like perfect current sources, the CW efficiency versus frequency at 6dB power back-off (see Figure 5.4) indicates that Doherty operation in its most elementary implementation allows an efficiency bandwidth of 28% (e.g., bandwidth where the efficiency is within 10% of its maximum value), while at full power there seems to be no bandwidth restriction. Note that bandwidth remains the same for deeper back-off power levels ($\geq 6dB$ for a symmetric two-way DPA) because the main amplifier operates alone, and the loading conditions are identical to the situation at 6dB power back-off.
The above set of equations (5.1) to (5.4) can also be applied to the asymmetrical Doherty case ($k \geq 1$). The resulting CW efficiency response versus frequency is shown in Figure 5.4. As expected, the asymmetrical DPA, due to its higher load modulation, shows a more narrow bandwidth behavior than the symmetrical DPA. Moreover, in the asymmetrical Doherty the bandwidth reduces with

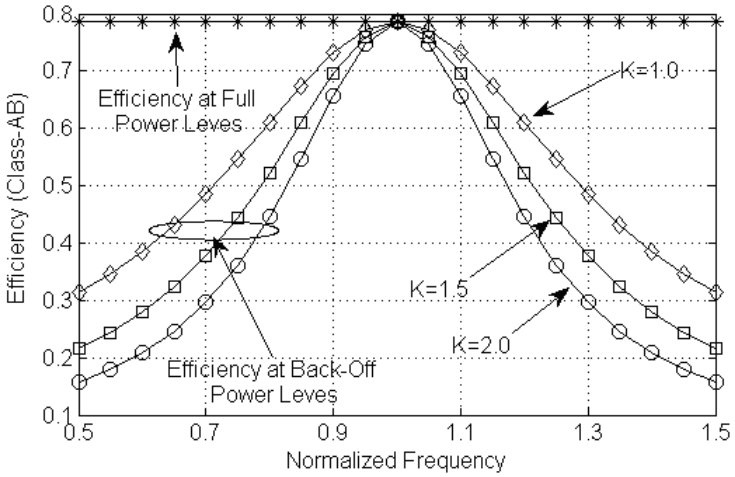


**Figure 5.4:** *CW efficiency characteristics of generic two-way DPA with different values of the asymmetry factor k.*

increasing '$k$'.
Although relatively straight forward to analyze, these results are quite surprising, since conventional DPA implementations show only narrow-band operation, typically resulting in an efficiency bandwidth of only 5% to 10%. This fact indicates that in conventional designs the TL impedance inverter is not the only bandwidth limiting component.
In view of this, attention also needs to be given to the bandwidth constraints imposed by other frequency dependent components in practical DPA implementations (e.g., the output capacitance of the PA devices). Doing so can direct us to new design methods that facilitate higher bandwidths for practical DPA designs.

### 5.2.2 DPA Bandwidth for Devices with Output Capacitance

To make our efficiency bandwidth analysis more realistic, the analysis is now extended by including the non-zero output capacitance of the active devices. Since practical PA devices have both output and input capacitance [6], their inherent bandwidth limitations (for a particular reflection coefficient $\Gamma_m$) due to input and output matching is given by the (5.5) for a parallel RC circuits [53][54]

$$\Delta\omega \ln(\frac{1}{\Gamma_m}) < \frac{\pi}{R_{opt}C_{dev}}, \tag{5.5}$$

whereas $\Gamma_m$ is the reflection coefficient, $R_{opt}$ is the output load which is usually equal to the optimum load of the PA device for maximum performance, and $C_{dev}$ is the output capacitance of the PA devices.

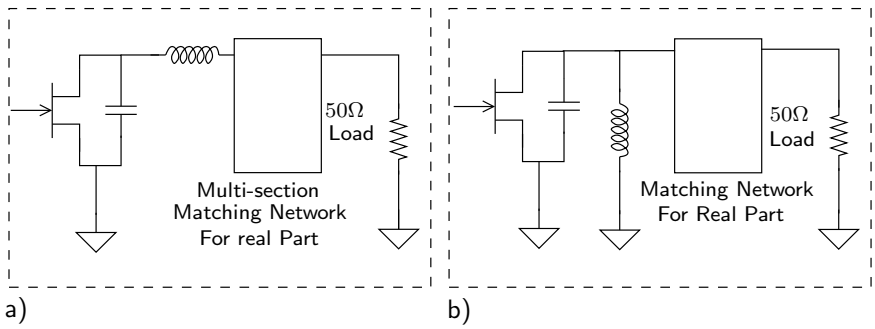


**Figure 5.5:** *a) Conventional wideband matching b) matching topology typically applied in load modulated PA's.*

However, this maximum bandwidth can only be achieved if the PA devices are matched using wideband impedance matching techniques, which is traditionally done by matching the output of the PA device as a (complex) impedance [54]. In such an approach, the reactance is first tuned out by a series inductor, after which the remaining real part is matched by a multi-section wideband matching network (Figure 5.5).
Doherty operation, however, requires load modulation [9]; therefore, it is more practical for DPA applications to match the PA devices as an admittance such that the load modulation can be applied directly at the output terminal of the PA devices [6]. This is usually done by first tuning out the output capacitance by a parallel inductor, and then providing the matching for the real part of the output admittance [12] (Figure 5.5). With this topology, the matching of the reactive part forms a parallel resonator at the output of the PA device, which by itself will have a band pass characteristic and therefore not only limit the bandwidth of the PA devices, but also of the total DPA. The related efficiency degradation of the PA devices as function of $C_{dev}$ and $R_{opt}$ can be represented as,

$$\eta_{degrad} = \cos(\tan^{-1}(2\pi C_{dev} R_{opt}(1 - f_n^2), \tag{5.6}$$

when deviating from the center frequency of the design.

The resulting efficiency given by (5.6) proves to be related to the output capacitance and optimum loading of the PA device which is characteristic for a given technology.
The effect of this efficiency degradation due to the parallel resonator can also be easily incorporated in (5.1) to (5.4). Moreover the CW efficiency-frequency characteristics of the DPA with devices having non-zero output capacitance are calculated for NXP's LDMOS Gen7 [49] devices and Cree Inc. GaN devices [38], and are plotted in Figure 5.6. The curves in Figure 5.6 show now the same narrow band behavior which is usually observed in practical implementations of DPAs.

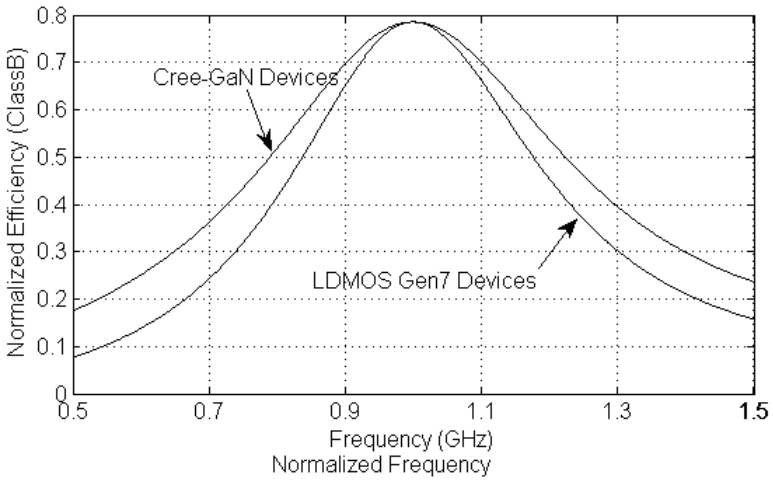


**Figure 5.6:** *CW efficiency versus relative bandwidth of a symmetric two-way DPA at 6dB output power back-off level for two different FET technologies.*

Note that the output capacitance of the GaN devices from Cree is almost half the capacitance of the LDMOS devices for a comparable output power level. This reduced output capacitance results in much better bandwidth characteristics of the individual devices (see equation (5.6)) thus, enabling the design of very wideband amplifiers with this technology. However, in DPA like configurations this reduced capacitance improves the bandwidth by only a few percent. Therefore, if conventional matching techniques (compensation with parallel inductors) are applied in DPA configuration, the bandwidth cannot be dramatically improved by optimizing the device technology.
It can be concluded from this section that the main cause of the narrow bandwidth of the DPA is the output capacitance of the PA devices and not the commonly blamed output power combiner. Therefore, the first step to improve the bandwidth of the DPA is to compensate the output capacitance of the PA devices in a wideband fashion in order to eliminate the parallel resonating structure at the output of the PA devices [14]. This topic will be discussed in the next section.

## 5.3 Output Capacitance Compensation for Wideband Operation

One attractive technique to compensate the output capacitance of active devices is to absorb the output capacitance along-with the connecting bond-wires in the impedance inverter [14]. Doing so, the efficiency versus frequency behavior improves, since in this situation we are only limited by the bandwidth of the quasi-lumped transmission line, rather than by the bandwidth of the parallel resonator

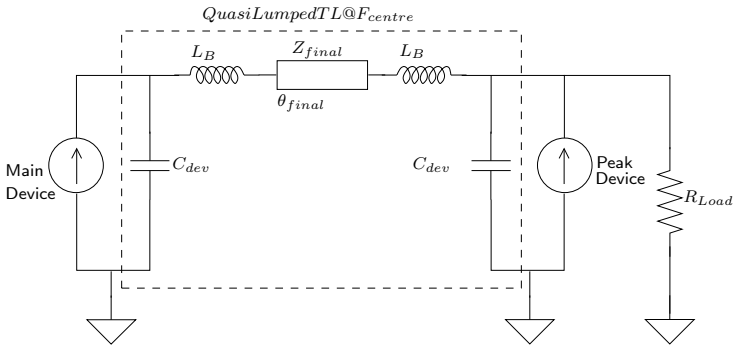


**Figure 5.7:** *Simplified schematic of a DPA which absorbs the output capacitance of the main and peak device, as well their connecting bond-wires into the quasi lumped transmission line impedance inverter.*

at the output of the active device. Figure 5.7 shows the related DPA schematic, which now also includes the output capacitances and connecting bond-wires of the active devices. Note that the transmission line along with bond-wires and output capacitance of the PA devices, indeed results in a quasi-lumped TL. Consequently, if the length and characteristic impedance of this artificial TL are adjusted in the proper way, it will act as an impedance inverter at the design frequency.
In order to evaluate the usability and limitation of the proposed concept, an analysis of this quasi lumped transmission line is performed. For this purpose we first neglect the bond-wire inductances in the initial analysis for sake of simplicity. Doing so, (5.7) and (5.8) give the electrical length and characteristic impedance of the required connecting transmission line needed to absorb the output capacitance of the PA devices in the quasi-lumped inverter

$$\theta_T = \cos^{-1}(\omega C_{dev} Z_o), \tag{5.7}$$

$$Z_T = \frac{Z_o}{\sin(\theta_T)}. \tag{5.8}$$

$Z_o$ is the characteristic impedance of the original full $\frac{\lambda}{4}$ impedance inverter, while $\theta_T$ and $Z_T$ are the calculated electrical length and characteristic impedance of the TL, which forms the inverter along-with the output capacitances of the PA devices. Equation (5.8) also imposes a restriction on the maximum capacitance value that can be absorbed in the quasi-lumped transmission line, which for a particular frequency ($\omega$) is given by,

$$C_{dev} < \frac{1}{\omega . Z_o} \tag{5.9}$$

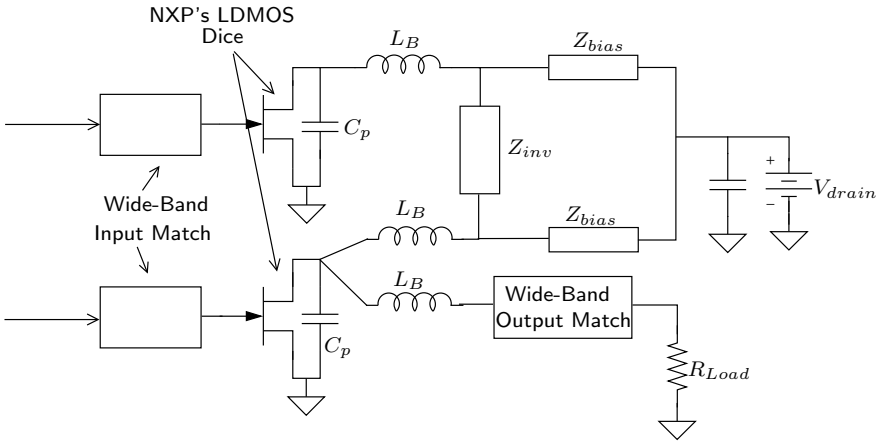


**Figure 5.8:** *Simplified block diagram of the 20-W NXP Gen6 wideband DPA demonstrator.*

which in turns sets a limit on the maximum design frequency of wide-band DPA using this method,

$$\omega_{max} = \frac{1}{Z_o.C_{dev}}. \tag{5.10}$$

As discussed before, $Z_o$ is normally taken equal to the optimum load of the active devices ($R_{opt}$) for delivering maximum power [6]. Therefore, when assuming linear power scaling, the product of $Z_o$ and $C_{dev}$ is fixed for a particular technology, and cannot be chosen independently. Consequently, (5.10) limits the maximum design frequency which can be selected for this particular DPA design technique with a given device technology.
Once the length and the characteristic impedance of this TL are known, then (5.11) and (5.12) can be used to refine the length and characteristic impedance of the TL by including the effect of the bond-wire inductances,

$$\theta_F = \tan^{-1}(\frac{Z_T}{\omega L_B}), \tag{5.11}$$

$$Z_F = Z_T \frac{\sin(\theta_T)}{\sin(\theta_F)}. \tag{5.12}$$

In which $L_B$ is the bond-wire inductance, while $\theta_F$ and $Z_F$ are the required electric length and the characteristic impedance of the final transmission line implementation needed to absorb the output capacitances of the active devices and their connecting bond-wires.

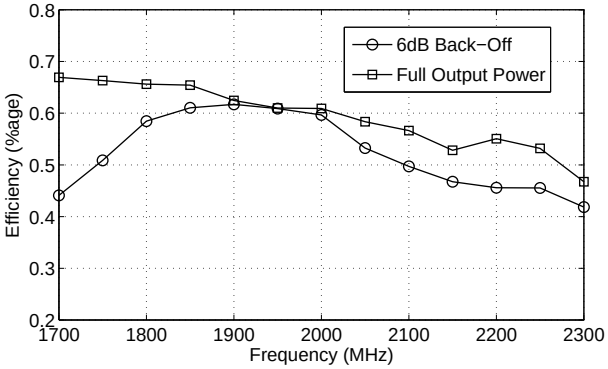


**Figure 5.9:** *Simulated efficiency vs. frequency at full output power and at 6dB power back-off of the 20W wideband Doherty power amplifier.*

## 5.4 Circuit Realization

A 20-W wideband DPA was designed to evaluate the forgoing theory. Two bare dice of 10-W NXP Gen 6 LDMOS devices were used for the branch amplifiers operating in class-B mode. The design center frequency is set to 1.95 GHz, in order to avoid the frequency limit imposed by (5.10). The required length and the impedance of the final transmission line were calculated using (5.7), (5.8), (5.11) and (5.12). The complete circuit diagram of the DPA along-with the biasing lines and harmonic terminations is shown in the Figure 5.8.
In this implementation the connection of the peaking amplifier to the load is very important, since the impedance inversion path of the main to peak amplifier should not be partially shared by the DPA connection to the external load. For this reason the output of the peaking device is directly bonded to the load in our design, along with bonding it directly to the quasi-lumped TL (Figure 5.8). The remaining tasks in the circuit design of the DPA are: the wideband output match to the 50Ω load, and the wideband input match of the PA devices. In our design it has been chosen to have two individual inputs for the DPA in order to allow independent control of the phase relations of the main and peak device to maximize its wideband performance.

## 5.5 Simulation Results

The circuit has been designed using Agilent Advanced System Design (ADS). Figure 5.9 shows the simulation results at maximum output power and at 6 dB power back-off operation. As expected, the DPA has its highest bandwidth at full power while still providing an excellent bandwidth ($\geq 300MHz$) at 6dB power

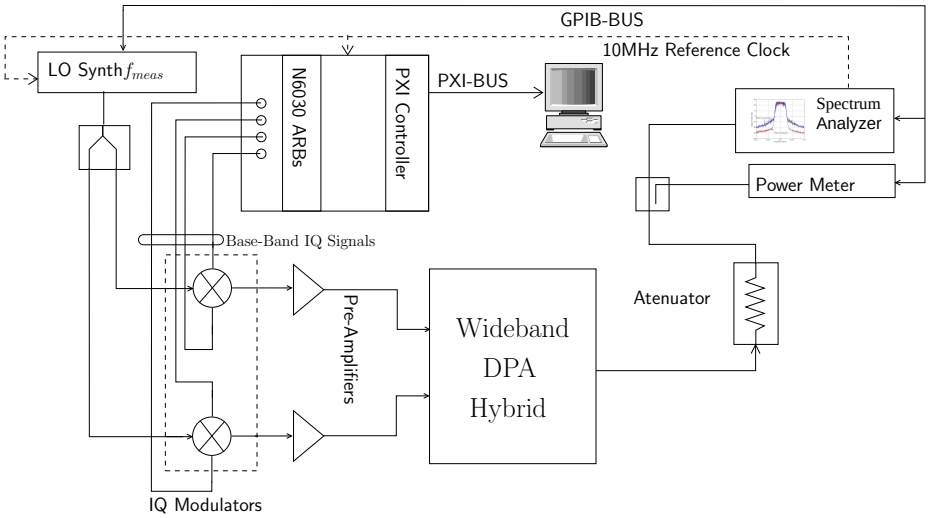


**Figure 5.10:** *Block diagram of the measurement setup used to characterize the wideband DPA.*

back-off. The slow efficiency roll-off at full power is due to frequency behavior of the quasi-lumped transmission, which yields a slightly reactive loading to the PA devices for frequencies higher than the center frequency.

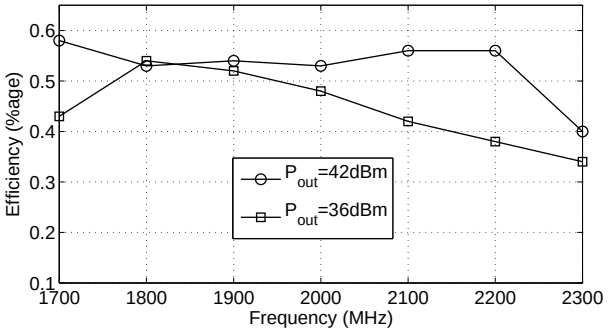


**Figure 5.11:** *Measured efficiency at peak output power and 6dB power back-off versus frequency of the 20W wideband Doherty power amplifier demonstrator.*

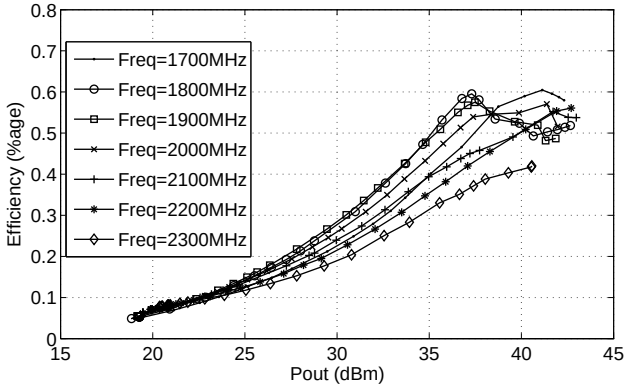


**Figure 5.12:** *Measured efficiency Vs. output power for the wideband Doherty at different frequencies.*

## 5.6 Measurements

Since the goal of this work is to evaluate the wideband DPA performance set by the improved output power combining network, a mixed-signal characterization setup was used to characterize the DPA demonstrator (Figure 5.10). It provides precise control of phase relations of the input signals, such that the output phases of the main and peak device track perfectly with the quasi-lumped impedance inverter [14]. Also the input signal amplitudes have be optimized for maximum performance. The efficiency measurements are performed from 1.7 GHz to 2.3 GHz, and their results are shown in Figure 5.11 and 5.12. The related gain of the DPA was 13 dB.

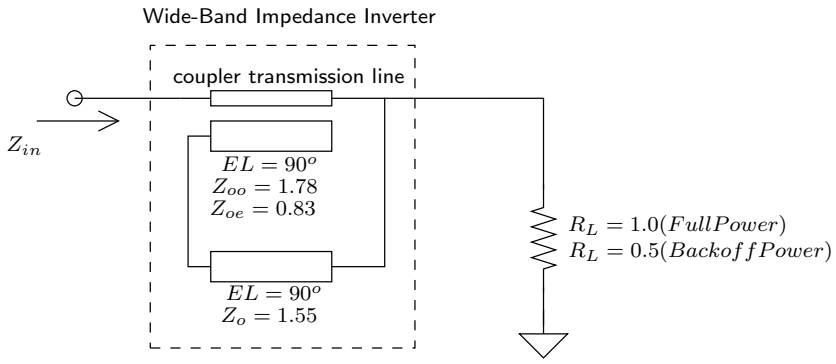


**Figure 5.13:** *Coupled-line based wideband impedance transformer.*

## 5.7 Bandwidth Improved DPA Power Combiners

In the previous section it is shown that, once the output capacitances of the PA devices are compensated by absorbing them into the output power combiner network, the bandwidth of the DPA can be significantly improved. This section shows that if a wideband impedance inverter [14][55][15] is used along-with the previously proposed output capacitance compensation, the bandwidth of the DPA can be further increased by another 17%.
A number of wideband impedance inverters exist in literature [56][57][58], which are mainly designed with coupled line structures. One of these structures, which is well suited for DPA applications, is proposed by Jordon Sveshtarov[59]. This configuration is based on a combination of a coupled line section (CLS) with a single transmission line (TL), as illustrated in Figure 5.13. This structure has wideband impedance inversion properties that can be utilized to improve the bandwidth of the DPA [15]
In order to investigate this opportunity, the magnitude and phase of the input impedance of this structure versus frequency at the 6dB power back-off point are plotted in Figure 5.14. Note that $R_L$ is set to be $0.5\Omega$ while the wideband impedance inverter parameters are chosen in such a way that it provides a wideband input impedance of $2\Omega$. In this way, this configuration mimics the classical two-way DPA situation with a 6 dB back-off high efficiency point.

From Figure 5.14 it can be noted that this wideband impedance inverter indeed provides an impedance inversion over much larger bandwidth than a quarter-wave transmission line. In addition to that, the phase variation of the input impedance is lower than that of the quarter-wave transmission line. Therefore, application of this inverter in a DPA should result in much larger bandwidths at the back-off power level. The analytical analysis of the actual bandwidth performance of this novel impedance inverter when applied in a DPA configuration at various power levels is quite tedious and results in very complex equations. Therefore, the band-

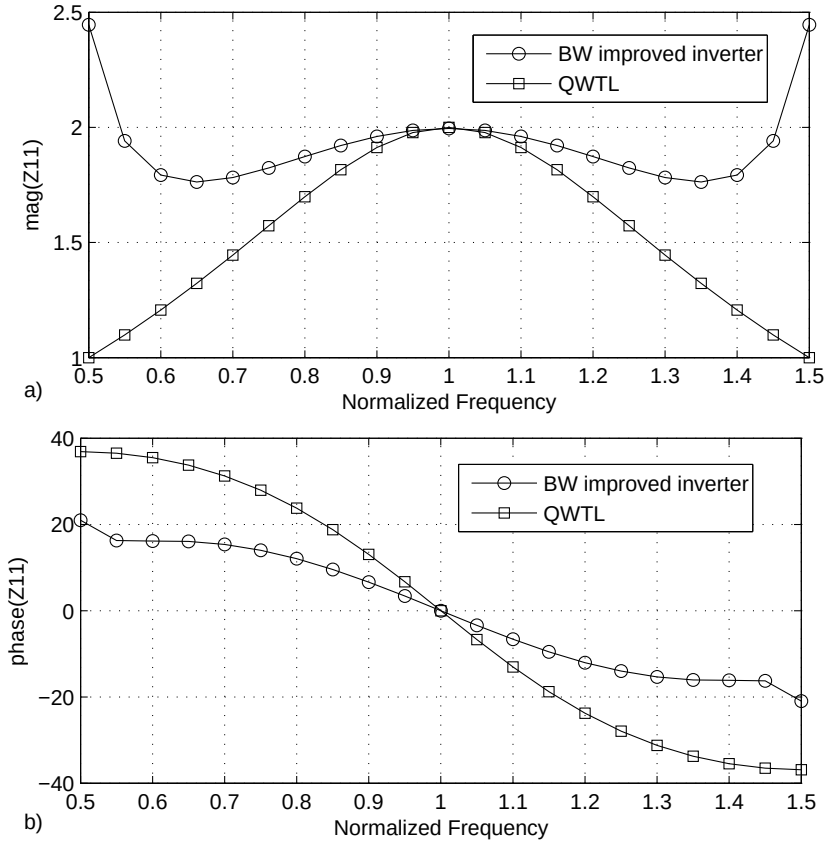


**Figure 5.14:** *a) Magnitude of the normalized input impedance of the coupled-line wideband inverter and QWTL. b) Phase of the input impedance of the coupled-line wideband inverter and QWTL. Note that the load impedance is chosen to be equal to normalized value of 0.5Ω which mimics the 6dB power back-off situation in a symmetrical two-way DPA.*

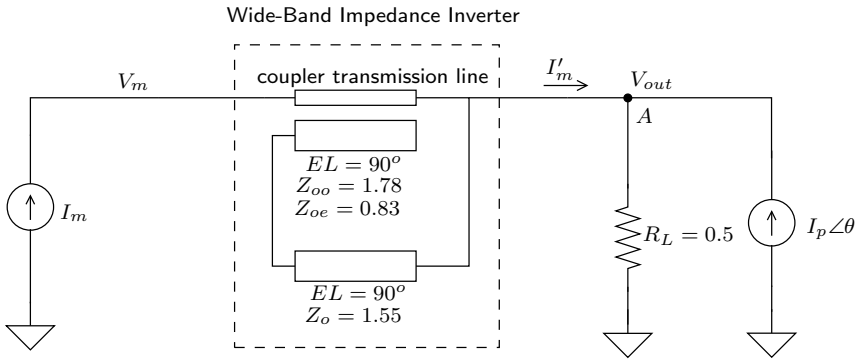


**Figure 5.15:** *Schematics of a 2-Way symmetrical DPA with bandwidth improved impedance inverter.*

width analysis is performed using ADS with the simplified schematics of a 2-way symmetrical DPA of Figure 5.15. At the back-off power level (6dB PBO), the current of the peaking device is assumed to be equal to zero, and at full power level the phase and magnitude of $I_p$ are assumed to track perfectly to the phase and amplitude of $I'_m$ so that the active load modulations at the node 'A' results in a real impedance only. The resulting terminal voltage of the main and the peaking devices are plotted in Figure 5.16 and Figure 5.17. Note that the terminal voltages of the main and the peaking device get higher than '1'because the input impedance of the currents sources gets higher than the nominal values of '2'(at 6 dB PBO) and '1'(at full power level). However, real PA devices (operating in class-B mode) show RF voltage saturation behavior once the RF voltage exceeds DC bias voltage. Therefore, while calculating the efficiency of the PA devices, (using Figure 5.15), it is assumed that the terminal voltages do not exceed the nominal value of '1'.

The efficiency of the DPA can be calculated using the magnitude and phase of the terminal voltage of main device ($V_m$) and magnitude of the terminal voltage of the peaking device ($V_{out}$) using the following relations,

$$\eta_{main} = \eta_{AB}|V_m|cos(\theta) \tag{5.13}$$

whereas $\eta_{AB}$ in (5.13) is the maximum efficiency of the class-B PA and $\theta$ is the phase angle between current and voltage waves at the main device, and

$$\eta_{peak} = \eta_{AB}|V_{out}|. \tag{5.14}$$

Moreover, by using the assumption that phase and magnitude of $I_p$ track $I'_m$ perfectly, the total efficiency of the symmetric two-way DPA at full power level

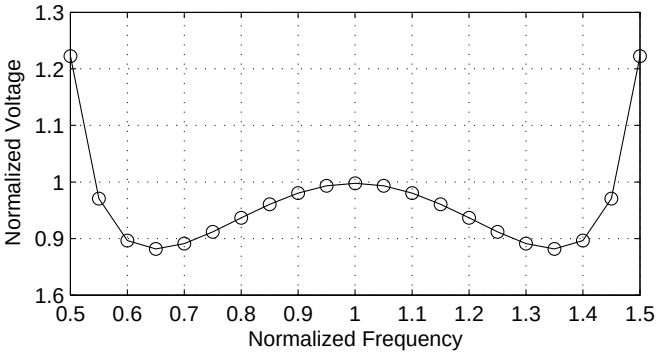


**Figure 5.16:** *Terminal voltage of main device for schematic of Figure 5.15 at 6dB PBO*

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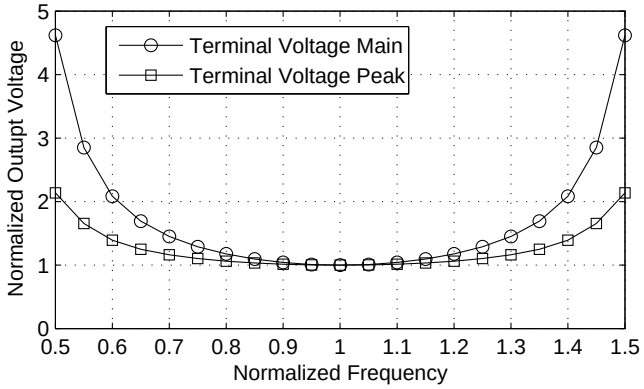


**Figure 5.17:** *Terminal voltage of main and peaking devices for schematics of Figure 5.15 at full power.*

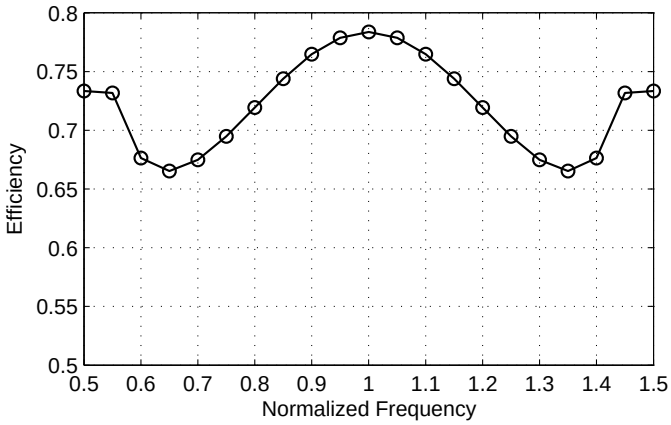


**Figure 5.18:** *Efficiency of the DPA at 6dB power back-off operation assuming class-B operation.*

can be calculated using (5.13) and (5.14), which reduces in this special case to,

$$\eta_{dpa,0dB} = \frac{\eta_{main} + \eta_{peak}}{2}. \tag{5.15}$$

The efficiencies at 6dB PBO as well as at full power levels are calculated by using (5.13), (5.14) and (5.15) and assuming hard clipping of the terminal voltages of the PA devices beyond '1'. It is also assumed that the both PA devices deliver equal power under the maximum power conditions. The results for these power levels are plotted in the Figure 5.18 for 6dB PBO and Figure 5.19 (for full power level).
Hence, the wideband impedance inverter demonstrates excellent performance (an efficiency BW of 100% at 6dB back-off as well as at 0dB back-off) but its integration in a real DPA circuit (along-with the output capacitance compensation technique of the previous sections) is quite tedious due the TL coupling involved and lack of space. A much simpler structure inspired by this configuration was derived by Xiaobo Deng [15][60] by assuming that the actual coupling between the coupled lines is reduced to zero (see Figure 5.20 and Figure 5.21).
To evaluate the efficiency performance of the DPA with this structure, an analysis similar to the one presented in section 5.2.1 can be performed. The Z-matrix of the structure shown in the Figure 5.21 can be obtained by replacing $R_L$ in (5.1) by the parallel combination of $R_L$ and the frequency dependent impedance of the short-circuited transmission line $TL_{sh}$ which is given by,

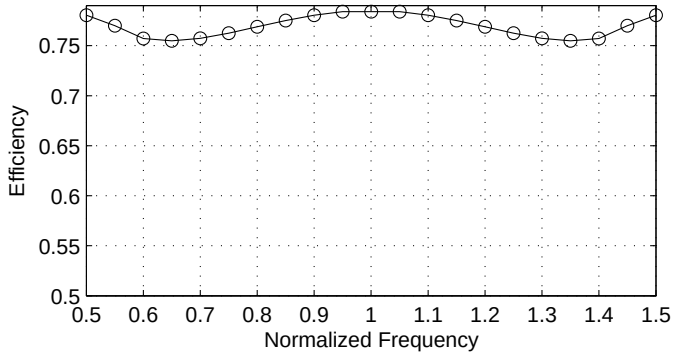


**Figure 5.19:** *Efficiency of the DPA at full power assuming class-B operation.*

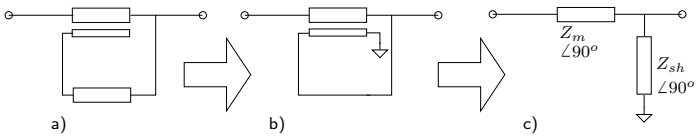


**Figure 5.20:** *a) Wideband impedance inverter b) Wideband impedance inverter after removing the* $90^o$ *feedback line. c) Equivalent of the wideband impedance inverter with coupling factor of zero.*

$$Z_{TL} = j.Z_{sh} tan(\frac{\pi}{2}\frac{f}{f_c}). \tag{5.16}$$

$Z_{sh}$ in (5.16) is the characteristic impedance of the short-circuited shunt transmission line, which can be chosen relative to $Z_m$ in order to provide the best compromise between the bandwidth at back-off and full power level. Note that $Z_m$ is characteristic impedance of the main transmission line. The new Z-matrix of the structure of Figure 5.16 is given by the following equation

$$\begin{bmatrix} \frac{Z_o(R_L^* \cos(f_n\frac{\pi}{2}) + jZ_o \sin(f_n\frac{\pi}{2}))}{Z_o \cos(f_n\frac{\pi}{2}) + jR_L^* \sin(f_n\frac{\pi}{2})} & \frac{Z_o R_L^*}{Z_o \cos(f_n\frac{\pi}{2}) + jR_L^* \sin(f_n\frac{\pi}{2})} \\ \frac{Z_o R_L^*}{Z_o \cos(f_n\frac{\pi}{2}) + jR_L^* \sin(f_n\frac{\pi}{2})} & \frac{Z_o R_L^* \cos(f_n\frac{\pi}{2})}{Z_o \cos(f_n\frac{\pi}{2}) + jR_L^* \sin(f_n\frac{\pi}{2})} \end{bmatrix}, \tag{5.17}$$

whereas $R_L^*$ in 5.17 is given by $(R_L \parallel j.Z_{sh} \tan(\frac{\pi}{2}\frac{f}{f_c}))$. The efficiency of the DPA using the simplified wideband impedance inverter of figure 5.20 is calculated by using (5.17) along-with (5.2), (5.3) & (5.4) and is plotted in Figure 5.22 for a symmetric two-way DPA at an output power back-off level of 6dB. It can be seen from the Figure 5.22, that this new impedance inverter provides roughly 17% more efficiency bandwidth than the conventional QWTL, which makes the

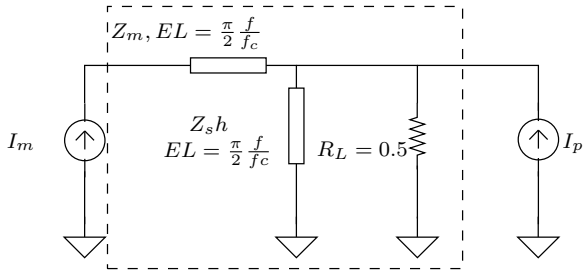


**Figure 5.21:** *Two-way wideband DPA using Xiaobo Deng's impedance inverter[15].*

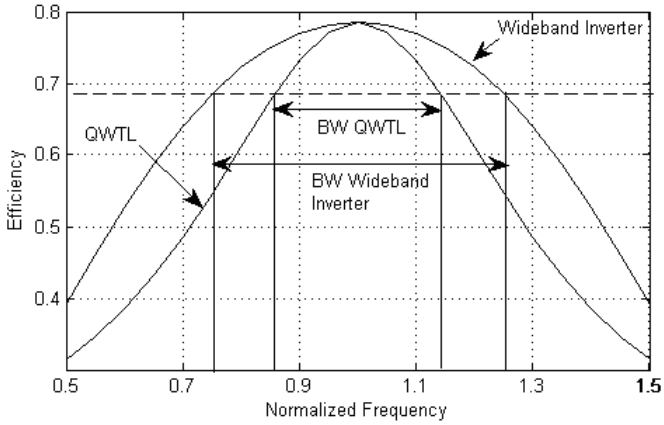


**Figure 5.22:** *Efficiency bandwidth of the bandwidth improved symmetrical two-way DPA at the 6dB power back-off level using simplified wideband impedance inverter as well as conventional QWTL.*

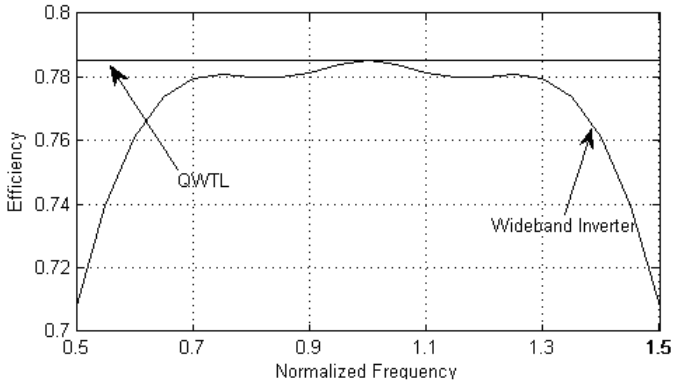


**Figure 5.23:** *Efficiency bandwidth of the bandwidth-improved symmetrical two-way DPA at full power level using the simplified wideband impedance inverteras well the conventional QWTL.*

total efficiency bandwidth of the DPA at back-off power levels equal to 45%. The performance of this novel impedance inverter at full power levels is plotted in Figure 5.23. Note that hard-clipping of the output RF voltage (beyond the normalized values of $'1'$ relative to the drain bias voltage) is assumed for generating the graphs of the Figure 5.23 and Figure 5.22. The resulting efficiency shows that unlike the QWTL, this impedance inverter has some BW limitations at full power. However this limitation does not really affect the overall bandwidth performance of the DPA, since its main BW restriction still arises from the bandwidth at power back-off operation.
From the discussion we can conclude that the best choice for impedance inverter for a wideband DPA is the coupled line impedance inverter. However, its integration in the DPA along-with wideband output capacitance compensation technique is quite troublesome. Therefore, the impedance inverter proposed by Xiaobo Deng [15] is used in the following sections to realize a wideband two-way symmetrical Doherty power amplifier.

## 5.8 Circuit Realization Based on the Improved DPA Combiner

In order to demonstrate the circuit idea presented in the previous section, a two-way DPA is designed using the new wideband impedance inverter proposed by Xiaobo Deng [15]. Its circuit diagram is shown in the Figure 5.24, which is quite similar to circuit of the wideband Doherty PA presented in the previous sections (see Figure 5.8). Again the output capacitances of the devices are absorbed in the output power combiner to improve the DPA wideband behavior. In addition to that, a short circuited QWTL is added to form the novel wideband band inverter along-with the quasi-lumped QWTL.
Figure 5.24 show the idealized schematic of the resulting wideband DPA, in which the short-circuited QWTL is directly connected to the drain of the peaking device. In practical implementations, however, it will be connected through bond-wires to the active device, which can disturb to some extend the desired transmission line operation. Therefore, in the actual circuit implementation, the bond-wire and the short-circuited QWTL are absorbed in the output matching network.

## 5.9 Simulation Performance

The Wideband DPA is designed and simulated using Agilents ADS (advanced system designer). The DPA of Figure 5.24 shows (in simulation) a very wideband efficiency performance both at full power as well as, at 6dB power back-off, yielding a efficiency of more than 50% over 700MHz bandwidth at back-off power levels and more than 60% at full power over a bandwidth of 800MHz (see Figure 5.25).

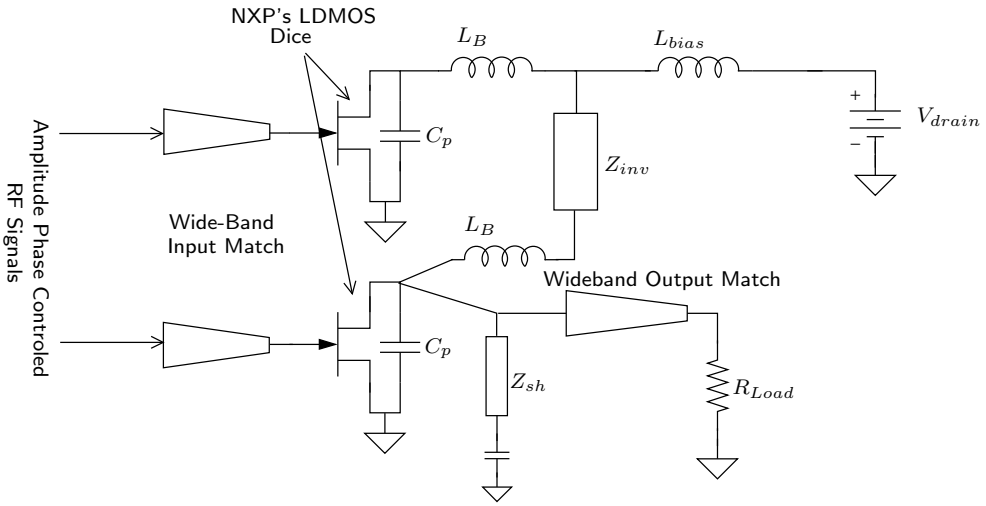


**Figure 5.24:** *Schematic of the improved wideband Doherty PA.*

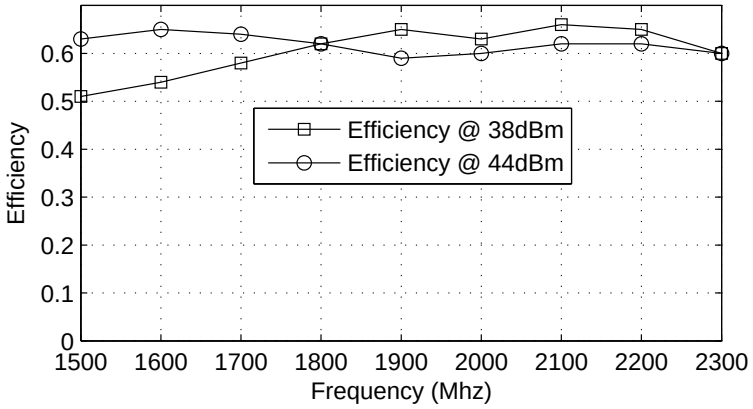


**Figure 5.25:** *Simulated performance of the improved wideband DPA at 6dB power back-off level (38dBm) and full power level (44dBm).*

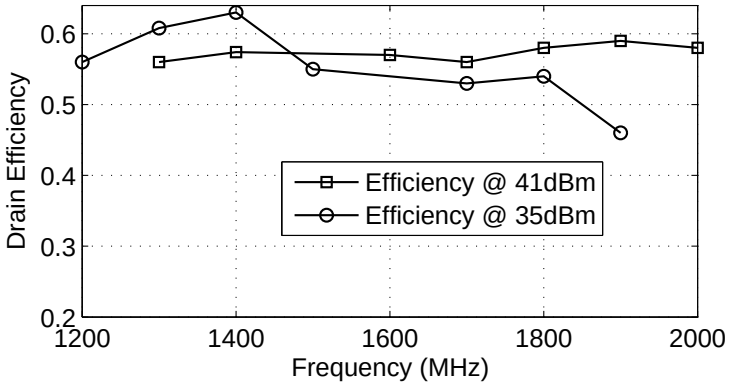


**Figure 5.26:** *Measured performance of the improved wideband DPA at 6dB back-off power level (35dBm) and full power level (41dBm).*

## 5.10 Measurements

The improved wideband DPA circuit was measured with a mixed-mode setup (explained in section 5.6). The initial measurements did not show good frequency response and it was concluded that the drain bond-wires heights were too low, therefore the DC supply voltage was reduced to 20V in order to increase the capacitance of the device and re-tune the output power combiner at a slightly different frequency band (1200MHz to 1900MHz) instead of (1500MHz to 2200MHz). The measured performance of the circuit with these bias adjustments is shown in the Fig. 5.26, which corresponds closely to the simulated results with a shift of center frequency, and proves the concept.

## 5.11 Conclusions

The bandwidth limitations of Doherty amplifiers have been evaluated. It is shown that the classical impedance inverter in a DPA has the ability to provide relative bandwidth of 28%. Moreover, the narrowband behavior which is typically exhibited in conventional DPAs is caused by the output capacitances of the PA devices. A technique is presented to absorb the output capacitance of the PA devices in QWTL, forming a quasi-lumped impedance inverter. With this technique the bandwidth of the DPA was only limited by the quasi-lumped impedance inverter. A prototype circuit with NXP's LDMOS devices demonstrated 300MHz bandwidth at 6dB power back-off level and 600MHz bandwidth at full power level. The second part of the chapter concentrated on improving the bandwidth of the impedance inverter itself. Two inverter topologies are presented. A coupled line

section (CLS) based impedance inverter and an impedance inverter derived from it in order to ease its circuit implementations. The CLS based impedance inverter provides the best performance, demonstrating 90% relative bandwidth at 6dB power back-off level and 100% bandwidth at full power levels, but due to the transmission line coupling involved, the implementation of this power combiner with the output capacitance compensation technique poses serious implementation issues.

The other wideband impedance inverter is derived from the CLS based impedance inverter by assuming the actual coupling between the coupled transmission line equal to zero. The circuit of this impedance inverter is very simple and suitable for integration with the output capacitance compensation technique presented in the first half of this chapter. Using this technique another improved demonstrator is designed which makes use of the output capacitance compensation technique along-with the improved power combiner. The simulations and measured results are quite promising, showing 700MHz bandwidth at back-off power level and 800MHz bandwidth at full power level, which out-perform the current state-of-the-art in the open literature. There are few wideband doherty power amplifiers are reported in literature which obtain the fractional bandwidth of 35% [61] and 42% [62]. These amplifier use the conventional doherty power combiner (QWTL) with degraded value of $k$, which results in high efficiency bandwidth of these amplifiers due to lower transformation ratio. However, this also moves the second efficiency peaking at PBO levels less than 6dB, thereby, causing lower average efficiency for modulated signals. This method is not very beneficial as the bandwidth is increased at the expense of average efficiency of the power amplifier.

Chapter 6

# Digital Pre-distortion Applied to Multi-Path Power Amplifiers

## 6.1 Introduction

As mentioned earlier in this thesis, modern communication systems use sophisticated digital modulation techniques (e.g., W-CDMA, OFDM) to increase their data rate and channel capacity [48][63]. This is accomplished by encoding the information in phase as well as amplitude of the RF carrier. Therefore, to obtain low bit error rates and reliable transmission of the signals, it is necessary that the transmitter does not introduce any amplitude or phase distortion in the output signals [6][48][63],which would result in (de)modulation errors [64]. The quality of the actual modulation is usually expressed in terms of the error vector magnitude (EVM) as given by [63]

$$EVM = \sqrt{\frac{\frac{1}{N}\sum_{r=1}^{N}|S_{ideal,r} - S_{meas,r}|^2}{\frac{1}{N}\sum_{r=1}^{N}|S_{ideal,r}|^2}}, \tag{6.1}$$

where $S_{ideal,r}$ and $S_{meas,r}$ represent the ideal and measured symbols in the symbol stream.
Additionally, all signals share the same communication media in wireless communication, therefore, it is also important that the transmitted signals must be confined to the allocated channel bandwidth only, and any out-of-channel emission is minimized in order to eliminate potential cross-channel interference [48]. The spectral emissions leaked into the frequency band of the adjacent channel(s)

are considered to be very important, since they cannot be filtered out using conventional techniques. A measure for these emissions, which we have used earlier in this thesis, is the Adjacent Channel Power Leakage Ratio (ACPLR) which is defined as the ratio of total signal power to the power, which is leaked into the (next) adjacent channels (ACPLR1 and ACPLR2). Different communication standards have different specification for their ACPLR1 and ACPLR2, e.g. 3G W-CDMA (base-station) has an ACPLR1 and ACPLR2 specification of 45dBc and 50dBc respectively [63][65].

Although the above mentioned performance parameters (EVM and ACPLR) seem to be independent at first glance, in reality they are closely related since they share the same physical origin, namely the non-linearities in the transmitters chain. Note, that although the transmit path contains many non-linear components (e.g.; mixers, pre-amplifiers, etc), usually the non-linearity of the final transmitting PA stage dominates the signal quality, since it has to handle the largest signal excursions in the transmitter chain [66].

The high peak-to-average power levels of these signals (e.g., WCDMA, OFDM) result in not only very stringent linearity requirements for the transmitter, but also result in efficiency degradation of the transmitter, which typically can only provide its maximum efficiency at peak-output power[6]. This problem of reduced average efficiency is addressed by using more advanced high-efficiency PA architectures (e.g., Doherty, EER, Outphasing), which utilize their active devices as close as possible to saturated operation for a substantial part of the envelope of the modulated signal [12][16]. It is not surprising that the active device and consequently the overall amplifier will behave nonlinearly under these conditions[6][12][16]. This will adversely affect the EVM, along-with an increase in emission in the adjacent channels. To solve for this linearity degradation, over time, various techniques have been introduced, e.g., feedback, feed-forward and digital pre-distortion.

In this chapter we first give a brief overview of the non-linearities introduced by PA devices and how they can affect the EVM and ACPLR of the transmitter. Later in this chapter, a linearization technique known as mapping-based digital pre-distortion, is discussed for improving the linearity of the PAs. Finally this technique is applied to the mixed-mode outphasing amplifier of Chapter 3 in order to improve its linearity performance.

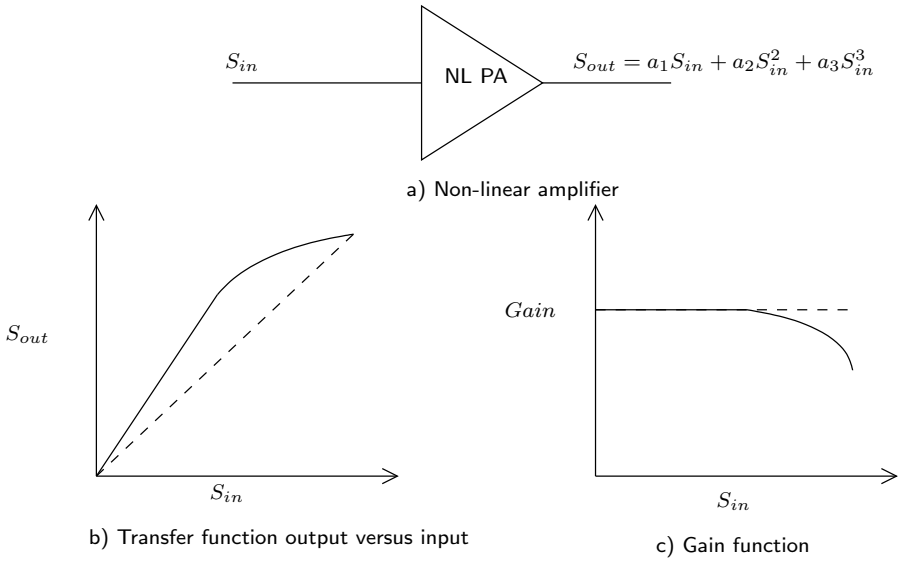


**Figure 6.1:** *Non-linear PA with transfer function*

## 6.2 Theory

It is important to understand the nature of non-linearities and their effects on the modulated signals, in order to fully understand the pre-distortion techniques presented later in this chapter. Therefore, the following paragraphs explain linear and non-linear systems alongwith their impact on the functionality of the RF power amplifiers.

### 6.2.1 Linear and Non-linear Systems

A system is considered to be linear if its output quantity is linearly proportional to its input quantity [64], as shown by the dashed line in Figure 6.1. In comparison, a non-linear system will exhibit a nonlinear relation-ship between input and output (e.g., a non-constant gain), for situations where the signal transfer becomes dependent on the amplitude of the input signal (Figure 6.1). Devices in power amplifiers can have either a quadratic (e.g FETs, LDMOS) or an exponential (e.g. BJT, GaAS and HBTs) input-output relation [39] depending on their physical nature, . However, when driving an active device closer to compression, other (stronger) nonlinearities also appear, yielding a degradation of the signal quality that becomes unacceptable for most communication standards [63]. At the same time, it is well known that PA devices operate most efficiently when operated at or close to their saturated conditions [6]. Consequently the linearity of efficient power amplifiers is usually poor.

The accurate modeling of the nonlinearities in PA devices is quite complex due to the multiple (undesired) mixing operations that occur at input and output of the active device [64]. Moreover, frequency selective (non)linear components in the PA devices and their surrounding circuitry makes modeling even more complex by introducing memory effects to the output signal. Although some techniques like Volterra series [67] can describe the behavior of PA stages with memory to some extent, the resulting expressions are usually too complex to be useful for understanding the exact implications of these nonlinearities on the resulting output signal with associated spectral re-growth.
Therefore, in order to support the understanding of the reader we will use a very simple model without memory effects here to describe a nonlinear equation,

$$S_{out} = a_1.S_{in} + a_2.S_{in}^2 + a_3.S_{in}^3, \tag{6.2}$$

where $S_{in}$ and $S_{out}$ are the input and output signals, respectively. Coefficient $a_1$ in (6.2) is the small-signal linear gain and $a_2$ and $a_3$ are the coefficients that relate to $2^{nd}$ order and $3^{rd}$ order nonlinearities, respectively. Although, only nonlinearities up-to third-order are considered here (6.2), practical situations can require a higher order to describe the dominant nonlinearities.
The input signals of RF power amplifiers are usually composed of sinusoidal signals constrained to a given frequency band. Therefore we will make use of a two-tone signal as input signal to analyze the linearity of the PA devices in the following text. A two-tone signal can be considered as a RF carrier modulated by a sinusoid consequently, a two-tone signal can be represented mathematically as,

$$S_{two-tone} = A\cos(\omega_c - \frac{\delta\omega}{2}) + A\cos(\omega_c + \frac{\delta\omega}{2}) \tag{6.3}$$

whereas $\omega_c$ in (6.3) is the frequency of the RF carrier and $\delta\omega$ is the frequency of the modulating baseband signal. The frequency spectrum of such a signal consists of two tones centered around $\omega_c$ and spaced $\delta\omega$ apart.

The output signal of the nonlinear PA represented by (6.2) for a two-tone signal can be calculated by substituting $S_{in} = S_{two-tone}$ and using some simple trigonometric manipulations [6]. The two tones in the input signal undergo self and cross-multiplication due to the quadratic and cubic nonlinearities, resulting in the generation of a number of new frequency components centered around DC: $\omega_c$ ,$2\omega_c$ and $3\omega_c$ (see Figure 6.2). The components generated around $2\omega_c$ and $3\omega_c$ are known as harmonic distortions, and are typically considered to be not very critical, since they fall outside the frequency band of interest and can be easily filtered out. In contrast the frequency components that appear close to carrier frequency $\omega_c$ , namely ($\omega_c - \frac{3}{2}\delta\omega$ and $\omega_c + \frac{3}{2}\delta\omega$) cannot be filtered out easily. These later components are known as intermodulation distortions (IMD) and are the main cause of degradation of the ACPLR1 and ACPLR2 of the transmitter under consideration.

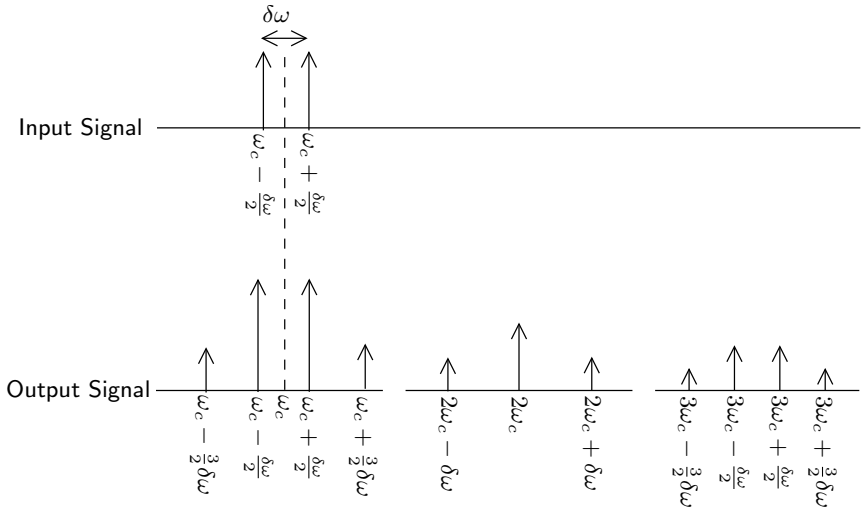


**Figure 6.2:** *Input and output spectrum of a two tone signal driving a nonlinear PA (in this figure nonlinearities up-to third order has been assumed)*

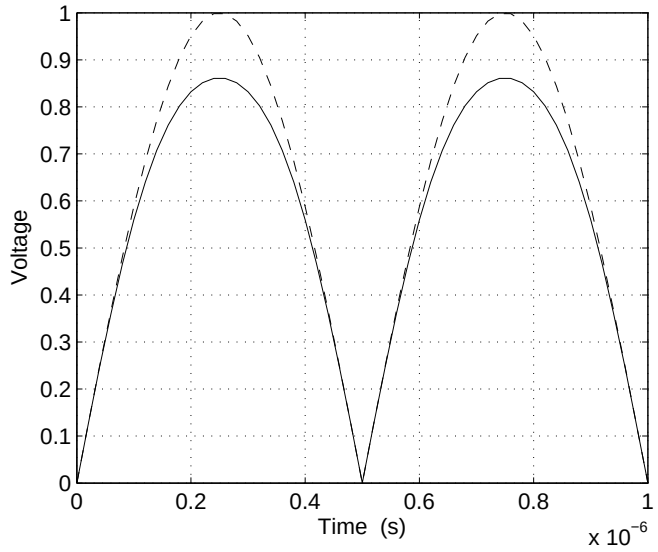


**Figure 6.3:** *Normalized input (dashed line) and output (solid line) envelope signals for a non-linear PA*

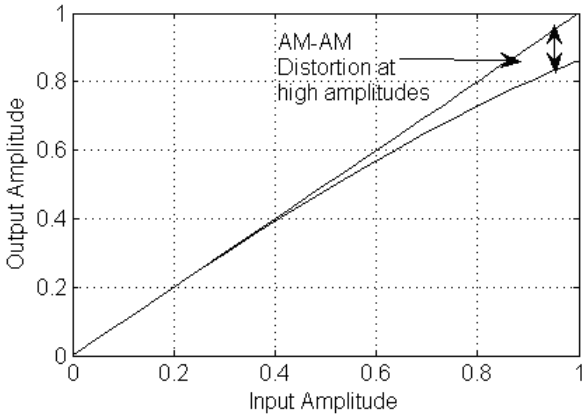


**Figure 6.4:** *Gain compression of a non-linear amplifier*

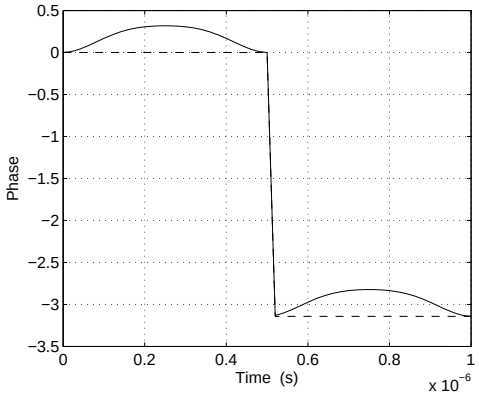


**Figure 6.5:** *AM-PM distortion for a non-linear amplifier*

In addition to the generation of the harmonic and inter-modulation components, nonlinearities also cause amplitude dependent gain of the fundamental components of the signal. This gain compression / expansion is given by (6.4) for nonlinear PA devices that can be represented by a third-order Taylor series expansion (6.4)

$$G = \frac{S_{out(fund)}}{S_{in}} = a_1 + a_3 S_{in}^3. \tag{6.4}$$

The sign of $a_3$ in (6.2) is usually negative which results in gain compression of the PA device as shown in Figure 6.4. This phenomenon is also revealed when considering the output signal in the time domain. Figure 6.3 shows the demodulated baseband output signal, which is distorted at higher amplitude levels. This distortion is due to the gain compression of the PA, and is also known as AM-AM distortion.

Moreover, as discussed previously, the presence of frequency selective components (e.g., nonlinear output capacitance) in the PA in combination with nonlinear distortion can also cause an undesired modulation of the phase of the output signal, which is known as AM-PM distortion. AM-PM signal conversion can also be modeled by (6.4) if the constants $a_1..a_3$ are assumed to be complex numbers. The AM-PM distortion of a non-linear PA modeled by (6.2) is shown in Figure 6.5.

In addition to the AM-PM conversion, other strong memory effects can also appear which can have a much more severe effect on the linearity of the amplifier [64]. An in-depth discussion of these strong memory effects, which can cause failure of amplifier linearization schemes, is beyond the scope of this thesis. Therefore, in the following text we only consider weak memory effects. Strong memory effects are avoided / minimized in this work by utilizing proper bias decoupling, good thermal grounding of the active devices as well as by the use of well-behaved harmonic terminations over the frequency band of interest [6].

In short, in this work the combined effect of AM-AM and AM-PM distortions dominate the amplifier linearity, causing a deformation of the information present in the modulated output signal. Due to these phenomena, the input and output constellation maps are no longer identical (Figure 6.6). Note that the cubic nonlinear model for the non-linearities of the PA is assumed in the Figure 6.6.

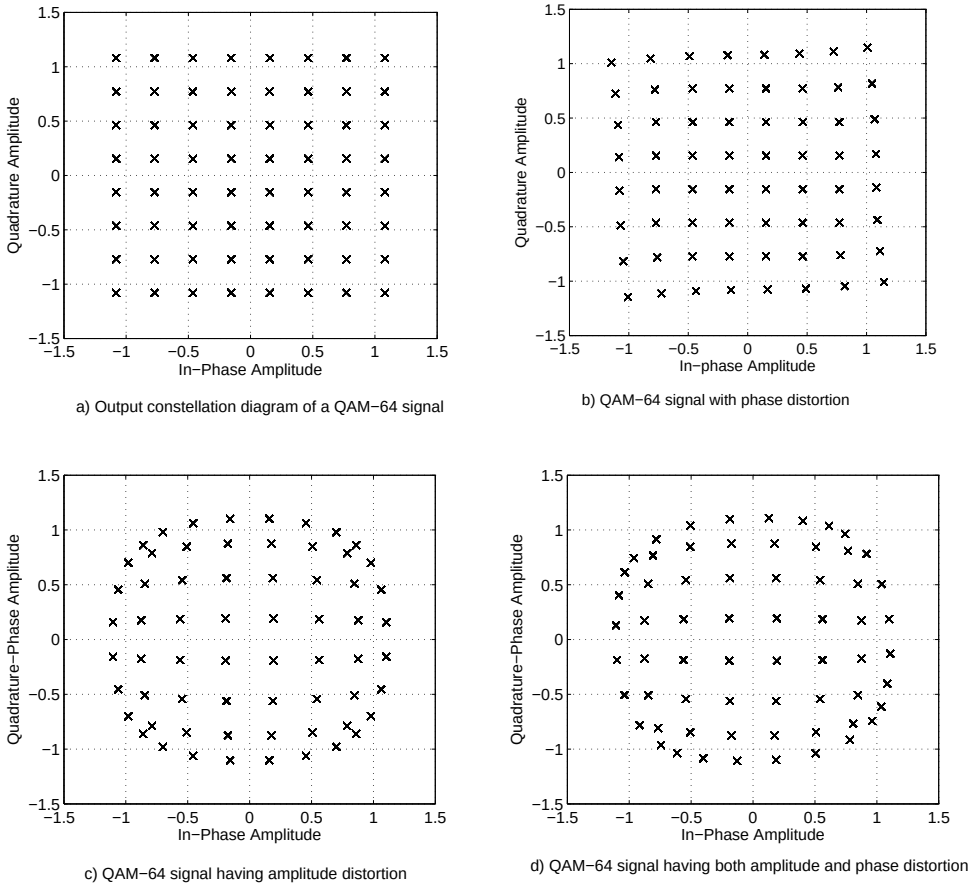


**Figure 6.6:** *Output constellation diagram of 64-QAM signal with and without amplitude and phase distortions*

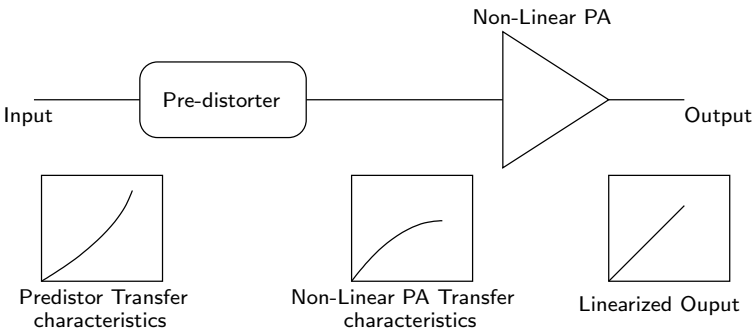


**Figure 6.7:** *Conceptual block diagram of a pre-distorter*

### 6.2.2 Pre-distortion

Pre-distortion is a technique to increase the linearity of the total transmit chain. In this concept a non-linear component (pre-distorter) precedes the power amplifier and shapes the input signal such that after passing through the (non-linear) power amplifier the output becomes a perfectly scaled linear replica of the original input signal [64]. More specifically, if the PA causes gain compression of the input signal at higher amplitudes, the pre-distorter should exhibit gain expansion at those amplitudes. As a result, the combined effect of the PA and pre-distorter should be a constant gain for all amplitudes (6.7). The overall transfer function of the PA and pre-distorter can be written as (6.5)

$$S_{out} = f_{PA}(f_{PD}(S_{in})) \rightarrow G.S_{in}. \tag{6.5}$$

The pre-distortion can be applied either directly to the input signal of the PA (analog pre-distortion) [68] or to the baseband input signal (digital pre-distortion) [64]. Both techniques are effective in principle, but digital pre-distortion is becoming more and more popular due to the increasing availability of low-cost high-speed digital signal processors (DSPs) and analog-to-digital converters. Moreover, digital pre-distortion allows easy adaption of the correction algorithm to adopt for drift in the nonlinear characteristics of the PA devices [64] (e.g., due to temperature changes, etc.).
Digital pre-distortion can be divided into two categories, namely: the model based digital pre-distortion [69][70] and lookup table based digital pre-distortion [71]. In the model based approach the nonlinearities of the power amplifier are described by techniques like the Volterra series [67]. In this method the linearity is improved by implementing the inverse function in the digital pre-distorter (DPD). This method is effective, robust and also able to handle memory effects. However, this approach requires more extensive computations alongwith careful characterization of the power amplifier in order to determine its parameters. In short, the actual implementation of this method can be quite difficult and time consuming.

The other category of digital pre-distortion is known as lookup table based digital pre-distortion [45][71]. In these approaches the phase and gain errors are usually stored in a lookup table and used to modify the input signal to improve for linearity. These methods are mostly quite effective and very simple to implement and yield rather competitive results. However, these methods do require larger digital memories and are therefore somewhat more expensive in their implementation.

#### Lookup-Table Based DPD

Different architectures of lookup-table (LUT) based digital pre-distorter have been presented in literature e.g., polar gain [72] , complex gain [73] and mapping based DPD [46]. The polar gain and complex gain based architectures use two 1-D lookup tables, to store the correction parameters for the amplifier gain and phase separately. These lookup tables are indexed with the input amplitude, after which the appropriate phase and gain correction is added to the input signal. In principle, these methods can be quite effective, but their input signal conditioning may require rectangular-to-polar and polar-to-rectangle conversion, making them computationally inefficient.
On the other hand constellation diagram mapping based pre-distortion algorithms operate directly on the in-phase (I) and quadrature-phase (Q) components of input signal using a two dimensional lookup table. Although this mapping based digital pre-distortion algorithm uses $\frac{N}{2}$ times more memory than needed by polar or complex gain type digital pre-distortion algorithms, it typically proves to be more computationally efficient [46]. In addition, when considering the operation of Chireix amplifiers with two independent branch amplifier inputs, the differential phase between these input signals will control the output amplitude. However, if the IQ modulators driving these branch inputs have phase and amplitude mismatches, these mismatches would directly appear as an amplitude error at the output of the amplifier. Consequently, a careful calibration of the IQ modulators is typically needed in practical outphasing systems to achieve correct operation. However, when the mapping based digital pre-distorter is used for pre-distortion of the outphasing amplifier, this IQ calibration would be automatically incorporated in the 2-D lookup table [16]. This advantage, combined with the low computational costs of this method, makes this algorithm a logical choice for the Chireix amplifier demonstrators introduced in this thesis.

### 6.2.3 Mapping Digital Pre-distorters

The block diagram of a mapping based digital pre-distorter is shown in Figure 6.9. In this concept the input in-phase ($I_{in}$) and quadrature-phase ($Q_{in}$) signals are added with the error correction signals $I_{corr}$ and $Q_{corr}$ (stored in a 2-D lookup table) and up-converted by an IQ modulator, after which amplification follows by

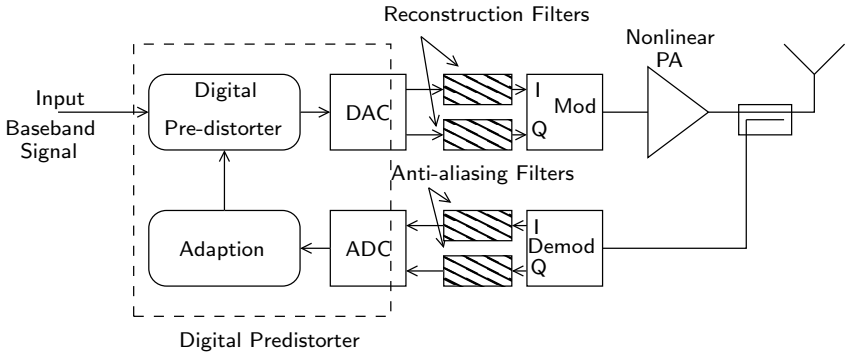


**Figure 6.8:** *Block diagram of the digital predistortion concept used for the outphasing amplifiers in this thesis*

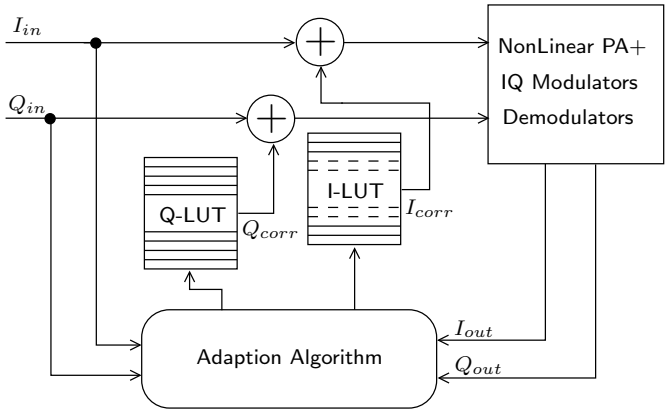


**Figure 6.9:** *Block diagram of a mapping based /cartesian digital pre-distorter*

a non-linear amplifier. The output of the PA is coupled to an IQ demodulator, which down-converts the RF output signal to generate the complex output vector ($S_{out} = I_{out} + Q_{out}$) as a baseband signal. This complex output vector along-with the complex input vector is then used to update the entries in the lookup table iteratively by using (6.6). At the very start, all the entries in the lookup table have a zero value, whereas, all the entries are updated after each iteration while operating. Once the entries in the lookup table converge, the adaption can be either stopped or slowed down in order to handle slow variations in the operating conditions of the amplifier,

$$I_{corr} = I_{corr} + \alpha(I_{out} - I_{in}), \tag{6.6}$$

$$Q_{corr} = Q_{corr} + \alpha(Q_{out} - Q_{in}). \tag{6.7}$$

In (6.6), $\alpha$ determines the convergence speed and the minimum final error in the modulation or linearity. A high value of $\alpha$ results in better speed and convergence but the final achievable modulation error can be higher. Note that the index to the 2-D lookup table is derived directly from $I_{in}$ and $Q_{in}$, and once the DPD is trained only a summation operation is needed to correct for the nonlinearity. Therefore, this method is considered to be more computationally efficient.

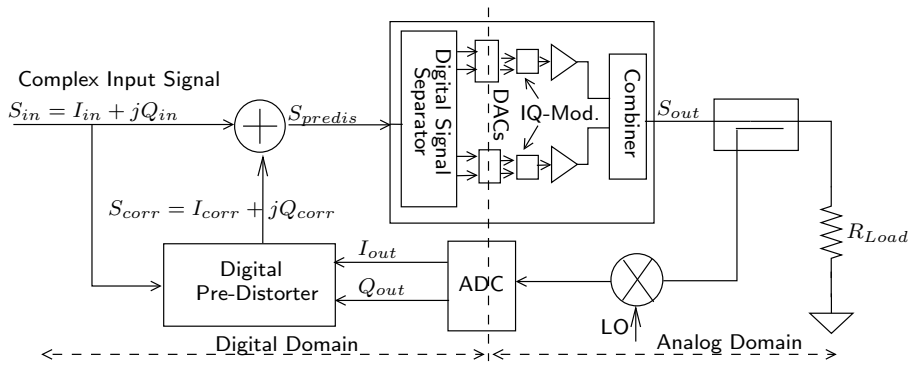


**Figure 6.10:** *Block diagram of the memoryless closed-loop DPD*

## 6.3 Pre-Distortion of Mixed-mode Outphasing Amplifier

The mixed-mode out-phasing amplifier as introduced in Chapter 3 contains two phase and amplitude modulated signals [16], which are optimized to maximize the efficiency of the amplifier. However, this optimization adversely affects the linearity of the amplifier and therefore the mixed-mode PA exhibits a relatively large amount of AM-AM and AM-PM distortion. This fact is also reflected by the measured gain and W-CDMA 3G response (see Figure 6.11 and Figure 6.13). The ACPLR1 and ACPLR2 for the W-CDMA signal is close to -30dBC and -35dBC respectively, which does not comply with the linearity specifications of the W-CDMA 3G communication standard. Therefore, mapping-based digital pre-distortion at the input is used to increase its linearity. Moreover, in order to simplify the pre-distortion algorithm, the mixed-mode PA along-with its IQ mixers and input signal splitter (implemented in software) is treated as a single-input, single-output baseband amplifier where its linearity is improved by matching the input and output constellation maps as closely as possible. Doing so, not only the non-linearities of the PA devices are corrected, but also the modulation errors due to the non-idealities of the IQ modulators and the signal path and phase unbalances of the branch amplifiers are eliminated. This property makes the calibration of the measurement setup simple and robust.

The block diagram of the pre-distorter along-with the mixed-mode out-phasing PA is shown in Figure 6.10. The input baseband signal ($S_{in} = I_{in} + jQ_{in}$) is summed with the correction signal $S_{corr} = I_{corr} + jQ_{corr}$ (generated from the 2-dimensional lookup table by using $I_{in}$ and $Q_{in}$ as an index). The resulting pre-distorted signal is then passed through the input signal splitter, which generates the complex signals for the individual IQ modulators. These IQ modulators convert the base-band complex signals to the phase and amplitude modulated

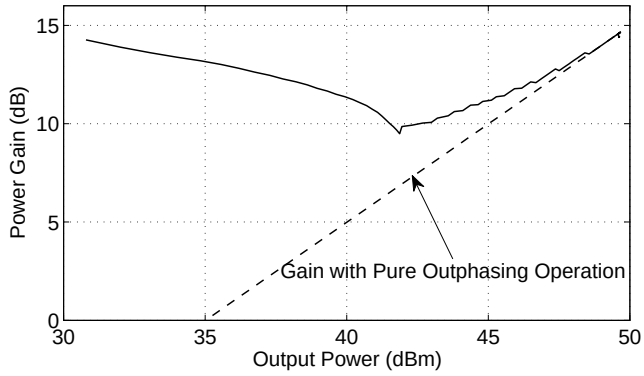


**Figure 6.11:** *Measured transducer power gain of the mixed mode amplifier and out-phasing amplifier as a function of output power*

RF signals used to drive the branch amplifiers. At the output of the mixed-mode amplifier the signal is also coupled to a down-converting mixer to generate a low IF replica. This low IF signal is then sampled by a high speed analog to digital converter which yields the baseband replica ($I_{out} + jQ_{out}$) in the digital domain. This output signal along-with the original input signal is then used by the pre-distortion algorithm to update the entries in the lookup table using (6.6). This pre-distortion algorithm is verified in a simulation environment using Matlab along with models that describe the complete measurement setup and the mixed-mode out-phasing amplifier. The simulation results are plotted in the Figure 6.12 and show a significant reduction of the inter-modulation sidebands in the output signal. With the pre-distortion algorithm verified, the algorithm was applied to the actual hardware, where it also proved to be successful yielding the results given in the Figure 6.13.

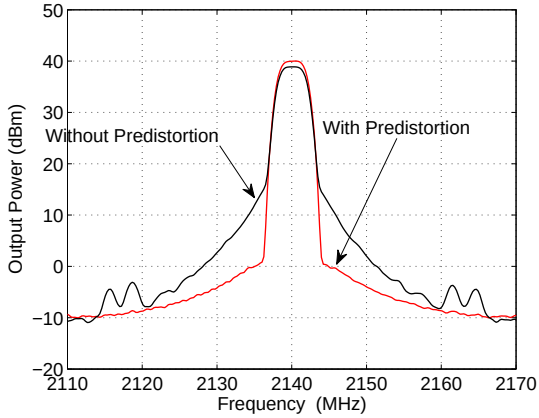


**Figure 6.12:** *Simulated W-CDMA signal with and without pre-distortion*

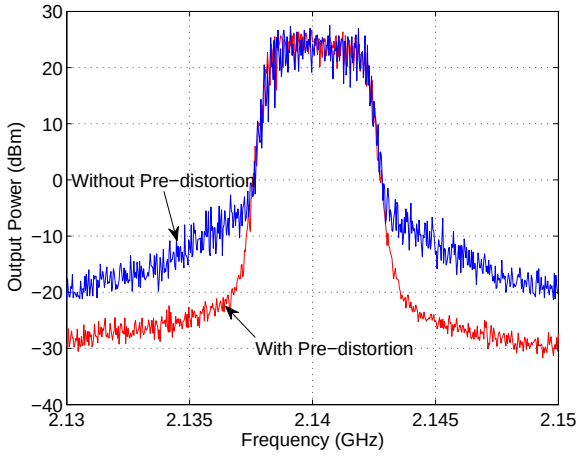


**Figure 6.13:** *Measured W-CDMA signal with and without pre-distortion*

## 6.4 Conclusions

The mapping based algorithm proves to be very effective for mixed-mode outphasing amplifiers [16], increasing linearity by almost 20dBc. Its main advantage lies in its simplicity, ease of implementation and being able to handle multi-path signals successfully. Moreover, another important benefit of the mapping based algorithm is the relaxation of the requirements of pre-calibration of the IQ mixers (in the transmit path) used to generate amplitude and phase-controlled signals. It has been observed that the LO leakage and phase-calibration of the IQ mixers is automatically corrected by the pre-distorter, making it an ideal choice for mixed-mode, multi-path power amplifiers.

Chapter 7

# Electronically-Tunable Phase Shifters for MIMO Systems

## 7.1 Introduction

Low cost, low loss tunable phase shifters that do not degrade the signal quality can act as an enabler of future MIMO (multiple-input multiple-output) communication and radar systems. An example of such a MIMO system is the phase-array antenna [74][75] (Figure 7.1), which consists of a number of antenna elements, each with individual phase control of its input/output signal. By controlling these phases, it is possible to steer the beam of the antenna without any mechanical movement. Such a feature not only allows the removal of mechanical rotation elements, but also provides a number of different advantages in terms of versatility, such as higher antenna gains and fast tracking of objects. So far, phased-array antennas are mostly being used only in military and space applica-

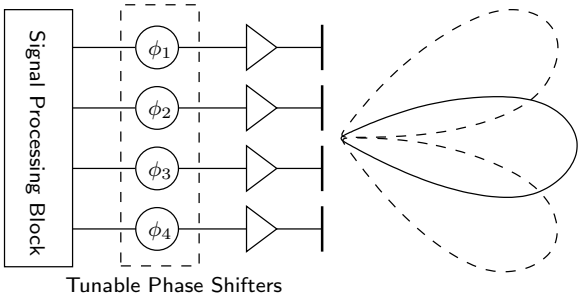


**Figure 7.1:** *Block diagram of a phased-array antenna*

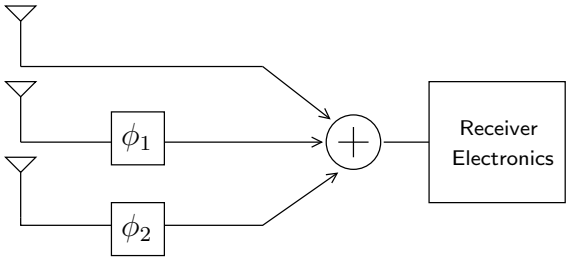


**Figure 7.2:** *Block Diagram of a Phase-Diversity Receiver*

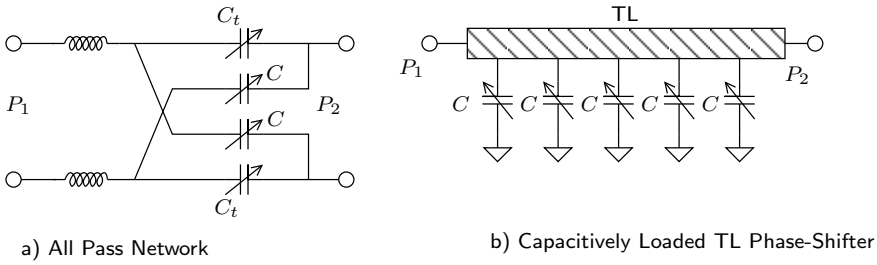


**Figure 7.3:** *a) All-phase network based phase-shifter. b) Capacitively loaded transmission line (TL) type phase-shifter*

tions due to their high implementation costs, however, recently these concepts are also proposed for use in mobile communication applications in order to increase link budget and therefore the transmission efficiency [76][77].
One such application of tunable phase shifters is in diversity transmitters / receivers (see Figure 7.2). In these systems, the communication signal is transmitted and received using more than one antenna. By controlling the phase relations between signal paths in combination with signal processing, multi-path fading can be reduced [78].
All the above-mentioned applications rely on the precise control of delay / phase relations between the multiple transmit or receive signals. Consequently, a phase-shifter with a large control range that behaves as a true time delay within the bandwidth of interest is desired in such applications. The position of the phase shifter in the transmitter and/or receiver chain also imposes some additional requirements in terms of insertion loss and linearity. On top of this, if the phase shifter has to be used in a handset receiver or a phased-array radar with many antenna elements, the DC power consumption and physical size of the phase shifter also becomes important.

Electronically-tunable phase shifters can be implemented either as an all-pass network [79][80](Figure 7.3a ), as a tunable lumped transmission line, or as a

capacitively-loaded transmission line [81][30] (see Figure 7.3b). The all-pass network implementations are quite compact and their phase control range can be high, however, their phase response is not linear with frequency. As a consequence they are less suited for applications which require a constant (controllable) delay over a large bandwidth [79]. The tunable lumped transmission lines and capacitively-loaded transmission lines on the other hand can be designed to provide a linear phase response over a wide bandwidth and therefore are known as true-time delay phase-shifters, which form the focus of this chapter.

In addition to the circuit topology, the choice of the tuning element also affects the linearity, size and DC power consumption of the tunable phase shifter. Most of the high-linearity phase shifters presented in the literature are based on PIN diodes or MEMS (Micro Electro-Mechanical Systems) varactors. PIN diode-based phase shifters can be low loss and highly linear, but they consume a significant amount of DC power [82][83] if they are designed to be low loss and highly linear. Due to their device nature the phase control they offer is mostly discrete. MEMS phase shifters, on the other hand, dissipate virtually no DC power and are both linear and low-loss [84]. The difficulties with MEMS based varactors are their moderate linearity for narrow tone spacing, the non-standard processing techniques required to fabricate them and the need for relatively expensive hermetic packaging. Moreover, due to the low capacitance density of MEMS varactors the area occupied by these devices is quite large, resulting in very large phase shifter implementations at low frequencies.

Another option for the tunable element(s) in a phase shifter is the use of semiconductor devices, e.g., the depletion capacitance of a MOS device or varactor diodes [39]. Such phase-shifters are compact, highly integrated, easy to tune and require almost no DC power. However, phase-shifters implemented with these elements have usually high insertion loss and poor linearity. Therefore, typically the performance of semiconductor-based phase shifters is often considered to be inadequate for the high demands of MIMO applications. However, if use is made of high-Q varactors in a silicon-on-glass (SOG) technology [85], combined with precise doping profile engineering and dedicated circuit techniques, varactor based phase shifters can provide both low-loss, and high linearity performance [86][87].

This chapter discusses the use of varicap diodes in true-time delay phase shifters, which are compact, low-loss and highly linear. To support the design of these components, the selection of the number of tunable segments and the characteristic impedance of true time delay phase shifters is discussed. The latter is important to optimize insertion loss, return loss of the phase shifter as well its linearity.

The ideas presented in this chapter are verified by designing a prototype phase-shifters using DIMES SOG (silicon-on-glass) technology.

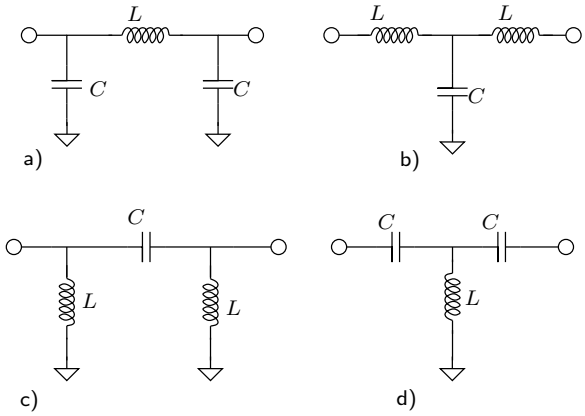


**Figure 7.4:** *a)* Π *lumped equivalent model of transmission line , b) T lumped equivalent model of transmission Line*

## 7.2 Theory

A transmission line as phase shifter will provide a constant delay at all frequencies. This delay depends on the propagation velocity ($v_p$) of the transmission line [52], which is the function of the inductance and capacitance per unit length of the transmission line

$$v_p = \frac{1}{\sqrt{L_i C_i}}, \tag{7.1}$$

where $L_i$ and $C_i$ in (7.1) is the inductance per unit length and the capacitance per unit of the transmission line, respectively.
The delay incurred by an ideal transmission line having a length ($l$) is given by

$$delay = v_p.l. \tag{7.2}$$

Equation (7.2) indicates that it is possible to make a true-time tunable delay phase-shifter if the propagation velocity of the transmission line can be varied, e.g., by varying $C_i$, $L_i$ or both [30][81]. However, in practice, it is quite difficult to vary these parameters since it involves changing physical properties [52]. Therefore, in more practical implementations of a transmission line based phase-shifter, a particular length of the transmission line is approximated by lumped inductors and tunable capacitors, and the phase velocity and associated delay can be changed by tuning the capacitors. The performance of such a phase-shifter depends on the ability of the lumped equivalent to approximate the behavior of a real transmission line over the desired bandwidth. This ability depends on several factors which are discussed in the following sections.

### 7.2.1 Lumped Equivalent Model of a Transmission Line

There are a number of choices for the lumped equivalent circuit of transmission line, e.g. Π network with capacitor / inductor as shunt elements (Figure 7.4a and 7.4c), $T$ network with capacitor / inductor as shunt element (Figure 7.4b and 7.4d). The lumped models of the Figure 7.4c and Figure 7.4d results in a phase response which is opposite to that of traditional transmission lines, therefore the use of these models is avoided for making tunable phase-shifters.
The lumped equivalent models of Figure 7.4a and Figure 7.4b have similar phase / delay characteristics and are compatible with traditional transmission lines. But the lumped model represented by Figure 7.4b results in a larger value of inductance required per unit electrical length of the represented transmission line. Hence the lumped model of Figure 7.4a is selected to make the electronically tunable phase-shifters.
The ABCD matrix for the elements of a single Π segment (as shown in the Figure 7.4a) is normalized to the characteristic impedance $Z_o$ of the transmission line (modeled by the circuit of the Figure 7.4a is given by

$$\begin{bmatrix} A & B \\ C & D \end{bmatrix} = \begin{bmatrix} 1 & 0 \\ jY_C & 1 \end{bmatrix} \begin{bmatrix} 1 & jX_L \\ 0 & 1 \end{bmatrix} \begin{bmatrix} 1 & 0 \\ jY_C & 1 \end{bmatrix} \tag{7.3}$$

$$\begin{bmatrix} 1 - Y_C X_L & jX_L \\ jY_C(2 - Y_C X_L) & 1 - Y_C X_L \end{bmatrix}, \tag{7.4}$$

whereas $Y_C$ and $X_L$ represents the normalized susceptance and reactance of the lumped capacitor and inductor respectively.

$$Y_C = \omega C Z_o \tag{7.5}$$

$$X_L = \frac{\omega L}{Z_o} \tag{7.6}$$

From the ABCD parameters, the $S_{21}$ and $S_{11}$ of the lumped equivalent structure can be calculated by using

$$S_{21} = \frac{2}{A + B + C + D} \tag{7.7}$$

and

$$S_{11} = \frac{-A + B - C + D}{A + B + C + D}, \tag{7.8}$$

which yields the following equations for $S_{21}$ and $S_{11}$

$$S_{21} = \frac{2}{2(1 - X_L Y_C) + j(X_L + 2Y_C - Y_C^2 X_L)} \tag{7.9}$$

$$\angle S_{21} = \tan^{-1}\left(\frac{Y_C^2 X_L - 2Y_C - X_L}{2(1 - Y_C X_L)}\right). \tag{7.10}$$

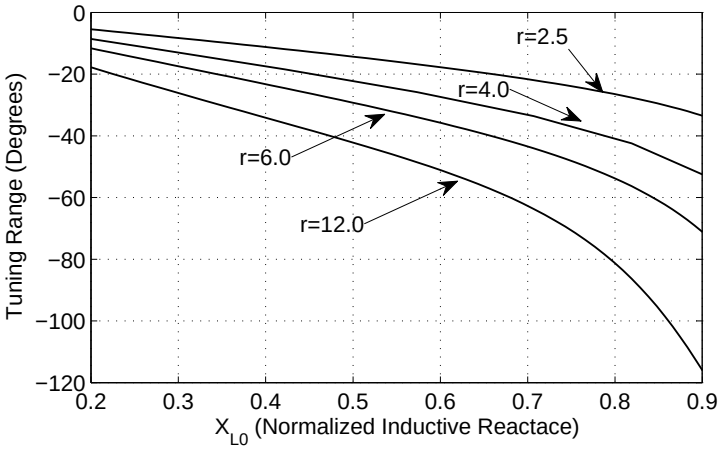


**Figure 7.5:** *Tuning range of a single segmented lumped-TL based phase-shifter*

The equations (7.9 and (7.10) can be solved for $S_{21} = 1$ and $S_{11} = 0$ for a single frequency $f_o$, which results in the following relation between $X_L$ and $Y_C$ of the lumped equivalent network:

$$X_{L,0} = \frac{2Y_{C,0}}{1 + Y_{C,0}^2}, \tag{7.11}$$

whereas $X_{L,0}$ and $Y_{C,0}$ are respectively the inductive reactance and capacitive susceptance at the center frequency $f_o$.

Equation (7.10) shows that the phase of the structure can be varied by changing $X_L$ (the inductor), $Y_C$ (the capacitor), or both. At first glance, varying both $X_L$ and $Y_C$ appears to be very attractive as it would always give zero reflection, however, this solution has some serious complications when aiming for practical implementations [88]. Namely, real tunable inductors are not available within conventional process technologies, although, tunable inductors are often approximated by a combination of a fixed inductor with a shunt varactor. Unfortunately, the related Q of the resulting tunable inductor drops quickly with the tuning range. Moreover, such a tunable inductor can only act as an inductor over a very narrow frequency band. Consequently, varying both inductance and capacitance in the ladder network is not beneficial in practical situations, since the increased losses and limited bandwidth quickly overwhelm the potential improvements that can be obtained by using tunable inductors. Therefore, from here on, the delay of the lumped equivalent transmission line is only varied by the value of the capacitor.
If '$r$'is assumed to be the tuning ratio of the capacitor, we can write ($Y_C = x.Y_{C,0}$)

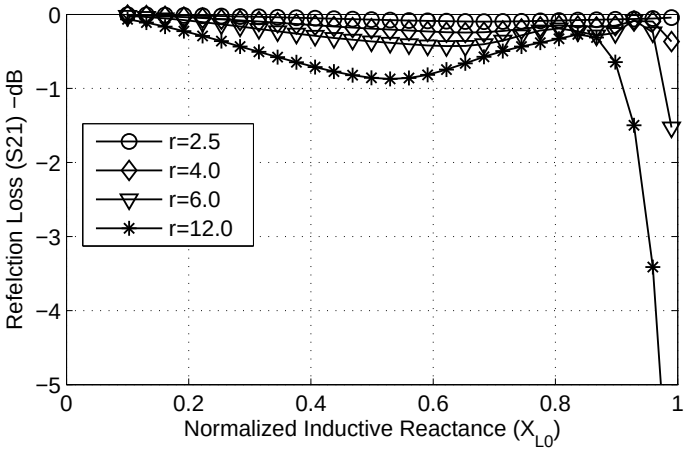


**Figure 7.6:** *Reflection loss of a single segmented lumped-TL based-phase-shifter*

with $x$ varying from $\frac{1}{\sqrt{r}}$ to $\sqrt{r}$. This results in variation in the phase of the structure and is shown in Figure 7.5. Note that the variation of $Y_C$ does not only changes the delay of the phase-shifter structure but also makes the relation (7.11) invalid, resulting in non-zero reflection loss as the varactor is tuned for changing the delay of the phase-shifter. Figure 7.6 shows the reflection loss of the structure for different values of tuning range '$r$'and normalized inductive reactance $X_{L,0}$. It can be seen from these plots that the combinations of '$r$'and $X_{L,0}$ which provide very high tuning range also incur very high reflection loss. Therefore the choice of such values is not beneficial in practical implementations.

Another interesting effect that can be seen from the Figure 7.6 is the dip in reflection loss for values of $X_{L,0}$ between 0.8 and 0.9. This can be explained with the help of the equation (7.11); $Y_{C,0}$ have two solutions for every value of $X_{L,0}$. For the above mentioned range of $X_{L,0}$ these two solutions fall between $\frac{Y_{C,0}}{\sqrt{r}}$ and $Y_{C,0}.\sqrt{r}$. Consequently the structure of the Figure 7.4a is tuned at two points within the tuning range of $Y_C$. In principle, such choice of $X_{L,0}$ would result in a phase-shifter with very high tuning range and very low maximum reflection loss, but it would be avoided due to other reasons, e.g., the phase-linearity and bandwidth of the phase-shifter.

Moreover, in practical situations, a number of such segments are used in cascade configuration (Figure 7.7) in order to realize wide-tuning range phase-shifters. The performance of such multi-segmented phase-shifters also depends on the choice of number of segments (N) alongwith the value of $X_{L0}$ chosen for each segment, an approach that we will analyze in detail in the following sections.

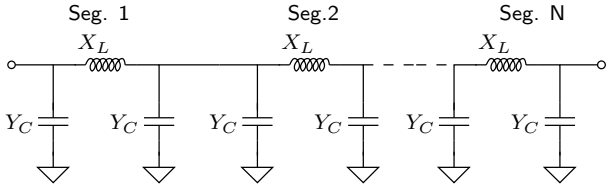


**Figure 7.7:** *The lumped equivalent circuit of a transmission having N segments*

### 7.2.2 Optimum Segmentation of a True-Time-Delay Phase-Shifter

The previous sections presented the electrical characteristics of a single segment varactor-loaded transmission line type phase-shifter. It was shown that a single segmented phase-shifter can provide a phase tuning range as high as $180^o$. However, it requires varactors with very high tuning range ($r \geq 16$) for that phase control range. Although there are some varactor technologies (e.g., MEMS) which can provide such a high tuning range, use of MEMS technologies requires the use of non-standard processing techniques and hermetic packages, which increases the costs. Moreover, it will be shown later in this chapter, that a single segmented phase shifter will be limited in its bandwidth and will exhibit a non-linear phase versus frequency response.

Therefore in most practical implementations of loaded transmission line based phase-shifters, a large number of segments are used. Unfortunately, the use of a large number of segments not only increases the chip area of the phase-shifter, but also increases its losses. In order to help the designer selecting the optimum number of segments for a given application, this section quantifies how the number of phase-shifter segments impacts the different performance parameters such as reflection loss, bandwidth, phase linearity and chip area.

The circuit diagram of a multi-segmented varactor loaded transmission phase-shifter containing N segments is shown in the Figure 7.7. The scattering matrix of the complete structure can be found by multiplying the transmission matrix of all individual segments and converting the result back to an s-parameters representation. This procedure can be quite cumbersome and may result in very complicated equations. Alternatively, if we assume that the number of lossless reciprocal segments always increases by a factor of two (e.g., 1,2,4,8,16,32 and so on), a very simple equation (7.12) for the s-parameters of the cascaded segment phase-shifter can be obtained [30], which can be recursively applied to obtain the s-parameters of the full structure

$$s_{21,c} = \frac{s_{21,o}^2}{1 - s_{11,o}^2}, s_{11,c} = \frac{(s_{11,o}^2 - 1 - s_{21,o}^2)s_{11,o}}{s_{11,o}^2 - 1}. \tag{7.12}$$

Note that the phase-tuning range of the complete phase-shifter is fixed to $90^o$ in the following sections, in order to study how the number of segments influences

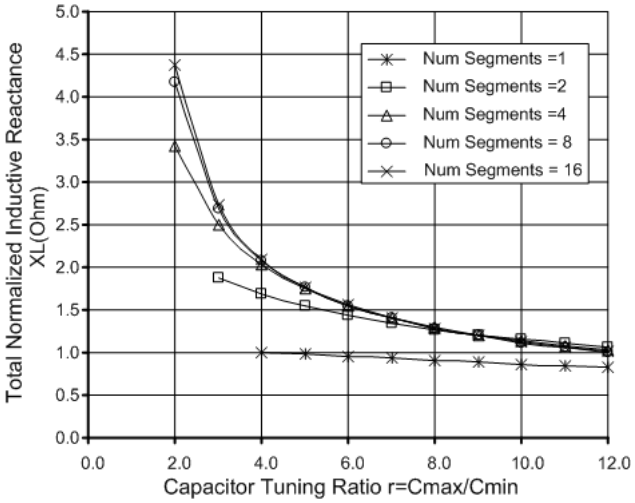


**Figure 7.8:** *Normalized inductive reactance ($\frac{X_L}{Z_o}$) versus capacitance tuning ratio, for a phase shifter with a $90^o$ phase control range using different numbers of line segments*

the various parameters (e.g., area, bandwidth, loss) .

### 7.2.3 Chip Area Optimization

In order to study the potential area reduction of the true-time-delay phase-shifter implementations, we plot (Figure 7.8) the total normalized reactance needed to realize a $90^o$ phase control range when using different numbers of line segments. To do this, we calculate the of value of $Y_C$ that yields $S_{21} = 1$ for a given $X_L$. Next , $Y_C$ is varied from $\frac{Y_C}{\sqrt{r}}$ to $\sqrt{r}.Y_C$ (with r being the tuning range; $r = \frac{Cmax}{Cmin}$). The resulting phase control range sets the number of segments needed for a $90^o$ tuning range (see Figure 7.8).
From this plot, we observe that the total inductance needed for $90^o$ phase control decreases with increasing tuning range. When only a small capacitance tuning range is feasible, a $90^o$ tuning range cannot be met using just a few segments (e.g., two segments can only provide a $90^o$ control range with a capacitance tuning ratio higher than three). Moreover, the total inductance required increases when finer segmentation is used. From an area perspective, a single segment phase-shifter appears to be the best choice, when feasible. In practical implementations, however, the varactor tuning range will be limited and other parameters like reflection loss, bandwidth, phase and amplitude linearity will be equally important. For this reason, we will analyze these performance parameters as well.

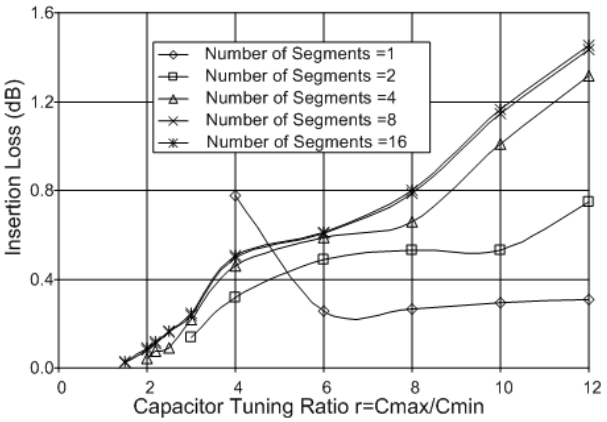


**Figure 7.9:** *Maximum insertion loss ($S_{21}(dB)$) for the $90^o$ phase shifters as function of capacitance tuning range and line segmentation.*

### 7.2.4 Phase-Shifter Insertion Loss

Another important property of the phase-shifter is its maximum insertion loss ($IL_{max}$) and the difference between its maximum and minimum insertion loss $\Delta IL$. The latter is important for the amplitude matching of different paths in a MIMO system. Note that in a phase-shifter composed out of lossless segments the insertion loss results entirely from the reflection loss. Therefore, these two terms can be used interchangeably for lossless phase-shifters. As discussed already, a capacitivly loaded phase-shifter will show its minimum insertion loss/reflection loss (which is zero in the case of a lossless line segments) where the relation($XL = \frac{2.Y_C}{1+Y_C^2}$) holds. When properly designed this point of minimum loss occurs at the middle of the tunable range of the varactor. The maximum insertion loss, on the other hand, occurs at the edges of the tuning range of capacitor and is given

$$IL_{max} = min(S_{21}(Y_{Cmax}), S_{21}(Y_{Cmin})), \tag{7.13}$$

whereas $\Delta IL$ is defined as

$$\Delta IL = max(S_{21}) - min(S_{21})). \tag{7.14}$$

The above relation indicates that $\Delta IL$ is equal to $IL_{max}$ for a phase-shifter composed out-of lossless line segments. Equation (7.13) along-with (7.12) can be used to calculated the $IL_{max}$ of a phase-shifter made with cascaded Π-sections. The results are plotted in Figure 7.9 for a $90^o$ tuning range phase-shifter. It can be concluded from Figure 7.10 that the use of high number of sections can provide the lowest insertion loss. However, the reflections from the individual segments result in a higher total loss than single or two-segment phase shifter when using

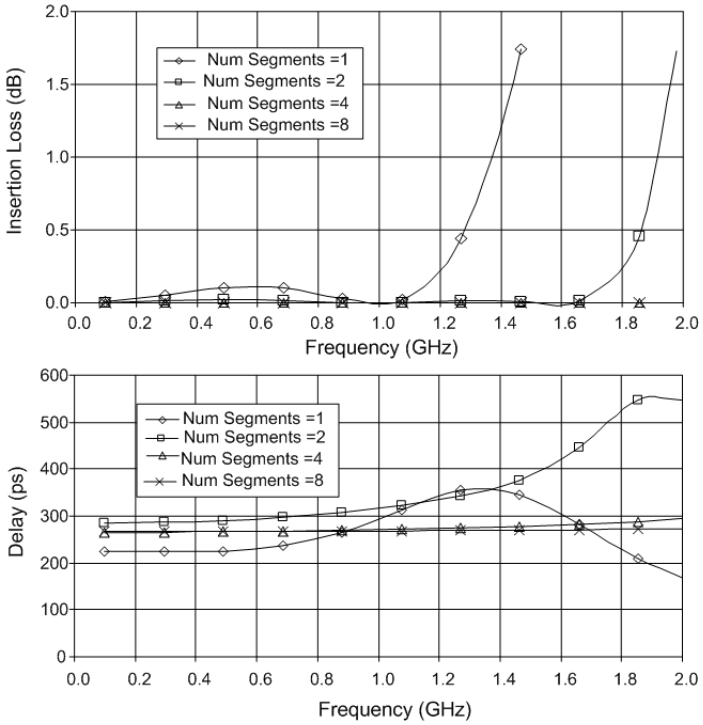


**Figure 7.10:** *Delay and insertion loss of Phase shifters with* $90^o$ *phase control as function of frequency with different line segmentations*

high tuning ratio varactors. It is therefore necessary that the number of the segments should be kept sufficiently high (i.e., $N \geq 4$ per $90^o$ tuning range). Another interesting observation, which can be made from Figure 7.9 is, that by increasing the number of segments to more than 4 for low tuning range varactors ($r \leq 3$) does not provide any significant benefit in terms of the insertion loss of the phase shifter.

### 7.2.5 Frequency Response & Phase Linearity

The number of transmission line segments has a strong influence on the phase linearity versus frequency. Figure 7.10 shows the group delay variations as a function of frequency for phase shifters using different line segmentations. When the number of segments becomes high, the phase shifter approximates the delay of an ideal transmission line. From Figure 7.10, we conclude that although the single segment phase shifter provides the smallest form-factor, it is the most narrowband implementation in terms of delay and insertion loss compared to phase shifters

with finer segmentation.

### 7.2.6 Impedance of the True-Time Delay Phase-Shifter

The choice of the characteristic impedance of the transmission line based phase-shifter has a strong effect on the inductance (and hence the area) required by the phase-shifter. Equation (7.6) show that the inductance required by the phase-shifter is inversely proportional to the characteristic impedance of the phase-shifter. Therefore, if a phase-shifter can be designed using a lower characteristic impedance, the required chip area can be greatly reduced. Moreover, if the variable capacitance in the phase-shifters are implemented using reverse-biased diodes, the low impedance of the phase-shifter can help improve the linearity of the phase-shifter, as the RF voltage swing for a given power level along the phase-shifter is lower, resulting in better linearity performance.

### 7.2.7 Differential versus Single-ended Design

Additional chip area savings can be achieved using a differential topology for the phase shifter implementation. The phase of $S_{21}$ for a single segment of this structure is given by (7.15). Note that this result is equivalent to that of the single-ended phase shifter when, in (7.10), $X_L$ is replaced by $2.X_D$ and $Y_C$ is replaced by $\frac{Y_D}{2}$. This implies that a differential phase shifter needs only half the inductance between the capacitors for the same phase tuning range compared to a single ended implementation.

$$\angle S_{21_{diff}} = tan^{-}1(\frac{0.5Y_D^2X_D - Y_D - 2X_D}{2(1 - X_DY_D)}) \tag{7.15}$$

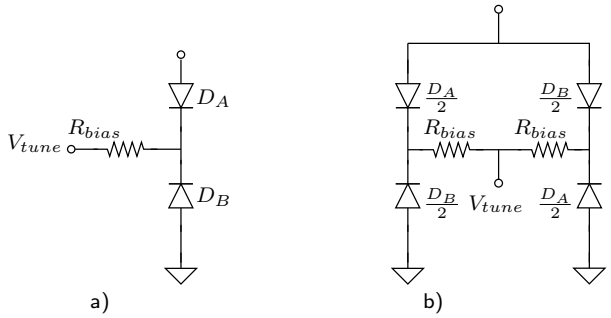


**Figure 7.11:** *Distortion free varactor stacks (DFVS), a) Anti-series configuration eliminating third order distortion for $n = 0.5$, b) Anti-series , Anti-parallel configuration suppressing third order distortion for $n \geq 0.5$*

## 7.3 High Linearity Low-Loss Varactors

The phase-shifters presented in this chapter use the depletion capacitance of diodes as tuning elements. A reverse-biased diode acts as a voltage-controlled variable capacitor with its capacitance given the following relation

$$C(V) = \frac{K}{(\psi + V)^n}, \tag{7.16}$$

whereas $\psi$ is the built-in potential of the diode, $V$ is the applied voltage, $n$ is the power law exponent of the diode capacitance, and $K$ is the capacitance constant. The power law exponent exhibits a wide variation in different situations, from a value of $n \approx 0.4$ for an implanted junction to $n \approx 0.5$ for an uniformly-doped junction, to $n \approx 1.5$ for an hyper-abrupt junction. Equation (7.16) shows that the capacitance of the reverse-biased diode exhibits a strong non-linear behavior which can be approximated by the following Taylor series for an incremental voltage $v$ [86].

$$C(v) = C_o + C_1.v + C_2.v^2 + ..., \tag{7.17}$$

where the $C_1$ term in (7.16) gives rise to second-order distortion and $C_2$ term in (7.16) gives rise to the third-order distortion. Fortunately, circuit design techniques can help to minimize these distortion prodcuts. It is shown in [86][55] that these distortion products can be minimized by using two varactor diodes (having the same size) in anti-series configuration (see Figure 7.11) with $n = 0.5$. Another low distortion topology which is employed for $n \geq 0.5$ uses four diodes in anti-series and anti-parallel configuration[86]. Selection of the active areas of the diodes in this configuration with respect to the value of $n$ cancels the third-order distortion products to a great extent.

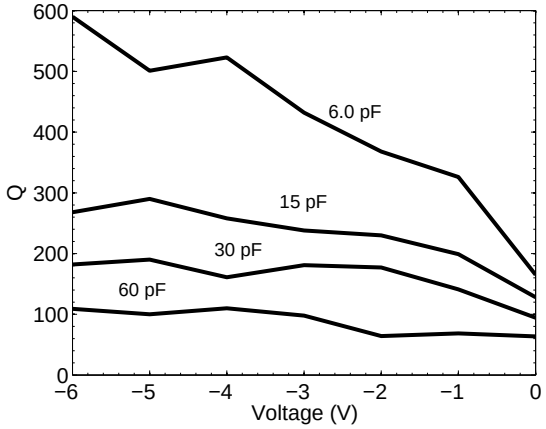


**Figure 7.12:** *Measured quality factor (Q) of the distortion-free varactor stacks developed in DIMES($f_{meas} = 2.0GHz$)*

Along-with their linearity, the Q of these varactors is also very important. Therefore, in order to fulfil the requirements of high performance RF adaptive circuits, a dedicated silicon-on glass varactor technology was developed at the Delft University of Technology. This technology provides a low-loss substrate. Patterning of both the front and back sides of the wafer enables the intrinsic varactor to be directly contacted by thick metal on both sides. This eliminates the need for a buried layer of finger structures, as would be the case in the conventional integrated varactor implementations. This technique results in quality factors greater than 100.
In short, the combination of novel design techniques (anti-series configuration) and advanced processing techniques (DIMES SOG) results in a very linear as well as very low-loss tunable capacitor which proves to be vital components in the realization of TL phase-shifters. Figure 7.12 shows the measured quality factors of these components versus reverse bias for different values of the zero-bias depletion capacitance Figure 7.13 shows the measured linearity for such a varactor stack.

## 7.4 Prototype High Linearity Low-Loss Phase-Shifter

A very low-loss phase-shifter [30] was designed using the DFVS (presented in the previous sections). The usable tuning range of the varactors is 2.5, which gives the optimum number of segments for a $90^o$ phase control to be between 4-5 (see also Figure 7.8) for optimum performance. Moreover, the impedance of the phase-shifter was chosen to be equal to $12\Omega$ and a differential topology was utilized in order to maximize the phase tuning range / area ratio. The targeted application for this phase-shifter type is phase-diversity transmitters / receivers, but for this

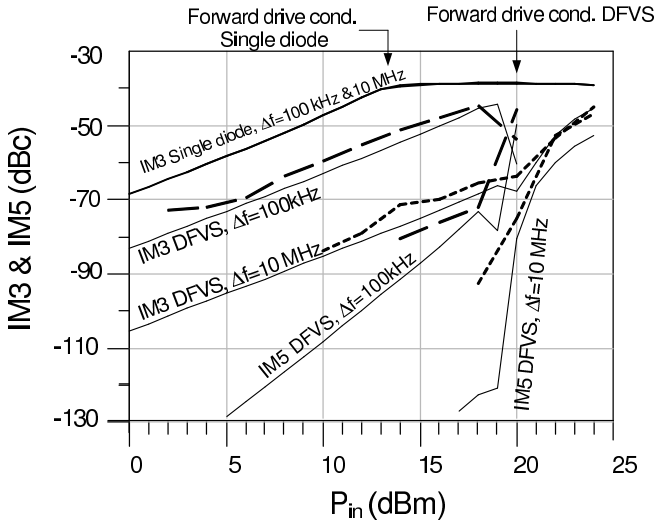


**Figure 7.13:** *Linearity performance of the distortion-free varactor stacks developed in DIMES*

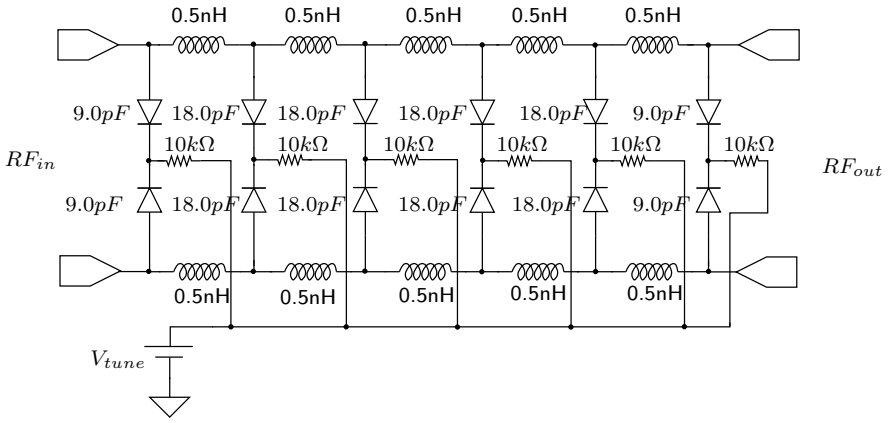


**Figure 7.14:** *Schematics of the low loss 12Ω differential phase-shifter*

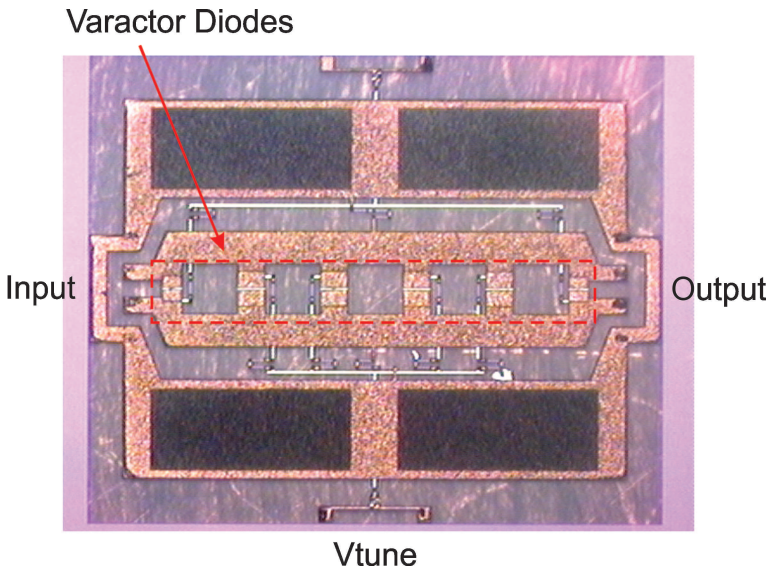


**Figure 7.15:** *Micro photograph of the implemented low-loss differential phase-shifter based on low distortion silicon-on-glass varactor configurations*

particular demonstrator the tuning range has been limited. Higher tuning ranges can be obtained by cascading multiples of such phase-shifter sections.

The schematic of the phase-shifter is presented in the Figure 7.14. The required series inductance value is low due to the use of the low characteristic impedance and differential structure. This facilitates us to use of thick straight copper lines to implement the inductors (0.5nH per segment). Note that this choice enables a very compact and simple integration and also results in a higher Q factor ($\geq$50) than is normally achieved with a spiral inductors. The micro-photograph of the implemented phase-shifter is shown in Figure 7.15, with it measured s-parameter given in Figure 7.16. Note the very low loss of 0.3dB at 1.0GHz indicating a 0.6dB per $90^o$ loss performance. The linearity of the phase shifter was measured with the load-pull system of TuDelft [89] . The linearity results are shown in Figure 7.17 showing an IM3 less than 56dBc at Pout=19 dBm, which corresponds to an IIP3 better than 47 dBm.

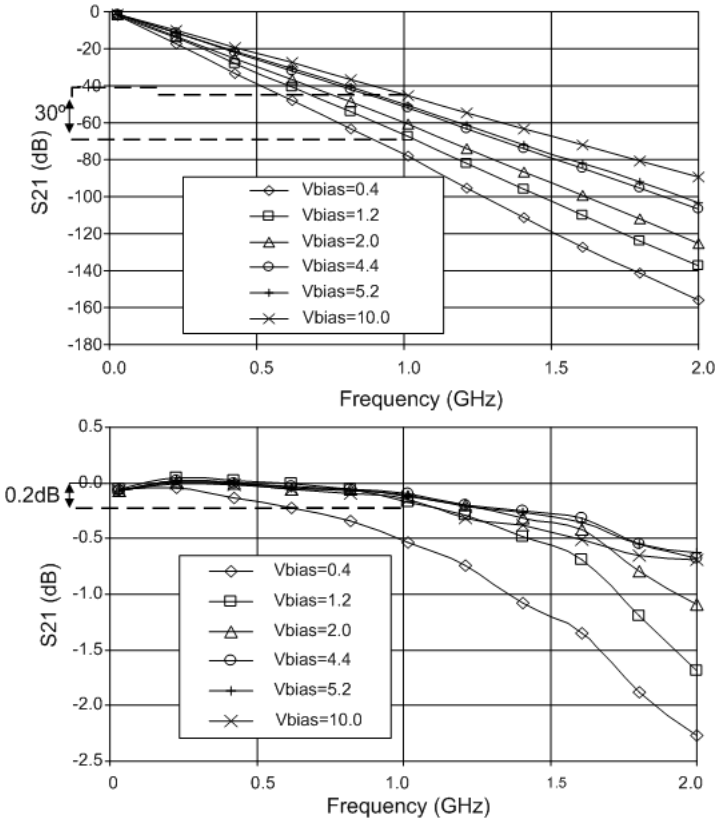


**Figure 7.16:** *The measured phase and magnitude of the differential $S_{21}$ of the implemented phase-shifter for different reverse bias voltages*

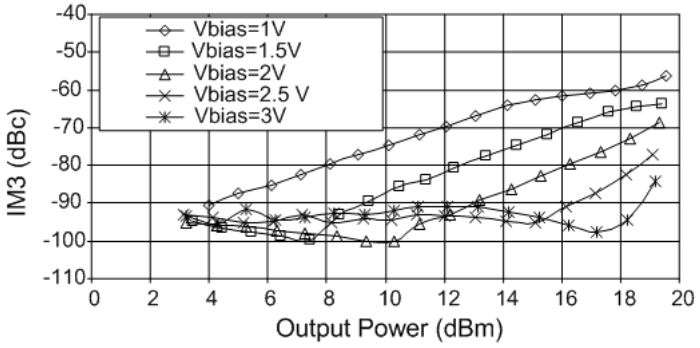


**Figure 7.17:** *Measured $IM_3$ ($\Delta$ f=10MHz RFfreq= 2.14GHz) of the differential phase shifter*

## 7.5 Conclusions

This chapter gives directions for the optimal design of compact true-time-delay phase shifters. Proper selection of the impedance level and use of differential operation proved to be effective measures to reduce the chip area required.
The use of the anti-series diode topology in combination with an ultra low-loss silicon-on-glass technology, high bandwidth and a compact area-optimized phase-shifter has been realized, which exhibit an unprecedented linearity of IP3 $>$ 45dBm making this phase shifter concept applicable to various demanding applications.

Chapter 8

# Conclusions and Recommendations

## 8.1 RF Power Amplifiers

In this thesis we have explored different multi-path RF Power Amplifier architectures for efficient and linear amplification of the modern base-station communication signals. Based on the discussions and results in the previous chapters we draw the following conclusions.

### 8.1.1 Conventional Outphasing Amplifiers

Outphasing is an interesting concept for basestation transmitters as it can combine high average efficiency and linearity [10]. In its original concept, the linearity of the output signal does not depend on the linearity of the branch amplifiers, thereby enabling linear amplification using non-linear active devices. Due to this property, this technique is also known as LINC (linear amplification using non-linear components). Although linear, the average efficiency of a traditional LINC outphasing amplifier is limited. By using the outphasing principle together with a Chireix power combiner, load modulation of the active devices in the branch amplifiers is achieved, yielding an improved average efficiency. This comes at the cost of a somewhat degraded linearity due to the non-isolating Chireix power combiner. Another property of outphasing is its capability to provide a relatively large high-efficiency wideband operation, since is no impedance inversion is required for its basic operation (as compared to the Doherty technique).
In spite of the above mentioned advantages, the application of outphasing in base-station transmitters is still very limited. The main reason for this is that it relies on the use of very high load modulation offered to the PA devices in the branch amplifiers. This makes the amplifier's performance sensitive to non-

idealities. For example, in order to efficiently amplify 3G WCDMA signals, the PA devices in an outphasing transmitter need to operate efficiently at load modulation ratios as high as a factor 8. The most commonly used devices of today (e.g. LDMOS), can only operate efficiently at load modulation ratios up to a factor 3, after which their performance starts to degrade. Consequently, the expected efficiency improvement when introducing outphasing is in practice overwhelmed by the related internal losses of practical PA devices when operating them at such a high load modulation ratio. Other high-efficiency power amplifier concepts like 2-Way and 3-Way Doherty amplifiers do not operate their devices beyond a load modulation of 3 for a similar efficiency versus power back-off characteristic. Although some advanced GaN devices can operate reasonably well at these high load modulation conditions, their performance drop is still quite significant.
Moreover, even with ideal transistor devices, the conventional outphasing concept is not suitable for 4G signals, which can have peak-to-average power ratios beyond 12dB. This is due to the rapid efficiency drop after the high efficiency back-off point and the dip in the efficiency characteristics between the two high efficiency points.
Another limitation of the outphasing concept comes from the input signal splitter. Outphasing uses a rather complex input signal splitter, which converts the amplitude modulation of the input signal into phase modulation. During this process some trigonometric operations are applied, which severely expands the modulation bandwidth of the input signals for the branch amplifiers. This modulation bandwidth expansion not only limits the maximum modulation bandwidth of the outphasing transmitter, but also introduces memory effects which complicates the pre-distortion of the outphasing PA. Moreover, the input signal splitter cannot be implemented with passives only, and additional digital or analog components are needed for its implementation, thereby increasing the complexity and cost of the outphasing transmitter.
In short, conventional outphasing transmitters provide only a moderate efficiency, high complexity, and are very sensitive to the losses of the PA devices. However, their basic concept does promise good linearity with improved efficiency, alongwith the potential of being wideband. These are important advantages which cannot be neglected, and have justified new research to overcome these drawbacks.

### 8.1.2 The Mixed-Mode Outphasing Concept

In this thesis an improved version of the outphasing amplifier is presented which is named as mixed-mode outphasing amplifier (Chapter 3). It used outphasing at higher power levels, while at lower power levels it operates in class-B mode. This switchover to class-B operation has a number of advantages which are listed in the following text.

The efficiency at deep back-off power levels is increased, as the very steep

roll-off of efficiency versus outphasing beyond the $2^{nd}$ high efficiency point is now replaced with the much lower efficiency roll-off of a class-B amplifier. This modification results in an increase in the average efficiency of 10% to 15% for 3G-WCDMA signals. Another benefit is that the load modulation of the PA devices is limited, as beyond the transition from outphasing to class- B the loading conditions of the devices in the branch amplifiers remain constant. Due to this lower load modulation, the performance of the mixed-mode outphasing transmitter is now less dependent on the non-idealities of the devices. Additionally, the bandwidth expansion of the PA devices is drastically limited and the power gain of the outphasing transmitter is also improved. The idea of mixed-mode outphasing was verified by the design of a prototype transmitter which indeed showed 10% to 15% efficiency improvement for WCDMA 3G signals over the conventional outphasing transmitter [16]. However, the benefits mentioned above come at the price of a slight increase in the complexity of the input power splitter and the loss of the LINC operation. But in general, the proposed mixed-mode outphasing amplifier with improved input signal conditioning shows superior performance over conventional outphasing transmitters.

### 8.1.3 The Adaptive Outphasing Concept

The efficiency of the out-phasing system can be further increased if the mixed-mode signal splitting techniques are combined with an adaptive matching network as power combiner (Chapter 4). The classical outphasing transmitter shows low efficiency at the mid back-off levels especially if the compensation power levels are chosen at more than 10dB back-off from full power (which is usually required for modern communication signals). By using adaptive susceptance compensation it is possible to improve the efficiency at mid back-off levels and obtain flat efficiency versus output power in the back-off characteristics. However, the losses of the adaptive matching network along-with the losses of the PA device can quickly overwhelm the potential improvements. This effect was also visible in the prototype circuit presented in Chapter 4, where the losses of the diodes limited the achieved average efficiency for a CDMA IS95 signal to 50%. However, when using a low-loss technology for the tunable matching network this technique has potential of providing a higher average efficiency than mixed-mode outphasing or Doherty operation, while the adaptive susceptance compensation enables multi-band multi-mode operation.

### 8.1.4 The Current state-of-the-art in Outphasing

The performance of recent state-of-art outphasing amplifiers is summarized in the table 8.1.

| WCDMA Test Signal | $P_{out}$ (W) | $\eta_{drain}$ | $\eta_{PAE}$ | ACLR1,2 (dBC) | Ref |
|---|---|---|---|---|---|
| PAR=7.5dB | 6.5 | 42.2% | —% | -35.9, -34.4 | [90] |
| PAR=7.5dB | 19 | 65.1% | —% | -47,-54 | [91] |
| PAR=9.6dB | 19 | 54.5% | —% | -47,-52 | [91] |
| PAR=9.6dB | 90 | 50.5% | 49.5% | -47,-52 | This Work |

**Table 8.1:** *Comparision of state of the art outphasing transmitters*

Note that the realized mixed-mode 90W outphasing amplifier provides significant efficiency improvements over earlier outphasing implementations, with an outstanding average PAE $\eta_{pae}$ of 49.5% for a 9.6dB PAR WCDMA signal.
One can observe from the table that the very recently published advanced compact 20 W outphasing amplifier [91], which makes use of a dedicated high-voltage CMOS driver IC, provides a very high average drain efficiency (see table). However, since this latter amplifier uses pure switching for its outphasing operation, it compromises a bit on its gain in power back-off operation. This fact reduces to some extent the (still very good) line up efficiency to 52% for a 7.5 PAR WCDMA signal, a performance number that appears to be in the same range to what can be reached with the mixed-mode demonstrator developed in this work. The work of [91], however, preserves pure outphasing operation, a fact that might have some impact on future basestation implementations, as we will discuss in our recommendations for future research.

### 8.1.5 Wide-band Doherty Power Amplifier

Doherty amplification is another technique for improving the efficiency of the RF Power Amplifiers that operate with complex modulated signals. Its high efficiency, low load-modulation ratio and low complexity makes it a very popular choice amongst basestation transmitter manufacturers. However, the needs of basestation manufacturers are now shifting towards larger bandwidths alongwith higher efficiency for future 4G transmitters. Unfortunately, traditional Doherty amplifiers are inherently narrowband due to the quarter wave transmission line (QWTL) used in the output power combining network, which provides only perfect impedance inversion at one frequency. Currently, the typical efficiency bandwidth of Doherty PAs is limited to 10% to 15% [12]. Although the common belief is that the QWTL is the main cause of this bandwidth restriction, the analysis done in Chapter 5 indicates that the bandwidth of the DPA should be around 30% if only the frequency dependence of the QWTL is considered. The root cause of the very narrow RF bandwidth in practical implementations is found in the large output capacitance of the PA devices. Therefore, as a first step in improving the bandwidth of the DPA, a DPA circuit was designed in which the output capac-

itances of the PA devices were absorbed in the QWTL forming a quasi-lumped QWTL. The prototype demonstrated an efficiency bandwidth of 25%. The bandwidth restriction beyond that value (25%) is entirely due to the QWTL forming the impedance inverter. Therefore, effort was made to also improve the bandwidth of the impedance inverter as a next step. There exist network structures which can provide a relatively wideband impedance inversion behavior. Therefore, another prototype circuit was designed using one of these novel wideband impedance inverters along-with an output capacitance compensation technique. The simulation results of this prototype are very promising, showing 40% efficiency bandwidth. This DPA high-efficiency bandwidth can further be increased to around 90% by using another novel wideband impedance inverter which utilizes a coupled-line structure. The practical implementation of these structure however, poses some serious realization problems, therefore further research is needed in this area.

### 8.1.6 High Linearity Phase-Shifters

Phase-shifters are basic building blocks for phased-array antennas, which currently have wide application in military systems, and hold future promises for the civil sector as well in terms of increased data throughput and improved link budget. Since phase-shifters are part of the RF front-end, their losses as well as their linearity are very important. Moreover, the requirement of a large bandwidth also imposes constraints in terms of phase linearity over the frequency range of interest.

There are various ways to design a phase-shifter. Some examples are, all-pass networks [80] or loaded TL type networks [30]. The all-pass networks tend to be narrowband and have a non-linear phase versus frequency response. For this reason the loaded TL type phase-shifter topology was selected in Chapter 7 to implement low-loss high linearity phase-shifters.

A loaded TL type phase-shifter is made of several sections of lumped LC networks, which results in a lumped transmission line equivalent. However, the optimal number of segments required to implement a phase-shifter with a certain tuning range and bandwidth was not clearly known. The analysis presented in the Chapter 7 relates the number of segments to the various parameters of the phase-shifter, namely: area, loss, linearity and bandwidth. As such, the optimal number of segments for the phase-shifter for a certain application can be determined. The theory presented in this chapter was verified by the design of a compact phase-shifter which showed extremely low-loss in combination with wide tuning range, high linearity and wide bandwidth. To demonstrate the effectiveness of the proposed phase-shifter design techniques and technology presented in the Chapter 7, the performances of several state-of-the-art phase-shifter implementations found in literature are given in the table 8.2.

| Frequency | Technology | $\frac{\Delta\phi}{dB}$ | IP3 | Ref |
|---|---|---|---|---|
| 5.2GHz | MESFET | $90^o$ | NA | [92] |
| 3-5GHz | MESFET | $63^o$ | NA | [81] |
| 2.4GHz | MESFET | $65^o$ | NA | [93] |
| 1.0GHz | Schottky | $150^o$ | 45dBm | This Work |

**Table 8.2:** *Comparision of state of the art diode and MESFET based phase shifters*

## 8.2 Future Work and Recommendations

The research presented in this thesis can act as a basis for further research in the areas of multi-path power amplifier design and true time delay phase shifters. In the following we give some suggestions / directions that might be useful in future investigations.

### 8.2.1 Mixed-Mode Outphasing Amplifiers

The mixed-mode outphasing amplifier demonstrator presented in Chapter 3 uses saturated class-B power amplifiers. These amplifiers are (theoretically) limited to a peak efficiency of 78.5%, yielding to the conclusion that the use of one of the 'linear' high-efficiency classes, like class-F can be applied in the mixed-mode outphasing concept to further enhance the average efficiency of the overall amplifier. Another improvement which can be made to the mixed-mode outphasing amplifier concept is to replace the output power combiner by the wideband power combiner presented in [94], which does not only simplifies the design of compensation elements but would results in better RF bandwidth.
When aiming for pure outphasing operation, the recently applied class-E branch amplifiers with duty-cycle control [18] can offer certain advantages in terms of drain efficiency and RF operating bandwidth. Important, however, for this approach is access to a high-gain device technology, which also offers low losses at high load impedance tuning ratios. Although pure outphasing is known to be sensitive to mismatches in the branch amplifiers and therefore might require additional calibration or feedback control loops, there are a few basic aspect of pure outphasing that are not always recognized, but might be of importance to future generations of low-cost, high data rate basestations. First of all, it is the digital nature of the outphasing PA drive, which allows cheap and easy system integration with the signal processing part of the basestation system. Secondly and this might be even more important, the outphasing amplifier is operated as a switching system. Consequently, no cascading of linear gain blocks is present in the system. As such the noise floor will not be lifted by the same amount as in a traditional 'linear' basestation. This reduced noise floor at the output, combined with the very clean spectral output of the outphasing amplifier, opens up the pos-

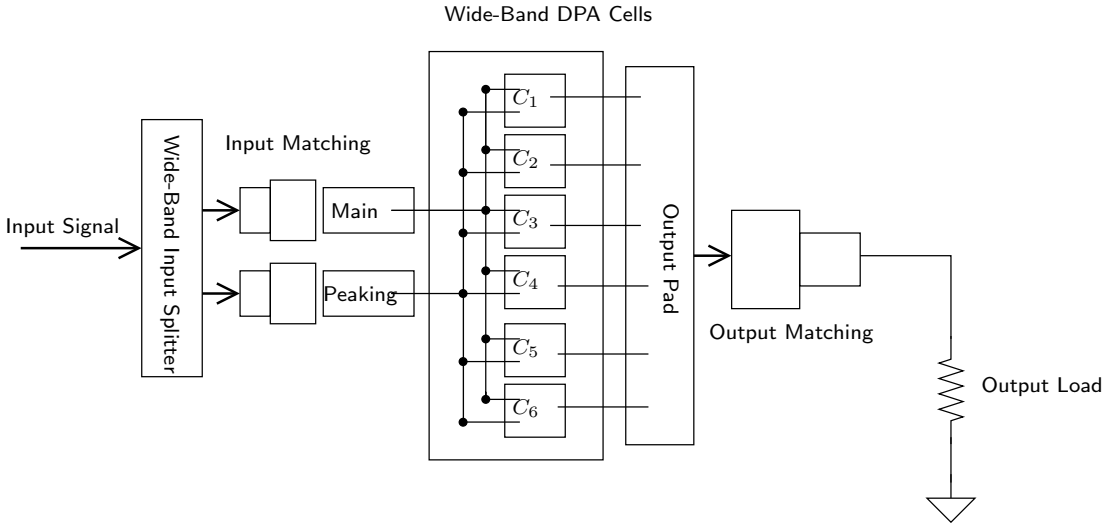


**Figure 8.1:** *High-power Wideband DPA using subcell power combining*

sibility to reduce the very stringent filter requirements in the basestation. This might yield major cost savings and simplification of the basestation hardware in the future.

### 8.2.2 High Power Wideband Doherty Power Amplifiers

The main purpose of the wideband DPA circuits presented in this thesis is to demonstrate the underlying bandwidth restrictions of current DPA implementations and prove the effectiveness of the wideband Doherty design concepts introduced. However, a useful Doherty power amplifier for today's basestation applications has an output power of at least a few times the output powers of these demonstrators. Unfortunately, the techniques presented in this thesis cannot be directly applied to truly high-power Doherty amplifier implementations (e.g., $>$ 100W) due to practical implementation constraints. However, constructing smaller wideband DPA cells, and then combining the resulting output powers of these wideband cells into a wideband load [95] (as shown in the Figure 8.1), provides a new route to high-power wideband DPA operation. Note that the package integration of the input power splitter is still a challenge in such a configuration. Implementing an input power splitter that can provide the required power and phase relations while keeping the main and peaking PA devices isolated from each other is very difficult. However if one brings the inputs of the peaking and the main devices outside the package, wide-band DPA operation can be achieved by

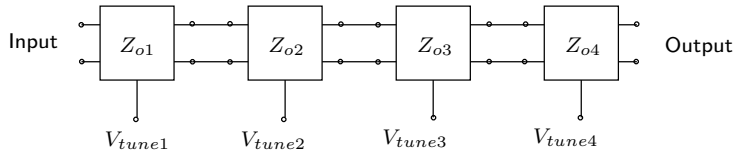


**Figure 8.2:** *Load transmission line type phase-shifter with non-identical segments*

using a wideband input power splitter along with a phase compensator. Even wider bandwidths and better DPA operation is possible if the input powers and phase relations are controlled using the digital Doherty techniques as presented in the Chapter 5.

### 8.2.3 Impedance Matched True-Time Delay Phase-Shifters

The ideas presented in the Chapter 7 can be extended to form true-time delay phase-shifters for future MIMO antenna systems. The phase-shifters presented in the Chapter 7 consists of identical lumped transmission line section, whose phase is varied by changing only the shunt capacitors. The disadvantage of this approach is that, the impedance of the structure also changes , as the tuning voltages of the varactors are varied for changing the delay of the structure, thereby increasing its reflection loss. One approach to solve this is to design a number of tunable lumped transmission lines with different characteristic impedances and different tuning control voltages (see Figure 8.2). The separate control of the tuning of each section enbles the operator to keep the characteristic impedance of the full structure constant, or nearly constant, during the whole phase tuning range over a very large bandwidth. In this way, the reflection loss and hence the performance of the structure can be significantly enhanced. This technique would have an adverse effect on the chip area and tuning range of the structure, but in turn it will provide a significantly better performance in terms of impedance match over the whole control range, and therefore also a much more predictable group delay.

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# Summary

The efficiency of the RF transmitter has always been a big concern in telecommunication systems. The increased popularity of complex modulating signals with high peak-to-average power ratios, has drastically increased the need for high efficiency, while yielding additional constrains on the linearity. Currently, the new generation of telecommunication systems seems to aim for multi-channel / multi-standard operation, this not only to save energy, but also to save on component costs, maintenance and (board) space. The main system component, hindering this development is the high-power RF amplifier, which now not only needs to be efficient, but also should support the simultaneous operation of multiple frequency bands with large video bandwidth, this to accommodate multi-carrier signals. Traditionally, concepts like Doherty, Outphasing, Envelop Tracking (ET) can provide high efficiency, however they tend to fail in providing high RF and video bandwidth simultaneously.

This thesis presents the analysis of various power amplifier architectures and evaluates their performance parameters in terms of gain, efficiency, video and RF bandwidth. Two popular PA configurations are discussed in detail, namely; the outphasing and Doherty amplifier. In chapter 2 conventional outphasing transmitters are evaluated for their performance in relation to the losses of the branch PA devices. From these results it is concluded that conventional outphasing PAs suffer from relative low-gain, yielding low power-added-efficiency for modulated signals with high peak-to-average power ratios. Also their video bandwidth and sensitivity to the losses in the branch amplifiers are points of concern. Following Chapter 3 an improved version of the outphasing transmitter is presented, which is referred to as the "Mixed-Mode Outphasing Amplifier". This modified outphasing concept overcomes most of the previously mentioned shortcomings by making use of intelligent input signal conditioning of the branch amplifiers. The concepts introduced in this Chapter are verified by a 90-W mixed-mode outphasing amplifier design, which was measured both in pure outphasing as well in mixed-mode oper-

ation to demonstrate the performance improvement. The achieved improvement with this demonstrator PA was a 10% higher average efficiency in mixed-mode of operation compared to conventional outphasing operation. In spite of this significant improvement, additional analysis indicated that using this new approach, the maximum attainable efficiency for signals with high peak-to-average power ratios (e.g. $>$ 12dB) is still below 60% (assuming class-B operation for the PA devices). This limit is mainly caused by the lower CW-efficiency at the mid power levels when the compensation angle is pushed to more extreme values in order to position the back-off peak efficiency at a relative low power level. One solution to this problem is the use of adaptive compensation in the Chireix power combiner instead of the traditional fixed compensation. Using this approach, high efficiency is not only achieved at 2 fixed compensation points but also at all other (mid) power levels. This dynamic compensation technique is presented in the Chapter 4, along-with an analysis for the impact of losses in the PA devices and adaptive network. These ideas are demonstrated by a 0.5 power amplifier operating at 870MHz, and tested with a CDMA signal. The achieved results of this later demonstrator indicate that, to have a significant improvement over the mixed-mode outphasing PA, the losses of the PA devices, as well as the losses of the adaptive matching networks need to be kept low. Moreover, high Q-tunable elements with high breakdown voltage are required to bring this concept to the power levels of macro-cell base-station amplifiers.

Another, very popular PA concept in the RF base-station industry is the Doherty PA, almost all modern high-average efficiency base-stations transmitters use this PA concept to increase the average efficiency. It are the simplicity and performance of this architecture that makes it the favorite among base-station transmitter designers. However, these days along-with its average efficiency also the bandwidth of the transmitter is becoming important. In view of this, traditional Doherty PA implementations are known to have very narrow bandwidths along-with being efficient. In fact the actual bandwidth capabilities of Doherty PAs are not very well known. It is the common belief that the output power combiner is the cause for this narrow bandwidth. In Chapter 5 the bandwidth of the DPA is analyzed reveling some interesting conclusions. One of these conclusions is that the Doherty PA can indeed provide an operational bandwidth of close to 28% (allowing 10% efficiency drop at the band edges). In practical situations this bandwidth can be obtained if the matching of the PA devices is done in a clever way (e.g. by absorbing the output capacitances of the devices in the power combiner). These ideas were verified through the design of a 20-W wideband LDMOS Doherty amplifier, which provided a 20% efficiency bandwidth, which at that time (June 2010), was the best result ever published. The analysis of the Chapter 5 is further extended by including some interesting wideband impedance inverter structures which in principle can provide a fractional bandwidth between 40% to 90%. One of those structures was chosen to demonstrate an ultra-wideband Doherty with a measured efficiency bandwidth of 42% for a 15-W LDMOS Doherty PA. The results of the Chapter 5 can be considered as very interesting since

they reject the commonly believed hypothesis that Doherty PAs cannot be made wideband. As such they presents some techniques that can form the basis of ultra-wide band Doherty amplifiers.
All PA demonstrators presented in this thesis make use of a dual input. To demonstrate the usability of these multi-path PAs, a dedicated pre-distortion method was implemented which is based on constellation mapping. This algorithm was chosen as it is simple while providing sufficient linearization to demonstrate the successful pre-distortion of these amplifiers. Chapter 6 explains the implementation and basic functioning of this algorithm. With the continuously rising energy costs, telecommunication industry is no longer only improving the efficiency of the broadcasting power amplifiers, but also aims to improve the antenna operation of future basestation systems. Instead of broadcasting radio waves in all directions, transmission ideally only takes place in the direction where the actual user(s) are located. The enormous energy saving potential is pushing the construction of low-cost phase array antennas, which would facilitate the broadcast transmissions only in the desired direction(s). One vital component of such system is a low-cost, highly-linear low-loss phase-shifter. Chapter 7 is devoted to the development of such an ultra-linear phase-shifter, which can enable these future developments.

# Samenvatting

Titel: Hoog efficinte RF vermogensversterker architecturen De efficintie van de RF-zender is nog altijd een groot probleem in telecommunicatiesystemen. De toegenomen populariteit van gemoduleerde signalen met een hoog piek-gemiddelde vermogensverhouding, vergroot de noodzaak van hoge efficintie en vereist tegelijkertijd een goede lineariteit. Op dit moment lijkt de nieuwe generatie telecommunicatiesystemen aan te sturen op "multi-channel / multi-standard" functionaliteit, dit niet alleen om energie te besparen maar ook om te besparen op kosten voor onderdelen, onderhoud en de afmetingen van een basestation. Het belangrijkste onderdeel van het systeem dat deze ontwikkeling belemmert, is echter de hoogvermogens RF-versterker. Die moet nu niet alleen energiezuinig zijn maar tegelijkertijd ook een aantal frequentiebanden kunnen bedienen om meerdere draaggolven simultaan uit te kunnen zenden. Traditionele hoog efficinte versterkerconcepten zoals, Doherty, "Outphasing" en "Envelope Tracking" (ET) kunnen wel een goed rendement garanderen maar falen in het gelijktijdig ondersteunen van een grote RF-bandbreedte als wel video bandbreedte.
Dit proefschrift presenteert de analyse van verschillende versterkerarchitecturen en evalueert hun prestatieparameters in termen van versterking, rendement, video en RF-bandbreedte. Twee populaire PA configuraties worden uitvoerig behandeld, namelijk; de Outphasing en Doherty versterker. In hoofdstuk 2 worden conventionele Outphasing zenders beoordeeld op hun prestaties m.b.t. de verliezen van de transistors in de versterkertakken. Deze resultaten leiden tot de conclusie dat conventionele outphasing methodiek gekenmerkt wordt door een relatief lage versterking, welke leidt tot een lage efficintie voor het toegevoegd vermogen (PAE) wanneer men werkt met gemoduleerde signalen met een hoog piek-gemiddelde vermogensverhouding. Ook de videobandbreedte en gevoeligheid voor de verliezen in de versterkertakken zijn punten van zorg. In het daarop volgende hoofdstuk 3 wordt een verbeterde versie van de Outphasing zender gentroduceerd, die wordt aangeduid als de "Mixed-Mode Outphasing Versterker". Dit gemodificeerde out-

phasing concept ondervangt de meeste van de eerder genoemde tekortkomingen door gebruik te maken van intelligente conditionering van de ingangssignalen voor de twee versterkertakken. Het verkregen inzicht is gecontroleerd aan de hand van een 90-W Mixed-Mode Outphasing versterker, die gemeten is in zowel outphasing operatie alsmede in mixed-mode operatie om de prestatieverbeteringen te kunnen aantonen. De bereikte verbetering met deze demonstratieversterker voor gemoduleerde signalen, is een 10% hoger rendement in mixed-mode operatie vergeleken met conventionele outphasing. Ondanks deze belangrijke verbetering toont aanvullende analyse aan dat met deze nieuwe aanpak, het maximaal haalbare rendement voor signalen met hoge piek-gemiddelde vermogens verhouding (bv. $>$ 12 DB) nog steeds beperkt is tot 60% (onder de veronderstelling dat klasse-B werking voor de PA transistor is gebruikt). Deze grens wordt voornamelijk veroorzaakt door het lage CW-rendement voor tussenliggende vermogensniveaus wanneer meer extreme waarden van de compensatiehoek worden gebruikt om het rendement bij lage vermogens te verbeteren. Een potentile oplossing voor dit probleem is het gebruik van dynamische Chireix compensatie in plaats van statische compensatie. Met behulp van deze nieuwe methode is de hoge efficintie niet langer beperkt tot 2 vaste vermogensniveaus maar ook sterk verbeterd bij alle andere vermogensniveaus. De techniek voor dit dynamisch compenseren wordt gepresenteerd in hoofdstuk 4, samen met een analyse van de gevolgen van verliezen in de vermogenstransistors en het verstelbare aanpassingsnetwerk. De haalbaarheid van deze ideen wordt aangetoond door een 0,5W versterker met een ontwerpfrequentie van 870MHz en zijn getoetst met een CDMA signaal. De resultaten met dit demonstratiemodel tonen aan dat om een significante verbetering te realiseren ten opzichte van de mixed-mode Outphasing PA, de verliezen van de vermogenstransistors alsmede de verliezen van de verstelbare aanpassingsnetwerken laag moeten worden gehouden. Bovendien zijn verstelbare componenten met een hoge doorslagspanning en lage verliezen nodig om dit concept op het energieniveaus van een macro-cell basestation te implementeren.

Een ander, zeer populair versterker concept in RF basestations is de Doherty PA, bijna alle moderne basestations zenders maken gebruik van deze PA architectuur om de energie-efficintie voor de versterking van gemoduleerde signalen te verbeteren. Het zijn de eenvoud en prestaties van deze architectuur die het tot de favoriet maken van vele basestation ontwerpers. Echter, naast de gemiddelde efficintie wordt tegenwoordig ook de bandbreedte steeds belangrijker. Van traditionele Doherty PA implementaties is echter bekend dat ze een zeer smalle bandbreedte hebben waarin ze efficint zijn. In werkelijkheid zijn de bandbreedte mogelijkheden van Doherty DAH niet erg goed onderzocht. Op dit moment is de algemene overtuiging dat de uitgangsvermogencombiner de oorzaak is voor deze bandbreedte beperking. In hoofdstuk 5 wordt de bandbreedte van de DPA geanalyseerd welke leidt tot een aantal interessante conclusies. En van deze conclusies is dat de Doherty versterker in staat is tot een operationele bandbreedte van bijna 28% (waarbij een 10% efficint reductie wordt getolereerd). In praktische schakelingen kan deze bandbreedte alleen worden verkregen als de matching

van de transistors wordt uitgevoerd op een slimme manier (bijvoorbeeld door het absorberen van de uitgangcapaciteiten in de vermogenscombiner). Deze ideen zijn geverifieerd d.m.v. een 20-W wideband LDMOS Doherty versterker, welke een 20% efficintie bandbreedte behaalt. Op dat moment (juni 2010) was dit het beste resultaat ooit gepubliceerd. De analyse van hoofdstuk 5 is verder uitgebreid met enkele interessante wideband impedantie inverter structuren, die in theorie kunnen zorgen voor een relatieve bandbreedte van 40% tot 90%. En van deze structuren is gekozen om een zeer breedbandige 15-W LDMOS Doherty te maken met een gemeten relatieve bandbreedte van 42% voor de efficintie. De resultaten van hoofdstuk 5 kunnen worden beschouwd als zeer interessant omdat ze strijdig zijn met de algemene hypothese dat breedband Doherty vermogensversterkers niet mogelijk zijn. Aldus presenteert hoofdstuk 5 enkele technieken die de basis kunnen vormen voor een nieuwe generatie breedbandige Doherty versterkers.
Alle vermogensversterkers gepresenteerd in dit proefschrift maken gebruik van een dubbele ingang. Om aan te tonen dat deze versterkers met meerdere ingangen en versterkingstakken inderdaad bruikbaar zijn, is er een speciale correctiemethode toegepast voor de ingangssignalen die gebaseerd is op “constellation mapping”. Dit algoritme is gekozen omdat het op eenvoudige en tegelijkertijd afdoende wijze de benodigde linearisatie geeft van deze versterkers. Hoofdstuk 6 behandelt de implementatie en de werking van dit algoritme.
Met de voortdurend stijgende energiekosten streeft de telecommunicatie-industrie niet langer alleen naar de verbetering van de zendversterkers maar ook naar de verbetering van complete antennesystemen van toekomstige basestations. In plaats van de radiogolven in alle richtingen uit te zenden, vindt in het ideale geval de transmissie uitsluitend plaats in richtingen waar de gebruikers zich daadwerkelijk bevinden. Deze enorme mogelijkheden voor energiebesparing sturen de ontwikkeling van goedkope en slimme antenne arrays, die selectieve uitzending in alleen de gewenste richtingen inderdaad mogelijk maken. Een essentieel onderdeel van zo?n dergelijk systeem is een goedkope, lineaire fasedriaar met lage-verliezen. Hoofdstuk 7 bespreekt de ontwikkeling van een ultra-lineare phase draaier die deze toekomstige ontwikkelingen kan ondersteunen.

# List of Publications

## Journal Papers

- E. Neo, **J.H.Qureshi**, M. Pelk, J.R. Gajadharsing and L.C.N. deVreede,"A mixed-signal approach towards linear and efficiency N-way Doherty Amplifiers",*IEEE Trans. in Microwave Theory and Techniques*, vol. 55, issue no. 5, May 2007.

- C. Haung, L.C.N. deVreede, F. Sarubbi, M. Popadic, K. Buisman **J.H. Qureshi**, A. Akhnoukh, T.L.M. Scholtes, L.E. Larson and L.K. Nanver, "Enabling Low-Distortion Varactors for Adaptive Transmitters",*IEEE Trans. in Microwave Theory and Techniques*, vo. 56, part 1, issue 5, 2008.

- **J.H. Qureshi**, M.J. Pelk, M. Marchetti, W.C.E., Neo J.R. Gajadharsing, M.P. Heijden and L.C.N. deVreede, "A 90-W peak power GaN outphasing amplifier with optimum input signal conditioning",*IEEE Trans. in Microwave Theory and Techniques*, vol. 57, issue 8, August 2009.

- S.J.C.H Theeuwen, **J.H. Qureshi**, "LDMOS Technology for RF Power Amplifiers", *IEEE Trans. in Microwave Theory and Techniques*, vo. 60 issue 6, June 2011.

## Conference Papers

- **J.H. Qureshi**, S.,Kim K., Buisman C., Haung, M.J. Pelk, A. Akhnoukh, L.E. Larson, L.K. Nanver and L.C.N. deVreede,"A low-loss compact linear varactor based phase-shifter ", *RFIC, MTT-S 2007 Honollulu USA*.

- **J.H. Qureshi**, R. Liu, A.J.M. de Graauw, M.P. Heijden, J.R. Gajadharsing and L.C.N. deVreede,"A highly efficient Chireix amplifier using adaptive power combining",*IMS, 2008, Atlanta, USA*.

- S. Kim, **J.H. Qureshi**, K. Buisman, L.E. Larson, L.C.N. deVreede,"A low-distortion low-loss varactor phase-shifter based on silicon-on-glass technology",*RFIC, June 2008, Atlanta, USA*.

- **J.H. Qureshi** L.Nan E. Neo F.R.Rijs I. Blednov and L.C.N. deVreede,"A wide-band 20-W LDMOS Doherty power amplifier", *IMS 2010, Anaheim , USA*

- L.C.N. deVreede, M.J. Pelk, E. Neo, **J.H. Qureshi**,M. Spirito, M. Squillante, M. Marchetti,"Enhanced RF power amplifier and device characterization setups using mixed-mode techniques", *WAMICON, April 2010, Florida, USA*.

- Haiying Cao, **J.H. Qureshi**, T. Eriksson, C. Fager, L.C.N. deVreede, "Digital Predistortion for dual-input Doherty power amplifier" *IEEE, PAWR, Santa Clara, USA, January 2012*

# Acknowledgments

Although I am the author of this Ph.D. dissertation, I would not have been able to complete it without the help of the following people;
First, I would like to thank Prof. John Long for putting his trust in me and being my promotor, it is a true honor for me to be one of his Ph.D. students. Special thanks goes to my co-promotor Dr. Leo de Vreede for giving me the opportunity to become part of this team, and supervising me in both my master and Ph.D. research. I must admit that when I started my masters project, I had almost no RF related knowledge. However, under his guidance I was able to develop myself to my current proficiency, which allows me to contribute to with this thesis to the state-of-the-art in RF PA design. Along-with being my teacher and co-promotor, he is also a tough squash partner. Although whenever he won, I use to say that "I let him win on purpose, since you are my supervisor and I still need to receive my Ph.D. degree", the truth is however, that he indeed played better than me..
I would like to thank NXP semiconductors for funding my Ph.D. project and providing me excellent technical guidance. In this context, one important name is John Gajadharsing of NXP's RF power & basestations PL, who really learned me a lot. I still remember the many hours of phone discussion related to the design of Doherty power amplifiers. In these long conversations he always carefully listened and answered all my stupid questions patiently. For this reason I see John Gajadharsing as one of my prime mentors during my Ph.D. study and I consider myself very lucky to receive such a good guidance from him. In addition to John, also a lot of help was received from Dr. Mark van der Heijden. With Mark I had numerous interesting discussions on outphasing amplifiers, which helped me to improve the outphasing demonstrator included in this thesis.
All circuits presented in this thesis needed characterization and therefore extensive use of the lab resources, for that I am very grateful to Atef Aknoukh who not only arranged and maintained the equipment in the RF laboratory, but also helped me to measure my RF-circuits. Moreover, Atef also acted as my "official" Dutch-to-

English translator, by not only translating the complicated Dutch letters, but also by explaining me the difficult Dutch taxations and housing rules. As such, I am very grateful for his steady support, and time.
Doing your Ph.D. in Delft is in my case not a lonely job, since I collaborated with numerous PhD students and people from industry to implement the ideas developed in this thesis. I have worked intensively with Edmund Neo on Doherty power amplifiers and benefited from his expertise on digital pre-distortion. I also teamed up with Koen Buisman while designing low-loss linear phase shifters. In my view, his open mind set makes him a true researcher and also a very nice friend. His wonderful "Distortion free varactor stack"(DFVS) varactors fabricated by Prof. Lis Nanvers group in Dimes enabled me to demonstrate state-of-the-art phase-shifters.One of the persons I admire most in the microwave group, is Marco Pelk. His support in preparing demo boards and his help in performing microwave measurements enabled me to obtain the experimental results that supported my research ideas. I can undoubtedly say that he is one of the best practical engineers I have ever worked with and I learnt lot of practical stuff from him, ranging from soldering components to the correct use of microwave equipment.
The major part of thesis write-up was done when I already started working at NXP Semiconductors. Therefore, I would like to thank Fred van Rijs, Rik Jos, John Gajadharsing, Robin Winson, Jordon Svcechtarov and Igor Blednov not only for supporting me during the write-up process, but also for the endless discussions related to power amplifier devices and circuits. It were these discussions, which helped me improve my knowledge and thesis write-up even more. After spending two years with such competent persons my understanding of PA devices and their ues in energy efficient PA circuits has been significantly expanded.
In addition to the people already mentioned, I had many other wonderful colleagues in Delft who made my work and life very pleasant. Namely, Mauro Marchetti, Cong Huang, Morteza Alwi, Michele and Marco Spirito and my close friends Amir Mehmood,Pedram Khalili, Omid Noorozian, Behnaz, Sharif ullah Khan, Umer Altaf, Shahzad Khan, Omer bin Youns, Saad Mirza, Kaleem , Zafar, Anser Saidan, Abdul Rehman for their wonderful companion-ship and helping me to survive socially during this long Ph.D. journey.
I would like end with thanking my family, In special my parents for providing the opportunity and resources to aim for a Ph.D. Degree in electrical engineering. It is only when you start raising your own children, that you realize how much effort your parents have put into us, for making us what we are now. I am also thankful to my brothers and sisters for supporting and helping me not only during this period but also in every happy or sad moment of my life. Finally, and most of all, I am thankful to my wife Abeera for her deep love and support over the last years. She had to tolerated many times my absent-mindedness when I was trying to multi-task family life with Ph.D. duties. Coming to the Netherlands to join me, also meant sacrificing her medical career, since in the Netherlands native Dutch skills and additional medical programs were demanded. I fully realize the offers she had to make for me and adore her for doing so..

# About the Author

Jawad Hussain Qureshi was born in 1976 in Multan, Pakistan. He received B.Sc in electrical engineering (with honors) from the university of engineering and technology Taxila, Pakistan in 2000. In 2000 he joined Communication Enabling Technologies, Islamabad Pakistan as system egnineer where he was involved in the design of hardware for VOIP based communication equipment. In 2002 he joined AERO (advanced engineering research organization) Pakistan, where he was involved in the designe of mixed-signal analog and digital hardware for communication systems. In 2006 he received masters degree (cum lade) in electrical engineering from technical university Delft (TUDelft). From 2006 till 2010 he worked in TuDelft as a Phd candidate working on high efficiency RF power amplifier architectures. In 2010 he joined NXP semiconductions, Nijmegen, Netherlands as an innovation engineer, where he is responsible for the development of high efficiency wideband RF power amplifier architectures for current and future microwave transmitters.