Radio-Frequency High-Voltage CMOS Drivers
for High-Efficiency Base-Station Power Amplifiers

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by

David Angel Calvillo Cortés

Thesis supervisors:

Ir. Mustafa Acar
Dr.-Ing. Mark P. van der Heijden
P.D.Eng. Melina Apostolidou

NXP Semiconductors Research
Eindhoven, The Netherlands

Dr.-Ing. Leo C.N. de Vreede

Delft University of Technology
Delft, The Netherlands

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Abstract

In base-station applications, there is a need of high-voltage CMOS drivers for cost and integration reasons. This is because RF power amplifiers (PA) for base stations are realized in dedicated transistor technologies, while Silicon CMOS is the technology of choice for digital/baseband blocks. Some of those PA technologies, like GaN HEMT, are wide bandgap semiconductors that require high-voltage swings (e.g. 5V) for their optimum input drive. Hence, this thesis investigates two approaches for implementing high-voltage (HV) CMOS drivers for such transistors in low-breakdown voltage baseline CMOS technology. In this work, TSMC 65-nm CMOS technology is employed in this work.

As a first approach, cascoding topologies are investigated. Class E has been used to preserve efficiency. The main efficiency loss mechanisms have been identified and two topologies are proposed: 3 and 4 stacked devices. Only standard devices has been used in this approach in order to be able to use the outcomes to other deep sub-micron CMOS technologies. More than 5.5 and 7.0V output swing has been reached with the 3 and 4 stacked devices topologies, respectively. The complexity increases and the efficiency reduces with the number of stacked devices. Deep N-Well and a dedicated biasing network were needed for the 4-device cascode. However, in spite of these efforts, other HV solutions employing special extended-drain (ED) devices outperformed the best results achieved by the cascode approach, showing than the use of those ED devices is advantageous for high-voltage/power applications.

The second approach consisted in exploring an inverter-base topology, employing the special ED devices available in the baseline 65-nm CMOS technology. Three CMOS drivers were designed, implemented and fabricated. CMOS drivers I and II employed novel thin-oxide ED devices, while CMOS driver III used thick-oxide ED devices. Additionally, pre-driver stages with standard thin-oxide devices were implemented in the CMOS driver I. The three CMOS drivers demonstrated the feasibility of a complete broadband and high-efficiency amplifier lineup bridging the gap between GaN and CMOS technologies. CMOS driver I reached the best performance due to its pre-drivers. The use of thick-gate oxide, in CMOS driver III, was found not to be optimum for the application due to its required high input power. Additionally, in view of the application, the drivers had duty-cycle control capabilities to enhance the efficiency. The CMOS driver I reached a duty-cycle range of 32 to 70% with a 5pF load, within a 2.1 to 2.7GHz bandwidth.

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Ing. David A. Calvillo
Eindhoven, The Netherlands
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Chapter 1

Introduction

1.1 Motivation

In modern cellular systems, power level, efficiency and linearity are key requirements for the design of power amplifiers (PAs). The PAs for handset applications must provide output powers up to 1-4 Watts, while the output power level for base-stations applications is substantially higher (50 to 600 W) [3].

In base-station applications, the RF power amplifiers are realized in dedicated transistor technologies (e.g. Si LDMOS, GaAs, GaN, InP) because of their superior break-down voltages, that translates in the higher output power levels required. Although at the moment LDMOS technology owns a significant part of the market (95%) for base-station applications, Gallium Nitride (GaN) is gaining interest [3]. The attraction of GaN technology is its substantially higher RF power density, due to its increased breakdown voltage, and higher current density. These factors in GaN devices enable power densities that are two to four times that of LDMOS and GaAs devices. However, GaN is a wide bandgap semiconductor optimized for high voltage (HV) applications, therefore this imposes special requirements on its driving circuitry.

Implementing the driver stages for GaN transistors in CMOS technology has cost and integration advantages; for example, it facilitates the use of digital techniques to improve system performance, or other digital blocks. However, driving GaN transistors using CMOS technology requires drivers able to withstand voltage swings in the order of 5V. Consequently, the implementation of these drivers is a big challenge in CMOS technology due to its limited breakdown

voltages and RF capabilities, which also limit the efficiency of the (pre-)driving stages. However, when implemented successfully, not only cost but also system functionality and system efficiency can be improved. By combining efficient amplifier designs with increased functionality offered by a CMOS driver chip, more complicated amplifier architectures such as Outphasing/LINC (LInear amplification using Non linear Components), Doherty, as well as others, can be further explored to overcome efficiency and linearity limitations.

1.2 Thesis Research Goal

The main objective in this thesis is to understand the feasibility and limitations in the design and implementation of high-voltage (HV) CMOS drivers for high-efficiency PAs in base-station applications. The target load of the CMOS driver is a broadband Class E GaN HEMT power amplifier.

The main challenge towards this objective is the low breakdown voltage of advanced sub-micron CMOS technologies, that in 65- and 45-nm CMOS is 1.2 and 1V, respectively. Designing power driver circuits that can sustain 5V swings reliably and efficiently is a big challenge. For our design study we have used the baseline 65-nm CMOS technology, from TSMC.

Two design approaches were explored as potential solutions to reach reliable high-voltage operation. First, a cascoding approach employing the Class E circuit topology, which provides high efficiency, was investigated. Second, an inverter-based driver approach was studied, which has a better wideband performance. This later approach can be considered as a Class D or Class DE like topology.

In the design of these driver circuits, use has been made of standard 65-nm CMOS devices, as well as novel high voltage devices. These later devices make use of a lightly doped drain extension to handle larger voltage swings than the standard devices. These extended-drain (ED) devices have been compared for their RF performance and design trade-offs when utilizing them in practical driver implementations.

1.3 State of the art review

To the best of the author's knowledge, there is very little published work on high-voltage CMOS drivers for compound semiconductors power amplifiers. In general, the published work is focused in demonstrating the capabilities of the power amplifiers themselves without considering the implementation of the driving stages.

The work in [4] demonstrates a Class S system that linearizes a switchmode power amplifier realized in GaAs pHEMT technology, for multi-carrier CDMA 2000 and WCDMA patterns, both at 874 MHz and 2.14 GHz. The system includes an integrated multi-stage broadband CMOS amplifier that drives the GaAs transistor. The CMOS amplifier is an inverter-based driver, fabricated in 0.18-μm technology. However, its swing is only 2V. Two volt swing is enough for GaAs, but it is insufficient for driving LDMOS and GaN [4].

The work in [5] shows a high-efficient and broadband (2.1 - 2.7GHz) Class-E GaN HEMT PA for base stations. It is concluded in that work, that square-wave input drive is required for a correct switching behavior of the GaN device in a class-E PA. Since that work did not implement a driver circuit, they made use of the nonlinear gate capacitance of the GaN HEMT and tuned the 2nd-harmonic at the input to shape the gate voltage drive waveform. The input power required to drive the PA in that work was 600mW (27.8dBm).

This thesis investigates the CMOS circuits that can drive PAs such as the one in [5], ensuring a reliable operation of the CMOS driver and maintaining the high-performance of the PA.

1.4 Thesis organization

Once the overall objective of this thesis has been established and the two main design approaches has been outlined, the rest of this document is organized as follows:

Chapter 2 - Background

An overview of basic concepts with respect to the content of this thesis is done in this chapter. We start with a brief description of the main performance parameters of PAs and drivers followed by a short review of all the amplifier classes. Then, the general Class E is introduced. Further details in this amplifier class can be found in two appendices: Appendix B (it presents

the complete analytical derivation of the General Class E model), and Appendix C (it extends the discussion about the general Class E model, including all its operating modes, and it presents a novel way to improve efficiency in back-off for broadband Class E power amplifiers by duty-cycle control). With the need of high voltage device operation in Class E exposed, an overview of the CMOS technology in the context of reliable HV operation is discussed. A description of the available standard and extended-drain devices in 65-nm CMOS technology is presented in Appendix A. Finally, ways to increase the voltage swing in drivers are given.

Chapter 3 - Class E cascoding approach for HV swings

The device cascoding approach towards HV CMOS driver circuits is presented in this chapter. It is based on Class E cascode topologies. In view of this, the efficiency loss mechanisms associated to the cascode topologies are discussed first. Then, two Class E cascode topologies based on standard devices in 65-nm CMOS are proposed. The Cadence Spectre simulation results of these circuits are presented. Then, a discussion is given between these simulated results and very recently published results of novel extended-drain HV CMOS devices, which have become recently available.

Chapter 4 - Inverter-based driver approach for HV swings, design and implementation

In this chapter, as alternative to the cascode Class E approach, an inverter-based CMOS HV driver topology is proposed and its target specifications are provided. Three inverter-based drivers have been implemented. The first two employed novel HV thin-oxide extended-drain devices, and the third CMOS driver employed thick-oxide extended-drain devices. At the moment of this thesis report, these devices are still under research.

All drivers were implemented in TSMC 65-nm CMOS technology and were sent to fabrication. These drivers have added functionality such as duty-cycle control to enhance the efficiency of the final PA stage, AC-coupling and -decoupling integrated capacitors to enhance their use in their final application.

Chapter 5 - Inverter-based CMOS drivers simulation results

The post layout simulation results for the CMOS driver I, II and III introduced in Chapter 4 are presented and discussed here. Those simulation results include the high-voltage operation

performance and the duty-cycle capabilities of the drivers. Also, simulations including the complete amplifier lineup, i.e. including the broadband Class E GaN power amplifier and the CMOS drivers, are presented. Finally, a comparison between the three CMOS drivers is performed.

Chapter 6 - Conclusions and recommendations

The main conclusions reached in this work are presented in this chapter. Additionally, suggestions for future work are provided along with some guidelines for their implementation.

Chapter 2

Background

2.1 Introduction

In this chapter, we mainly present background information about the area of this work. First, the main performance metrics and classification of power amplifiers are presented, with a focus on Class E. Then an overview of the most important reliability concerns when designing CMOS power amplifiers/drivers is provided. Finally, a discussion in the options to generate high-voltage swings is given.

2.2 RF power amplifier basics

A Power Amplifier (PA) is a key building block in the physical layer of any communication system. A PA is the last block in any transmitter chain and its goal is to provide the required output power to its load, an antenna. It can be composed of several cascaded stages (some of which could be cascoded, as it will be seen later) to boost the output power to the level required. In general, the stages before the output are called *drivers*. Drivers and power amplifiers share many features, and probably the only main difference is the load of each one. A driver will generally have a capacitive load (i.e. the input of another transistor) while the amplifier will have a real load (i.e. an antenna). Next, we discuss the main amplifier performance parameters which we will utilize in this work.

2.2.1 Main performance metrics

2.2.1.1 Power Gain

The (operating) power gain, G_P, of a PA is the ratio between the output power (i.e. the power delivered to the load[1]), P_{out}, and the driving input power, P_{in}. This is,

$$G_{P,dB} = 10\log_{10}\left(\frac{P_{out}}{P_{in}}\right) \tag{2.1}$$

2.2.1.2 Efficiency

The efficiency tells about how good or bad a PA is in converting DC power into RF output power, controlled by an RF input signal. There are several metrics to measure and report the efficiency of a PA [6].

The *Drain* (or *Collector*) *Efficiency*, η, is the ratio between the RF output power to the DC supply power, P_{DC}:

$$\eta = \frac{P_{out}}{P_{DC}} \tag{2.2}$$

If the gain of the amplifier is not high (as it is usually the case at RF) the driving input power will be significant and η will not properly describe the efficiency of the PA for not considering the driving input power level, P_{in}. The *Power Added Efficiency*, PAE, includes the driving input power by subtract it from the output power, this is:

$$PAE = \frac{P_{out} - P_{in}}{P_{DC}} \tag{2.3}$$

Notice that PAE approaches η for high values of G_P[2] and it could become negative if $G_P < 0dB$ since:

$$PAE = \frac{P_{out} - P_{in}}{P_{DC}} = \frac{1 - \frac{P_{in}}{P_{out}}}{\frac{P_{DC}}{P_{out}}} = \eta\left(1 - \frac{1}{G_P}\right) \tag{2.4}$$

[1] In this document, the output power will refer to the power delivered to the load at the fundamental frequency.
[2] For $G_P = 10dB \rightarrow PAE = 0.9\eta$; $G_P = 15dB \rightarrow PAE \approx 0.97\eta$; $G_P \geq 20dB \rightarrow PAE \geq 0.99\eta$

A more general metric is the *Overall Efficiency*, $\eta_{overall}$. This metric is always applicable and accounts for the DC power of the driving stages [6], $\sum P_{DC,drivers}$:

$$\eta_{overall} = \frac{P_{out}}{P_{DC} + P_{in} + \sum P_{DC,drivers}} \tag{2.5}$$

2.2.1.3 Linearity

Linearity of a power amplifier can be defined by its phase linearity and amplitude linearity. Phase nonlinearity or phase distortion is denoted as PM-PM distortion. Likewise, AM-AM denotes amplitude distortion. The varying envelope of the RF signal may also induce phase errors, indicated as AM-PM. Similarly, PM-AM are amplitude or envelope errors caused by the phase or frequency modulation of the carrier [7].

Linearity is characterized, measured, and specified by various techniques, depending upon the specific signal and application. Single and dual tone tests provide quick and rough information about the linearity of an amplifier, although the real performance is obtained when the amplifier is measured with the real modulated complex signal. The most widely used measure of linearity is the adjacent channel power ratio (ACPR), which compares the power in an adjacent channel to that of the signal [6]. Error vector magnitude (EVM) is a measure of the accuracy of the modulation of the transmitted waveform; it is a measure of the distance between the ideal and measured signal vectors.

2.2.2 Output power

A reliable operation of the transistors in any PA is a very important consideration. The *output power capability factor* (also called *transistor utilization factor*) [6] is a metric that measures the amount of output power deliverable from a PA when the transistor is operating under the technology's maximum reliable limits[3]. It is given as

$$C_P = \frac{P_{out,max}}{v_{DS,max} \cdot i_{DS,max}} \tag{2.6}$$

[3] Since the transistors used in PAs are in general among the most expensive components in the system, an optimum use of those devices close to their maximum capabilities has become mandatory in practical designs.

where $P_{out,max}$ is the maximum output power, $v_{DS,max}$ is the maximum (peak) voltage at the transistor's terminals, and $i_{DS,max}$ is the maximum current flowing through the transistor.

The output power delivered to a real load R_L by a PA is proportional to the square of the output voltage swing (drain-source voltage in the case of MOS transistors) and inversely proportional to the load itself. The output voltage swing is in turn directly proportional to the supply voltage V_{DD}; this is $v_{DS} = \overline{v_{pk}} \cdot V_{DD}$, where $\overline{v_{pk}}$ is the (unitless) proportionality factor. $\overline{v_{pk}}$ depends on the amplifier class of operation. Hence, the proportionality factor between P_{out} and V_{DD}/R_L will also be determined by the amplifier class of operation. This factor will be called K_P. Then, the output power of any 'PA class' can be written as:

$$P_{out_{\text{PA class}}} = K_P \cdot \frac{{V_{DD}}^2}{R_L} \tag{2.7a}$$

$$K_P = f\,(\text{PA class}) \tag{2.7b}$$

Note that the K_P factor can be seen as the output power level normalized with respect to the (square of the) voltage supply for a given load. This rather general quantitative definition of output power will help to make direct comparisons between all the amplifier classes that will be discussed in the next section.

However, observe that K_P does not state anything about the reliability of the PAs, as C_P does. K_P only states how much P_{out} will be generated from a given supply voltage, regardless of whether or not the voltage swing due to that supply voltage can be supported by the transistor in the PA. For this reason, the maximum output power level can also be normalized with respect to the *maximum reliable supply voltage*, that will be called $V_{DD,max}$, for a given load. This normalization will be done through a parameter that will be called κ_P. This last parameter can be very useful for switchmode-based power amplifiers[4], and it is introduced here as a tool to compare those amplifiers with the gm-based PAs. These two PAs types will be discussed in the next section.

[4] In CMOS, the reliability of switchmode PAs is more concerned with the limited breakdown voltage capabilities than with the maximum currents, as they scale directly with the number of parallel instances used to constitute the switching devices [8], while the limited voltage does not.

The κ_P factor will be defined from

$$P_{out,max} = \kappa_P \cdot \frac{{V_{DD,max}}^2}{R_L} \tag{2.8a}$$

$$\tag{2.8b}$$

Then, κ_P states the maximum output power $P_{out,max}$ obtainable with a supply voltage $V_{DD,max} = v_{DS,max}/\overline{v_{pk}}$ that always ensure a reliable voltage operation of the transistor in the PA. Observe that both K_P and κ_P are directly related, through $\kappa_P = K_P/\overline{v_{pk}}^2$.

2.2.3 PA classification

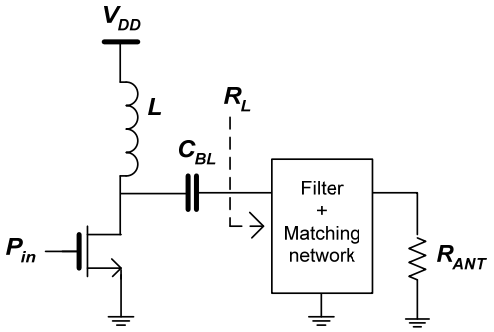
Power amplifiers can be mainly classified in two big groups [9]: transconductance-based (or gm-based) and switchmode-based. The familiar lettered classification (Class A, B, C, D, E, F, etc.) of PAs makes reference to amplifiers belonging to one of the two groups. Briefly, the first type of PA (gm-based) works as a high impedance *current source* while the second group (switchmode-based) works as a *switch* toggling between two opposite states: ON (or low-impedance) and OFF (or high-impedance). These very different behaviors have important implications in the design methodology and capabilities of such amplifiers.

The closed-form analysis of some of those amplifiers (specially of the switchmode ones) can be very complex, however a basic understanding of those two groups of amplifiers can provide valuable insight for PA and drivers design. A brief description of both types of PA will be given next for that purpose. For a complete and detailed description the reader is referred to more comprehensible works (e.g. [10–12]). This thesis deals with the drivers of switchmode-based PAs for base station applications, specifically Class E.

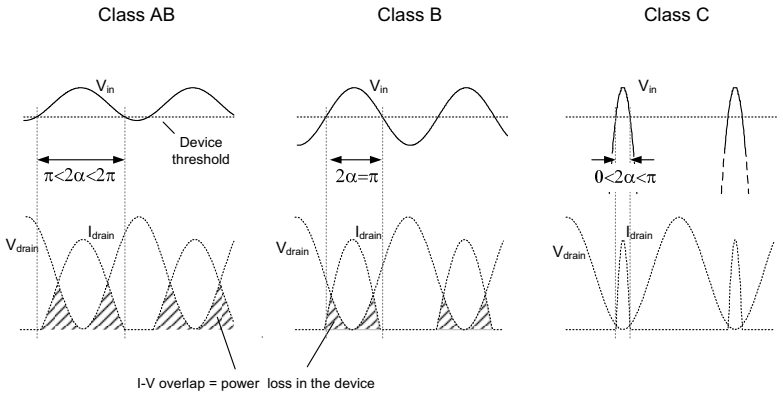
2.2.3.1 gm-based PAs

The transconductance-based PAs are designed with the assumption that they behave as high-impedance *current sources*. An input signal directly controls the output current waveform, and hence these groups of amplifiers are considered to be linear. This is, *there is a linear relationship*[5] *between the amplitude and phase* of the output and input signals.

[5] Class B and C could be considered nonlinear, but still there is some relationship between input and output.



(a) Generic power amplifier schematic



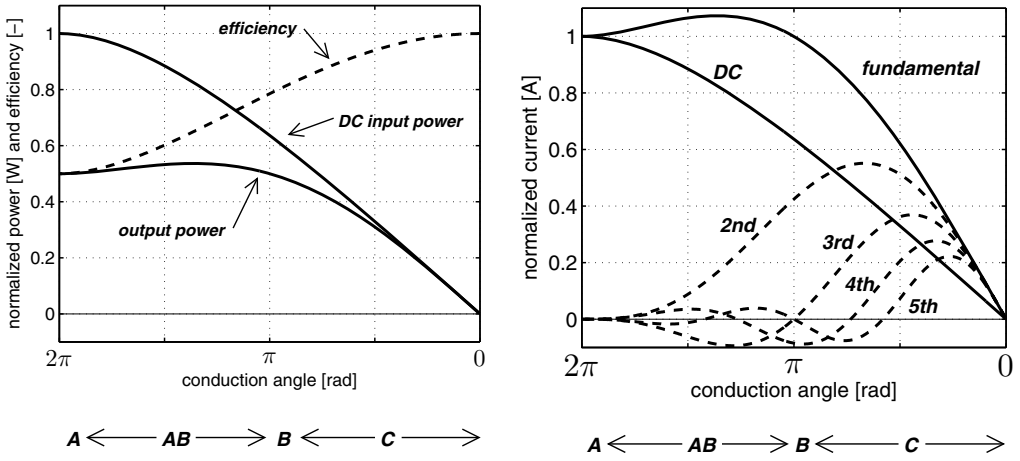
(b) Generic power amplifier waveforms (from [8])

FIGURE 2.1: Generic gm-based power amplifier a) schematic, and b)waveforms.

A generic and basic schematic for this type of PAs is given in Figure 2.1(a). In general, the DC-feed L_{DC} inductor is an RF-Choke and the C_{BL} capacitor is for AC-coupling. A matching network between the load and the PA can be needed in order to present a more 'optimum load' to the power amplifier than a direct connection to the final load (e.g. the antenna). R_L represents the load that the PA will see due to the matching network. The matching network commonly makes a down-transform action, but there are practical limits in the transformation ratio; this is, R_L will have a minimum practical value in order to maintain in a reasonable level the losses due to a practical matching network[6]. Additionally, an optional filter or harmonic trap (in shunt with the final load) could be needed to suppress harmonics in the output signal.

The gm-based amplifiers in Class A, AB, B and C differ only in their biasing conditions, which changes their main parameters. Class A conducts current all the time, Class B does it during only half of the time (or during π radians), and as we go to Class C the conduction angle is further reduced. A general model for all these gm-based classes has discussed extensively in [10] and [7]. It is worth to highlight here the most important conclusions, presented in Figure 2.2.

[6]Roughly, a value lower than 5Ω for R_L is not very practical.



(a) η and normalized P_{out} (with respect to V_{DD}) for Class A, AB, B and C (from [7])

(b) Harmonic content for Class A, AB, B and C (from [7])

FIGURE 2.2: η, normalized P_{out} (with respect to V_{DD}) and harmonic content for Class A, AB, B and C (from [7]).

The reduction in conduction angle yields to higher efficiency (see Fig. 2.2(a)), since it reduces the overlap of current and voltage waveforms at the output, as seen in Fig. 2.1(b). The maximum theoretical efficiency is 50% for Class A, 78.5% for Class B and approaching 100% as the conduction angle approaches zero. However, the output power will reduce with smaller conduction angles, with a soft peak at 1.36π radians. The reduction of the conduction angle will lead to an increase of higher harmonics at the output signal, as seen in Fig. 2.2(b). At reduced conduction angles the waveforms are not only determined by the transistors in the PAs but also by the load conditions during the *off* times (or non-conduction angles), and hence the load network will influence the efficiency too [7]. As observed in Figure 2.2(a), there is a trade-of between efficiency and output power level. Many authors have agreed that a good compromise is class B, since it has the same amount of output power than Class A (see Fig. 2.2(a)), with an increased efficiency. If higher linearity is needed, then Class AB would be a better option, at the expense of reduced efficiency.

The plots shown in Figure 2.2 assume a fixed maximum transistor current and an optimum load R_L that maximizes the output voltage swing at each conduction angle. Hence, the maximum drain-source voltage of Class A and all the reduced conduction angle amplifiers is independent of the conduction angle and equals to two times the supply voltage, $v_{DS} = 2 \cdot V_{DD}$. Then, the

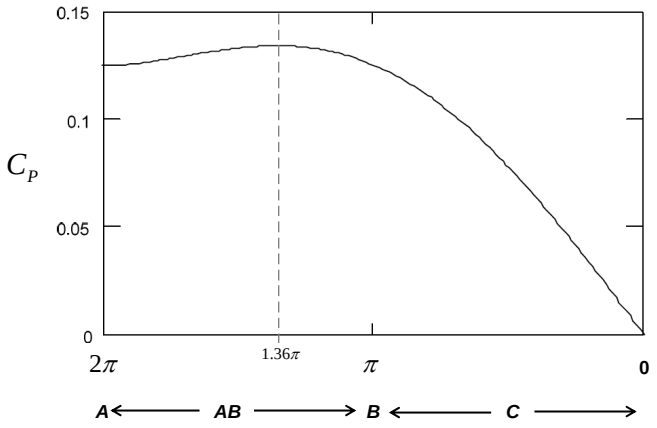


FIGURE 2.3: Output power capability factor, C_P, for Class A, AB, B and C (from [8]).

output power level for Class A and Class B is

$$P_{out_{A,B}} = \frac{\left(\frac{V_{DD}}{\sqrt{2}}\right)^2}{R} = K_{P_{A,B}} \frac{{V_{DD}}^2}{R} \tag{2.9a}$$

$$K_{P_{A,B}} = 0.5 \tag{2.9b}$$

Observe that the plot for the 'normalized output power' in Figure 2.2(a) can be seen as the plot of K_P for Class A and all the reduced conduction angle PAs (only for Class A and Class B, the optimum load R_L has the same value). Figure 2.3 shows the output power capability factor C_P for Class A to Class C.

If the biasing condition of Class A is unaffected and the input power is increased such that the output waveform starts to clip, the overlap between voltage and current waveforms will reduce and hence the efficiency will increase. This amplifier is called *Saturated* Class A and it is more efficient than a normal Class A, but less linear (because of the clipping) and with a lower power gain (due to a higher increase of P_{in} than of P_{out}). For an overdrive angle of π radians, the output voltage will look like a square wave with total rising and falling times of π radians. The efficiency of this class goes from 50% to 81% and its output power increases 62% with respect to the normal Class A. [7]

Class F is another gm-based amplifier that boosts both efficiency and output power by using one or more harmonic resonators in the output network to shape the drain waveforms. The voltage waveform includes one or more odd harmonics and approximates a square wave, while the current includes even harmonics and approximates a half sine wave [6]. Shaping the voltage

and current waveforms help to reduce the voltage-current overlap at the transistor to enhance the drain efficiency. The shape of the output voltage is still determined by an harmonic trap across the load resistor R_L. If the quality factor of this harmonic trap is high enough, the output voltage will be a sine wave. In practice, a finite number of harmonic resonators is enough (e.g. up to the third or fifth harmonic) to provide high efficiency levels.

Table 2.1 summarizes the drain efficiency and normalized output power factors for gm-based power amplifiers.

2.2.3.2 Switchmode-based PAs

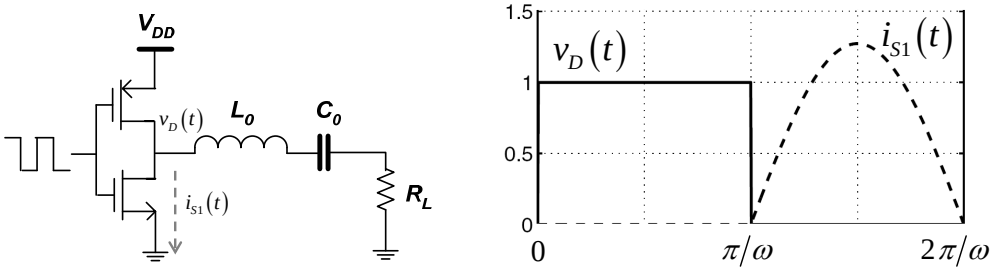
The switchmode-based amplifiers are designed with the assumption that the amplifying device works as an *ON-OFF* switch; this is, the (voltage-controlled current-source) transistor is driven in such a way that it goes from its triode region to its cut-off region as fast as possible. As a zero-th order approximation, this switch is assumed to be perfect, going from its ON-state (0Ω) to its OFF-state ($\infty\Omega$) instantaneously[7] with a certain duty-cycle, commonly of 50%. These amplifiers are considered to be *non-linear* since as long as the input power is high enough to keep the transistor in triode region, there is no relationship between the amplitude of the output signal with the input signal. However, this 'non linearity' refers only to the amplitude, since *phase linearity* is still present. The switchmode amplifiers can provide theoretically up to 100% of drain efficiency[8]. These amplifiers are able to directly process *constant-envelope* input signals (fixed amplitude with only varying frequency or phase) by themselves. However, amplitude-modulation can also be obtained by using switchmode PAs within systems able to reconstruct the amplitude of the original signal, like in LINC (LInear amplification using Nonlinear Components) systems[9].

Even a simple circuit as the one shown in Fig. 2.1 without the filter could work in switchmode if the driving power is high enough. The load for that circuit would be a broadband resistor. Since the transistor would work as a switch, the voltage across its terminals would not overlap the current passing through it and hence the device would *not* dissipate power into heat. However, a more meticulous analysis of that circuit [10] shows that its efficiency will be at most about 81% at 50% duty cycle (just as the efficiency in the Saturated Class A). The drop in efficiency is due

[7] This apparently crude approximation could be compared to the assumption of zero knee-voltage in the gm-based amplifiers.

[8] PAE and $\eta_{overall}$ will never reach 1 (or 100%) since $P_{in} \neq 0$, otherwise we would have an oscillator.

[9] [10] provides a good introduction to this vast topic



(a) Class D schematic

(b) Class D normalized voltage and current waveforms

FIGURE 2.4: Class D power amplifier a) schematic, and b) waveforms at the drain node.

to the fact that power is being wasted in harmonic generation. If a harmonic short across the load es employed, higher efficiencies can be reached. However, there will be a trade-off between P_{out} and efficiency as a function of conduction angle. At the point where the output power peaks the efficiency will be just around 63%, and as the efficiency tends to 100% P_{out} will tend to zero [10]. This is a similar P_{out}–efficiency trade-off as in the case of reduced conduction angle gm-based PAs.

Class D

A Class D amplifier is a switching-mode amplifier that uses two active devices driven in a way that they are alternately switched ON and OFF. The active devices form a two-pole switch that defines either a rectangular voltage or rectangular current waveform at the input of a tuned circuit that includes the load. The load circuit contains a band- or low-pass filter that removes the harmonics of the rectangular waveform producing a sinusoidal output [13]. The basic schematic of a Class D Complementary Voltage Switching (CVS) power amplifier is shown in Figure 2.4(a) (the top transistor could also be an NMOS transistor -and the name would change to *quasi-Complementary* Voltage Switching-, but for an integrated circuit, the use of a PMOS simplifies the circuitry). The characteristic voltage and current waveforms at the drain node are shown in Figure 2.4(b).

For this amplifier the maximum voltage swing will be equal to the supply voltage, this is, $v_{DS,max} = V_{DD}$. The output power capability factor is $C_{P_D} = 0.1592$. Table 2.2 presents the normalized output power factors for the Class D amplifier.

The Class D amplifier is limited in its use as PA final stages at high frequencies due to several drawbacks. First, it employs hard switching for both transistors (turning-ON the transistors with

Parameter	Class A	Class B	Sat. Class A	Class F_3	Class F_5
η	50.0%	78.5%	81.0%	88.4%	92.0%
K_P	0.500	0.500	0.8106	0.6328	0.6866
κ_P	0.125	0.125	0.2026	0.1582	0.1717

TABLE 2.1: Summary of ideal drain efficiency (η), and normalized output power factor with respect to V_{DD} (K_P) and with respect to $v_{DS,max}$ (κ_P) for the main gm-based power amplifiers.

Parameter	Class D	RF-choke Class E [14]	Parallel-circuit Class E [15]
η	100%	100%	100%
K_P	0.2026	0.5768	1.365
κ_P	0.2026	0.0455	0.103

TABLE 2.2: Summary of ideal drain efficiency (η), and normalized output power factor with respect to V_{DD} (K_P) and with respect to $v_{DS,max}$ (κ_P) for the main switchmode-based power amplifiers.

finite voltage at their terminals) and therefore there is a power loss that is proportional to the operating frequency, f, the parasitic drain capacitance of *each* transistor, $C_{d_{1,2}}$, and the square of the supply voltage, V_{DD}; this is,

$$P_{diss,D} = (C_{d_1} + C_{d_2}) \cdot f \cdot {V_{DD}}^2 \tag{2.10}$$

which at high frequencies can be an important amount of wasted power. Other drawback is that two switches must be driven and hence the power gain will reduce. Power gain is an important issue at RF. Additionally, the finite ON resistances of the transistors will degrade the efficiency of the amplifier and the use of a PMOS transistor will worsen this effect. On the other hand, this power amplifier does not require DC-feed inductors (which can be an important feature) and it has high output power capabilities, as seen in Table 2.2. Class D can find important uses as drivers for high-power power amplifiers, as it is discussed in Chapter 4.

Class E

The Class E is a switchmode-based circuit that employs an active device working as an ON/OFF switch. The basic circuit schematic of Class E can be seen in Figure 2.5. Due to the tuned series filter (L_0 and C_0) the output voltage will be sinusoidal. If the loaded quality factor of such a filter is high enough, no harmonic power will be dissipated in theory[10]. The switch S can be

[10]For the selection of the series filter loaded quality factor, there is a trade-off between bandwidth and efficiency.

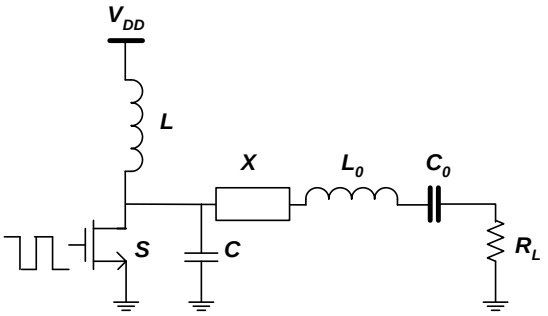


FIGURE 2.5: Single-ended Class E circuit schematic.

implemented by a single NMOS transistor, or a stack of NMOS transistors as it will be seen in Chapter 3.

The load network, composed by L, C and X is designed in time-domain such as to provide an specific steady-state voltage waveform at the drain of the NMOS transistor. The output capacitance of the transistor can be absorbed by the load network by means of C. In general, C is implemented entirely by this output capacitance. Including the parasitic output capacitance of the transistor is probably one of the most important features of this class of amplifier, since losses of this capacitance are avoided in theory.

There are two operating modes, whose original names are *optimum mode* and *suboptimum mode* [14]. Those operating modes are defined according to the *Generalized Class-E Switching Conditions*, which are:

$$v_C(t)\Big|_{t=\frac{2\pi}{\omega}} = \alpha \cdot V_{DD} \tag{2.11a}$$

$$\frac{\mathrm{d}v_C(t)}{\mathrm{d}t}\Big|_{t=\frac{2\pi}{\omega}} = k \cdot \omega \cdot V_{DD} \tag{2.11b}$$

where $\alpha \cdot V_{DD}$ is the capacitor C voltage at the moment the switch is turned-ON, and $k \cdot \omega \cdot V_{DD}$ is its slope. Notice that if both $\alpha = 0$ and $k = 0$, then eqs. (2.11a) & (2.11b) are the well-known *optimum* Class-E switching conditions [14, 16, 17]. Eq. (2.11a) for $\alpha \neq 0$ defines the so-called *Variable-Voltage* Class-E mode [18], denoted as Class-E_{VV}. Eq. (2.11b) for $k \neq 0$ defines the so-called *Variable-Slope* Class-E mode [19, 20], denoted as Class-E_{VS}. If $\alpha \neq 0$ or $k \neq 0$, then the Class E amplifier is operating in the *suboptimum mode*.

The full analytical derivation of the general model for Class E is presented in Appendix B. A detailed discussion on such a model and all the Class E operating modes is done in Appendix C. In this section only a short summary on the design of Class E circuits is presented. For further details, please refer to those appendices.

The Class E power amplifier is straight forward to design once its analytical model has been solved (refer to the Appendix B). The design procedure requires certain technology parameters as well as some user defined operating conditions as inputs (like operating frequency, ω, optimum or suboptimum mode of operation, etc.). The outcome of the model is the so-called design set $\mathbf{K_E} = \{K_L, K_C, K_P, K_X\}$[11] [17] that relates the model solution to the circuit elements L (DC-feed inductor size), C (switch S size), X (reactive element X) as well as to the PA performance parameters, P_{out} and η. In theory, there is an infinite number of possible designs [17], however some of them are more convenient than others, as discussed in Appendix C.

The Class E with parallel circuit topology [15] provides the maximum output power for a given supply voltage and loading resistance. That specific topology makes $X = 0$, and hence the Class E circuitry is further simplified. This Class E with parallel circuit can be freely designed at any operating mode (and duty-cycle), as demonstrated in Appendix C. This topology will be the one employed in rest of this work.

Designing a Class E circuit in suboptimum mode (variable-voltage and variable-slope) has advantages. Allowing a finite voltage up to approximately the supply voltage (i.e. $\alpha = 1$) at the turn-ON moment reduces the peak voltage of the Class E circuit significantly. This allows an increase in the maximum output power with a very small drop in drain efficiency [18]. Also, negative slopes of the voltage during the turn-ON moment contributes to reduce the peak voltage and increase the maximum output power [20]. Interestingly, both variable-voltage and variable-slope can be combined simultaneously to combine their advantages.

In general, the duty-cycle of the driving signal in a switchmode PA is 50%. However, in this work it was found that duty-cycle control can modify the performance of a Class E PA. Specifically, duty-cycle control can recover efficiency at backed-off power levels (due by both, load and supply modulation) over a wide bandwidth. Further details about this finding can be read in Section C.3 of Appendix C. This outcome can be usefully applied in novel broadband high-efficiency power amplifiers. Therefore, duty-cycle control capability in driver circuits can be an

[11] Where $K_L = \omega \cdot L/R_L$, $K_C = \omega \cdot C \cdot R_L$, $K_P = P_{out} \cdot R_L/{V_{DD}}^2$, and $K_X = X/R_L$.

important added feature.

Class DE

There is a power amplifier called Class DE that employs a similar circuit topology than the Class D but that introduces a dead-time between the ON moments of each switch. The idea is to incorporate the parasitic drain capacitances into the operation of the amplifier and to avoid the hard-switching. In order to accomplish this, it introduces in its operation the so-called Class E switching conditions (in optimum mode, they would be the zero drain voltage with zero slope at the turn-ON moment of each switch). An important drawback of this amplifier is the high complexity in the driving circuitry, since a precise control of the dead-times is needed. Also, the power gain is reduced by needing to drive two switches, as in Class D. Although Class DE can operate at higher frequencies than Class D, Class E is able to work at around 3 times higher frequencies than Class DE [11].

2.2.4 Conclusions about the output power of the different PA classes

The former sections have briefly described the main classes of power amplifiers and have summarized their maximum theoretical efficiencies and output power capabilities. The normalizing parameters for the output power capabilities of such amplifiers, K_P and κ_P, can lead to the following conclusions, from Tables 2.1 and 2.2:

- If the active devices are not constrained by oxide breakdown voltage, then the parallel circuit Class E will yield the higher output power for a given supply voltage and load. This is expressed by the parameter K_P.
- If the active devices are constrained by oxide breakdown voltage, then the Class D (and the Saturated Class A, but with an inferior theoretical drain efficiency) will yield the higher output power for a given 'reliable supply voltage' and load. This is expressed by the parameter κ_P.

Hence, κ_P can be very important for the design of CMOS power amplifiers and drivers, due to the reliability constrains of CMOS technology, which are reviewed in the next section.

2.3 CMOS technology and reliability

It is known that standard silicon CMOS is the preferred choice for most integrated circuits, and hence the integration of HV drivers in CMOS technology has attracted much interest. Logic circuitry has profited from advances in each new technology node (intrinsic device speed, device density, etc.), although layout parasitics in the state of the art nodes have started to dominate and hence to compensate those advantages. Contrarily to logic implemented in CMOS, power amplification has becoming more challenging with the newest technology nodes; mainly because of the reduced breakdown voltages as well as the limited quality of the integrated passives.

Most state of the art CMOS technologies offer standard thin- and thick-oxide devices that have different breakdown voltage levels. This combination of devices allow the designer more flexibility for the implementation of high voltage drivers and power amplifiers. Additionally, some technology nodes have permitted the construction of novel extended-drain (ED) MOS transistors [21, 22]. Because of the drain extension, the intrinsic RF performance of the ED devices will be lower than for the standard devices, but they will have an increased breakdown voltage capability[12].

The main reliability concerns in MOS transistors are associated to three electric field strengths that appear to be dominant for the lifetime of MOS transistors [23]: the vertical and lateral electric field in the (intrinsic) transistor, and electric fields across junctions. Specifically, there are three lifetime-determining mechanisms corresponding to these fields, which are: oxide breakdown, hot-carrier degradation and junction breakdown, respectively. Those effects have different impacts according to the amplifier class of operation and transistor usage.

2.3.0.1 Hot-carrier degradation

In the presence of large drain-source voltages for transistors operating in saturation, carriers flowing from source to drain may gain high energies. Upon collisions with the silicon lattice, a small fraction of these hot carriers shoot into the gate oxide near the drain area, thereby slowly degrading the gate oxide and the transistor's performance. This hot-carrier degradation effect depends among others on the transistor's length and its biasing conditions, see figure 2.6. [23]

[12] Appendix A describes the standard and extended-drain MOS devices that are available in the 65-nm CMOS technology employed in this work.

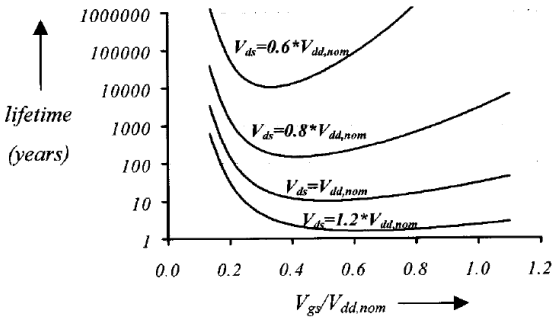


FIGURE 2.6: Typical hot-carrier-based lifetime behavior versus biasing for a minimum length transistor; for longer transistors the lifetime is larger [23].

The hot carrier effect is a reliability issue. It increases the threshold voltage and consequently degrades the performance of the device. Since hot-carriers are only generated in the presence of both a high drain current and a high drain voltage, switchmode PAs are immune to this effect by avoiding, ideally, the simultaneous presence of voltage and current. Although, the maximum voltage to avoid hot carriers is determined experimentally, for production requirements it is recommended not to exceed 5% to 10% above the maximum allowed supply voltage to guarantee a product lifetime of ten years [24].

2.3.0.2 Junction breakdown

Junction breakdown can occur across the drain-substrate reverse biased junction. Two physical mechanism give rise to the reverse-bias breakdown in a pn junction [25]: the *Zener effect* and the *avalanche effect*. Zener breakdown occurs in highly doped junctions through a tunneling mechanism. The avalanche breakdown occurs when electrons and/or holes acquire sufficient energy from the electric field, while moving across the space charge region, colliding and ionizing other atoms, and hence creating more electrons and/or holes. This effect starts an avalanche process. For most pn junctions, the dominant breakdown mechanism will be the avalanche effect.

For modern CMOS processes this junction breakdown occurs at voltages of at least a number of times the nominal supply voltage. Therefore, it is not a real concern for circuits that should operate at voltages up to roughly 2.5 times the nominal supply voltage [23]. It can be observed in figure 2.7, that the breakdown voltage of Si is relatively high at all impurity levels with respect to the low oxide breakdown in the state of the art CMOS (e.g. 1.2V in thin-oxide 65-nm CMOS). Additionally, the junction breakdown voltage can be significantly increased interleaving dielectric regions (STI) with the junctions (active regions in CMOS), as explained in [21].

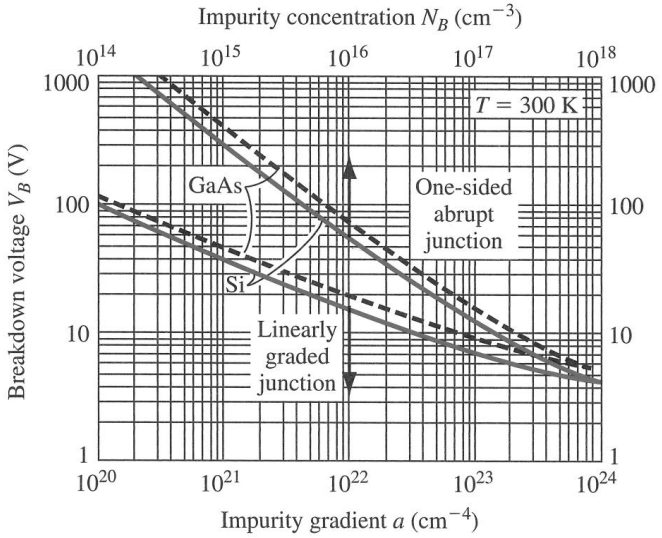


FIGURE 2.7: Breakdown voltage versus impurity concentration for Si and GaAs (from [25]).

2.3.0.3 Oxide breakdown

In modern sub-micron CMOS process, oxide breakdown is typically the limiting factor [8]. Oxide breakdown is a catastrophic effect and sets limits on the maximum voltage swings on the terminals of the transistor. This breakdown mechanism is present in all the amplifier classes as: a) oxide breakdown across the oxide in the gate-source overlap area and, b) across the drain-gate overlap area. The breakdown limit is a function of the oxide thickness, which is reduced with each new technology node. The most probable effect is the breakdown at the oxide in the drain-gate area due to the larger voltage swing between those nodes in a practical amplifier, that depends on the amplifier class[13].

The oxide breakdown process occurs in two phases [8]: a gradual, field-induced defect accumulation, followed by thermal runaway and permanent damage of the oxide. It can be characterized by the *Mean Time to Failure* (MTTF), which states the anticipated time for the defect density to reach a critical level that triggers the thermal runaway process. This thermal runaway process quickly results in a short across the oxide and hence in a permanent destruction of the device [8]. The intrinsic breakdown field[14] for SiO_2 is around 1.1V/nm, however the maximum practical voltage ratings in typical CMOS are always lower [8]. It was found that oxide lifetime is sufficient if the electric field is limited to about 0.55 V/nm [8, 26]. For example, for a 65-nm

[13]For example, in the Class E when the transistor is turned-off, the gate is tied to ground and the drain could swing up to more than 3.5 times the supply voltage. In the other hand, for the same Class E, the swing at the gate-source can be easily limited at the maximum rated supply voltage, avoiding any risk of breaking down the oxide at that area.

[14]The intrinsic breakdown field is the maximum field that is sustainable by a defect-free dielectric. The defect density has significantly been reduced over CMOS generations, but still there are built-in defects in the oxide, which will cause breakdown to occur before the intrinsic limit. [8]

CMOS process, the maximum rated gate voltage is 1.2V for thin-oxide ($t_{ox,G01} \approx$ 2.6nm) and 2.5V ($t_{ox,G02} \approx$ 5.6nm) for thick-oxide devices; which corresponds to oxide fields of less than 0.5V/nm, for both cases.

2.3.0.4 AC oxide breakdown limit

From the discussion above of the three MOS transistors lifetime-determining mechanisms, the oxide breakdown is the most important for switchmode power amplifiers, specifically at the gate-drain nodes. For RF power amplifiers, the active device experiences a large voltage across their gate oxide only for a portion of the operation cycle. Unfortunately the exact limits to avoid oxide breakdown are pretty difficult to determine. Oxide degradation has been mostly investigated in DC conditions, using high field test to accelerate oxide breakdown and to predict maximum voltages for safe device operation [27]. However, one could expect the devices to exhibit a different breakdown limit under high frequency conditions. For example, [28] (taken from [8]) found an increase in gate oxide lifetime of ten times if the transistor is subjected to AC instead of DC stressing. Unfortunately AC oxide breakdown testing is currently not part of the standard characterization in production CMOS [8].

The lack of an AC oxide breakdown standardization has lead to the usage of different maximum limits for the supply voltage from several authors in literature, even for the same class of amplifier. For example, for a class E power amplifier: [1] employs $1.1 \times V_{DD,nom}$ in 65-nm CMOS, [8] uses the limit of $1.7 \times V_{DD,nom}$ in CMOS 0.35um, and [29] prefers $2.0 \times V_{DD,nom}$ for CMOS 0.25um, where $V_{DD,nom}$ is the rated supply voltage at each technology node. The first two authors seem to be following the same DC conservative limit that aims to avoid the electric field to exceed about 0.6V/nm. However, the third author employs the limit of 1V/nm (which is close to the intrinsic breakdown field of 1.1V/nm of SiO_2). Observe that there is roughly a difference of 70% in the electric field limits employed by those authors.

The difference between AC and DC stressing reported in [28] provide insight on the relative reliability of PAs with different voltage waveforms [8]. In fact, [27] demonstrated experimentally that the physical mechanism of oxide degradation is triggered by the *rms* value of the oxide field, and not by its maximum. This shows that the maximum RF voltage peaks for safe device operation are much larger than the usual DC limits used nowadays [27]. However, the lack of a common consensus with respect to the AC oxide breakdown limit, forces to the designers to employ the most conservative DC limits.

2.4 Addressing the high-voltage needs of power amplifiers and their drivers

To address the needs for power amplifiers and their drivers, three approaches can be followed to make high-voltage circuits [23]. First, technological solutions can be pursued (e.g., multiple gate oxides) which yield high-voltage-tolerant transistors at the cost of a more expensive process. Second, extended-drain devices in baseline CMOS technology [21, 22] can be employed. Third, novel circuit solutions using only standard baseline transistors can be applied [23, 30], that provide high-voltage tolerance.

The first option is not attractive due to the increased cost (additional masks and processing steps must be added to the baseline process). The second option does not add cost since it is based on smart layout in baseline processes; profiting from fine dimensions in ACTIVE (silicon), STI (oxide) and GATE (polysilicon) regions [22]). However, this second option must be employed with care, since the extended-drain transistors have reduced intrinsic RF performance compared with the standard baseline devices. The third option tries to limit the voltages across all transistors' terminals to reliable levels by proper circuit topologies. This last option could imply an increase in the circuit complexity that could reduce performance.

Device stacking or cascoding is one of the most popular circuits of the third option. This approach will be further investigated in Chapter 3. It will be seen that the complexity increases significantly as the number of cascoded (or stacked) devices increases to more than 3, imposing a practical limit in the number of stacked devices.

Inverter-based drivers (Class D like) are also an alternative that could be considered part of the third option. Although this circuit does not imposes severe oxide stress in the devices (since the swing is equal to the supply voltage), it is not a high-voltage solution if only standard devices are employed. However, implementing this driver topology with extended-drain (ED) devices can provide a high-voltage operation, due to the ED devices. Then, this approach using ED devices could be considered part of the second option. This approach is further investigated in Chapters 4 and 5.

Chapter 3

Class E cascoding approach for HV swings

3.1 Introduction

The cascoding technique enables to increase the output swing in low-breakdown voltage technologies. A cascode topology consists of a bottom common-source (CS) transistor with one or several common-gate (CG) transistors on top, as shown in Figure 3.1. If the bulk of any of the stacked transistors in Fig. 3.1 is not connected to the substrate, then a tripe well CMOS process will be required, since the p-type bulk of that NMOS transistor will be separated (by an N-well) from the p-type grounded substrate. In general, only the gate of the bottom CS transistor is

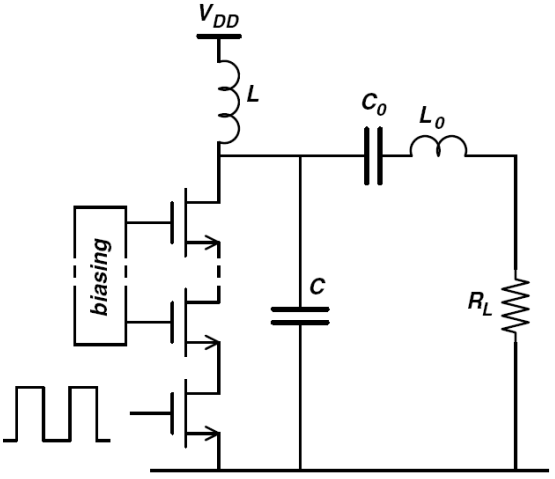


FIGURE 3.1: Class E amplifier/driver using several cascoded devices.

driven directly with an RF input signal while the gates of the other transistors are AC grounded. The biasing levels of the CG transistors are chosen to avoid oxide breakdown of any of the transistors in the stack. However, under large signal operation, the voltage swing between the gate and drain of the common-gate transistors could become larger than that of the common-source transistor unless AC signals are allowed at the gate of some of the stacked transistors [24]. The cascode topology can sustain higher output voltage swings by distributing the voltage stress among all its transistors, and hence the supply voltage can be increased. There are, however, practical limitations in the cascoding approach that will be discussed in this chapter.

This chapter studies the possibilities of high-efficient and high-voltage topologies using the cascode/stacking approach with only *standard* devices in 65-nm CMOS, employing the Class E operation. In the second section of this chapter, we discuss the efficiency loss mechanisms that are associated to the cascode topology. Next, in the third section, two specific cascode topologies (3 and 4 stacked devices) are described and Cadence Spectre simulation results are discussed. In the final section, a comparison is performed between those specific solutions and other high-voltage state of the art solutions reported in literature. Finally, the conclusions from the cascoding approach for high-voltage tolerant circuits in 65-nm CMOS is presented at the end of this chapter.

3.2 Sources of efficiency loss on a cascode topology

When implementing Class E cascode circuits, the efficiency loss mechanisms will be due to the general circuit and to the cascode topology themselves. First, we summarize the efficiency loss mechanisms in any Class E circuit and then, the specific loss mechanisms in cascode topologies.

Any Class E amplifier/driver will have inherently some practical sources of efficiency loss[1]. These losses are due to the finite R_{ON} resistance of the switch (expressed in the $m = R_{ON} \cdot C \cdot f$ parameter), the finite quality factor of the DC-feed inductor L, and the specific Class E mode of operation, determined by the values of α (switch voltage at the turn-ON moment of the switch) and k (the slope of the switch voltage at the turn-ON moment). Also, in Class E, the finite quality factor of the components in the series filter and the X element will degrade the drain efficiency. The losses of the X circuit element can be eliminated by designing a Class E with parallel circuit [15].

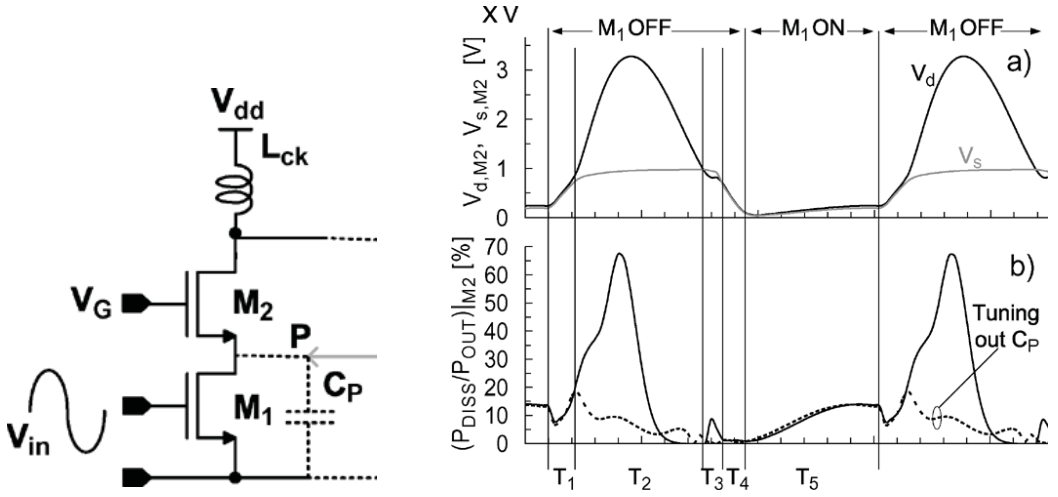
[1]For details on the Class E, refer to Appendix C.

The cascode topology has mainly two sources of efficiency loss. During the ON periods of the CS device, the finite ON resistances of all the stacked CG transistors will dissipate power, and during the OFF periods there will be charging/discharging losses at the internal nodes between the drain and source terminals of the stacked devices [29]. All the internal nodes, i.e. the nodes between transistors, will have the combination of the parasitic capacitances at the drain of the bottom device and at the source of the top device. The total parasitic capacitance at each node will depend on the type and size of each transistor and could be of similar magnitude as the overall shunt parasitic capacitance at the top-most drain node when employing a Class E configuration [29]. The voltage at each internal node will be close to zero during the ON-times, and during the OFF-times it will track the gate voltage of the corresponding top transistor with an offset equal to the threshold voltage of that transistor.

The work in [29] explains in detail the loss mechanisms in a Class E cascode topology attributed to the internal capacitances between the stacked devices. For completeness of this work, we summarize here these loss mechanisms. In Figure 3.2, when M1 is turned-off, the internal parasitic capacitance C_P (see Fig. 3.2(a)) starts charging since M2 is still in its triode region during T1 (see the top plot in Fig. 3.2(b)). At the end of T1, M2 approaches weak inversion/sub-threshold region of operation and the drain to source voltage difference increases. During T2, C_P charges at a relatively low-current (proportional to $C_P \cdot \frac{\mathrm{d}V_{S,M2}}{\mathrm{d}t}$), but the dissipated power is not negligible because of the relatively large drain to source voltage. At the end of T3, M1 turns-on, and the soft switching condition of class-E could no longer be realized, discharging C_P and C (the overall shunt capacitance at the drain of the top-most device -M2 in this case-) towards the grounded substrate dissipating the stored energy (this last effect is not quantified in the figure) [29].

From the explanation in [29] it is possible to observe two specific mechanisms of power dissipation; the one during T2 and the capacitive charging/discharging loss of C_P. The second effect is similar to the familiar hard switching mechanism and occurs at each internal node. Therefore, the losses associated to this last effect should be proportional to the switching frequency, the parasitic capacitance C_P and the square of the corresponding internal P node voltage (which is in turn given by $V_G - V_{TH}$ of the transistor on top of C_P), this is, $P_{loss,2} \propto f \cdot C_P \cdot {V_P}^2$.

The ON-OFF control of the cascode topology is determined by the CS device. There is an ON-OFF sequence for the stacked devices. Once M1 (bottom-most device) is turned-on, M2 will start to be turned-on during a finite time. Once M2 is turned-on, M3 (if applicable) will start



(a) Cascoded Class E (main part of) circuit schematic

(b) Cascoded Class E voltage and dissipated power waveforms

FIGURE 3.2: Cascoded Class E internal capacitive losses description (from [29]); a) circuit schematic and, b) voltage and dissipated power waveforms.

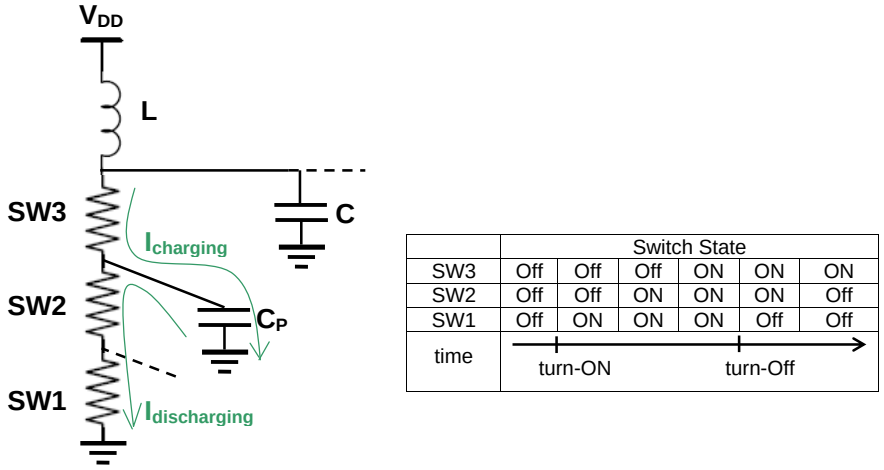


FIGURE 3.3: Switching and charging/discharging process in a 3-device cascode topology.

its own turning-on process and so on until all transistors are turned-on. The turn-off process will be similar, starting with M1 and following the same ordered sequence. This will mean that *each* internal node will dissipate power due to its associated parasitic capacitance. This charging/discharging loss mechanism is schematically shown in Figure 3.3 for 3 transistors, where only the top-most internal capacitance is shown (named C_P for convenience). However, since this loss mechanism is expected to be a function of the *square* of the internal node voltage (determined by the gate and threshold voltage of the transistor on top), then the dominant source of power dissipation will be located at the top-most internal node.

The work in [29] proposes tuning-out the parasitic capacitance C_P in order to diminish the above

cascode dissipating losses. This solution does not require a high quality factor inductor (in series with a decoupling capacitor) nor a very accurate value for it, but it could occupy a significant silicon area when integrated in the same chip. Another way to diminish this loss mechanism, which is not exclusive to the former one, is to combine active devices such that the top most internal node swings at a voltage significantly lower than the output voltage (since both, P_{out} and the dissipated power are functions of the square of the output and internal node swings, respectively). This last idea would mean that employing higher-voltage transistor at the top will be advantageous (for example, stacking an extended-drain transistor on top of a thin-oxide device, as in [1]).

A closed-form expression for these loss mechanisms is quite complicated, as also indicated in [29]. One could include specific cascode topologies in the general Class E model of Appendix B by means of the parameter $m = \omega \cdot C \cdot R_{ON}$. Originally, m represents a single transistor, however it could be generalized into a *total* m parameter representing the complete switch stack by adding up the ON-resistance of each switch and using the drain capacitance of the top-most device as the outermost C. Employing that 'total m' would help predicting to some extend the losses due to the total stack composite ON-resistance. Still, the capacitive charging/discharging losses at the internal nodes could become dominant, and this effect is not including in the Class E model. Increasing the size of the stacked devices will reduce the total m parameter, promising higher efficiency, but would increase the internal node capacitances, lowering the efficiency again. The trade-off between reducing the ON-resistance of the composite switch and reducing the capacitive loading at the internal nodes is best resolved by means of PSS simulations until finding an optimum size of each transistor in the stack.

3.3 Study of two proposed cascode topologies

In this section, two cascode topologies are presented: with 3 and 4 stacked devices[2]. They aim to achieve as high output voltage swings as possible employing only standard devices in 65-nm CMOS. The reason of using only standard devices in this chapter is to know the capabilities of the cascoding approach towards HV swings. The two cascode topologies in this section were designed employing the Class E circuit topology. All the simulation results were obtained from Cadence Spectre using the so-called 'RF-models' of the devices.

[2]Stacking less devices will not lead to high-voltage swings. For a stack of more than 4 devices, the biasing circuitry will become very complex and the efficiency will not be high.

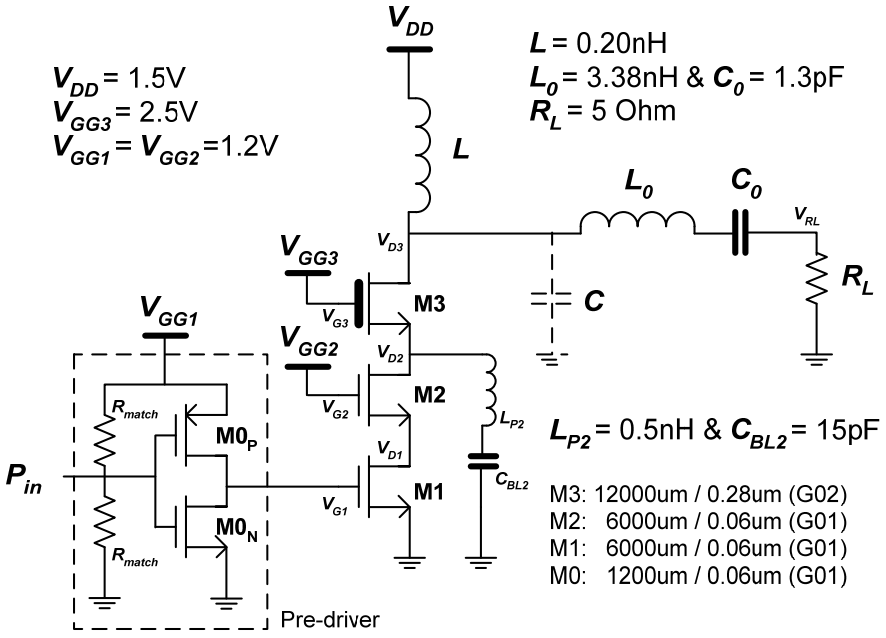


FIGURE 3.4: 3-MOS cascode Class E topology schematic.

3.3.1 3-device class E cascode topology

The design methodology followed for the design of the Class E cascode topologies is explained here by means of the design of a stack of 3 devices. The design of a cascode Class E amplifier requires the sizing of each stacked device in addition to assigning values to the rest of the circuit elements. The design procedure for the cascode topology will use the Class E model to get starting values for each circuit element and the size of the top-most transistor in the stack (which implements the overall shunt capacitance C, as seen in Fig. 3.1). Several design loops, with the aid of circuit simulations, will provide improved values for the circuit elements as well as the proper size of each transistor in the stack. The schematic for the 3-MOS transistor cascode is shown in Fig. 3.4.

As observed in the schematic of Fig. 3.4, the stack comprises two thin-oxide (G01) and one thick-oxide (G02) transistors. The load is considered to be $R_L = 5$. The series filter formed by L_0-C_0 is designed with a quality factor of 10 at the operating frequency, $f_0 = 2.4$ GHz. The *total m* parameter is $m \approx 0.01$ at the operating frequency. From the Class E model, $q \approx 1.45$ in order to maximize the output power (i.e. to make $X = 0$), and then $K_L \approx 0.67$ and $K_C \approx 0.71$. The last values of K_L and K_C provide the initial sizes for the DC-feed inductor and the top-most transistor (M3 in Fig. 3.4); this is, $L_{initial} \approx 0.22$nH and the size of M3 $\approx$ 15mm (using the estimated parasitic drain capacitance for G02, as obtained in Appendix A).

The top-most transistor of the stack is determined by the Class E conditions (through K_C). For the remaining devices in the stack, there is a trade-off in their size, as explained earlier. Also, each internal node must charge/discharge fast enough not to interfere with the overall OFF-state voltage waveform. Additionally, the input driving power is a direct function of the size of the bottom-most device.

After several simulation-based optimizations performed in Cadence Spectre, the final values for this cascode topology were found as shown in Fig. 3.4. Observe that the schematic includes also an inverter-based driver for the Class E cascode. The resistors R_{match} shown in the figure are for input matching purposes of this driver [1]. Observe that the final values for the circuit elements in the schematic shown in Fig. 3.4 do not differ too much from the initial values.

As proposed in [29], a tuning network composed of L_{P2} and C_{BL2} in Fig. 3.4 is employed to resonate out the parasitics at the V_{D2} internal node.

The admittance of an the internal node P, called V_{D2} in Fig. 3.4, is given by

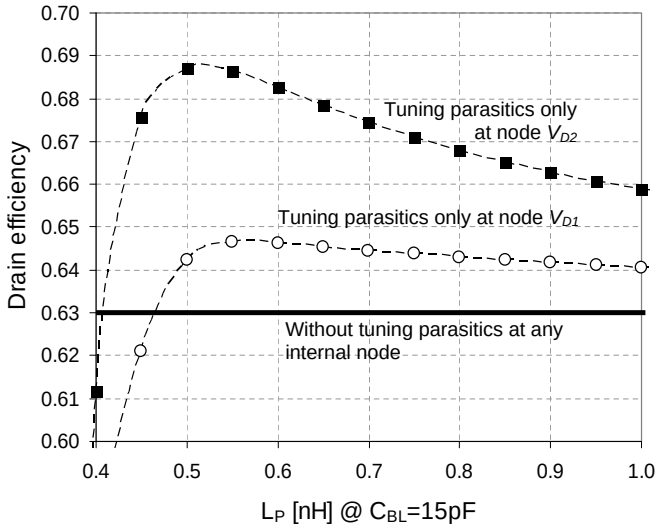
$$Y_P = \frac{1}{j \cdot \omega \cdot L_P + \frac{1}{j \cdot \omega \cdot C_{BL}}} + j \cdot \omega \cdot C_P \tag{3.1}$$

and hence, $L_P = \frac{1}{\omega^2 \cdot C_P}$ for resonating out C_P, provided that the DC-blocking capacitor $C_{BL} >> \frac{1}{\omega^2 \cdot L_P}$.

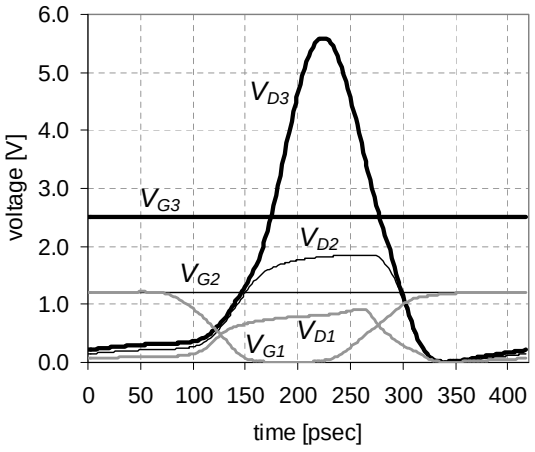
There are two internal nodes in this cascode topology, namely V_{D1} and V_{D2}. As stated before, it is expected that the top-most internal node has a greater influence on the efficiency than the other internal node. Figure 3.5(a) shows the simulation results for the drain efficiency of the 3-MOS cascode when resonating out the parasitic capacitances at both internal nodes in comparison with not adding any resonating network. Observe that resonating out the parasitics at V_{D1} has only a marginal benefit over not employing this technique at this node. However, placing L_{P2} and C_{BL2} at V_{D2} increases the drain efficiency by 6% as seen in Fig. 3.5(a).

Figure 3.5(b) shows the periodic steady state (PSS) simulation results for the voltage waveforms at all internal nodes in this 3-MOS cascode before resonating out any parasitic capacitance. Figure 3.5(c) shows the PSS voltage waveforms after resonating out the parasitics at node V_{D2}. The DC voltages at the gates of M1[3] to M3 are 1.2V and 2.5V for the G01 and G02 devices (note that even using the most conservative oxide breakdown voltage DC limit, an increment for these

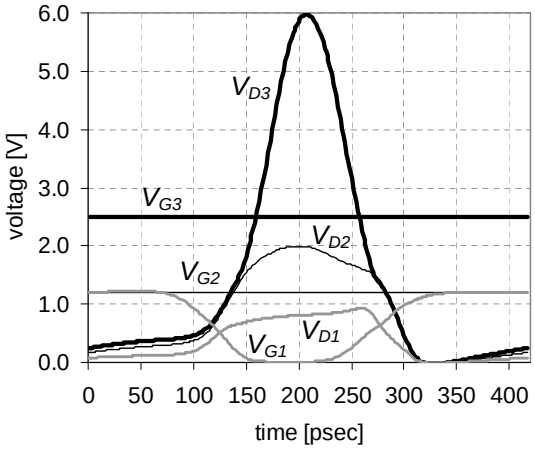
[3]The biasing of 'M1' refers to the driver of M1.



(a) Effect of resonating capacitive parasitics out at V_{D1} and V_{D2}



(b) V-waveforms before resonating out parasitics



(c) V-waveforms after resonating parasitics out at V_{D2}

FIGURE 3.5: 3-MOS cascode Class E topology simulation results; a) effect of resonating capacitive parasitics out at V_{D1} and V_{D2}, and voltage waveforms at all internal nodes b) before resonating any parasitic out, and c) after resonating them out at V_{D2}.

biasing levels of 10% is possible [24]). The gate-drain voltages of M1 and M2 are lower than any conservative breakdown voltage limit. This explains the use of the second thin-oxide device, M2. If M2 were omitted, then the gate-drain oxide of M1 would be stressed more, probably imposing concerns in its reliability, unless the DC-voltage of the thick-oxide was reduced (increasing its ON-resistance and lowering the efficiency of the cascode). Whether having a single thin-oxide, instead of a pair of G01 stacked devices (as in Fig. 3.4), would become the bottleneck for the reliability of the stack is very difficult to determine, since the exact oxide breakdown voltage limit has not been unanimously recognized at RF [27, 29]. In this case, a stacked of two G01 devices (M1 and M2) at the bottom part of the cascode has been chosen in order to show new

Parameter	65-nm 3-MOS cascode (without resonating parasitics)	65-nm 3-MOS cascode (resonating parasitics at V_{D2})
Frequency [GHz]	2.4	2.4
η [%]	63.1	68.7
PAE [%]	61.7	67.3
$\eta_{overall}$ [%]	58.6	63.6
P_{out} [dBm]	26.6	26.7
Gain [dB]	17	17
$K_P = P_{out} \cdot R_L / {V_{DD}}^2 \approx$	1.02	1.04
V_{DD} [V]	1.5	1.5
$V_{swing,peak}$ [V]	5.6	6.0

TABLE 3.1: Summary of simulated performance for the 3-MOS Class E topology.

ways for stacking devices, that could probe important at deeper sub-micron technologies. The gate–drain voltage for the M3 device is slightly higher than the conservative DC-breakdown limit, but if a more AC-oriented limit (e.g. an RMS limit, as proposed in [27]) were used there will not be any concern. Observe from Figs. 3.5(b) and 3.5(c), that resonating the parasitics out increased the peak values of the voltage waveforms.

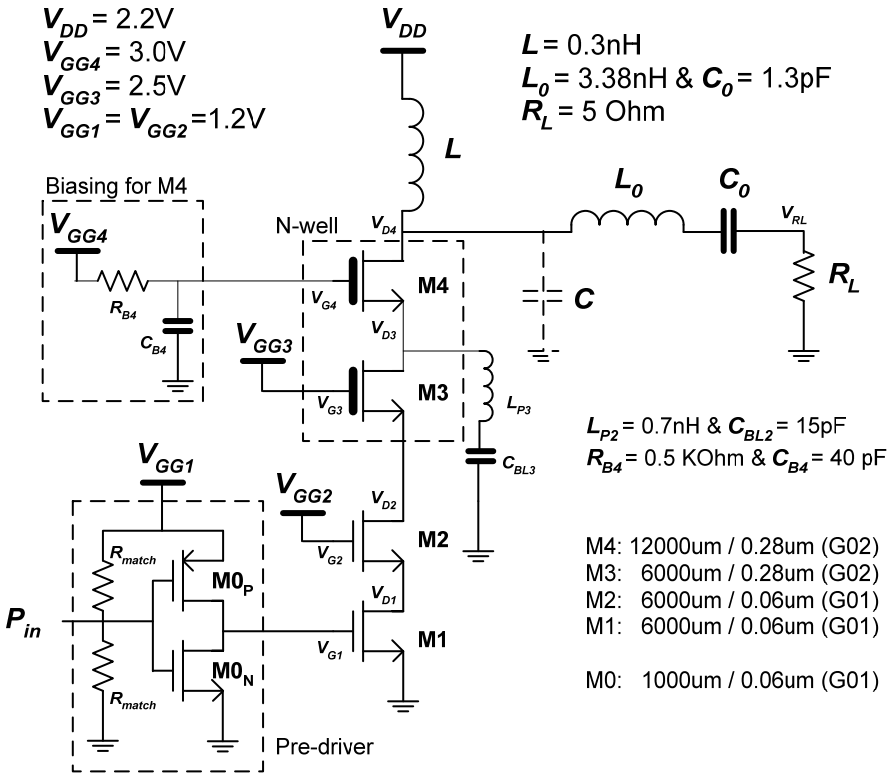
Table 3.1 summarizes the main performance metrics for this 3-MOS cascode, with and without the resonating technique.

3.3.2 4-device class E cascode topology

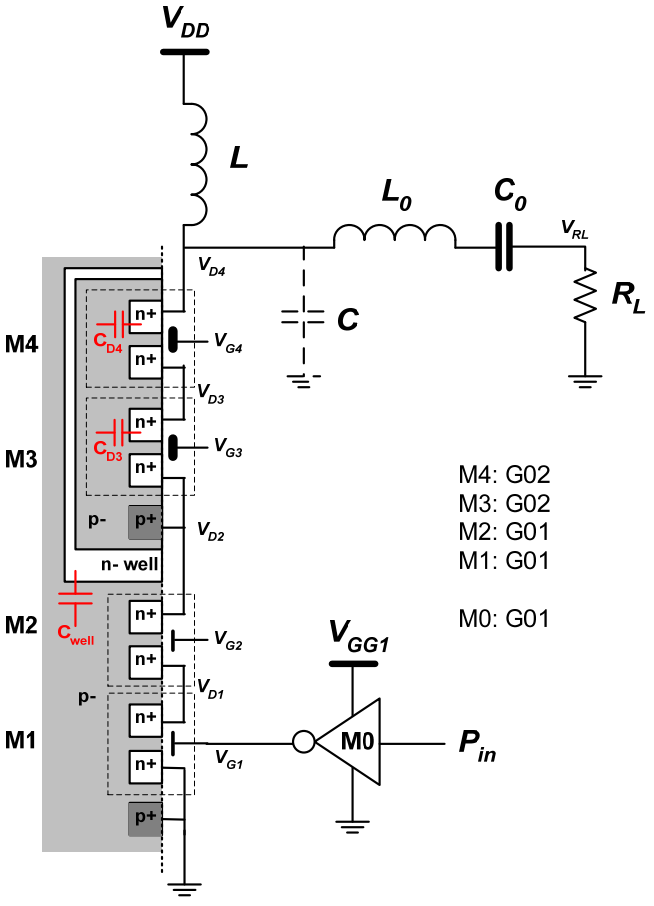
More stacked devices will increase the output voltage. However, the complexity of the cascoding approach increases rapidly with the number of stacked devices, especially after 3 devices. In this section a 4-MOS stack is presented. It will be seen than additional techniques were needed to make it possible.

The circuit schematic for the cascode of two G01 and two GO2 devices for this 4-MOS stack is shown in Figure 3.6(a). Observe from the figure that the two top-most devices were put inside of an N-well. Figure 3.6(b) shows a representative cross section view of the transistors showing the detail of this N-well and some associated parasitic capacitances (C_{D4}, C_{D3} and C_{well}).

The idea is that in order to stack the forth device, M4, a biasing scheme different than a DC level would be necessary. This is, the gate of M4 would need to swing in-phase with the output signal to be able to increase the supply voltage of the complete cascode while maintaining the gate-drain voltage of M4 within reliable levels. Allowing a large signal at V_{G4} could break down the *gate-bulk* oxide area of M4, since V_{G4} would have a large signal swing and a large DC-level



(a) 4-MOS cascode Class E topology schematic



(b) 4-MOS cascode Silicon cross section detail

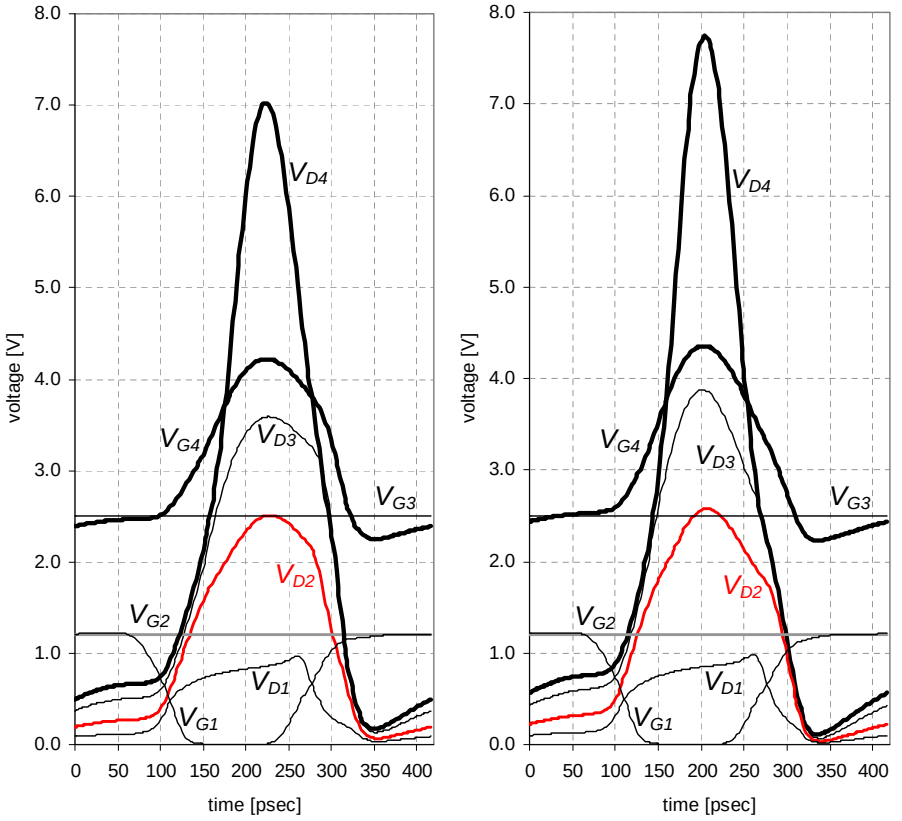
FIGURE 3.6: 4-MOS cascode Class E topology a) schematic, and b) a representative cross section of the Silicon implementation.

simultaneously. Then, even using an RMS breakdown voltage limit [27], the reliability of M4 could be severely compromised. To avoid this issue, M3 and M4 are placed inside of an N-well (65-nm CMOS technology has triple-well option, so this is possible).

The implementation of the overall shunt C capacitance is still determined by M4. However, C becomes now also a function of the size of the N-well. Observe in Fig. 3.6(b) that C would be the series combination of the parasitic drain capacitance of M4, C_{D4}, and the N-well parasitic capacitance, C_{well}. If $C_{well} >> C_{D4}$, then $C \approx C_{D4}$. Similar reasoning can be applied to the parasitic capacitance at the top-most internal node V_{D3}. However, having a big C_{well} will load the V_{D2} node, affecting the efficiency of the stack despite the lower voltage swing at this node with respect to the output swing. A good approach for designing this 4-MOS stack would be minimizing the N-well and increasing the width size of M4 until it fully implements C, along with the given C_{well}. For the design shown in Fig. 3.6(a), an N-well of approximately $100\mu m$ by $200\mu m$ has been considered (this value came from rough sizes of the RF-model layout for two G02-devices, each with a similar size to the ones shown in the final schematic for the 4-MOS cascode, in Fig. 3.6).

The biasing network for M4 allows an RF voltage swing in-phase with the output voltage. It consists of resistor R_{B4}, capacitor C_{B4} and supply voltage V_{GG4}, as shown in Fig. 3.6(a). This network is similar in operation to the one proposed in [24]. In [24], R_{B4} is connected directly across the gate-drain nodes of the top-most device, and hence the technique is called 'self-biasing technique' since the biasing voltage for the 2-MOS cascode in that work and for the top-most device is the same. However, in this case, an additional supply voltage for M4 is needed since the overall V_{DD} supply voltage of this Class E cascode is different than V_{GG4}, due to reliability limits. V_{GG4} sets the DC-voltage and the low-pass R_{B4}-C_{B4} network determines the RF-swing at the V_{G4} node. Interestingly, this biasing scheme is very insensitive to R_{B4} as long as $R_{B4} >> 0$. Note that at RF, there will be an AC-voltage divider between C_{B4} and the gate–drain parasitic capacitance of M4. If V_{GG4} could be the same as the overall V_{DD}, then R_{B4} would be connected across the gate–drain nodes of M4, as in [24], and the AC swing at V_{G4} would come thanks to the swing at V_{D4}.

In the 4-MOS cascode topology of Fig. 3.6(a), a parasitic resonating network has also been tried at different internal nodes to boost the drain efficiency. From PSS simulations, resonating out the parasitics at V_{D3} provided only a marginal improvement with respect to resonating out the parasitics at V_{D2}.



(a) V-waveforms before resonating out parasitics (b) V-waveforms after resonating parasitics out at V_{D3}

FIGURE 3.7: 4-MOS cascode Class E topology voltage waveforms at all internal nodes, for a) before resonating any parasitics out, and b) after resonating parasitics out at V_{D3}.

Figures 3.7(a) and 3.7(b) shows the PSS voltage waveforms at all internal nodes before and after resonating out the parasitics at V_{D3}, respectively. Note that, from Fig. 3.6(b), the reference for the oxide reliable voltage limits for M1 and M2 is the substrate (or ground), and it is the N-well voltage for M3 and M4, which is represented by the voltage at node V_{D2} (marked red in Fig. 3.7). From Fig. 3.7, it can be observed that the oxide at the gate and drain area for M1 and M2 are kept within the most conservative DC-breakdown limits. The gate of M3 is biased at 2.5V to limit the drain voltage swing of M2, ensuring the oxide reliability at the drain of M2 and at the gate of M3. The gate-oxide of M4 is ensured thanks to the swing of the N-well voltage, this is $(V_{G4} - V_{D2})$ and $(V_{G4} - V_{D3})$ are within reliable levels at any time. $(V_{D3} - V_{G3})$ is also within the most conservative DC reliability levels, and so is $(V_{D4} - V_{G4})$ in Fig. 3.7(a). $(V_{D4} - V_{G4})$ in Fig. 3.7(b) would exceed the +10% DC-limit by around 20% due to the resonating network at V_{D3}, but this is expected not to cause any harm at RF (employing an AC-oriented breakdown limit [27]). Table 3.2 summarizes the simulated performance parameters for this 4-MOS cascode

Parameter	65-nm 4-MOS cascode (without resonating parasitics)	65-nm 4-MOS cascode (resonating parasitics at V_{D3})
Frequency [GHz]	2.4	2.4
η [%]	57.3	62.4
PAE [%]	56.3	61.4
$\eta_{overall}$ [%]	54.9	59.8
P_{out} [dBm]	28.8	29.0
Gain [dB]	17.8	18.0
$K_P = P_{out} \cdot R_L / {V_{DD}}^2 \approx$	0.78	0.82
V_{DD} [V]	2.2	2.2
$V_{swing,peak}$ [V]	7.0	7.7

TABLE 3.2: Summary of simulated performance for the 4-MOS Class E topology.

Parameter	65-nm G01-EDG02 cascode in [1]	65-nm single EDG02 in [2]
Frequency [GHz]	2.0	2.0
η [%]	≈ 60	≈ 73
PAE [%]	60	70
$\eta_{overall}$ [%]	≈ 59	N/A
P_{out} [dBm]	30	35.3
Gain [dB]	24.5	≈ 15
$K_P = P_{out} \cdot R_L / {V_{DD}}^2 \approx$	0.26	0.42
V_{DD} [V]	4.8	6.0

TABLE 3.3: Summary of *measured* performance for the Class E implementations in [1] and [2].

topology.

3.3.3 Other topologies employing extended-drain devices

Recent published works [1, 2] have presented the capabilities for efficient high-power operation employing custom extended-drain devices that can be implemented in the same 65-nm CMOS technology [22]. Those works also implemented topologies operated in Class E. The authors in [1] implemented a G01-G02 (standard thin-oxide and thick-oxide) and a G01-EDG02 (standard thin-oxide and extended-drain thick-oxide) cascode topologies. The authors in [2] implemented scalable versions of single EDG02 devices operated in suboptimum Class E mode. Table 3.3 summarizes the *measured* performance metrics from these works.

Observe the high efficiency and high reliable supply voltage of both implementations in standard 65-nm CMOS, shown in Table 3.3. The circuit in [1] has lower drain efficiency (which could be recovered by employing the resonating network proposed in [29]) but increased gain than the circuit in [2], which is due to the cascode approach. Note also the increase of the output power

level in the circuit of [2] due to the use of a suboptimum Class E mode and the use of a scalable layout approach in the design of the EDG02 transistors.

3.4 Conclusions

The design of two cascode topologies employing only standard devices in 65-nm CMOS has been presented and discussed with the aid of Cadence Spectre simulations. The reliable supply voltage increases with the number of stacked devices. However, stacking more than 3 devices requires additional techniques that increases the complexity of the circuitry. Stacking 4 devices required the use of deep N-well, which in turn requires the CMOS technology to have a triple-well option (this is the case for the 65-nm CMOS technology employed along this thesis). The maximum drain efficiency in these cascode topologies was reached by using a single resonating network [29] at the top-most internal node. However, this technique requires the integration of a resonating inductor and a DC-blocking capacitor, which could consume an important silicon area and provides only around 5 to 6% of increase in efficiency. Also, the use of this resonating network will limit the bandwidth. The reliable output swing reached was around 5.6 and 7 V for the 3-MOS and 4-MOS cascode topologies, respectivelly. The 4-MOS cascode had a lower drain efficiency than the 3-MOS cascode, of approximately −6%. From the simulation results, both topologies were able to reach a similar PAE of slightly above 60%. Similar cascode topologies to the ones presented in this chapter can be implemented in deeper sub-micron CMOS technologies, due to the use of only standard devices.

For the specific case of the 65-nm CMOS technology employed in this thesis, the published *measured* results in [1] and in [2] outperform the ones reached in the *simulated* cascode topologies presented in this chapter, as seen by comparing the summary of results in Table 3.3 with the ones in Tables 3.1 and 3.2. This is due to the use of the custom extended-drain thick-oxide transistors available [22]. The EDG02 transistors have lower RF performance (f_T = 30 GHz, f_{MAX} = 52GHz) compared with the standard G02 transistors (f_T = 38 GHz, f_{MAX} = 100GHz) [1]. However, the EDG02 transistor roughly quadruples the breakdown capabilities of the standard G02 device [22]; approximately 10 V against 2.5 V, respectively. For high-voltage swing applications, this breakdown advantage of the ED devices becomes essential and ultimately provides a better circuit performance despite the intrinsic ED transistors' lower RF performance. The ED technology advantage provides finally higher PAE and simpler circuits, since no cascoding complexity is needed (and hence its associated efficiency degradation is avoided). Additionally, the

lower gain of the EDG02 devices could be overcome by novel EDG01 devices (see Appendix A for more details about both devices).

Chapter 4

Inverter-based driver approach for HV swings, design and implementation

4.1 Introduction

The significantly increased breakdown capabilities of the extended-drain transistors in 65-nm CMOS leads to more efficient high-voltage/high-power circuits, compared to the use of standard CMOS devices (Chapter 3). Therefore, the use of such devices becomes a logic choice for further exploration towards high-voltage RF circuits.

In practice, DC-feed inductors will not be ideal and they contribute to efficiency loss when implemented. This efficiency loss can be 10% to 20% for bondwire inductors and integrated inductors, respectivelly (refer to Appendix C for details). These inductors, however, are important components in all amplifing topologies, except of the Voltage-Mode Class-D (VMCD) amplifier. This later topology uses an extra transistor (in general a PMOS) to replace the DC-feed inductor. Still, either component will not be ideal, leading to power losses in both cases. However, a reconsideration of the VMCD topology on the basis of lossy integrated inductors can be made.

It is known that the VMCD circuit will be less efficient at higher frequencies than a comparable Class E circuit [11], but the VMCD-like, or inverter-based, CMOS circuits can be used as high-voltage drivers for the high-power transistors employed in base-station applications (e.g. [4]). The base-station power amplifier itself can be implemented in Class-E. At the system level, i.e.

the complete amplifier lineup, the efficiency of the driver will be less critical than the efficiency of the PA stage. So, providing an adequate waveform at the gate of the PA should be the highest priority of the driver. This waveform is a square-wave for a Class-E GaN PA [5].

In this chapter, an inverter-based high-voltage driver circuit topology is explored as the second approach towards high-voltage CMOS driver circuits. This exploration finally led to the design and implementation of CMOS driver circuits in 65-nm technology. Because of the inductor-free nature of this new approach, broadband operation is now possible. Also, duty-cycle control in the driver can be easily implemented, which can be a valuable feature for broadband Class-E power amplifiers (see Section C.3 of Appendix C for details). This duty-cycle capability was added to the CMOS driver topology described in this chapter.

Employing the special extended-drain transistors EDG01/EDG02 [22] in an inverter-based driver topology will enable to reach high-voltage swings in baseline CMOS technology, without sacrificing efficiency (like in the cascode topologies explored previously in Chapter 3). Output swings in the order of 5V have now become feasible but special design and layout techniques will be needed for the CMOS drivers to come to successful implementations.

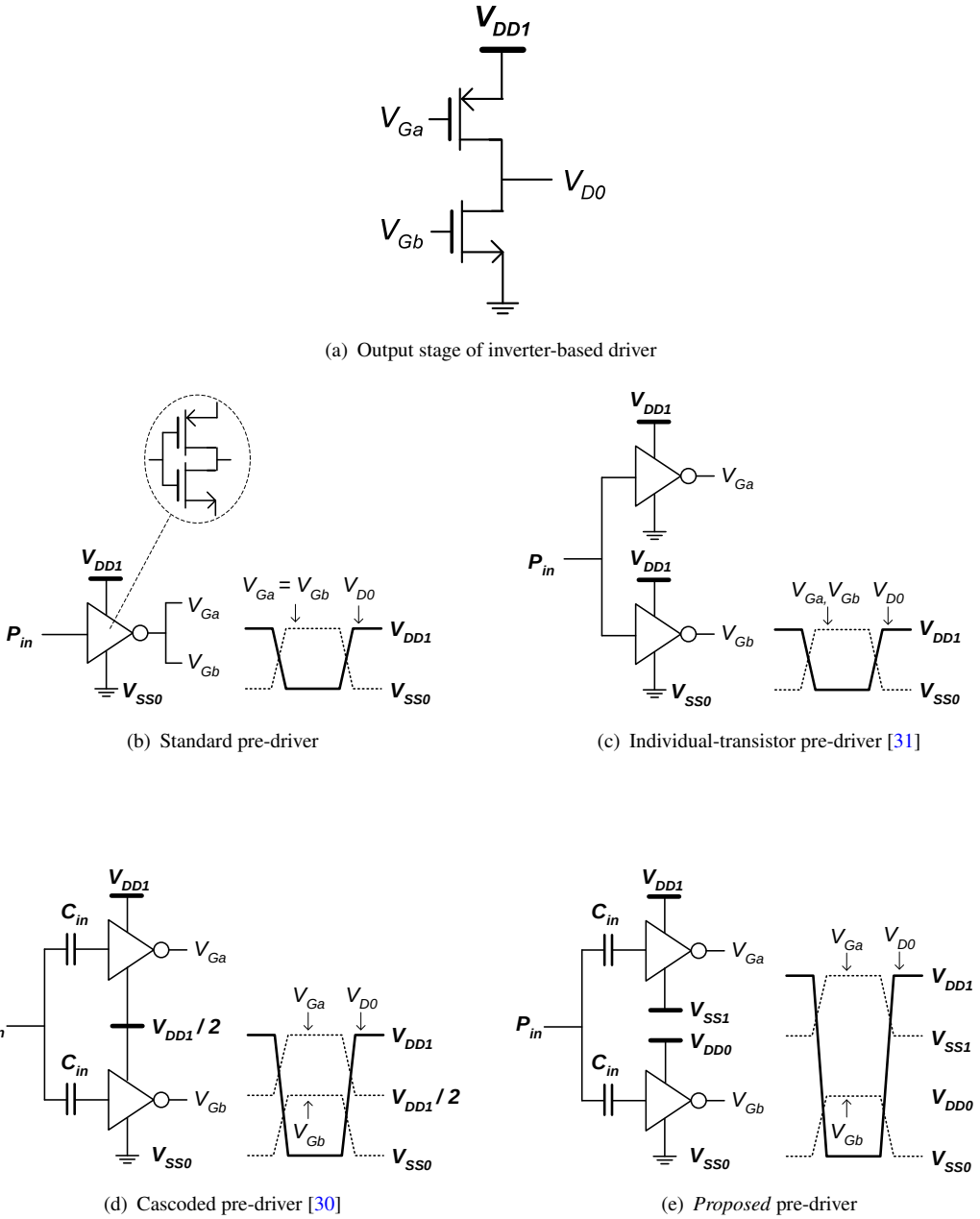
Three CMOS drivers are described in this chapter. CMOS driver I and II employ thin-oxide devices with an extended-drain, while CMOS driver III uses thick-oxide devices with an extended-drain. CMOS driver I is the only driver that includes pre-driving stages (implemented with standard thin-oxide devices). CMOS drivers II and III are based on the design of CMOS driver I. Therefore, the detailed design description is focused in the first CMOS driver.

4.2 Inverter-based driver topologies

4.2.1 General inverter-based driver topologies

The output stage of an inverter-based driver topology is a classical CMOS stage consisting of a pull-up (PMOS) and a pull-down (NMOS) device, as shown in Fig. 4.1(a). There are, however, several options for driving such a stage. The selection on the driving stage will determine the maximum reliable swing of the output stage.

Figure 4.1(b) shows an standard inverter-based pre-driving stage. This topology severely restricts the supply voltage of the complete circuit to the lowest gate-oxide breakdown voltage



(a) Output stage of inverter-based driver

(b) Standard pre-driver

(c) Individual-transistor pre-driver [31]

(d) Cascoded pre-driver [30]

(e) *Proposed* pre-driver

FIGURE 4.1: Inverter-based driver topologies (different pre-driving stages): a) output stage, b) standard pre-driving stage, c) individual-transistor pre-driving stage [31], d) cascoded pre-driving stage [30], e) *proposed* pre-driving stage.

limit of any of the transistors in the complete circuit. In general, this limitation comes from the pre-driving transistors rather than from the output ones (in case of using different transistors). The topology in Figure 4.1(c) is similar to the topology in Fig. 4.1(b) but it reduces the power loss at the output stage due to the 'shoot-through' (or 'direct-path') current[1] due to the use of individual (and properly sized) pre-driving stages for each output device [31]. However, this last pre-driving stage also suffers from the same voltage supply limitation as the first one. These two topologies are not adequate for employing extended-drain devices at the output stage due to the voltage limitation of the pre-driving stage, which in general is implemented with the faster standard devices.

The extended-drain devices can have 2X to 4X (or more) higher breakdown voltage capability at the drain–gate oxide area that at the source–gate oxide area [22] (this last one is equal to the one of an equivalent standard device), at the expense of reduced intrinsic RF performance. Then, it is important to exploit the full breakdown capabilities of the ED devices to overcome their reduced performance.

Figure 4.1(d) shows a cascoded inverter-based pre-driving stage. It can be observed that this topology doubles the reliable voltage supply that can be employed and hence allows the use of extended-drain devices at the output. The pre-driving stage would be made of standard devices. Due to the cascoding, there is a need for voltage level shifters at the input of each pre-driving buffer. This voltage shifter is made by an AC-coupling capacitor and a biasing circuitry at the input of the buffers. This topology needs Deep N-well. The internal node in Fig. 4.1(d), biased at $V_{DD1}/2$, can be externally supplied (requiring complex layout) or generated internally by voltage division (and filtering) or by self biasing in a differential implementation (no additional external supplies are required) [30]. However, this topology still does not exploit the maximum capabilities of the extended-drain transistors because of its maximum 2X increment in the supply voltage, when the ED transistors could support more. Additionally, if EDG02 devices were used, then the supply voltage would be limited at 5V and high input power would be required (due to the use of standard 2.5V G02 devices in the pre-driving stage). If (1.2V) EDG01 devices were employed to reduce the input power, then the output swing would be limited at $\approx$ 2.5V, which is not high enough for the driver in this work.

[1] During the ON-OFF transition of the active devices at the output stage, there is generally a short period of time when both PMOS and NMOS transistors could be simultaneously ON, resulting in a momentary low resistance path between power supply and ground. This is known as the 'shoot-through current' and it is an important source of power dissipation.

4.2.2 The proposed driver topology

The pre-driving circuitry shown in Figure 4.1(e) is the one proposed in this thesis to reach high voltage swings employing the inverter-based approach for HV drivers. This topology will also need a triple-well process due to the use of Deep N-Well. The Deep N-Well is needed due to the two sets of supply voltages observed in Fig. 4.1(e). This will require special layout techniques to provide that many low-ohmic and high power internal traces (this issue will be addressed later in this chapter). Each supply voltage set ensures the reliability of the pre-driving stages by limiting the voltage between the local supplies of each pre-driving stage. This is, $V_{DDx} - V_{SSx} \leq 2.5V$ if G02 devices are employed and $V_{DDx} - V_{SSx} \leq 1.2V$ for G01 devices in 65-nm CMOS. Observe that the swing required at the input of the ED devices is the same as the voltage supplying the two buffer chains in Fig. 4.1(e), while the output swing of the ED devices can be orthogonalized. Then, the output can swing at $V_{DD1} - V_{SS0}$, and hence it could be adjusted depending on the drain-oxide breakdown limit of the ED devices. Since the breakdown limit of the gate-drain voltage of the EDG01 devices is expected to be at least 5V, then G01 devices were decided to be used in the main CMOS driver design. A G01-based driver will require less than 4X input power compared to an G02 solution. Additionally, all the internal swings in the driver will be limited at 1.2V for the case of a G01-based design, limiting the $\propto f \cdot C_P \cdot V_P{}^2$ losses at those internal P nodes. Hence, the efficiency of a G01-based driver will be dominated by the output node, which will swing at, for example 5V[2].

The proposed topology is rather general and hence even larger output swings can be reached by employing G02-based devices. However, the design in this thesis focuses on the G01-based solution (CMOS drivers I and II), since only 5V output swing is required for driving GaN transistors. The design of CMOS driver III, which employs EDG02 devices, was done to quantify the differences between employing EDG02 and EDG01 devices. In all the drivers, the output voltage swing is controlled by the main supply voltage. However, in the CMOS driver I, the use of two supply sets gives freedom in the final output voltage swing without compromising the reliability of the pre-driving stages.

Interestingly, observe that the topologies of Figs. 4.1(c), 4.1(d) and 4.1(e) are all equal from an AC signal point of view. However, the proposed topology in Fig. 4.1(e) enables the swing

[2]Assuming similar internal node capacitances, then the dissipated power at the output node is expected to be at least 17X higher than at any other internal node.

of the output stage (Fig. 4.1(a)) to be freely set and hence to reach its maximum level without compromising the reliability of the entire CMOS driver.

4.3 Circuit and layout design description for the CMOS driver I

The design and layout of high power circuits in CMOS is a very challenging task. A simultaneous circuit and layout design becomes essential for this type of high power circuits. The circuit design and the layout phase usually goes hand by hand since the overall chip floor plan, the multiple power traces, the big transistor sizes, etc., become critical and minimizing the parasitic elements is of primordial importance. Additionally, many traces in this design must be very low ohmic (e.g. all the supply and output lines) requiring wide traces in the top metal layers. This section describes the main steps taken during both circuit and layout design phases for the implementation of the CMOS driver I.

In the design of this CMOS driver a P–Cell (Parameterized Cell [32]) approach was used for almost all of the blocks in the layout. The final driver layout was in the order of some mm^2, so using the P–Cell layout strategy proved to be very useful due to the complexity and limited time of the design.

4.3.1 Initial considerations

4.3.1.1 Target specifications

The CMOS driver is intended for driving high-voltage (e.g. 5V) input transistors in switchmode-based power amplifiers (e.g. Class E) for base-station applications. An example of such loads is a GaN HEMT transistor [33], which has a typical input capacitance of 3.7pF. For the design of the CMOS driver a lumped capacitance load of 5pF was considered for generality. Figure 4.2 shows an schematic of the intended application of the CMOS driver circuit designed in this chapter.

Table 4.1 summarizes the requirements of the CMOS driver. Table 4.2 summarizes the extra features that the proposed driver topology brings along.

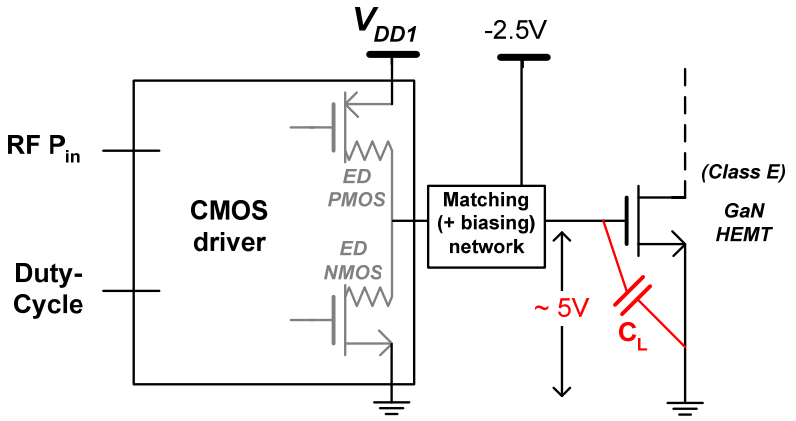


FIGURE 4.2: Schematic for the intended application of the CMOS driver circuit.

Specification	Target value
Output voltage swing	5 V
Operating bandwidth	2.1 to 2.7 GHz
Duty-cycle control	30 to 70%
Layout	for out-phasing systems

TABLE 4.1: Summary of target specifications for the CMOS HV driver.

Additional features
Adaptable supply voltage (and output swing)
Integrated AC-coupling and -decoupling capacitors

TABLE 4.2: Summary of additional features in the CMOS HV driver.

4.3.1.2 Duty-cycle control requirement

One of the added features in the CMOS driver is duty-cycle control to enhance the efficiency of the final PA stage. In Section C.3 of Appendix C it is shown that duty-cycle control can recover efficiency at back-off power levels. This was demonstrated through simulations of a broadband Class E GaN HEMT power amplifier with ideal driving that was backed-off by both load and supply modulation.

The duty-cycle control functionality is implemented by controlling the gate biasing levels of each of the inverter chains in Figure 4.1(e). This technique is called *Pulse Width Modulation by Variable Gate Bias* (PWMVGB) [34, 35]. The biasing level V_{GG} at the input of each inverter shifts up/down the input signal v_{in} with respect to the switching threshold level V_M of the first inverter in the chain, varying the duty-cycle of the output signal v_{out}. Two cases illustrate the operating principle of PWMVGB in Figure 4.3.

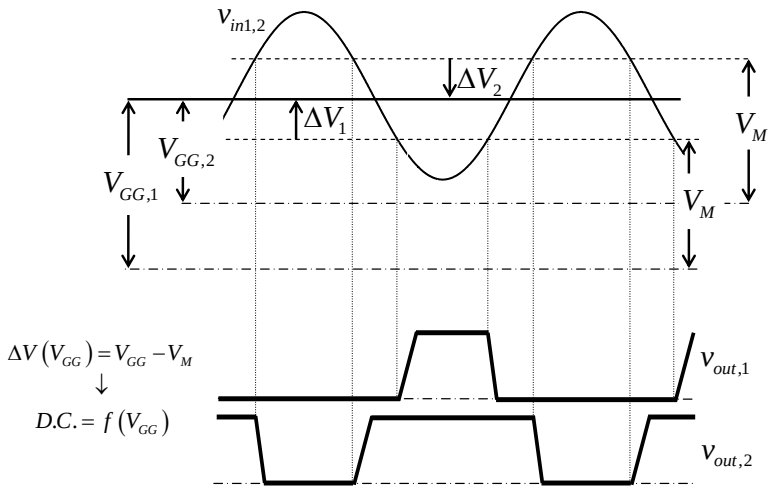


FIGURE 4.3: Operating principle of PWMVGB. The duty-cycle (*D.C.*) is a function of the gate biasing level V_{GG} of the input signal V_{in}.

PWMVGB is applied to each driving inverter chain of the CMOS driver. Hence, there are two biasing signals ($BIAS_a$ and $BIAS_b$) with a voltage difference approximately equal to the offset between the two voltage supply sets. However, the voltage difference between $BIAS_a$ and $BIAS_b$ can be slightly modified in order to reduce the 'shoot through current' at the output stage to prevent additional power dissipation. If this voltage difference is further modified, then the operating mode of the CMOS driver could go from a Class-D to a Class-DE like (i.e. the dead times are controlled by the gate biasing levels of the two inverter chains).

4.3.1.3 NMOS/PMOS transistors size ratio

The PMOS and NMOS transistors of an inverter are normally sized to accomplish a symmetrical voltage transfer curve (VTC) and to equate the high-to-low and low-to-high propagation delays. If symmetry and reduced noise margins are not of prime concern, another sizing possibility is to minimize the overall propagation delay by reducing the width of the PMOS device [36].

In the specific case of the CMOS driver of this chapter, the size ratio between the NMOS and PMOS transistors in each CMOS block (output and pre-driving stages) was set to one. This is justified by the following observations. For the CMOS driver application, the VTC and the noise margins are not of primary importance. Reducing the overall propagation delay (or equivalently the total rising and falling times) is still very important. However, more important than reaching a minimum total propagation delay is ensuring a proper driver operation and keeping its efficiency as high as possible. From the overall driver topology, shown in Fig. 4.1(e), the RF input signal is split into two signals, one per (top and bottom) inverter chain. Those signals

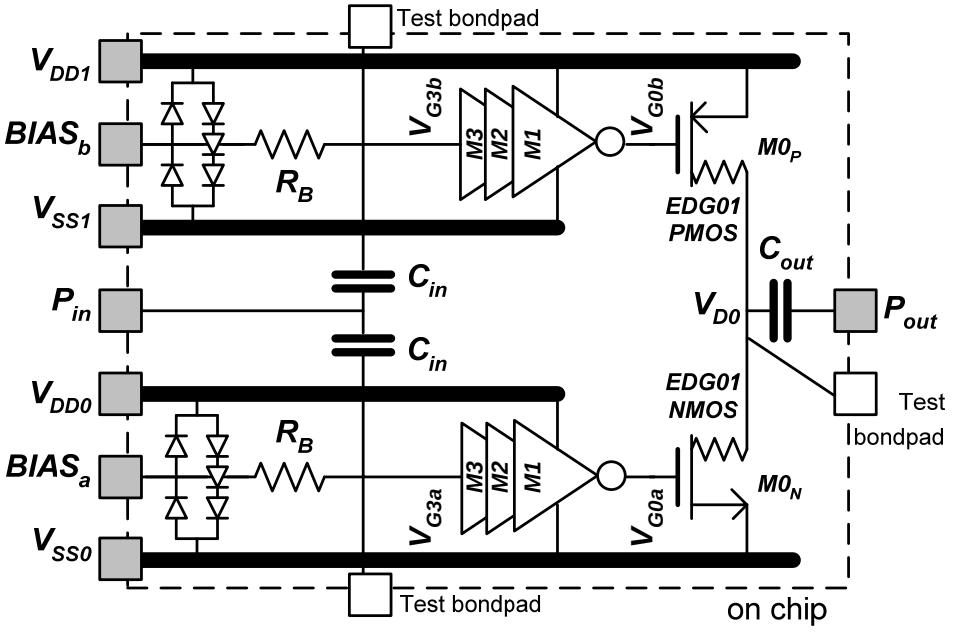
pass through the inverter chains before reaching the output stage. This requires a high degree of symmetry between those two inverter chains in order to precisely control the activation of the EDG01 devices at the output by means of the PWMVGB technique. A phase shift difference between those two inverter chains could lead to a poor control on the overall output duty-cycle and/or an increase of the 'shoot through current' at the output stage. Hence, by equally sizing the output EDG01 devices, the load seen by the inverter chains is approximately equal and then they can be designed identically. Now, if each PMOS and NMOS are of the same size within each inverter in the pre-driving chain, they can be designed from a single block that can be just scaled accordingly, simplifying the layout activity and ensuring symmetry in the layout. The overall chip layout symmetry is highly desired and it also simplifies the power routing strategy.

By making the size of the PMOS equal to the NMOS, the low-to-high propagation delay will be undoubtedly larger (or equivalently, the rising time will be larger) with respect to the high-to-low propagation delay (or equivalently, the falling time). However, in a Class E power amplifier, the falling time at the input control signal is more critical than the rising time [37]. This is because the switch current in the Class E amplifier during the ON-state is suddenly stopped when the power switch is turned OFF. When the Class E switch is turned ON, generally the switch current starts circulating with an smaller slope (please, refer to the current waveform in Fig. B.2 of Appendix B). Hence a faster turn-OFF signal (i.e. a faster falling time) is required from the CMOS driver than a turn-ON signal. Then, sizing PMOS and NMOS transistor equally does not negatively affect the Class E power amplifier following the CMOS driver circuit.

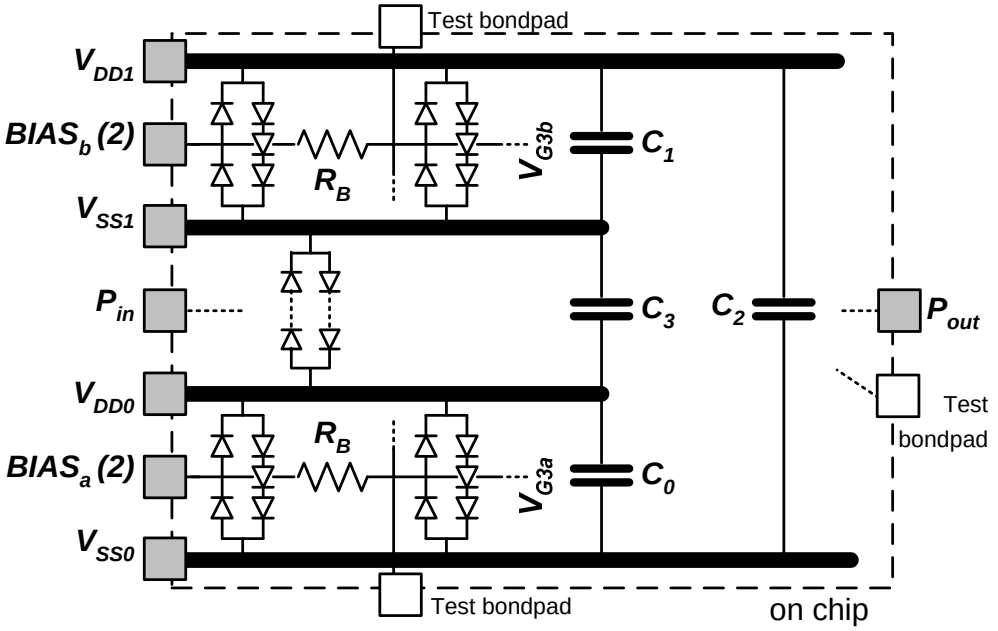
The duty-cycle information is preserved through the entire inverter chains by equating the rising and falling times of all the inverter stages. However, equal rising and falling times are not required in the same inverter stage for this purpose.

4.3.1.4 Out-phasing system oriented layout requirement

The CMOS driver chip is also intended to be used in an out-phasing system and hence the complete chip layout and pin-out must be symmetric with respect to an axis (e.g. the horizontal axis), since two chips will be placed side-by-side in the real application. More details about this out-phasing oriented layout will be discussed in a later section. For now, it is important to realize that this out-phasing oriented layout led to some non-functional redundancy of some blocks and pin-out.



(a) Main functional schematic (CMOS driver I)



(b) ESD and decoupling capacitors schematic details (CMOS driver I)

FIGURE 4.4: Top schematic view of the implemented CMOS driver I: a) main functional schematic, and b) ESD and decoupling capacitors schematic details.

4.3.2 General schematic for the CMOS driver I

The general schematic of the CMOS driver I is shown in Figure 4.4. Fig. 4.4(a) shows the functional circuit schematic of the implemented design. The implemented circuit has two equal biasing inputs (*A* and *B*) per each inverter buffer branch, due to the out-phasing layout oriented

requirement explained previously (see Fig. 4.17(a) in a later section for details). Fig. 4.4(b) shows the AC-decoupling capacitors that were integrated into the same chip to stabilize the circuit against the effects of the parasitic inductance of the bondwires (not shown in the figure). Also, Fig. 4.4(b) shows the ESD circuitry that was implemented to protect the chip. In the following sections, a detailed explanation for the design of each of the blocks in Fig. 4.4 is presented.

4.3.3 Output stage design

The CMOS driver should turn ON-OFF its intended transistor load with variable duty-cycles, from approximately 30 to 70% (targeted duty-cycle) in a 2.1 to 2.7 GHz bandwidth. Therefore, the design criteria for sizing the output stage was to be able to meet the following condition

$$\frac{\left(t_r + t_f\right)}{T_{min}} < 0.3 \tag{4.1}$$

where t_r and t_f are the rising and falling times at the output node (including the load), and T_{min} is the smallest time period (i.e. the one at 2.7 GHz). It is important to realize that sizing the output transistors is somehow an iterative task during the complete design of the driver. The parasitics coming from the layout of a big transistor can be as large as the device intrinsic capacitances [2] and they greatly depend in the layout strategy. Also, the lateral parasitic capacitances of the output AC–coupling capacitor in Fig. 4.4(a) will load the output node as well. These parasitic capacitances can be obtained after some layout activity through extracted layout views and then the output stage can be finely tuned with this information. For the sizing of the output stage, there is a trade-off between the speed of the driver and its power consumption [36]. After extensive extracted layout view simulations of several layout implementations for the output transistors, their total width transistors was determined to be 4032 μm, for both PMOS and NMOS (as explained before).

4.3.3.1 Unit transistor (P)cell design

Due to the great influence of the layout capacitive parasitics in the RF performance and in the circuit efficiency [1, 2], the layout of each big EDG01 transistor was split up in hundreds of small interconnected unit transistor (P)cells. The number of these unit cells equals to the ratio

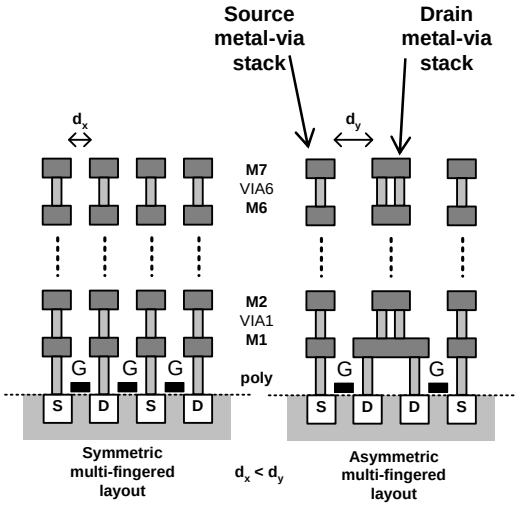


FIGURE 4.5: Cross section view for the symmetric and asymmetric multi-fingered transistor layouts.

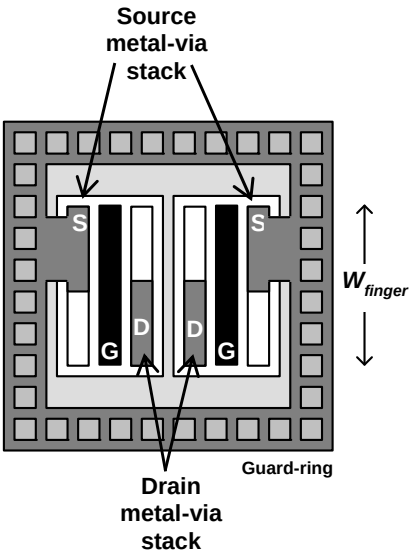


FIGURE 4.6: Top view for a unit transistor P–cell with two fingers.

between the total transistor width and the total gate width within each of those P–cells. The procedure for determining the gate width within each unit cell will be addressed soon.

Each of these custom-made P–cells was optimized to reduce the parasitics, and it contains a small multi-fingered transistor with all its interconnections up to metal 7 (M7). The transistor P–cell also includes its own guard-ring and substrate connections, and employs an asymmetric multi-fingered transistor layout [38] instead of a classical multi-fingered layout. Figure 4.5 shows both types of multi-fingered transistor layouts. The asymmetric layout allows larger metal track distances which decreases the parasitic metal interconnection capacitances of the final transistors [2]. This comes at the price of an increased silicon area of the P–cell, i.e. there is a trade-off between the P–cell area and the parasitic capacitances. However, this added area could be considered negligible at the complete circuit level, since the overall chip size depends in other blocks (e.g. bondpads, AC-decoupling capacitors, etc) rather than in the active devices. Additionally, the drain–source parasitic capacitance is further reduced by separating as much as possible the drain and source metal–via stacks, as seen in the unit transistor P–cell of Figure 4.6 (it can be observed that the Source metal–via stack does not extend all the gate width and it is flipped horizontally with respect to the Drain stack, reducing the side-to-side parasitic capacitances).

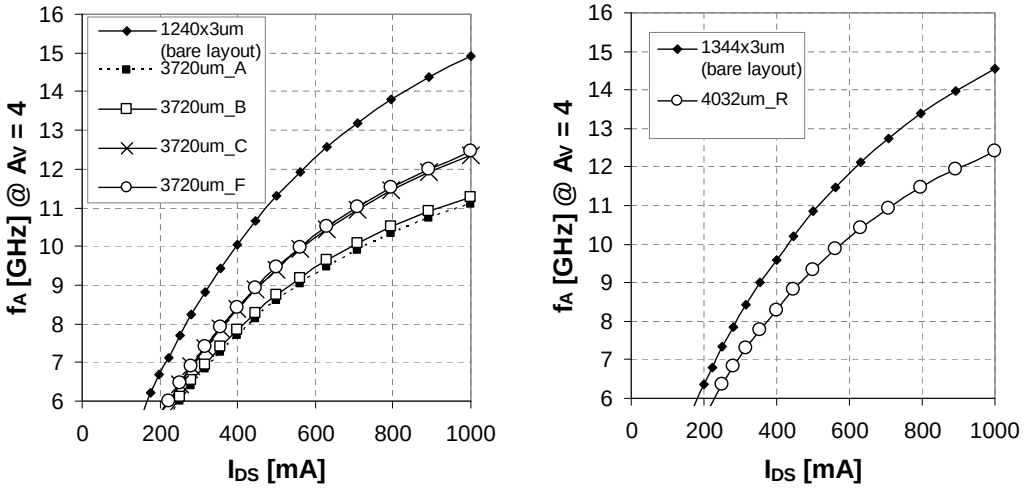
The design of the unit transistor P–cell involves other considerations as well. The maximum size of a single P–cell is determined by the substrate ohmic connection. In order to ensure a

low ohmic connection (which is quite important at RF) to the substrate, a customary practice is to restrict the unit transistor cell size to about 10 by 10 μm. Within this area, several transistor fingers can be placed inside a single guard-ring, as illustrated in Fig. 4.6. Optimizing the finger width within each P–cell is also very important, since it will highly influence the RF performance of the final transistor. A convenient procedure for this purpose is by obtaining a figure-of-merit called *available bandwidth*, f_A, for several layout implementations of unit transistor P–cells with varying finger widths until the finger width that maximizes f_A is found [1].

The available bandwidth, f_A, is defined as the $-3dB$ bandwidth of the voltage gain of a common-source stage loaded with a resistor so that the low-frequency DC voltage gain is fixed to a given value. A gain of four is often used in logic applications while a larger gain (e.g. 10) is often used in analogue applications [39]. The use of f_A has advantages as compared to f_T (current-gain cut-off frequency) or f_{max} (maximum oscillation frequency). Unlike f_T or f_{max}, f_A can be measured without any extrapolation [39]. Furthermore, f_A is a much better representation of the actual delays involved than f_T or f_{max}, since it is determined by both input and output parasitic capacitances [1, 39]. f_T assumes that the output of the transistor is short-circuited, while f_{max} assumes simultaneous input and output conjugate matching to the rest of the circuit. These are rather specific-application assumptions. Additionally, f_T is primarily used for the optimization of the *intrinsic device* while the available bandwidth is a measure of the influence of the device parasitics on the accessibility of the intrinsic device by the external voltages at high frequencies [39].

Hence, maximizing the f_A will provide a good indication for an optimal transistor layout and hence RF circuit performance [1]. This applies to either the unit transistor P–cell layout design or to the arrangement of such unit cells into the total transistor. It is important to realize that f_A can be used to compare the performance between different layout implementations of the same transistor despite of the specific value of the DC voltage gain employed, as long as this value is kept constant.

Due to the novelty of the EDG01 device (refer to Appendix A for further details), the layout optimization strategy was slightly modified for the output stage. Accurate simulations for the EDG01 devices were not possible due to the absence of an official electrical model for it. Then, a finger width of $3\mu m$ was decided based in the available information, the initial device samples and the experience from the design team at NXP Semiconductors. Normally, a formal procedure would be followed to get this value (based in the optimization of multiple P–cell layout designs



(a) EDG01 NMOS of $W_{total} = 3720\mu m$

(b) EDG01 NMOS of $W_{total} = 4032\mu m$

FIGURE 4.7: f_A test results for several layout implementations for the output EDG01 NMOS transistor, with a total width of a) 3760 μm, and b) 4032 μm (final implementation).

until maximizing the f_A of one of them). A P–cell for the EDG01 device was built a long with an equivalent version based in standard G01 devices. The idea was that the equivalent layout based in G01 devices could be used to perform accurate simulations and hence layout extractions, and the real EDG01 layout could not. Then, the layout optimization for the EDG01 transistors was based in this equivalent G01 layout and at the end, the devices were replaced accordingly (in the final CMOS driver layout).

In Figure 4.7(a) it can be seen part of the optimization process of the overall output transistor. An NMOS output transistor of total width $W_{total} = 3720\mu m$ was implemented in several versions, each of them yielding different f_A, as it can be observed in the figure (only few layout implementations are reported for brevity). In the same figure, the performance of an equivalent 'bare layout' can be observed as reference for the maximum performance. This bare layout consisted in the layout of the whole transistor but just up to metal 1 (M1) employing ideal interconnections between the individual P–cells. The other results in Fig. 4.7(a) correspond to complete transistor implementations up to M7. The final transistor was based upon the best implementation shown in Fig. 4.7(a), and it was increased in size up to its final size of $W_{total} = 4032\mu m$, due to the fine sizing activity towards the end of the CMOS driver design. In Figure 4.7(b) the f_A of the final output transistor implementation can be observed, along with an equivalent 'bare layout' transistor of the same size as reference. All the f_A values were obtained by using an NXP Semiconductors proprietary script in Cadence Spectre [40] that automatically calculated the f_A from the extracted layout views of each implemented transistor layout.

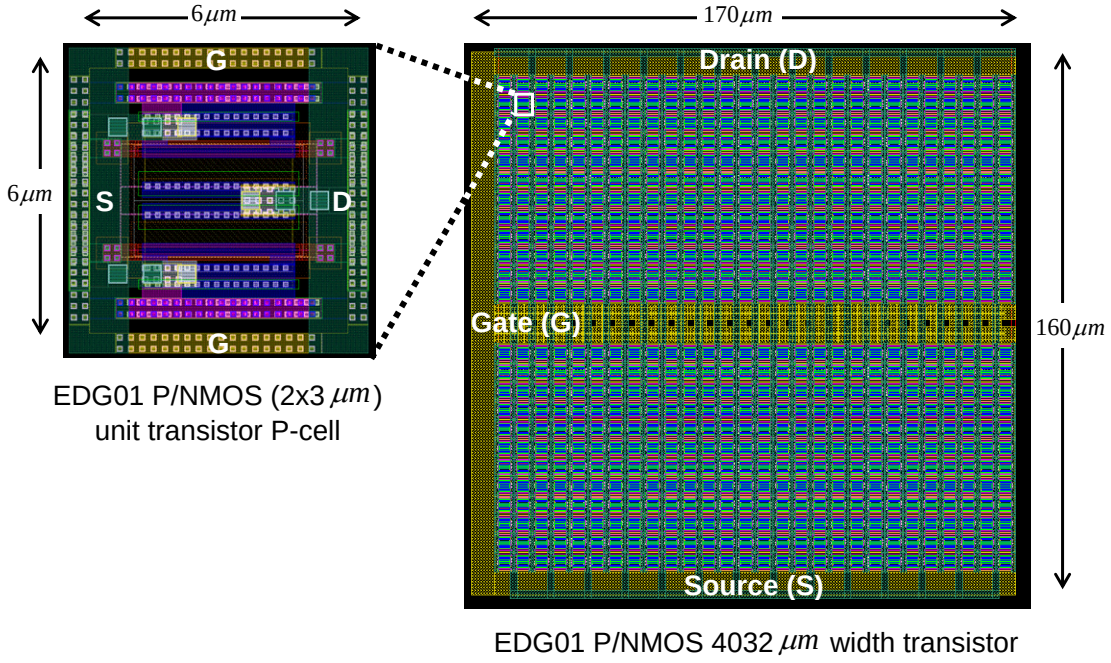


FIGURE 4.8: Layout view of the EDG01 NMOS output transistor, showing the detail of a single transistor unit P–cell.

4.3.3.2 Final layout implementation

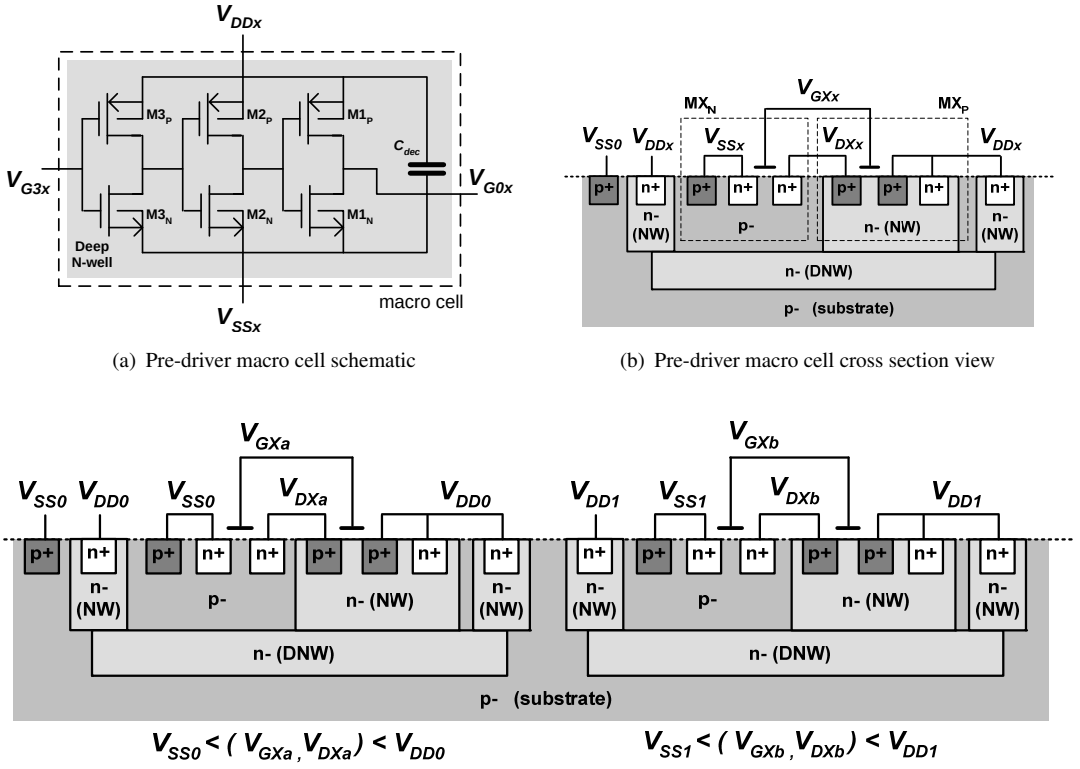
The final implemented layout of the NMOS EDG01 device can be seen in Figure 4.8. The layouts of both EDG01 PMOS and NMOS are identical (except, of course, of the intrinsic devices). In the same figure, the layout view of a single transistor unit P–cell can also be observed.

4.3.4 Pre-driver design

The pre-driver block is the chain of inverters M1 to M3 shown in the schematic of Fig. 4.4(a). As it can be seen in the figure, there are two identical blocks and each one drives one of the EDG01 output transistors. Since both EDG01 transistors are of the same size, the load of each pre-driver is the same, and hence a single design for this block is possible. The schematic of the pre-driver block can be seen in Figure 4.9(a). The transistors employed in this block are all standard G01 devices of 1440, 480 and 240 μm total width for M1, M2, and M3, respectively. Those transistor sizes were found by extensive PSS Cadence Spectre simulations and they preserve the duty-cycle information along the complete transistor chain, following the condition in eq. (4.1) at each stage. Table 4.3 summarizes all the transistor sizes in the CMOS driver.

Device type	EDG01	G01	G01	G01
Device reference	M0	M1	M2	M3
W_{total} [μm]	4032	1440	480	240
W_{finger} [μm]	3	3	3	3

TABLE 4.3: Summary of all the transistors sizes in the CMOS driver. See the schematic of Fig. 4.4(a) for each transistor reference.



(a) Pre-driver macro cell schematic

(b) Pre-driver macro cell cross section view

(c) The two pre-driver macro cells cross section

FIGURE 4.9: Details for the design of the pre-driver circuit block (M1–M3): a) schematic for the pre-driver macro cell, b) cross section view for the pre-driver macro cell at transistor MX, and c) cross section view for the two pre-driver macro cells at transistor MX.

4.3.4.1 Use of Deep N-Well

The only difference between the two pre-driver blocks in Fig. 4.4(a) is their DC biasing levels. In order to allow having two different sets of supply voltages (V_{SS0}-V_{DD0} and V_{SS1}-V_{DD1}), the three inverters shown in Fig. 4.9(a) were placed inside a Deep N-well (DNW). This is possible in the 65-nm CMOS technology employed in this thesis, since it has triple-well option. The use of this DNW permitted the design of a single and generic 'macro cell' for the pre-driver block. A cross section view showing the details of the common pre-driver macro cell is shown in Figure 4.9(b). In that figure only a standard CMOS pair can be seen (MX$_P$-MX$_N$). This CMOS pair represents any of the inverters (M1 to M3) in the chain. Underneath of the 3 inverters in

the macro cell a Deep N-well was placed, as shown in Fig. 4.9(b) for one of such inverters. In order to ensure a proper operation of the inverter-chain and of the DNW, the DC-biasing scheme showed in the same figure must be followed. Observe that the DNW is biased at the highest DC-level of the inverter-chain (i.e. V_{DD1} or V_{DD0}, depending on the macro cell location) by using NW strips in the outer edges of the complete structure. The bottom substrate must be biased at the lowest DC-level in the CMOS driver, i.e. at ground. This will ensure that the DNW is kept reverse biased with respect to the bottom substrate during the driver operation, providing isolation to the inverter chains regardless of their specific biasing levels. As observed in Fig. 4.9(b), each of these NW strips contacts the DNW, and wide metal–contact stacks provide a low ohmic connection between the NW strips and the V_{DDx} supply lines (which are in the top metal layers –M6 and M7– of the chip).

Figure 4.9(c) depicts a cross section view of the two macro cells placed in the same bottom substrate. This is a very close representation of the implementation of the two pre-driver blocks in the real CMOS driver I chip. The bottom substrate is biased at V_{SS0} or ground, as stated before. The DNWs are biased at V_{DD0} and at V_{DD1} for the pre-driver blocks driving the EDG01 NMOS and PMOS output transistors, respectively. This will create two local (isolated) substrates at each pre-driver circuit block, biased at V_{SS0} and at V_{SS1}, respectively. Then, each of the inverter chains will be biased at one of the two supply voltage sets (V_{SS0}-V_{DD0} and V_{SS1}-V_{DD1}) and will work as normal inverter chains, but at different DC-levels!

This arrangement permits to have two equal magnitude RF voltage swings at different DC-levels at the input of the EDG01 NMOS and PMOS transistors, as shown in Fig. 4.1(e). And this in turn, will allow to freely set the overall CMOS driver I supply voltage without compromising the reliability and performance of any active device in the CMOS driver, as intended. This is of great importance. Due to the employment of thin-oxide devices in the complete CMOS driver, the following requirements must be observed by the two sets of voltage supplies:

$$V_{DD1} - V_{SS1} \leq V_{DD,G01,max} \tag{4.2a}$$

$$V_{DD0} - V_{SS0} \leq V_{DD,G01,max} \tag{4.2b}$$

$$V_{DD1} - V_{SS0} \leq V_{DG,EDG01,max} \tag{4.2c}$$

$$V_{SS1} - V_{DD0} \leq V_{ESD,rev,max} \tag{4.2d}$$

(4.2e)

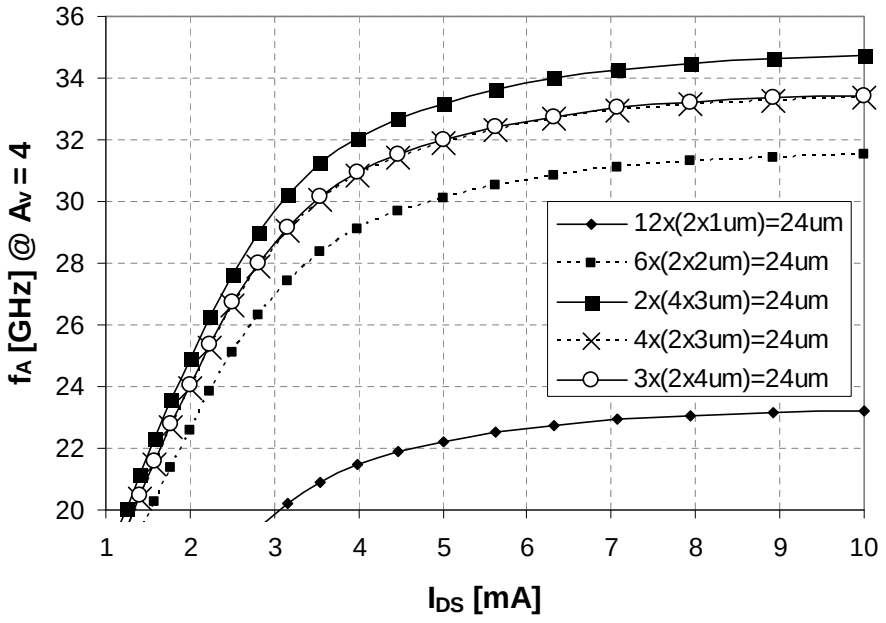


FIGURE 4.10: f_A results for several G01 NMOS unit cell implementations as a function of biasing current.

where $V_{DD,G01,max}$ is the breakdown voltage limit of the thin-oxide devices (1.2V using the nominal 65-nm CMOS supply voltage limit or +10% that value [24] [3]), $V_{DG,EDG01,max}$ is the gate–drain breakdown voltage limit of the EDG01 PMOS and NMOS devices[4], and $V_{ESD,rev,max}$ is the maximum voltage to keep the ESD protective diodes between V_{SS1}-V_{DD0}, shown in Fig. 4.4(b), reverse biased. The $V_{DD,G01,max}$ limit ensures the reliability of the entire pre-driver block and the oxide at the gate–source area of the EDG01 output transistors.

4.3.4.2 Optimum unit transistor (P)cell design

Each of the transistors in the pre-driver block were also split up into smaller unit transistor P–cells, as for the case of the output transistors. However in this case, after the unit transistor cell was optimized, a CMOS (PMOS-NMOS) cell was formed and used as the basic building block of each inverter.

The optimum finger width for the standard G01 devices in the unit cell was obtained through the following procedure. The f_A of a 'sample' G01 NMOS transistor was measured for different unit

[3] As discussed previously, this is the most conservative DC-based oxide reliability limit. An extended AC-based limit can be explored experimentally, due to the freedom in setting the biasing voltages of the complete CMOS driver.

[4] This breakdown limit is unkown at the moment, but can also be explored experimentally with this CMOS driver circuit.

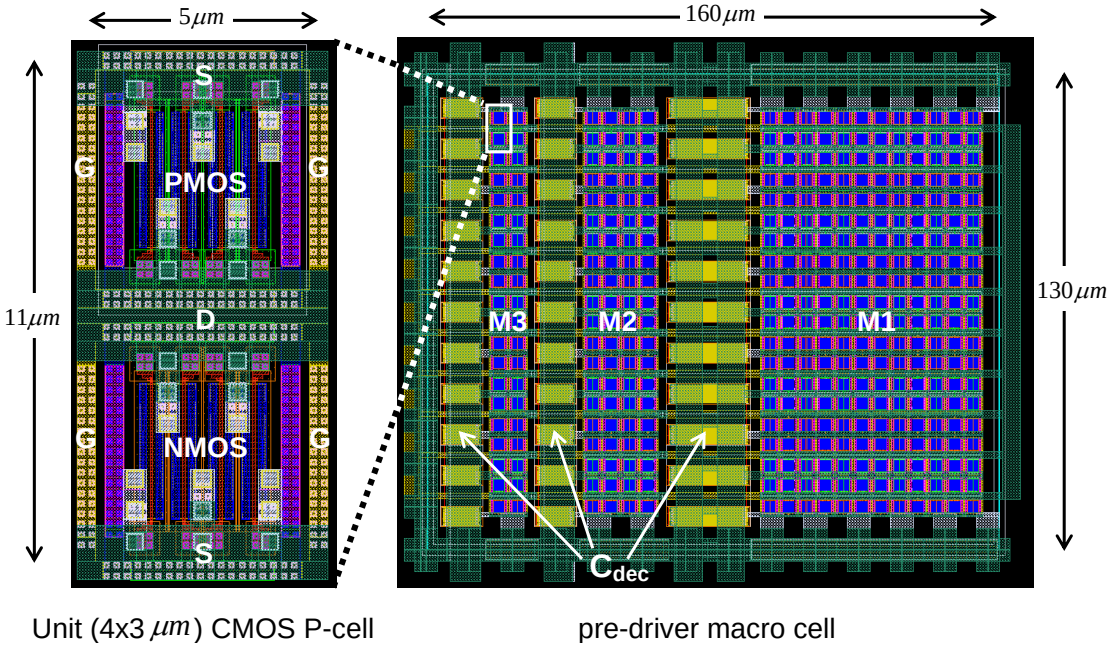


FIGURE 4.11: Layout view of the G01 pre-driver macro cell, showing the detail of a single CMOS unit P–cell.

cell layout implementations[5]. This sample transistor had a total width of 24 μm, and five unit cells with different finger widths were created. From [1] it was known that the optimal finger width of the standard G01 devices in 65-nm CMOS was smaller than 6 μm. Then, the finger widths of the unit G01 cells were 1, 2, 3 and 4 μm; arranged into $2 \times 1\mu m$, $2 \times 2\mu m$, $2 \times 3\mu m$, $2 \times 4\mu m$ and $4 \times 3\mu m$ unit cells (where the first number indicates the number of gate fingers within the same cell). Therefore, five different transistors of 24 μm total width were formed with a different number of those cells. Then the f_A was obtained (using the script of [40]) from the corresponding extracted layout views for the different transistor implementations. These results are shown in Figure 4.10 as a function of biasing current. From that figure, it can be seen that the optimum finger width for the G01 transistors is $W_{finger} = 3\mu m$, employing the unit cell of $4 \times 3\mu m$ gate fingers.

4.3.4.3 Final layout implementation

Once the optimum finger width and unit transistor cell was determined, each of the inverter stages in the pre-driver was built employing the same unit CMOS cell with the sizes shown in Table 4.3. Figure 4.11 shows the final layout implementation of the pre-driver macro cell. In

[5]This is the formal procedure that could not be implemented during the design of the EDG01 unit transistor P–cell due to the lack of the EDG01 transistor model at the moment this work was performed.

the same figure, it can be observed the unit CMOS P–cell from which each inverter stage was constructed. Note that also some AC-decoupling capacitance, C_{dec}, was placed inside the macro cell itself, as shown in Figs. 4.11 and 4.9(a). Having AC-decoupling as close as possible to the active circuits is highly desired, however only a very limited (but very useful) quantity of the total decoupling capacitance can be put just right aside of the inverter-chain inside the macro cell. The total amount of decoupling capacitance that could be placed inside the macro cell itself was $C_{well} \approx 2.4pF$.

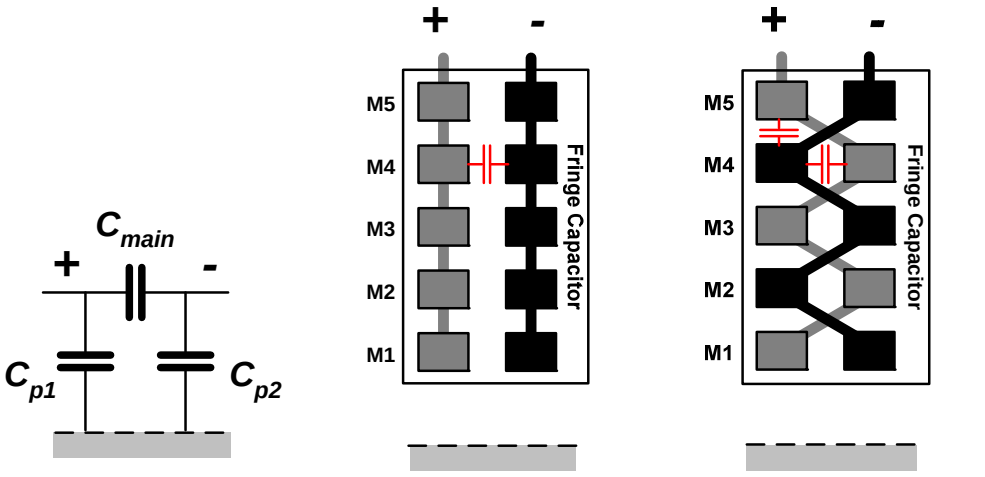
4.3.5 Capacitors design concepts

As seen in the circuit schematic of Fig. 4.4, there are two kinds of capacitors that were integrated into the CMOS driver: AC-coupling and -decoupling capacitors. The requirements of both types of capacitors is slightly different due to the parasitics that come along with any integrated capacitor. This section describes the general design of both types of capacitors and describe some ideas that were implemented and that led to the increase on the quality of those capacitors and to important reductions in the total silicon area of the chip.

4.3.5.1 Fringe Capacitor P–cell design

Despite the larger capacitance densities of MOS capacitors, the interdigitated metal plate or lateral flux capacitor was chosen for this design. This type of capacitor does not depend in biasing levels as the first one, and then it can be used for either AC-coupling or -decoupling. Additionally, MOS capacitors will have a maximum 2.5V limit to avoid breakdown (because of the thick-oxide active devices), so special techniques should be employed to use them within our 5V CMOS driver.

Any integrated capacitor will have losses due to its finite quality factor, but more importantly, it will come with two associated parasitic lateral capacitances, as shown in Fig. 4.12(a). C_{main} is the intended capacitor value and C_{p1}, C_{p2} are the lateral parasitic bottom-plate capacitances at each capacitor terminal. C_{p1}, C_{p2} are a function of the capacitor area, and hence they are proportional to C_{main}. Therefore, it is important to maximize the capacitance density of an integrated capacitor in order to reduce the influence of those parasitic capacitances, which is of high importance for AC-coupling capacitors (especially at the output). Decoupling capacitors also benefit from higher capacitance densities.



(a) Lateral parasitic capacitances

(b) Original fringe capacitor P–cell

(c) Modified fringe capacitor P–cell (20% increase in capacitance density)

FIGURE 4.12: Fringe capacitor (M1 to M5) P–cells: a) very simplified capacitor model (to show only the lateral parasitic capacitances) b) original P–cell, and c) modified P–cell that yield a 20% increase in capacitance density.

In 65-nm CMOS there is a standard fringe capacitor P–cell available. This P–cell consists of minimum size interdigitated metal plates from M1 to M5, as shown in Fig. 4.12(b). Two options to modify this standard P–cell in the search of increased capacitance densities were explored. The first one was to add inter-metal VIAS in each finger to increase the lateral capacitance. However, since the P–cell was built with minimum dimensions, the addition of these VIAS would expand the finger width (due to the technology rules), causing an overall reduction in the capacitance density instead of the desired increase. The second option was to interleave the fingers of the two capacitor terminals as shown in Fig. 4.12(c) [41]. This change does not require a modification of any of the capacitor cell dimensions, and it increases the capacitance density due to the added top-bottom plate capacitance of the interleaved fingers. This change led to an important increase of $\approx 20\%$ in the capacitance density with respect to the standard fringe capacitor cell. A direct consequence of this improvement is that the added capacitance density can be traded-off with lower parasitic lateral capacitances in AC-coupling capacitors. Reducing the area of a constant value capacitor or eliminating some of the bottom-most metal layers will yield lower parasitics. This is particualrly important at the output node (see Fig. 4.4(a)) due to the large capacitor needed and its loading effects (which affects both speed and efficiency of the CMOS driver).

In RF applications, the self resonance and quality factor of the capacitors is important as well.

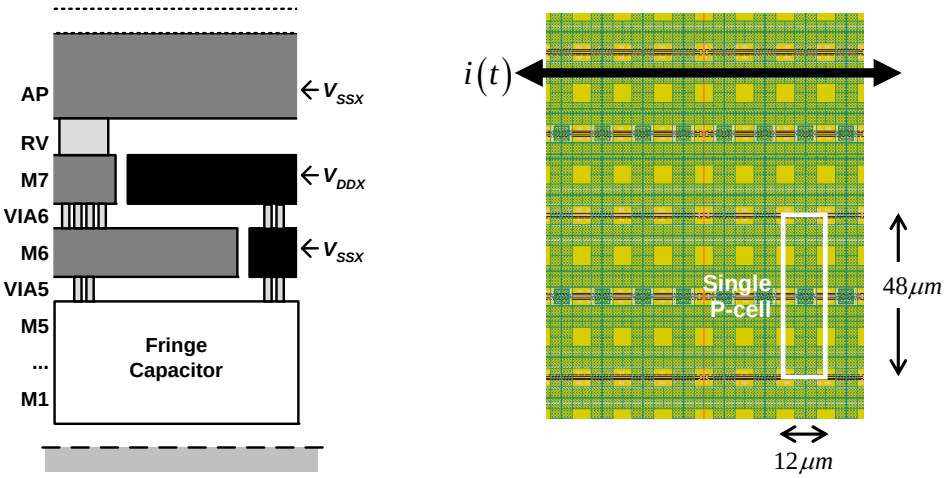
The parasitic inductance and series resistance of the fringe capacitors must be kept at their minimum. For a given capacitor size, the smaller the individual finger length is, the more interconnections will be needed. Smaller finger lengths have lower parasitics. More interconnections means more parasitics. So, there is a trade-off between the individual finger length and the number of interconnections.

4.3.5.2 Power routes with embedded capacitor concept

The CMOS technology employed has seven Copper metal layers (M1 to M7) and an additional Aluminum metal layer (AP) on top. All these layers can be used to create power traces, however M6 and M7 (both are equal) are the most appropriate ones for this purpose since either one can handle as much current as an equivalent stack of M1 to M5 (these layers are equal among themselves). Although the AP layer is $\approx 61\%$ thicker than M6 or M7, its maximum DC current rating is only around 35% of the one for M6 or M7 for the same width. This would make the AP layer of only auxiliar use. The relative thickness size of each metal layer can be observed in Figure 4.13.

An important technology requirement in state-of-the-art CMOS technologies, when building power traces, is the maximum metal density that is allowed. This maximum metal density must be met at different area sizes, starting at around $20\mu m \times 20\mu m$, for levels of about 70-80%. Since the power traces implemented in the CMOS driver can be up to more than $150\mu m$ width, a P–cell approach was also employed in building these power traces. A generic metal square of $12\mu m \times 12\mu m$ with square holes at its four corners implemented this P–cell. Those holes control the metal density in the power traces. When several of the unit P–cell blocks are placed next to each other, the resulting power trace will contain uniformely distributed 'holes' that reduces the total metal density to the values required. This simple but powerfull technique was employed for all the power traces within the CMOS driver.

As observed in the schematic of Fig. 4.4(b), all the AC-decoupling capacitors were connected at high-current power traces, i.e. the ones for the voltage supply sets. These power lines were routed in the top-most metal layers, M6 and M7 (and AP as an auxiliary trace). Then, the improved fringe capacitor P–cell discussed in the last section was integrated along with those internal power traces. This led to a new P–cell, whose cross section view can be seen in Figure 4.13(a). From the figure it can be observed that M6-AP was dedicated for the V_{SSx} power traces and M7 for the V_{DDx} ones. Observe also that the sandwich-type of structure will slightly

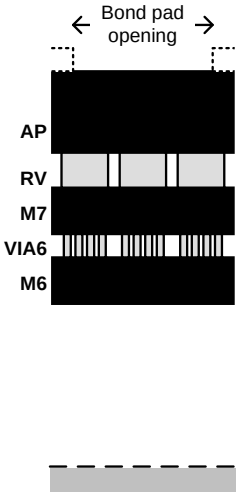


(a) Cross section view (b) Layout top view

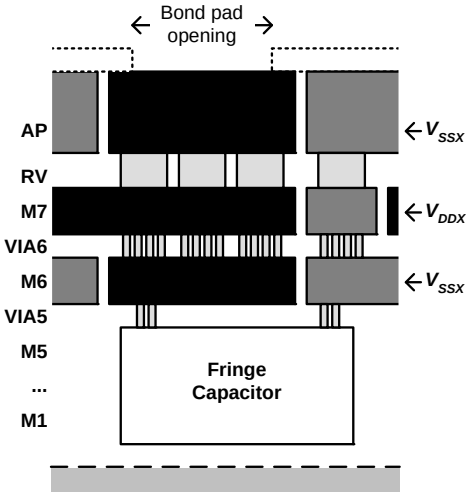
FIGURE 4.13: *Power traces with embedded capacitor* concept: a) cross section view, and b) example layout top view, showing the detail of a single unit P–cell.

increase the capacitive density of the resulting P–cell. The limitation for the quality factor of this new special capacitor P–cell concept is the number of VIAS between the fringe capacitor cell and the power traces on top. This is due to the very low ohmic power traces on M6-AP and M7 and the reduced finger length in the fringe capacitor P–cell, converting those VIAS in the bottle neck for the capacitor quality factor.

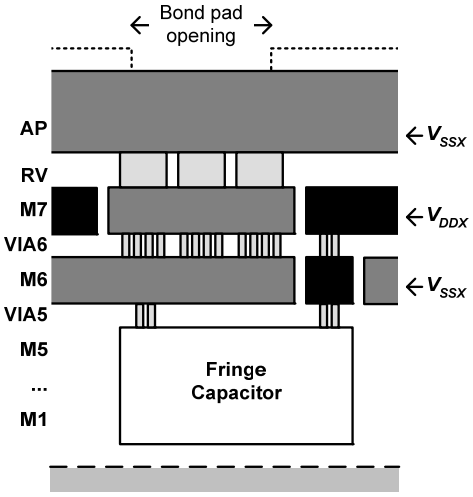
This innovative capacitor structure reached densities in the order of $\approx 1.6pF/\mu m^2$, a quality factor of > 150 and lateral parasitic capacitances of less than $\approx 3\%C_{main}$. All these values were obtained through extracted layout view simulations of a sample structure of $\approx 200\mu m \times 300\mu m$, implementing $\approx 110pF$. Additionally, this new P–cell has an important feature. Due to its construction (Fig. 4.13(a)), many of these new capacitor P–cells can be placed next to each other in both the X- and Y-direction without inter-spacing and the capacitor terminals are automatically connected. This means that scalable capacitors can be realized with this P–cell, preserving the capacitance density and frequency performance of the entire structure. Figure 4.13(b) shows the layout top view of a (section of a) capacitor implemented using this new P–cell. If the AP layer is used, then the current can only flow in one orthogonal direction within the top metals of the capacitor, either in the X- or in the Y-direction (depending on the capacitor placement), as shown in Fig. 4.13(b). This is due to the holes in the M7 layer required to allow RV vias go through it without electrical contact, as shown in Fig. 4.13(a). If the AP layer is not used, then the current can flow freely in both X- and Y-direction (since not RV vias and their holes



(a) Simple bondpad



(b) Special V_{DDx} bondpad



(c) Special V_{SSx} bondpad

FIGURE 4.14: Cross section views of different bondpads: a) simple bondpad, b) V_{DDx} bondpad with embedded capacitor, and c) V_{SSx} bondpad with embedded capacitor.

in M7 will be needed). Ths special capacitor P–cell implemented the highest density capacitors employed in the CMOS driver.

4.3.5.3 Bondpad with embedded capacitor concept

A similar concept as the one presented in the last section was developed for an indispensable but high area consuming block: the bondpad. Figure 4.14(a) shows a cross section of a classical bondpad, implemented by stacking the top metal layers, M6 to AP, for mechanical stress requirements during bond-wiring. Figures 4.14(b) and 4.14(c) shows the cross section view of the *Bondpad with embedded capacitor concept* for the bondpads of V_{DDx} and V_{SSx}, respectively. As

it will be seen soon, in an overall top view of the complete CMOS driver chip, many bondpads were used to reduce the inductance of the bondwires. All the bondpads consume a significant portion of the total area of the CMOS driver, and most of them are supply bondpads. Therefore, by combining the improved fringe capacitor P–cell with the traditional bondpad, a new structure providing both functions was obtained and a lot of silicon area was saved in the driver chip.

As stated before, M6-AP was reserved for the V_{SSx} power traces while M7 for the V_{DDx} ones. Therefore, two different bondpads structures were needed as shown in Figs. 4.14(b) and 4.14(c). Observe how the interconnections between each of the top metal layers and the bondpads are realized, making it possible to create bondpad P–cells that automatically provide the correct connections once placed anywhere in the chip. The density and quality of the capacitors under each bondpad was slightly inferior to the one of last section, due to the need of placing internal traces made of M1 to M5 underneath the bondpad itself. This special bondpad with embedded capacitor P–cell occupies $108\mu m \times 108\mu m$ and has a $80\mu m \times 80\mu m$ bondpad opening. Each bondpad provides $\approx 9.7pF$ of capacitance, employing metal layers from M1 to AP (as seen in Figs. 4.14(b) and 4.14(c)).

4.3.5.4 AC-coupling capacitors

For the AC-coupling capacitors (at the input and at the output of the CMOS driver), other special measures were additionally taken to reduce the negative influence of the parasitic lateral capacitances. The first one was to limit the use of the bottom-most metal layers (i.e. the closest to the substrate) to reduce the parasitic capacitances at the expense of a reduced capacitance density. The other measure was to precisely control the required dummy metal filling process in the AC-coupling capacitors. Both measures were employed for the creation of the input and output AC-coupling capacitors that were integrated in the CMOS driver.

For the first measure, some conclusions were obtained from extracted layout view simulations of several identical fringe capacitors build from M1, M2, M3 to M5. Each metal layer within the fringe capacitor P–cell contributes to approximately 20% of the total fringe capacitance. However, the lateral parasitic capacitances will be approximately 3.4% and 2.8% for the M1–M5 and M2–M5 fringe capacitors, respectively. The parasitics of the M3–M5 capacitor are very similar to the ones for the M2–M5 capacitor. From these results, it can be observed that taking out only M1 from the fringe capacitor P–cell will produce a capacitor of 20% lower density with *another* $\approx 18\%$ reduction of the lateral parasitic capacitances. If M2 is also taken out from the

Capacitor reference	C_{in} (each)	C_{out}
$C_{total} \approx$ [pF]	16	49
$C_{p1} \approx C_{p2} \approx$ [pF]	0.4	1.2
Metal layers	M2-AP	M3-AP

TABLE 4.4: Summary of all the AC-coupling capacitors in the CMOS driver I. See the schematic of Fig. 4.4(a) for each capacitor reference.

Capacitor reference	C0	C1	C2	C3
$C_{total} \approx$ [pF]	97	96	437	104
Metal layers	M1-AP	M1-AP	M1-AP	M1-AP

TABLE 4.5: Summary of all the AC-decoupling capacitors in the CMOS driver I. See the schematic of Fig. 4.4(b) for each capacitor reference.

fringe capacitor, then its density will also reduce but the parasitic capacitances will not improve. It was concluded that M1 had the greatest influence in the lateral parasitics while M2 had not. Therefore, M1 was not used for the AC-coupling capacitors.

To reduce further the parasitics in the AC-coupling capacitors, the metal dummy filling process was precisely controlled. This dummy filling process is required by the CMOS technology to comply with minimum metal density rules (in the order of 10%). This process is normally carried out with the aid of automated scripts during the chip finishing phase. Previously, it was concluded that not employing M1 in the (large area) AC-coupling capacitors was advantageous (to avoid loading of sensitive nodes). Not employing M1 will cause minimum metal density issues. The dummy filling automated script would solve these issues but will eliminate the advantage of not using M1, because of the uniformly distributed and high density metal pieces that are placed by the script. A solution to this problem was to place special 'stop metal' layers in the form of strips that limited the access of the automated script to certain areas to be filled in, controlling the metal density at its minimum in order to get minimum parasitics in the final produced chip.

4.3.5.5 Implemented capacitors summary

All the ideas described in this section were employed in the layout of the AC-decoupling and -coupling capacitors. A summary of the values of each implemented capacitor of the schematic shown in Fig. 4.4(b), is presented in Tables 4.4 and 4.5.

4.3.6 ESD protection design

Electrostatic Discharge (ESD) is a charge balancing process between two objects at different potential. It can occur during manufacturing, shipping, assembly, and field handling of ICs or circuit boards. There are two ways to reduce IC failures due to ESD events: by proper handling of the ICs during all the above mentioned situations and by implementing on-chip protection circuits to increase the ESD robustness of the ICs. On-chip ESD protection should provide a current path between any two pins of an integrated circuit. There must be a low-ohmic ESD current path between every pair of those pins, designed to carry high AC currents for both possible polarities of a discharging event (i_{ESD}) [42].

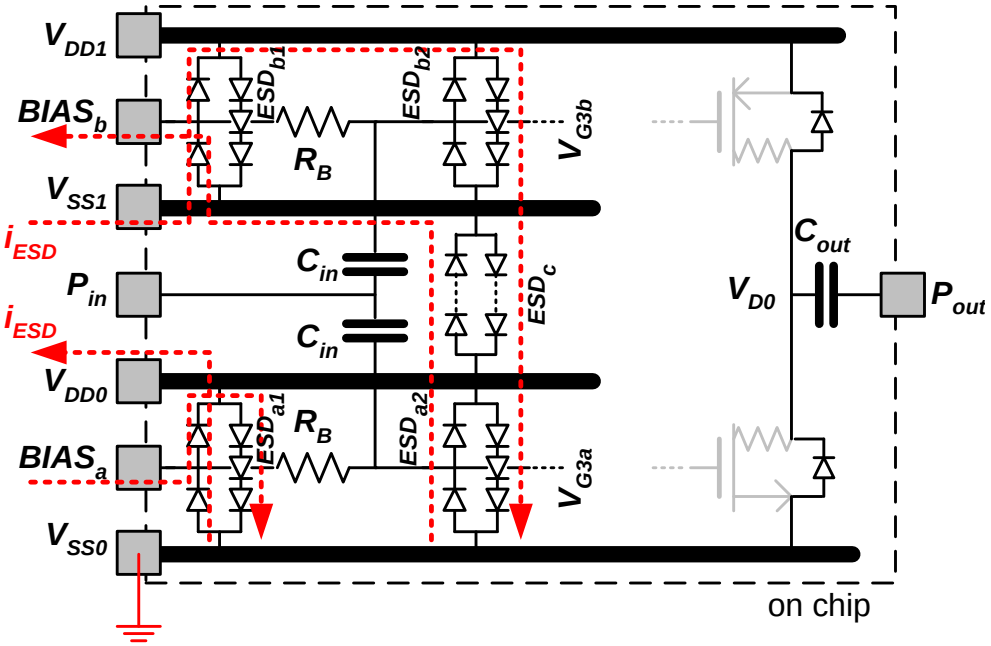
Due to the highly experimental nature of the CMOS driver ICs designed for this thesis, proper handling during PCB assembly should be observed since a mass-production ESD robustness was not pursued in these designs. However, due to the use of a couple of supply sets, a dedicated rail-based ESD protection scheme was proposed to protect the chip.

4.3.6.1 ESD protection strategy

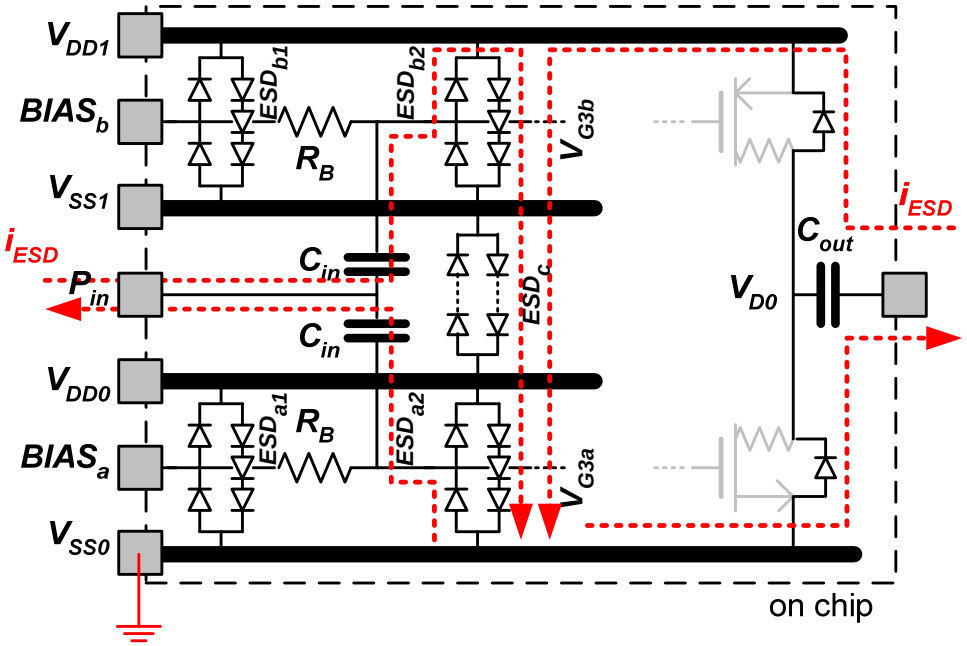
All the pins of the CMOS driver are either explicitly or implicitly protected against ESD events. The explicit ESD protection circuitry is realized by the diodes showed in the schematic of Fig. 4.4(b). The implemented ESD circuitry establishes low-ohmic current paths in case of ESD events at any pin with respect to the overall ground pin, V_{SS0}. Some of these ESD current paths are shown in Figure 4.15.

Observe from the explicit ESD circuitry in Fig. 4.15 that there are two kind of protective circuit blocks: $ESD_{a1,a2} = ESD_{b1,b2}$ and ESD_c. The diodes of $ESD_{ax,bx}$ implement a standard ESD protection for an input signal node and its associated local supply. However, due to the existence of two sets of local supply voltages, V_{SS0}–V_{DD0} and V_{SS1}–V_{DD1}, the anti-parallel diodes of ESD_c are used to connect all the power supply lines in case of any ESD event. From Eq. (4.2d), $V_{SS1} - V_{DD0} \leq V_{ESD,rev,max}$, it can be observed that for proper operation, the number of series diodes in ESD_c is selected according to the maximum expected offset difference between the two supply sets and the V_{th} of each (transistor) diode.

The V_{DDx}, V_{SSx} and $BIAS_x$ pins are protected by means of ESD_{a1}, ESD_{b1}, and ESD_c. Some of the current paths in case of ESD events involving those pins are shown in Fig. 4.15(a). In case



(a) ESD (some) current paths at V_{DDx}, V_{SSx} and $BIAS_x$ pins



(b) ESD current paths at P_{in} and P_{out} pins

FIGURE 4.15: Schematic of the ESD circuitry, showing the ESD current paths: a) (some) at V_{DDx}, V_{SSx} and $BIAS_x$ pins, and b) at P_{in} and P_{out} pins.

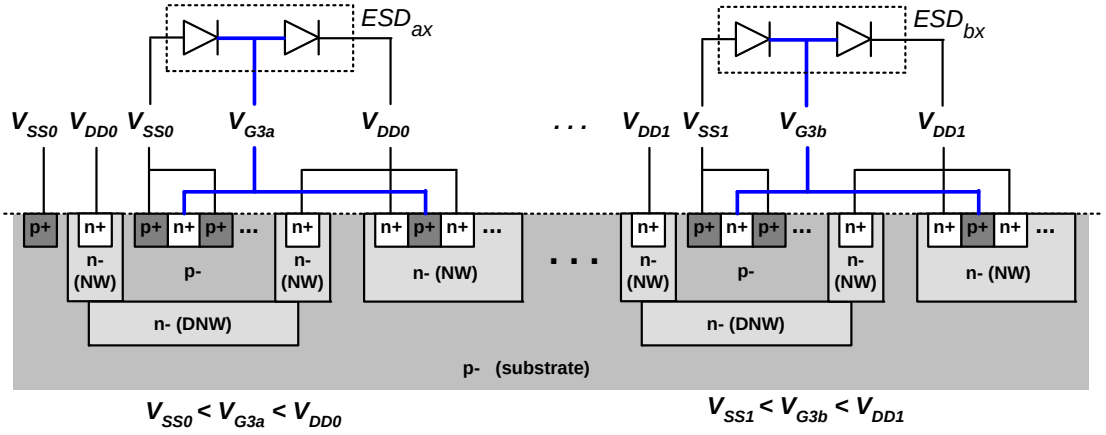


FIGURE 4.16: Cross section view for the ESD protection circuits involving the signal paths.

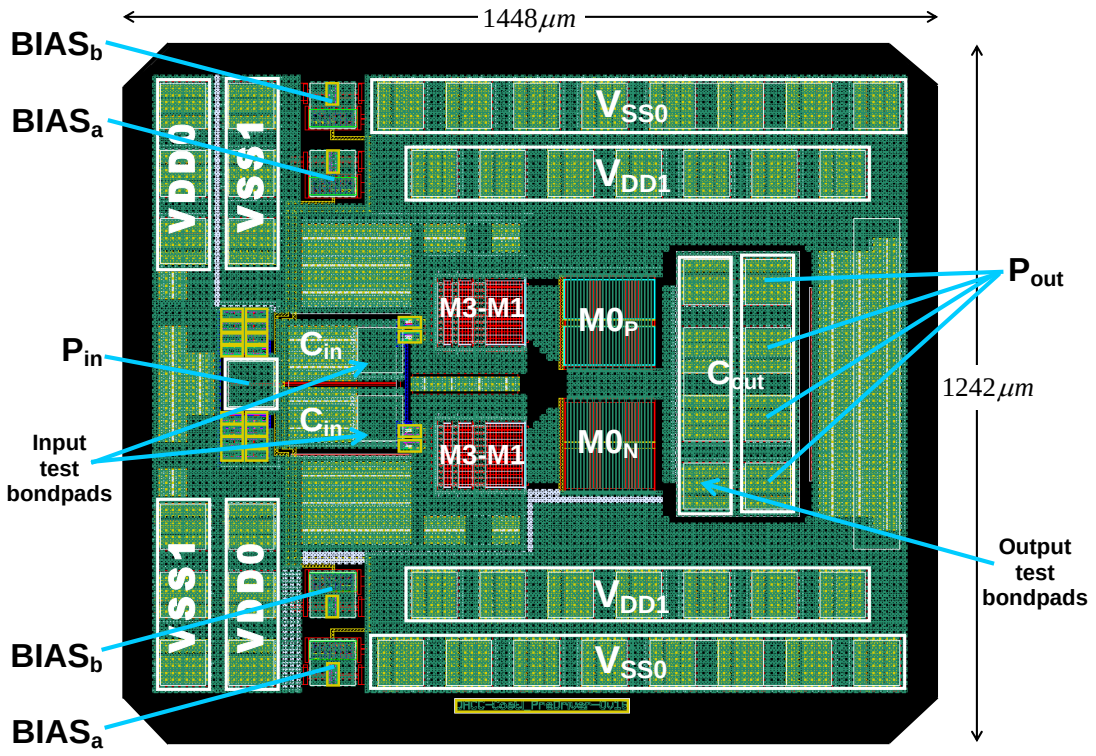
of an ESD event at the input and output pins, the AC-coupling capacitors, C_{in} and C_{out}, could be seen as AC shorts by the ESD currents so the internal nodes V_{G3x} and V_{D0} would be reached, respectively. In this case, the P_{in} and P_{out} pins are protected by means of ESD_{a2}, ESD_{b2}, and ESD_c. ESD_{a1} and ESD_{b1} can not be used to protect these last pins due to the presence of the not low-ohmic biasing resistor R_B. In the case of the output pin, there is an implicit ESD protection by the parasitic drain–source diodes of the EDG01 devices. Fig. 4.15(b) shows the ESD current paths in case of ESD events at the input and output pins.

4.3.6.2 Use of Deep N-Well

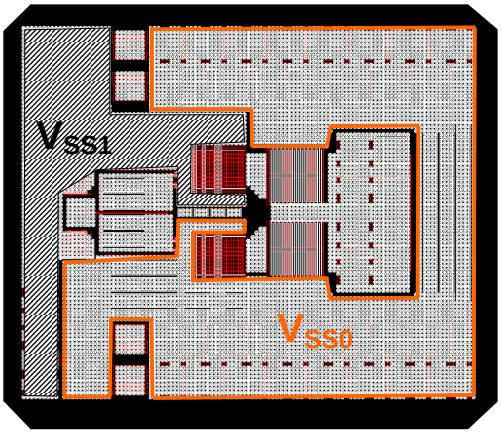
In order to reduce the loading of the ESD structures in the signal path, a Deep N–Well is used in the ESD diodes involving the signal path, i.e. $ESD_{ax,bx}$. Figure 4.16 shows a cross section view of such ESD diodes. The rest of the diodes are placed inside simple N–Wells.

4.3.7 Complete layout of the CMOS driver I

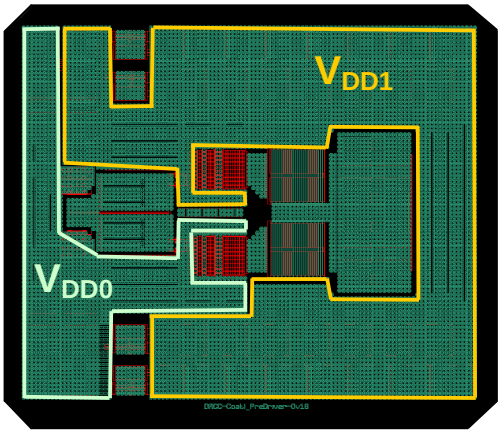
Finally, the complete EDG01-based CMOS driver I layout is depicted in Figure 4.17(a). The chip pin-out and all the blocks that have been described previously can be seen in the figure. Observe that the active circuits (i.e. the pre-drivers and the output stages) occupy only a limited area with respect to the whole chip. The large number of bondpads consumes most of the chip area. If the decoupling capacitance were not embedded within the bondpads, then it would also consume an important silicon area.



(a) CMOS driver I chip layout top view and pin-out



(b) CMOS driver I chip power traces at M6



(c) CMOS driver I chip power traces at M7

FIGURE 4.17: Complete CMOS driver I chip layout: a) top view and pin-out, b) power traces at M6, and c) power traces at M7

The redundancy of the biasing pins and the symmetry with respect to the X-axis, coming from the out-phasing layout requirement, can be observed in the top layout picture of Fig. 4.17(a). Also, the redundancy in the supply pin-out was required to acess V_{SS0} and V_{DD1} by the top and bottom side interchangeably when placing two of these chips in a single out-phasing power module.

In Figs. 4.17(b) and 4.17(c) the detail of the internal power traces at M6 and M7 can be observed. Notice that most of the chip area in the M6/M7 metal layer is dedicated at the four power supply lines in order to provide wide and low-ohmic power traces. This power trace strategy enabled the required pin redundancy of the chip.

Additionally, there are internal bondpads (not explicitly indicated in Fig. 4.17(a)) at the nodes V_{G3a}, V_{G3b}, and V_{D0} (see the schematic in Fig. 4.4(a)) that provide some testability of the chip at the PCB assembly level[6].

As stated before, all the simulation results from the designed CMOS driver chip will be presented in the next chapter.

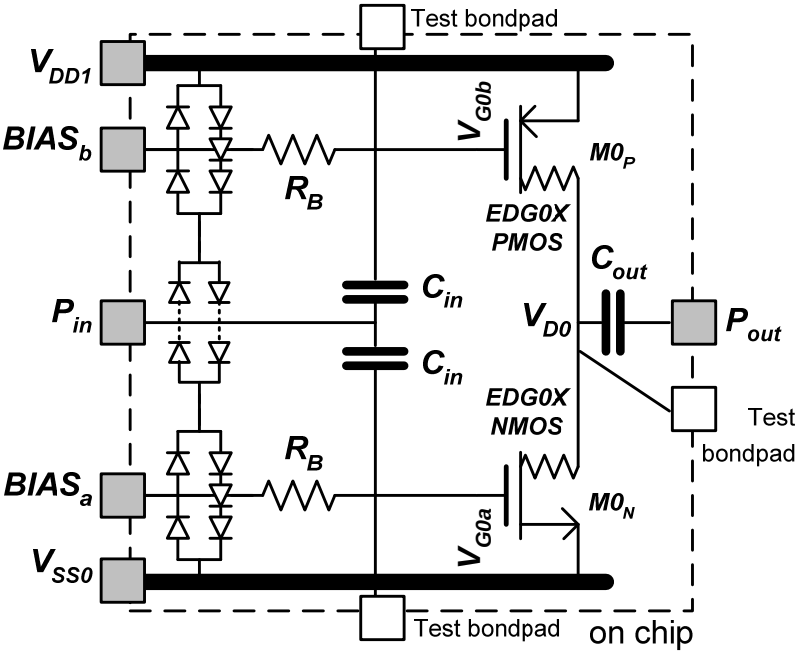
4.4 CMOS drivers II and III

Other two CMOS driver chips were also fabricated, as indicated earlier. Their design was completely based in the design of the first CMOS driver (CMOS driver I) described in the former sections. The pre-driver macro cells were removed in both CMOS drivers II and III. The goal was to investigate the performance of the drivers without the top and bottom inverter chains.

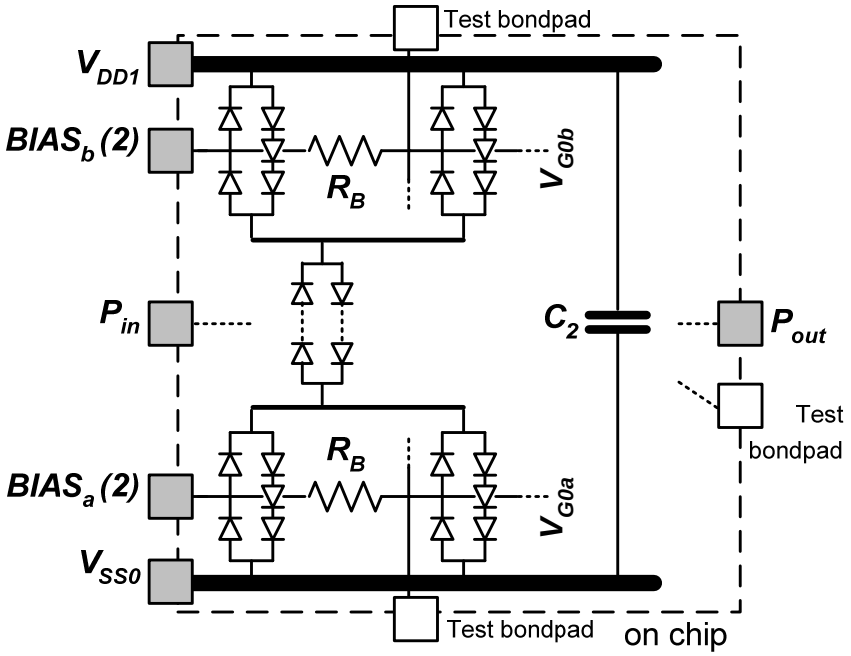
The CMOS driver II employs exactly the same devices as the CMOS driver I, while the CMOS driver III has EDG02 devices instead. In the three CMOS drivers, the ED devices have all the same total width ($4032\mu m$) and finger length ($3\mu m$)[7]. Since these two new chips do not have pre-drivers, the input AC-coupling capacitances were increased.

Figure 4.18 shows the schematic of the CMOS driver II and III. The only difference is the output device type: EDG01 and EDG02 devices for the CMOS driver II and III, respectively. Fig. 4.18(a) shows the functional schematic, while Fig. 4.18(b) shows the details for the ESD

[6]Due to the complexity of the CMOS driver chip, it cannot be easily tested directly on-wafer.
[7]Unit transistor P–cells for the EDG02 devices were created based on the original P–cells for the EDG01 devices.



(a) Main functional schematic (CMOS drivers II and III)



(b) ESD and decoupling capacitors schematic details (CMOS drivers II and III)

FIGURE 4.18: Top schematic view of the implemented CMOS drivers II and III: a) main functional schematic (the only difference is the output device type: EDG01 and EDG02 devices for the CMOS driver II and III, respectively), and b) ESD and decoupling capacitors schematic details.

Capacitor reference	C2	C_{in} (each)	C_{out}
$C_{total} \approx$ [pF]	560	36.9	49
$C_{p1} \approx C_{p2} \approx$ [pF]	-	0.7	1.2
Metal layers	M1-AP	M2-AP	M3-AP

TABLE 4.6: Summary of all the AC-decoupling and -coupling capacitors in the CMOS drivers II and III. See the schematics of Fig. 4.18 for each capacitor reference.

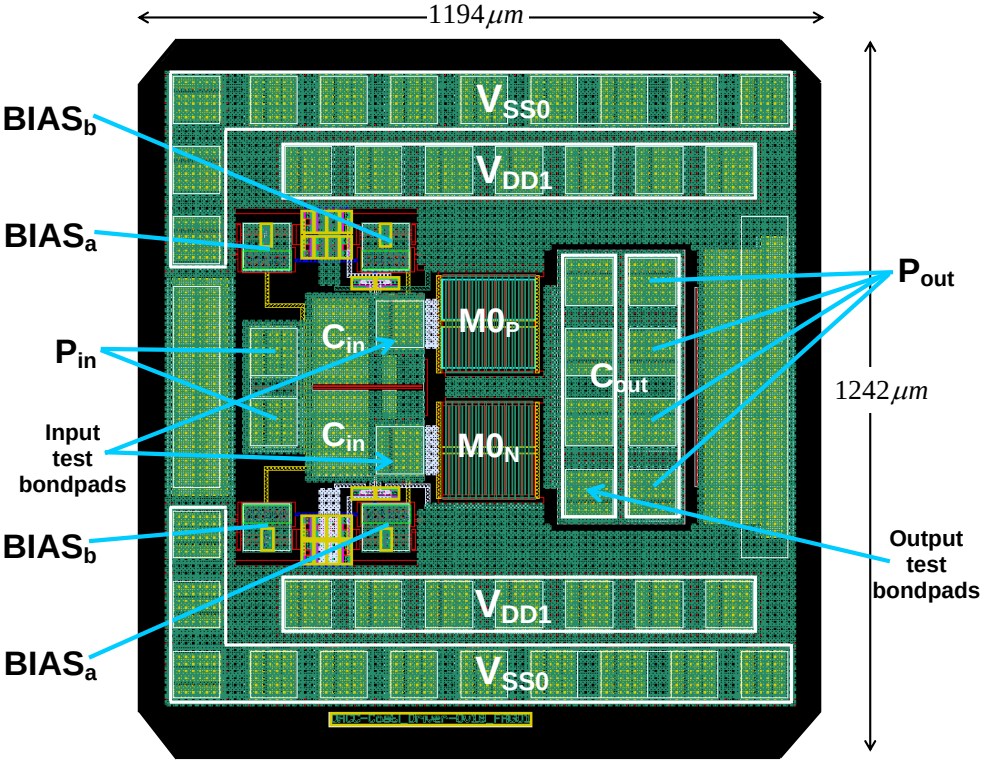


FIGURE 4.19: Layout top view and pin-out for the CMOS driver II and III chips (the only difference is the output device type: EDG01 and EDG02 devices for the CMOS driver II and III, respectively).

protection circuitry and the AC-decoupling capacitor. Table 4.6 summarizes the AC-decoupling and -coupling capacitors values for the CMOS driver II and III.

The common layout and pin-out of the CMOS driver II and III can be seen in Figure 4.19. Note that the X-size of these two chips is smaller than the one of the CMOS driver I, there are more bondpads for V_{SS0} and there are two bondpads for the input signal (both are shorted internally).

Chapter 5

Inverter-based CMOS drivers simulation results

5.1 Introduction

This chapter presents the main simulation results for the three CMOS drivers described in Chapter 4, with an emphasis in the CMOS driver I. All the simulations in this chapter are performed with the extracted layout view of the CMOS drivers.

The first section of this chapter deals with all the simulation results of the CMOS driver I. The following section presents the most important results from the simulations of CMOS driver II and III. The third section makes an overview and comparison of the results for the three drivers. Finally, the last section provides the conclusions about the inverter-based approach for HV swings.

5.2 Performance of CMOS driver I

5.2.1 Performance with ideal capacitive load

This section presents the simulation results of the CMOS driver I employing an ideal capacitive load. The objective is to understand the performance of the chip without the influence of non-linearities of a real transistor load and without the influence of bondwires. These effects will be considered later in this chapter.

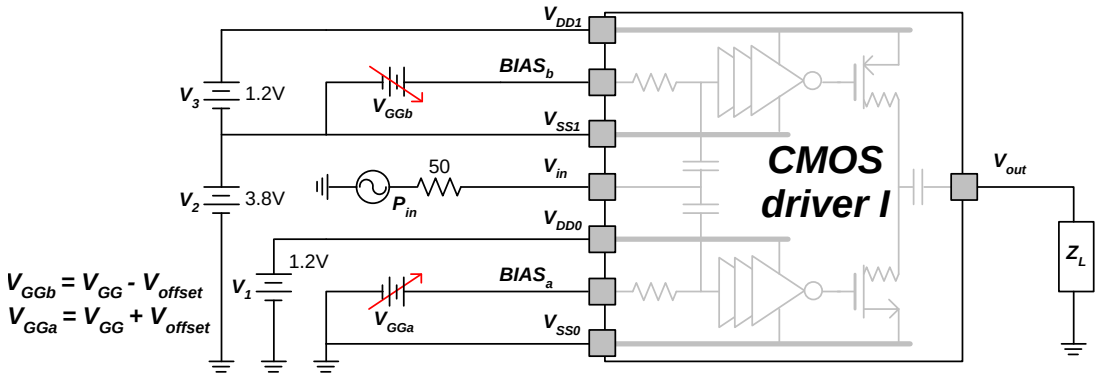


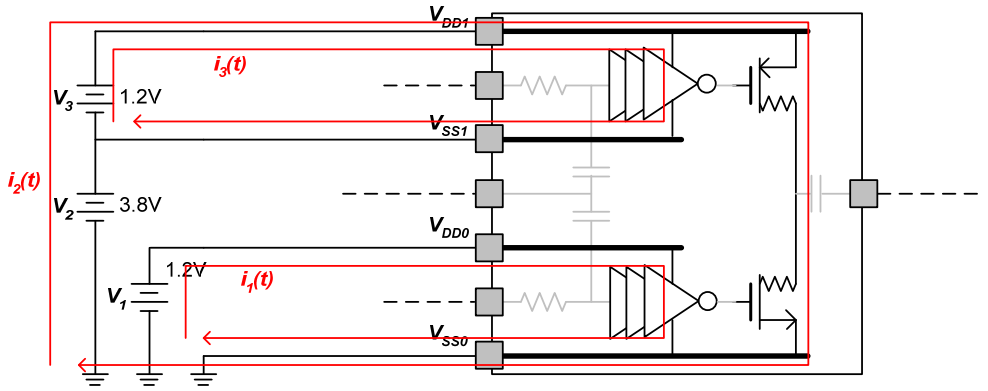
FIGURE 5.1: Simulation setup for the CMOS driver I chip.

5.2.1.1 Simulation setup

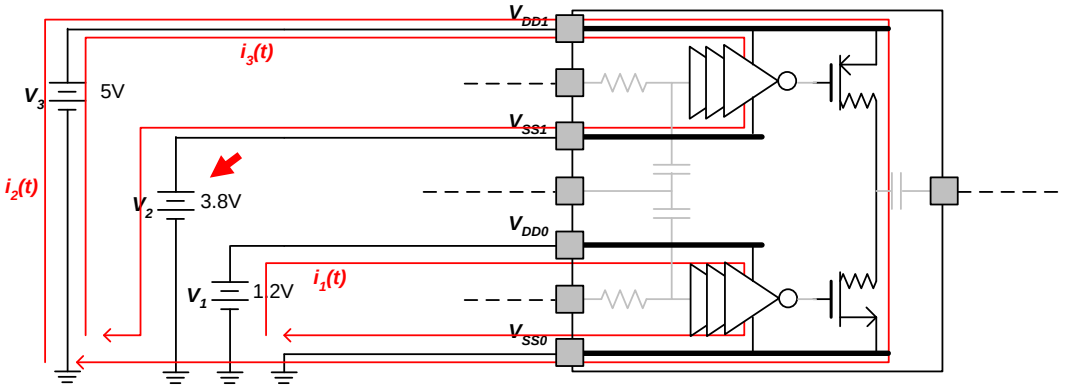
The simulation setup employed in this section is depicted in Figure 5.1. The output stage ED transistors have been simulated using the model developed in Appendix A[1]. The load is a 5pF capacitor. All the supply voltages are provided by the voltage sources V_1, V_2, and V_3. Different arrangements for the voltage supplies are possible in practice (e.g. in a real hardware measurement setup), however the one shown in Fig. 5.1 provides a direct reading of the total DC power consumed by the driver. For simplicity, each biasing voltage has been referred to its local V_{SSx}. V_{GG} represents the biasing level for each biasing input; this is $BIAS_a = V_{SS0} + V_{GGa}$ and $BIAS_b = V_{SS1} + V_{GGb}$, where $V_{GGa} = V_{GG} + V_{offset}$ and $V_{GGb} = V_{GG} - V_{offset}$. Unless otherwise stated, $V_{offset} = 0$. Increasing V_{GG} will increase the duty-cycle D of the output signal, as it will be seen shortly.

Care must be taken when computing the total DC power dissipated by the driver, $P_{DC,driver}$, as exemplified in Figure 5.2. Fig. 5.2(a) shows the simulation setup employed here and a representation of the DC supply currents associated to each main block of the CMOS driver I. $i_1(t)$ and $i_3(t)$ are the supply currents for the pre-driver stages. $i_2(t)$ represents the current required for the output stage. It can be observed from Fig. 5.2(a) that V_1 provides the power to the bottom inverter chain, V_3 provides the power for the top inverter chain and a fraction of the power for the output stage, while V_2 provides the rest of the power for the output stage. Therefore, that setup provides a direct reading for the total DC power of the driver as $P_{DC,driver} = P_{DC_1} + P_{DC_2} + P_{DC_3}$. Fig. 5.2(b) shows a different arrangement for the voltage supplies. Observe in this case that the current $i_3(t)$ circulates for both V_3 and V_2. V_2 in this case does not provide power but 'absorbs' it, and V_3 is the one that supplies that power. Hence, the correct computation in this specific

[1] Additionally, the main extracted layout view parasitics has been added to that model (R_G, C_{GS}, C_{GD}, and C_{DS}).



(a) In this setup: $P_{DC,driver} = P_{DC_1} + P_{DC_2} + P_{DC_3}$



(b) In this setup: $P_{DC,driver} = P_{DC_1} - P_{DC_2} + P_{DC_3}$

FIGURE 5.2: Two possible arrangements for the voltage supplies in the simulation setup for the CMOS driver: a) setup that provides a direct reading of the total $P_{DC,driver} = P_{DC_1} + P_{DC_2} + P_{DC_3}$, and b) setup that requires care when computing the total $P_{DC,driver} = P_{DC_1} - P_{DC_2} + P_{DC_3}$ (note the subtraction of P_{DC_2}).

setup must correct for the 'absorbed' power of V_2; this is, $P_{DC,driver} = P_{DC_1} - P_{DC_2} + P_{DC_3}$ (note the subtraction of P_{DC_2}).

5.2.1.2 High-voltage operation and PSS voltage waveforms

In Figure 5.3, the main PSS voltage waveforms at 2.4GHz can be observed, as expected from the ideal waveforms showed previously in Fig. 4.1(e), in section 4.2.1 of Chapter 4. The sinusoidal signals V_{G3a} and V_{G3b} are the input waveforms at each inverter chain, derived from the RF input signal by the AC-coupling input capacitors and the biasing circuitry. V_{G0a} and V_{G0b} are the output signals of the inverter chains, which drive the EDG01 transistors. V_{D0} is the signal at the common drain node of the EDG01 transistors, before the output AC-coupling capacitor C_{out}. V_{out} is the output signal, after C_{out}. The reduced swing of V_{out} with respect to V_{D0} is due to the capacitive voltage division between C_{out} (49pF) and C_L (5pF, in this case).

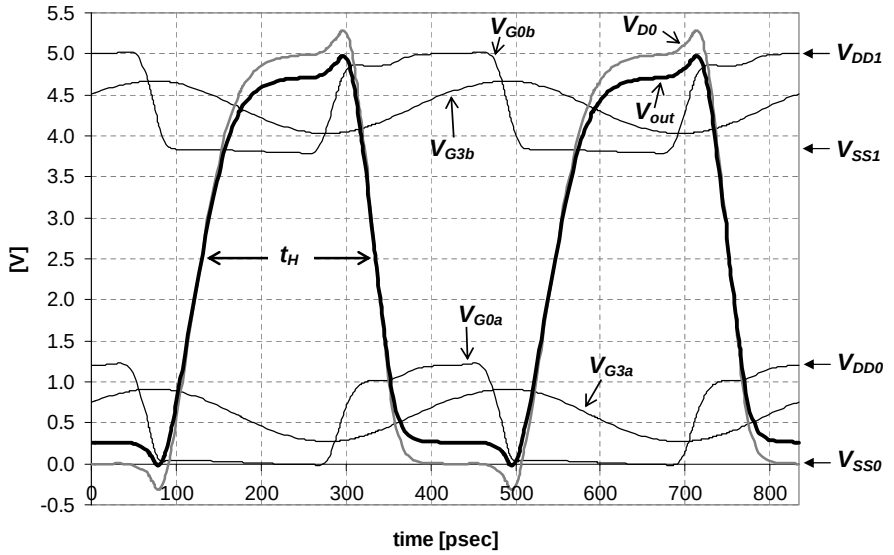


FIGURE 5.3: PSS voltage waveforms for the CMOS driver I at f_0 = 2.4GHz @ P_{in} = 7dBm, V_{GG} = 0.6V, C_L = 5pF.

The duty-cycle is defined as $D = \frac{t_H}{T}$ where t_H is the ON-time shown in Fig. 5.3, and $T = \frac{1}{f_0}$ is the time period. t_H is the time difference between the rising and falling edges at their middle-amplitude level point.

All the voltage swings, except the output, are limited to 1.2V due to the use of the two voltage supply sets (V_{SSx},V_{DDx}). The output swing is determined by $V_{DD1} - V_{SS0}$ which is set externally according to the oxide breakdown voltage capabilities at the gate–drain of the EDG01 devices[2]. Hence, the reliability of the entire CMOS driver is ensured.

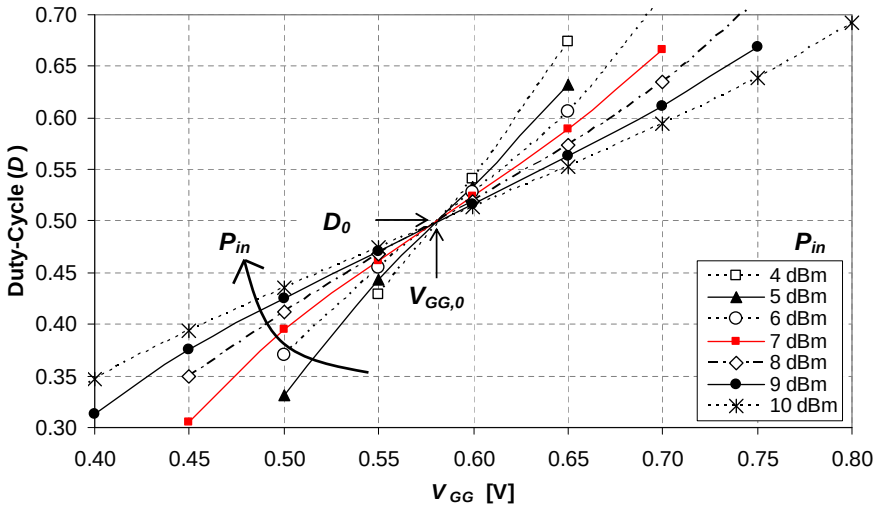
The PSS voltage waveforms in Fig. 5.3 demonstrates the feasibility of reaching the targeted HV output swing by employing the proposed CMOS driver topology.

5.2.1.3 Duty-cycle sensitivity

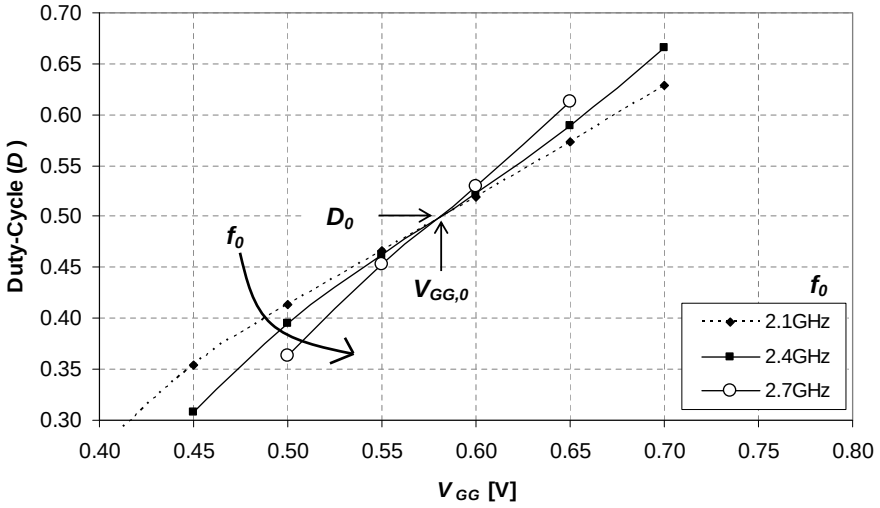
The duty-cycle D controllability of the CMOS driver was possible due to the use of the PWMVGB technique, introduced in section 4.3.1.2 in Chapter 4. For a given load, the duty-cycle is a function of the biasing level at the input of the inverters chain, the frequency, and the input power. This is,

$$D = f\,(V_{GG}, f_0, P_{in}) \tag{5.1}$$

[2]This limit is still to be determined experimentally at the time of writing this document, but it is expected to be at least of 5V.



(a) $D = f(V_{GG}, P_{in})\,|_{f_0=2.4\text{GHz}}$



(b) $D = f(V_{GG}, f_0)\,|_{P_{in}=7\text{dBm}}$

FIGURE 5.4: Duty-cycle as a function of biasing level V_{GG} and a) P_{in} at f_0 = 2.4GHz, and b) f_0 at P_{in} = 7dBm for the CMOS driver I with C_L = 5pF.

Figure 5.4(a) shows the duty-cycle as a function of the biasing level V_{GG} for several input driving powers at 2.4GHz. In this figure, the influence of P_{in} in the duty-cycle can be observed. The larger the input driving power, the lower the duty-cycle sensitivity to V_{GG} (i.e. smaller slope in the lines of Fig. 5.4(a)). If P_{in} is too big, then $D \rightarrow 0.5$ and it will not be controlled. Larger P_{in} means larger voltage swings at the gates of the first transistors, and above a certain level this compromises the reliability of the input transistors. If P_{in} is too small, then the input inverters will not be properly activated. Then, there is a range of input power levels that ensure a correct operation of the CMOS driver. P_{in} = 7dBm has been selected as a trade-off between lower driving power, duty-cycle sensitivity and gate-oxide reliability.

Figure 5.4(b) shows the duty-cycle as a function of the biasing level V_{GG} for the intended frequency bandwidth with P_{in} = 7dBm. The influence of f_0 in the duty-cycle is due to the frequency dependent impedances looking into the first transistor of the inverter chains. As the frequency increases, such impedances will reduce (the source impedance is assumed to be frequency independent) and hence the voltage swing will reduce for a given input power. Then, smaller changes in V_{GG} will cause larger duty-cycle changes, as shown in Fig. 5.4(b). In other words, the sensitivity of the duty-cycle will increase with frequency.

From the PWMVGB technique it can be noticed that the duty-cycle will be approximately linear with respect to the biasing level V_{GG} closer to its 50%. It will become less linear as the top and bottom valleys of the sinusoidal input voltage waveform approach the switching threshold level of the inverter chains. From Figs. 5.4(a) and 5.4(b) it can observed that the duty-cycle can be fairly considered linear with respect to V_{GG} within a useful duty-cycle range of about 30 to 70%. Also, observe that there is common 'pivot' point in the duty-cycle lines $(V_{GG,0}, D_0)$ at $D = 0.5$. Therefore, the duty-cycle can be modeled as

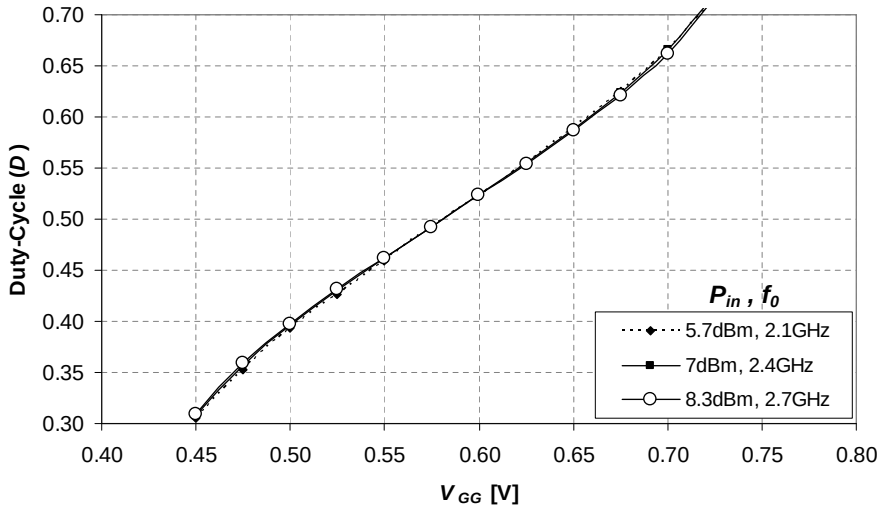
$$D\left(V_{GG}, f_0, P_{in}\right) \approx m_D \cdot \left(V_{GG} - V_{GG,0}\right) + D_0 \tag{5.2}$$

where

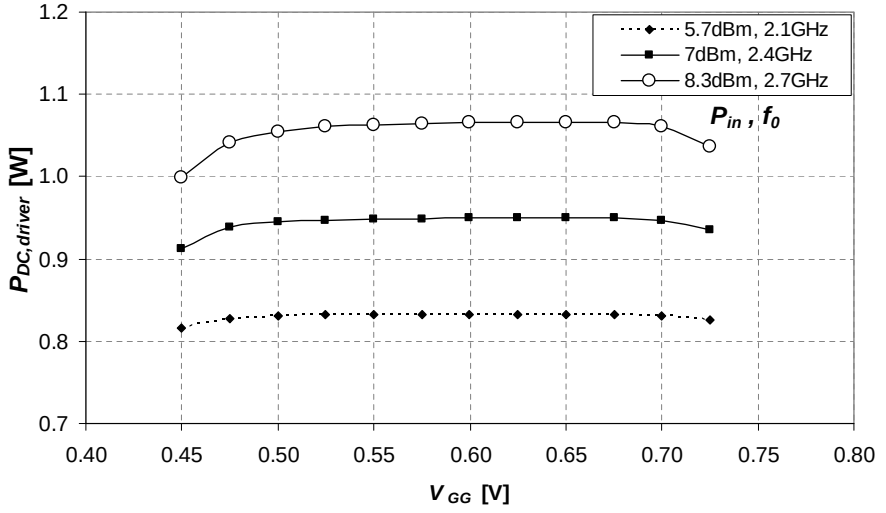
$$m_D = f\left(f_0, P_{in}\right) \propto f_0, \frac{1}{P_{in}} \tag{5.3}$$

Observe that $D = 0.5$ does not happen at the middle of the V_{GG} range. This is expected due to the asymmetric voltage transfer curve of the inverters, which in turn is due to the unitary width ratio of the PMOS and NMOS transistors. Although the switching threshold level V_M (see Fig. 4.3 in section 4.3.1.2) of the inverters is relatively insensitive to the device ratio, reducing the width of the PMOS moves V_M towards V_{SSx} [36].

From eq.(5.3), it can be noticed that m_D could be maintained constant within a given bandwidth with a proper P_{in} adjustment at each frequency of interest, i.e. by making the required $P_{in} = f\left(f_0\right)$.



(a) $D = f(V_{GG})$



(b) $P_{DC,driver}$

FIGURE 5.5: Simulation results keeping m_D constant for the entire operating bandwidth for the CMOS driver I with C_L = 5pF: a) $D = f(V_{GG})$, and b) $P_{DC,driver}$.

5.2.1.4 Duty-cycle results

Figure 5.5 shows the results of keeping m_D constant in the entire bandwidth, represented by the three frequencies in the figure. The corresponding input driving power is 5.7, 7.0 and 8.3 dBm at 2.1, 2.4 and 2.7 GHz respectively. Therefore, Fig. 5.5(a) shows that the duty-cycle has become a (almost) linear function of V_{GG} only. From Fig. 5.5(a), it can be observed that the CMOS driver I reached a duty-cycle range of 32 to 70% within the 2.1 to 2.7GHz bandwidth. Fig. 5.5(b) shows the total DC power dissipation of the CMOS driver at the 3 frequencies for the same V_{GG} range. As expected, $P_{DC,driver}$ is mainly a function of the frequency of operation.

f_0 [GHz]	P_{in} [dBm]	t_r [psec]	t_f [psec]	$\left(t_r + t_f\right)/T$ [-]	$P_{DC,driver}$ [W]
2.1	5.7			0.247	0.83
2.4	7.0	73.9	43.8	0.283	0.95
2.7	8.3			0.318	1.06

TABLE 5.1: Summary of CMOS driver I simulation performance with C_L = 5pF.

f_0 [GHz]	P_{in} [dBm]	t_r [psec]	t_f [psec]	$\left(t_r + t_f\right)/T$ [-]	$P_{DC,driver}$ [W]
2.1	5.7			0.233	0.79
2.4	7.0	69.1	41.7	0.266	0.90
2.7	8.3			0.299	1.01

TABLE 5.2: Summary of CMOS driver I simulation performance with C_L = 4pF.

Table 5.1 presents a summary of the performance metrics for the CMOS driver I with a load of 5pF. Note that $\left(t_r + t_f\right)/T$ at 2.7 GHz is close to the original design condition stated in equation (4.1). The condition in equation (4.1) was employed as a design reference (not as a tight specification) in order to cover the widest possible duty-cycle range. Table 5.2 presents a summary of performance metrics for the CMOS driver with a load of 4pF. In this later case, $\left(t_r + t_f\right)/T$ have improved due to the lower loading.

Notice that the output transistors of the CMOS driver are seeing the (simplified) load depicted in Figure 5.6. R_{subs} is the equivalent substrate resistance between the substrate at the bottom of C_{out} and the low-ohmic V_{SS0} power line. This resistance is neither zero nor very big. The worst case condition is $R_{subs} \rightarrow 0$, which will mean that a load of $C_{p1} + \left(C_{p2} + C_L\right) \| C_{out} \approx C_{p1} + C_{p2} + C_L$ will be seen by the output transistors, where $C_{out} \approx$ 49pF and $C_{p1} \approx C_{p2} \approx$ 1.2pF. This worst case condition has been the one employed during all the simulations performed in this chapter. The lateral parasitic capacitances of C_{out} are the most dominant parasitic capacitances of the CMOS driver, imposing an important loading effect on the output node.

5.2.1.5 Sources of power dissipation

From traditional inverter theory [36], the dominant sources of power dissipation in the CMOS driver are the dynamic losses due to charging and discharging of (parasitic) capacitances and the direct-path (or shoot-through) current. The direct-path current is due to the PMOS and NMOS transistors being simultaneously ON during each switching instant, creating an instantaneous short between the supply lines.

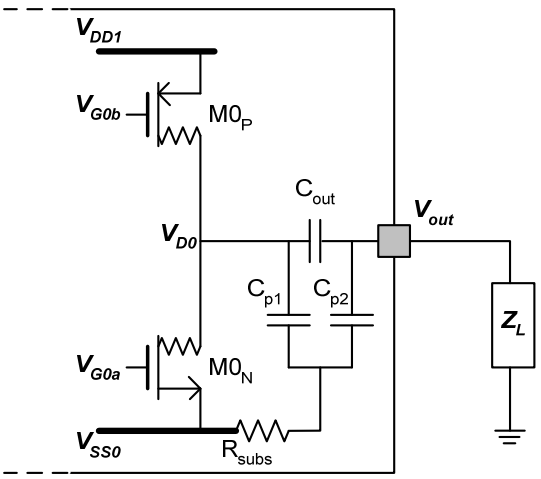


FIGURE 5.6: Load seen by the EDG01 output transistors.

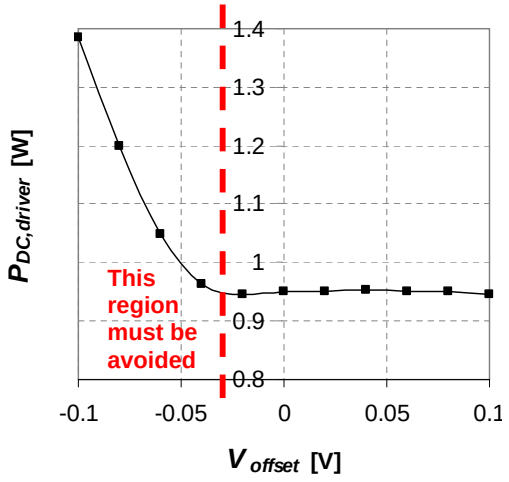


FIGURE 5.7: $P_{DC,driver}$ as a function of V_{offset} @ f_o = 2.4GHz, C_L = 5pF, V_{GG} = 0.6V.

In the CMOS driver design, the direct-path losses are eliminated by avoiding the overlap between the ON times of the EDG01 PMOS and NMOS devices during each period. This overlapping is directly controlled by a voltage offset difference (V_{offset}) between the biasing signals $BIAS_a$ and $BIAS_b$. From the simulation setup shown in Fig. 5.1, it was seen that each biasing voltage was set as $BIAS_{a,b} = V_{SS0,SS1} + V_{GG} \pm V_{offset}$. Figure 5.7 shows the effect of setting V_{offset} different than zero in the total DC power consumption of the CMOS driver I. Observe that there is a minimum value of V_{offset} that keeps the DC power dissipation at its lowest level (-25mV as observed in Fig. 5.7). If V_{offset} is made smaller (i.e. more negative) than that level, then the power dissipation increases rapidly due to the direct-path current. In the other hand, if V_{offset} increases then the power dissipation is at its minimum and nearly constant. If it is further increased, then there will be dead-times (times during which both PMOS and NMOS are simultaneously OFF). Dead-times can lead to higher driver efficiencies if the proper loading

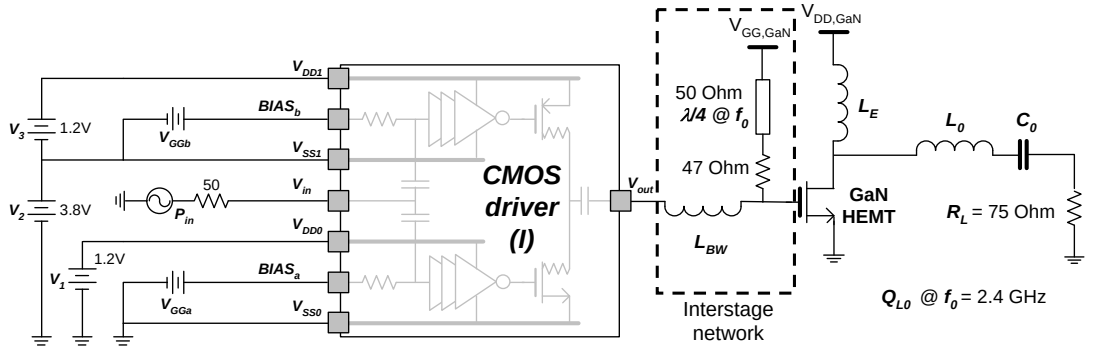


FIGURE 5.8: Simulation setup for the lineup of the GaN PA with the CMOS driver I chip.

conditions are met, as with a Class-DE amplifier [11].

5.2.2 Performance driving a Class-E GaN power amplifier

The intended load for the CMOS drivers is a GaN HEMT transistor working in Class-E. Although the system performance mainly depends on the Class-E design, driving of the GaN has some influence as well. This section presents the simulation results of the complete lineup of a broadband Class-E GaN power amplifier (very similar to the one in [5]) driven by the CMOS driver I. The focus of this section is to verify that the CMOS driver is able to properly drive the GaN transistor. The Class-E GaN power amplifier is working in suboptimum mode and its optimization is out of the scope of this work, but a good starting point is given, based in [5].

5.2.2.1 Simulation setup

The simulation setup for this section is given in Figure 5.8. In that figure, the Class-E GaN PA schematic is depicted. Unless otherwise stated, for all the simulations involving the GaN Class-E PA in the remaining of this chapter, $V_{DD,GaN} = 35\text{V}$ and $V_{GG,GaN} = -2.5\text{V}$. Two versions of the Class-E PA were simulated, their difference is only the loaded quality factor of the output filter Q_{L0} and the DC-feed inductor L_E. The first version is the GaN power amplifier already discussed in section C.3, of Chapter 2 ($Q_{L0} = 3$ and $L_E = 2.2nH$). The second version has an improved bandwidth performance ($Q_{L0} = 1.5$ and $L_E = 2.3nH$).

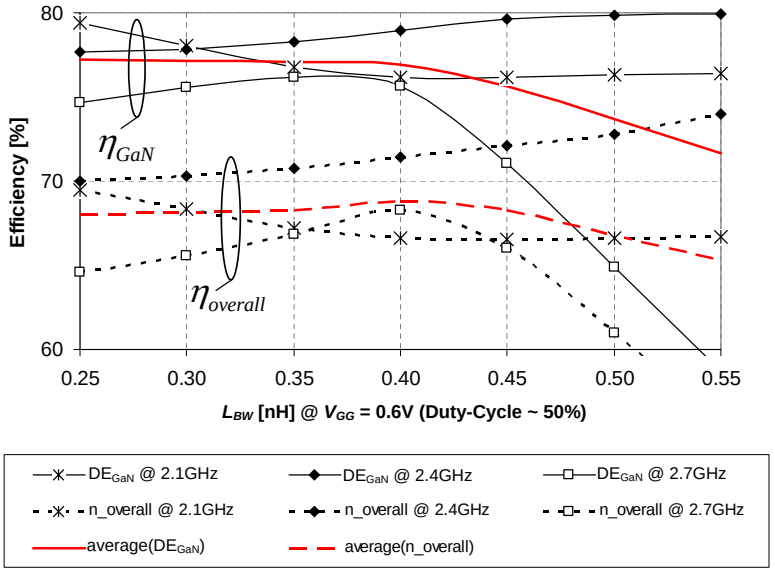


FIGURE 5.9: Selection of interstage bondwire. Note that L_{BW} = 0.4nH maximizes the efficiency performance over the entire bandwidth of interest (observed through the average efficiency values).

5.2.2.2 Influence of interstage network

The interstage network between the CMOS driver and the GaN transistor is of high importance. It must comply certain bandwidth and biasing requirements in order to allow the duty-cycle information to be transferred from the CMOS to the GaN stage, at the proper voltage levels required by the GaN transistor. This important issue will be discussed in detail in section 5.5, at the end of this chapter. For the moment, a very simple interstage network has been considered. This network, observed in Fig. 5.8, is composed of a bias network (a resistor and a quarter wavelength transmission line) and a bondwire connecting the output of the CMOS driver and the gate of the GaN transistor.

The value of the interstage bondwire L_{BW} has a big influence on the waveform at the GaN gate, and hence it must be properly chosen. Figure 5.9 shows the simulation results for the drain efficiency η_{GaN}[3] and overall efficiency $\eta_{overall}$[4] of the entire amplifier lineup as a function of the bondwire size at different frequencies within the bandwidth of interest. L_{BW} = 0.4nH was chosen since it maximizes the system efficiency performance over the entire bandwidth of interest, as observed through the average efficiency values shown in Figure 5.9.

[3] $\eta_{GaN} = \frac{P_{out}}{P_{DC,GaN}}$

[4] $\eta_{overall} = \frac{P_{out}}{P_{DC,GaN}+P_{in}+P_{DC,CMOS\,driver}}$ and PAE are approximately equal if the DC power dissipation of the CMOS driver is considered part of the total DC power dissipation of both GaN and CMOS stages in the PAE computation.

5.2.2.3 Simulations results without bondwires

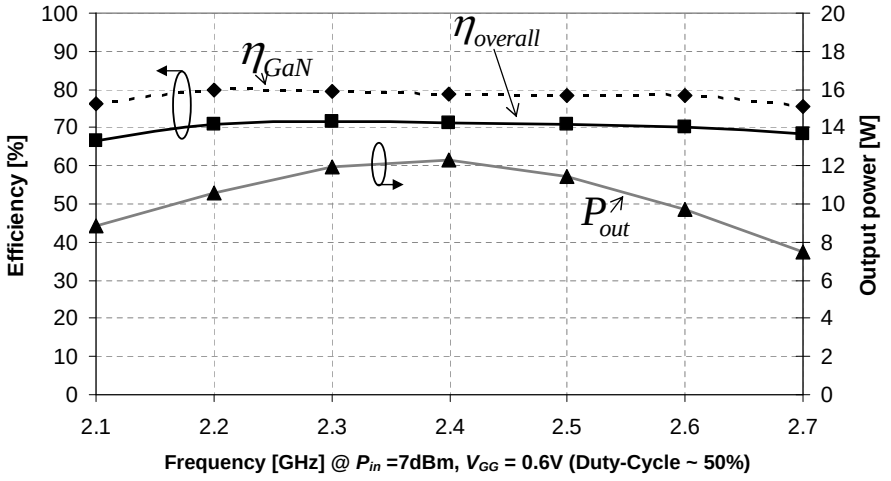
With a proper interstage bondwire selection, the system performance can be shown for the entire bandwidth of interest (2.1 to 2.7 GHz). This is done in Figure 5.10. Fig. 5.10(a) shows the performance of the CMOS driver I along with the same Class-E GaN power amplifier presented in section C.3 when discussing the ideal Class-E GaN performance. Note however that the bandwidth performance is limited due to the employed value of $Q_{L0} = 3$, as seen by the output power level as a function of frequency. In order to show that this was indeed the case, a slight modification of the Class-E power amplifier was done and Q_{L0} and L_E were modified to 1.5 and 2.3nH, respectively (very close to the design in [5]). Figure 5.10(b) shows the results of this second version of the Class-E GaN PA driven by the CMOS driver I. Note that also the input power of the CMOS driver has been reduced, since duty-cycle control is not employed here.

Although the system performance is mainly determined by the Class-E stage, as stated earlier, the simulation results in Fig. 5.10 shows the feasibility of a CMOS–GaN amplifier lineup.

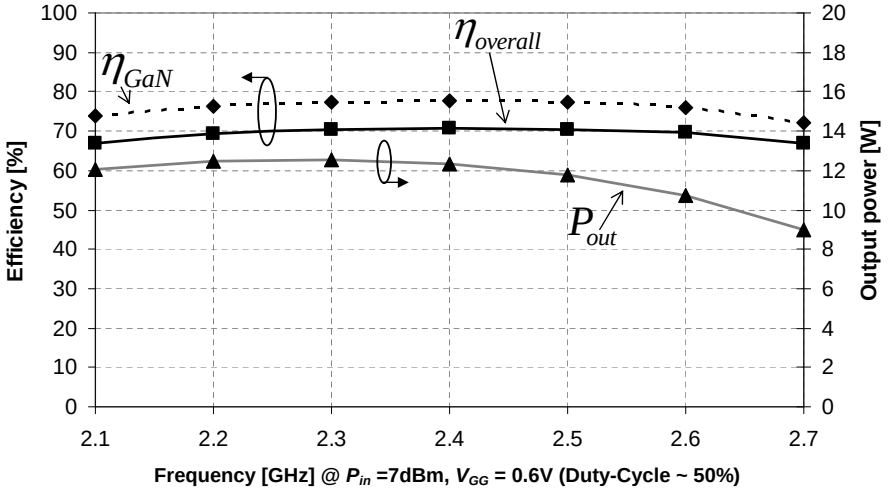
5.2.2.4 Simulations results with bondwires

This section presents the performance of the same amplifier lineup when including realistic bondwire models for the CMOS driver I. The bondwire shapes are dependent on the specific printed circuit board (PCB) design and the capabilities for the wiring process. For the simulations of this section, a thickness of 150μm for the CMOS driver I die and a direct bondwire connection to a 400μm thick PCB have been assumed for most of the pins. The bondwires at the output of the CMOS driver go directly to the GaN transistor die (both dies are assumed 200μm apart from each other). The bondwires were simulated in Agilent ADS and their 3D views can be observed in Figure 5.11. Shorter bondwires are possible in practice, however the simulated shapes are intended as a worst case condition to test the effectiveness of the AC-decoupling capacitors of the CMOS driver I.

Figure 5.12 shows the PSS voltage waveforms of the internal nodes of the chip (accessible only in simulations). Fig. 5.12(a) shows the voltages of the input and output of each inverter chain as well as all the supply lines, using the external (system) ground as a reference. Fig. 5.12(b) shows the same internal nodes but using the internal V_{SS0} as a reference. This last figure shows the waveforms that the chip will really see. Note that in this last figure, the stabilization of the supply voltages by the AC-decoupling capacitors can be observed.



(a) Q_{L0} = 3 and L_E = 2.2nH



(b) Q_{L0} = 1.5 and L_E = 2.3nH

FIGURE 5.10: Simulation results (without bondwires) for the lineup of the GaN PA (two versions) with the CMOS driver I chip: a) Q_{L0} = 3 and L_E = 2.2nH (same GaN Class E PA presented in section C.3, of Chapter 2), and b) Q_{L0} = 1.5 and L_E = 2.3nH (improved version of the original GaN Class E PA).

Figure 5.13 shows the performance of the complete lineup of the GaN PA driven by the CMOS driver I, including bondwires, for the entire bandwidth. The L_{BW} was implemented by the parallel of the 4 bondwires shown in Fig. 5.11 plus an additional series inductance. This additional series inductance (0.22nH) was needed to realize the proper value of L_{BW}. In practice, the AC-coupling output capacitor will have an equivalent series inductance (in the order of 0.1nH) that must be accounted for by L_{BW}. Hence, the series inductance of C_{out} and a proper shape (and number) of the output bondwires will implement L_{BW}. Notice that the amplifier lineup performance with (worst case) bondwires is comparable to the case without bondwires, demonstrating the effectiveness of the internal AC-decoupling capacitances.

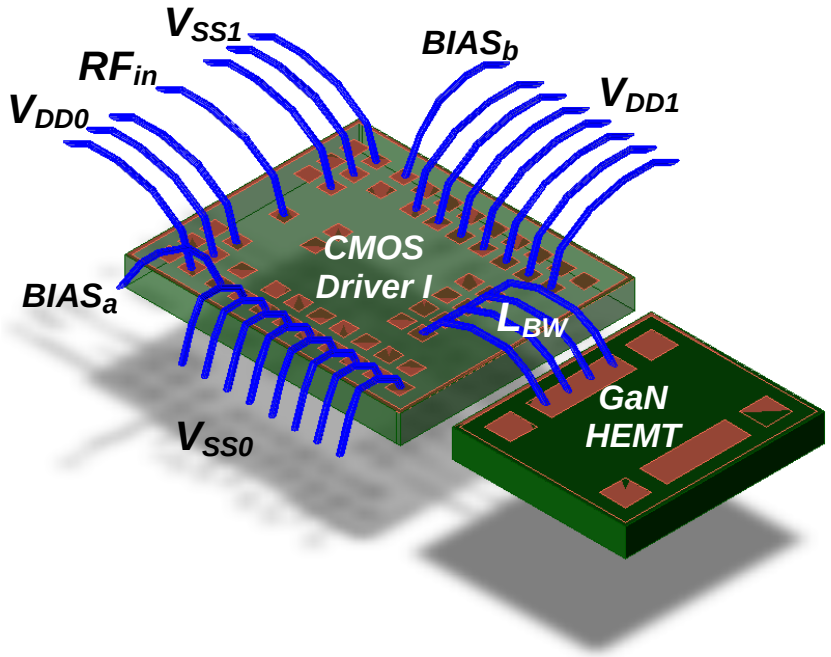


FIGURE 5.11: 3D view of the bondwire models employed in the simulation of the CMOS driver I and the Class-E GaN PA. The bondwires at the output of the CMOS driver represents L_{BW} but its actual implementation must be carefully designed.

5.3 Performance of CMOS drivers II and III

As stated earlier, this section provides only the most important simulation results for the CMOS driver II and III. It will not cover as many details as the former section because it is only intended to provide a framework for comparison between the three drivers.

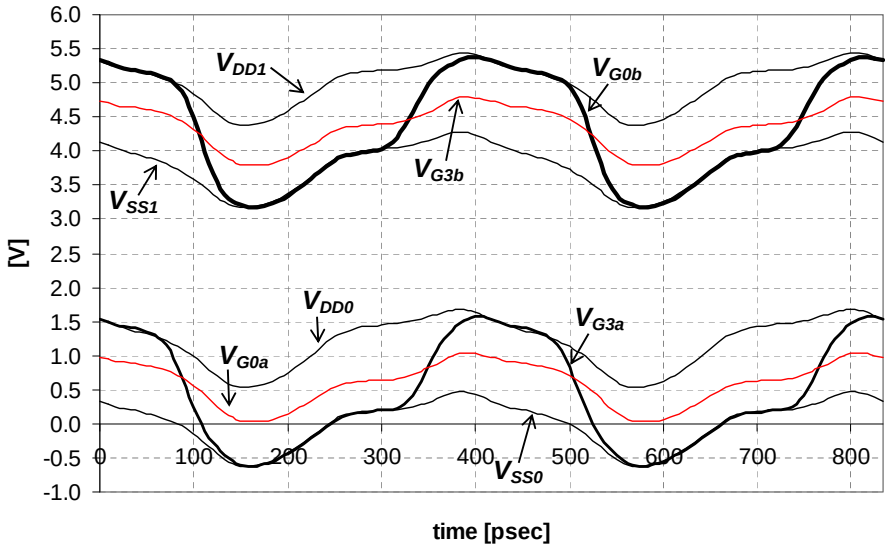
5.3.1 Performance with ideal capacitive load

5.3.1.1 Simulation setup

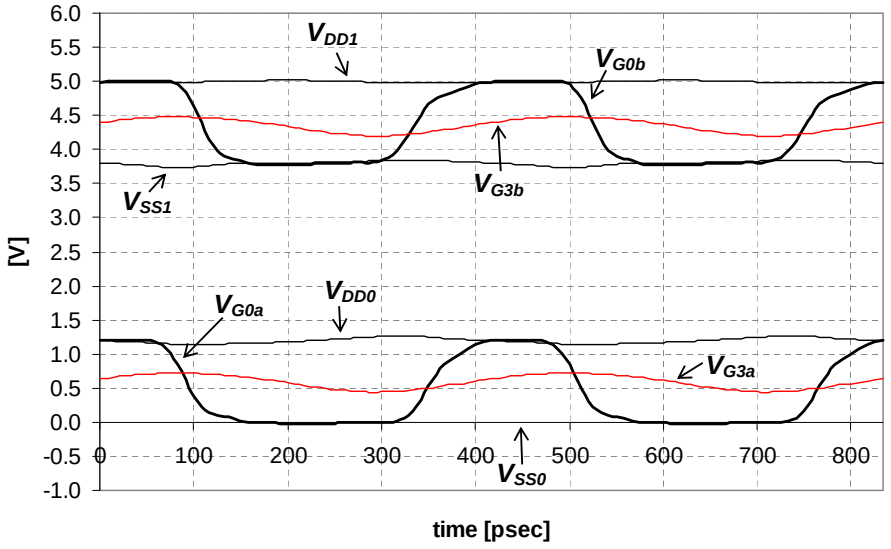
The simulation setup for the CMOS drivers II and III is shown in Figure 5.14. The load is an ideal capacitor of 5pF, as for the case of the CMOS driver I.

5.3.1.2 PSS voltage waveforms

Figures 5.15(a) and 5.15(b) depict the PSS voltage waveforms at 2.4GHz for the CMOS driver II and III, respectively. An important difference with respect to the CMOS driver I is that the waveform at the gate of the ED devices (EDG01 for CMOS driver II and EDG02 for CMOS



(a) Reference = chip outside ground



(b) Reference = chip internal V_{SS0}

FIGURE 5.12: PSS internal voltage waveforms of the CMOS driver I with bondwires at 2.4GHz @ P_{in} = 4dBm, V_{GG} = 0.6V: a) with respect to the chip outside ground, and b) with respect to the chip internal V_{SS0} reference (this is what the chip will see internally).

driver III) is not longer a square wave. This causes the output waveforms to be dependent on the input power level. The larger the input power, the more square the output signal will be. However, such an input power must be carefully selected not to compromise the reliability of the gate-oxide. The increased driving power for the CMOS driver III is due to the use of (2.5V) thick-oxide transistors (EDG02).

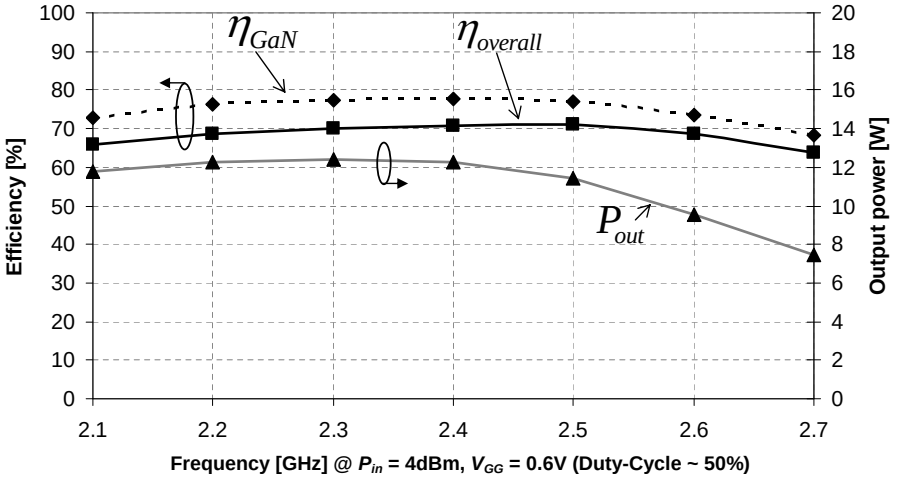


FIGURE 5.13: Simulation results for the lineup of the GaN PA driven by the CMOS driver I chip with bondwires. The L_{BW} was simulated with the parallel of the 4 bondwires at the output of the chip, shown in Fig. 5.11, plus 0.22nH of additional inductance.

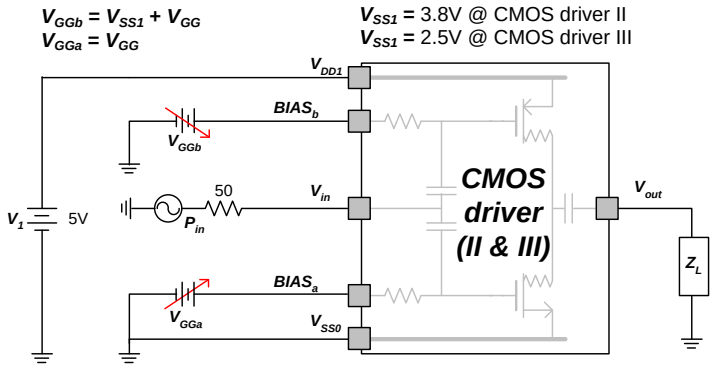
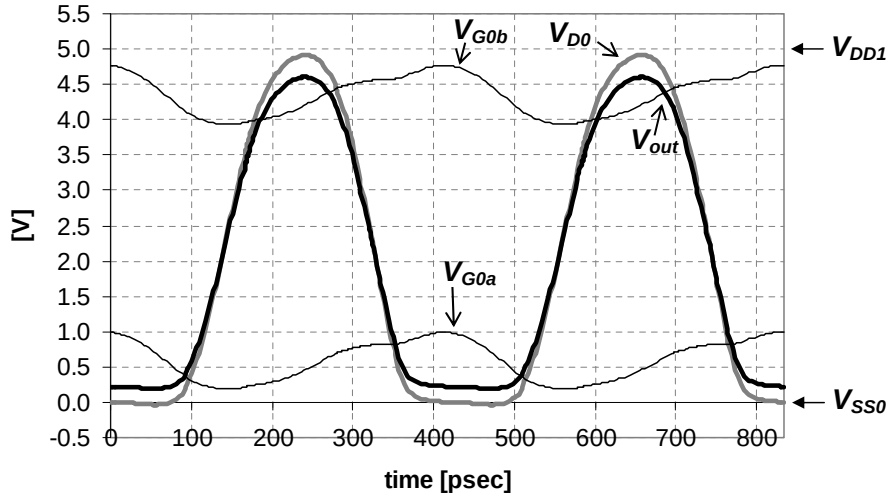


FIGURE 5.14: Simulation setup for the CMOS drivers II and III. The load is an ideal capacitor of 5pF.

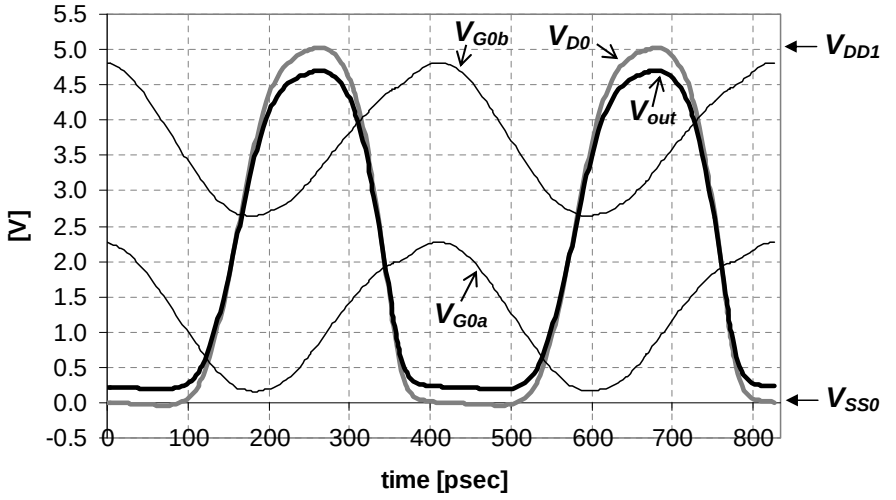
5.3.1.3 Duty-cycle performance

Figures 5.16(a) and 5.16(b) show the duty-cycle at 2.4GHz as a function of the gate bias voltage V_{GG} and the input power level for the CMOS driver II and III, respectively. Different than for the CMOS driver I case, the duty-cycle is an inverse function of V_{GG}. The duty-cycle being a direct or inverse function of V_{GG} is determined by the number of total inverter stages; an even number of stages will yield a direct function, while an odd number will cause an inverse relationship. The sensitivity of the duty-cycle (given by the slope of the lines in Fig. 5.16) reduces for larger input powers, as explained for the case of the CMOS driver I.

The absence of pre-driver stages makes the output waveforms dependent on the input driving power. Then, it is expected that the rising and falling times are a direct function of the input driving power. This effect can be observed in the normalized values of t_r/T, t_f/T and $\left(t_r + t_f\right)/T$



(a) PSS voltage waveforms for CMOS driver II @ P_{in} = 24dBm, V_{GG} = 0.6V

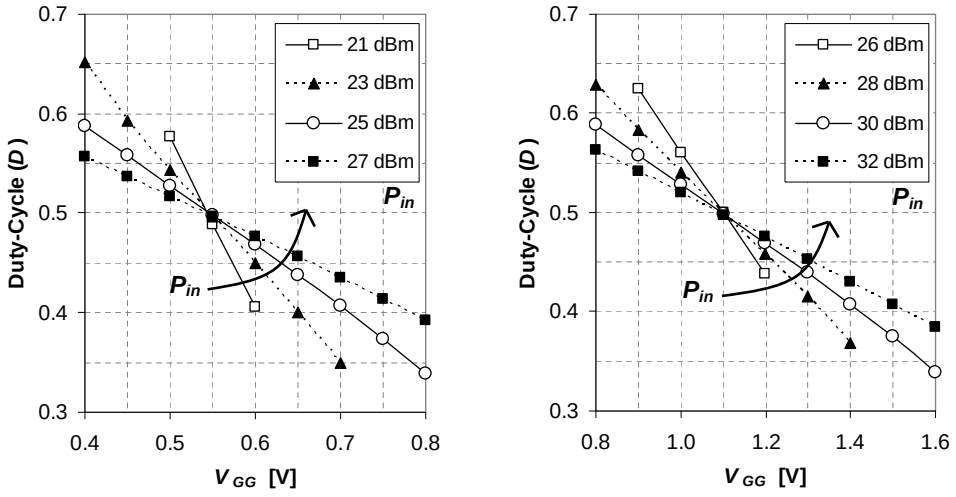


(b) PSS voltage waveforms for CMOS driver III @ P_{in} = 30dBm, V_{GG} = 1.25V

FIGURE 5.15: PSS voltage waveforms at f_0 = 2.4GHz @ C_L = 5pF, for a) CMOS driver II, and b) CMOS driver III.

as a function of input power given in Figures 5.17(a) and 5.17(b) for the CMOS driver II and III, respectively. Note that $\left(t_r + t_f\right)/T$ approach 0.3 as the input power is increased. However, large P_{in} levels will cause reliability issues.

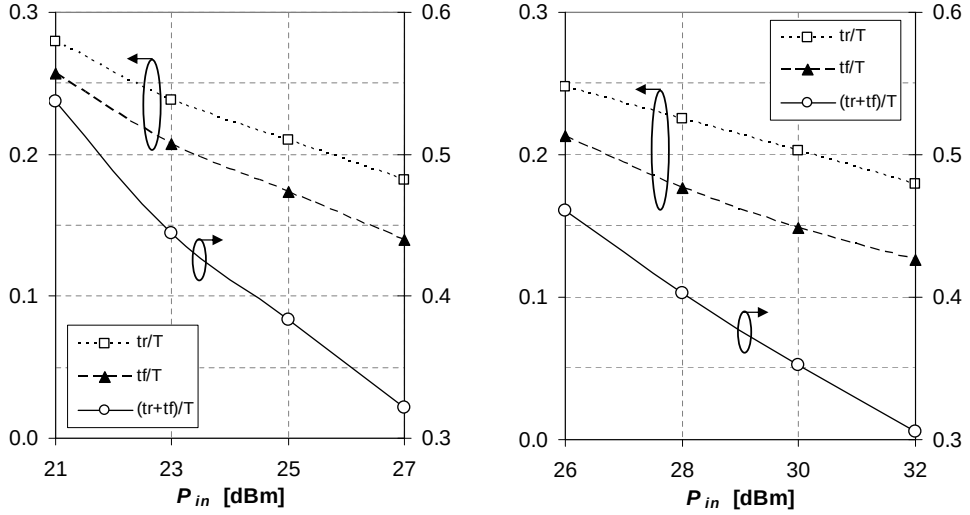
Tables 5.3 and 5.4 summarize the performance of the CMOS driver II and III, respectively, at 2.1, 2.4 and 2.7GHz for fixed input power. The selection of P_{in} was done based in the amplifier lineup performance, as it will be seen in the next section. Note that the normalized $\left(t_r + t_f\right)/T$ at 2.7GHz for both CMOS drivers II and III is significantly larger than for the CMOS driver I (see Table 5.1). This translates in a smaller duty-cycle range with respect to the CMOS driver I, as observed in Figs. 5.17(a) and 5.17(b).



(a) $D = f(V_{GG}, P_{in})$ for CMOS driver II

(b) $D = f(V_{GG}, P_{in})$ for CMOS driver III

FIGURE 5.16: Duty-cycle as a function of biasing level V_{GG} and P_{in} at f_0 = 2.4GHz, C_L = 5pF, for a) CMOS driver II, and b) CMOS driver III.



(a) Normalized t_r and t_f at f_0 = 2.4GHz for CMOS driver II

(b) Normalized t_r and t_f at f_0 = 2.4GHz for CMOS driver III

FIGURE 5.17: Normalized rising (t_r) and falling (t_f) times at f_0 = 2.4GHz as a function of P_{in} for a) CMOS driver II, and b) CMOS driver III.

f_0 [GHz]	P_{in} [dBm]	t_r [psec]	t_f [psec]	$\left(t_r + t_f\right)/T$ [-]	$P_{DC,driver}$ [W]
2.1	24	91.1	76.1	0.351	0.699
2.4	24	91.7	77.1	0.405	0.797
2.7	24	92.8	78.7	0.463	0.892

TABLE 5.3: Summary of CMOS driver II simulation performance with C_L = 5pF.

f_0 [GHz]	P_{in} [dBm]	t_r [psec]	t_f [psec]	$(t_r + t_f)/T$ [-]	$P_{DC,driver}$ [W]
2.1	30	82.1	59.5	0.297	0.722
2.4	30	83.0	59.8	0.343	0.820
2.7	30	84.7	60.7	0.393	0.913

TABLE 5.4: Summary of CMOS driver III simulation performance with C_L = 5pF.

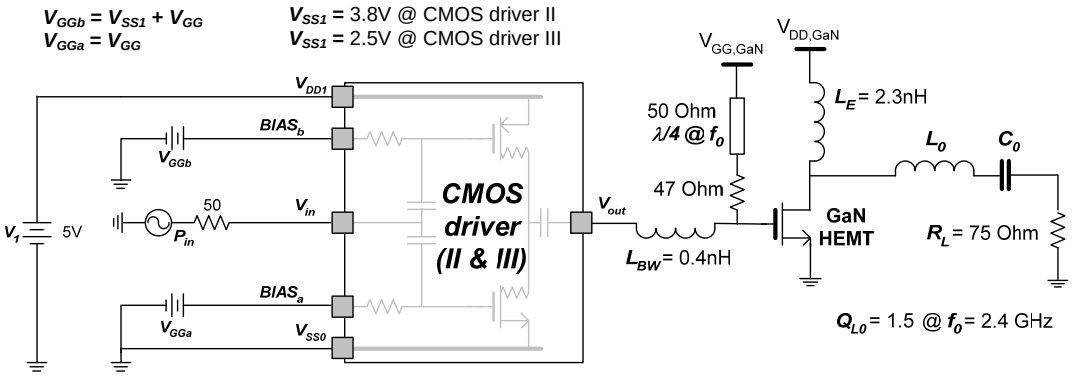


FIGURE 5.18: Simulation setup for the line-up of the GaN PA with the CMOS drivers II and III

5.3.2 Performance driving a Class E GaN power amplifier

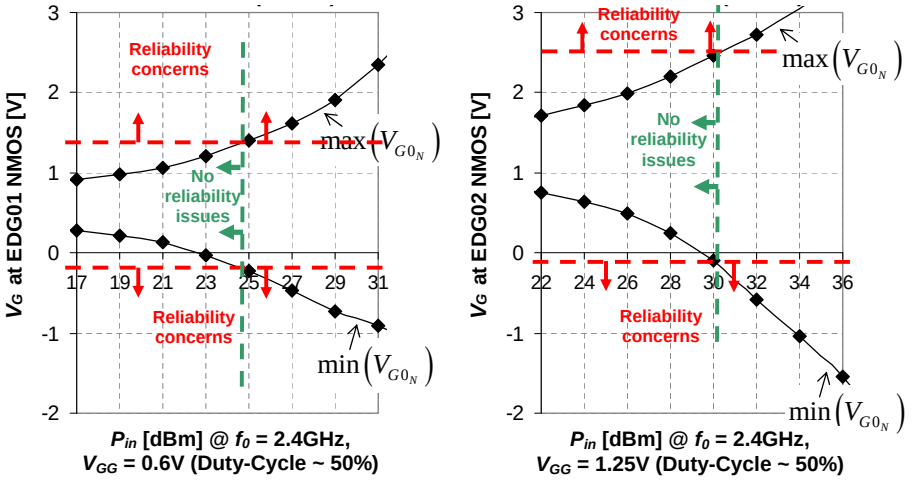
5.3.2.1 Simulation setup

The simulation setup for the complete amplifier lineup, employing both CMOS drivers II and III, is shown in Figure 5.18. The Class-E GaN stage is the same as the one employed earlier with the CMOS driver I. This is in order to directly compare the influence of the different CMOS drivers in the system performance.

5.3.2.2 Influence of input power on the Class-E GaN PA

Unlike the CMOS driver I, the input power in both CMOS drivers II and III influence the performance of the Class-E GaN power amplifier. As commented earlier, the larger the P_{in} the better the driving of the EDG0x devices. However, this imposes also a reliability risk for the gate-oxide of those devices.

Figure 5.19(a) and 5.19(b) shows the maximum and minimum levels of the voltage at the gate of the EDG0x NMOS devices in the CMOS driver II and III, respectively, as a function of input power. There is a similar increase on the peak to peak voltage of the PMOS devices as a function of input power, which is not shown in the figures for simplicity. Since the ED devices in the



(a) Min/Max(V_{G0a}) in CMOS driver II

(b) Min/Max(V_{G0a}) in CMOS driver III

FIGURE 5.19: Minimum and maximum gate voltage at the EDG0x NMOS transistor of a) CMOS driver II, and b) CMOS driver III as a function of P_{in}. The vertical line shows the boundary between the absolute reliable regions (according to the gate-oxide breakdown voltage limit of the EDG0x transistors); the left side is risk-free.

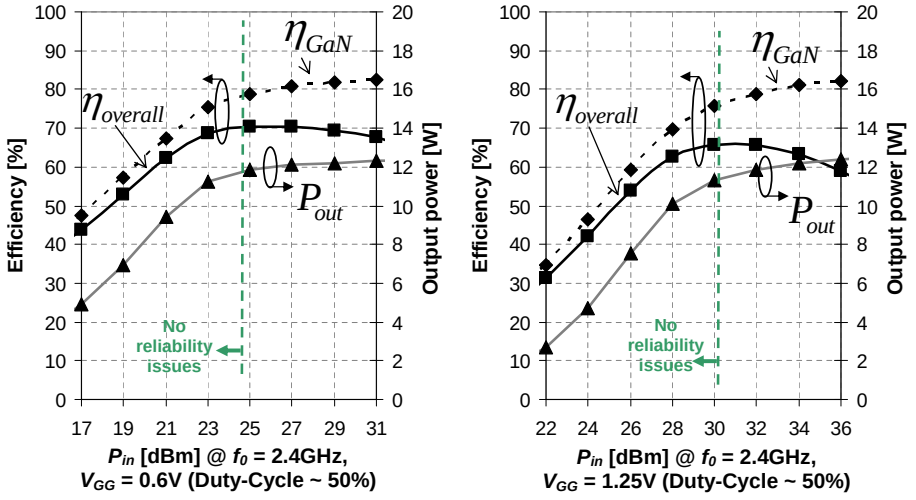
CMOS driver II are thin-oxide based, their reliable voltage limit for the gate-source oxide area is 1.2V to avoid breakdown[5]. Similarly, the ED devices in the CMOS driver III are thick-oxide based and therefore the limit is 2.5V. Due to these limits, there is a maximum reliable input power for each of the CMOS drivers II and III, as indicated in Fig. 5.19.

Figures 5.20(a) and 5.20(b) shows the performance of the entire amplifier lineup at 2.4GHz as a function of the input power when driving the GaN transistor with the CMOS driver II and III, respectively. Note that the overall efficiency $\eta_{overall}$ peaks for an input power level close to the maximum reliable one (derived from the gate maximum and minimum voltage levels shown in Fig. 5.19).

5.3.2.3 Simulations results without bondwires

Figures 5.21(a) and 5.21(b) show the simulation results over the entire bandwidth for the broadband Class-E GaN power amplifier driven by the CMOS drivers II and III, respectively. The input driving powers were selected as 24dBm and 30dBm for the CMOS drivers II and III, respectively, based on the results shown in Fig. 5.20 (smaller P_{in} for the highest $n_{overall}$).

[5]Although an extra margin of 10% is accepted in industry [24], here the most conservative DC limit has been adopted.



(a) GaN driven by CMOS driver II

(b) GaN driven by CMOS driver III

FIGURE 5.20: Power efficiencies and output power of the GaN driven by c) CMOS driver II and d) CMOS driver III as a function of P_{in}. The vertical red line shows the boundary between the absolute reliable regions (according to the gate-oxide breakdown voltage limit of the EDG0x transistors); the left side is risk-free.

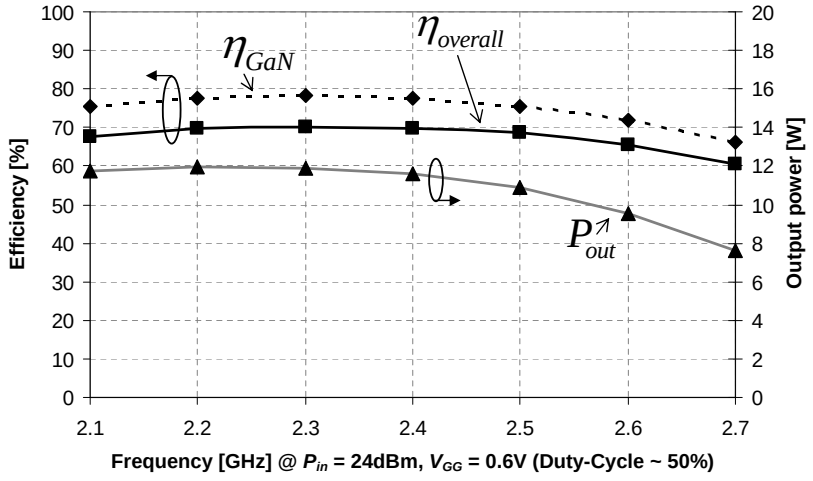
5.4 Performance comparison of the CMOS drivers I, II and III

This section summarizes the main differences among the three CMOS drivers with respect to their performance.

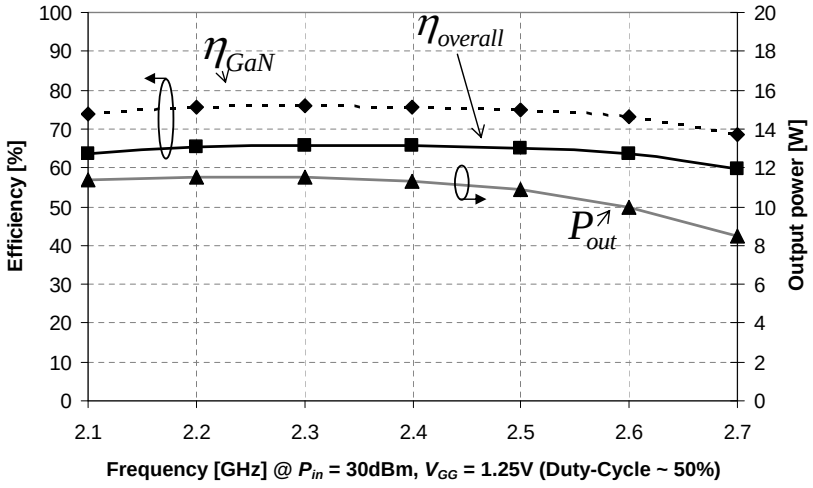
5.4.1 Duty-cycle capabilities

Due to the use of pre-drivers in the CMOS driver I, the performance of the EDG01 devices is independent of the input power level and it has the fastest rising and falling times among the three drivers. This in turn, translates in a wider controllable duty-cycle range.

Additionally, the reliability of gate-oxide in the CMOS driver II and III can be compromised if the input power levels are not properly selected. This means that there is a trade-off between driver performance and reliability with respect to the input power level, that does not exist in the CMOS driver I.



(a) GaN driven by CMOS driver II @ P_{in} = 24dBm, V_{GG} = 0.6V



(b) GaN driven by CMOS driver III @ P_{in} = 30dBm, V_{GG} = 1.25V

FIGURE 5.21: Simulation results (without bondwires) for the entire bandwidth for the amplifier lineup with the GaN transistor driven by the: a) CMOS driver II, and b) CMOS driver III.

5.4.2 Driving a broadband Class-E GaN power amplifier

Employing the common broadband Class-E GaN HEMT power amplifier, shown in the schematic of Fig. 5.18, the performance of the three CMOS drivers can be now compared at a system level. The results showed in Figs. 5.10(b), 5.21(a), and 5.21(b) (for the case of not using bondwires for the CMOS drivers) have been averaged over the 2.1 to 2.7 GHz bandwidth and are summarized in Table 5.5. From the data in that table, the following can be concluded:

- The average drain and overall efficiencies of the amplifier lineup can be considered comparable with the three CMOS drivers. However, there is a slight advantage for the CMOS driver I over the others.

Metric	CMOS driver		
	I (EDG01 with pre-drivers)	II (EDG01)	III (EDG02)
Average η_{GaN} [%]	75.7	74.6	74.0
Average $\eta_{overall}$ [%]	69.2	67.4	64.1
Average P_{out} [dBm]	40.6	40.3	40.3
P_{in} [dBm]	4	24	30
Average *Gain* [dB]	36.6	16.3	10.3

TABLE 5.5: Summary of (average) performance of the CMOS drivers when driving a common broadband Class-E GaN HEMT power amplifier.

- The drop of 0.3dB in the output power when using the CMOS drivers II and III show the dependency of the performance of the Class-E GaN PA with the input power level of those drivers. This does not happen with the CMOS driver I due to the square voltage signal at the ED devices, generated by its pre-driver stages.

- There is an important difference in the driving power required for the three drivers. The increased driving power for the CMOS driver III is due to the thick-oxide of the EDG02 devices with respect to the driver II. As expected, the pre-driver stages in the driver I reduces the input power required. This translates, at a system level, in different transducer power gains for the complete amplifier lineup according to the driver employed. The GaN transistor can provide by itself 17dB of transducer power gain [5][6]. Then, it can be observed that the CMOS driver I is the only driver that adds transducer gain to the amplifier lineup. The input driving power of the driver III is so high that the gain is significantly reduced with respect to the G_T of the GaN transistor above.

The advantages of the CMOS driver I come at the expense of a more complicated biasing scheme.

5.5 Interstage network requirements to preserve duty-cycle

A dedicated interstage network between the CMOS drivers and the GaN HEMT transistor is needed to preserve the duty-cycle information up to the GaN transistor, as indicated previously. This network must comply with certain bandwidth properties and biasing requirements. However, its design is out of the scope of this work. The simplest version of this network was already employed in this chapter (see Fig. 5.8). Note that in this configuration, due to the DC decoupling,

[6] In this work, we employed the same GaN transistor that was used in [5] and the Class E PA was almost the same.

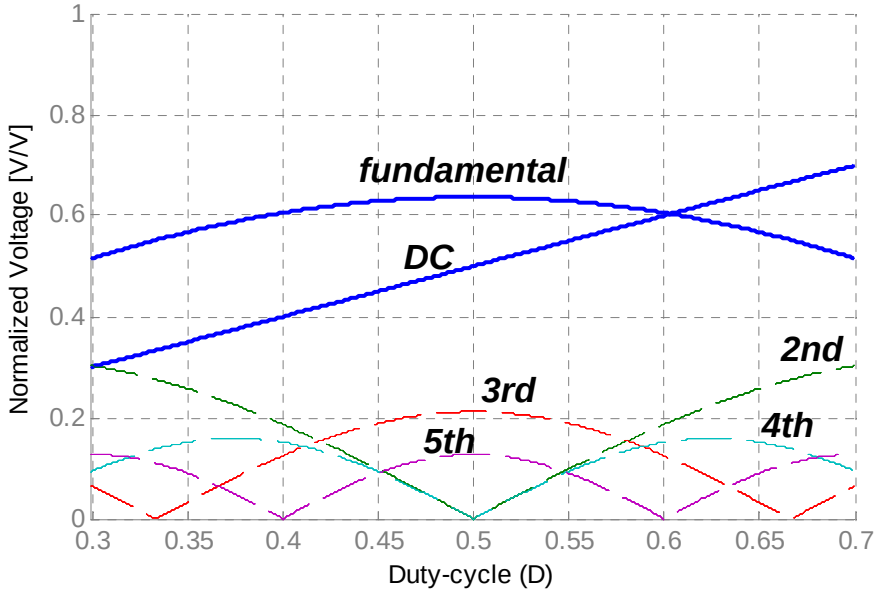


FIGURE 5.22: Harmonic content of a square wave as a function of its duty-cycle (D).

the duty-cycle is fixed to 50%. Hence, up to now, the performance of the complete amplifier lineup was demonstrated only at 50% duty-cycle. In this section, some of the requirements of the interstage network are discussed, but its final design and implementation is suggested as future work.

Note that the harmonic content of a square waveform will change with its duty-cycle. Figure 5.22 shows the normalized DC component and the first fifth harmonics of a square wave as a function of its duty-cycle, from 30 to 70% (i.e. $0.3 < D < 0.7$). Notice that only at 50% duty-cycle the voltage waveform does not contain even harmonics. Also observe that the DC component increases linearly with the duty-cycle, as expected from Fourier series.

The optimum driving of the Class E GaN HEMT power amplifier [33] was found to be an square wave [5] of approximately 5V swing, from -5 to 0V as previously shown in the schematic with ideal driving of Fig. C.11, in Section C.3 of Chapter 2. In the intended application, voltage shifting is needed to adjust the drive voltage to the needs of the GaN devices which can vary between +2 to -7V, over process generations. At this stage, this was solved by integrating an AC-coupling capacitor within the CMOS drivers and by biasing the gate of the GaN transistor at -2.5V. However, this is not the optimum solution from the duty-cycle controllability point of view.

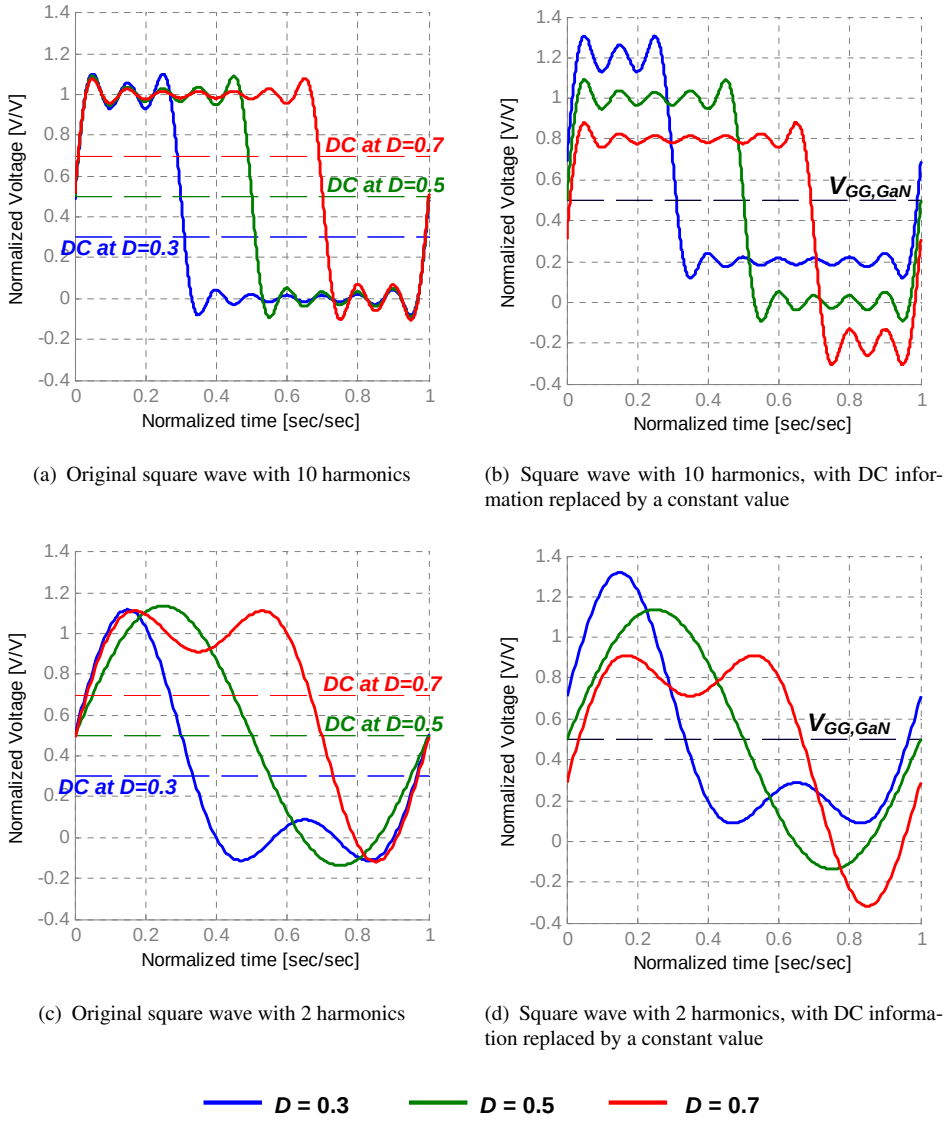
As observed from Fig. 5.22, the DC component is part of the duty-cycle signal. However, the AC-coupling capacitor removes this component from the signal that the CMOS driver generates.

Such a DC component is replaced by a *constant* biasing level ($V_{GG,GaN}$) at the GaN gate. This causes the waveform to not be optimum at duty-cycles different than 50% when no gate bias adjustment takes place.

To illustrate this better, Figure 5.23 shows the normalized square voltage waveforms at 30, 50 and 70% duty-cycle with 10, and 2 harmonics for the case of DC coupling (left-hand side) and when no DC coupling is present (right-hand side). Observe that it is possible to have duty-cycle information as long as the bandwidth of the interstage network covers the first two harmonics, as seen in Fig. 5.23(c). More harmonics will sharpen the waveform, but the bandwidth requirements for the interstage network will be more demanding. Second, observe the 'up/down shifting effect' on the waveform as a function of the duty-cycle when the DC component is replaced by a constant value. Without gate bias adjustment, this shifting effect will yield *non-optimum* driving signals at the gate of the GaN, leading to an overall reduction of drain efficiency in the Class E GaN power amplifier. So, in the testing phase using AC coupling, gate bias adjustments need to be done when changing the duty-cycle.

Although in this work an AC-coupling capacitor has been implemented, it is possible also to skip it and connect directly to the DC output of the inverter (through the output test bondpads). This allows more advanced testing, for example by biasing the CMOS driver between $V_{DD1} = 0$V and $V_{SS0} = -5$V to directly interface the CMOS driver swing with the GaN gate's needs.

To overcome the output voltage shifting problem in the next buffer/driver generation, a DC shift-able configuration should be employed. This can be realized by making use of Deep N-Well structures on the complete driver, that at the state of this design was not possible due to the internal construction of the EDG01 PMOS device.



(a) Original square wave with 10 harmonics

(b) Square wave with 10 harmonics, with DC information replaced by a constant value

(c) Original square wave with 2 harmonics

(d) Square wave with 2 harmonics, with DC information replaced by a constant value

FIGURE 5.23: Original square wave signals with: a) 10 harmonics, and b) 2 harmonics. Square wave signals with DC component replaced by a constant voltage ($V_{GG,GaN}$), with: c) 10 harmonics, and d) 2 harmonics. Note the 'up/down shifting effect' on the waveform when the DC component has been replaced by a constant.

Chapter 6

Conclusions and recommendations

In this thesis, two approaches for reaching high-voltage swings in CMOS technology have been investigated. The goal for those approaches was to reach a targeted 5V swing in order to enable CMOS technology to drive wide bandgap transistors, such as GaN HEMT. TSMC 65-nm CMOS technology was employed. The first approach studied cascode topologies employing standard devices. The second approach investigated and implemented inverter-based drivers employing custom extended-drain transistors.

6.1 Summary of main contributions

From the cascoded driver approach:

- A cascode topology of 4 stacked devices was proposed. This topology required the use of Deep N-Well and a dedicated biasing network in order to enable the stack of the fourth device. It reached a minimum output voltage swing of 7V, without compromising the reliability of the transistors. This topology can be applied in deeper sub-micron CMOS technologies due to the use of only standard devices.

From the inverter-based driver approach:

- Significant improvements in efficiency in back-off for broadband Class-E power amplifiers by duty-cycle control was proposed. This was shown by means of simulations of a broadband GaN HEMT power amplifier with ideal driving.

- An inverter-based driver topology was proposed that can exploit the maximum reliable drain-gate voltage limit of its output devices. Three versions of such topology were designed, implemented and fabricated. These versions employed extended-drain thin-oxide (CMOS driver I and II) and thick-oxide (CMOS driver III) devices. CMOS driver I included pre-driver stages made of standard thin-oxide devices in a Deep N-Well.

- Feasibility, at the CMOS driver chip level, of duty-cycle control was demonstrated. The CMOS driver I reached a duty-cycle range of 32 to 70% with a 5pF load, within a 2.1 to 2.7GHz bandwidth. Also, the variables involved in the duty-cycle control were identified and duty-cycle linearization was performed for broadband operation.

- The feasibility of a complete broadband amplifier lineup, consisting of a Class E GaN HEMT power amplifier and 65-nm CMOS drivers, has been demonstrated by means of post layout simulation results. A comparison between the three CMOS drivers has been performed, and the differences have been discussed.

- Several layout innovations were proposed and implemented in the CMOS drivers. They enabled higher performance and reduced silicon area usage.

6.2 Conclusions

The main conclusions reached on this thesis are the following.

From the Class-E cascoded driver approach:

- The voltage swing increases with the number of stacked devices but the efficiency reduces. It is advantageous to employ thin-oxide devices at the bottom of the stack, for speed, and thick-oxide devices on top, for high-voltage operation. The biasing circuitry complexity increases significantly after 3 or 4 stacked devices.

- Sizing each individual transistor in the stack is a compromise between the total switch resistance of the stack and the loading of each individual internal node. Capacitive losses at the internal nodes are proportional to the square of the voltage swing at the node, and hence, the top-most internal node parasitic capacitance has the largest effect on efficiency loss. Those losses can be reduced by inductive tuning (as proposed by [29]), but this consumes extra silicon area and narrows the operating bandwidth.

- The significantly increased breakdown capabilities of the extended-drain transistors with respect to the standard devices, despite their intrinsic reduced RF performance, leads to more efficient high-voltage/power circuits. This is, although the drain extension in the ED devices lower their intrinsic RF performance, the use of cascode topologies are less efficient than an equivalent solution employing only ED devices.

From the inverter-based driver approach:

- An inverter-based driver with extended-drain devices can provide the high-voltage swing required to drive wide bandgap transistors, such as GaN HEMT. It does not require inductors and hence it is a broadband solution. With this approach, a high-efficient and broadband complete amplifier lineup of CMOS + GaN technologies has been demonstrated[1].

- The CMOS driver (III) employs thick-oxide extended-drain (EDG02) devices. It can exceed by much the voltage swing required by the intended application (e.g. at least of 10V [22]). However, due to its 2.5V thick-oxide gate, the required driving power is very high and it reduces the power gain of the entire amplifier lineup. Hence, its use with the intended Class-E GaN power amplifier seems to be not justified. Still, it could be employed in other higher power applications.

- The CMOS drivers (I and II) employ thin-oxide extended-drain (EDG01) devices. Besides the reduced driving power required, they allow the direct implementation of pre-driver stages employing standard thin-oxide devices (Deep N-Well is necessary). These pre-driver stages avoid influencing the performance of the final switchmode power amplifier with respect to the input power level, providing a more optimum waveform at the gate of the GaN transistor. Also, the thin-oxide pre-drivers of the CMOS driver I facilitates its integration with other processing high-speed CMOS blocks.

- The interstage network between the CMOS drivers and the GaN transistor requires a special design since it has a major influence in the performance of the complete amplifier lineup. If only static 50% duty-cycle is required, this network can be as simple as a properly designed bondwire inductor and a DC bias at the gate of the GaN transistor (since an AC-coupling capacitor has been integrated in the CMOS drivers). However, if variable

[1] At the moment of writing this document, only simulation results were available due to the manufacturing time of the CMOS drivers.

duty-cycle is desired for the GaN power amplifier, this network must permit at least two harmonics and include the DC component of the signal generated by the CMOS driver.

6.3 Future work recommendations

The suggestions for further work are for the inverter-based approach:

- Measurements should be carried out in order to experimentally verify the results of this work.
- The EDG01 devices have great potential for high-voltage/power CMOS applications. However, those (NMOS/PMOS) devices must still be properly characterized; a better model should be developed and reliability tests should be carried out.
- The special design of an interstage network, between the CMOS drivers and the GaN transistor, that allows duty-cycle control is recommended as future work. This is so in order to experimentally explore the advantages of duty-cycle control at a system level. Initial steps towards this suggestion are presented in Section 5.5 of Chapter 5.
- In the CMOS drivers, further work is suggested in simplifying their biasing scheme (i.e., generating internally the voltage supplies) and duty-cycle control (i.e., reducing the number of control/biasing external pins), with a focus on system-level usage. If duty-cycle control is not required, then simplifications of the CMOS drivers future implementations are possible (e.g. the biasing network can be implemented inside the chip by a simple resistive voltage divider, etc.).

Appendix A

Brief 65-nm CMOS technology characterization for switchmode circuits

In this appendix, some relevant information about 65-nm CMOS is provided that will support quantitatively the ideas developed in this thesis. This technology overview is mainly concerned with the implementation of RF switchmode power amplifiers and drivers. In these kind of circuits the transistors must work as switches[1]. A simple but useful characterization of the transistors for such purposes is in terms of ON-resistance, R_{ON}, gate and drain parasitic capacitances, C_g and C_d.

A.1 65-nm CMOS technology overview

The designs presented along this work employed a standard 65-nm low-standby-power (LP) CMOS technology from TSMC. This technology has dual gate oxide and up to seven Copper (Cu) metal layers[2]. It also includes triple–well option.

[1] An ideal switching transistor will go instantaneously from cut-off to deep triode region. However, at RF frequencies this behavior can be questionable. If a transistor can be considered, or not, as a switch will depend on the specific operating frequency and the technology capabilities. For 65-nm CMOS the switch approximation seems to be valid are good enough for up to a few GHz.

[2] There is an additional Aluminum (Al) metal layer on top that can be used as well. However, despite the fact that this layer is $\approx 61\%$ thicker than the thickest Cu metal layer, its maximum DC current rating is only around 35% of the Cu layer for the same width. This makes the Al metal layer not much advantageous for power routing compared with the Cu layer, converting it in only an *auxiliary metal layer* for this purpose.

This technology offers thin and thick oxide MOS devices. Additionally, novel high-voltage extended-drain (ED) devices have recently been able to implement in this technology at no extra cost [21, 22]. The characterization for the standard and custom ED devices in this CMOS technology will be discussed in the next sections.

A.2 Standard MOS devices

The standard transistors available in this technology are 1.2V thin-oxide (that will be called G01 devices) and 2.5V thick-oxide (G02) devices. The gate oxide thickness in the G01 devices is around 2.6nm for NMOS and 2.8nm for PMOS, while their minimum drawn gate length is 60nm. The gate oxide thickness of the G02 devices is around 5.6nm for NMOS and 5.9nm for PMOS, while their minimum drawn gate length is 280nm. The G02 devices are slower I/O devices intended for interfacing the core G01 devices. However, due to their increased break-down capabilities[3], the G02 devices can also be used for power amplification purposes in the low GHz range of frequencies where they are fast enough.

The characterization of the MOS devices was done by simulations using Cadence Spectre and the RF models available within the 65-nm CMOS technology package provided[4]. For obtaining R_{ON}, C_g and C_d, a common simulation set-up was employed, which is shown in Fig. A.1. R_{ON} is obtained from DC-simulations while the parasitic capacitances C_g and C_d are obtained from AC-simulations.

Figure A.2 shows the simulation results for the R_{ON} of the standard G01 and G02 transistors as a function of V_{DS} for 90%, 95% and 100% of the nominal gate–source voltage (1.2V for G01 devices and 2.5V for G02 devices). A factor of $\approx$ 2.6 exists between the ON-resistance of the G01 PMOS and the NMOS switches. This factor was $\approx$ 2.7 for the G02 devices. The condition for deep triode region is $V_{DS} << 2\,(V_{GS} - V_{th})$, and hence the lowest ON-resistance happens for values of V_{DS} close to zero in the plots of Fig. A.2 (the threshold voltage is around 0.4 and 0.5V for the standard G01 and G02 NMOS devices, respectively).

The parasitic capacitances are non-linear and a function of *biasing* conditions as well as of lay-out implementations (due to the junction capacitances, whose area and perimeter depend on the

[3]The higher break-down voltages come at the cost of reduced RF performance.

[4]The RF models in 65-nm CMOS include only up-to metal 1. Although the results from such models will be more realistic than taking the 'naked models', they can still be considered somehow optimistic for a practical design (which could include up-to 7 or 8 metal layers). However, they are still a good reference for initial design purposes.

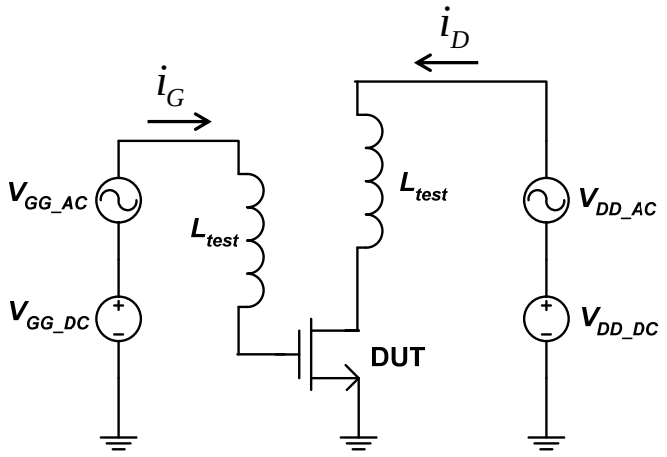
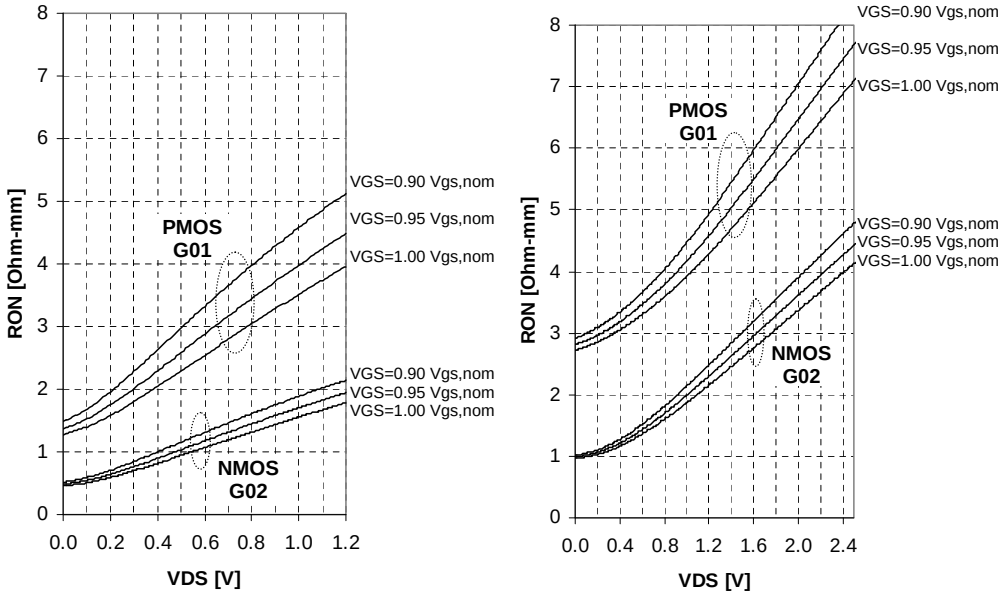


FIGURE A.1: Common simulation setup for the extraction of R_{ON}, C_g and C_d



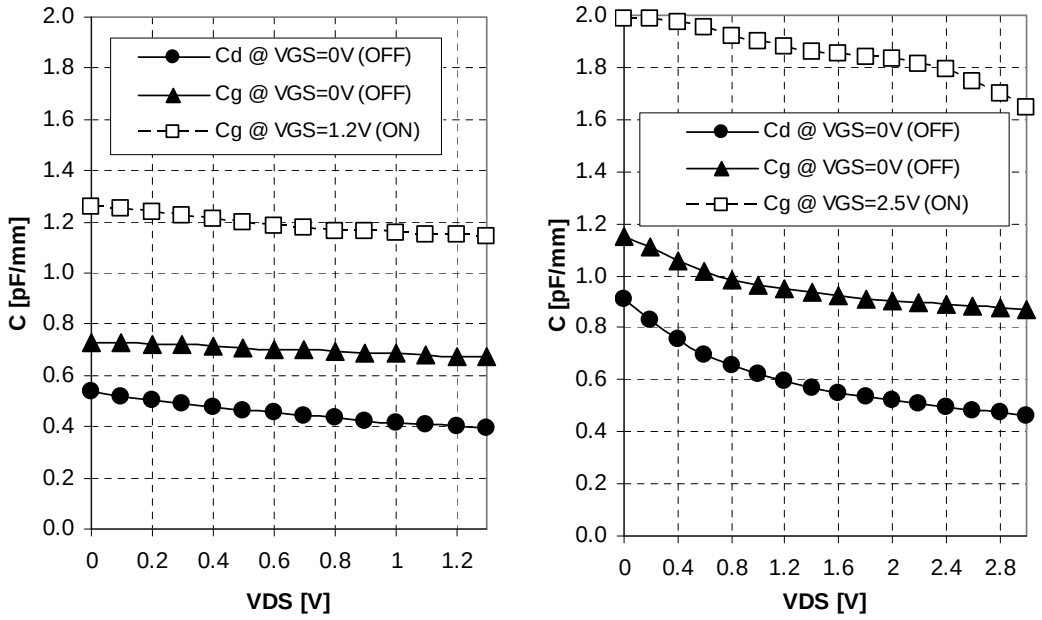
(a) at V_{GS} = 1.08, 1.14, 1.2 V (b) at V_{GS} = 2.25, 2.375, 2.5 V

FIGURE A.2: R_{ON} as a function of V_{DS} for standard G01 and G02 transistors in 65-nm CMOS.

MOS layout [43]). However a simple lumped-equivalent value is good enough for this work and will yield to powerful insights for the design of switchmode circuits. The gate parasitic capacitance will include the gate-source, gate-substrate and gate-drain[5] parasitic capacitances. The drain parasitic capacitance will include the drain-source and drain-substrate parasitic capacitances.

Since the parasitic capacitances between NMOS and PMOS devices of same size can be considered equal, only the NMOS has been used to extract those capacitances. Figure A.3 shows

[5]The gate-drain capacitance will be normally seen increased due to the *Miller effect*, since the transistor is working as a switch and the gate and drain voltage changes with opposite directions in each RF cycle.



(a) standard G01 NMOS

(b) standard G02 NMOS

FIGURE A.3: C_g and C_d as a function of V_{DS} for standard transistors in 65-nm CMOS.

	G01 NMOS	G01 PMOS	G02 NMOS	G02 PMOS
R_{ON} [Ω-mm]	0.5	1.3	1.0	2.7
C_g [pF/mm]	1.3	1.3	2.0	2.0
C_d [pF/mm]	0.5	0.5	0.6	0.6

TABLE A.1: Summary of the characterization for Standard MOS devices in 65-nm CMOS.

the simulation results for the G01 and G02 NMOS gate and drain capacitances per mm of gate width, given as a function of V_{DS} for ON- ($V_{GS} = 1.2V/2.5V$) and OFF-state ($V_{GS} = 0V$). In switchmode PAs, the characterization of C_d is meaningful during the OFF-state (when the drain voltage swings).

Although the simulation results in figures A.2 and A.3 show the dependency on biasing conditions, a single equivalent lumped value is needed per each parameter in the context of the present work, as stated before. A very accurate way to obtain such values would be by considering the probability density function of the dynamic load line of the switching transistors. However, in this work a more pragmatic and general approach has been adopted, which is still good enough for quantitative purposes. The R_{ON} value is taken at its minimum value (this is somehow optimistic, but simple and general). C_d comes from a standard average over the V_{DS} voltage range in the OFF-state. Since C_g will be used to estimate the input driving power, it will be taken at its worst case condition. The summary of those values, per mm of gate width, is presented in Table A.1.

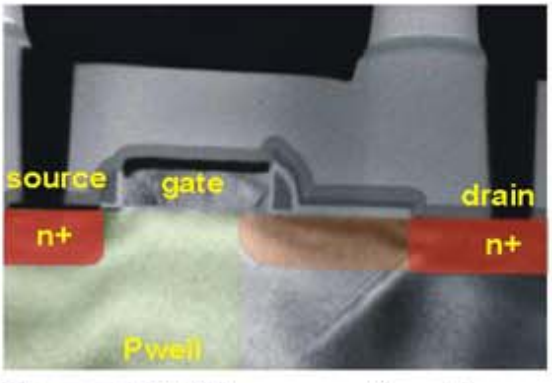


FIGURE A.4: SEM cross-section of an extended-drain NMOS in baseline 65-nm CMOS (from [22]).

Since both C_g and C_d are proportional to the transistor gate width, $\left(C_g, C_d\right) \propto W_g$, and $R_{ON} \propto 1/W_g$, then the product $R_{ON} \cdot C_d$ is constant and technology defined [18]. In general, a larger switch will imply a more efficient amplifier, since the ratio between the ON-resistance and the real load will reduce, increasing the efficiency (this is, briefly speaking, more power will be dissipated into the load than into the switch) [11]. However, increasing the switch size after certain point will not longer help since other sources of power dissipation will start to dominate. Such an increase would demand higher input powers, reducing the power gain (and hence the PAE) and the maximum frequency of operation due to increased parasitic capacitances if a proper layout strategy is not followed [2].

A.3 Extended-drain MOS devices

The fine lithography dimensions and alignment, the standard large number of process steps and masks, as well as smart layout techniques have enabled the construction of innovative high-voltage extended-drain MOSFETs [21, 22]. Such devices can be based in thin (1.2V) and in thick (2.5V) gate oxides [1]. Figure A.4 shows a scanning electron microscope (SEM) cross-section of one of those extended-drain devices.

The extended-drain thick-oxide device (EDG02) has been recently measured and fabricated to implement high efficient Class E power amplifiers from 1W with 60% PAE (in a cascode topology) [1] up to 3.4W with 70% PAE [2]. However, at the time this work was performed, very little information about the EDG01 device was known. No electrical model for such a device was yet available.

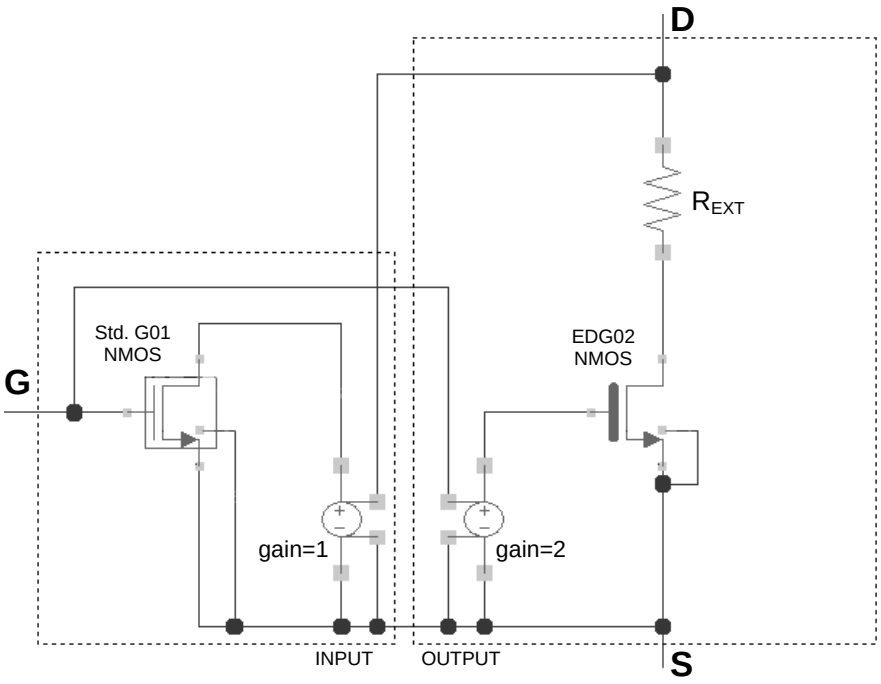


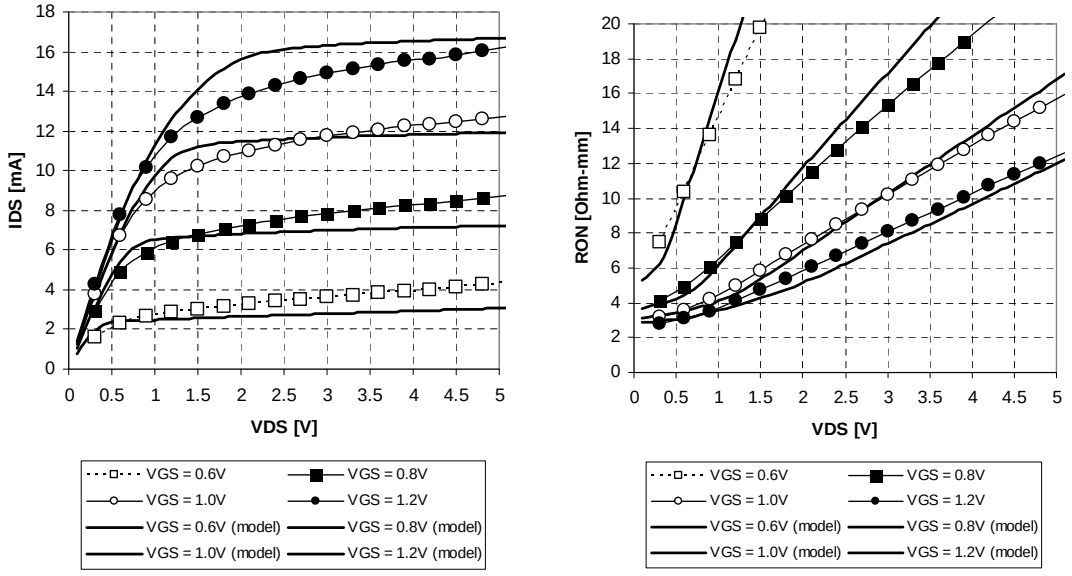
FIGURE A.5: Schematic of the zero-order electrical model developed for the EDG01 NMOS transistor in 65-nm CMOS.

This author had access to an on-wafer EDG01 NMOS transistor[6]. On a single EDG01 device, fast DC measurements were performed in order to characterize it at a zero order level. The basic layout cell of such a device was available. Such a layout cell resembled a cascode configuration between a standard G01 and a extended-drain G02 device [37]. From this observation and the DC measurements of the device, an electrical model of *zero-order* was developed in order to have a basic tool to perform simulations[7]. From the construction of this novel EDG01 device (which uses the same concepts and was developed by the same author of [22]), the device is expected to support at least 5V DC gate-drain oxide voltage before breakdown. This breakdown limit is particularly important for the designs presented in Chapter 4.

The circuit schematic of the electrical model that was developed is shown in figure A.5. The transistor at the gate side is the standard G01 NMOS, as resembled in the EDG01 cell layout. The transistor at the drain is a thick-oxide (EDG02) transistor that uses a NXP Semiconductors proprietary model for the EDG02 device. The resistor R_{EXT} was used to get a better fitting with respect to the DC measurement results. Note that, although the output part of the transistor behaves like an EDG02 device, the input of the model is the one of a thin-oxide G01 1.2V device. Therefore, in the model there is a voltage controlled voltage source with a gain of 2 to

[6]This transistor was a 40μm width EDG01 NMOS with 16 fingers (i.e. finger length = 2.5μm).

[7]The output stage of the integrated CMOS drivers I and II, designed and discussed in Chapter 4, is based in the EDG01 devices, so having a minimum tool to simulate those devices was essential.



(a) I_{DS}-V_{DS} curves

(b) R_{ON} as a function of V_{DS} for several values of V_{GS}

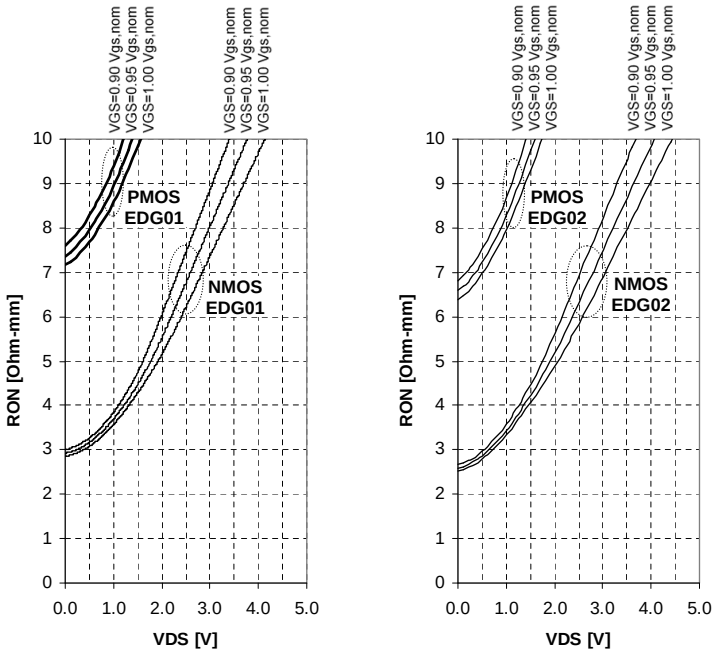
FIGURE A.6: Comparison between the simulation of the EDG01 zero-order model (solid lines) and the on-wafer DC measurements performed on a single 40μm EDG01 NMOS device (lines with symbols).

interface the input side (i.e. the G01 device) to the gate of the G02 device. Additionally, the reverse voltage controlled voltage source with a unitary gain helps to include some output-to-input dynamic behavior in the model.

Despite its simplicity, this zero-order model was close enough to the real DC measurements, allowing its use in later simulations. The original on-wafer DC measurements of the available EDG01 device can be seen in figure A.6(a) (with symbol marks) along with the simulation results of the model developed (with solid lines). Figure A.6(b) shows the ON-resistance DC measurements along with the model simulation results. Please observe that the model is more accurate for the lowest values of R_{ON}, which is important for the characterization of the EDG01 device in the context of this work.

Once an initial model for the EDG01 device was obtained, the properties of both types of extended drain transistors (i.e. EDG01 and EDG02) can complete the basic characterization of the 65-nm CMOS technology for switchmode PAs and drivers. Figure A.7 shows the simulation results for the R_{ON} of EDG01 and EDG02. For the case of the EDG01 PMOS, an extension of the quick model developed for the EDG01 NMOS was done by scaling up the R_{ON} resistance with a factor of 2.5.

Figure A.8 shows the simulation results for the gate and drain parasitic capacitances of the



(a) at V_{GS} = 1.08, 1.14, 1.2 V (b) at V_{GS} = 2.25, 2.375, 2.5 V

FIGURE A.7: R_{ON} as a function of V_{DS} for Extended Drain G01 and G02 transistors in 65-nm CMOS.

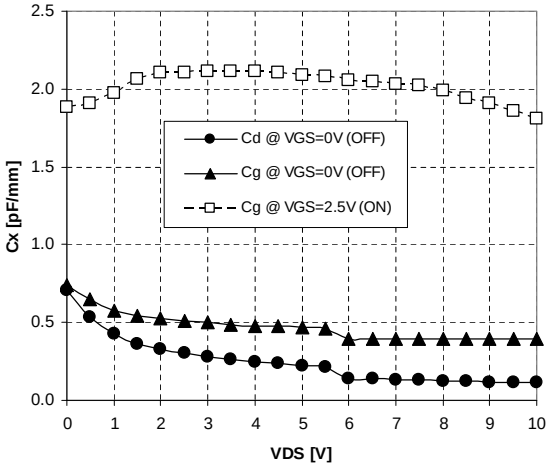


FIGURE A.8: C_g and C_d as a function of V_{DS} for Extended Drain G02 transistors in 65-nm CMOS.

	EDG01 NMOS	EDG01 PMOS	EDG02 NMOS	EDG02 PMOS
R_{ON} [Ω-mm]	2.9∗	7.2∗	2.6	6.4
C_g [pF/mm]	1.3∗	1.3∗	1.9	1.9
C_d [pF/mm]	0.5∗	0.5∗	0.3	0.3

TABLE A.2: Summary of the characterization for extended-drain MOS devices in 65-nm CMOS. *These values are estimated from the zero-order model developed for the EDG01 devices, as explained.

EDG02 NMOS transistor. Since there was not official electrical model, nor RF measurements available, for the EDG01 NMOS transistor, its parasitics were estimated based in the construction of the device; its C_g is expected to be similar to the one of the standard G01 device, while its C_d should be similar to the standard G02 NMOS (since the EDG01 expected reliable swing is lower than the one for the EDG02). Note that in Figures A.7 and A.8, a maximum V_{DS}=10V is used for the EDG02 NMOS, which is its minimum breakdown voltage [22], and V_{DS}=5V is employed for the EDG01, which is its expected (minimum) breakdown voltage capability. Table A.2 summarizes the main parameters of the extended-drain transistors available in 65-nm CMOS.

Appendix B

Detailed Analytical Derivation for the General Class E Model

In this appendix, a detailed step-by-step derivation of the general Class E model is developed. This general model assumes narrow-band operation; however the bandwidth can be extended in practical designs. The model covers optimum Class E [14], as well as sub-optimum modes. For the sub-optimum modes we can distinguish between Variable-Voltage [18] and Variable-Slope [20] modes, and a simultaneous mix of both.

The analytical procedure for the derivation presented in this appendix is based in the works of [17, 18, 20, 44, 45]. The model developed in this appendix unifies the model in all the former works and it also extends it by adding the influence of the finite DC-feed inductor quality factor and a finite resistance during the OFF-state. The results of this model is extensively discussed in Appendix C from a design point of view.

B.1 Circuit description and assumptions

This model is based on the circuit schematic shown in Figure B.1. The assumptions in the model are the following ones:

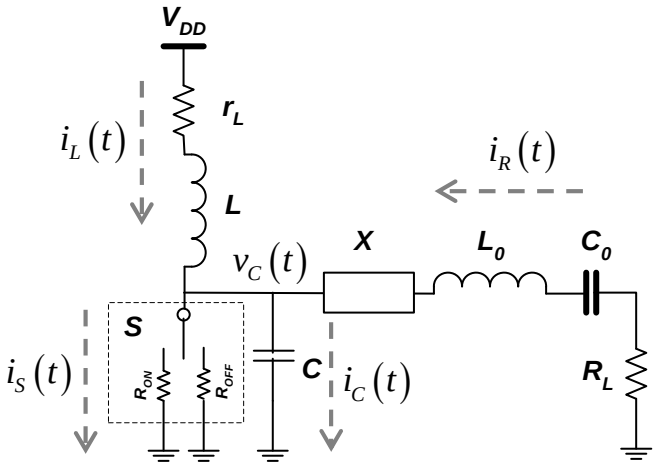


FIGURE B.1: General Class E circuit schematic.

- The only real power dissipation in the circuit occurs in load R_L[1], the switch finite resistances during ON- and OFF-state (R_{ON} and R_{OFF}, respectively) and r_L (that accounts for the finite DC-feed inductor quality factor).
- The switching device toggles instantaneously between its ON-state with finite R_{ON} resistance and its OFF-state with finite R_{OFF} resistance.
- The loaded quality factor (Q_{L0}) of the series resonant circuit (L_0 and C_0) is high enough for the current at the load to be considered sinusoidal at the operating frequency.

Note that for the last condition to be true, Q_{L0} must go to infinity, however such an assumption is widely used since it simplifies the analysis considerably [17].

Table B.1 describe the parameters used in the derivation of the Class E model equations. Some of those parameters will be used to group other parameters in order to handle the equations more conveniently. Most of those simplifying parameters were taken as proposed in [17]. Figure B.2 shows the voltage and current waveforms for the general Class E model, and there the meaning of some of the parameters in Table B.1 can be appreciated.

B.2 Derivation of the switch voltage equations

The analytical model of Class E is done in time-domain. It starts with the currents at the switch drain node, this is

[1]Note that the load R_L represents the real load that the amplifier sees.

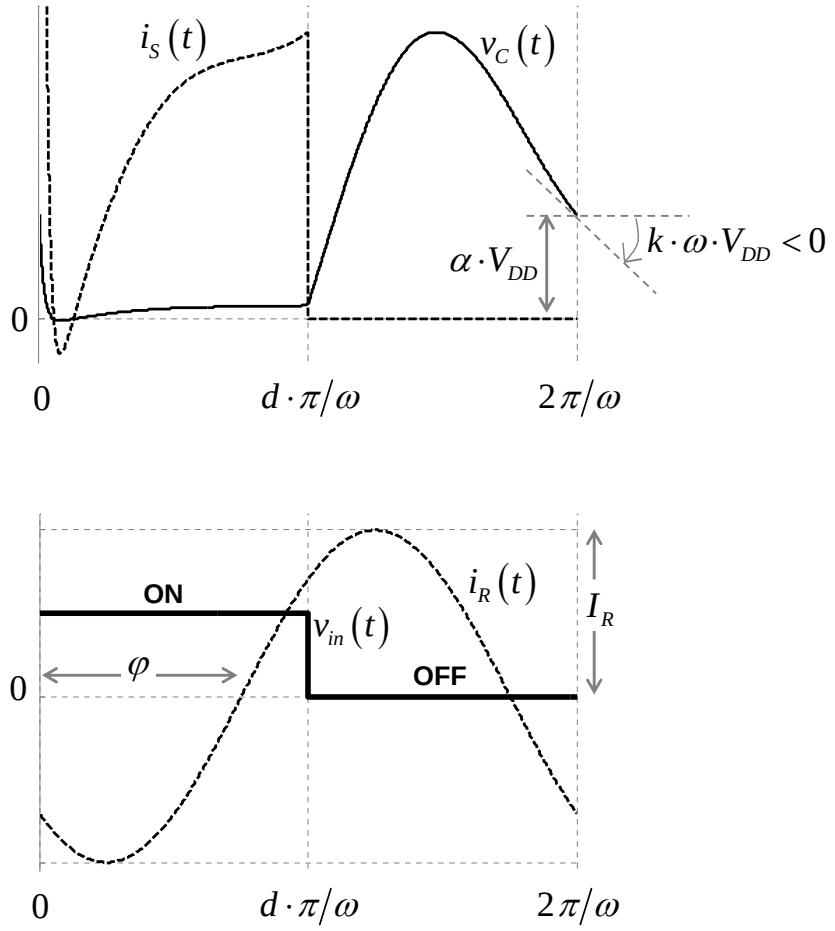


FIGURE B.2: General Class E voltage and current waveforms.

Symbol	Parameter description
V_{DD}	Supply voltage [V]
I_R	Load R_L current amplitude [A]
$\omega = 2\pi \cdot f$	Operating frequency [rad/s]
$Q_L = \omega \cdot L/r_L$	DC-feed inductor L quality factor [-]
$m = \omega \cdot R_{ON} \cdot C$	A technology-frequency parameter [rad]
$h = \omega \cdot R_{OFF} \cdot C$	A technology-frequency parameter [rad]
α	Variable-Voltage defining parameter [-]
k	Variable-Slope defining parameter [-]
d	Duty-Cycle defining parameter [-]
φ	Output voltage phase [rad]
$\omega_p = \frac{1}{\sqrt{LC}}$	LC tuning angular frequency [rad/s]
$q = \omega_p/\omega = \frac{1}{\omega\sqrt{LC}}$	Ratio between ω_p and ω [-]
$p = \omega \cdot L \cdot I_R/V_{DD}$	A grouping parameter for simplification [-]

TABLE B.1: Description of the parameters used in the Class E Model.

$$i_R(t) + i_L(t) - i_C(t) - i_S(t) = 0 \tag{B.1}$$

where

$$i_R(t) = I_R \sin(\omega t + \varphi) \tag{B.2a}$$

$$i_L(t) = \frac{1}{L}\int_{-\infty}^{t} v_L(t)\,\mathrm{d}t = \frac{1}{L}\int_{\tau^+}^{t} [V_{DD} - r_L \cdot i_L(t) - v_C(t)]\,\mathrm{d}t + I_L(\tau^-) \tag{B.2b}$$

$$i_C(t) = C\frac{\mathrm{d}v_C(t)}{\mathrm{d}t} \tag{B.2c}$$

$$i_S(t) = \begin{cases} \frac{v_{C_{ON}}(t)}{R_{ON}} & \text{for } 0 < t < d \cdot \pi/\omega \\ \frac{v_{C_{OFF}}(t)}{R_{OFF}} & \text{for } d \cdot \pi/\omega < t < 2 \cdot \pi/\omega \end{cases} \tag{B.2d}$$

are the load R_L, inductor L, capacitor C and switch S currents, respectively. $v_C(t)$ is the voltage across the switch terminals, while $v_{C_{ON}}(t)$ and $v_{C_{OFF}}(t)$ is the same voltage during the ON-state and OFF-state, respectively. τ in eq. (B.2b) represents the time when the switch toggles, i.e. $\tau = 0$ and $\tau = d \cdot \pi/\omega$ at the start of the ON-state and OFF-state, respectively.

During the ON-state, i.e. during the time interval $0 < t < d \cdot \pi/\omega$, eq. (B.1) is

$$\begin{aligned} I_R \sin(\omega t + \varphi) + \left\{\frac{1}{L}\int_{0^+}^{t} [V_{DD} - r_L \cdot i_L(t) - v_C(t)]\,\mathrm{d}t + I_L(0^-)\right\} \\ - C\frac{\mathrm{d}v_{C_{ON}}(t)}{\mathrm{d}t} - \frac{v_{C_{ON}}(t)}{R_{ON}} = 0 \end{aligned} \tag{B.3}$$

which after deriving by t gets to:

$$\omega I_R \cos(\omega t + \varphi) + \frac{1}{L}[V_{DD} - r_L \cdot i_L(t) - v_{C_{ON}}(t)] - C\frac{\mathrm{d}^2 v_{C_{ON}}(t)}{\mathrm{d}^2 t} - \frac{v_{C_{ON}}(t)}{R_{ON}} = 0 \tag{B.4}$$

since $i_L(t) = i_C(t) + i_S(t) - i_R(t)$ (from eq. (B.1)), the above equation is equivalent to:

$$\omega I_R \cos(\omega t + \varphi) + \frac{1}{L}\left[V_{DD} - r_L\left\{i_C(t) + i_S(t) - i_R(t)\right\} - v_{C_{ON}}(t)\right] - C\frac{\mathrm{d}^2 v_{C_{ON}}(t)}{\mathrm{d}^2 t} - \frac{v_{C_{ON}}(t)}{R_{ON}} = 0 \tag{B.5a}$$

$$\omega I_R \cos(\omega t + \varphi) + \frac{1}{L}\left[V_{DD} - r_L\left\{C\frac{\mathrm{d}v_{C_{ON}}(t)}{\mathrm{d}t} + \frac{v_{C_{ON}}(t)}{R_{ON}} - I_R \sin(\omega t + \varphi)\right\} - v_{C_{ON}}(t)\right] - C\frac{\mathrm{d}^2 v_{C_{ON}}(t)}{\mathrm{d}^2 t} - \frac{v_{C_{ON}}(t)}{R_{ON}} = 0 \tag{B.5b}$$

$$C\frac{\mathrm{d}^2 v_{C_{ON}}(t)}{\mathrm{d}^2 t} + \frac{\mathrm{d}v_{C_{ON}}(t)}{\mathrm{d}t}\left(\frac{1}{R_{ON}} + \frac{r_L \cdot C}{L}\right) + v_{C_{ON}}(t)\left(\frac{1}{L} + \frac{r_L}{L \cdot R_{ON}}\right) = \frac{r_L \cdot I_R}{L}\sin(\omega t + \varphi) + \omega I_R \cos(\omega t + \varphi) + \frac{V_{DD}}{L} \tag{B.5c}$$

The above equation can be conveniently re-arranged, using the equivalent parameters shown in Table B.1, as

$$\frac{\mathrm{d}^2 v_{C_{ON}}(t)}{\mathrm{d}^2 t} + \frac{\mathrm{d}v_{C_{ON}}(t)}{\mathrm{d}t}\left(\frac{\omega}{m} + \frac{\omega}{Q_L}\right) + v_{C_{ON}}(t)\left(\omega^2 q^2 + \frac{\omega^2}{Q_L \cdot m}\right) = \frac{V_{DD} \cdot q^2 \omega^2 p}{Q_L}\sin(\omega t + \varphi) + V_{DD} \cdot q^2 \omega^2 p \cos(\omega t + \varphi) + V_{DD} \cdot q^2 \omega \tag{B.6}$$

Notice that equations (B.4), (B.5), & (B.6) are all equivalent expressions of the same second-order, linear, non-homogeneous, differential equation that models the switch voltage during the ON-state. However, for convenience eq. (B.6) will be the one to be used in future references.

During the OFF-state, i.e. during the time interval $d \cdot \pi/\omega < t < 2 \cdot \pi/\omega$, eq. (B.1) is

$$I_R \sin(\omega t + \varphi) + \left\{\frac{1}{L}\int_{d\cdot\pi/\omega^+}^{t}\left[V_{DD} - r_L \cdot i_L(t) - v_C(t)\right]\mathrm{d}t + I_L(d \cdot \pi/\omega^-)\right\} - C\frac{\mathrm{d}v_{C_{OFF}}(t)}{\mathrm{d}t} - \frac{v_{C_{OFF}}(t)}{R_{OFF}} = 0 \tag{B.7}$$

which after deriving by t gets to:

$$\omega I_R \cos(\omega t + \varphi) + \frac{1}{L}\left[V_{DD} - r_L \cdot i_L(t) - v_{C_{OFF}}(t)\right] - C\frac{\mathrm{d}^2 v_{C_{OFF}}(t)}{\mathrm{d}^2 t} - \frac{v_{C_{OFF}}(t)}{R_{OFF}} = 0 \tag{B.8}$$

The above equation is equivalent to:

$$C\frac{\mathrm{d}^2 v_{C_{OFF}}(t)}{\mathrm{d}^2 t} + \frac{\mathrm{d}v_{C_{OFF}}(t)}{\mathrm{d}t}\left(\frac{1}{R_{OFF}} + \frac{r_L \cdot C}{L}\right) + v_{C_{OFF}}(t)\left(\frac{1}{L} + \frac{r_L}{L \cdot R_{OFF}}\right) = \frac{r_L \cdot I_R}{L}\sin(\omega t + \varphi) + \omega I_R \cos(\omega t + \varphi) + \frac{V_{DD}}{L} \tag{B.9}$$

Also, the above expression can be conveniently re-arranged, using $h = \omega \cdot R_{OFF} \cdot C$, as

$$\frac{\mathrm{d}^2 v_{C_{OFF}}(t)}{\mathrm{d}^2 t} + \frac{\mathrm{d}v_{C_{OFF}}(t)}{\mathrm{d}t}\left(\frac{\omega}{h} + \frac{\omega}{Q_L}\right) + v_{C_{OFF}}(t)\left(\omega^2 q^2 + \frac{\omega^2}{Q_L \cdot h}\right) = \frac{V_{DD} \cdot q^2 \omega^2 p}{Q_L}\sin(\omega t + \varphi) + V_{DD} \cdot q^2 \omega^2 p \cos(\omega t + \varphi) + V_{DD} \cdot q^2 \omega \tag{B.10}$$

Equations (B.8), (B.9) & (B.10) are all equivalent expressions of the same second-order, linear, non-homogeneous, differential equation that models the switch voltage during the OFF-state. Eq. (B.10) will be the one to be solved, to be in line with eq. (B.6).

B.3 Solving the switch voltage equations

The voltage across the switch is given by:

$$v_C(t) = \begin{cases} v_{C_{ON}}(t) & \text{for } 0 < t < d \cdot \pi/\omega \\ v_{C_{OFF}}(t) & \text{for } d \cdot \pi/\omega < t < 2 \cdot \pi/\omega \end{cases} \tag{B.11}$$

where $v_{C_{ON}}(t)$ and $v_{C_{OFF}}(t)$ are found by solving the second-order differential equations given by eqs. (B.6) and (B.10), respectively. The solution to those differential equations are of the form

$$v_{C_{ON}}(t) = K_{1,1} \cdot e^{a_{1,1} \cdot \omega t} + K_{1,2} \cdot e^{a_{1,2} \cdot \omega t} + K_{1,3} \cdot \sin(\omega t + \varphi) + K_{1,4} \cdot \cos(\omega t + \varphi) + K_{1,5} \tag{B.12a}$$

$$v_{C_{OFF}}(t) = K_{2,1} \cdot e^{a_{2,1} \cdot \omega t} + K_{2,2} \cdot e^{a_{2,2} \cdot \omega t} + K_{2,3} \cdot \sin(\omega t + \varphi) + K_{2,4} \cdot \cos(\omega t + \varphi) + K_{2,5} \tag{B.12b}$$

The constants in the above equations are found as follows:

- $a_{1,1}$, $a_{1,2}$ and $a_{2,1}$, $a_{2,2}$ by solving the *homogeneous* part of eqs. (B.6) & (B.10);
- $K_{1,3}$–$K_{1,5}$ and $K_{2,3}$–$K_{2,5}$ by solving the *non-homogeneous* part of eqs. (B.6) & (B.10); and,
- $K_{1,1}$, $K_{1,2}$ and $K_{2,1}$, $K_{2,2}$ by using a pair of boundary conditions[2] and solving simultaneously eqs. (B.12a) & (B.12b) in the switching moments.

B.3.1 Finding $a_{1,1}$, $a_{1,2}$ and $a_{2,1}$, $a_{2,2}$

The homogeneous part of eq. (B.6) is

$$\frac{\mathrm{d}^2 v_{C_{ON}}(t)}{\mathrm{d}^2 t} + \frac{\mathrm{d}v_{C_{ON}}(t)}{\mathrm{d}t}\left(\frac{\omega}{m} + \frac{\omega}{Q_L}\right) + v_{C_{ON}}(t)\left(\omega^2 q^2 + \frac{\omega^2}{Q_L \cdot m}\right) = 0 \tag{B.13}$$

whose solution is given by

$$v_{C_{ON}}(t) = K_{1,1} \cdot e^{A_{1,1} \cdot t} + K_{1,2} \cdot e^{A_{1,2} \cdot t} \tag{B.14}$$

where,

$$\begin{aligned} A_{1,1}, A_{1,2} &= \frac{-\left(\frac{\omega}{m} + \frac{\omega}{Q_L}\right) \pm \sqrt{\left(\frac{\omega}{m} + \frac{\omega}{Q_L}\right)^2 - 4\left(\omega^2 q^2 + \frac{\omega^2}{Q_L \cdot m}\right)}}{2} \\ &= \omega \cdot \{a_{1,1}, a_{1,2}\} \end{aligned} \tag{B.15}$$

Hence,

$$a_{1,1}, a_{1,2} = \frac{1}{2}\left[-\left(\frac{1}{m} + \frac{1}{Q_L}\right) \pm \sqrt{\left(\frac{1}{m} + \frac{1}{Q_L}\right)^2 - 4\left(q^2 + \frac{1}{Q_L \cdot m}\right)}\right] \tag{B.16}$$

Similarly, the homogeneous part of eq. (B.10) is

[2] These boundary conditions are derived from the continuity of the capacitor C charge and from the continuity of the inductor L flux, as it will be seen later.

$$\frac{\mathrm{d}^2 v_{C_{OFF}}(t)}{\mathrm{d}^2 t} + \frac{\mathrm{d}v_{C_{OFF}}(t)}{\mathrm{d}t}\left(\frac{\omega}{h} + \frac{\omega}{Q_L}\right) + v_{C_{OFF}}(t)\left(\omega^2 q^2 + \frac{\omega^2}{Q_L \cdot h}\right) = 0 \tag{B.17}$$

whose solution is given by

$$v_{C_{OFF}}(t) = K_{2,1} \cdot e^{A_{2,1} \cdot t} + K_{2,2} \cdot e^{A_{2,2} \cdot t} = K_{2,1} \cdot e^{a_{2,1} \cdot \omega t} + K_{2,2} \cdot e^{a_{2,2} \cdot \omega t} \tag{B.18}$$

where,

$$a_{2,1}, a_{2,2} = \frac{1}{2}\left[-\left(\frac{1}{h} + \frac{1}{Q_L}\right) \pm \sqrt{\left(\frac{1}{h} + \frac{1}{Q_L}\right)^2 - 4\left(q^2 + \frac{1}{Q_L \cdot h}\right)}\right] \tag{B.19}$$

B.3.2 Finding $K_{1,3}$–$K_{1,5}$ and $K_{2,3}$–$K_{2,5}$

The solution of the non-homogeneous differential equation given by eq. (B.6) is

$$v_{C_{ON}}(t) = K_{1,3} \cdot \sin(\omega t + \varphi) + K_{1,4} \cdot \cos(\omega t + \varphi) + K_{1,5} \tag{B.20}$$

whose K-constants were found as follows:

$$K_{1,3} = \frac{V_{DD} \cdot q^2 p}{\left(q^2 - 1 + \frac{1}{Q_L \cdot m}\right)^2 + \left(\frac{1}{m} + \frac{1}{Q_L}\right)^2}\left(\frac{q^2}{Q_L} + \frac{1}{{Q_L}^2 \cdot m} + \frac{1}{m}\right) \tag{B.21a}$$

$$K_{1,4} = \frac{V_{DD} \cdot q^2 p}{\left(q^2 - 1 + \frac{1}{Q_L \cdot m}\right)^2 + \left(\frac{1}{m} + \frac{1}{Q_L}\right)^2}\left(q^2 - 1 - \frac{1}{{Q_L}^2}\right) \tag{B.21b}$$

$$K_{1,5} = \frac{V_{DD} \cdot q^2}{\left(q^2 + \frac{1}{Q_L \cdot m}\right)} \tag{B.21c}$$

Similarly, the solution of the non-homogeneous differential equation given by eq. (B.10) is

$$v_{C_{OFF}}(t) = K_{2,3} \cdot \sin(\omega t + \varphi) + K_{2,4} \cdot \cos(\omega t + \varphi) + K_{2,5} \tag{B.22}$$

where,

$$K_{2,3} = \frac{V_{DD} \cdot q^2 p}{\left(q^2 - 1 + \frac{1}{Q_L \cdot h}\right)^2 + \left(\frac{1}{h} + \frac{1}{Q_L}\right)^2} \left(\frac{q^2}{Q_L} + \frac{1}{{Q_L}^2 \cdot h} + \frac{1}{h}\right) \tag{B.23a}$$

$$K_{2,4} = \frac{V_{DD} \cdot q^2 p}{\left(q^2 - 1 + \frac{1}{Q_L \cdot h}\right)^2 + \left(\frac{1}{h} + \frac{1}{Q_L}\right)^2} \left(q^2 - 1 - \frac{1}{{Q_L}^2}\right) \tag{B.23b}$$

$$K_{2,5} = \frac{V_{DD} \cdot q^2}{\left(q^2 + \frac{1}{Q_L \cdot h}\right)} \tag{B.23c}$$

B.3.3 Finding $K_{1,1}$, $K_{1,2}$ and $K_{2,1}$, $K_{2,2}$

In order to find the remaining four constants $K_{1,1}$, $K_{1,2}$, $K_{2,1}$, and $K_{2,2}$, four extra equations are needed. Those equations can be obtained from two boundary conditions at the switch turn-ON *or* turn-OFF moments along with the two Class-E switching conditions. Those boundary conditions come from fundamental properties: the continuity of electrical charge in capacitors and the continuity of magnetic flux in inductors.

The continuity of the electrical charge in the capacitor C at any switching moment, $t = \tau$, implies the continuity of the voltage across it, this is:

$$C = \frac{Q_C(t)}{v_C(t)} \tag{B.24a}$$

$$Q_C(\tau^-) = Q_C(\tau^+) \tag{B.24b}$$

$$v_C(\tau^-) \cdot C = v_C(\tau^+) \cdot C \tag{B.24c}$$

$$v_C(\tau^-) = v_C(\tau^+) \tag{B.24d}$$

The continuity of the magnetic flux in the inductor L at any switching moment implies the continuity of the current through it, this is:

$$L \propto \frac{\Phi_L(t)}{i_L(t)} \tag{B.25a}$$

$$\Phi_L(\tau^-) = \Phi_L(\tau^+) \tag{B.25b}$$

$$i_L(\tau^-) \cdot L = i_L(\tau^+) \cdot L \tag{B.25c}$$

$$i_L(\tau^-) = i_L(\tau^+) \tag{B.25d}$$

The switching moments are defined as follows, as seen in Fig. B.2: the turn-ON moment is defined at $0^- < t < 0^+$, or equivalently, $2\pi/\omega^- < t < 0^+$; while the turn-OFF moment is defined at $d \cdot \pi/\omega^- < t < d \cdot \pi/\omega^+$.

Applying eq. (B.24d) at the *turn-ON moment*, we get:

$$v_{C_{OFF}}(2\pi/\omega^-) = v_{C_{ON}}(0^+) \tag{B.26}$$

Eq. (B.25d) applied at the *turn-ON moment* yields

$$i_L(2\pi/\omega^-) = i_L(0^+) \tag{B.27a}$$

$$i_C(2\pi/\omega^-) + i_S(2\pi/\omega^-) - i_R(2\pi/\omega^-) = i_C(0^+) + i_S(0^+) - i_R(0^+) \tag{B.27b}$$

Since the load current $i_R(t)$ is continue by definition, we have that $i_R(2\pi/\omega^-) = i_R(0^+)$ and hence (using the current definitions in eq. (B.2)) eq. (B.27) gets to

$$i_C(2\pi/\omega^-) + i_S(2\pi/\omega^-) = i_C(0^+) + i_S(0^+) \tag{B.28a}$$

$$C\frac{\mathrm{d}v_{C_{OFF}}(2\pi/\omega^-)}{\mathrm{d}t} + \frac{v_{C_{OFF}}(2\pi/\omega^-)}{R_{OFF}} = C\frac{\mathrm{d}v_{C_{ON}}(0^+)}{\mathrm{d}t} + \frac{v_{C_{ON}}(0^+)}{R_{ON}} \tag{B.28b}$$

which can be re-arranged more conveniently as

$$\frac{\mathrm{d}v_{C_{OFF}}(2\pi/\omega^{-})}{\mathrm{d}t} + \frac{\omega}{h}v_{C_{OFF}}(2\pi/\omega^{-}) = \frac{\mathrm{d}v_{C_{ON}}(0^{+})}{\mathrm{d}t} + \frac{\omega}{m}v_{C_{ON}}(0^{+}) \tag{B.29}$$

Applying eq. (B.24d) at the *turn-OFF moment* gives

$$v_{C_{ON}}(d\cdot\pi/\omega^{-}) = v_{C_{OFF}}(d\cdot\pi/\omega^{+}) \tag{B.30}$$

Eq. (B.25d) applied at the *turn-OFF moment* yields

$$i_L(d\cdot\pi/\omega^{-}) = i_L(d\cdot\pi/\omega^{+}) \tag{B.31a}$$

$$i_C(d\cdot\pi/\omega^{-}) + i_S(d\cdot\pi/\omega^{-}) = i_C(d\cdot\pi/\omega^{+}) + i_S(d\cdot\pi/\omega^{+}) \tag{B.31b}$$

$$C\frac{\mathrm{d}v_{C_{ON}}(d\cdot\pi/\omega^{-})}{\mathrm{d}t} + \frac{v_{C_{ON}}(d\cdot\pi/\omega^{-})}{R_{ON}} = C\frac{\mathrm{d}v_{C_{OFF}}(d\cdot\pi/\omega^{+})}{\mathrm{d}t} + \frac{v_{C_{OFF}}(d\cdot\pi/\omega^{+})}{R_{OFF}} \tag{B.31c}$$

which can also be conveniently re-arranged into

$$\frac{\mathrm{d}v_{C_{ON}}(d\cdot\pi/\omega^{-})}{\mathrm{d}t} + \frac{\omega}{m}v_{C_{ON}}(d\cdot\pi/\omega^{-}) = \frac{\mathrm{d}v_{C_{OFF}}(d\cdot\pi/\omega^{+})}{\mathrm{d}t} + \frac{\omega}{h}v_{C_{OFF}}(d\cdot\pi/\omega^{+}) \tag{B.32}$$

Eqs. (B.26) & (B.29), and (B.30) & (B.32) are four equations derived from the boundary conditions. However, only a pair of them, along with the *Generalized Class-E Switching Conditions* to be introduced, is needed at this step for generating the necessary equations for finding the remaining $K_{1,1}$, $K_{1,2}$, $K_{2,1}$, and $K_{2,2}$ constants. For simplicity in this step, eqs. (B.26) & (B.29) will be the ones used in finding those constants. The other pair of boundary conditions, in eqs. (B.30) & (B.32), will be used in a later step.

The *Generalized Class-E Switching Conditions*, as seen in Fig. B.2, are:

$$v_C(t)\Big|_{t=\frac{2\pi}{\omega}} = \alpha\cdot V_{DD} \tag{B.33a}$$

$$\frac{\mathrm{d}v_C(t)}{\mathrm{d}t}\Big|_{t=\frac{2\pi}{\omega}} = k\cdot\omega\cdot V_{DD} \tag{B.33b}$$

where $\alpha \cdot V_{DD}$ is the capacitor C voltage at the moment the switch is turned-ON, and $k \cdot \omega \cdot V_{DD}$ is its slope. Notice that if both $\alpha = 0$ and $k = 0$, then eqs. (B.33a) & (B.33b) are the well-known *optimum Class-E switching conditions* [14, 16, 17]. Eq. (B.33a) for $\alpha \neq 0$ defines the so-called *Variable-Voltage Class-E mode* [18], denoted as Class-E_{VV}. Eq. (B.33b) for $k \neq 0$ defines the so-called *Variable-Slope Class-E mode* [19, 20], denoted as Class-E_{VS}. If $\alpha \neq 0$ or $k \neq 0$, then the Class E amplifier is operating in the so-called *suboptimum mode* [14]. The advantages that a given suboptimum mode can provide are discussed in Appendix C.

Directly from eqs. (B.33a) & (B.33b), we have that

$$v_{C_{OFF}}(2\pi/\omega) = \alpha \cdot V_{DD} \tag{B.34}$$

$$\frac{\mathrm{d}v_{C_{OFF}}(2\pi/\omega)}{\mathrm{d}t} = k \cdot \omega \cdot V_{DD} \tag{B.35}$$

form a 2 by 2 system of equations from which $K_{2,1}$ and $K_{2,2}$ can be obtained.

Using eq. (B.33a) and eq. (B.26) yields

$$v_{C_{ON}}(0) = \alpha \cdot V_{DD} \tag{B.36}$$

Employing eqs. (B.34), (B.35) and (B.36) into eq. (B.29) will lead to

$$\begin{aligned} \frac{\mathrm{d}v_{C_{ON}}(0)}{\mathrm{d}t} &= \frac{\mathrm{d}v_{C_{OFF}}(2\pi/\omega)}{\mathrm{d}t} + \frac{\omega}{h} v_{C_{OFF}}(2\pi/\omega) - \frac{\omega}{m} v_{C_{ON}}(0) \\ &= k \cdot \omega \cdot V_{DD} + \left(\frac{\omega}{h} - \frac{\omega}{m}\right) \alpha \cdot \ V_{DD} \end{aligned} \tag{B.37}$$

Eqs. (B.36) & (B.37) form another 2 by 2 system of equations from which $K_{1,1}$ and $K_{1,2}$ can be found.

Finally, by solving the above two system of equations, given by eqs. (B.36) & (B.37) and eqs. (B.34) & (B.35), the constants are found as shown next:

$$K_{1,1} = \frac{b_{1,2} - b_{1,1} \cdot a_{1,2}}{a_{1,1} - a_{1,2}} \tag{B.38a}$$

$$K_{1,2} = \frac{b_{1,1} \cdot a_{1,1} - b_{1,2}}{a_{1,1} - a_{1,2}} \tag{B.38b}$$

$$b_{1,1} = \alpha \cdot V_{DD} - K_{1,3} \cdot \sin(\varphi) - K_{1,4} \cdot \cos(\varphi) - K_{1,5} \tag{B.38c}$$

$$b_{1,2} = k \cdot V_{DD} + \alpha \cdot V_{DD} \cdot \left(\frac{1}{h} - \frac{1}{m}\right) - K_{1,3} \cdot \cos(\varphi) + K_{1,4} \cdot \sin(\varphi) \tag{B.38d}$$

$$K_{2,1} = e^{-a_{2,1} \cdot 2\pi} \left(\frac{b_{2,2} - b_{2,1} \cdot a_{2,2}}{a_{2,1} - a_{2,2}}\right) \tag{B.39a}$$

$$K_{2,2} = e^{-a_{2,2} \cdot 2\pi} \left(\frac{b_{2,1} \cdot a_{2,1} - b_{2,2}}{a_{2,1} - a_{2,2}}\right) \tag{B.39b}$$

$$b_{2,1} = \alpha \cdot V_{DD} - K_{2,3} \cdot \sin(\varphi) - K_{2,4} \cdot \cos(\varphi) - K_{2,5} \tag{B.39c}$$

$$b_{2,2} = k \cdot V_{DD} - K_{2,3} \cdot \cos(\varphi) + K_{2,4} \cdot \sin(\varphi) \tag{B.39d}$$

where $a_{1,1}$, $a_{1,2}$, $a_{2,1}$, and $a_{2,2}$ were given in eqs. (B.16) and (B.19), respectively.

B.3.4 Finding the unknown parameters

So far, the complete analytical solution for $v_C(t)$, eq. (B.11), in the Class E model has been completely determined in the former sections. However, it is given in terms of many parameters, some of them must be known *a priori* while others are a function of the first ones. The parameters that are a function of the other ones will be called 'unknown parameters'. From the discussion in section B.3.3, we must employ a couple of equations such that the complete model can be solved for *only two unknown parameters*. These equations are eqs. (B.30) & (B.32). Then, the selection of those two unknown parameters should be design-oriented. All the parameters have been classified for this purpose, as shown in Table B.2.

The technology and design related parameters are assumed to be known a priori[3]. The user defined parameters are also considered to be known, since they are chosen by the designer according to the specific behavior (s)he wants to obtain from his/her specific Class E design.

[3]Note that V_{DD} is selected as a function of the transistor's gate-drain breakdown voltage limit in order to maximize the amplifier output power without compromising its reliability.

Technology and design related	User defined	Unknowns
m, h	k	p
Q_L	α	φ
V_{DD}	d	
ω	q	

TABLE B.2: Classification of the parameters used in the general Class E model.

Appendix C discusses the implications in the amplifier performance as a function of those user-defined parameters, as well as the influence of the technology parameters.

Although the *two unknown parameters* can be any, the ones stated as such in Table B.2 make more sense for design purposes by allowing complete freedom in the selection of the amplifier behavior by selecting the other parameters. Therefore, the goal of this section is to find those unknown parameters as a function of the other parameters. Be aware that the design procedure of a Class E circuit is not interested in the specific value of p and φ, but rather in the *circuit elements* shown in figure B.1. Finding those circuit elements will be discussed in the next section.

In order to find p and φ as a function of the rest of the parameters, a 2 by 2 system of equations is generated by using eqs. (B.30) & (B.32). Those equations are repeated below for the reader's convenience,

$$v_{C_{ON}}(d \cdot \pi/\omega) = v_{C_{OFF}}(d \cdot \pi/\omega)$$
$$\frac{\mathrm{d}v_{C_{ON}}(d \cdot \pi/\omega)}{\mathrm{d}t} + \frac{\omega}{m} v_{C_{ON}}(d \cdot \pi/\omega) = \frac{\mathrm{d}v_{C_{OFF}}(d \cdot \pi/\omega)}{\mathrm{d}t} + \frac{\omega}{h} v_{C_{OFF}}(d \cdot \pi/\omega)$$

The analytical solution of that system of equations is left as an exercise for the curious reader. In this work, such a system is solved numerically[4].

B.4 Finding the Class E Circuit Elements

The link between the complex solution for the General Class E model, presented in sections B.2 and B.3, and the circuit elements of such an amplifier, as shown in Fig. B.1, is done through the so-called

[4]Other complex analytical expressions will be also computed numerically. The objective of this work is focused on the design implications of the Class-E model rather than in showing the beauty of the solution of such complex and long equations. Ultimately, all those equations are transcribed into a MATLAB-Maple code for their solution and visualization. Still, most of the equations are solved analytically and transcribed into that code.

$\mathbf{K_E}$
$K_L = \omega \cdot L/R_L$
$K_C = \omega \cdot C \cdot R_L$
$K_P = P_{out} \cdot R_L/{V_{DD}}^2$
$K_X = X/R_L$

TABLE B.3: Design Set $\mathbf{K_E}$.

Design Set $\mathbf{K_E}$ [17] shown in Table B.3. With the aid of this design set, a simple procedure for designing any kind of Class E amplifier can be followed, once the solution of the model is known (e.g. by graphical or numerical-tabular representations, etc.) for given specific input parameters (i.e. the ones in Table B.2). This procedure is explained in Appendix C. This section deals with the solution of each element in the design set $\mathbf{K_E}$ as well as the drain efficiency η.

$K_C()$ and $K_P()$ can be expressed as function of $K_L()$[5], using the definitions presented in Tables B.1 and B.3. This is,

$$K_C() = \omega \cdot C \cdot R_L = \frac{R_L}{\omega \cdot L \cdot q^2} = \frac{1}{q^2 \cdot K_L()} \tag{B.40}$$

$$\begin{aligned} K_P() &= \frac{P_{out} \cdot R}{{V_{DD}}^2} = \left(\frac{P_{out} \cdot R_L}{{I_R}^2}\right)\left(\frac{p^2}{\omega^2 \cdot L^2}\right) = \frac{1}{2}\left(\frac{R_L}{\omega \cdot L}\right)^2 p^2 \\ &= \frac{1}{2}\frac{p^2}{K_L()^2} \end{aligned} \tag{B.41}$$

The derivation of $K_L()$ follows from the principle of power conservation, i.e. all the dissipated power is described by the next equation:

$$P_{out} + P_{switch} + P_{Q_L} = P_{supply} \tag{B.42}$$

where, P_{out} is the power delivered to the load R_L, P_{switch} is the power dissipated in the finite switch resistances, P_{Q_L} is the power dissipated in the r_L resistor of the DC-feed inductor L, and P_{supply} is the power from the DC-supply.

The DC-supply power P_{supply} is equivalent to

[5]The symbol '()' after the elements in the design set $\mathbf{K_E}$ represents that they are functions of the parameters in Table B.1, except of V_{DD} (which for the model is just a scaling factor).

$$P_{supply} = I_0 \cdot V_{DD} \tag{B.43}$$

where the average supply current, I_0, is

$$\begin{aligned} I_0 &= \frac{\omega}{2\pi} \int_0^{2\cdot\pi/\omega} i_S(t)\,\mathrm{d}t \\ &= \frac{\omega}{2\pi}\left[\frac{1}{R_{ON}} \int_0^{d\cdot\pi/\omega} v_{C_{ON}}(t)\,\mathrm{d}t + \frac{1}{R_{OFF}} \int_{d\cdot\pi/\omega}^{2\pi/\omega} v_{C_{OFF}}(t)\,\mathrm{d}t\right] \end{aligned} \tag{B.44}$$

Then, eq. (B.43) can be re-arranged for later use as

$$P_{supply} = \frac{1}{2\pi \cdot L \cdot q^2}\left[\frac{V_{DD}}{m} \int_0^{d\cdot\pi/\omega} v_{C_{ON}}(t)\,\mathrm{d}t + \frac{V_{DD}}{h} \int_{d\cdot\pi/\omega}^{2\pi/\omega} v_{C_{OFF}}(t)\,\mathrm{d}t\right] \tag{B.45}$$

The power dissipated at the switch[6], P_{switch}, is given by

$$\begin{aligned} P_{switch} &= \frac{\omega}{2\pi}\left[\frac{1}{R_{ON}} \int_0^{d\cdot\pi/\omega} v_{C_{ON}}(t)^2\,\mathrm{d}t + \frac{1}{R_{OFF}} \int_{d\cdot\pi/\omega}^{2\pi/\omega} v_{C_{OFF}}(t)^2\,\mathrm{d}t\right] \\ &= \frac{1}{2\pi \cdot L \cdot q^2}\left[\frac{1}{m} \int_0^{d\cdot\pi/\omega} v_{C_{ON}}(t)^2\,\mathrm{d}t + \frac{1}{h} \int_{d\cdot\pi/\omega}^{2\pi/\omega} v_{C_{OFF}}(t)^2\,\mathrm{d}t\right] \end{aligned} \tag{B.46}$$

The power dissipated in the r_L resistor of the DC-feed inductor L is

$$\begin{aligned} P_{Q_L} &= \frac{\omega \cdot r_L}{2\pi} \int_0^{2\pi/\omega} i_L(t)^2\,\mathrm{d}t \\ &= \frac{L \cdot \omega^2}{Q_L \cdot 2\pi}\left[\int_0^{d\cdot\pi/\omega} i_{L_{ON}}(t)^2\,\mathrm{d}t + \int_{d\cdot\pi/\omega}^{2\pi/\omega} i_{L_{OFF}}(t)^2\,\mathrm{d}t\right] \end{aligned} \tag{B.47}$$

[6] P_{switch} includes any losses due to finite charge stored at the switch turn-on moment for the case that $\alpha \neq 0$.

In the above equation, $i_{L_{ON}}(t)$ and $i_{L_{ON}}(t)$ are, from eqs. (B.1) & (B.2),

$$i_{L_{ON}}(t) = C\frac{\mathrm{d}v_{C_{ON}}(t)}{\mathrm{d}t} + \frac{v_{C_{ON}}(t)}{R_{ON}} - I_R \sin(\omega t + \varphi) \tag{B.48a}$$

$$= \frac{1}{\omega^2 \cdot L \cdot q^2} x_{L_{ON}}(t) \tag{B.48b}$$

$$i_{L_{OFF}}(t) = C\frac{\mathrm{d}v_{C_{OFF}}(t)}{\mathrm{d}t} + \frac{v_{C_{OFF}}(t)}{R_{OFF}} - I_R \sin(\omega t + \varphi) \tag{B.48c}$$

$$= \frac{1}{\omega^2 \cdot L \cdot q^2} x_{L_{OFF}}(t) \tag{B.48d}$$

where,

$$x_{L_{ON}}(t) = \frac{\mathrm{d}v_{C_{ON}}(t)}{\mathrm{d}t} + \frac{\omega}{m} v_{C_{ON}}(t) - q^2 \cdot V_{DD} \cdot \omega \cdot p \cdot \sin(\omega t + \varphi) \tag{B.49a}$$

$$x_{L_{OFF}}(t) = \frac{\mathrm{d}v_{C_{OFF}}(t)}{\mathrm{d}t} + \frac{\omega}{h} v_{C_{OFF}}(t) - q^2 \cdot V_{DD} \cdot \omega \cdot p \cdot \sin(\omega t + \varphi) \tag{B.49b}$$

Then, eq. (B.47) can be expressed more conveniently as

$$P_{Q_L} = \left(\frac{1}{2\pi \cdot L \cdot q^2}\right)\left(\frac{1}{Q_L \cdot q^2 \cdot \omega^2}\right)\left\{\int_0^{d\cdot\pi/\omega} x_{L_{ON}}(t)^2 \,\mathrm{d}t + \int_{d\cdot\pi/\omega}^{2\pi/\omega} x_{L_{OFF}}(t)^2 \,\mathrm{d}t\right\} \tag{B.50}$$

The power delivered to the load, P_{out}, can be expressed as

$$\begin{aligned} P_{out} &= \left(\frac{I_R}{\sqrt{2}}\right)^2 R = \frac{I_R^2 \cdot R}{2} \\ &= \frac{p^2 \cdot V_{DD}^2}{2K_L() \cdot \omega \cdot L} \end{aligned} \tag{B.51}$$

From the last equation we have that, using eqs. (B.45), (B.46), and (B.50),

$$\begin{aligned} K_L() &= \frac{p^2 \cdot {V_{DD}}^2}{2 \cdot \omega \cdot L}\left(\frac{1}{P_{supply} - P_{switch} - P_{Q_L}}\right) \\ &= \frac{\pi \cdot (q \cdot p \cdot V_{DD})^2}{\omega}\left[\frac{1}{2\pi \cdot q^2 \cdot L \cdot \left(P_{supply} - P_{switch} - P_{Q_L}\right)}\right] \end{aligned} \tag{B.52}$$

where,

$$\left(2\pi \cdot q^2 \cdot L \cdot P_{supply}\right) = \frac{V_{DD}}{m}\int_0^{d\cdot\pi/\omega} v_{C_{ON}}(t)\,\mathrm{d}t + \frac{V_{DD}}{h}\int_{d\cdot\pi/\omega}^{2\pi/\omega} v_{C_{OFF}}(t)\,\mathrm{d}t \tag{B.53a}$$

$$\left(2\pi \cdot q^2 \cdot L \cdot P_{switch}\right) = \frac{1}{m}\int_0^{d\cdot\pi/\omega} v_{C_{ON}}(t)^2\,\mathrm{d}t + \frac{1}{h}\int_{d\cdot\pi/\omega}^{2\pi/\omega} v_{C_{OFF}}(t)^2\,\mathrm{d}t \tag{B.53b}$$

$$\left(2\pi \cdot q^2 \cdot L \cdot P_{Q_L}\right) = \left(\frac{1}{Q_L \cdot q^2 \cdot \omega^2}\right)\left[\int_0^{d\cdot\pi/\omega} x_{L_{ON}}(t)^2\,\mathrm{d}t + \int_{d\cdot\pi/\omega}^{2\pi/\omega} x_{L_{OFF}}(t)^2\,\mathrm{d}t\right] \tag{B.53c}$$

The design set element K_X can be found by using the amplitudes of two fundamental-frequency quadrature components of the voltage $v_C(t)$ across the switch, this is,

$$K_X() = \frac{V_X}{V_R} \tag{B.54}$$

where,

$$V_R = \frac{1}{\pi}\left[\int_0^{d\cdot\pi/\omega} v_{C_{ON}}(t)\sin(\omega t + \varphi)\,\mathrm{d}t + \int_{d\cdot\pi/\omega}^{2\pi/\omega} v_{C_{OFF}}(t)\sin(\omega t + \varphi)\,\mathrm{d}t\right] \tag{B.55a}$$

$$V_X = \frac{1}{\pi}\left[\int_0^{d\cdot\pi/\omega} v_{C_{ON}}(t)\cos(\omega t + \varphi)\,\mathrm{d}t + \int_{d\cdot\pi/\omega}^{2\pi/\omega} v_{C_{OFF}}(t)\cos(\omega t + \varphi)\,\mathrm{d}t\right] \tag{B.55b}$$

Finally, the drain efficiency η is given by

$$\begin{aligned}\eta() &= \frac{P_{out}}{P_{supply}} = 1 - \frac{P_{switch} + P_{Q_L}}{P_{supply}} \\ &= 1 - \frac{\left(2\pi \cdot q^2 \cdot L\right)\left[P_{switch} + P_{Q_L}\right]}{\left(2\pi \cdot q^2 \cdot L\right)\left[P_{supply}\right]}\end{aligned} \tag{B.56}$$

where eq. (B.53) can be used for convenience.

Appendix C

Analysis and discussion of the general Class E model

C.1 Introduction

The goal of the present appendix is to study the Class E circuit topology from a theoretical point of view, employing the model developed in Appendix B. Class E is well known for its high theoretical drain efficiency and simplicity but it could impose severe reliability concerns in practical implementations due to the high output swings for a given output power with respect to other amplifier classes. There is almost an infinity number of possibilities to design a Class E circuit [17]. However, the possibilities that a *general* Class E circuit has to offer are only starting to be recognized. For example, some authors [29] still employs the classical RF-choke Class E instead of exploiting the advantages of other versions of Class E (e.g. the Class E with parallel circuit [15] or a variable-voltage Class E [18]), as we will see in this appendix. For this reason it was decided to unify the latest and more generic Class E models available in literature towards a more comprehensible design tool for such circuits. This turned out in the generalized Class E model developed in Appendix B, whose results are discussed in this appendix. With this generalized model, we can: first, study the general Class E model and understand the inherent sources of efficiency loss; and second, find an optimum design approach to extract more output power with high efficiency and reliability.

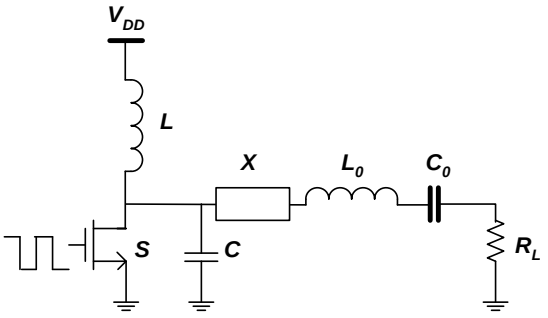


FIGURE C.1: Single-ended Class E circuit schematic.

C.2 Narrow-Band General Class E model

The Class-E concept was introduced in 1964 by G.D. Ewing [46]. Later, many works followed, presenting and analyzing the Class E power amplifiers. For example, some initial ones are [14, 16, 47] while many others are described in [17]. The common trend in most of these works is that they present only some characteristics of the Class E operation, while others are assumed ideal. For this work, an unified and general model for the Class E power amplifier is discussed, keeping a design perspective. The derivation of the model is based in the works of M. Acar in [17, 18, 20, 44, 45] and its derivation is presented in detail in Appendix B.

The Class E concept avoids the power dissipation of the shunt parasitic capacitance in the transistor switch at high frequencies by providing the so-called *soft switching condition* when turning it ON. This avoids the well-known $1/2 \cdot f \cdot C \cdot V^2$ power dissipation produced during a *hard switching condition* (i.e. turning the switch ON when it has finite voltage across its terminals). Although this idea can be applied in a variety of circuit topologies, the most common one is the single-ended common-source circuitry shown in figure C.1. The analytical model developed in Appendix B and the discussion presented in this appendix refers to that specific topology, but it could be extended to others.

In the class E power amplifier shown in fig. C.1, the transistor S is driven hard enough to act as a switch. The shunt capacitor C can be constituted by an external shunt capacitor and/or the internal switch transistor drain capacitance. The incorporation of the switch parasitic capacitance into the power amplifier itself is probably the most important feature of the Class E, since it enables its operation at high frequencies. In this work, C is considered to be implemented

completely by the switch parasitic capacitance[1]. The DC-feed inductor L was originally considered to be an RF-choke [14], and still many authors do [29, 48]. However using a finite inductor have several advantages, as studied by some authors already [45]. The circuit element X in fig. C.1 can be either an inductor, L_X, a capacitor, C_X, or even a short. The model in Appendix B considers also the losses due to finite values in the quality factor Q_L of the DC-feed inductor L.

The derivation of the general Class E model done in Appendix B makes the traditional assumption of having a sinusoidal waveform at the load R_L. This assumption of a high enough loaded quality factor Q_{L0} in the series filter L_0-C_0, simplifies the model derivation considerably and comes in line with the original idea for the Class E of being a *tuned power amplifier*. Due to this assumption, the model developed in Appendix B will be referred to as the 'General *Narrow-band* Class E model'. The loaded quality factor of L_0-C_0 can be reduced in a practical implementation to increase the bandwidth, but this will come at the cost of some efficiency loss (and the model will become less accurate).

C.2.1 Design of Class E power amplifiers

The Class E power amplifier is straight forward to design once its analytical model has been solved (refer to the Appendix B). The design procedure requires certain technology parameters as well as some user defined operating conditions as inputs (like operating frequency ω, optimum or suboptimum mode of operation, etc.). The outcome of the model is the so-called design set $\mathbf{K_E} = \{K_L, K_C, K_P, K_X\}$[2] [17] that relates the model solution to the circuit elements L (DC-feed inductor size), C (switch S size), X (reactive element X) as well as to the PA performance parameters, P_{out} and η. In theory, there is an infinite number of possible designs [17], however some of them are more convenient than others, as discussed in Appendix C.

There are two operating modes, whose original names are *optimum mode* and *suboptimum mode*

[1] The maximum transistor width minimizing the power loss due to finite R_{ON} is found when the C capacitance is entirely made of the transistor's drain capacitance, but at the cost of an increased driving input power [29] (since the gate capacitance scales directly with the transistor width).

[2] Where $K_L = \omega \cdot L/R_L$, $K_C = \omega \cdot C \cdot R_L$, $K_P = P_{out} \cdot R_L/{V_{DD}}^2$, and $K_X = X/R_L$.

[14]. Those operating modes are defined according to the *Generalized Class-E Switching Conditions*, which are:

$$v_C(t)\Big|_{t=\frac{2\pi}{\omega}} = \alpha \cdot V_{DD} \tag{C.1a}$$

$$\frac{\mathrm{d}v_C(t)}{\mathrm{d}t}\Big|_{t=\frac{2\pi}{\omega}} = k \cdot \omega \cdot V_{DD} \tag{C.1b}$$

where $\alpha \cdot V_{DD}$ is the capacitor C voltage at the moment the switch is turned-ON, and $k \cdot \omega \cdot V_{DD}$ is its slope. Notice that if both $\alpha = 0$ and $k = 0$, then eqs. (C.1a) & (C.1b) are the well-known *optimum* Class-E switching conditions [14, 16, 17]. Eq. (C.1a) for $\alpha \neq 0$ defines the so-called *Variable-Voltage* Class-E mode [18], denoted as Class-E_{VV}. Eq. (C.1b) for $k \neq 0$ defines the so-called *Variable-Slope* Class-E mode [19, 20], denoted as Class-E_{VS}. If $\alpha \neq 0$ or $k \neq 0$, then the Class E amplifier is operating in the *suboptimum mode*.

The design set elements $K_L = \omega L/R_L$ and $K_X = X/R_L$ are defined as the ratio of the impedance of the passive elements L and X, respectively, at the operating frequency ω with respect to the load R_L. $K_C = \omega C \cdot R_L$ is the inverse of such a ratio for the capacitor C. The element $K_P = P_{out} \cdot R_L/{V_{DD}}^2$ shows the output power that the amplifier can deliver as a function its supply voltage V_{DD} and load R_L[3]. [17]

The design set $\mathbf{K_E}$ is a function of many parameters, as shown in Table B.2 in Appendix B. Some of those parameters are also explained here for convenience. The parameter d determines the switching duty-cycle, since it is defined as duty-cycle = $d \cdot 50\%$. The parameter q can be seen as the ratio between the frequency ω_p of the parallel L-C tuned network (DC-feed inductor L and switch capacitance C) and the operating frequency ω, this is $q = \omega_p/\omega = \frac{1}{\omega\sqrt{LC}}$. The parameter m is defined as $m = \omega \cdot R_{ON} \cdot C$, where $R_{ON} \cdot C$ is defined by the technology employed[4] [45].

Figure C.2 shows the design set $\mathbf{K_E}$ and drain efficiency η for several values of m and q at 50% duty-cycle for the Class E *optimum mode* of operation. Note that $q \to 0$ represents the classical RF-choke Class E [14]. Similarly, other published Class E circuits can fit within the same model and can be expressed in terms of the design set $\mathbf{K_E}$ [17].

[3] The K_P factor for the most common gm-based PAs and other switchmode-based PAs was summarized in Tables 2.1 and 2.2 in Chapter 2.

[4] For example, in 65-nm CMOS, $m \approx 0.002$ for 1.2V thin-oxide NMOS and $m \approx 0.004$ for 2.5V thick-oxide NMOS at 1GHz. Note that those values are somehow optimistic since they were obtained from ideal models through simulation (not layout extracted views, or real measurements). Layouted devices will have bigger parasitic capacitances and hence m will increase in practice. See Appendix A for details about those devices in 65-nm CMOS.

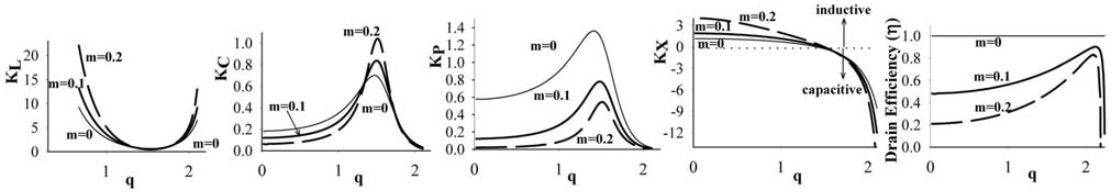


FIGURE C.2: Design Set $\mathbf{K_E}$ and drain efficiency η for Class E Optimum Mode, as a function of q for $m = 0, 0.1, 0.2$ and $d = 1$ (from [45]).

C.2.2 Discussion of the Class E model results

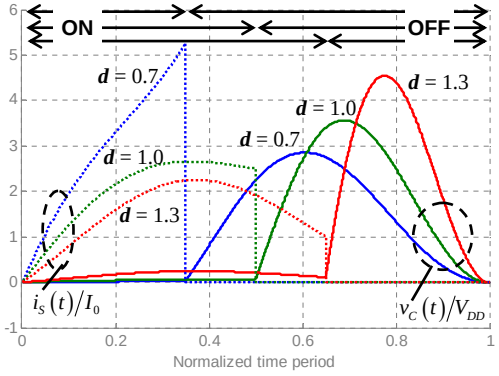
The developed model makes the design of any Class E a simple task. However, it requires the input of a given operating mode expressed in terms of α and k, besides the normal technology parameters. This is, the model in Appendix B finds the circuit elements of the class E for a given output voltage waveform in time domain, but it is still the task of the designer to tell the model *which* output waveform is (s)he looking for. For this reason it is important to have insights into those modes of operation. This is the goal of this section. The initial discussion will start with the *optimum* Class E mode. Later, the *suboptimum* modes will be addressed.

From the infinite number of possibilities, all the parameters have been reduced to practical ranges to extract useful conclusions from the model. Also, some parameters like m, d and Q_L have been considered with only a reduced number of values with the purpose of have an overview of their influence in the design[5]. Q_L has been considered for the ideal case of a loss-less DC-inductor ($Q_L \to \infty$), a bondwire inductor ($Q_L \approx 30$) and a CMOS integrated inductor ($Q_L \approx 10$). The duty-cycle has been considered as 35% ($d = 0.7$), 50% ($d = 1.0$) and 65% ($d = 1.3$). The employed values of m try to represent state of the art CMOS transistors operating up to around 10 GHz[6]. Also, the value of q has been restricted to avoid extreme current and voltage waveforms [17] and hence useless designs. It was observed that the range of q is related to the duty-cycle. Therefore, the following ranges were finally chosen: $0 < q < 1.8$ for $d = 0.7$, $0 < q < 2.0$ for $d = 1.0$, and $0 < q < 2.5$ for $d = 1.3$.

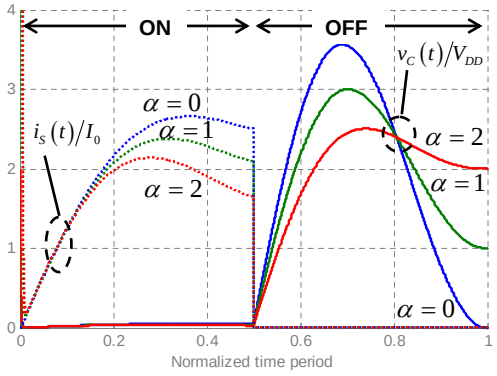
An important observation is that for the mathematical model, the switch is a simple two-state resistor: an R_{ON} resistor for the ON-state and an R_{OFF} resistor for the OFF-state. A *transistor* switch can be modeled as a two-state resistor for most of the practical cases. However, a

[5]For a practical design requiring specific values of any of those parameters, then the full analytical model in Appendix B should be used.

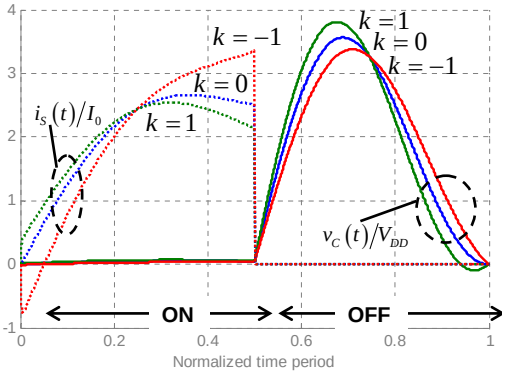
[6]For example: $m \approx 0.002$ and $m \approx 0.004$ for standard thin- and thick-oxide NMOS, and $m \approx 0.01$ and $m \approx 0.005$ for thin- and thick-oxide extended-drain NMOS transistors in 65-nm CMOS at 1GHz. Note that this values are approximate and somehow optimistic (see Appendix A for details.



(a) Optimum Class E I & V waveforms at different duty-cycles



(b) Class E_{VV} I & V waveforms



(c) Class E_{VS} I & V waveforms

FIGURE C.3: Class E power amplifier typical current and voltage waveforms (normalized with respect to the average supply current and DC-supply voltage, respectively) for a) optimum mode at different duty-cycles, b) variable-voltage, and c) variable-slope.

MOS transistor has other properties that are not taken into account in this simple mathematical model. One important example is that the output voltage cannot swing to negative values during the OFF-state in a transistor switch (because the parasitic drain to substrate diode will get forward biased) while this is possible for the mathematical model. Therefore, it is important to be aware that some extreme results from the model could not be physically possible in practice. Fortunately, this only happens in very exotic conditions out of the normal parameter ranges.

Figure C.3 shows several typical current and voltage waveforms for the optimum and suboptimum modes of the Class E power amplifier. Fig. C.3(a) shows the current and voltage (I & V) waveforms for optimum mode at several duty-cycles (35%, 50%, and 65%). Fig. C.3(b) shows the I & V waveforms for different variable-voltage Class E amplifiers. Fig. C.3(c) shows the I & V waveforms for different variable-slope Class E amplifiers. Simultaneous variable-voltage and

variable-slope is also possible. In the next section the optimum and suboptimum modes will be discussed.

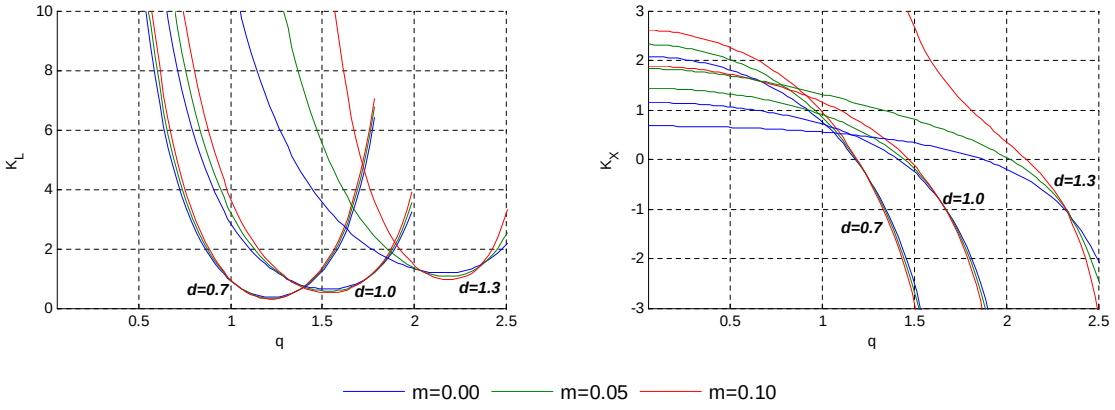
C.2.2.1 Class E in optimum mode

Figures C.4 and C.5 show the complete design set $\mathbf{K_E}$ for Class E in Optimum Mode as a function of q with 35%, 50% and 65% of duty-cycle (d=0.7, 1.0, 1.3) for several values of m and Q_L.

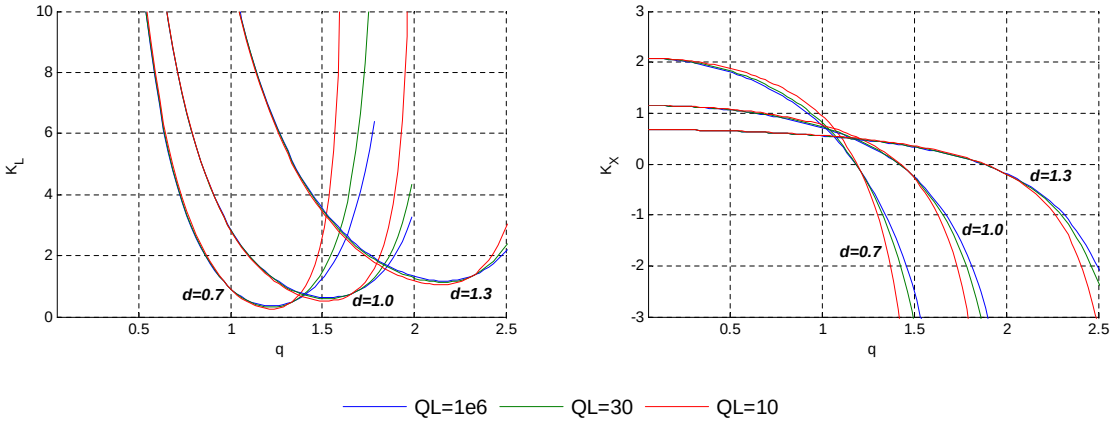
The first important observation is that K_X can be zero at specific q values. This observation was first made in [15], and the resulting circuit topology was called *Class E with parallel circuit*. However, in [15] the condition $K_X = 0$ is derived only for 50% duty-cycle and an ideal switch, while in this work this condition is found for the general case, for optimum and suboptimum conditions. The q values at which $K_X = 0$ are observed to be mainly a function of the duty-cycle. The higher the duty-cycle, the higher the value of q to get $K_X = 0$. Having a null K_X implies that the reactive element X is not needed for the Class E amplifier. This has immediate advantages: simplier circuitry, not practical losses associated to that element and, most importantly, higher output power. In fact, the output power peaks at this particular condition, i.e. at the q for which $K_X = 0$. This is due to the fact that P_{out} is proportional to the (square of) load voltage swing and if $K_X \neq 0$ there would be a lossless voltage division that would limit P_{out} for reaching its maximum. The conditions for having the maximum levels for P_{out} can be observed in the plots for K_P in figure C.5. As a comparison, $K_P = 0.5768$ for the lossless RF-choke Class E [14] (observed in Fig. C.5(a) at $q = 0$ for $d = 1.0$ and $m = 0$) while $K_P = 1.365$ [15] for the parallel circuit Class E with finite inductor (which can be observed in the same figure at $q \approx 1.41$ for $d = 1.0$ and $m = 0$). Also, notice that from the figure C.5, K_P is further increased for a higher duty-cycle. However, this last observation could be missleading since a higher duty-cycle comes along with higher peak voltages (as observed in the plot of the normalized peak switch voltages, in Fig. C.7) and therefore the same supply voltage could not be used due to reliability concerns. In order to solve the last problem a comparative parameter called κ_P will be used[7].

Another observation is that higher duty-cycle values *shift* the entire design set towards higher values of q (or to the right in the figures C.4 and C.5). Note that both the duty-cycle (indicated by d) and q are inversely proportional to the operating frequency ω. This would imply that the duty-cycle could modify the performance of a fixed Class E amplifier designed at frequency ω_0

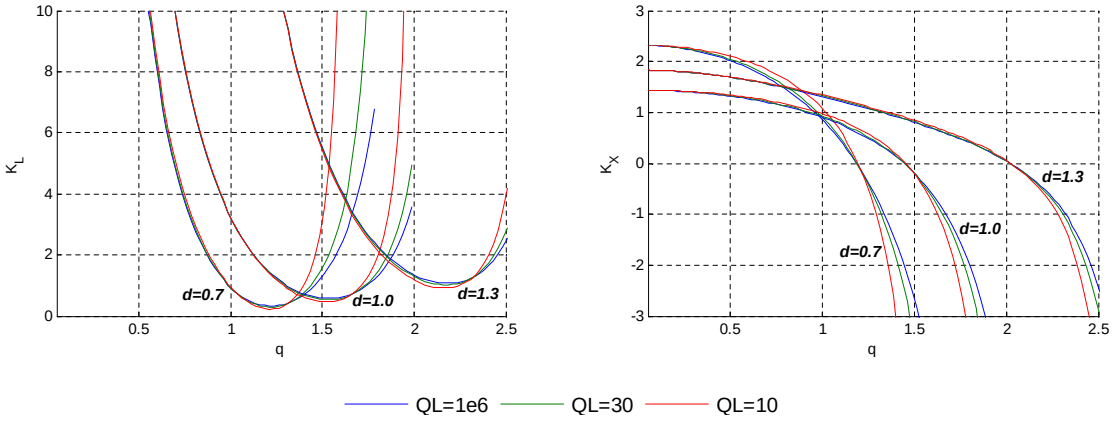
[7] This κ_P parameter was already employed in Chapter 2 for other gm- and switchmode-based PAs.



(a) several values of m.

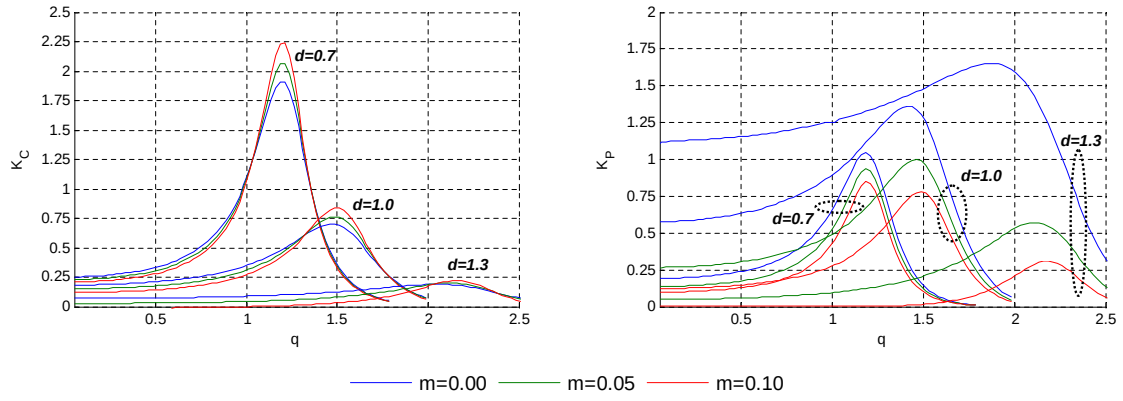


(b) several values of Q_L

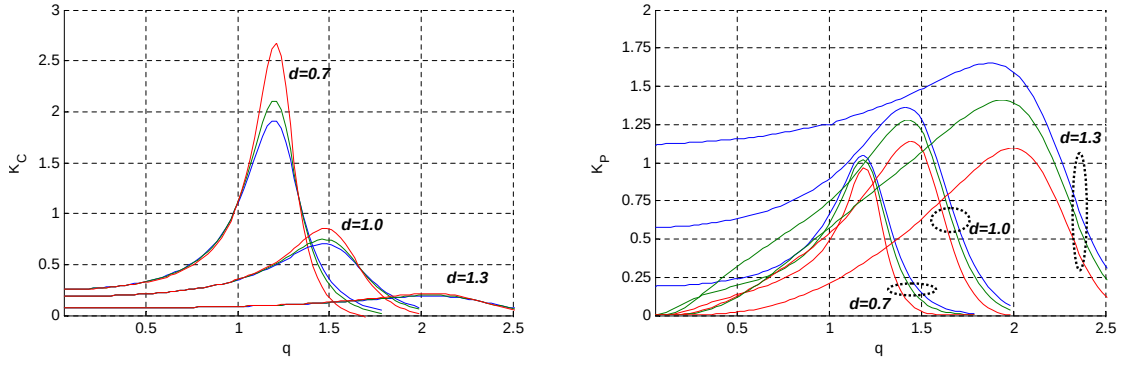


(c) finite $m = 0.05$ and several values of Q_L

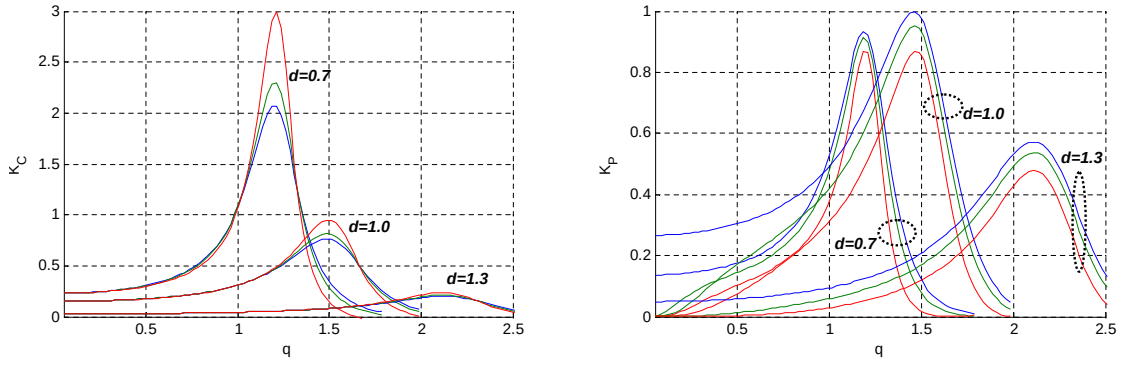
FIGURE C.4: K_L and K_X for Class E in Optimum Mode as a function of q with 35%, 50% and 65% of duty-cycle (d=0.7, 1.0, 1.3), for a) several values of m (Q_L ideal), b) several values of Q_L (m ideal), c) finite $m = 0.05$ and several values of Q_L.



(a) several values of m.



(b) several values of Q_L



(c) finite m = 0.05 and several values of Q_L

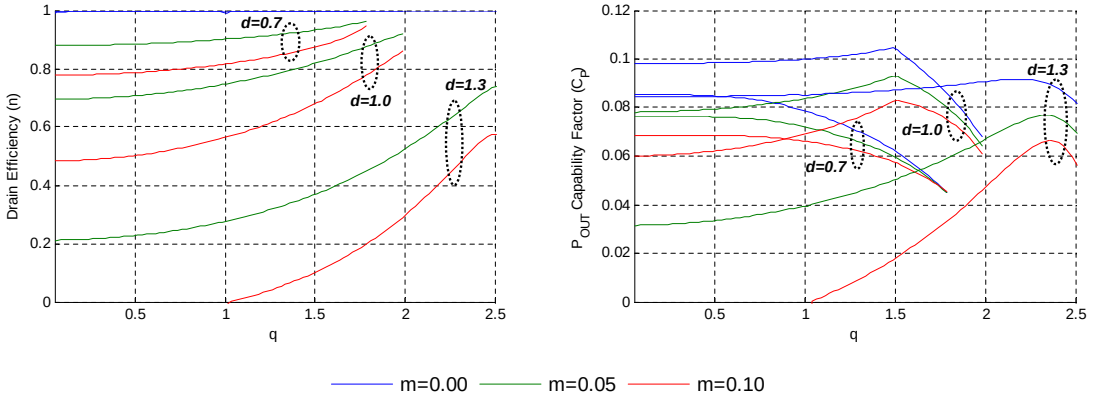
FIGURE C.5: K_C and K_P for Class E in Optimum Mode as a function of q with 35%, 50% and 65% of duty-cycle (d=0.7, 1.0, 1.3), for a) several values of m (Q_L ideal), b) several values of Q_L (m ideal), c) finite m = 0.05 and several values of Q_L.

operating at different frequencies. However, the implications of this 'shift to the right' are not simple to extract since the parameters of the entire design set $\mathbf{K_E}$ also change for different duty-cycles, and different design set $\mathbf{K_E}$ means different hardware designs. Although the theoretical design procedure is ultimately based in getting an specific time-domain voltage waveform, this could not be completely necessary for a practical Class E circuit trying to make use of this duty-cycle property for modifying its performance. Further details of this interesting observation are out of the scope of the present work, and hence they will not be deeply explored here. At the end of this Appendix, an experiment is shown that demonstrate the effects of duty-cycle control on the performance of a broadband Class E PA.

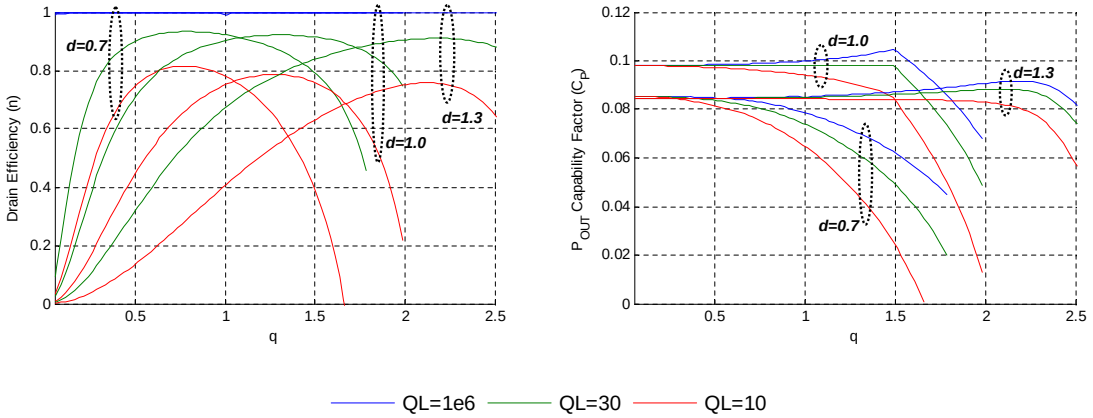
The values for K_L and K_C also peak at values of q very close to the ones that make K_P to peak. At the vicinity of the peak output power (i.e. when K_P peaks), K_L is at its minimum value having some design consequences. The DC-feed inductor could be small enough to be implemented using a bondwire, with the advantage of a higher quality factor, but it could also be so small to be hardly realizable in practice. Also, K_C is at its maximum value at the same vicinity, implying a bigger transistor and hence a lower ON-resistance.

Figure C.6 shows the drain efficiency, η, and the output power capability, C_P, for Class E in Optimum Mode as a function of q with 35%, 50% and 65% of duty-cycle for several values of m and Q_L. As expected, finite values of $m = \omega \cdot R_{ON} \cdot C$ and $Q_L = \omega \cdot L/r_L$ lower the maximum achievable drain efficiency as they increase. Observe in the same figure that the drain efficiency is higher for lower duty-cycles for the same finite values of m. This can be explained by observing that K_C, in figure C.5, is bigger for smaller duty-cycles (e.g. $d = 0.7$) which corresponds to larger transistor widths and hence smaller R_{ON}, so for a fixed load R_L the drain efficiency is increased. The efficiency losses due to the transistor switch is technology and frequency dependent, and it is characterized with the parameter m[8] [45]. The use of a bondwire ($Q_L \approx 30$) will cause an efficiency loss of less than 10% while this loss would be around 20% (or more) for an integrated inductor with $Q_L \approx 10$. Consider also that in a practical design both effects, finite m and finite Q_L, will be present. An example of the effect of having simultaneously both sources of power loss can be observed in figures C.4 and C.5 for the design set $\mathbf{K_E}$ and in figure C.6 for the drain efficiency and the output power capability. The finite values of m and Q_L also affects the output power levels, as seen in figure C.5.

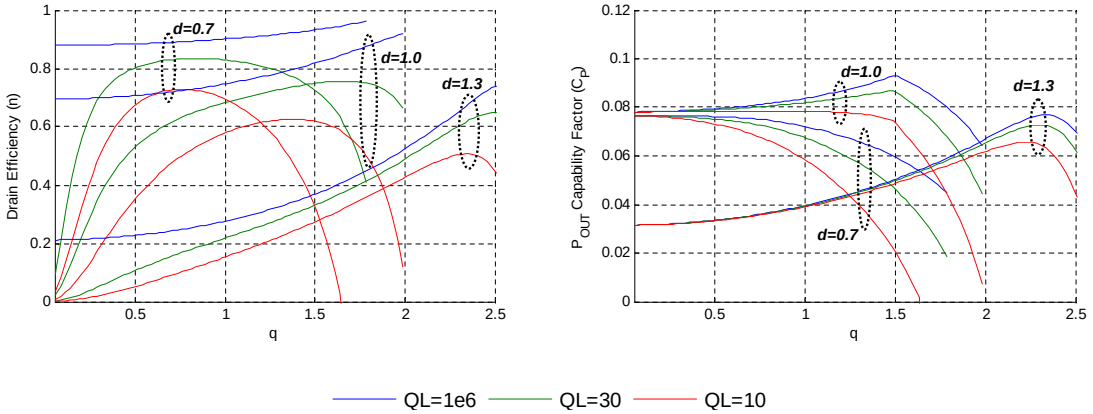
[8]Observe that larger m will represent either a technology with worst performance or the same device used in at a higher frequency.



(a) several values of m.

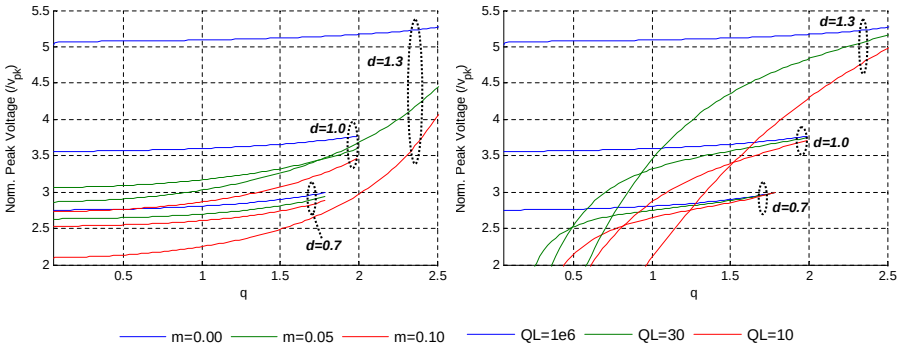


(b) several values of Q_L



(c) finite m = 0.05 and several values of Q_L

FIGURE C.6: Drain efficiency, η, and output power capability, C_P, for Class E in Optimum Mode as a function of q with 35%, 50% and 65% of duty-cycle (d=0.7, 1.0, 1.3), for a) several values of m (Q_L ideal), b) several values of Q_L (m ideal), c) finite m = 0.05 and several values of Q_L.



(a) several values of m (b) several values of Q_L

FIGURE C.7: Normalized peak switch voltage, $\overline{v_{pk}}$, for Class E in Optimum Mode as a function of q with 35%, 50% and 65% of duty-cycle (d=0.7, 1.0, 1.3), for a) several values of m (Q_L ideal), b) several values of Q_L (m ideal).

The higher values of K_P for $d = 1.3$ in figure C.5 could be misleading, as stated before, if the equivalent plots for C_P were not available. C_P normalizes the maximum output power with respect to the peak switch voltage and current. In CMOS, the reliability of switchmode PAs is more concerned with the limited breakdown voltage capabilities than with the maximum currents, as they scale directly with the number of parallel instances used to constitute the switching devices [8], while the limited voltage does not[9]. For this reason, a couple of additional parameters will be (re-)introduced in order to be able to fairly compare the capabilities of different Class E modes with other power amplifiers. The idea of using *normalizing parameters* is not new as it already exists in the output power capability factor, for example. C_P includes both the peak voltage and the peak current values, which can be appropriate for evaluating the stress of the device in transconductance-based power amplifiers and switchmode-based amplifiers in optimum mode. However, in switching amplifiers working in suboptimum modes with $\alpha \neq 0$ (i.e. variable-voltage mode), this is an issue since narrow and large current spikes are predicted in theory (in variable-voltage mode the switch is turned ON when there is a finite voltage across it) and then $C_P \rightarrow 0$, leading to no useful information about the output power capabilities of such amplifiers with respect to their stress.

The first parameter (re-)introduced is called κ_P, and it is similar to K_P. However, K_P does not state anything about the reliability of the PAs, as C_P does for example. K_P only states how much P_{out} will be generated from a given supply voltage, regardless of whether or not the voltage swing due to that supply voltage can be supported by the transistor in the PA. This is an important consideration, since in Class E the transistor output voltage will have different peak

[9]The maximum voltage swing can be extended by employing a number of techniques, from which *cascoding* is probably the most common one. Cascoding is discussed in Chapter 3 to achieve higher voltage swings.

voltages of several times the supply voltage according to its mode of operation and its specific operating conditions, as observed in Fig. C.3. This means that for a maximum output power within reliable voltage limits, the supply voltage must be scaled down (or up) appropriately. In other classes of amplifiers the switch voltage will peak with a different factor with respect to the supply (e.g. this factor will be 1 in a Class D(E) and 2 for a Class B). Figure C.7 shows the normalized peak voltage, $\overline{v_{pk}} = v_{DS}/V_{DD}$ (v_{DS} is the drain–source voltage in the case of a CMOS implementation), at the switch with respect to the supply voltage for Class E in optimum mode as a function of q for different values of d, m and Q_L. Note in that figure that the peak voltages for $d = 1.3$ are more than 5 times the supply voltage, which could severely compromise the reliability of the switching device. For $d = 0.7$, the peak voltages are smaller but also the maximum K_P and C_P are reduced.

For the last reasons, the maximum output power level can be normalized with respect to the *maximum reliable supply voltage*, that will be called $V_{DD,max}$, for a given load. This normalization will be done through the parameter κ_P. The κ_P factor will be defined from

$$P_{out,max} = \kappa_P \cdot \frac{{V_{DD,max}}^2}{R_L} \tag{C.2a}$$

(C.2b)

Then, κ_P states the maximum output power $P_{out,max}$ obtainable with a supply voltage $V_{DD,max} = v_{DS,max}/\overline{v_{pk}}$ that always ensure a reliable voltage operation of the transistor in the PA[10]. Observe that both K_P and κ_P are directly related, through $\kappa_P = K_P/\overline{v_{pk}}^2$.

Due to the same observation of the current spikes in suboptimum modes, a second normalizing parameter will be introduced to support fair comparisons between different classes of amplifiers and modes of operation. This parameter will be an alternative output power capability factor, C_{P2}, given as

$$C_{P2} = \frac{P_{o,max}}{v_{DS,max} \cdot i_{DS,avg}} \tag{C.3}$$

[10]For example, let us assume that we have NMOS and PMOS transistors with a breakdown voltage of 1V. If an ideal and optimum Class E is built with one of those NMOS, then $V_{DD,max} \approx 0.28V$ since $\overline{v_{pk}} \approx 3.56$. If a CMOS inverter or a Class D(E) amplifier was built, then $V_{DD,max} \approx 1V$ since $\overline{v_{pk}} \approx 1$. With this example, the usefulness of κ_P over K_P for the comparison of the reliable maximum output power level for the same technology in different circuit classes can be appreciated. This is because it is enough to know the κ_P value to make a direct comparison between the two classes of amplifiers (otherwise, for doing the same with K_P, $\overline{v_{pk}}$ must be known as well).

where the only difference with C_P is that the average of the current $i_{DS}(t)$ is taken instead of its peak. This standard average in the current waveform will prevent the current spikes from giving a rather low C_P that otherwise could become meaningless. Averaging the switch current will permit the current spikes to be taken into account in C_{P2}, as their value will be seen in the final average (very narrow pulses will not modify the final average, while less narrow pulses will do). The peak voltage information is preserved in C_{P2} to consider the breakdown voltage reliability concerns[11].

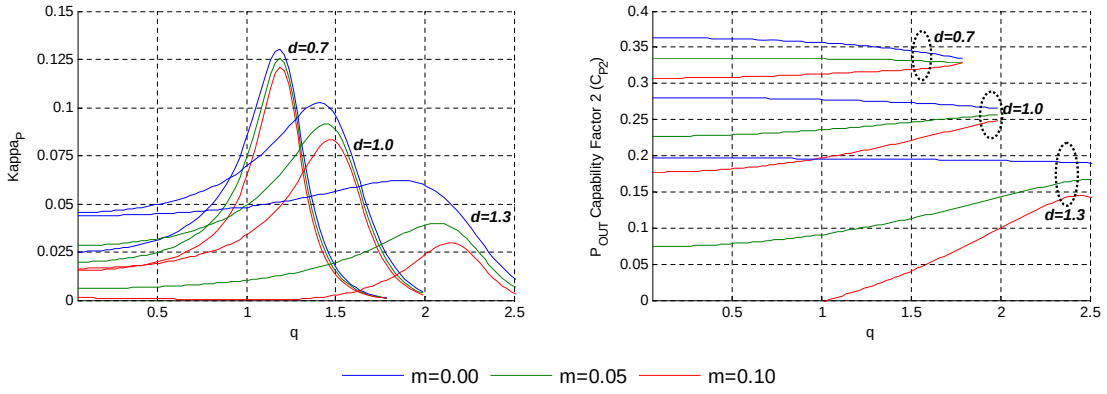
Figure C.8 shows κ_P and C_{P2} for the Class E in optimum mode as a function of q with 35%, 50% and 65% of duty-cycle for several values of m and Q_L. Note that from this perspective, the maximum *reliable* output power will happen at a smaller duty-cycle. The output power at $d = 0.7$ will be 27% larger than at $d = 1.0$ if the transistor is supplied with a voltage such that in both cases the output swing at its terminals uses all the reliability capabilities of the transistor (same reliable voltage level, but different supply voltages). This is an important statement that requires a detailed explanation. For an ideal Class E working in optimum mode, $K_P = 1.046$ at $q = 1.181$ and $K_P = 1.362$ at $q = 1.412$, for $d = 0.7$ and $d = 1.0$ respectivelly (see Fig. C.5(a) for $m = 0$). At those conditions, the normalized peak voltage is different, as seen in figure C.7(a); $\overline{v_{pk}} = 2.832$ and $\overline{v_{pk}} = 3.646$, for $d = 0.7$ and $d = 1.0$ respectivelly. Then, $V_{DD,max}$ can be $\approx 29\%$ larger for $d = 0.7$ than for $d = 1.0$. Therefore, the maximum output for $d = 0.7$ will be $\approx \frac{1.046(1.287)^2}{1.362} = 1.27$ larger than the one for $d = 1.0$. This factor can be equivalently found by the ratio of $\kappa_P|_{q=1.18,d=0.7} = 0.131$ to $\kappa_P|_{q=1.41,d=1.0} = 0.103$, both seen in figure C.8.

C.2.2.2 Class E in suboptimum mode

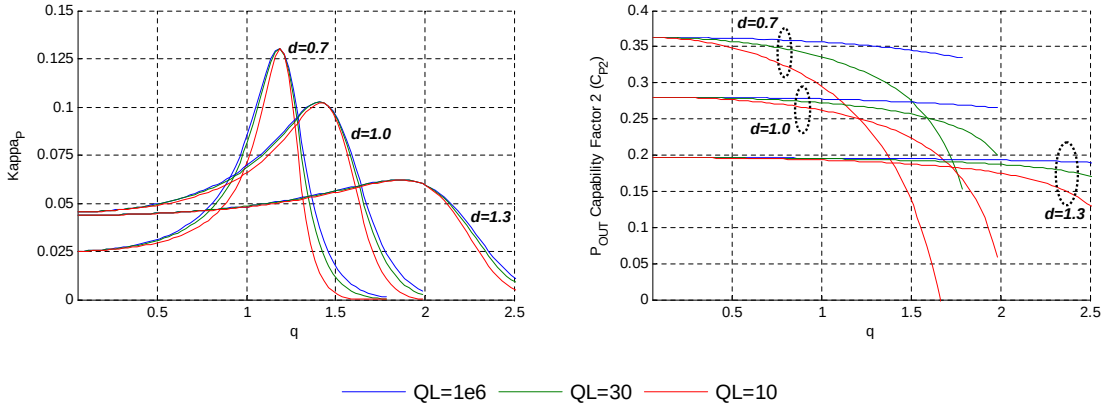
For each of the suboptimum modes, determined by the values of α and k, similar plots to the ones in the last section can be generated. The characteristic condition for which $K_X = 0$ has been chosen to analyze the properties of the variable-voltage [18] and variable-slope [20] Class E amplifiers, due to the peaking of the output power levels.

Figure C.9 shows the main parameters for the variable-voltage Class E, given as a function of α (remember that $\alpha \cdot V_{DD}$ is the capacitor voltage at the moment the switch is turned-ON). The left side of Fig. C.9(a) shows the values of q for which $K_X = 0$ at each α, while in the right side it can be seen how the peak voltage is indeed reduced for increased α values, as it can also be

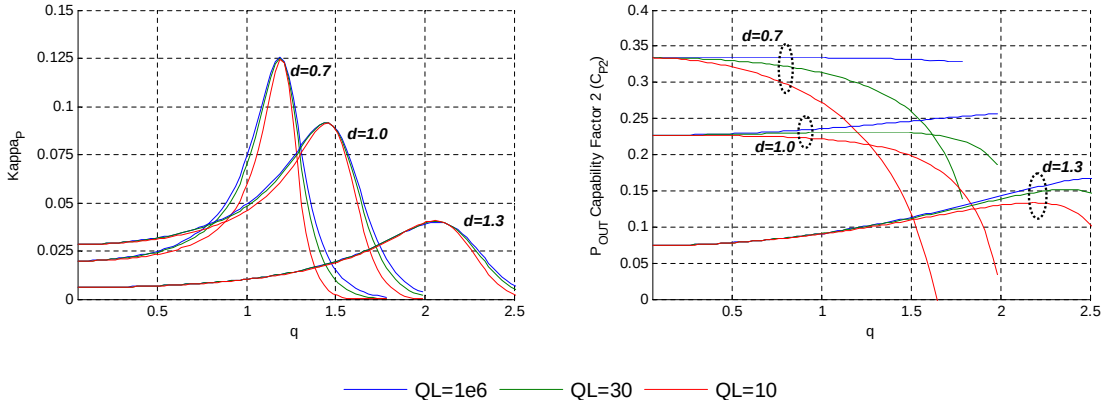
[11] It is still not unanimously recognized the RF oxide breakdown limits [29] and it is customary to employ instantaneous peak voltage levels to asset the reliability of an amplifier.



(a) several values of m.



(b) several values of Q_L



(c) finite $m = 0.05$ and several values of Q_L

FIGURE C.8: κ_P and the alternative output power capability factor, C_{P2}, for Class E in optimum mode as a function of q with 35%, 50% and 65% of duty-cycle (d=0.7, 1.0, 1.3), for a) several values of m (Q_L ideal), b) several values of Q_L (m ideal), c) finite $m = 0.05$ and several values of Q_L.

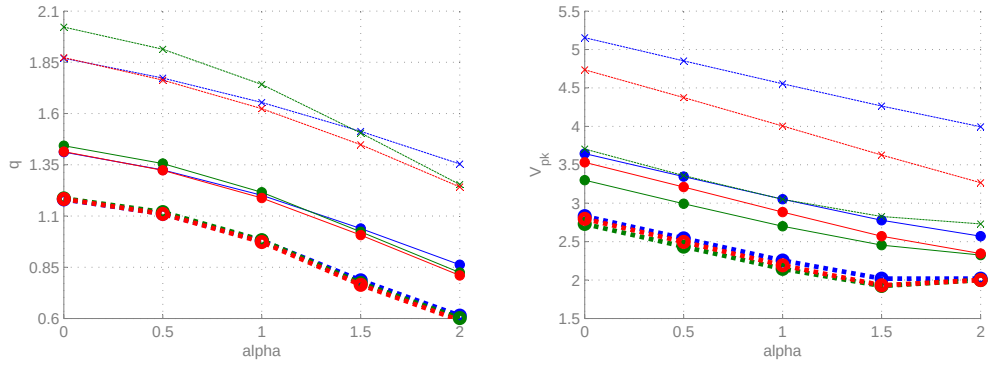
observed in the voltage waveforms of Fig. C.3(b). Fig. C.9(b) shows in its left-hand side the drain efficiency at different values of α; as expected, larger values of α causes larger efficiency losses due to the ON switching losses. The right-hand side of Fig. C.9(b) shows the values of κ_P. Observe that κ_P increases with α and that η does not drop very rapidly for up to around $\alpha = 1$, implying that more output power can be extracted in variable-voltage Class E traded-off with a small loss in drain efficiency (as stated in [18]). Also notice that the sensitivity for the efficiency losses, as well as the values of κ_P, for increasing values of α are a function of the duty-cycle. For example, at 50% duty-cycle and an ideal switch, going to $\alpha = 1$ will increase κ_P by +19% while η will drop less than 4% points. If the switch has a finite $m = 0.05$, then κ_P will increase by +17% for only a loss of 2% in drain efficiency. Similar conclusions can be drawn for a finite quality factor in the DC-feed inductor. A higher value of α will increase further κ_P at the cost of a higher loss in η. Finally, Fig. C.9(c) shows the alternative output power capability factor and K_P for completeness.

The variable-slope Class E has the advantage of allowing higher switch sizes (i.e. higher K_C) with the benefit of increased drain efficiency for negative slopes (i.e. $k < 0$) [20]. Figure C.10(a) shows the values of q that make $K_X = 0$ and the normalized peak voltages $\overline{v_{pk}}$ as a function of k, for an ideal switch and a switch with finite ON-resistance. Figure C.10(b) shows the η and κ_P for the same values of k. Observe that going to positive values of k does not seem to be attractive, since it increases the peak voltages and reduces the maximum output power, as observed in Fig. C.10. In the other hand, negative values of k do fortunately the opposite, smaller $\overline{v_{pk}}$ and increased values of κ_P, while the drain efficiency is improved. Fig. C.10(c) shows the alternative output power capability factor and K_P for completeness.

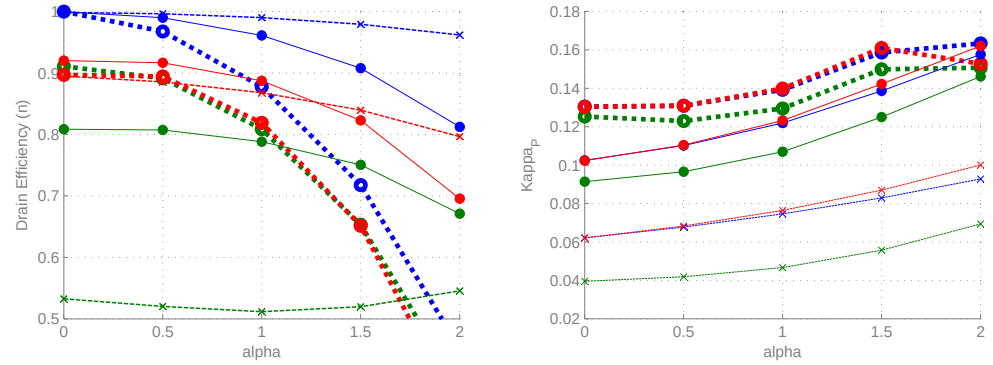
C.2.3 Conclusions

The Class E with parallel circuit topology [15] provides the maximum output power. That specific topology makes $X = 0$, and hence the Class E circuitry is further simplified. This Class E with parallel circuit can be freely designed at any operating mode (and duty-cycle), as demonstrated in Appendix C. This topology will be the one employed in rest of this work.

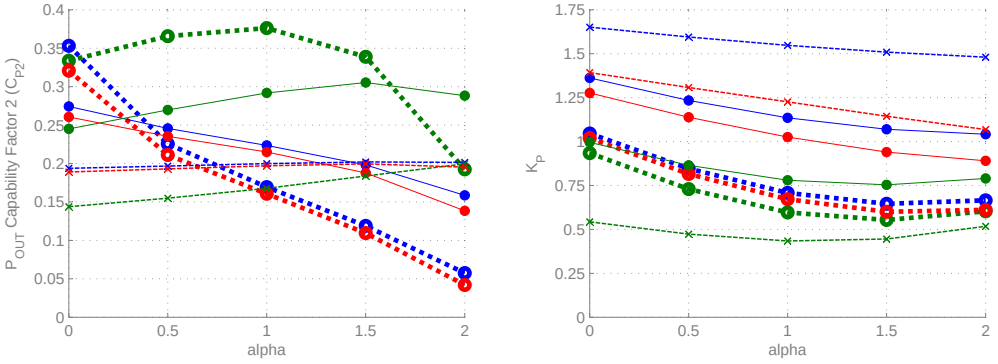
Designing a Class E circuit in suboptimum mode (variable-voltage and variable-slope) has advantages. Allowing a finite voltage up to approximately the supply voltage (i.e. $\alpha = 1$) at the turn-ON moment reduces the peak voltage of the Class E circuit significantly. This allows an increase in the maximum output power with a very small drop in drain efficiency [18]. Also,



(a) q and $\overline{v_{pk}}$.



(b) η and κ_P.



(c) C_{P2} and K_P.

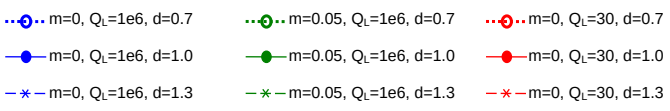
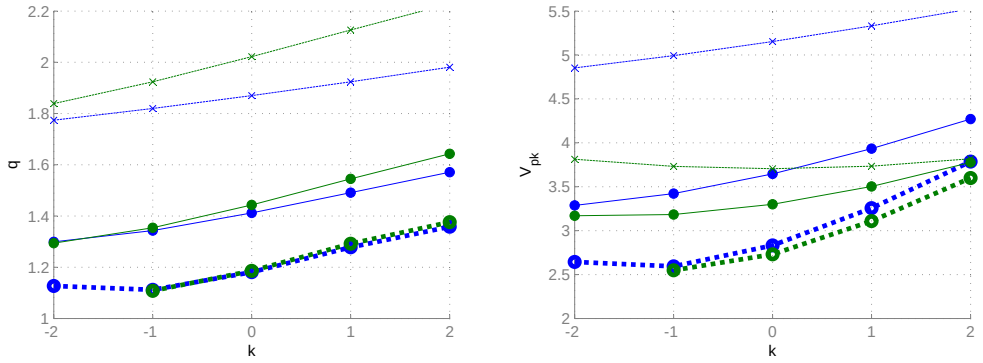
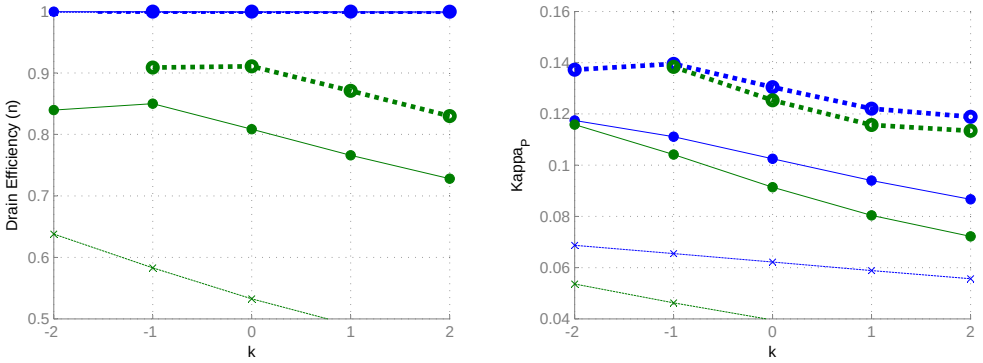


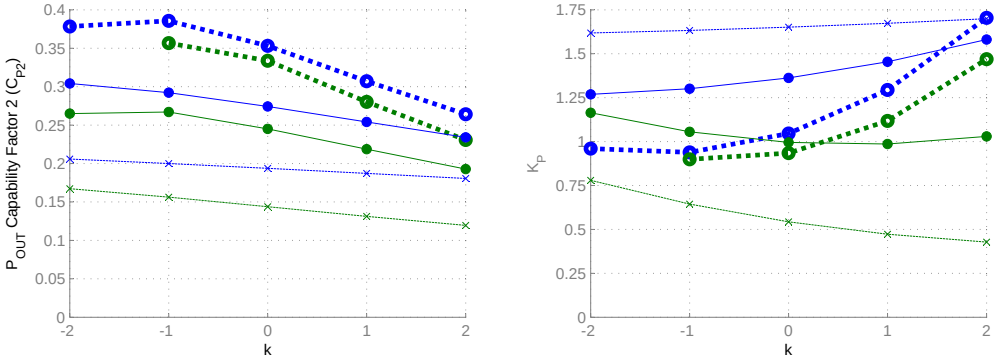
FIGURE C.9: Properties for Variable-Voltage Class E as a function of α with 35%, 50% and 65% of duty-cycle (d=0.7, 1.0, 1.3) for the ideal case ($m = 0$ and $Q_L = \infty$), finite m ($m = 0.05$ and $Q_L = \infty$) and finite Q_L ($m = 0$ and $Q_L = 30$).



(a) q and $\overline{v_{pk}}$.



(b) η and κ_P.



(c) C_{P2} and K_P.

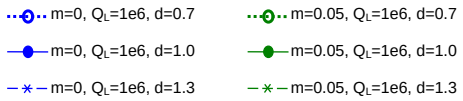


FIGURE C.10: Properties for Variable-Slope Class E as a function of k with 35%, 50% and 65% of duty-cycle (d=0.7, 1.0, 1.3) for the ideal case ($m = 0$ and $Q_L = \infty$), and for finite m ($m = 0.05$ and $Q_L = \infty$).

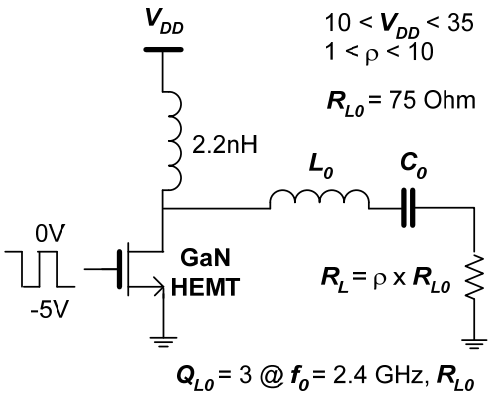


FIGURE C.11: Schematic for the broadband Class E amplifier designed with a GaN HEMT transistor.

negative slopes of the voltage during the turn-ON moment contributes to reduce the peak voltage and increase the maximum output power [20]. Interestingly, both variable-voltage and variable-slope can be combined simultaneously to combine their advantages.

C.3 Broadband Class E design with duty-cycle control

From the discussion about the general Class E model in the former sections, it was found that duty-cycle control can modify dynamically the performance of a Class E amplifier. In order to demonstrate this important observation, this section presents simulations results performed on a suboptimum mode 12W Class E GaN power amplifier. The goal of this experiment is to observe the impact of variable duty-cycles in the behavior of the Class E amplifier, using this GaN design as an example. The transistor of this power amplifier is the intended load for the CMOS drivers that are designed and implemented in the remaining chapters of this thesis.

The schematic of the Class E GaN design is shown in Figure C.11. The parasitic drain capacitance of the GaN transistor fully implements the shunt C capacitance of the Class E topology. The DC-feed inductor L has been sized so as to provide a suboptimum mode of operation. The series filter has been designed at $f_0 = 2.4$ GHz with a loaded quality factor of $Q_{L0} = 3$ when a load $R_L = 75\Omega$ (this load is an application-specific requirement) is employed, to provide broadband operation.

The simulations are performed using an Harmonic Balance setup in Agilent ADS with a GaN HEMT large signal model provided by Cree, Inc. [33]. For this experiment, we assumed an ideal square wave (10 harmonics) swinging from −5 to 0V as the driving signal. The frequency

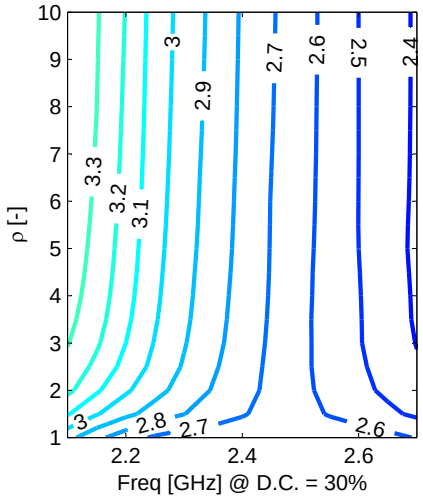
is swept from 2.1 to 2.7 GHz and the output power is backed-off (approximately up to -10 dB) by means of supply and load modulation. The supply modulation is accomplished by sweeping the supply voltage; $10 < V_{DD} < 35$ V. The load modulation is done by increasing the load resistance through a variable called ρ, as shown in the schematic of Fig. C.11, from 1 to 10. The duty-cycle is swept from 30 to 70%.

From the results of the harmonic balance simulations, three parameters were calculated at each simulation point: the normalized peak output voltage (with respect to the supply voltage) $\overline{v_{pk}} = v_{DS,pk}/V_{DD}$, the output power P_{out} and the drain efficiency η. These parameters are shown in the contour plots of Figures C.12 and C.13 for the load modulation, and in Figures C.14 and C.15 for the supply modulation.

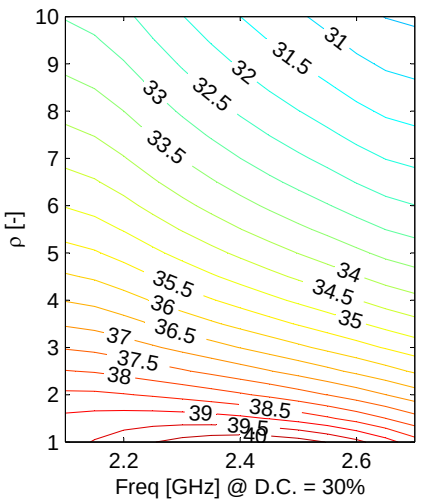
In Fig. C.12(c) it can be observed that, at 2.4GHz, $\overline{v_{pk}}$ is indeed lower than 3, indicating a suboptimum mode for Class E, as expected from design. Also, observe that $\overline{v_{pk}}$ has its higher values at 70% duty-cycle, seen in Fig.C.12(e), which is also according to the Class E model's prediction. In Figs. C.12(b), C.12(d), and C.12(f) it can be seen that the output power is backed-off as ρ increases from 1 to 10. In this case, the supply is maintained constant and only the load is increased by means of ρ.

In the contour plane of Fig. C.13(c), one can observe the drain efficiency at different frequencies and backed-off output power levels (due to load modulation) at the customary 50% duty-cycle. Compare those efficiency levels with the ones in the contour planes at smaller duty-cycles, shown in Figs. C.13(a) and C.13(b). Observe the improvement in efficiency in most of the contour plane, except in the left-top corner region. Note also that larger duty-cycles (> 50%) seem not to provide any advantage (i.e. lower drain efficiency and higher peak voltages), as seen in Figs. C.13(d) and C.13(e).

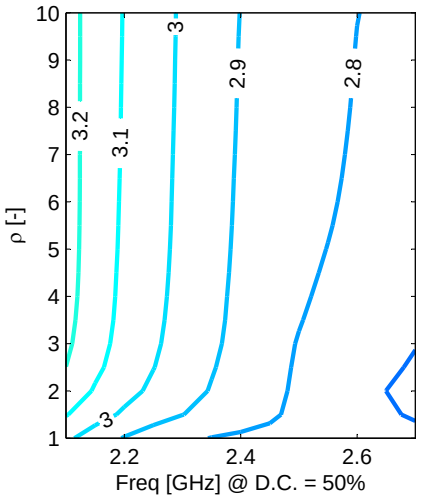
Figures C.14 and C.15 show the normalized peak voltage, output power, and drain efficiency, when the output power is backed-off through supply modulation. In this case, the load is fixed and the supply voltage varies. Observe again how the normalized peak voltages increase with larger duty-cycles, as seen in the left-hand side of Fig. C.14. The right-hand side of Fig. C.14 shows the backing-off for the output power and its bandwidth around 2.4 GHz (due to $Q_{L0} = 3$). In Figs. C.15(a), C.15(b) and C.15(c), observe the improvements in drain efficiency for smaller duty-cycles for similar output power contour planes (in Figs. C.14(d) and C.14(b)). For larger duty-cycles, notice also here the significant drop in efficiency, in Figs. C.15(d) and C.15(e), and the increased peak voltages, in Fig. C.14(e).



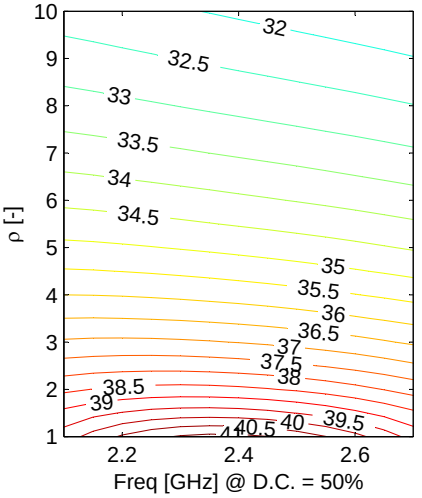
(a) $\overline{v_{pk}}$ (V/V) at D.C.=30%



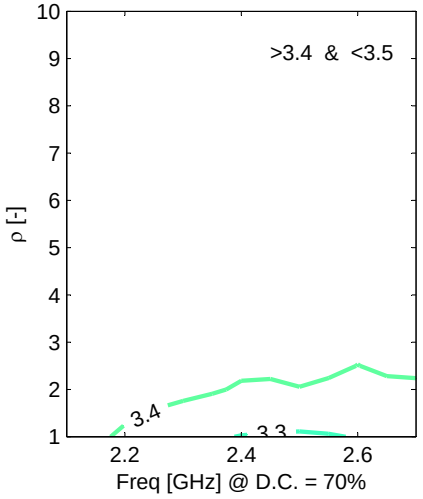
(b) P_{out} (dBm) at D.C.=30%



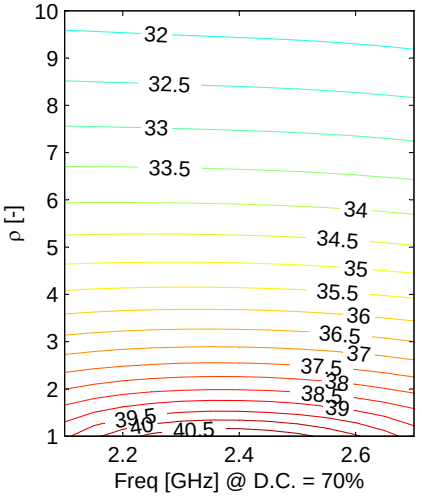
(c) $\overline{v_{pk}}$ (V/V) at D.C.=50%



(d) P_{out} (dBm) at D.C.=50%

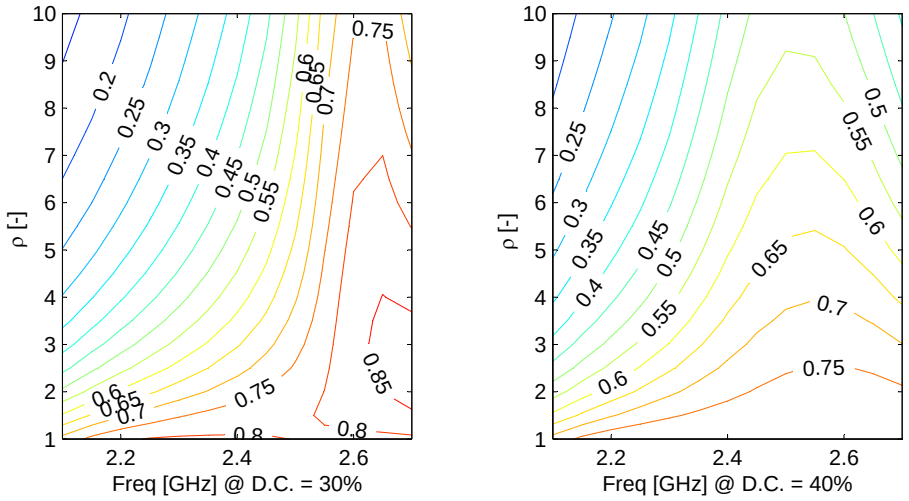


(e) $\overline{v_{pk}}$ (V/V) at D.C.=70%



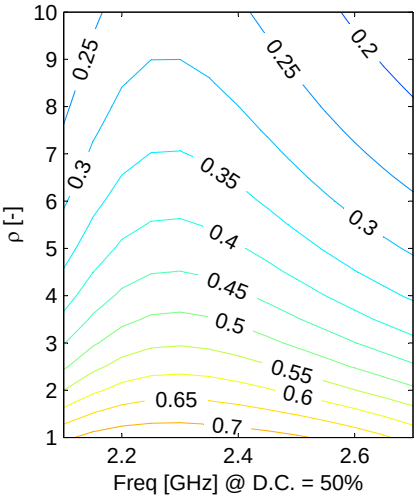
(f) P_{out} (dBm) at D.C.=70%

FIGURE C.12: $\overline{v_{pk}}$ and P_{out} planes for $2.1 < freq < 2.7$ GHz and *load modulation* (i.e. $R_L = \rho \cdot R_{L0}$ for $1 < \rho < 10$) for the Class E amplifier shown in Fig. C.11 at different duty-cycles (30%, 50%, and 70%).

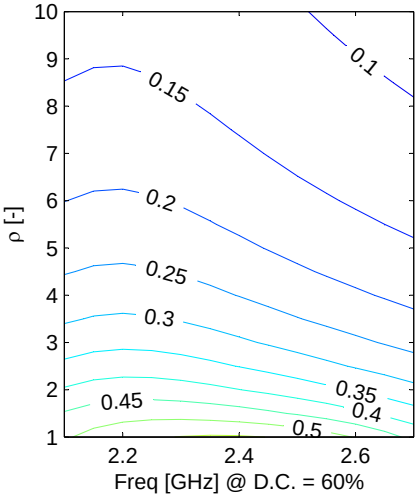


(a) η at D.C.=30%

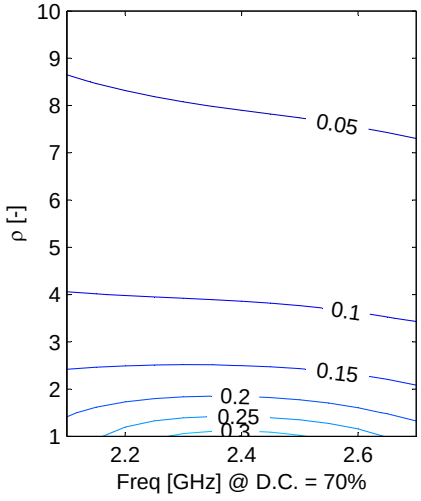
(b) η at D.C.=40%



(c) η at D.C.=50%

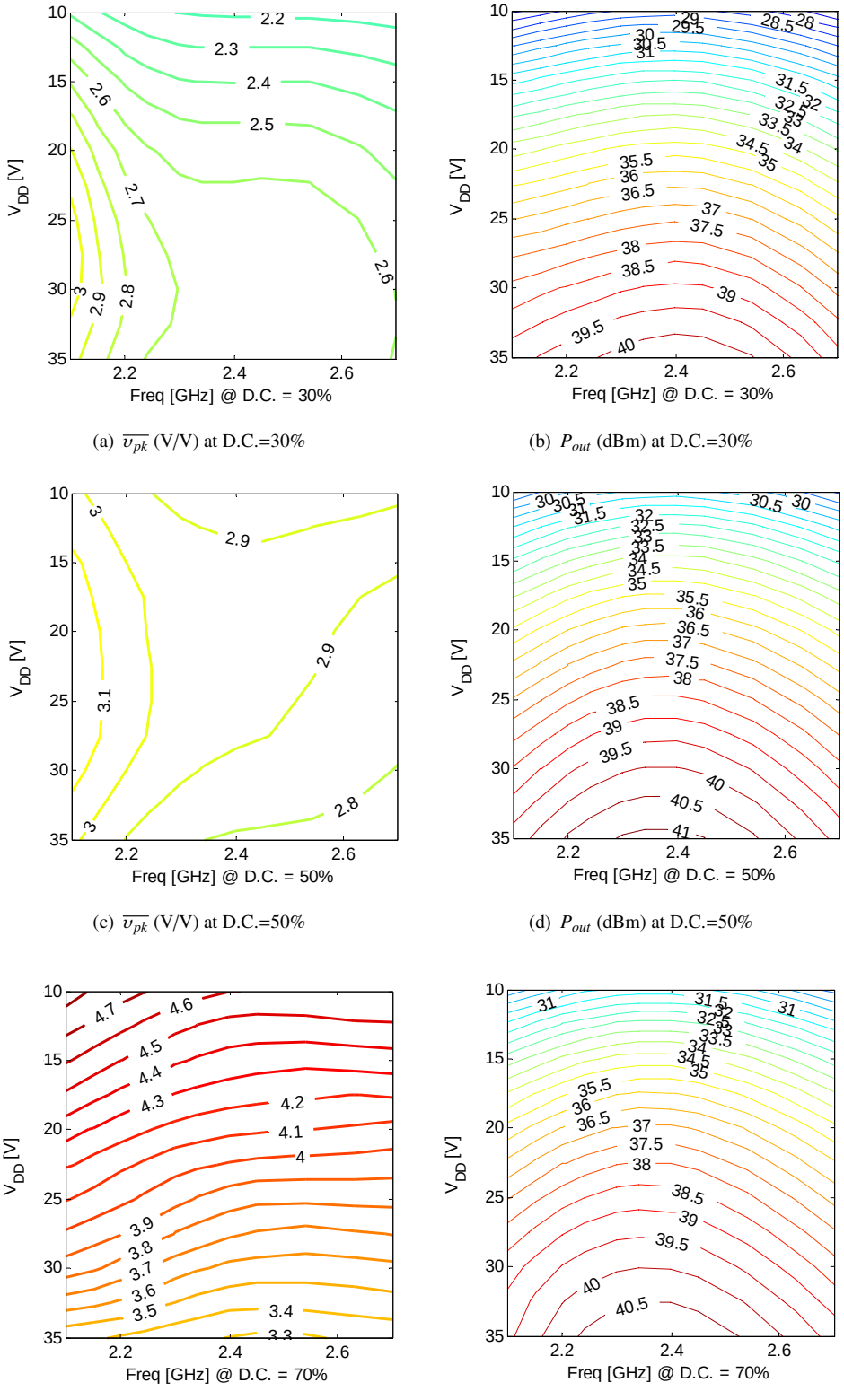


(d) η at D.C.=60%



(e) η at D.C.=70%

FIGURE C.13: η planes for $2.1 < freq < 2.7$ GHz and *load modulation* (i.e. $R_L = \rho \cdot R_{L0}$ for $1 < \rho < 10$) for the Class E amplifier shown in Fig. C.11 at different duty-cycles (30%, 40%, 50%, 60%, and 70%).



(a) $\overline{v_{pk}}$ (V/V) at D.C.=30%

(b) P_{out} (dBm) at D.C.=30%

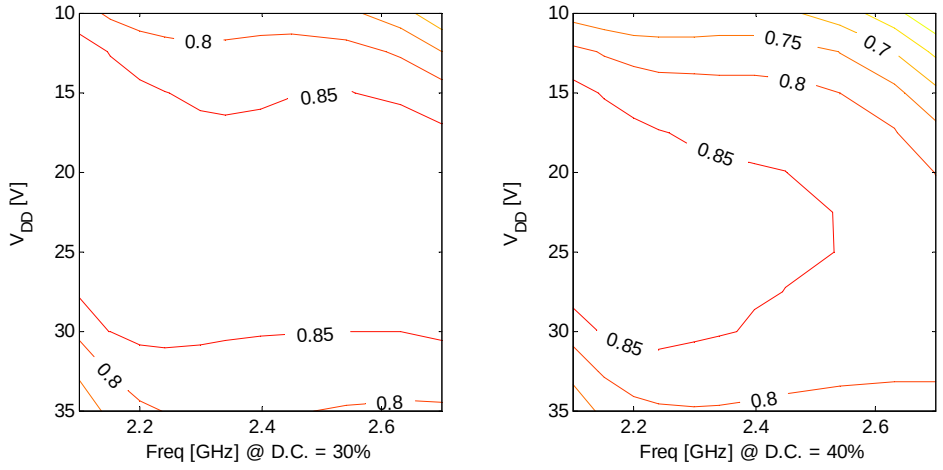
(c) $\overline{v_{pk}}$ (V/V) at D.C.=50%

(d) P_{out} (dBm) at D.C.=50%

(e) $\overline{v_{pk}}$ (V/V) at D.C.=70%

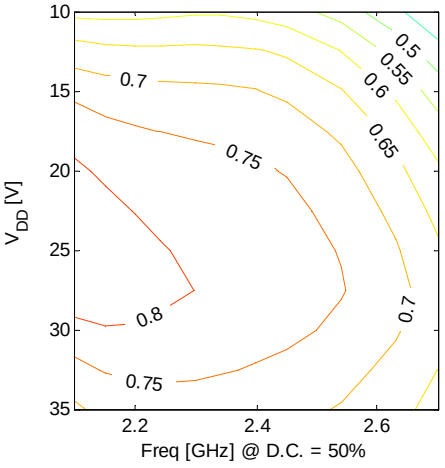
(f) P_{out} (dBm) at D.C.=70%

FIGURE C.14: $\overline{v_{pk}}$ and P_{out} planes for $2.1 < freq < 2.7$ GHz and *supply modulation* ($10 < V_{DD} < 35$ V) for the Class E amplifier shown in Fig. C.11 at different duty-cycles (30%, 50%, and 70%).

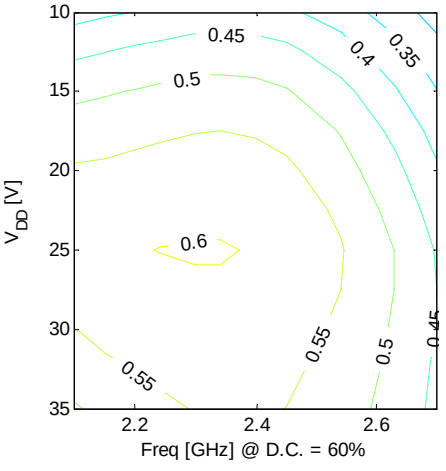


(a) η at D.C.=30%

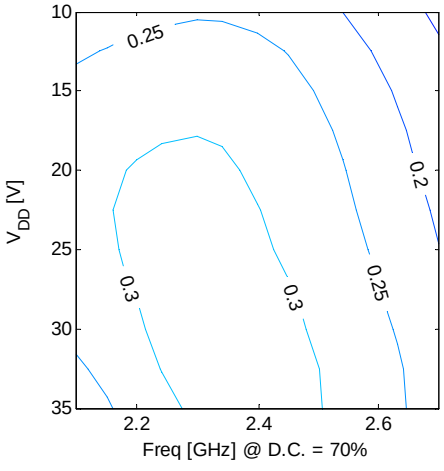
(b) η at D.C.=40%



(c) η at D.C.=50%



(d) η at D.C.=60%



(e) η at D.C.=70%

FIGURE C.15: η planes for $2.1 < freq < 2.7$ GHz and *supply modulation* ($10 < V_{DD} < 35$ V) for the Class E amplifier shown in Fig. C.11 at different duty-cycles (30%, 40%, 50%, 60%, and 70%).

This experiment has demonstrated that the efficiency of a Class E amplifier can be recovered at backed-off power levels (due by both, load and supply modulation) over a wide bandwidth, by duty-cycle control as showed in Figs. C.13 and C.15. This outcome can be usefully applied in novel broadband high-efficiency power amplifiers. Therefore, duty-cycle control capability in driver circuits can be an important added feature.

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