Pick & Place of waveguide structures

Heterogeneous Integration

Master Graduation Project
Electrical Engineering

S.C. Fakkel

Delft University of Technology

TU Delft

Pick & Place of waveguide structures

Heterogeneous Integration

by

S.C. Fakkel

A thesis presented for the degree of MSc Electrical Engineering.

Studentnumber:	4966538	
Project duration:	Januari, 2023 - December 21, 2023	
Master Thesis commitee:	Dr. R. Ishihara,	TU Delft, supervisor
	Prof. dr. P.J. French	TU Delft
	M. van der Maas,	TU Delft

This thesis is confidential and cannot be made public until December 21th, 2028

TU Delft

Abstract

Classical computer have difficulties simulating specific complex problems, therefore other computation options are being explored. One of these options is the quantum computer, which is expected to excel in various industries. The challenge for the quantum computer is scaling it up to a high number of qubits. The diamond-based quantum computer is a suitable candidate for quantum computer, because it can be made scalable, with long coherence times, relatively high temperatures and low cross talk. Making such a scalable modular quantum computer using diamond qubits requires heterogeneous integration of optical components. Multiple integrations techniques for optical components exist, however in this thesis we are particularly interested in integrating a superconducting nanowire single photon detector (SNSPD) with pick & place onto the quantum chip to read out the photons emitted by diamond color-centers. The main goal of this thesis is to find out which integration scheme leads to the highest on-chip detection efficiency of a pick & place on waveguide integrated SNSPD.

In this work we designed a silicon nitride structure with low loss tapered support structures. Next different releasing methods are introduced to release the fabricated silicon nitride structure independent of the material stack and with a high yield. Lastly, we show how waveguide structures can be pick & placed on receptor chips that underwent surface treatment.

Preface

This thesis has been written in the context of the Master Graduation Project. The project is part of the Fujitsu project, a joint project to build a scalable quantum computer in collaboration with the Delft University of Technology, QuTech, TNO and Fujitsu.

I would like to thank my daily supervisor Maurice van der Maas for all the effective feedback and guidance during the project. Together with Salahuddin Nur we have had some enjoyable and meaningful discussion throughout the year. Furthermore, I would like to thank Aryan Dubey, Erbin Hua and Yannis Varveris for training and accompanying me in the cleanroom. Last but not least, I would like to express my gratitude to Ryoichi Ishihara for giving me the opportunity to work on this project.

S.C. Fakkel
Delft, December 2023

Contents

1

Motivation for Quantum Computing

The transistor, invented in 1947, is one of science's greatest inventions [1]. After its discovery, the development and engineering issues, such as the vacuum tube and the relay time had to be solved, before it could be widely manufactured for industry, as the advantage of the transistor is that its a small size and low power device [2]. switching from Geranium to Silicon solved these issues. Furthermore, the sizes of transistors began shrinking, following Moore's Law, which stated that the number of components would double every two years [3], as can be seen in Fig. 1.1. However, as transistor sizes are nearing the scale of just a few atoms, it is getting more difficult and expensive to increase the amount of transistors on a given silicon area, resulting in Moore's Law to slow down [4]. Moreover classical computers have difficulties tackling exponentially scaling problems [5]. Therefore, other computations options are being explored.

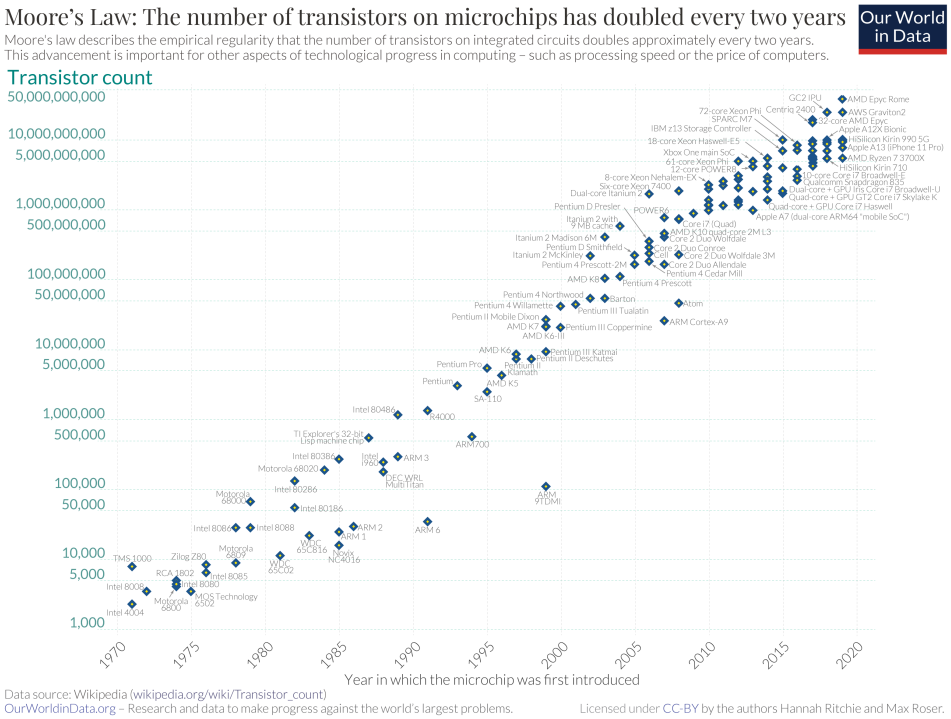


Figure 1.1: A plot depicting the number of transistors on microchips over time, following Moore's Law. Adopted from Roser et al. (2023)[6].

1.1. Introduction to Quantum Computing

One of those options is the quantum computer. This computer is expected to excel in various industries. For example, in quantum chemistry the design of drugs, catalysts and materials could be simulated with significantly geater accuracy and speed [7]. Furthermore, the work in [8] already showed that a quantum computer could perform an experiment 1 million times in 200 seconds, while a classical supercomputer would take 10,000 years to do the same task.

The quantum computer does not use classical computer bits, that could be either a 0 or 1, instead it makes use of qubits. Qubits can be a 1 or 0, but also a combination both, which is called superposition and can be represented with the following vector [9]:

$$|\psi\rangle = cos\frac{\theta}{2}|0\rangle + e^{i\phi}sin\frac{\theta}{2}|1\rangle \tag{1.1}$$

The qubit can be visualized using a Bloch sphere, where a vector is used to represent the state of the qubit, as can be seen in Fig. 1.2. When a qubit is measured it collapses to one pole of the two poles of the Bloch sphere, resulting either in a 0 or 1.

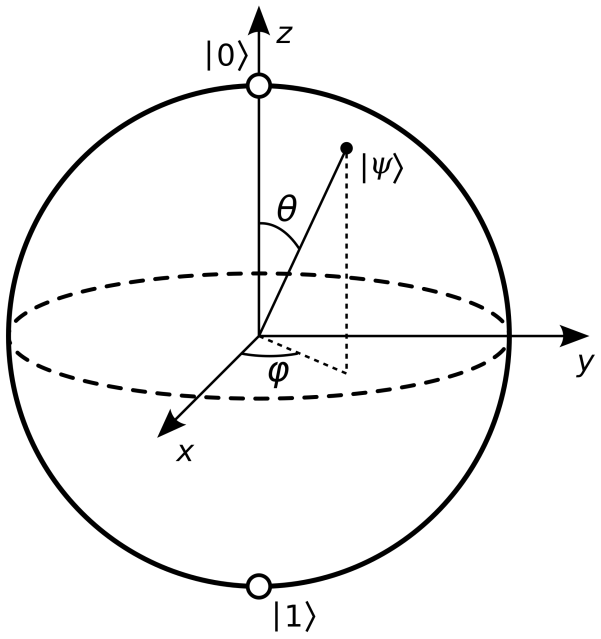


Figure 1.2: A qubit visualized by a Bloch sphere. Adopted from Nielsen et al. (2010) [9].

1.2. Diamond-based Quantum Computer

Quantum computers that exist today and have over 10 or more connected qubits are diamond and superconducting based. The next challenge for these quantum systems is to scale up towards a large number of qubits, so it could be used for quantum computation.

Qubits in diamond have two advantages over using superconducting qubits. The first reason being that a diamond quantum computer could be made of smaller modules that could be coupled together by optical connections. This makes it scalable, while superconducting qubits are limited by their size and cross talk. The second reason being that the diamond

based quantum computer can work at relatively high temperatures with long coherence times, compared to the operating temperature of a superconducting qubit.

Diamond based quantum computer are based on color-centers that have an electron spin and carbon-13 nuclear spins that can can be used as a memory element [10]. These color centers have a ground state (M_S=0) and an excited state (M_S=±1), as can be seen in Fig. 1.3. To use these color-centers as a qubit two levels are selected, namely (M_S=0) for spin up and and the (M_S=−1) for spin down. By using microwave pules the spin of the electron can be controlled from the spin up state to the spin down state, and up again in a oscillating pattern. Exactly halfway there will be a superposition of the spin being in the up state and down state. When a laser pulses is applied that is only resonant when the spin is in its excited state, a photon will be emitted. When the spin is in its ground state, it will remain dark and no photon will be emitted.

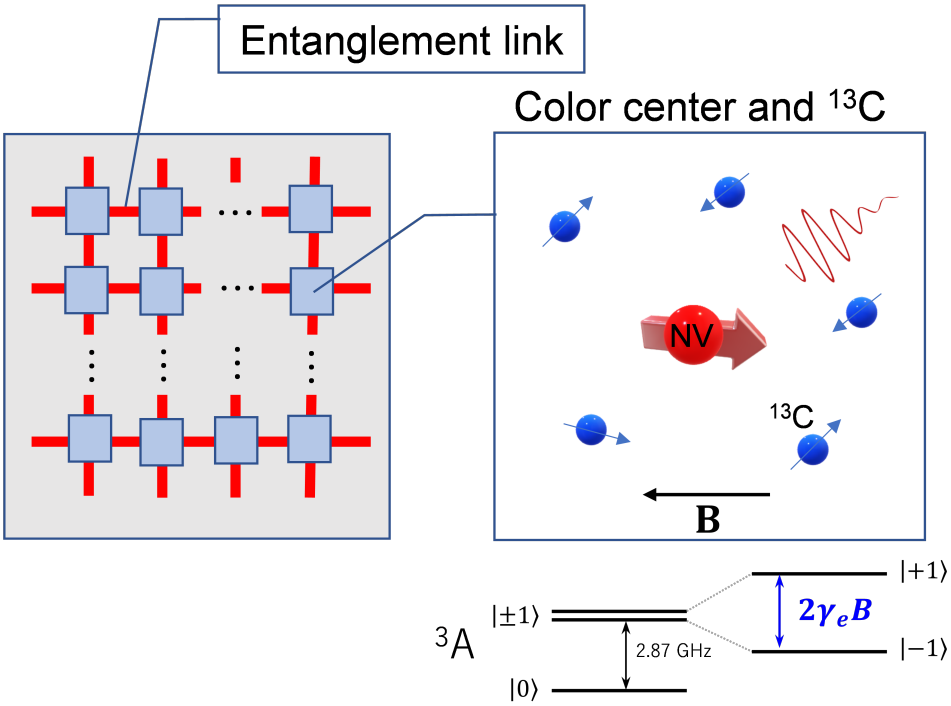


Figure 1.3: NV-center spin-qubit for a modular quantum computer chip. Adopted from Ishihara et al. (2021) [11].

1.3. Heterogeneous Integration

At the Ishihara lab in Delft we are working on a 3D integrated scalable modular quantum computer using diamond qubits. This quantum chip contains diamond color-centers that are linked with optical modules [11], together with a magnetic-field generator for controlling the qubits, photonic circuits for the readout of photons emitted by the color-centers and micro-bumps to connect a cryo-cmos chip using flip-chip bonding for a complete package [11], as can be seen in Fig 1.4.

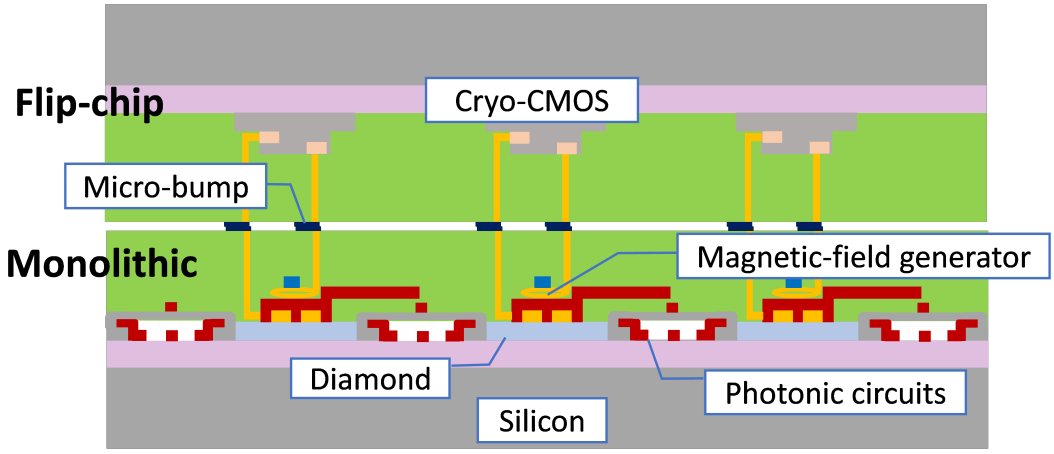


Figure 1.4: 3D integration of a modular quantum computer chip based on color-centers in diamond. Adopted from Ishihara et al. (2021) [11].

For that heterogeneous integration is required, since this method has the advantage of using thin film techniques to make optical components, which are difficult to make in diamond.

Furthermore, a heterogeneous approach for building a quantum computer improves the performance, power, mechanical stability, ability of integrating thermal dissipating materials for heat regulation, multiple power/voltage domains and more testing capabilities [12].

By fabricating optical components on a separate chip, the high-quality devices could be tested, selected and then integrated onto the quantum chip. Moreover, when they are integrated heterogeneously, the fabrication process of different components can be separated. Meaning that there is more freedom and flexibility in changing and optimizing the fabrication process, allowing the process to be reliable, low cost and scalable [13].

Assembling a chiplet[1] - in this case an optical component - on to a quantum chip is difficult, as the misalignment tolerances are small. Therefore, to align the chiplet, one could either use the conventional methods, like pick & place and transfer printing, or self-assembly methods, like surface tension and topographical control.

1.3.1. Conventional Alignment methods

Pick & place

Pick & place is not a new concept, it is widely used in industry and has an important role in PCB assembly lines. The machines use vacuum nozzles that can pick up the components of the donor chip and release them on the solder paste of the receptor chip. The misalignment of most assembly lines is allowed to be in the micrometers for electronic circuits, however, for photonic circuits the misalignment tolerances are in the nanometers. Moreover, this approach is extremely challeging, because having a vacuum nozzle in the nanoscale has not been shown.

In order to still pick & place nanostructures, a needle could be used. This needle makes use of the van der Waals forces that act between the needle and the nansostructure to pick

[1] A small modular integrated circuit component that is designed to provide a specific function [14].

it up. Once the nanostructure is close to the receptor chip, the forces acting between the receptor chip and nanostructure would be larger than the forces between the needle and the nanostructure, meaning that structure is released from the needle and assembled to the receptor chip. The work in [15] demonstrated the pick & place of diamond nanostructures with a misalignment of 38 $\pm$ 16nm.

However, this process takes a lot of time, since it is manually controlled. This also means that the placement of the nanostructure is dependent on skills of the user. In later stages machine learning could potentially be used to automate the pick & place.

Transfer printing
Another approach for assembling photonic structures is transfer printing. This method is also known as stamping, because a stamp is used to transfer the structures from the donor substrate to the receptor substrate, as can be seen in Fig. 1.5. The work in [16] has already demonstrated the use of transfer printing for SNSPD's. And the work in [17] managed to achieve a mean misalignment of -110nm with some placements reaching a misalignment of only a few nanometers.

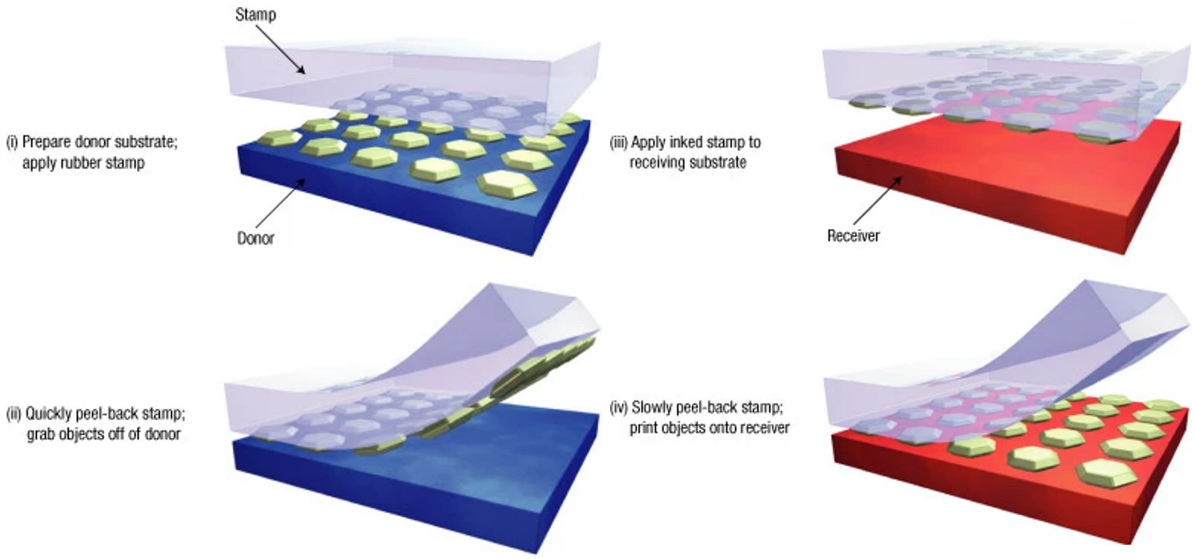


Figure 1.5: Schematic illustration of the process flow for transfer printing. Adopted from Matthew A. Meitl et al. (2017) [18].

1.3.2. Self-Assembly

Unfortunately, self-assembly methods are limited to sub-micron alignment accuracy's with topographical control being the exception. Topographical control makes use of alterations to the substrate surface to guide components to their intended location. Some topographical features that could be used are trenches and side walls to redirect and trap the nanostructures.

An example of topographical control can be found in figure 1.6. It uses a wet solution with nanoparticles that flow over the surface with the help of a top plate. After evaporation, only the nanoparticles that got stuck in the traps remain.

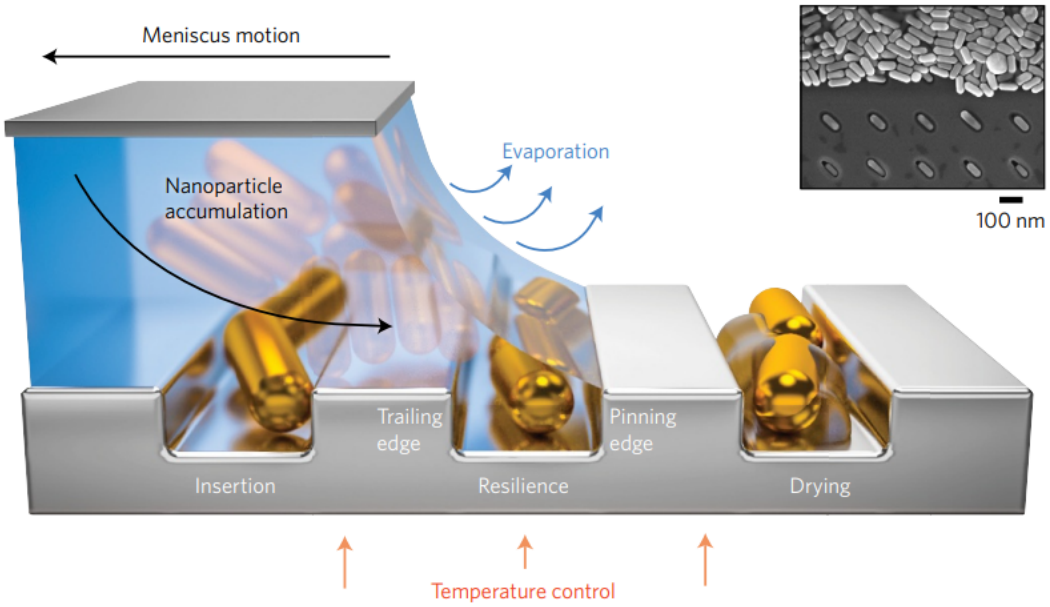


Figure 1.6: Schematic description of self-alignment using topographical control. Adopted from Valentin Flauraud et al. (2017) [19]

If topographical control is combined with surface tension, it can reach nanometric control, as presented in [19], where nanorods are touching each other and a very small scale is reached.

Apart from having contact-to-contact alignment - which is important for the photonic properties - topographical control is independent of the surface substrate and can be scaled up. Besides they have a high assembly yield.

1.4. Single Photon Detectors

The optical component of the quantum computer we are interested in for this thesis project is the photon detector.

The photon detector can be used to detect the photons emitted by the color-centers. This photon detector should be able to detect single photons with a high detection efficiency otherwise it is still unknown what the quantum state of the diamond spin qubit was.

Apart from the detection efficiency other important parameters of single photon detectors are [20]:

Timing jitter: The lower the jitter the more precise in time the arrival of a photon can be detected. Hence, the timing jitter is preferred to be as low as possible so that more quantum states could be measured in a smaller time frame without mixing them up.

Dark counts: A dark count is a detection of a photon without a photon actually being there. Thus, a low dark count is preferred for the photon detector otherwise a quantum state could be read out wrong.

Maximum count rate: The maximum count rate is the amount of photons that can be counted in each second. The higher the maximum count rate the more photons can be detected, thus the more quantum states could be measured.

Optical range: The optical range of the detector should cover the wavelength of the photon emitted by the color-center for it to detect the photon.

Photon number resolution: This means that a detector is able to detect multiple photons at the same time.

Operating temperature: The operating temperature is the temperature at which the photon detector operates. A quantum computer is cooled down to cryogenic temperatures for the qubits to be more stable and have a longer coherence time.

A table that compares different single photon detectors by the previously determined key metrics has been published in [21]. From the table it can be noticed that both the transition edge sensor (TES) and the superconducting nanowire single photon detect (SNSPD) can achieve a high detector efficiency. What is remarkable is that both the TES and SNSPD make use of superconductivity. Other superconductivity based single photon detectors are the superconducting tunnel junction (STJ) and microwave kinetic inductance detector (MKID) [22].

Following the key parameters set for the photon detector to detect photons emitted by color-centers in diamond, the SNSPD is the most promising canditate. Because it can read-out the color-centers fast (maximum count rate), distinctively (timing jitter), miss a low percentage of photons (detection efficiency), while counting a low amount of non-existing photons (dark count). An example of how an SNSPD looks like can be seen in Fig. 1.7

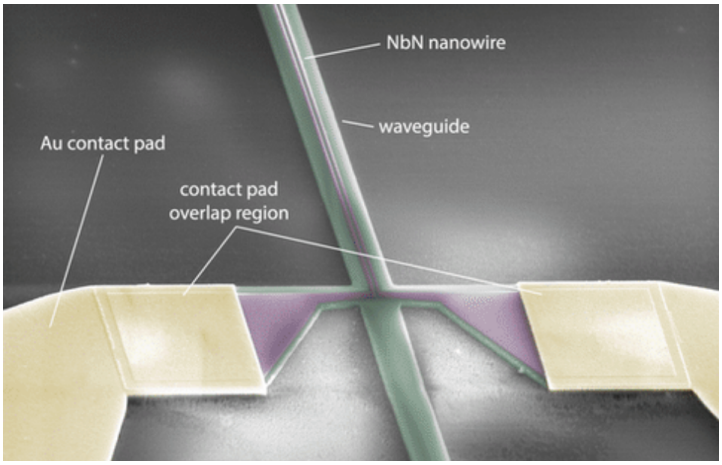


Figure 1.7: A NbN waveguide integrated on top of a Si_3N_4 SNSPD. Adopted from Oliver Kahl et al. (2015) [23].

Table 1.1: The performance table of different single photon detectors based on the key matrices. Adopted and altered from S. Ferrari et al. (2018) [21].

	Timing jitter (FWHM)	Dark counts	Maximum count rate	Optical range	Detector Efficiency	Photon Number Resolution	Operating temperature
GaAsP PMT	80 ps	<10 kcps	10 Mcps	VIS	40%	Only using spatial/time multiplexing	300K
InP/InGaAs PMT	400 ps	250 kcps	n.a.	NIR	2%	Intrinsically limited	213K
VLPC	2 ns	20 kcps	100 kcps	VIS	88%	Intrinsically limited	6.9K
Si SPAD	20 ps	<100 cps	1 Mcps	VIS	55%	Only using spatial/time multiplexing	120K
InGaAs SPAD	140 cps	12 kcps	197 Mcps	NIR	45%	Only using spatial/time multiplexing	200K
TES	25 ns	Negligible	1 Mcps	VIS to MIR	>97%	Yes	100mK
SNSPD	<5 ps	<10 cps	25 Mcps	UV to MIR	>90%	Only using spatial/time multiplexing	<4 K

1.4.1. Working principle SNSPD

Since the SNSPD is the most promising candidate to readout color-center in a diamond based quantum computer, it is necessary to understand how the device works.

The superconducting nanowire single photon detector (SNSPD) is a narrow wire made from a superconducting material. For the length of the wire there are trade offs to make as on one hand a short nanowire, has a high maximum count rate, low death count rate and low timing jitter, and on the other hand a long nanowire has a higher detection efficiency [24].

In order for the nanowire to detect single photons it is cooled down to cryogenic temperatures. Cooling down the superconducting material to such low temperatures causes the electrons to form cooper pairs.

When a photon is propagating through either free space, an optical cable or a waveguide and is absorbed by the SNSPD, the photon could cause quasiparticles to form also known as the breaking of cooper pairs [25]. Therefore, parts of the nanowire will not be superconducting anymore, this resistive region will cause heating and grow further till a resistance of a few kΩ, resulting in a redirection of the bias current into the readout circuitry [26].

1.4.2. Nanowire materials

To achieve the previously mentioned superconductivity, the nanowire must be cooled down to its specific operating temperature. Each superconductor has its own unique properties for it to become superconductive, such as the critical temperature, current and magnetic field [27]. A comparison table is made to compare superconductors for SNSPD's, as can be seen in Table 1.2. From this table it can be concluded that NbTiN seems to be a suitable

candidate for the superconducting nanowire of a SNSPD, as SNSPD's made from NbTiN have shown a high detection efficiency and low timing jitter, which is important parameters for the detection of photons emitted by the color-centers.

Table 1.2: A comparison table of SNSPD's with nanowires made out of different materials. Adopted from J. Chang (2021) [28].

Detector type	Detector efficiency	Timing jitter	Operating temperature	Wavelength
NbN [29][30]	$92 - 98.2\%$	40-106.1 ps	0.8-2.1K	1550-1590 nm
NbTiN [31][32]	$92 - 99.5\%$	14.8-34 ps	2.5-2.8K	1290-1500 nm
WSi [33][34]	$93 - 98\%$	150 ps	$120mK \leq 2K$	1550 nm
MoGe [35]	20%	69-187 ps	250mk-2.5K	1550 nm
MoRe [36]	-	-	9.7K	-
MoSi [37][38][39]	$80 - 87\%$	26-76 ps	0.8-1.2K	1550 nm
NbRe [40]	-	35 ps	2.8K	500-1550 nm
NbTiN [41]	$15 - 82\%$	30-70 ps	2.5-6.2K	400-1550 nm
NbSi [42]	-	-	300mK	1100-1900 nm
TaN [43]	-	-	0.6-2K	600-1700 nm
MgB_2 [44][45][46]	-	-	3-5K	Visible

1.5. Waveguides

Optical waveguides are important for the diamond quantum computer as they are used to guide photons over the chip. In free space these photons travel with the speed of light, however when these electromagnetic waves propagates through a material they interact with electrons inside the material which reduces the propagation speed. Instead of using this reduced propagation speed, the refractive index of a material is often used to describe how a wave behaves inside a material.

The refractive index of a material relates to the propagation speed by the following formula:

$$n = \frac{c}{v} \tag{1.2}$$

where n is the refractive index, c the speed of light and v the propagation speed through a medium.

Unfortunately, waveguides are not perfect and suffer from propagation losses, such as absorption loss in the core material, radiation loss because of leaky higher order modes, bending loss when the route of the waveguide has an arc over the chip and scatter losses caused by fabrication imperfections such as side wall roughness [47]. For the diamond quantum computer it is important that the propagation losses are minimized.

LiNbO3 is seen as a viable option for integrated photonics on quantum chips, because of its electro-optic, acousto-optic and nonlinear properties [48]. The forming of a waveguide for LiNbO3 can either be realised by a proton exchange process [49] or titanium in-diffused lithium niobate (Ti:LiNbO3) [50].

According to [48], the titanium in-diffused lithium niobate has the preference over the proton exchange process, because Ti-diffusion allows waveguides propagation in both TE and TM polarisation, which is useful for polarisation qubits.

Another viable option is silicon nitride because of its low propagation losses [51][52], and it is also less complex to fabricate in comparison to lithium niobate, because of these properties silicon nitride has been chosen to serve as the waveguide material for the diamond quantum computer in our project.

1.6. Goal of this Thesis

This work focuses on the heterogeneous integration of awaveguide integrated SNSPD. This SNSPD should have a detection efficiency greater than 80%, with a preferred detection efficiency of 90% as stated as a deliverable for this project. The SNSPD itself consists of a SiN based waveguide, a metal contact pad and preferably a $NbTiN$ superconducting nanowire. It will be fabricated on a separate chip for it to be pick & placed onto the quantum computer chip, as can be seen in Fig. 1.8.

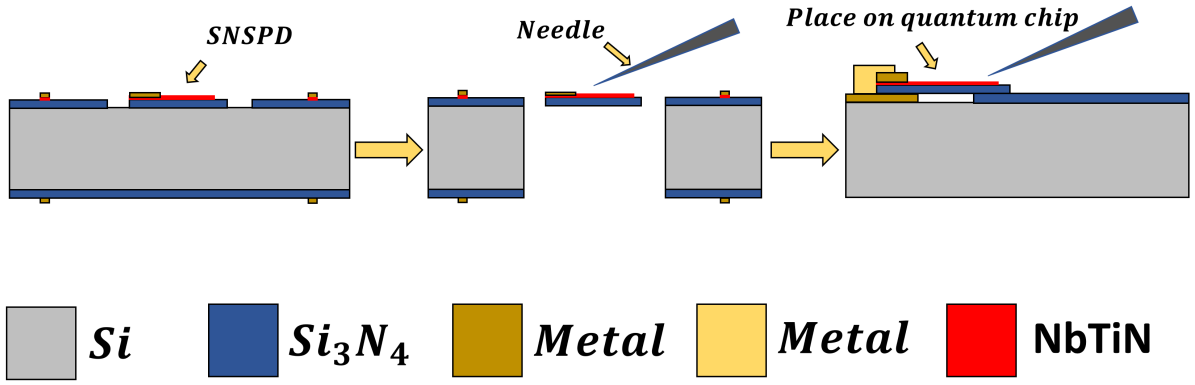


Figure 1.8: Schematic illustration of an SNSPD placed onto the quantum chip.

This thesis thesis hopes to contribute to this state-of-the-art research by finding out which integration scheme leads to the highest on-chip detection efficiency (OCDE) of a pick & place on waveguide integrated superconducting nanowire single photon detector.

1.7. Outline

In this thesis, we will work towards an integration scheme for a pick & place on waveguide integrated superconducting nanowire single photon detector (SNSPD). To achieve this the thesis is split up into three main parts, namely design, fabrication and pick & place. An overview of the thesis is given in Fig. 1.9.

Figure 1.9: The flowchart of the project.

In Chapter 2 - the first part of the thesis - the misalignment tolerances of butt & tapered coupling structures are determined for pick & place. Furthermore, the support structure of a chiplet is designed, so that it can be fabricated in the next chapter.

In Chapter 3 - the second and most crucial part of the thesis - wet and dry etching approaches for releasing the previously designed chiplet are discussed. This chapter also includes, back-side alignment and the chiplet fabrication process itself. The chapter ends with an overview of all the fabrication steps for making and releasing a chiplet.

In Chapter 4 - the third part of the thesis - pick & place operations of diamond chiplets are performed. Moreover, different surface treatments are analyzed for improving the process.

Lastly, in Chapter 5, a conclusion is drawed based on the findings during this project. In addition, suggestions are given for future research.

2

Design

This chapter covers the Design of the chiplet. It is the first part of the project, as can be seen in Fig. 2.1.

In this chapter the chiplet will be designed so that it could be fabricated in Chapter 3 and pick & placed in Chapter 4. First the misalignment tolerances of different coupling structures are explored. Second a low loss support structure is designed.

Figure 2.1: The flowchart of the project highlighting the current chapter: Design

2.1. Requirements

In the deliverable for this project it states that the required detection efficiency of the photon detector should be greater than 80% with the preference of being greater than 90%.

The detection efficiency is also know as the the On-Chip Detection Efficiency(OCDE) that consists of 3 efficiency parameters, namely the absorption efficiency, the intrinsic efficiency and the threshold efficiency [53]. However, since the SNSPD is integrated on top of a waveguide, an extra coupling efficiency parameter is added to take the coupling losses between the waveguide and the chiplet waveguide into account.

The four efficiency parameters:

absorption efficiency(η_{abs}): When a photon nears the detector it should be absorbed, so that it could be detected. This parameter describes the probability of a photon to be absorbed by the detector.

intrinsic efficiency(η_{ide}): When a photon is absorbed by the detector, an electrical signal should be generated. This parameter describes the probability of an absorbed photon to create an electrical signal.

threshold efficiency(η_{thres}): When an electrical signal has been generated by an absorbed photon, the signal should be amplified and registered by external electronics. This parameter describes the probability of the generated electrical signal to be registered by external

electronics.

coupling efficiency(η_c): When the initial waveguide ends, the photon should couple to the waveguide of the chiplet with the SNSPD on top. This parameter describes the probability of a photon coupling to the chiplet waveguide.

Combining the four parameters, gives

$$OCDE = \eta_{abs}\eta_{ide}\eta_{thres}\eta_c \tag{2.1}$$

For the design of the chiplet waveguide, only the coupling efficiency is of importance, as the other parameters depend more on the quality of the SNSPD and the readout circuitry. The other parameters are not known yet for the SNSPD that is going to be fabricated, therefore we take a look at literature for the remaining parameters.

The work in [54] showed that a non-pick & placed NbTiN SNSPD on top of a Si_3N_4 waveguide achieved a OCDE of 52.5% for a 1542nm wavelength and a OCDE of 80.1% for a 768nm wavelength. This doesn't include the coupling efficiency parameter, meaning that the coupling efficiency of the pick & place integrated chiplet and the on chip waveguide has to be 100% for it to meet the requirements. The work in [55] showed a near-unity detection efficiency of a NbTiN nanowire on top a silicon-on-insulator waveguide for a 1545nm wavelength, which means that the coupling efficiency should at least be greater than 80%. Other works also based on a NbTiN SNSPD and a Si_3N_4 waveguide show detection efficiencies up to 90% [56][57][58]. As the average and expected detection efficiency of non-heterogeneously integrated SNSPD's is about 90%, the coupling efficiency should at least be greater than 90% to meet the required OCDE of 80%.

Apart from the coupling efficiency, also the losses of the support structure should be taken into account. The aim for the support structures is to have the losses as low loss as possible, as it is not yet known how the support structure influences the detection efficiency of the SNSPD.

The SnV color-center in the diamond chip is excited by a 515nm light source, and the fluorescence emitted by the SnV color-center has a wavelength of 620nm [59]. The thickness and width of the waveguide have been determined to be 150nm and 500nm for a Si_3N_4 waveguide on a SiO_2 insulator, accordingly, for single-mode propagation by Saliha Neji[1].

To summarize ther requirements for this chapter:

- The coupling efficiency should be 90% or greater.
- The support structure losses should be minimized.
- The wavelength should be 620nm.
- The Si_3N_4 waveguide should have a 150nm thickness and a 500nm width.
- The SiO_2 should serve as the insulator.

[1]Master Thesis at Ishihara lab, QuTech, Delft, the Netherlands

2.2. Simulation parameters

All the Finite-Difference Time-Domain (FDTD) simulations for the coupling and support structures were conducted using RSoft. Furthermore, for all the simulations the total length of the waveguide was 10μm. Using a longer waveguide would unecessarily increase the simulation time.

To reduce the simulation time, the structure was divided into small grid cells that calculate the electromagnetic fields in both space and time. For the grid sizes the following rule of thumb was used:

$$gridsize = \frac{\lambda}{10} \tag{2.2}$$

Which means that the grid should be at least smaller than 10% of the wavelength. Sometimes smaller grid sizes are preferred near small structures for more accurate simulations.

The launch filed of the simulation had bad coupling to the Si_3N_4 waveguide. To solve this problem, first the fundamental mode was simulated, and then used as the launch field for the upcoming simulations.

2.3. Coupling

In this section we will discuss two different coupling structures, namely tapered coupling and butt coupling. The function of the coupling structure is to couple the light from the waveguide into the waveguide of the chiplet, while minimizing reflections and losses. Since the placement of the chiplet is not perfect, the coupling efficiency of misaligned chiplets has been simulated.

2.3.1. Tapered

The idea of tapered coupling is to make the tip of the waveguide pointy, such that the mode gradually transforms into the other waveguide, which also has a pointy tip. An example of such an adiabatic coupler can be seen in Fig. 2.2. In the research [47] conducted by Saliha Neji, different variations of adiabatic couplers have been simulated. Each variations had an adjustment in either the width or length of the tip. A chiplet with dimensions of 200nm thickness, 500nm width, 10μm taper length, and 100nm taper width can achieve a coupling efficiency above 90% when the misalignment is less or equal than 60nm, and 95% for a misalignment of 50nm.

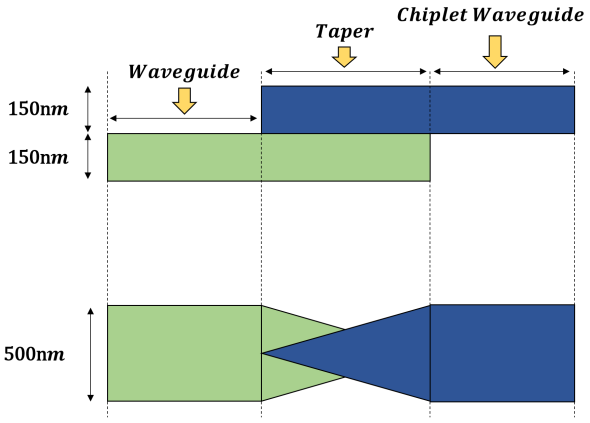


Figure 2.2: Side and top view of an adiabatic coupler.

2.3.2. Butt

Another coupling method is butt coupling. There, the two ends of the waveguides are aligned with each other preferably even touching. However, since this is difficult to achieve on nanoscale, there will always be a gap between the waveguides, as can be seen in Fig. 2.3. The gap with of the two waveguides is of utter importances for the coupling efficiency, therefore different gap widths have been simulated.

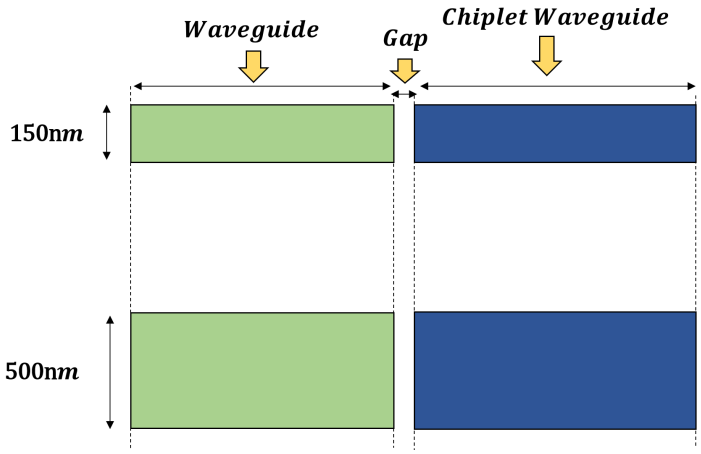


Figure 2.3: Side and top view of a butt coupler.

For the gap simulations a monitor was placed just prior to the gap at z=2.5μm and one after the gap at z=7.6μm. The following formula is used to compare the coupling losses of different gap lengths by their power:

$$\eta_C = \frac{P_{z=0.1}}{P_{z=7.6}} \tag{2.3}$$

Table 2.1 shows the coupling efficiency for different gap lengths along the z-direction. A misalignment along the x-direction yielded similar results, hence the misalignment of the chiplet should be about 50nm or less for a butt coupled waveguide to meet the requirements, and having contact to contact alignment results in a near unity coupling efficiency. Increasing

Gap length	Coupling Efficiency
100nm	80.4%
50nm	93.4%
40nm	95.3%
30nm	97.3%
20nm	98.5%
10nm	99.6%
0nm	99.9%

Table 2.1: Coupling efficiency table for different gap lengths along the z-direction.

the width of the chiplet waveguide did not result in higher coupling efficiencies.

In Fig. 2.4 it can be seen that the electric field becomes far weaker after the 100nm gap, indicating that there are coupling losses. Reducing, the gap length results in a stronger electric field after the gap.

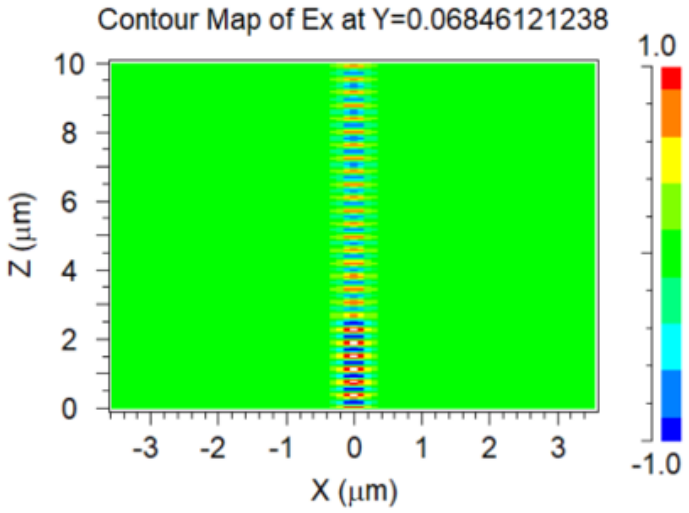
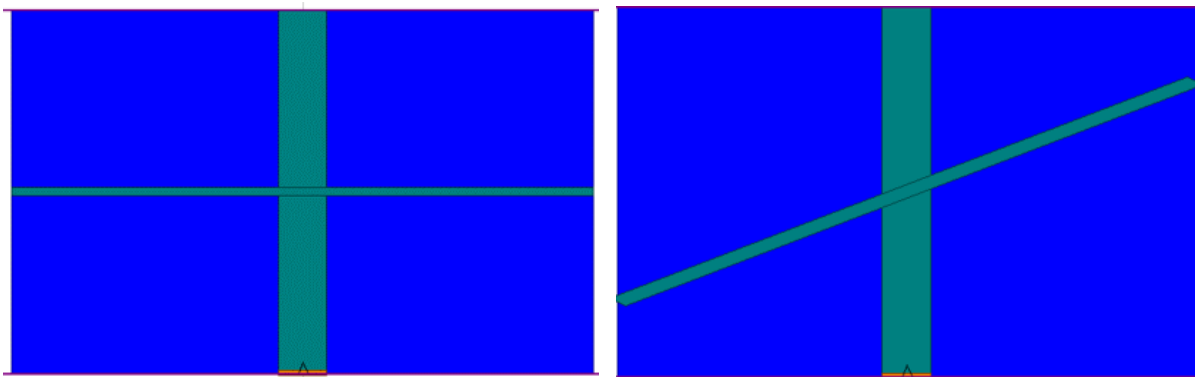


Figure 2.4: RSoft butt coupling simulation for a gap of 100nm along the Z-direction showing the electric field strength.

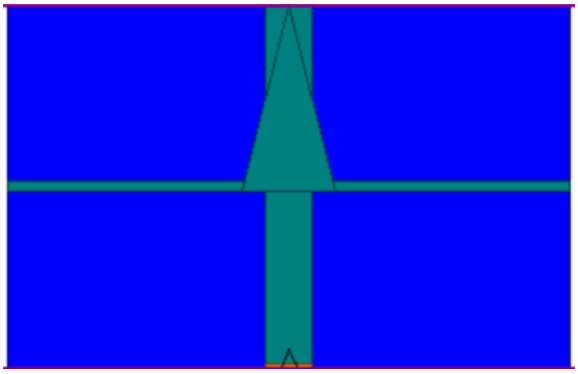
2.4. Support Structure

The main purpose of adding a support structure to the chiplet is to prevent the structure from breaking in the pick- & place process. The support structure also serves as a handle for picking it up with a needle. The support structure is made out of the same material as the waveguide, thus silicon nitride, and will be made around the waveguide.

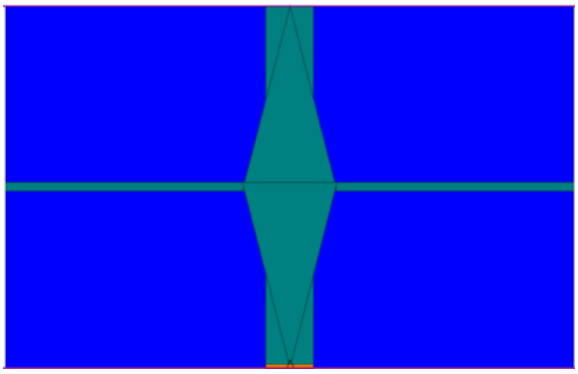


(a) 250nm wide horizontal support structure.

(b) 250nm wide 45-degree diagonal support structure.



(c) 250nm wide horizontal support structure including a taper.



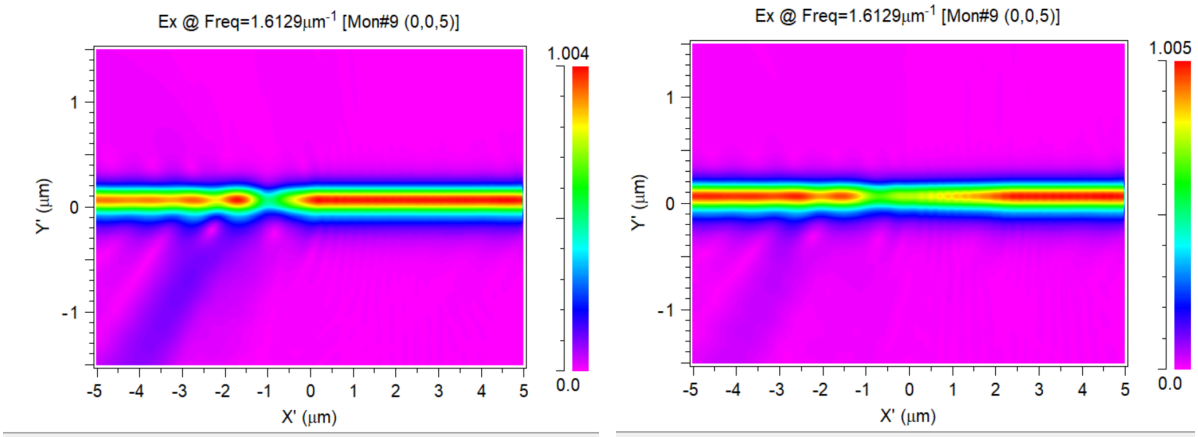
(d) 250nm wide horizontal support structure including two tapers.

Figure 2.5: Silicon nitride support structures intersections with a 500nm wide and 150nm thick silicon nitride waveguide.

The first support structure intersection was 250nm wide and had a propagation loss of 6.71%, as can be seen in Fig. 2.5a. Increasing the width of this support structure results in an increased propagation loss, while decreasing the width of the support structure reduces the propagation loss.

The second version featured a diagonal intersection between a 250nm wide support structure, oriented at a 45-degree angle, as can be seen in Fig. 2.5b. This resulted in a propagation loss of 3.64%.

To reduce the propagation loss a taper variant was simulated. This taper is 1μm wide at the intersection, as can be seen in Fig. 2.5c, this resulted in a propagation loss of 1.85%. That is a 3.6x decrease in loss compared to using no taper. However, using one taper caused reflection as shown in Fig. 2.6a, which is not preferred, as returning photons could disturb the system. Using two tapers, as shown in Fig. 2.5d, reduced the reflection, while the loss remained the same.



(a) Horizontal support structure with 1 taper.

(b) Horizontal support structure with 2 tapers.

Figure 2.6: Crossection of the waveguide, starting from X'=-5 and ending at X'=5 , with a 250nm wide horizonal support in the middle at X'=0.

2.5. Chiplet Design

First a silicon nitride structure is designed for testing the coupling efficiency and support structures so that it can be fabricated in the next chapter. This structure contains either a butt or tapered coupling structure. Furthermore, it includes a horizontal support structures with a taper on both sides.

In the upcoming Chapter 4 we will find out that suspending the structure with 2 releasing tethers together with a strong side structure, results in chiplets that are less challenging to be picked up. The length of the SNSPD and thus the chiplet waveguide are unknown. Therefore multiple variants have been made, that also include different sizes for the tether releasing structures. An example of a silicon nitride structure with tapers and releasing tethers for testing purposes is shown in Fig. 2.7.

It is important to note that this design doesn't include a nanowire and contact pads, and will solely be made out of silicon nitride for testing the pick & place. The final chiplet would include the previously mentioned parts so that the SNSPD could be characterized.

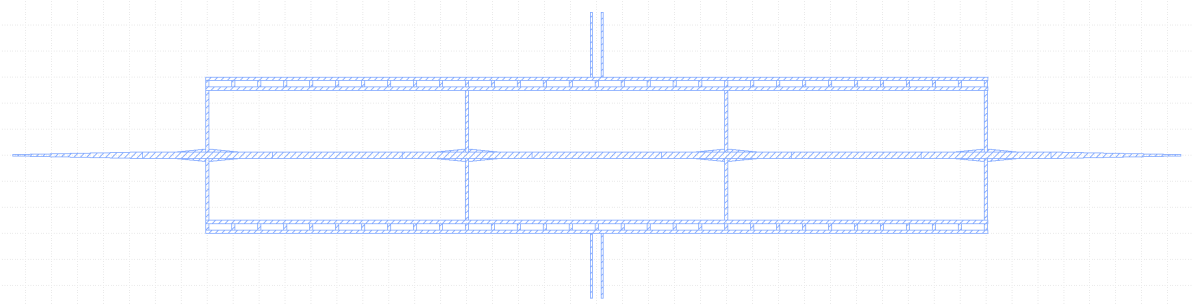


Figure 2.7: A design of a 70μm long chiplet with tapers.

2.6. Conclusion

To achieve a coupling efficiency higher than 90% between the on chip waveguide and the chiplet waveguide, a misalignment tolerance of about 50nm is allowed. Also a horizontal support structure with a taper on each side seems to reduce the propagation losses. These simulations, however, should be validated with real measurements to ensure they are reliable. Therefore, various strucutes have been designed to be fabricated and to test their behaviour in the real world.

3

Fabrication

This chapter covers the Fabrication process. It is the second and most crucial part of the thesis, as can be seen in Fig. 3.1.

In the previous chapter the chiplet was designed. In this chapter the chiplet will be fabricated and released, so that it can be pick & placed in the next chapter. For releasing the chiplet multiple backedging steps have been explored, as well as the making of alignment markers. All of the fabrication steps for this project are carried out within the cleanroom facilities of the Kavli Institute of Nanoscience Delft[1].

Figure 3.1: The flowchart of the project highlighting the current chapter: Fabrication.

3.1. Requirements

The chiplet designed in Chapter 2 should be fabricated in a way that the needle can pick it up during the pick & place phase in Chapter 4.

The final chiplet consists of a silicon nitride waveguide, preferably a niobium titanium nitride superconductor as the nanowire and a contact pad for the electrical connection of the SNSPD to the readout circuitry. This whole material stack is subject to the releasing method used. Each material of this stack could be deposited in different types of the same material. For example, silicon nitride deposited with Plasma-Enhanced Chemical Vapor Deposition (PECVD) could have a low refractive index or a high refractive index, and it could also be deposited with Low-Pressure Chemical Vapor Deposition (LPCVD), each type has its own unique etch rates [60][61][52]. The exact type of each material has not yet been decided. Therefore, it is important that the releasing process should be independent to the type of material used.

The chiplets should also remain undamaged during the fabrication, so that they can be used for pick & place.

To summarize the requirements for this chapter:

[1] https://kavli.tudelft.nl/

- The chiplet should be released such that it is suitable for pick & place.
- The releasing process should be independent to the material stack
- The chiplet should remain undamaged (yield)

3.2. Releasing methods

In order for the chiplet to be released, it should be suspended to a donor chip only via its tethers. This could be realised with either a dry or wet etching approach.

3.2.1. Dry etching

Dry etching has the advantage that the selectivity for etching is high, moreover photoresist could be used to protect the vulnerable parts. Therefore, the layer stack of the chiplets could be alterned without any concern, which meets the requirements set.

The chiplets could be released by etching through the backside of a silicon substrate till the top. For this a deep silicon etch process is needed, namely the Bosch process. A machine capable of performing the Bosch process is the AMS Bosch, since it could etch silicon using Bosch etching and has the advantage of etching silicon dioxide that is often used as the hard mask for deep silicon etching.

3.2.2. Bosch etching

The Bosch process consists of two steps that are repeated after each other, till the preferred etching depth is reached.

Those steps are the following:

- **Etching** silicon with SF_6
- **Passivation** of the sidewalls with $C4F8$

During each cycle a bias voltage is used, causing the bombardment of ions to break the polymer as shown in Fig. 3.2, thus making room for the chemical to further etch through the substrate [62].

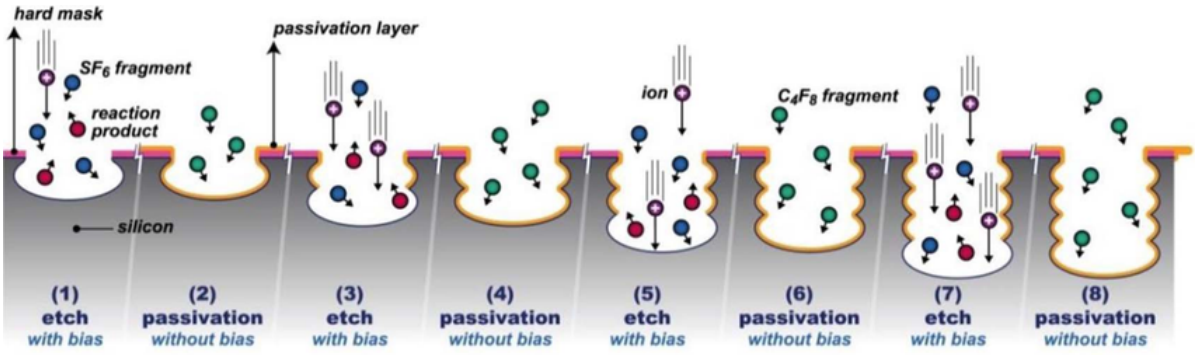


Figure 3.2: The Bosch cycling steps illustrated. Adopted from Roozeboom et al. (2015) [62].

This process could be used to release the chiplets via the backside, as depicted in Fig. 3.3. The silicon dioxide serves as the hardmask for the silicon Deep Reactive Ion Etch(DRIE). The silicon dioxide at the topside serves as the stopping layer for the Bosch process.

The last step would be to etch through the silicon dioxide dry, however the etching selectivity between silicon dioxide and silicon nitride is not very good. this means that a slight over-etch results in the reduction of the silicon nitride chiplet thickness. This problem could be solved by etching away the oxide away till there is a small layer of oxide left. This small layer could then be removed with HF, however this approach defeats the purpose of dry etching. Since all the materials in the stack should then be resistant to HF.

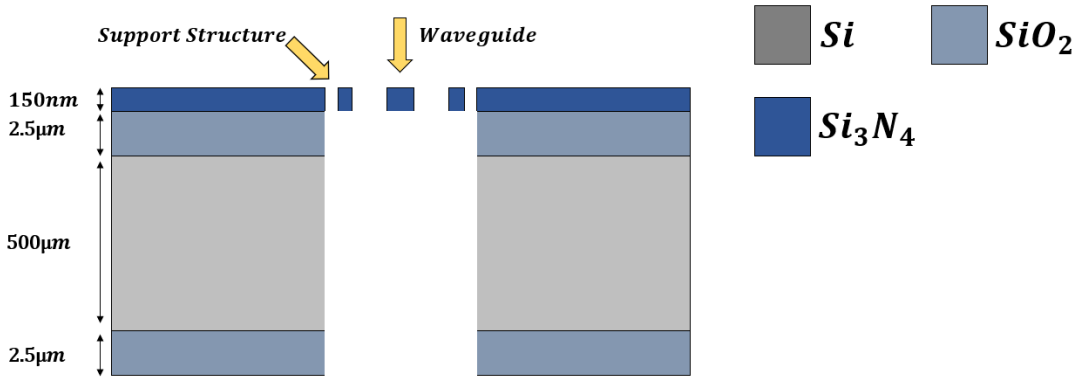


Figure 3.3: The expected layer stack after Bosch etching.

3.2.3. Wet etching

An advantage of wet etching over dry etching is that it is machine independent. This means that the setups are in general fairly simple to use. The downside of wet etching is that it could potentially attack a layer stack of the chiplet or slightly damage it under long etching times. Two most common chemicals that could be used for releasing the chiplet are hydrofluoric acid (HF) and potassium hydroxide (KOH).

3.2.4. Hydrofluoric acid (HF)

At the first glance HF seems to be a good approach for releasing the chiplets, as it is commonly used for etching SiO_2 and silicon nitride is known for its high HF etch resistivity. One could either use 40% HF or Buffered Oxide Etch (BOE). 40% HF has a higher SiO_2 etch rate than BOE(HF), while using BOE(HF) could extend the lifetime of a photoresist mask [63]. In Fig. 3.4 the best case scenario for etching with HF is shown.

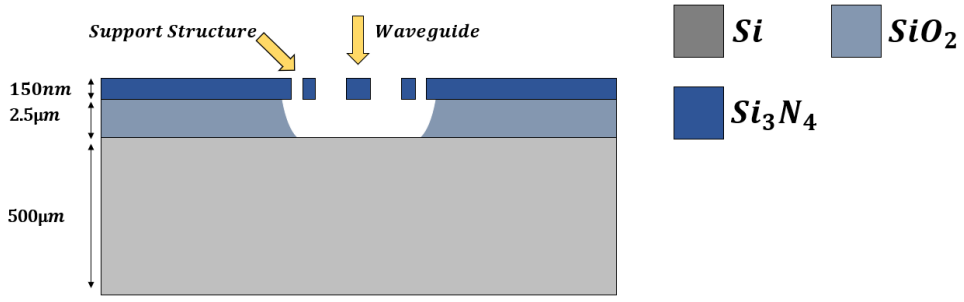


Figure 3.4: The best case scenario after HF etching.

However, this approach is not suitable for releasing the chiplets, because hydrofluoric acid affects the silicon nitride. One could of course use silicon nitride with a high selectivity to $SiO2$, resulting in minor defects [60]. Yet, this makes the recipe dependent on the type of silicon nitride used, and thus doesn't meet the requirements set. Since some types of silicon nitride are prone to HF etching, such as LPCVD stiochiometric silicon nitride [60].

3.2.5. Potassium Hydroxide (KOH)

Another option for releasing the chiplets is KOH. The selectivity between silicon nitride and silicon dioxide is insufficient for etching from above, for the same reason as previously mentioned for HF [60].

The other option would be to etch via the backside of the chip. KOH attacks silicon <100> plane, which results into a V-etch with sidewalls that forms a 54.74 degree angle, as can be seen in Fig. 3.5 [64].

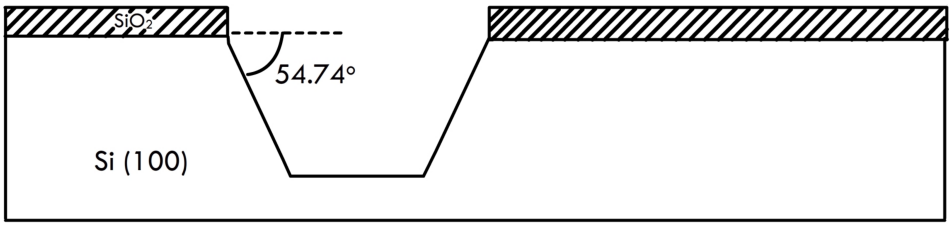


Figure 3.5: Depiction of the wet etching of Si with KOH [65].

The minimum width of the backside opening required for fully etching through a substrate with KOH:

$$W_{BacksideOpening} = 2\frac{thickness}{tan(54.74°)} + W_{Chiplet} \tag{3.1}$$

Where thickness stands for the thickness of the substrate and $W_{Chiplet}$ for the width of the chiplet.

For this approach one could use silicon nitride as a hard mask for KOH etching, because of its high KOH etch resistivity. To protect the chiplets on the topside of the sample, a holder is used that is closed off at the topside and open at the bottom, as can be seen in Fig.

3.6. Still some KOH could leak into the side of the holder that is closed off, causing KOH to etch the topside of the sample slightly.

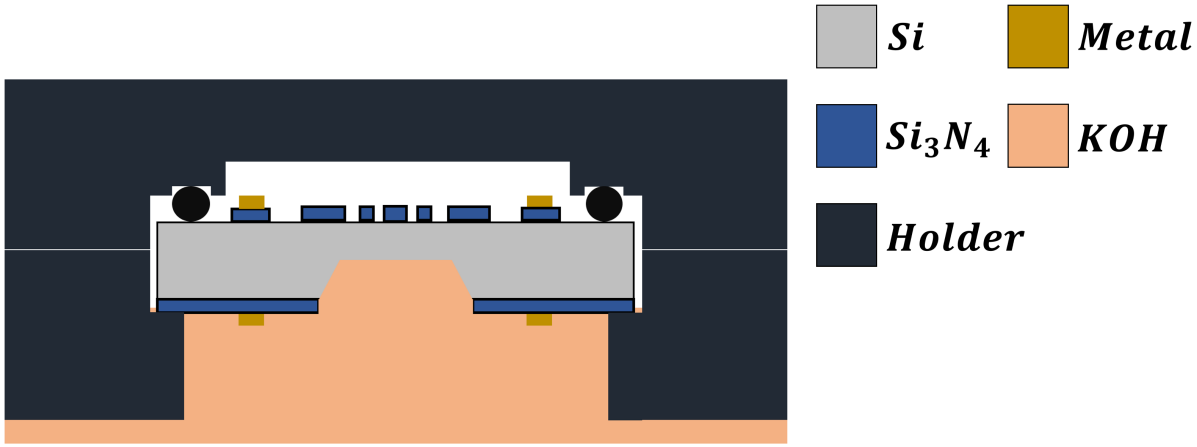


Figure 3.6: The expected layer stack after KOH etching via the backside inlcuding the holder.

3.2.6. Combining Bosch and KOH etching

The last proposed method for releasing the chiplets is a hybrid approach. The general idea of this method is to increase the density of chiplets that could be released. First, the bosch etching process will be performed till a small layer of silicon is left. Second, the remaining part of silicon will be etched with KOH, as can be seen in Fig. 3.7.

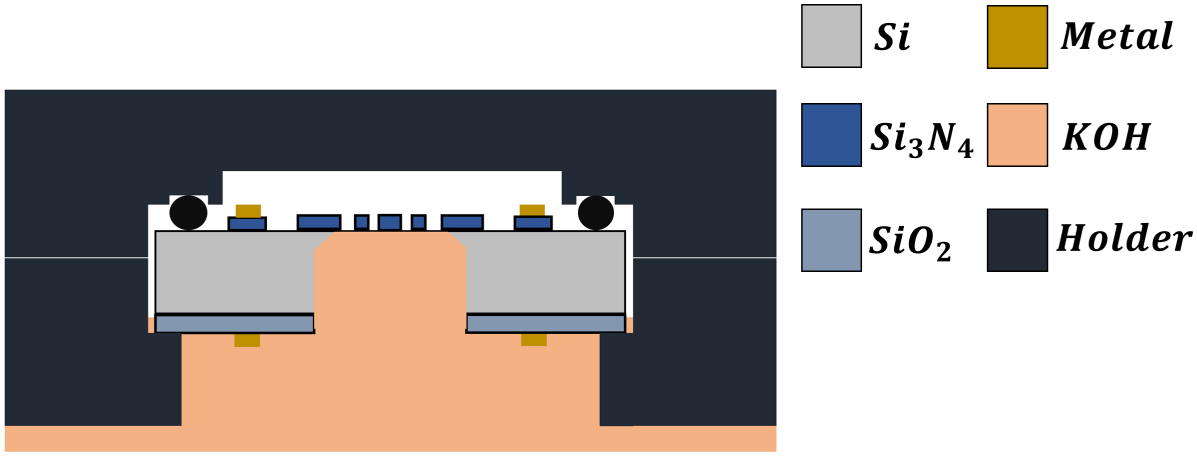


Figure 3.7: The expected layer stack after etching Bosch first and KOH second including the holder.

3.3. Backside Etching dry

Instead of fabricating the chiplets designed in Chapter 2 in-house, the fabrication of the first batch of chiplets has been outsourced. These chiplets are fabricated on a one-sided polished wafer with a layer stack consisting of Silicon (Si), Silicon Dioxide (SiO_2), Silicon Nitride (Si_3N_4) and occasionally, a Gold (Au) or Copper (Cu) layer for testing bonding in later conductivity experiments, as depicted in Fig. 3.8.

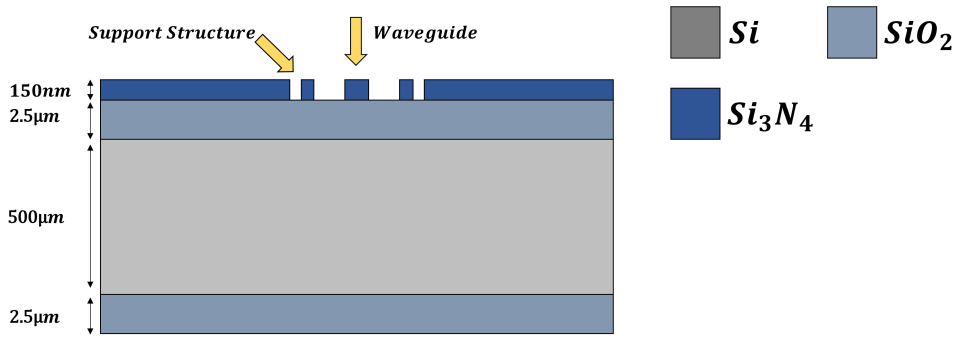


Figure 3.8: The layer stack of the outsourced chiplets.

3.3.1. Unpolished Backside

Since the first batch of chiplets has been fabricated on a one-sided polished wafer, the backside of the wafer is unpolished and thus rough. The unpolished backside is full of squares with different heights deviating sometimes with a few microns. To etch through the backside, first a photoresist mask needs to be applied for etching the silicon dioxide. Next, the silicon dioxide serves as hard mask for the deep silicon etch.

3.3.2. Silicon dioxide (SiO_2) etch

To etch silicon dioxide, S1813 is spinned at 2000RPM and baked for 1 min at 115°C to form a 2μm photomask. This is enough resist to fully etch through the silicon dioxide. Next, square patterns are patterned into the resist with a dose of 250mJ/cm^2 and a defocus of 6 using the Heidelberg microMLA Laserwriter. The resist is developed in MF21A for 1 min, while the development is stopped by dipping it in H_2O for 30 seconds. Afterwards, the silicon oxide is fully etched through using the AMS Bosch.

Etching through the unpolished backside causes SiO_2 islands to form. The first thought was that the etch time was not long enough, therefore the next sample was etched for twice as long. This however did not solve the problem, as the island still appeared. The second thought was that either unexposed or developed resist was preventing the islands to be etched. Therefore, descuum and longer development was tried. This however did also not prevent the islands from forming. Exposing the same pattern twice with the laserwriter seemed to reduce the amounts of islands forming slightly, however still lots of islands were present after the silicon dioxide etch, which prevents the silicon from being etched underneath during the next step of Bosch etching.

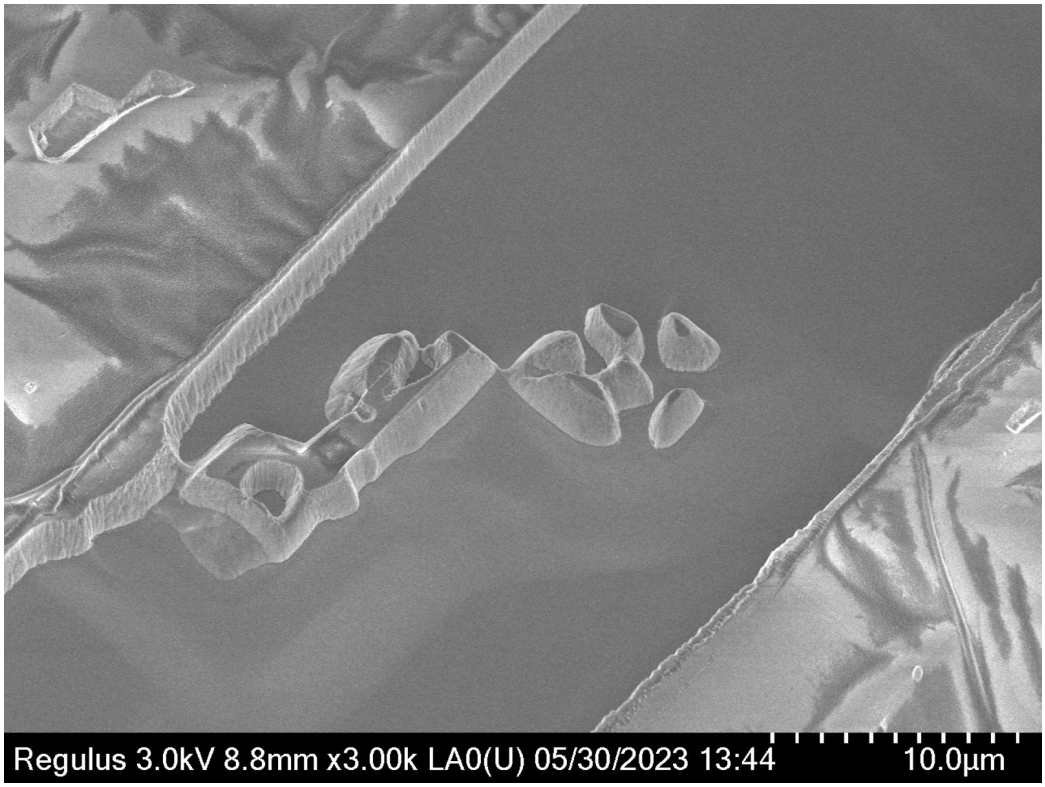
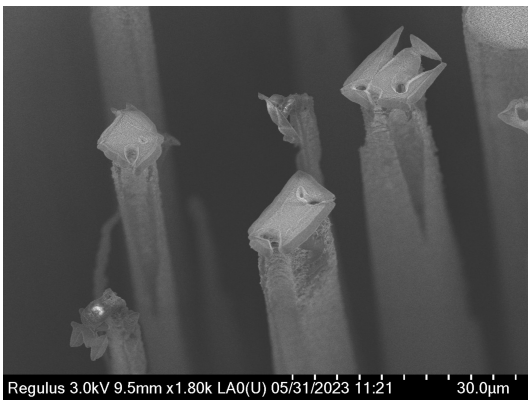


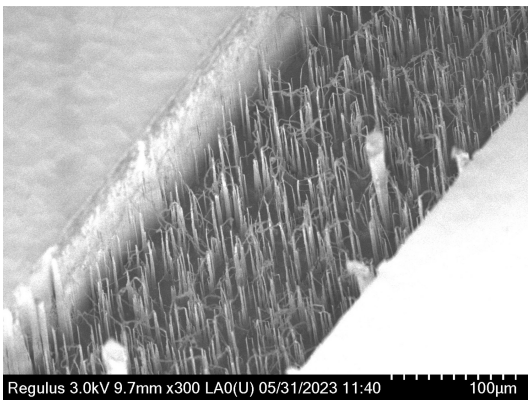
Figure 3.9: Silicon dioxide islands after etching 2.5μm..

3.3.3. Silicon etch

During the first attempt of etching the silicon, although silicon dioxide islands were present, the sample was etched for 250μm in the AMS Bosch. This resulted in the forming of silicon pillars with a silicon dioxide layer at the top and the forming of grass, as can be seen in Fig. 3.10.



(a) Pillar forming



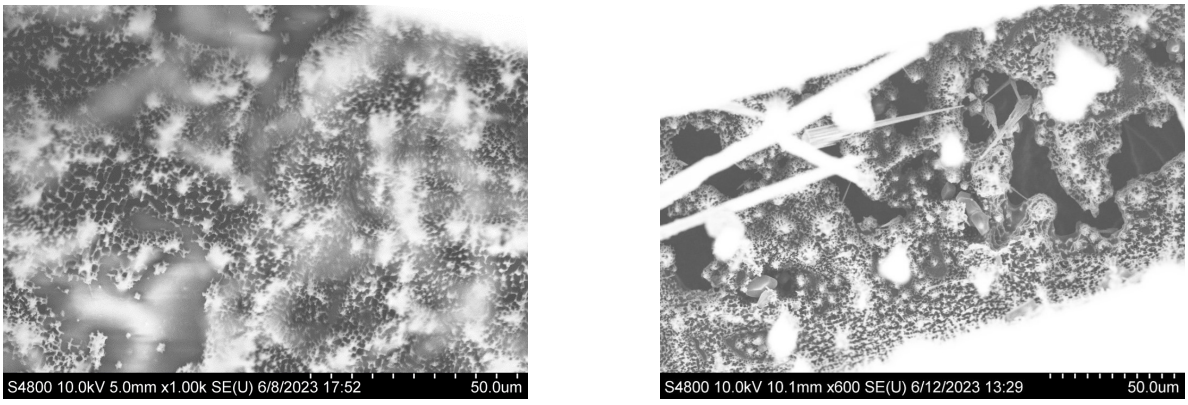
(b) Grass forming.

Figure 3.10: Backside etching for 250μm on an unpolished sample.

During the second attempt, the goal was to etch fully through the silicon 500um-thick sample until the silicon oxide stopping layer was reached. This resulted in a snowy landscape of

either silicon or silicon dioxide, and it was possible to look through the sample. Therefore, HF was used with the hopes of etching through the stopping layer. This approach did not work, as the stopping layer looked like a mess afterwards, meaning that the leftovers are silicon, as can be seen in Fig. 3.12.

Since etching through an unpolished backside, does not result in a clean stopping layer with good sidewalls, and without the forming of grass and pillars, we chose to make the chiplets in-house. By doing so there is more freedom in the choice for the layer stack. Additionally, a KOH approach could now be considered.



(a) Snowy stopping layer.

(b) Snowy stopping layer after HF.

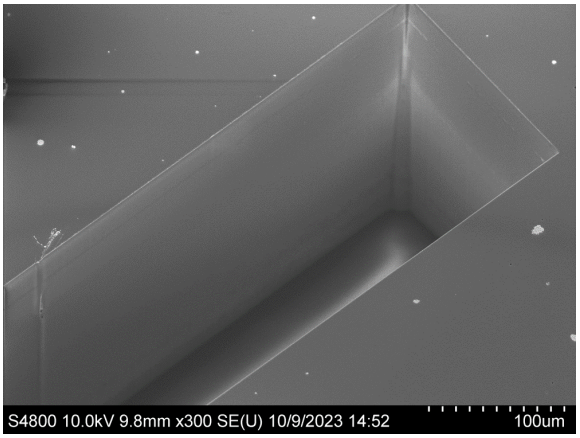
Figure 3.11: Backside etching fully through a 500μm-thick unpolished sample.

3.3.4. Polished Backside

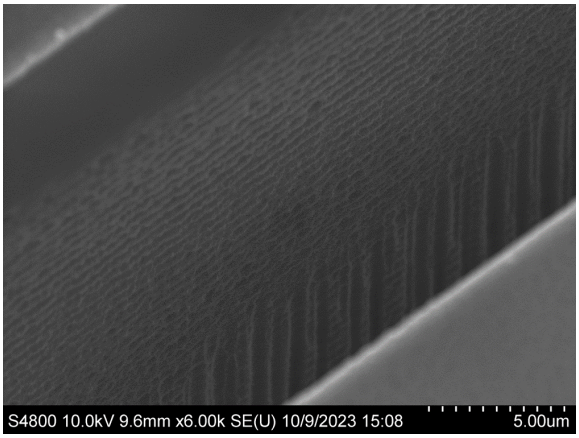
Now, that there is more freedom in the layer stack, as the chiplets are fabricated in-house. It has been chosen to use thinner wafers for the backside etching. Using 300μm-thick wafers instead of 500μm-thick wafers decreases the total etch time by 40%. Also, at this moment the AMS Bosch broke down, and has not been up since. Meaning other options had to be explored. One of these was etching in EKL.

Hande Aydogmus[2] performed both the silicon dioxide and deep silicon etch using the Rapier. This resulted in good side walls, a clean silicon dioxide stopping layer and no grass and pillars forming. We have not yet experimented with the removal of the silicon dioxide stopping layer.

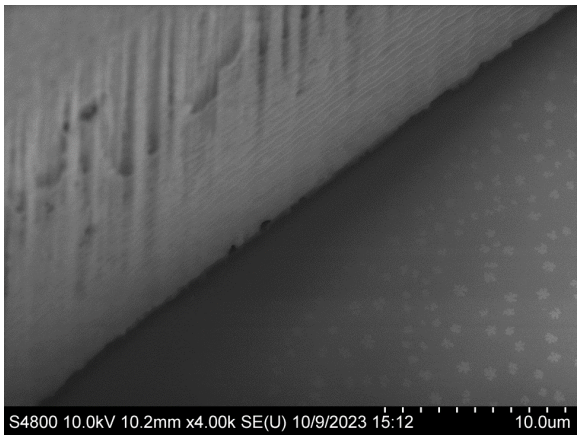
[2]PhD Student at Electronic Components, Technology and Materials, TU Delft, the Netherlands.



(a) No grass and pillars.



(b) Good looking sidewalls.



(c) Clean stoppinglayer.

Figure 3.12: Backside etching through a 300μm-thick polished sample.

3.4. Backside etching wet

In this alignment markers are introduced to align the top and bottom side of the chip, ensuring that the backside etching is done at the correct location for reaching the chiplets. These are fabricated on top of the already existing materials stack consisting of a 300μm double-sided polished wafer with 170nm of annealed PECVD silicon nitride on both sides of the wafer, as can be seen in Fig. 3.15.

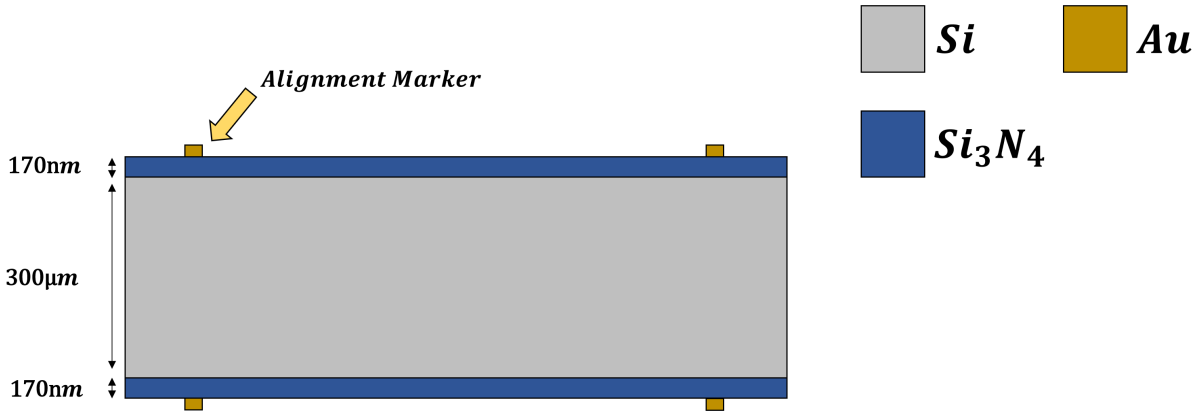


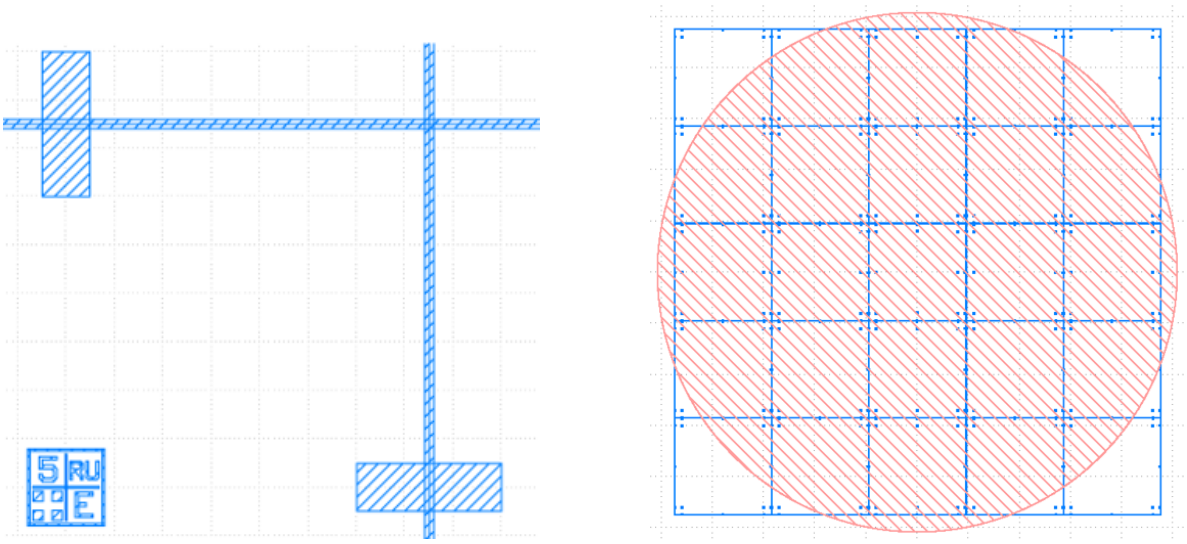
Figure 3.13: The material stack of the KOH etching experiment.

3.4.1. Mask design

For the alignment markers it is important that the markers at the top of the sample are well aligned with the markers at the bottom of the sample with a misalignment tolerance of only a few micrometers. A machine that is able to do such backside alignment is the EVG-620 NUV. This machine requires a photomask and uses two microscope for backside alignment, and a minimum separation of 8mm between them is required.

The first mask was designed for the first batch of chiplets as mentioned earlier. These samples are 10mmx10mm, hence it was expected that the minimum separation distance between the microscopes wouldn't cause a problem. However, it turned out to be pushing the machine's limit. Next to this, using a small sample for backside alignment resulted in a scratched mask plate. Increasing, the separation distances between the mask and the sample did not prevent the mask from being scratched. Using a 5" mask plate instead of a 4" mask plate for wafer scale backside alignment solved the scratching issue.

As mentioned earlier the updated mask is meant for the alignment of wafers. This mask is designed with features that simplify the backside alignment process. These lines and pads are used to indicate when an alignment marker is close by, but also serve the purpose of diving the wafer into 19mmx19mm samples for dicing, as can be seen in Fig. 3.14.



(a) Alignment marker.

(b) Lines indicate 19mmx19mm samples.

Figure 3.14: The gdsII design of a 5" mask plate for backside alignment.

3.4.2. Alignment markers

Ideally, the metal used for the alignment markers is the same as the metal that is going to be used for the contact pads of the SNSPD's. However, since the metal choice for the contacts pads is still unknown, gold has been chosen for the alignment markers. The reason for this is that gold deposition and lift-off are relatively straightforward. Since the aim was to test the chiplets as fast as possible, the simplest and fastest method had the priority.

Of course, gold can lead to contamination issues into the quantum chip. Therefore, it is important to note that the metal of the alignment markers could still be changed to the metal that is going to be used for the contact pads. Another pro of using gold is that gold does not get etched by KOH [60].

At first S1813 was used to lift-off the gold evaporated by the AJA QT. However, gold leftovers remained on the substrate when it was lift-offed by acetone. Adding LOR5B as lift-off resist under the standard resist S1813, and using NMP to lift-off gold instead resulted in high quality markers with minor defects.

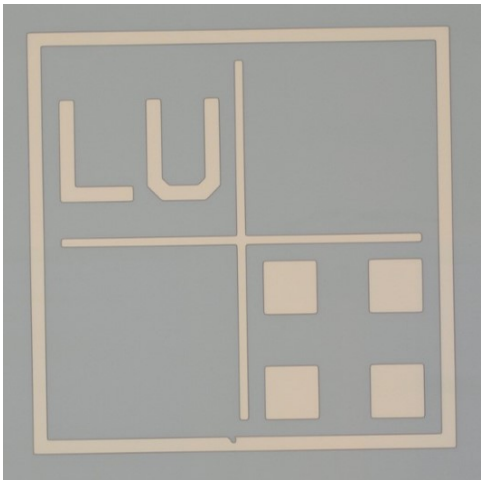


Figure 3.15: A gold alignment marker with minor defects.

3.4.3. KOH etching

Etching each chiplet separately with KOH requires a great a area, therefore to increase the amount of chiplets that could be released, the chiplets have been fabricated in arrays that could be etched.

The holder that is used to protect the chiplets on the topside and allows KOH to etch via the backside is shown in Fig. 3.16. The etchant at the surfaces could become saturated, therefore a rotating magnet is placed under the holder to stir the solution, ensuring fresh etchant reaches the surface and accelerates the etching [64].

Figure 3.16: The holder used for KOH etching.

During the first attempt of releasing the chiplets with KOH, we did not manage to release

the chiplets, because of the following reasons:

- The substrate holder was made for 500μm thick samples, while for this experiment 300μm substrate were used. This caused KOH to etch the topside, however most of the structures managed to survive.
- The etching time was to short for etching through the substrate.
- The silicon nitride openings at the back of the sample, where located to close to each other. This resulted in holes between the silicon nitride openings.

These problems were solved for the next attempt. During this second attempt the sample broke down in several pieces, because the silicon nitride mask did not manage to withstand the long KOH exposure.

Therefore, for the third and final attempt, a 150nm PECVD silicon nitride layer was deposited on top of the existing layer of silicon nitride on the backside of the sample. During this attempt the silicon nitride mask did survive. Furthermore, the substrate was fully etched through and most of the silicon nitride structures were hanging on their breaking tethers, as can be seen in Fig. 3.17. This means that the liftoff and thus the release of the silicon nitride structures was successful.

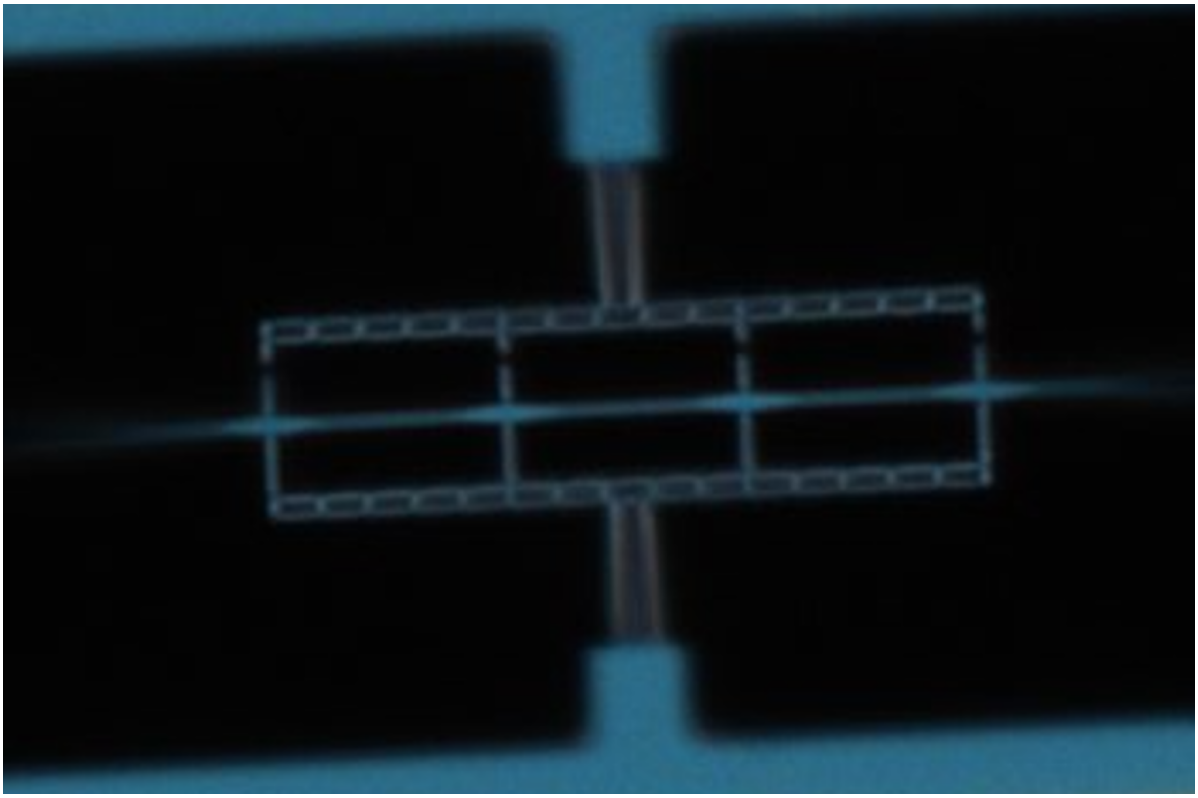


Figure 3.17: A silicon nitride structure that is suspended by its tethers after KOH etching.

3.5. Conclusion

In this chapter we proposed different methods for releasing the chiplets designed in Chapter 2. Bosch etching for releasing the chiplets resulted in a clean silicon dioxide stopping layer

that still has to be removed before the chiplets can be released. KOH etching together with a holder that prevents the chiplets from being etched independent to the material stack used resulted in silicon nitride structures that could be pick & placed. The chiplet density of the KOH approach could be increased by combining Bosch and KOH etching.

4

Pick & Place

This chapter covers the topic of Pick & Place. It is the third and final part of the thesis as can be seen in Fig. 4.1, before we will conclude and discuss our findings.

Previously, the chiplet was designed and fabricated. In this chapter the chiplet will be pick & placed. However, since the chiplet was not ready at the start of the project, diamond test chiplets where used to determine the misalignment of the placed chiplets. Next to the misalignment measurements, also contact angle measurements where performed to test the effect of surface treatments on the receptor chip. Lastly, the silicon nitride structures have been pick & placed.

Figure 4.1: The flowchart of the project highlighting the current chapter: Pick & Place.

4.1. Requirements

In Chapter 2 we have simulated the misalignment tolerances for butt & tapered waveguide endings. From these simulations we have found out that having a misalignment of 50nm or less between the chiplet and the waveguide results in a coupling efficiency greater than 90%.

During the pick & place process it is important that the chiplet doesn't break. Not only because the chiplet cannot be used for the detection of single photons, but also to prevent the fabrication yield to be too low, because the SNSPD fabrication yield is already expected to be low.

To summarize the requirements for this chapter:

- The chiplet should be placed with a maximum misalignment tolerance of 50nm relative to the waveguide.
- The chiplet should not break during the pick & place process. (yield)

4.2. Setup

To pick & place the waveguide structures a a customized setup was designed from scratch by Alan Yu[1]. The schematic of the setup can be seen in Fig. 4.2. The needle that will be used for the pick & place has to be controlled in the X-, Y- and Z-axis so that the chiplet can be assembled. This needle has to be controlled with a resolution sufficient enough to place the chiplet comfortably, therefore the Eppendorf TransferMan 4r 519300012 was used as the micromanipulator, which can be controlled by a joystick. The samples are placed on top of 4 piezo stages. These piezo stages are used to bring the sample under the objective and can be controlled in the X-, Y- and Z-axis, while it can also be used to rotate the sample using the ZABER X-RSW60C-E03. The piezo stages in the X- and Y-axis have 47.6nm stepsize, since the ZABER X-LSM100A is used. The Olympus STM7 is used as the microscope. This microscope can be manually controlled and has a camera that is connected to a screen, which has the advantage of making pictures and videos of the placements. Everything is build upon an air stabilized optical table to prevent the setup from being hindered by vibrations.

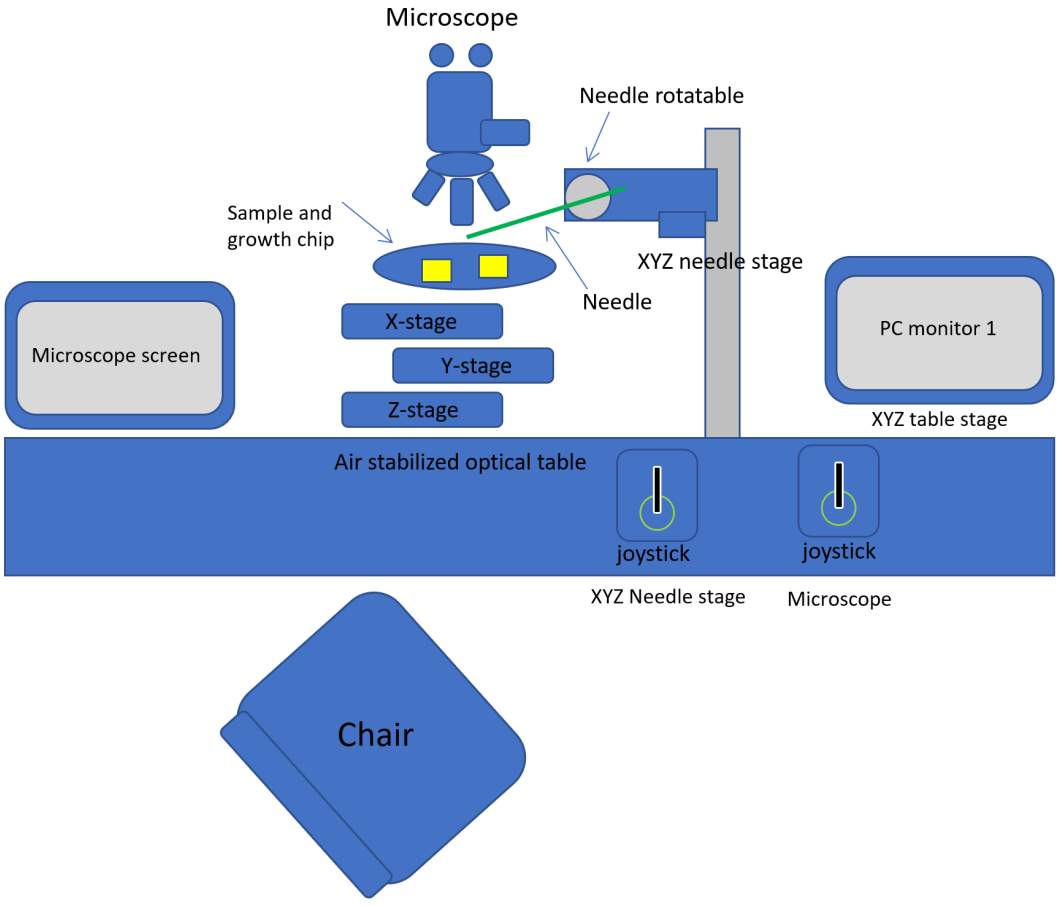


Figure 4.2: The setup customized setup for pick & place.

The zoomed in version of the setup can be seen in Fig. 4.3. It shows the donor chip, receptor chip, tungsten needle, objectives and a piezo stage.

[1]PhD student at Ishihara lab, QuTech, Delft University of Technology, Delft, the Netherlands.

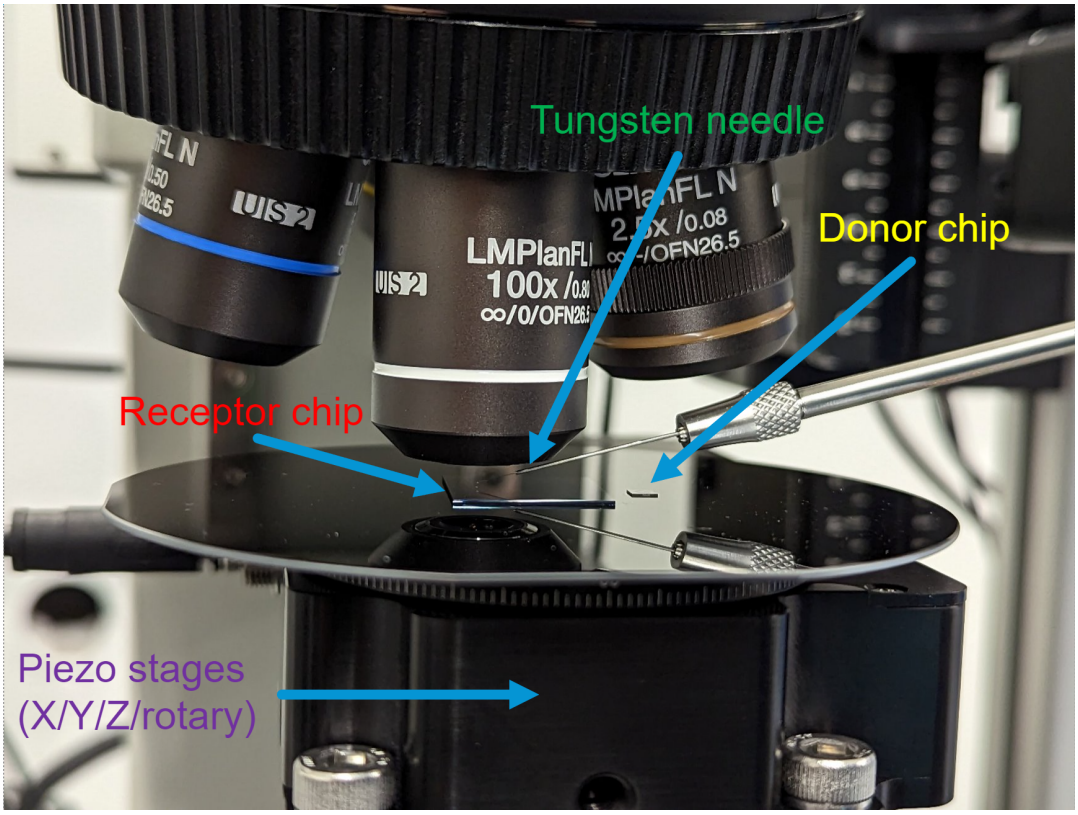


Figure 4.3: The zoomed in setup for pick & place. Consisting of a; Donor chip containing chiplets, Receptor chip with SiN waveguides, Tungsten Needle, Objective and Piezo stages.

4.2.1. Donor chip

On the donor chip, chiplets that should be pick & placed are present. To test the pick & place process, diamond chiplets were used first, because the SiN chiplets were not ready to be pick & placed yet. The diamond chiplets, however, could not be fabricated on our, hence the number of chiplets available was limited.

4.2.2. Receptor chip

On the receptor chip, the chiplets should be placed. The receptor chiplet contains SiN waveguides, on which the diamond and silicon nitride test chiplets could be placed.

4.2.3. Tungsten Needle

The Tungsten Needle has a tip diameter of 200nm and is prone to breaking. However, because of the design, the broken needle can be replaced relatively easily.

The needle is attached to the motor module of the Transferman 4r and can be manually controlled by the joystick on the corresponding control board. The motion of the needle can be controlled in the X-, Y- and Z-direction with a calculated step size resolution of $< 20nm$.

4.2.4. Objectives

The objectives used for the pick & place setup have the following magnifications: 2.5x, 5x, 20x, 50x and 100x. The focus can be adjusted by moving the objectives up or down. However, since the needle and substrate are mostly located at different heights, it is not possible to have both of them in focus during the start of the process. When the needle approaches the height level of the substrate, only then both the needle and substrate could be in focus at the same time.

4.3. Process

The pick & place process itself consists of 3 steps:

- Focus procedure
- Picking up
- Placing down

4.3.1. Focus procedure

To focus the objective on the location of interest, it is important to move the piezo stage so that the substrate with the location of interest is directly under the objective. It is also important to have the needle focal plane close to the substrate focal plane. If that is not the case, move the needle down and/or move the piezo stage holding the substrate up.

The next step would be to get the needle in focus under the 2.5x objective by adjusting the height of the objective. Once the needle is in the middle of the objective and in focus, the location of interest could be made into focus by adjusting the height of the objective and by moving the piezo stages so that the location of interest is exactly in the middle. If it is difficult to focus on the substrate, it is recommend to first focus on the edge of the sample.

The following action would be to increase the magnification gradually up to 100x. When doing so, the location of interest and the needle should be adjusted to the middle of the plane, before moving on to the next magnification.

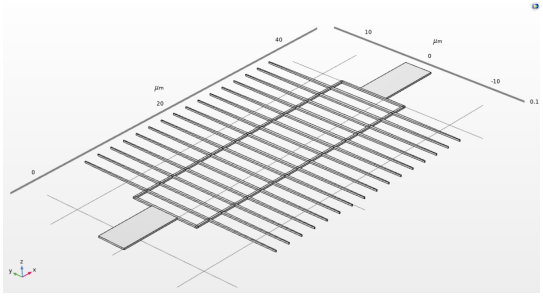
It is important to note that it is possible to see the reflection of the needle under the objective, hence always make sure to have the correct plane of focus.

4.3.2. Picking up

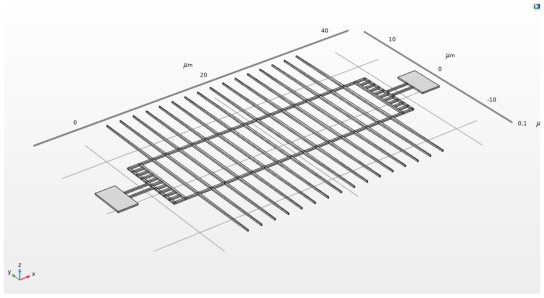
During the picking up phase, the chiplet should be picked up from the donor chip. However, the chiplet is attached to the donor chip via breaking tethers that should be broken first, before the chiplet could be picked up.

To test which breaking tethers are the easiest to break, three different suspension versions were made for the diamond test chiplets, as can be seen in Fig. 4.4. After trial and error of multiple chiplets, Jean Claude Rihani[2] concluded that version 2 & 3 were the easiest to pick up, hence having a breaking tethers is preferred over having none.

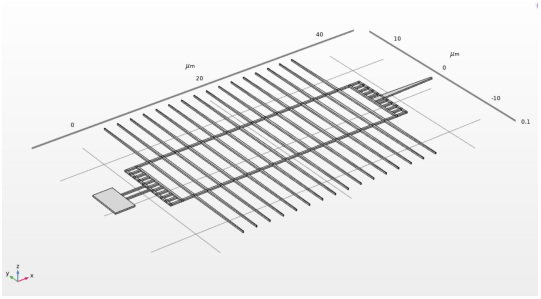
[2]Bachelor Internship at Ishihara lab, QuTech, Delft, the Netherlands.



(a) Version 1 isn't suspended with tethers.



(b) Version 2 is suspended with 2 tethers connected to each side.



(c) Version 3 is suspended with 2 tethers connected to one side.

Figure 4.4: 3 versions of diamond chiplet suspensions.

There are two approaches on picking up the chiplet. The chiplet could either be picked up from above or from under. The reason for exploring these options is the rough backside of the diamond chiplet. The chiplet sticks to the needle because of the van der Waals forces acting between the needle and the chiplet. Having a rough backside would make it more difficult to release the chiplet from the needle, because the van der Waals forces acting between the receptor substrate and the rough backside of the diamond chiplet would be less than having a smooth topside. Hence in the approach of picking up the chiplet from under there is a step where the needle is rotated by 180°, so that the smooth topside would be upside down and in contact with the receptor substrate instead.

Apart from having the rough side up, there are no advantages for picking up the from under. In the contrary, there a lot of disadvantages compared to picking up the chiplet from above. Picking up the needle from under as the increase risk of losing or breaking the chiplet, therefore the yield would be lower and that violates our requirements set for pick & place. Another disadvantage is the increased risk of bending or breaking the needle, due to the needle being moved under the chiplet and thus having a higher chance to come in contact with the donor chip.

4.3.3. Placing down

Before the chiplet could be placed down the receptor chip has to be under the needle and focal plane first. By moving the piezo stages, the receptor chip is moved under the objective, while the needle remains at the same place.

Now, it is time to align and place down the chiplet onto the receptor chip as shown in Fig. 4.5. When lowering the needle with the chiplet to the SiN waveguides, three things could happen: the chiplet may attach to the substrate, the chiplet may start shivering, or the chiplet may adhere to the side of the needle.

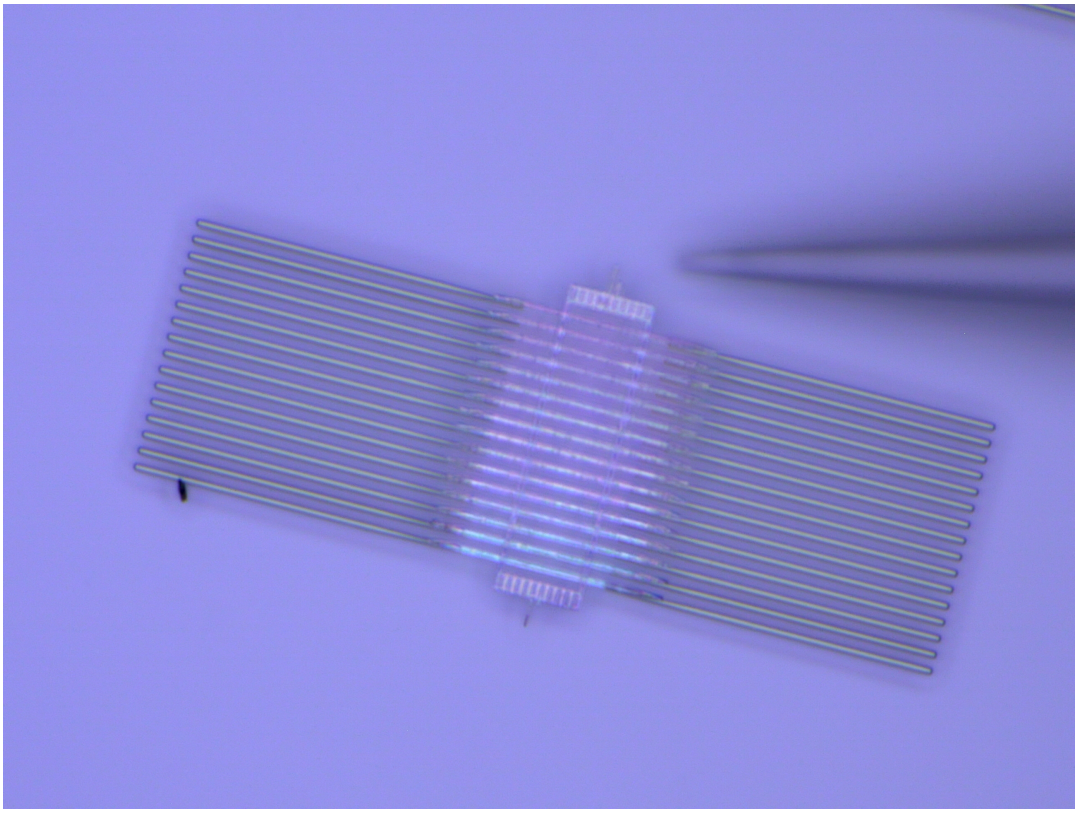


Figure 4.5: A diamond chiplet placed onto SiN waveguides of the receiver chip.

4.4. Surface Treatment

Increasing the surface energy by surface treating the receptor chip could potentially solve the shivering and improve the adhesion of the chiplet to the surface. Surface energy arises when two surfaces touch due to short-range intermolecular interactions, such as van der Waals and Coulomb forces.

Van der Waals

Van der Waals forces contain 3 types of interactions [66][67]:.

- **Keesom interactions:** Permanent dipole-permanent dipole
- **Debye interactions:** Permanent dipole-induces dipole
- **London interactions:** Induced dipole-induced dipole

For two surfaces the van der Waals forces are dependent on the distance, medium and surface roughness [68][69], which gives

$$F_{vdW} = -\frac{A_{123}}{12\pi h^2} \tag{4.1}$$

where A_{123} is the Hamaker constant and h is the height separation. The hamaker constant contains the surfaces marked as 1 & 3 and a medium marked as 2, as given in

$$A_{123} = A_{u=0} + A_{u>0} \approx \frac{3kT}{4}\left(\frac{\varepsilon_1 - \varepsilon_2}{\varepsilon_1 + \varepsilon_2}\right)\left(\frac{\varepsilon_3 - \varepsilon_2}{\varepsilon_3 + \varepsilon_2}\right) + \frac{3hu_e}{8\sqrt{2}} \frac{\left(n_1^2 - n_2^2\right)\left(n_3^2 - n_2^2\right)}{\sqrt{n_1^2 + n_2^2}\sqrt{n_3^2 + n_2^2}\left\{\sqrt{n_1^2 + n_2^2} + \sqrt{n_3^2 + n_2^2}\right\}} \tag{4.2}$$

where ϵ_i and n_i are the dielectric constants and the refractive indices of the respective materials. The Keesom and Debye interactions represent the first two terms, while the London interaction desribes the last term in the Hamaker constant equation.

Coulomb
The Coulomb forces acting on the two charged particles is inversely proportional to the square of the distance between the centers of the particle [70], which gives

$$F_C = \frac{k_e q_1 q_2}{r^2} \tag{4.3}$$

where

$$k_e = \frac{1}{4\pi\epsilon_0} \tag{4.4}$$

is the coulomb constant.

4.4.1. Surface Treatments

To test the effect of surface treatments on the receptor chip. The following treatments were performed:

No treatment: This was used as a reference sample for the other treatments.

HMDS: Hexamethyldisilazan (HMDS) was used with to hope of removing impurities and making the to make the hydrophilic wafer hydrophobic. This was done by heating the wafer for removing the water, and then exposing it to HMDS as the hydroxylgroups will react with the methyl groups, as can be seen in Fig. 4.6.

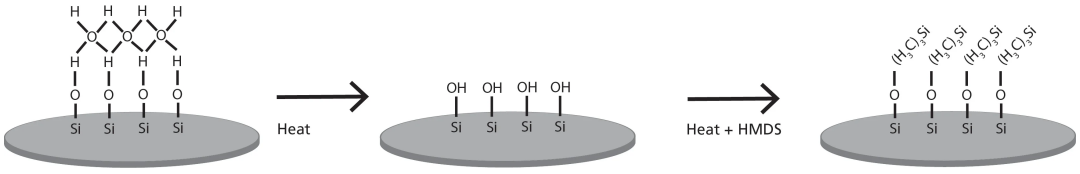


Figure 4.6: The HMDS treatment process. Adopted from Laurén (2021) [71].

HMDS removed by BOE(HF): After removing the HMDS by using BOE(HF) 45:1 to reuse a sample for pick & place, the adhesion of the chiplet to the receptor chip seemed

to be different, therefore two approaches for removing the HMDS are tested. HF tends to smoothen the silicon wafer and making the surface hydrophobic [72][73].

HMDS removed by oxygen plasma: The other approach for removing HMDS is oxygen plasma. Oxygen plasma also tends to increase the wettability, hence the surface becomes more hydrophilic [74]. The $O2$ Tepla was used for this.

4.4.2. Contact angle measurements

To determine the effect of the surface treatments on the surface energy of the receptor chip, contact angle measurement were performed. The concept of a contact angle measurement is simple. A drop of liquid placed on top of a solid surface and forms a droplet. The surface energy of the substrate will be high if the contact of the droplet and the surface is small, and if the angle is large the surface energy will be low.

4 samples of a double-side polished wafer with silicon nitride PECVD deposited on both sides and 4 pieces of a wafer with silicon nitride LPCVD deposited on one side have been cleaned using Acetone/IPA. Next the surface treatments were performed on the samples and the surface energy was measured using the OCA20 measuring device.

The results of these measurements can be seen in Table 4.1. It shows that HMDS and BOE(HF) treatmens do not seem to affect the surface energy in a significant amount, while O2 plasma seems to reduce the surface energy, especially for PECVD silicon nitride. Also the surface energy difference between the top and bottom side of a double-side polished wafer is noteworthy.

Table 4.1: Surface energy results of the performed surface treatments.

Surface Energy (mN/m)	PECVD (Top)	PECVD (Bot)	LPCVD
No treatment	53.55	43.06	48
HMDS	59.37 (no HMDS)	41.61	43.92
HMDS removed by BOE(HF)	56.35	40.97	42.51
HMDS removed by O2	35.67	30.40	41.59

Also the polar term of the PECVD silicon nitride seems to drop with oxygen plasma treatment, as can be seen in Table 4.2. The other treatments do not seem to affect the polar and dispersion term.

Table 4.2: Surface energy results of PECVD silicon nitride including the dispersion and polar term.

PECVD Silicon Nitride	Surface Energy (mN/m)	Dispersion (mN/m)	Polar (mN/m)
No treatment	43.06	11.89	31.17
HMDS	41.61	7.50	34.12
HMDS removed by BOE(HF)	40.97	11.03	29.93
HMDS removed by O2	30.40	7.70	22.70

4.4.3. Placement results

On each receptor substrate at least four diamond chiplets placements were performed. For each placement the adhesion and manoeuvrability of the diamond chiplet to the receptor substrate have been given a grade from 1 to 5 by Ravi Gopie[3], where a grade of 1 means bad adhesion or difficult to manoeuvre and a grade of 5 means good adhesion or easy to manoeuvre the chiplet. It is important to note that the pick & place operator was unbiased, since he did not know which substrate underwent which treatment.

Next to the adhesion and manoeuvrability, the picking up and placing down phase of the chiplet have been timed. As well as the percentage of the chiplet that broke during the process. The average data of the placement measurements per receptor chip can be seen in Table. 4.3. And the following observations were made:

No treatment: The diamond did not stick well to the receptor chip and repositioning the chiplet was difficult, therefore the time it took for placing it down was relatively high compared to the other receptor substrates.

HMDS: The diamond chiplet did stick well to to the receptor and could be repositioned easily.

HMDS removed by BOE(HF): The adhesion and manoeuvrability was good, however tends to flip during the repositioning of the chiplet, which causes it to break.

HMDS removed by oxygen plasma: The chiplet had bad adhesion to the substrate and started to shiver during the placing down process. Once it was placed down it could be repositioned.

[3]Bachelor Thesis at Ishihara lab, QuTech, Delft, the Netherlands.

Table 4.3: Surface treatment placement results.

	Picking up(s)	Placing down(s)	Adhesion	Manoeuvrability	Breakage($\%$)
No treatment	152.2	889.8	2	2.5	2.4
HMDS	83.8	500.1	3.25	4	3.25
HMDS removed by BOE(HF)	38.4	332.9	3.6	3.6	20.6
HMDS removed by O2	83.8	444.1	2.25	3	13.3

Another observation was made when wet droplets were coincidentally present on a receptor chip. The wet droplet functioned as a temporary glue for the chiplet. Therefore, the chiplet could be repositioned without the danger of it flying away and breaking.

Furthermore, the diamond chiplets tend to be placed with their smooth side down and rough side up as can be seen in Fig. 4.7. This can be explained by the fact that the van der Waals forces are stronger acting between the chiplet and the receptor substrate are stronger for the smooth side than the rough side.

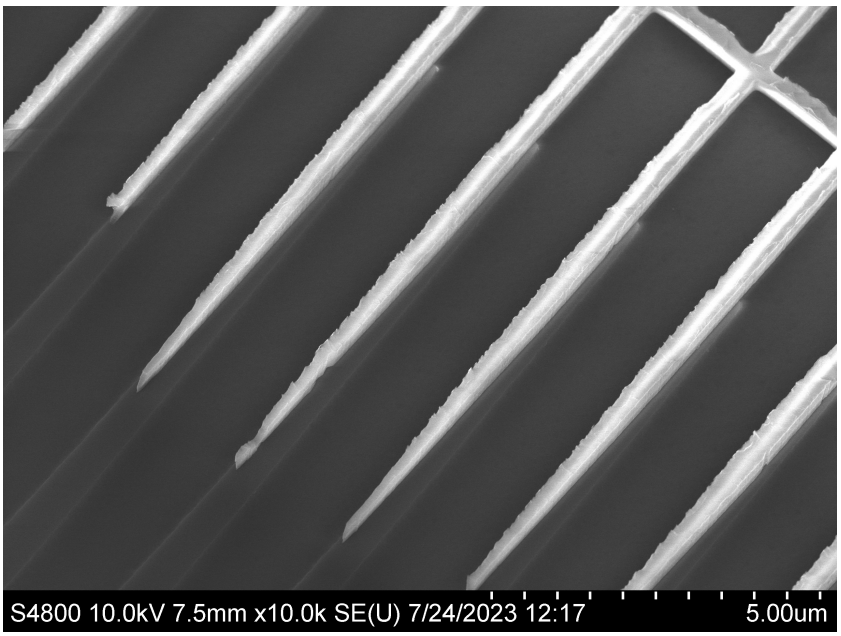


Figure 4.7: A placement of a diamond chiplet with the rough side up.

Lastly, the misalignment of the chiplets has been measured by analyzing SEM images of the placements. As the placements are also dependent on the angle, only the misalignment from one side taper of the crossing has been plotted against the time it took to place the diamond chiplet down. In Fig. 4.8 it can be seen that there is a correlation between the misalignment and the time it takes to place down the diamond chiplet. Furthermore, a misalignment of 50nm has been achieved on a receptor substrate that had its HMDS removed by oxygen plasma.

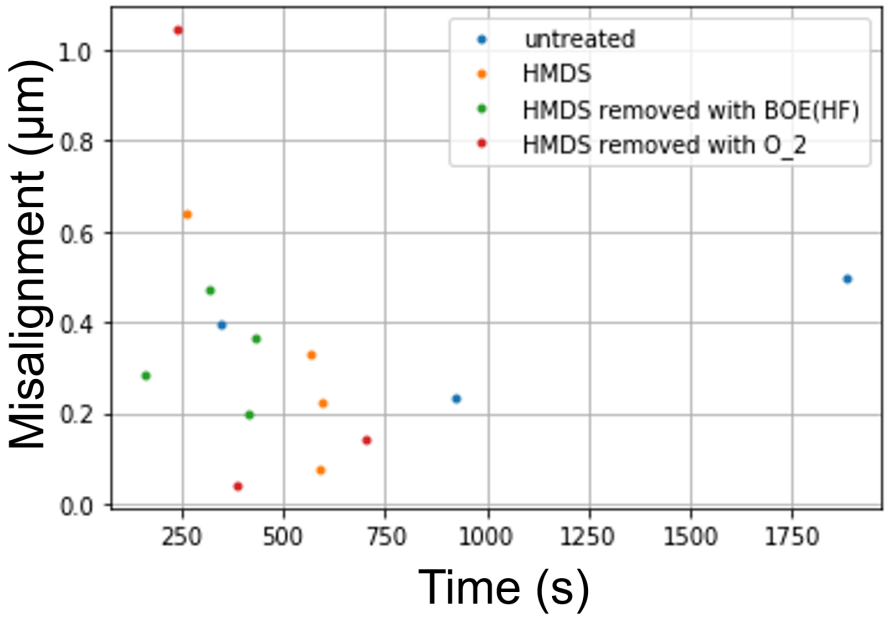


Figure 4.8: Misalignment of the diamond chiplet plotted against the time it took to place the chiplet.

4.5. Silicon nitride structures placements

Lastly, the fabricated silicon nitride structures were pick & placed. Picking up the structures with a needle that has a 100nm tip was not doable. It did not stick to the needle and was very flexible. Therefore, breaking the supporting tethers was not possible, unless broken from below, however then the it falls into the KOH etched hole as the structure did not stick to the needle tip. Another possibility is that the structure is hanging as a bridge over the KOH etched gap, as can be seen in Fig. 4.9. Still it was not possible to pick it up with a 100nm tip width needle.

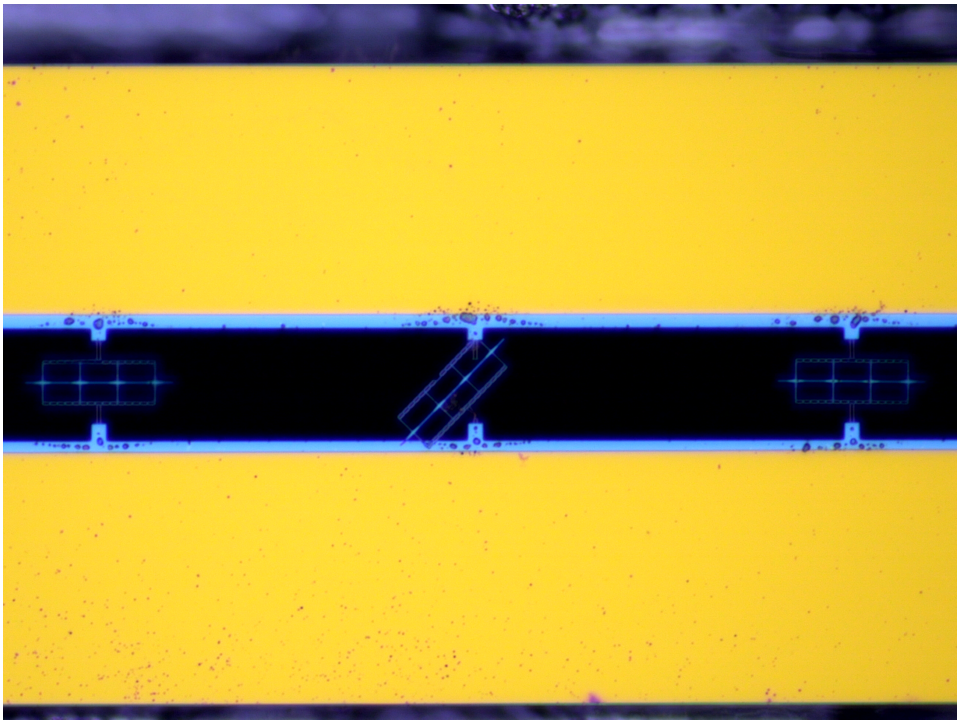


Figure 4.9: Silicon nitride structure hanging over the KOH etched gap.

Using a tip with of 10μm it was possible to pick up a silicon nitride structure in some cases. However, when moving the needle from the donor chip to the receptor the structure has a high chance of falling of. Despite all the inconveniences, some structures could be placed on the receptor chip, as can be seen in Fig. 4.10. The silicon nitride structures stick well to the surface and could be repositioned using a needle with a 2μm tip width, since a tip width of 10μm is to big for repositioning. Unfortunately, no measurements could be performed, because the structures were made from silicon nitride with bad optical qualities.

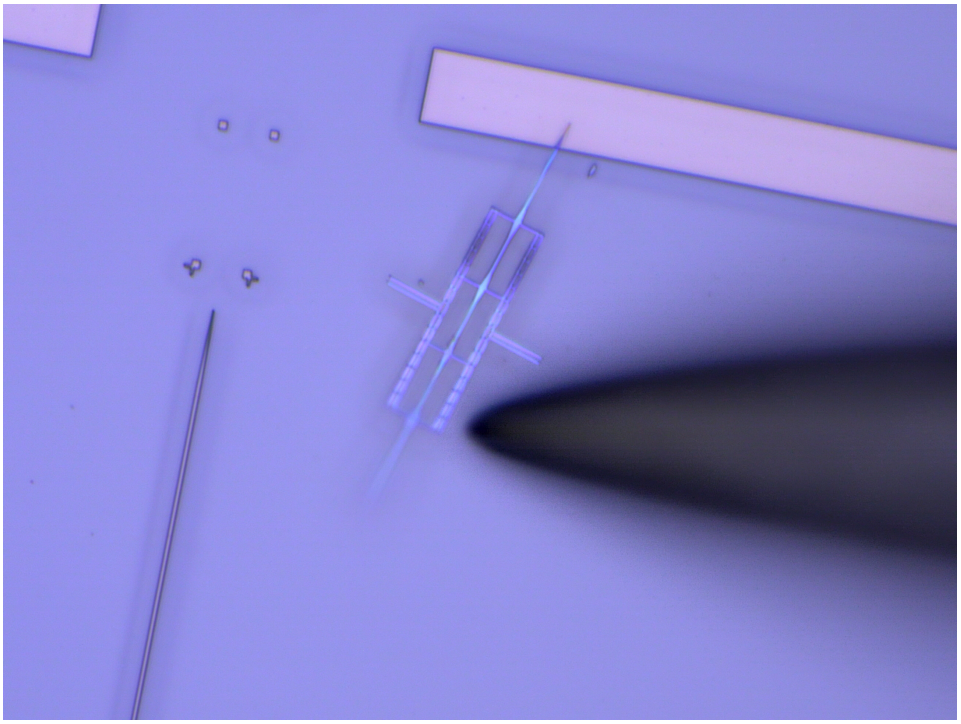


Figure 4.10: Silicon nitride structure placed on the receptor chip.

4.6. Conclusion

In this chapter we found out that picking up chiplets from the topside has the preference over picking it up from under. However, the diamond chiplets tend to be placed with the rough side up, and smooth side down. The surface treatments performed do influence the surface energy of the receptor chip and the chiplet placement. The chiplet also had a higher chance of breaking dependent on what surface treatment was used. Using a wet droplet could prevent the chiplet from flying away and breaking when the needle is used to reposition the chiplet, however this has to be explored more, since it could increase the placement yield as well as the alignment. The maximum misalignment requirement of 50nm has been achieved once with a diamond chiplet on a receptor substrate that underwent an oxygen plasma surface treatment. The placement of silicon nitride chiplets requires a big tip width for it to be pick & placed, and still optical measurements have to be performed.

5

Conclusion, Discussion & Recommendations

5.1. Summary

The goal of this project was to find out which integration scheme leads to the highest on-chip detection efficiency (OCDE) of a pick & place on waveguide integrated superconducting nanowire single photon detector. So that the SNSPD could be heterogeneously integrated into the scalable modular quantum computer using diamond qubits.

In this work the misalignment tolerances of tapered and butt coupling waveguides have been simulated. Where a misalignment of 50nm achieves a coupling efficiency well over 90%. Moreover, a new type of support structure has been proposed. This support structure consist of a horizontal support structure with a taper on each side and the simulations point out that this design achieves a propagation loss 3.6 times smaller than the same horizontal support structure without tapers. Also a design of the chiplet's silicon nitride base has been designed for fabrication and testing.

Multiple releasing methods for a waveguide integrated SNSPD have been proposed and tested. We managed to release the chiplets independent of the material stack using KOH. A combination of bosch etching and KOH seems to be the most suitable method for releasing the chiplets to increase the amount of chiplets on the donor chip that could be pick & placed. Bosch etching on its own through an unpolished backside results in grass and pillar forming. And bosch etching through a polished backside resulted in clean silicon dioxide layer that still has to be removed by either dry etching or wet etching.

Furthermore, a pick & place process of diamond structures is shown. The simplest method for picking up these diamond chiplets is by breaking its tethers using a needle from above. When placing the diamond chiplet down the rough side tends to be up, which means that a smooth surface hatches better to the surface and is preferred for placements. Surface treatments were performed on the receptor substrate in an attempt to improve the adhesion of the diamond chiplet to the receptor chip. We managed to place down a diamond chiplet with a misalignment of 50nm on a receptor chiplet that did undergo oxygen plasma treatment to remove HMDS. Furthemore, we managed to pick & place silicon nitride structures.

Overall, we managed to introduce various integration schemes for heterogeneously integrating a waveguide coupled SNSPD into a scalable modular quantum computer. Although the propagation losses and OCDE couldn't be measured, the results of this research provide a foundation for future work, which can be built upon to reach the ultimate goal of fully operational Diamond-based Spin-Qubit Quantum Computer.

5.2. Recommendations for future work

Here we recommend future research for a heterogeneously integrated SNSPD based on the findings in this work:

- Measuring the propagation losses of both the silicon nitride structures and the diamond chiplets.
- Improving the support structure design: Either by reducing the width of the support structures to reduce the propagation loss. Also the width of the breaking tethers could be reduced for a faster releasing process. The optimal support structure taper size for low loss and no backside reflection intersections can be optimized with simulations.
- Finding a good metal that could be used as a contact pad and make a liftoff recipe that could be used for the alignment markers.
- Integrating the superconducting nanowire and contact pads into the chiplets design and perform OCDE measurements: In this project only the silicon nitride base structure of the SNSPD has been made. However, still the superconducting nanowire and contact pads have to be integrated, before the detection efficiency of the SNSPD could be determined.
- Combining Bosch and KOH etching to increase the density of released chiplets: The amount of chiplets that can be fabricated and released on a single chip could be increased by using the Bosch process first and KOH etching afterwards.
- Experimenting with a 2-needle pick & place setup: By using two needles the chiplet structure can be placed in a more controlled way.
- Experimenting with topographical control on the receptor substrate: Topographical control of nanoparticles has already been demonstrated to reach an alignment of contact to contact. Hence, finding a way to implement the use of topographical onto the receptor chip could potentially increase the aligment accuracy.
- Experiment with adding wet droplets on the receptor substrate as temporary glue for the chiplets: When repositioning the chiplet, it could sometimes fly away and break. Hence, using a droplet that prevents this from happening, could be experiment with.
- Automating the rotating stage of the pick & place machine: The rotating piezo stage moves the sample out the plane of focus when being used, hence a code that controls the piezo stages in a way that it automatically brings back the sample in the right plane of can be made, to decrease the time it takes for a placement.
- Experimenting with transfer printing: In this thesis only the pick & place method has been used for the integration of waveguide structures. However, transfer printing is another method that is promising for the integration of optical components on the scalable quantum computer.

Acknowledgement

We gratefully acknowledge support from the joint research program "Modular quantum computers" by Fujitsu Limited and Delft University of Technology, co-funded by the Netherlands Enterprise Agency under project number PPS2007.

Bibliography

[1] J. Bardeen and W. H. Brattain. "The Transistor, A Semi-Conductor Triode". In: *Phys. Rev.* 74 (2 July 1948), pp. 230–231. DOI: 10.1103/PhysRev.74.230. URL: https://link.aps.org/doi/10.1103/PhysRev.74.230.

[2] I.M. Ross. "The invention of the transistor". In: *Proceedings of the IEEE* 86.1 (1998), pp. 7–28. DOI: 10.1109/5.658752.

[3] Gordon E. Moore. "Cramming more components onto integrated circuits, Reprinted from Electronics, volume 38, number 8, April 19, 1965, pp.114 ff." In: *IEEE Solid-State Circuits Society Newsletter* 11.3 (2006), pp. 33–35. DOI: 10.1109/N-SSC.2006.4785860.

[4] Stephen Cass. "The Future of Moore's Law Is Inside This Willy Wonka Machine". In: *IEEE Spectrum* (). URL: https://spectrum.ieee.org/the-moores-law-machine (visited on 11/22/2023).

[5] Richard P. Feynman. "Simulating physics with computers". In: *International Journal of Theoretical Physics* 21.6 (June 1982), pp. 467–488. ISSN: 1572-9575. DOI: 10.1007/BF02650179. URL: https://doi.org/10.1007/BF02650179.

[6] M. Roser, H. Ritchie, and E. Mathieu. In: *Our World in Data* (). URL: https://ourworldindata.org/moores-law (visited on 10/25/2023).

[7] V. E. Elfving et al. *How will quantum computers provide an industrially relevant computational advantage in quantum chemistry?* 2020. arXiv: 2009.12472 [quant-ph].

[8] Frank Arute et al. "Quantum supremacy using a programmable superconducting processor". In: *Nature* 574.7779 (Oct. 2019), pp. 505–510. ISSN: 1476-4687. DOI: 10.1038/s41586-019-1666-5. URL: https://doi.org/10.1038/s41586-019-1666-5.

[9] M.A. Nielsen and I.L. Chuang. *Quantum Computation and Quantum Information: 10th Anniversary Edition*. Cambridge University Press, 2010. ISBN: 9781139495486. URL: https://books.google.nl/books?id=-s4DEy7o-a0C.

[10] O. R. Rubinas et al. *Interaction of Nitrogen-Vacancy Centers in Diamond with a Dense Ensemble of Carbon-13*. 2023. arXiv: 2310.06359 [quant-ph].

[11] R. Ishihara et al. "3D Integration Technology for Quantum Computer based on Diamond Spin Qubits". In: *2021 IEEE International Electron Devices Meeting (IEDM)*. 2021, pp. 14.5.1–14.5.4. DOI: 10.1109/IEDM19574.2021.9720552.

[12] Ramesh Kudalippalliyalil et al. "Heterogeneously Integrated Quantum Chip Interposer Packaging". In: *2022 IEEE 72nd Electronic Components and Technology Conference (ECTC)*. 2022, pp. 1869–1874. DOI: 10.1109/ECTC51906.2022.00294.

[13] Paramjeet Kaur et al. "Hybrid and heterogeneous photonic integration". In: *APL Photonics* 6.6 (June 2021), p. 061102. ISSN: 2378-0967. DOI: 10.1063/5.0052700. eprint: https://pubs.aip.org/aip/app/article-pdf/doi/10.1063/5.0052700/14572150/061102_1_online.pdf. URL: https://doi.org/10.1063/5.0052700.

[14] Merriam-Webster.com Dictionary. *Chiplet*. URL: https://www.merriam-webster.com/dictionary/chiplet.

[15] Noel H. Wan et al. "Large-scale integration of artificial atoms in hybrid photonic circuits". In: *Nature* 583.7815 (July 2020), pp. 226–231. DOI: 10.1038/s41586-020-2441-3. URL: https://doi.org/10.1038%2Fs41586-020-2441-3.

[16] F. Najafi et al. "On-chip detection of non-classical light by scalable integration of single-photon detectors". In: *Nature Communications* (2015).

[17] Jungmin Lee et al. "Printed Nanolaser on Silicon". In: *ACS Photonics* 4 (Aug. 2017). DOI: 10.1021/acsphotonics.7b00488.

[18] Matthew A. Meitl et al. "Transfer printing by kinetic control of adhesion to an elastomeric stamp". In: *Nature Materials* 5 (2006).

[19] Valentin Flauraud et al. "Nanoscale topographical control of capillary assembly of nanoparticles". In: *Nature Nanotechnology* 12 (2017). DOI: 10.1038/nnano.2016.179.

[20] J. Altepeter. "Fundamental Limits of Photon Detection". In: *https://www.darpa.mil/program/fundame limits-of-photon-detection* (2022).

[21] S. Ferrari, C Schuck, and W. Pernice. "Waveguide-integrated superconducting nanowire single-photon detectors". In: *Nanophotonics* 7 (sep 2018), pp. 1725–1758. DOI: https://doi.org/10.1515/nanoph-2018-0059.

[22] Y. Lixing. "Superconducting nanowire single-photon detectors for quantum information". In: *Nanophotonics* 9.9 (2020), pp. 2673–2692. DOI: https://doi.org/10.1515/nanoph-2020-0186.

[23] Oliver Kahl et al. "Waveguide integrated superconducting single-photon detectors with high internal quantum efficiency at telecom wavelengths". In: *Scientific reports* 5 (June 2015), p. 10941. DOI: 10.1038/srep10941.

[24] Yilin Xu et al. "Superconducting nanowire single-photon detector with 3D-printed free-form microlenses". In: *Opt. Express* 29.17 (Aug. 2021), pp. 27708–27731. DOI: 10.1364/OE.427639. URL: https://opg.optica.org/oe/abstract.cfm?URI=oe-29-17-27708.

[25] S. Ferrari. "Characterization of NbN waveguide-integrated superconducting nanowire single-photon detectors in the near-infrared range". In: *WWU Münster* (2019). DOI: https://doi.org/10.13140/RG.2.2.29539.71208.

[26] Iman Esmaeil Zadeh et al. "Superconducting nanowire single-photon detectors: A perspective on evolution, state-of-the-art, future developments, and applications". In: *Applied Physics Letters* 118 (May 2021), p. 190502. DOI: 10.1063/5.0045990.

[27] V.V. Shmidt, P. Müller, and A.V. Ustinov. *The Physics of Superconductors: Introduction to Fundamentals and Applications*. Springer, 1997. ISBN: 9783540612438. URL: https://books.google.nl/books?id=8O8svNo_tWoC.

[28] J. Chang. "Detecting Single Photons with Superconducting Nanowires". In: *https://doi.org/10.4233/u d083-4138-b835-c9c84d8a99d1* (2021). DOI: https://doi.org/10.4233/uuid:dddca4bd-d083-4138-b835-c9c84d8a99d1.

[29] WeiJun Zhang et al. "Nbn superconducting nanowire single photon detector with efficiency over 90% at 1550 nm wavelength operational at compact cryocooler temperature". In: *Science China Physics, Mechanics & Astronomy* 60 (2017), pp. 1869–1927. DOI: https://doi.org/10.1007/s11433-017-9113-4.

[30] P Hu et al. "Detecting single infrared photons toward optimal system detection efficiency". In: *Optics Express* 28 (2020).

[31] I. Esmaeil Zadeh et al. "Single-photon detectors combining high efficiency, high detection rates, and ultra-high timing resolution". In: *APL Photonics* 2 (2017).

[32] J. Chang et al. "Detecting telecom single photons with 99.5- 2.07+ 0.5% system detection efficiency and high time resolution". In: *APL Photonics* 6 (2021).

[33] F. Marsili et al. "Detecting single infrared photons with 93% system efficiency". In: *Nature Photonics* 7 (2013). DOI: https://doi.org/10.1038/nphoton.2013.13.

[34] Dileep V. Reddy et al. "Superconducting nanowire single-photon detectors with 98% system detection efficiency at 1550 nm". In: *Optica* 7.12 (Dec. 2020), pp. 1649–1653. DOI: 10.1364/OPTICA.400751. URL: https://opg.optica.org/optica/abstract.cfm?URI=optica-7-12-1649.

[35] V.B. Verma et al. "Superconducting nanowire single photon detectors fabricated from an amorphous mo0.75ge0.25 thin film". In: *Applied Physics Letters* 105 (2014).

[36] I. Milostnaya et al. "Superconducting single photon nanowire detectors development for ir and thz applications". In: *Journal of Low Temperature Physics* 151 (2008).

[37] Yu P Korneeva et al. "Superconducting single-photon detector made of MoSi film". In: *Superconductor Science and Technology* 27.9 (Aug. 2014), p. 095012. DOI: 10.1088/0953-2048/27/9/095012. URL: https://dx.doi.org/10.1088/0953-2048/27/9/095012.

[38] V.B. Verma et al. "High-efficiency superconducting nanowire single-photon detectors fabricated from mosi thin-films". In: *Optics Express* 23 (2015).

[39] M. Caloz et al. "High-detection efficiency and low-timing jitter with amorphous superconducting nanowire single-photon detectors". In: *Applied Physics Letters* 112 (2018).

[40] C. Cirillo et al. "Superconducting nanowire single photon detectors based on disordered nbre films". In: *Applied Physics Letters* 117 (2020).

[41] R. Gourgues et al. "Superconducting nanowire single photon detectors operating at temperature from 4 to 7 k". In: *Optics Express* 27 (2019).

[42] S.N. Dorenbos et al. "Low gap superconducting single photon detectors for infrared sensitivity". In: *Applied Physics Letters* 98 (2011).

[43] A. Engel et al. "Tantalum nitride superconducting single-photon detectors with low cut-off energy". In: *Applied Physics Letters* 100 (2012).

[44] H. Shibata, T. Akazaki, and Y. Tokura. "Fabrication of mgb2 nanowire singlephoton detector with meander structure". In: *Applied Physics Express* 6 (2013).

[45] S. Cherednichenko et al. "Low kinetic inductance superconducting mgb2 nanowire photon detectors with a 100 picosecond relaxation time". In: *arXiv:1911.01480* (2019).

[46] S. Cherednichenko et al. "Ir- and visible- light single photon detection in superconducting mgb2 nanowires". In: *arXiv:1911.01652* (2019).

[47] Neji Saliha. "Pick & Place Integration of Diamond Nanophotonic Structures for Modular, On Chip Diamond Quantum Systems". In: *Delft University of Technology* (2023).

[48] P.R. Sharapova et al. "Toolbox for the design of LiNbO3-based passive and active integrated quantum circuits". In: *New Journal of Physics* 19.12 (2017), p. 123009. DOI: 10.1088/1367-2630/aa9033.

[49] Optiwave. "Proton Exchange Process in Lithium Niobate". In: *https://optiwave.com/optibpm-manuals/bpm-proton-exchange-process-in-lithium-niobate/* (2022).

[50] R.C. Alferness. "Titanium-Diffused Lithium Niobate Waveguide Devices". In: *Springer Berlin Heidelberg* (1988), pp. 145–210. DOI: 10.1007/978-3-642-97074-0_4.

[51] Jared F. Bauters et al. "Planar waveguides with less than 0.1 dB/m propagation loss fabricated with wafer bonding". In: *Opt. Express* 19.24 (Nov. 2011), pp. 24090–24101. DOI: 10.1364/OE.19.024090. URL: https://opg.optica.org/oe/abstract.cfm?URI=oe-19-24-24090.

[52] Zhaoyi Li et al. "Process Development of Low-Loss LPCVD Silicon Nitride Waveguides on 8-Inch Wafer". In: *Applied Sciences* 13.6 (2023). ISSN: 2076-3417. DOI: 10.3390/app13063660. URL: https://www.mdpi.com/2076-3417/13/6/3660.

[53] S. Ferrari, C Schuck, and W. Pernice. "Waveguide-integrated superconducting nanowire single-photon detectors". In: *Nanophotonics* 7 (sep 2018), pp. 1725–1758. DOI: https://doi.org/10.1515/nanoph-2018-0059.

[54] C. Schuck, W. H. P. Pernice, and H. X. Tang. "NbTiN superconducting nanowire detectors for visible and telecom wavelengths single photon counting on Si3N4 photonic circuits". In: *Applied Physics Letters* 102.5 (Feb. 2013). DOI: 10.1063/1.4788931. URL: https://doi.org/10.1063%2F1.4788931.

[55] Mohsen Akhlaghi, Ellen Schelew, and Jeff Young. "Waveguide Integrated Superconducting Single Photon Detectors Implemented as Coherent Perfect Absorbers". In: *Nature communications* 6 (Sept. 2014). DOI: 10.1038/ncomms9233.

[56] W.H.P. Pernice et al. "High-speed and high-efficiency travelling wave single-photon detectors embedded in nanophotonic circuits". In: *Nature Communications* 3.1 (Dec. 2012). DOI: 10.1038/ncomms2307. URL: https://doi.org/10.1038%2Fncomms2307.

[57] C. Schuck, W. H. P. Pernice, and H. X. Tang. "NbTiN superconducting nanowire detectors for visible and telecom wavelengths single photon counting on Si3N4 photonic circuits". In: *Applied Physics Letters* 102.5 (Feb. 2013), p. 051101. ISSN: 0003-6951. DOI: 10.1063/1.4788931. eprint: https://pubs.aip.org/aip/apl/article-pdf/doi/10.1063/1.4788931/14277511/051101_1_online.pdf. URL: https://doi.org/10.1063/1.4788931.

[58] Carsten Schuck et al. "Quantum interference in heterogeneous superconducting-photonic circuits on a silicon chip". In: *Nature Communications* 7 (Nov. 2015). DOI: 10.1038/ncomms10352.

[59] Johannes Görlitz et al. "Spectroscopic investigations of negatively charged tin-vacancy centres in diamond". In: *New Journal of Physics* 22.1 (Jan. 2020), p. 013048. DOI: 10.1088/1367-2630/ab6631. URL: https://dx.doi.org/10.1088/1367-2630/ab6631.

[60] K.R. Williams, K. Gupta, and M. Wasilik. "Etch rates for micromachining processing-Part II". In: *Journal of Microelectromechanical Systems* 12.6 (2003), pp. 761–778. DOI: 10.1109/JMEMS.2003.820936.

[61] Kazuhiro Ikeda et al. "Thermal and Kerr nonlinear properties of plasma-deposited silicon nitride/silicon dioxide waveguides". In: *Opt. Express* 16.17 (Aug. 2008), pp. 12987–12994. DOI: 10.1364/OE.16.012987. URL: https://opg.optica.org/oe/abstract.cfm?URI=oe-16-17-12987.

[62] Fred Roozeboom et al. "Cyclic Etch/Passivation-Deposition as an All-Spatial Concept toward High-Rate Room Temperature Atomic Layer Etching". In: *ECS Journal of Solid State Science and Technology* 4 (Feb. 2015), N5067–N5076. DOI: 10.1149/2.0111506jss.

[63] Pauline Stevic. *BOE/HF - Silicon dioxide Etching Standard Operating Procedure*. 2018. URL: https://d2k0ddhflgrk1i.cloudfront.net/TNW/Afdelingen/Quantum%20Nanoscience/Kavli%20Nanolab%20Delft/Equipment/BOE-HF%20SOP%20Silicon%20Etching.pdf.

[64] Pauline Stevic. *KOH Etchant Standard Operating Procedure*. 2018. URL: https://d2k0ddhflgrk1i.cloudfront.net/TNW/Afdelingen/Quantum%20Nanoscience/Kavli%20Nanolab%20Delft/Equipment/KOH%20-%20Silicon%20Etching%20SOP.pdf.

[65] *Lecture 26: Etching and deposition*. URL: https://staff-old.najah.edu/sites/default/files/Lec26.pdf (visited on 10/30/2023).

[66] J.H. Adair, E. Suvaci, and J. Sindel. "Surface and Colloid Chemistry". In: *Encyclopedia of Materials: Science and Technology*. Ed. by K.H. Jürgen Buschow et al. Oxford: Elsevier, 2001, pp. 1–10. ISBN: 978-0-08-043152-9. DOI: https://doi.org/10.1016/B0-08-043152-6/01622-3. URL: https://www.sciencedirect.com/science/article/pii/B0080431526016223.

[67] Manish Keswani and Zhenxing Han. "Chapter 4 - Post-CMP Cleaning". In: *Developments in Surface Contamination and Cleaning*. Ed. by Rajiv Kohli and K.L. Mittal. Oxford: William Andrew Publishing, 2015, pp. 145–183. ISBN: 978-0-323-29961-9. DOI: https://doi.org/10.1016/B978-0-323-29961-9.00004-1. URL: https://www.sciencedirect.com/science/article/pii/B9780323299619000041.

[68] G. Kumar and S. Beaudoin. "Undercut Removal of Micrometer-Scale Particles from Surfaces". In: *Journal of The Electrochemical Society* 153.2 (Jan. 2006), G175. DOI: 10.1149/1.2149224. URL: https://dx.doi.org/10.1149/1.2149224.

[69] Marina Ruths. "Surface Forces, Surface Tension, and Adhesion". In: *Encyclopedia of Tribology*. Ed. by Q. Jane Wang and Yip-Wah Chung. Boston, MA: Springer US, 2013, pp. 3435–3443. ISBN: 978-0-387-92897-5. DOI: 10.1007/978-0-387-92897-5_463. URL: https://doi.org/10.1007/978-0-387-92897-5_463.

[70] C.A. Coulomb. "Premiere Memoire sur l'electricite et le Magnetisme". In: *Histoire de l'Academie Royale des Sciences* (1785), pp. 569–577.

[71] Susanna Laurén. 2021. URL: https://www.biolinscientific.com/blog/wetting-in-electronics-how-hmds-treatment-works (visited on 10/27/2023).

[72] Chan Kok Sheng et al. "INFLUENCE OF HF ETCHING TIME AND CONCENTRATION ON SI WAFER IN THE MIXTURE SOLUTION OF HF/HNO 3 /CH 3 COOH". In: *Journal of Sustainability Science and Management* 15 (Feb. 2020), pp. 6–11.

[73] J.K. Bal, S. Kundu, and S. Hazra. "Hydrophobic to hydrophilic transition of HF-treated Si surface during Langmuir–Blodgett film deposition". In: *Chemical Physics Letters* 500.1 (2010), pp. 90–95. ISSN: 0009-2614. DOI: https://doi.org/10.1016/j.cplett.2010.10.004. URL: https://www.sciencedirect.com/science/article/pii/S0009261410013527.

[74] Ananda Ria Safitri et al. "Wettability comparison of argon and oxygen plasma treatment for coconut fiber with 2 MHZ RF plasma system". In: *AIP Conference Proceedings* 2296.1 (Nov. 2020), p. 020078. ISSN: 0094-243X. DOI: 10.1063/5.0032545. eprint: https://pubs.aip.org/aip/acp/article-pdf/doi/10.1063/5.0032545/14222427/020078_1_online.pdf. URL: https://doi.org/10.1063/5.0032545.

A

Appendix: Fabrication Recipe

Alignment marker recipe:

1. 4" wafer double polished 300μm silicon wafer
2. Deposit 200nm $Si3N4$ on both sides using the Oxford Instruments PlasmaPro 80:
   (a) Set temperature to 300^{o}C
   (b) Pre-deposit silicon nitride for 5 min with the standard "dep. HiQual $Si3N4$ 300C" recipe
   (c) Deposit silicon nitride for 17min with the standard "dep. HiQual $Si3N4$ 300C" recipe
   (d) Flip the wafer and deposit silicon nitride for 17 min with the standard "dep. HiQual $Si3N4$ 300C" recipe
3. Anneal @ 800^o for 4 hours to 170nm silicon nitride
4. Prebake @ 200oC for 5 min
5. Spin coating Lor5B @ 4000RPM for 1 min
6. Bake @ 190^{o}C for 5 min
7. Spin coating S1813 @ 4000RPM for 1 min
8. Bake @ 115^{o}C for 1 min
9. Pattern using uMLA Laserwriter (Dose = 250mJ/cm2, Defoc = 6)
10. Development in MF21A for 1.5 min, rinse in H_2O for 30 sec.
11. Deposit 200nm of gold using the AJA QT:
    (a) Deposit 5nm Ti @ 0.5Å/s
    (b) Deposit 200nm Au @ 2Å/s
12. Liftoff with NMP using the sonicator @ 50^{o}C for 4 hours
13. Spin coating S1813 as a protection layer @ 4000RPM for 1 min
14. Bake @ 115^{o}C for 1 min
15. Spin coating Lor5B on otherside of the wafer @ 4000RPM for 1 min
16. Bake @ 190^{o}C for 5 min
17. Spin coating S1813 @ 4000RPM for 1 min
18. Bake @ 115^{o}C for 1 min
19. Align top and backside using EVG-620 NUV:
    (a) Thickness substrate 0.3μm

   (b) Thickness mask 2.3mm
   (c) Thickness resist 2μm
   (d) Soft contact backside alignment
   (e) 7 sec exposure time

20. Development in MF21A for 1.5 min, rinse in H_2O for 30 sec.
21. Deposit 200nm of gold using the AJA QT:

   (a) Deposit 5nm Ti @ 0.5Å/s
   (b) Deposit 200nm Au @ 2Å/s

22. Liftoff with NMP using the sonicator @ 50^{o}C for 4 hours