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A 0.049mm^2 7.1-to-16.8GHz Dual-Core Triple-Mode VCO Achieving 200dB FOM$_A$ in 22nm FinFET

LC VCOs with low phase noise (PN) and an octave frequency tuning range (FTR) are required for multi-standard communication devices, software-defined radios, and wireline data links. A viable popular approach is to exploit multi-core mode-switching VCOs for two reasons: (1) their PN improves linearly by in-phase coupling of N identical VCOs; (2) the resonant-mode switching enhances the VCO's FTR without degrading the tank's quality factor (Q) as no RF current ideally flows through lossy mode-selection switches. However, it is still challenging for dual-mode VCOs to achieve a competitive FOM while covering an octave FTR at oscillation frequencies (F_{OSC}) above 6GHz [1]. To enhance the number of oscillation modes to 3, [2] added a center loop inductor (L_C) to a transformer, as shown in Fig.1. However, a large FTR gap is measured, since the transformer windings should be strongly coupled to accommodate L_C. [3] and [4] respectively realized a triple- and quad-mode operation by coupling two individual transformer-based resonators (see Fig.1). Apart from the large area penalty, the former needs an extra third winding (L_T) in each transformer that degrades the tank's Q, while the latter used large fixed coupling capacitors (C_M) that load the tank in two of the resonant modes, thus limiting the VCO's FTR.

Consequently, prior-art mode-switching VCOs either suffer from a severe FOM degradation [1], or FTR discontinuity [2], or a large area penalty [3, 4] as they typically occupy the footprint of two standalone oscillators. To improve on those limitations, this paper presents a 0.049mm^2 dual-core triple-mode VCO. Specifically, three distinct resonant frequencies are synthesized through the constructive/destructive magnetic coupling, coil current cancellation, and inductor shortcutting of a high-Q compact 4-port tapped inductor and the capacitive mode-switching. Compared with prior art at a similar F_{OSC} range, this work improves FOM$_A$ by >3dB without sacrificing FOM$_T$.

Fig.1 right shows the proposed triple-mode resonator consisting of two loop-inductors and two sets of tuning capacitors (C_B and C_S, where C_B>C_S). The outer and inner inductors are realized between P_1-P_2 and P_3-P_4 ports with a self-inductance of $2L_1$+$2L_3$ and $2L_2$+$2L_3$, respectively. By differential-mode (DM) or common-mode (CM) excitation of the inductors' ports through negative transconductors (-G_{M1-4}) and mode-selection switches (S_L, S_M,

and S_H), three different equivalent inductances (L_{eff}) and capacitances (C_{eff}) can be realized to achieve three distinct resonant frequencies ($\omega_{1,2,3}$).

As shown in Fig.2 top-left, in the low-frequency mode (mode-1), by closing S_L and opening $S_{M,H}$, while enabling -G_{M1} and -G_{M2} cores, two coupled VCOs employing inner and outer inductors are realized. In this mode, signals at P_1 and P_3 are in phase while showing a 180° phase difference with respect to P_2 and P_4 signals. This forces an in-phase coupling between L_1 and L_2, enhancing the magnetic flux and creating a positive mutual inductance (M_{12}). Moreover, anti-phase coupling occurs between two L_2 inductors, thus creating a negative mutual inductance of -M_{22}. Consequently, the effective inductances seen by the inner and outer VCOs are ~$2(L_2+2L_3+M_{12}-M_{22})$ and ~$2(L_1+2L_3+M_{12})$, respectively. Note that in the presence of a mismatch between the free-running frequencies of the two VCOs, a current would flow through the lossy mode-selection switches to balance the resonators' energy and force the VCOs to oscillate at the same frequency, thus degrading tank's Q and limiting the 3dB theoretical PN improvement due to the coupling. To avoid this issue, the effective inductance of the two VCOs should be equal. Hence, L_1 is deliberately designed to be smaller than L_2 (i.e., $L_1=L_2-M_{22}$). Furthermore, as a CM oscillation is realized across C_S plates, C_{eff} equals C_B in this mode.

In the middle-frequency mode (mode-2), -G_{M1} and -G_{M2} cores are kept active, but the mode-selection switches S_M and $S_{L,H}$ are respectively closed and opened to realize a DM oscillation between in-phase $P_{1,4}$ and $P_{2,3}$ signals (see Fig.2 top-middle). This forces an anti-phase magnetic coupling between L_1 and L_2 segments of inner and outer inductors. Moreover, L_3 conducts virtually zero current as the oscillation currents of the inner and outer VCOs circulate in opposite directions, thus sharply dropping the VCOs' effective inductance to $L_{eff2}\approx 2L_2-2M_{12}-2M_{22}=2L_1-2M_{12}$. However, as both C_B and C_S experience a DM oscillation voltage, C_{eff2} increases to C_B+C_S. Consequently, the difference in both the capacitive and inductive components (i.e., $C_{eff2}-C_{eff1} = C_S$ and $L_{eff2}-L_{eff1} = -4L_3-4M_{12}$) are exploited to separate mode-2 from mode-1. Note that L_{eff2}/L_{eff1} reduction is designed to be much larger than C_{eff2}/C_{eff1} increase to adjust $\omega_2\approx 1.3\omega_1$.

The high-frequency mode (mode-3) is excited by activating -G_{M3} and -G_{M4} cores, closing S_H, and opening $S_{L,M}$, as shown in Fig.2 top-right. In this mode, the currents of the left and right VCOs can find a shortcut and avoid flowing into L_3, and consequently, L_{eff3} can be approximated by $L_1+L_2-2M_{12}+M_{22}=2(L_1-M_{12}+M_{22})$. Moreover, C_{eff3} reduces to its minimum value, C_S. Hence, mode-3 is capacitively and inductively separated from other modes to place $\omega_3 \approx 1.3\omega_2$.

Fig.2 bottom depicts the simulated resonator impedance and Q based on the inductor's EM and $C_{B,S}$ parasitic extraction. The resonant frequency can be tuned over more than an octave frequency range while going from mode-1 to mode-3. The tank's Q in mode-2 and 3 is ~15% lower than mode-1 due to the anti-phase coupling between L_1 and L_2. Yet, the resulting FOM_T variation is within 1.5dB. Since PN is proportional to R_P/Q^2, the lower impedance peak (R_P) in mode-2 and 3 (caused by the reduced L_{eff}) will partially compensate their lower tank's Q to achieve a similar normalized PN as in mode-1. Moreover, to ensure a robust start-up over PVT variations, -$G_{M3,4}$ can be optionally enabled in mode-2, where R_P is the lowest.

Fig.3 top shows the VCO's schematic in which the four identical G_M cells are implemented by CMOS differential pairs. To regulate the oscillation amplitude against R_P variations in different operation modes, 11 equally-sized switched resistors are added to adjust the VCO current. The mode-selection switches are realized by plain transmission gates and sized such that their ON-resistance ($R_{ON,M}$) is low enough (i.e., $R_{ON,M}/R_P<0.25$) to minimize PN degradation when VCOs' tanks face a pessimistic 5% mismatch. Further reducing $R_{ON,M}$ would increase the switches' parasitic capacitance and limit the FTR. For coarse tuning, C_B and C_S are each realized by a small fixed capacitor in parallel with a 7-b binary switched-capacitor bank with a maximum frequency step of 60MHz. Four varactors with an average tuning gain (K_{VCO}) of 120MHz/V are also added to C_B and C_S to achieve continuous frequency tuning. Notice that C_S and C_B experience a CM voltage in mode-1 and 3, respectively, and should not contribute to the total tank's capacitance. However, in those modes, the gate capacitor of C_B/C_S bank switches (C_G) in series with the ON-resistance ($R_{ON,D}$) of the switch driver forms a return path for the tank's CM current (see Fig.3 bottom), thus degrading the tank's Q. Although the Q reduction could be minimized by lowering $R_{ON,D}$, a massive driver with a strong power/ground connection would be required, complicating the layout. Besides, C_G

would be visible to the tank, thus limiting the FTR and maximum F_{OSC}. Instead, 8 stacked devices with minimum channel length and width are used to simultaneously minimize the driver output capacitance and increase $R_{ON,D}$, thus impeding current flow through the driver. Therefore, FTR and PN are not affected as C_G is no longer visible to the tank. An $R_{ON,D}$ of 10kΩ is sufficiently large for this purpose and yet low enough to ensure ~500MHz switching speed for the capacitor bank.

The proposed dual-core triple-mode VCO, implemented within an analog sub-sampling PLL, was fabricated in a 22nm FinFET CMOS with a core area of 0.049mm^2, as shown in Fig.7. An on-chip divider-by-8 is used to ease the measurements. The VCO consumes 5.5 to 13.5mW from a 1.1V supply. Fig.4 and 5 show the measured VCO frequency tuning curves, PN plots of the three operation modes, and PN variations over F_{OSC} and a temperature range of -55°C to 85°C. At 25°C, the VCO shows a triple-mode operation by covering 7.1-9.6GHz, 8.9-13GHz, and 11.8-16.8GHz. Moreover, from -55°C to 85°C, a continuous FTR of 80.6% with >0.65GHz frequency overlap between adjacent modes is achieved. At 25°C, the PN at a 10MHz offset varies from -137.9dBc/Hz at 7.1GHz to -128.7dBc/Hz at 16.8GHz, resulting in only <3dB normalized PN and FOM variations over the entire FTR. The measured PN variation over a 140°C temperature range is <3.6dB at a similar F_{OSC}. Thanks to the enhanced $R_{ON,D}$, changing C_S (C_B) in mode-1 (mode-3) has a negligible impact on the measured PN (<0.3dB) and F_{OSC} (<0.1%). To demonstrate that the VCO has a sufficiently small coarse frequency step and a large K_{VCO} to be incorporated into a PLL without incurring extra area and noise, the closed-loop PN plots are also included in Fig.5. Due to the VCO's negligible FOM variations, the measured RMS jitter of the PLL is almost constant and remains <80fsec over different operation modes.

Compared with prior-art octave FTR VCOs operating at similar frequencies (Fig. 6), only the dual-mode VCO in [1] occupies a smaller area, but with >4dB worse FOM_T. Although [3] achieves a better maximum FOM_T, it occupies ~8x larger area and its performance drops by >10dB over the FTR. Without sacrificing FOM_T, our triple-mode VCO achieves the best reported FOM_A of 200dB, thus improving prior art by >3dB.

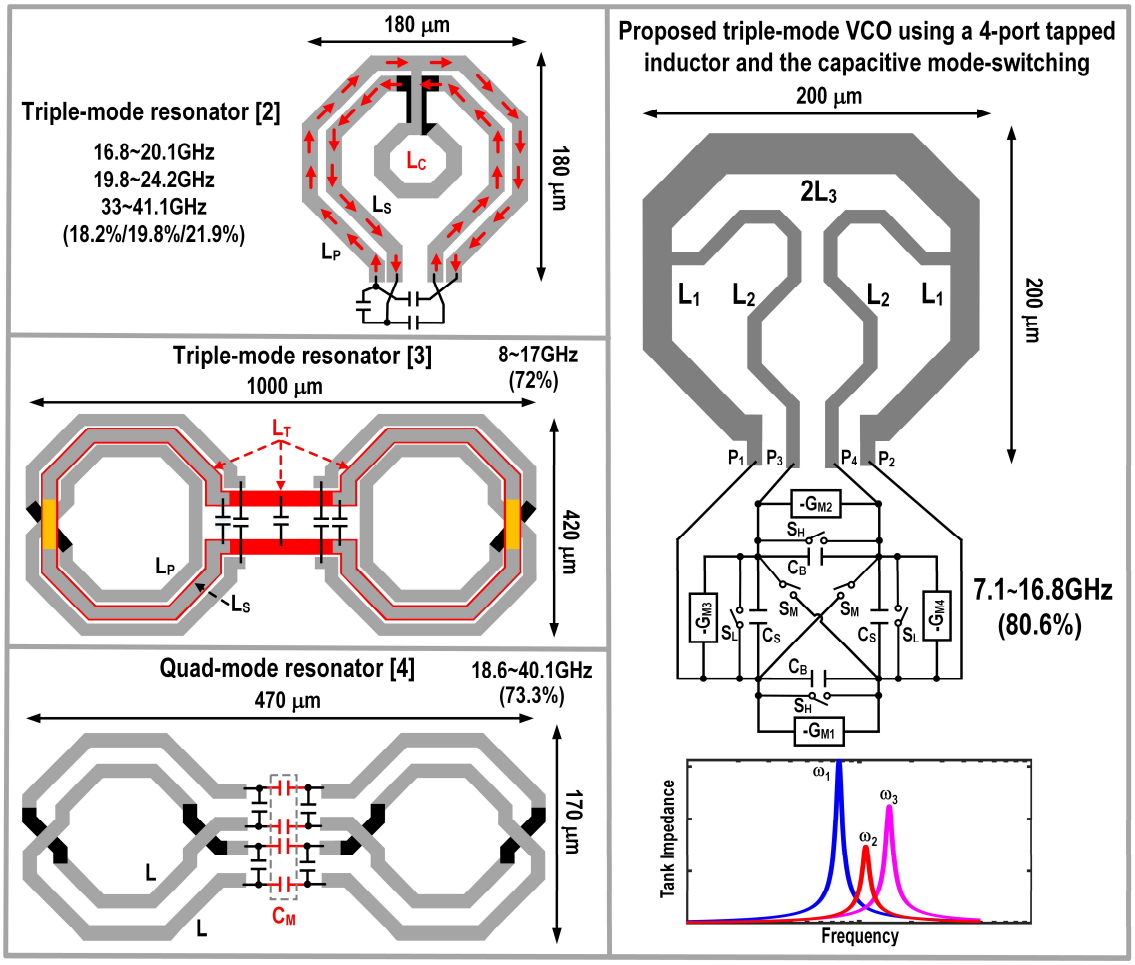


Fig. 1: Prior-art multi-mode resonators (left) and the proposed triple-mode VCO (right).

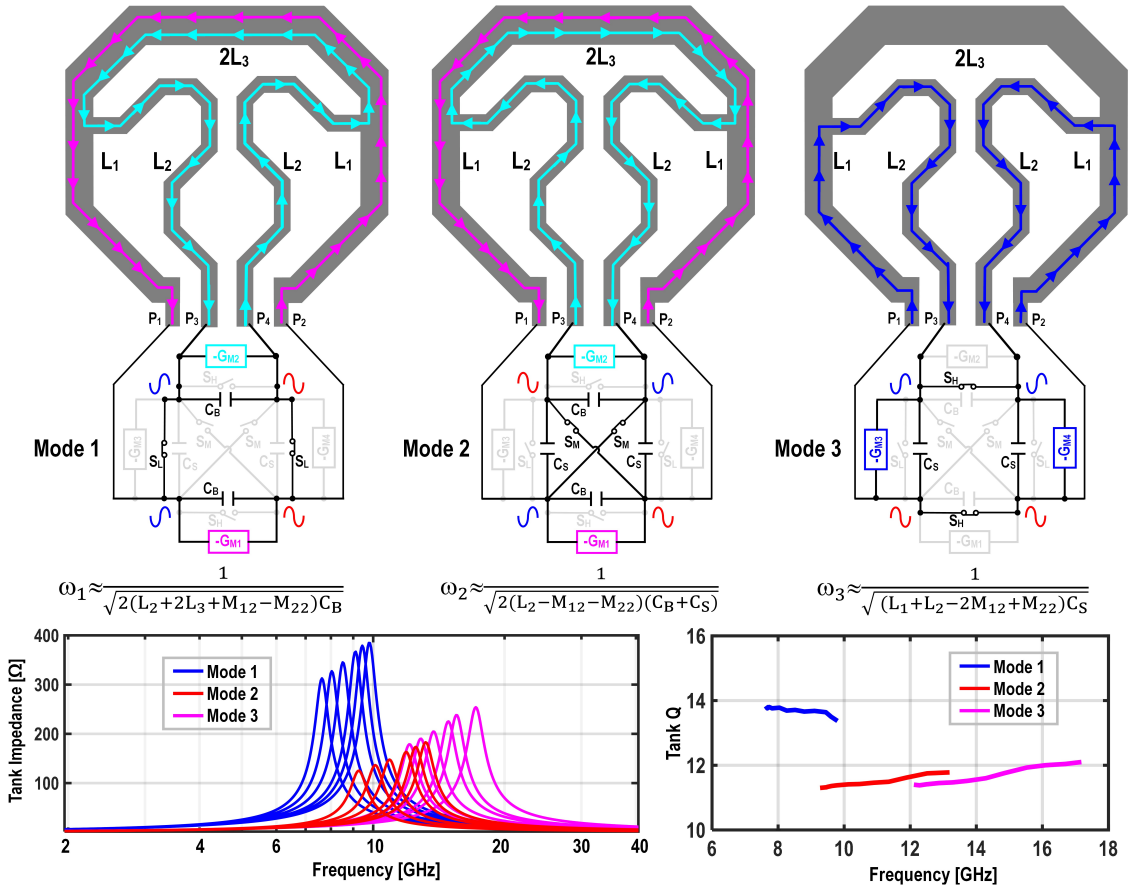


Fig. 2: Circuit configuration, oscillation voltages and currents of the proposed VCO in its three operation modes (top) and simulated tank's impedance and quality factor over the frequency (bottom).

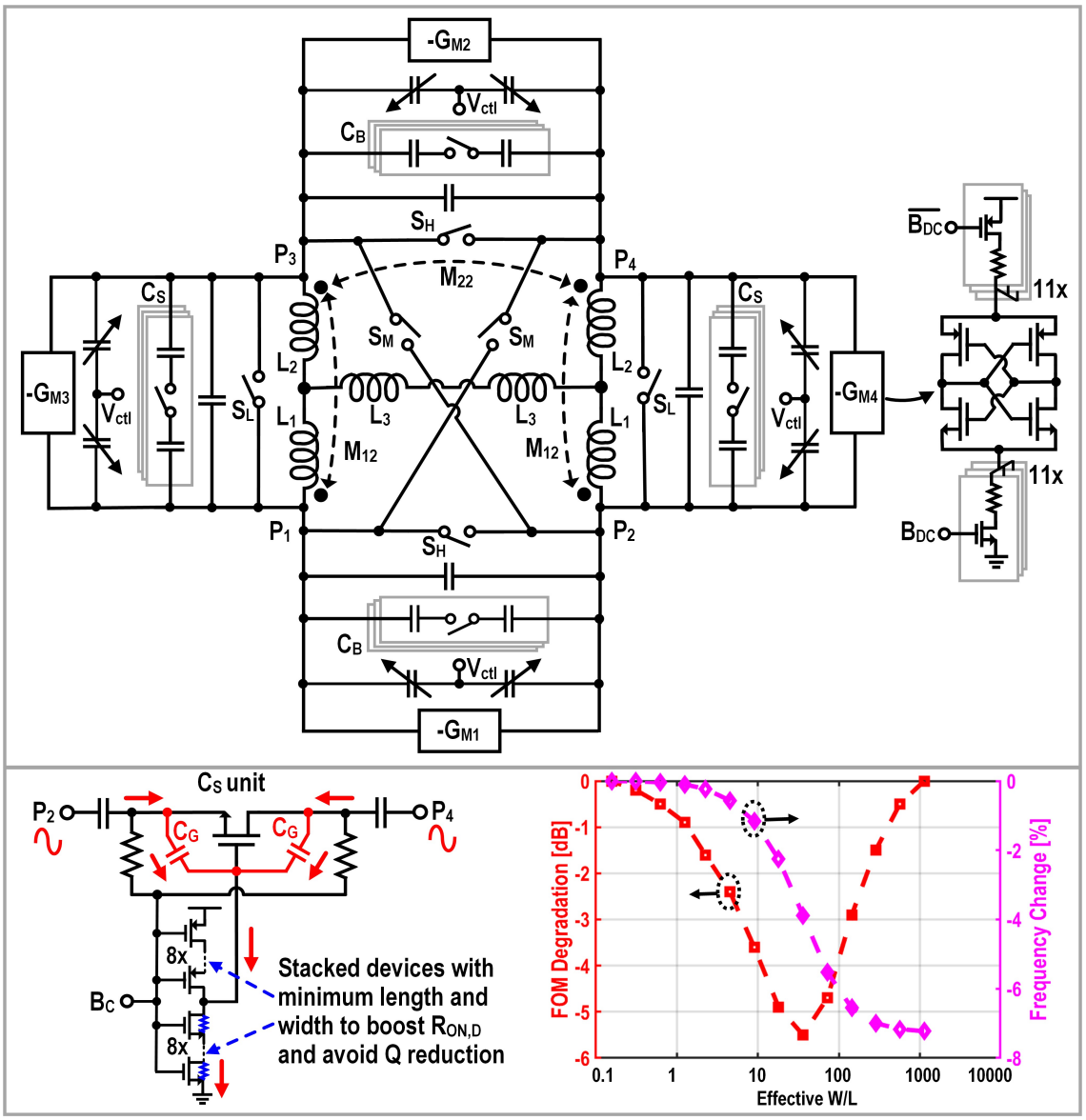


Fig. 3: Circuit implementation of the proposed VCO (top). Illustration of the undesired common-mode current return path, and simulated FOM degradation and frequency change (compared to the case that an ideal switch driver with a high output impedance is used) versus the effective size of the switch driver (bottom).

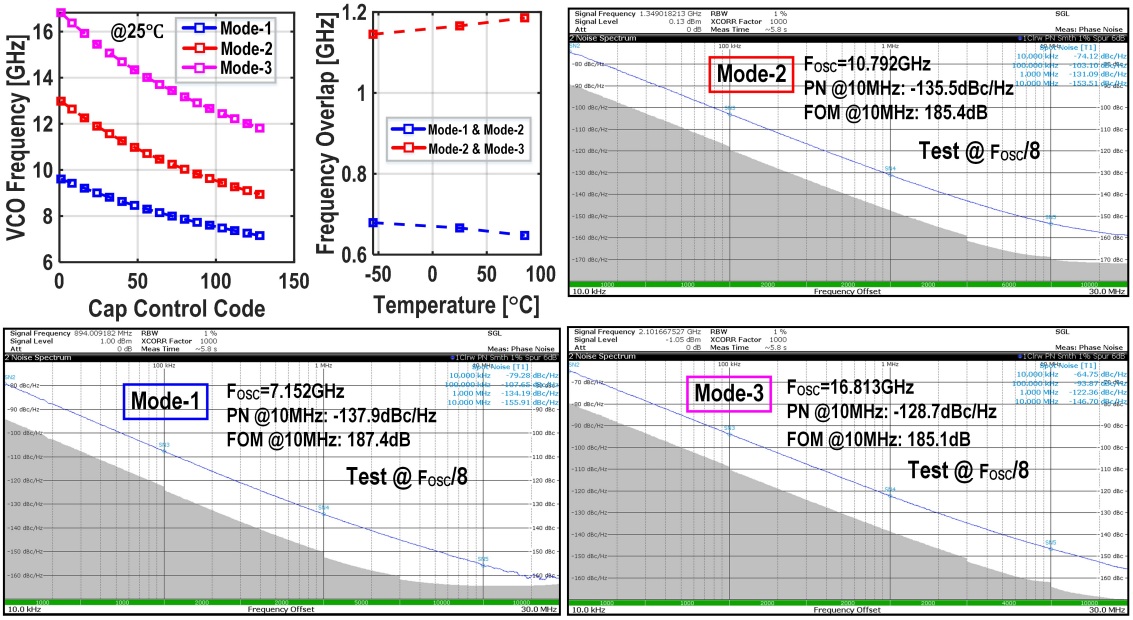


Fig. 4: Measured frequency tuning curves, frequency overlap between adjacent modes over temperature, and PN plots in different operation modes at 25°C after an on-chip divider-by-8.

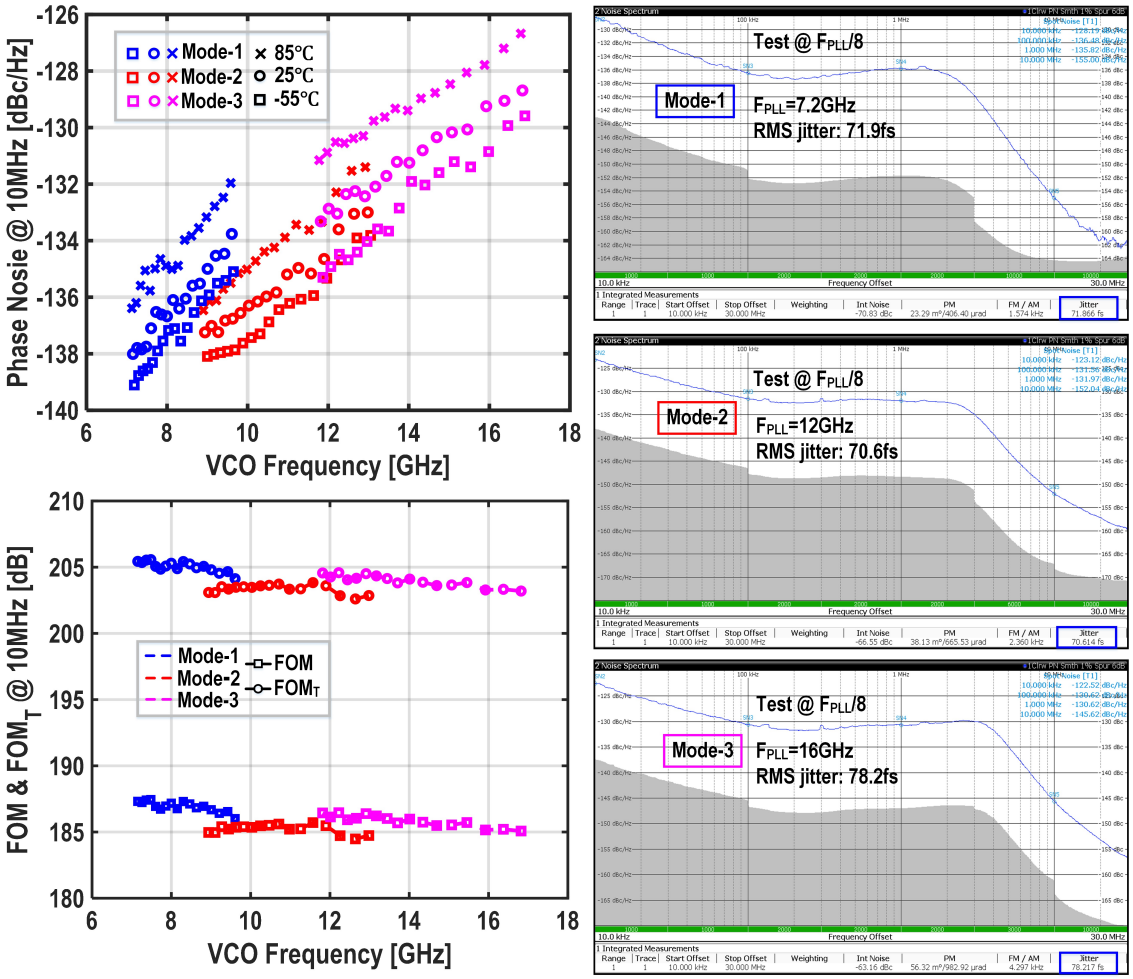


Fig. 5: Measured PN and FOM & FOM_T at a 10MHz frequency offset in different operation modes over temperature (left). Measured PN plots of the octave FTR sub-sampling PLL in different operation modes at 25°C after an on-chip divider-by-8 (right).

	This Work	M. Raj VLSI'16 [1]	O. El-Aassar JSSC'21 [3]	A. Agrawal TMTT'17[5]	W. Deng CICC'21[6]	Y. Shu ISSCC'20 [4]
VCO Topology	**Dual-core Triple-mode**	Single-core Dual-mode	Dual-core Triple-mode	Single-core Dual-mode	Dual-core Quad-mode	Quad-core Quad-mode
Supply [V]	**1.1**	0.8	0.45/0.9***	0.45~0.6	NA	0.95
Frequency [GHz]	**7.1~16.8**	7~18.3	8~17	6.39~14	8.2~21.5	18.6~40.1
Tuning Range [%]	**80.6**	89.3	72	74.6	89.6	73.2
Power [mW]	**5.5~13.5***	4.4~3	17^~33^^	2.2~10.3	4~6	9~15
PN @10MHz [dBc/Hz]	**-137.9~-128.7**	-131.8**~-119**	-143.1^~-134.7^^	-137.7~-130.3	-129~-120	-130.3~-122.7
PN @10MHz [dBc/Hz] (normalized to 1GHz)	**-155~-153.2**	-148.8~-144.2	-163.8~-155.8	-153.8~-153.2	-147.3~-146.7	-156~-154.7
Average FOM / FOM Variation @10MHz [dB]	**186.3** **187.6~185.1**	180.9 182.3~179.5	186.15 191.65~180.65	187 188~186	179 181~177	184.65 186.3~183
Average FOM_T / FOM_T Variation @10MHz [dB]	**204.4** **205.7~203.2**	199.9 201.3~198.5	203.3 208.8~197.8	204 205~203	198.5 201~196	201.95 203.6~200.3
Average FOM_A / FOM_A Variation @10MHz [dB]	**199.4** **200.7~198.2**	196.1 197.5~194.7	190.2 195.7~184.7	196 197~195	183 185~181	195.65 197.3~194
Technology	**22nm FinFET**	16nm FinFET	22nm FDSOI	65nm CMOS	65nm CMOS	40nm CMOS
Core Area [mm^2]	**0.049**	0.03	0.39	0.126	0.4	0.08

*6-5.5mW (mode-1), 13.5-11.3mW (mode-2), and 6.8-6.5mW (mode-3) **Estimated from plots ***0.9V Forward body biasing voltage used in switched capacitors ^Reported value @11.02GHz ^^Reported value @11.4GHz

$FOM = |PN(\Delta f)| + 20\log_{10}(F_{OSC}/\Delta f) - 10\log_{10}(P_{DC}/1mW)$

$FOM_T = FOM + 20\log_{10}(FTR/10)$

$FOM_A = FOM + 10\log_{10}(1mm^2/A)$ defined in [B. Soltanian, JSSC'07]

Fig. 6: Comparison with prior-art octave FTR VCOs at similar frequencies (>6GHz).

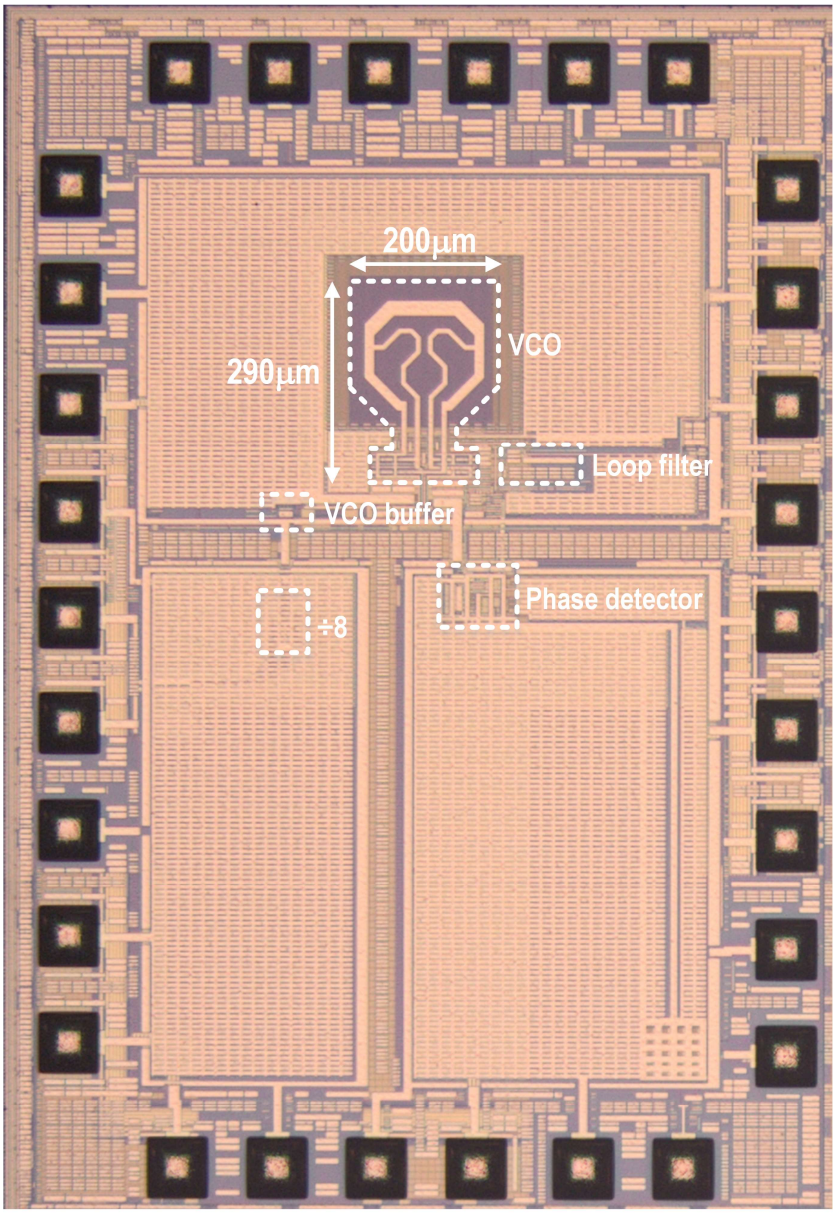


Fig. 7: Chip micrograph.

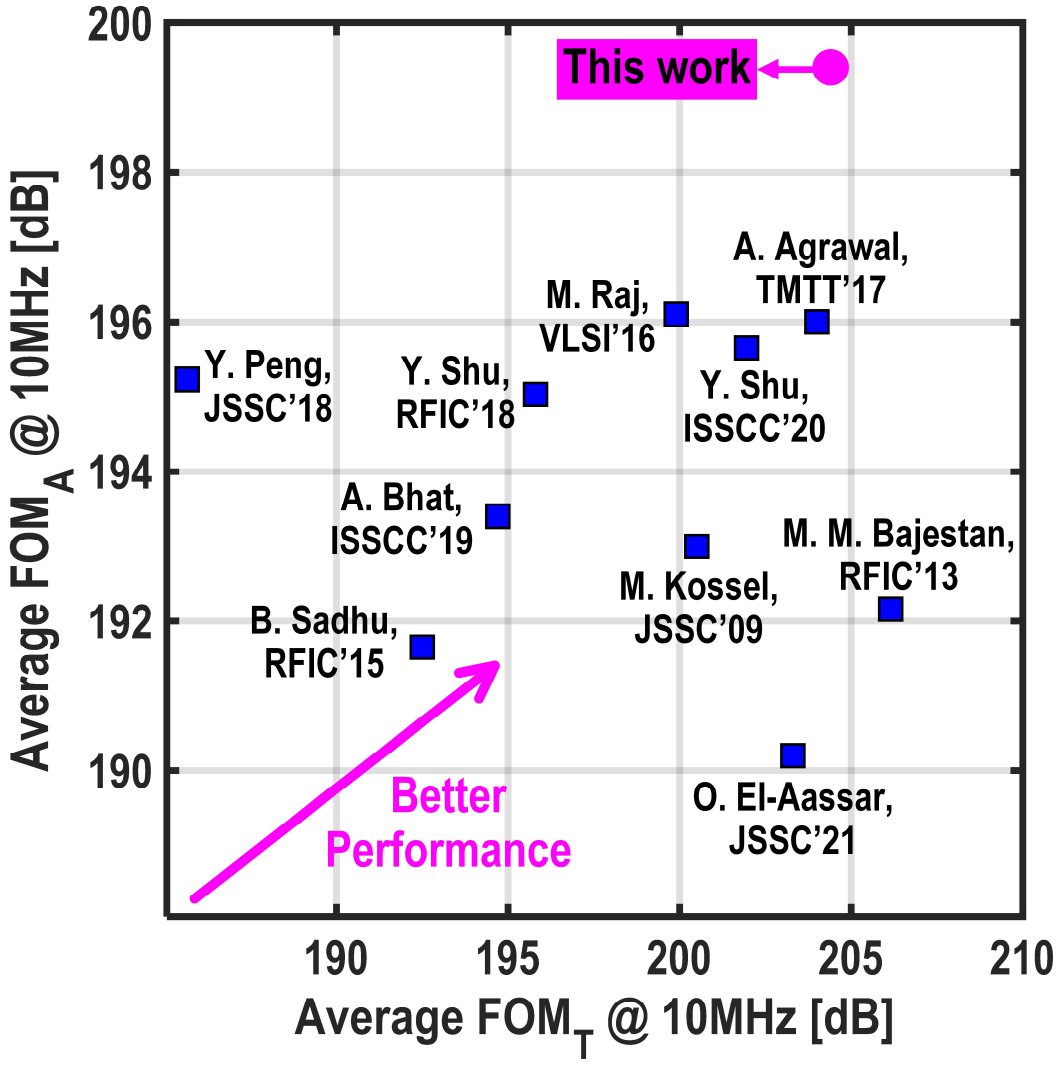
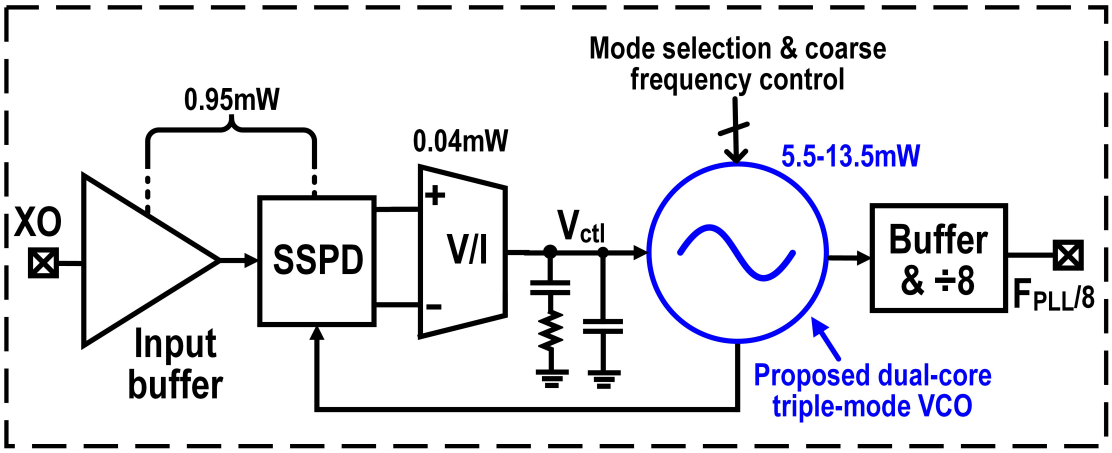


Fig. S.1: Average FOM_A versus average FOM_T performance of the existing continuous frequency tuning range mode-switching oscillators with oscillation frequencies higher than 6GHz. This work clearly demonstrates the best trade-off between the oscillator performance (i.e., FOM, and tuning range) and area.



	This Work	M. Raj, VLSI'17	D. Turker, ISSCC'18
PLL Architecture	Integer N, Sub-Sampling PLL	Integer N, Sampling PLL	Integer N, Charge-Pump PLL
Power Supply [V]	1.1	0.9/1.8	NA
Reference Freq. [MHz]	100	450	500
FTR [GHz]	7.1-16.8 (80.6%)	9-18 (66.7%)	7.4-14 (61.7%)
Test Frequency [GHz]	16	18	12.5
PN @ 100kHz/1MHz (normalized to 1GHz)	-136.6/-136.6	-129.2/-132.4 (@200kHz)	-135.9/-139.1
RMS Jitter, σ_{rms} [fs] [Int. Bandwidth]	78.2 (69~79)* [10k-30MHz]	164 [1k-100MHz]	53.6 [10k-10M]
Power, P_{DC} [mW]	7.6** (6.5~14.5)	29.2	45
^FOM_{PLL} [dB]	-253.3 (-254.5~-252)	-241	-248.9
^^FOM_N [dB]	-275.3 (-272.6~-275.8)	-257	-262
Core Area [mm^2]	0.078	0.39	0.35
Process [nm]	22nm FinFET	16nm FinFET	16nm FinFET

*Over the entire frequency tuning range **Include the power consumption of the input buffer

^$FOM_{PLL} = 20*\log_{10}(\sigma_{rms}/1s)+10*\log_{10}(P_{DC}/1mW)$ ^^$FOM_N = FOM_{PLL} +10*\log_{10}(F_{REF}/F_{PLL})$

Fig. S.2: Simplified block diagram of our analog sub-sampling PLL and its performance summary and comparison with prior-art wide tuning range PLLs. Thanks to the proposed compact and low-power triple-mode VCO, our FOM_{PLL} (FOM_N) advances prior art by >4dB (~13dB) while occupying 4x less area, using a 4.5x lower reference frequency, and offering the highest frequency tuning range.

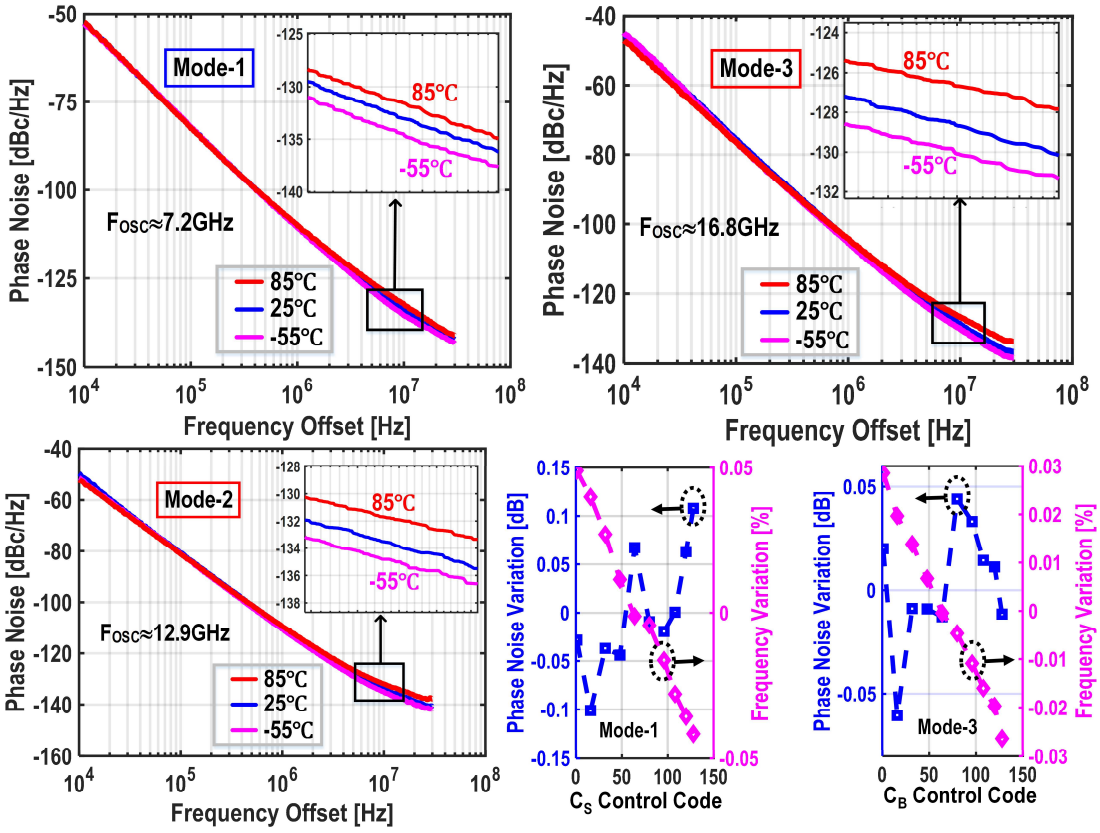


Fig. S.3: Measured phase noise plots of the VCO over operation modes for different temperatures, and phase noise and frequency variations by changing C_S (C_B) in mode-1 (mode-3). Thanks to the enhanced $R_{ON,D}$, changing C_S (C_B) in mode-1 (mode-3) has a negligible impact on the measured phase noise (<0.3dB) and oscillation frequency (<0.1%).