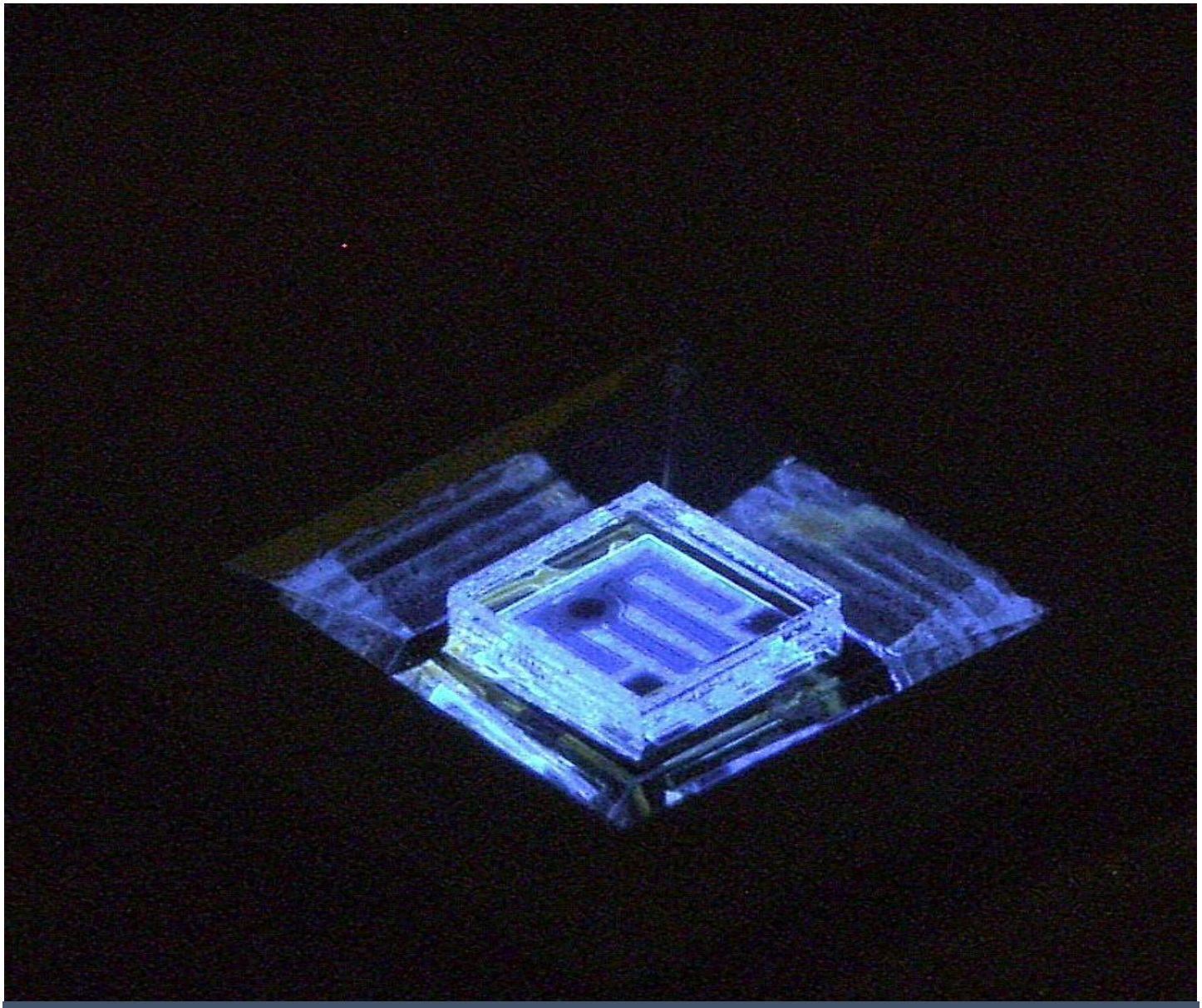

Wafer Level Packaging With Nano Metal Paste Interconnects For UV-C LEDs

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Philips TU Delft

Wafer Level Packaging With Nano Metal Paste Interconnects For UV-C LEDs

MASTER OF SCIENCE THESIS

by

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ABSTRACT

Light emitting diodes (LEDs) have made remarkable progress since their invention and today they can be found in a wide range of applications such as TV remotes, automotive headlamps, general lighting, traffic signals, camera flashes, display and screens. LEDs that emit light in the ultraviolet-C (UV-C) range are used in applications such as air/water purification and sterilization. Cost per chip of these LEDs is relatively higher than the blue LEDs due to the expensive manufacturing process and low demand. But, the market for these LEDs in applications such as water purification is expected to grow in the coming years into a multimillion dollar market resulting in high volume manufacturing and low cost of chips. Consequently there will be a need for high volume and cost effective packaging solution with excellent thermal and optical performance. Existing packaging technologies like ceramic and lead frame packaging are expensive, less productive, and offer limited processing options. Meanwhile, wafer level packaging is a highly productive and cost-effective solution. Today, Silicon is the most common substrate of the integrated circuits. Moreover, its close coefficient of thermal expansion (CTE) with the LED base materials such as GaN and AlGaN, and the high thermal conductivity make it a good choice as a substrate of UV-C wafer level package.

In this study we developed a silicon wafer level packaging approach combining advanced processes such as through silicon via (TSV) technology and chip to wafer (C2W) bonding for flip chip UV-C LEDs. We have integrated Si reflector cups for redirecting light from the sidewalls of UV-C LEDs using suitable material such as Aluminum. Complexities of a monolithic flow and the advantages of a dual wafer flow will be discussed. A new method to establish the interconnection in TSVs with metal nano pastes (MNPs) is introduced. The current vs voltage characteristics, optical performances, merits of reflectors, and improvements in spectral distributions of each package are measured and characterized. Different ways of bonding the chips to the submount and the thermal resistances of each package are studied. In conclusion we demonstrate the fabrication of a wafer level package for UV-C LEDs with a new cost-effective TSV interconnection method using MNPs. We also show that sidewall emission of the LEDs is redirected with almost no loss in light which will be suitable for applications like water purification and protein analysis where the target doesn’t encapsulate the LED.

1 INTRODUCTION

Light emitting diode (LED) is one of the most interesting additions to the rapidly expanding range of solid state devices in recent decades [1]. By utilizing a special case of luminescence entitled as electroluminescence, where photons are emitted from the recombination of electrons and holes as a result of applied electric field, LEDs can be found in vast amount of applications today. Due to their low power consumption and compact size, their initial applications included remote control, seven segment displays, switching indicators, traffic lights, etc. In the recent years their outstanding features such as rather low energy consumption, long lifetime, easy color tuning, predictable lifetime behavior, and low abrupt failure rate have put them in the scope of contention with conventional lighting sources like incandescent bulbs and fluorescent lamps [2]. This happened by the introduction of high-brightness blue LEDs (based on wide band-gap nitride materials such as GaN) that transformed the LED industry into a multi-billion dollar business by improving LED dichromatic white light sources [3] . Their potential for use in wide range of applications such as home, street, decorative, and automotive lighting; health care, display, and screens with low energy consumption has led the industry to increase research and development investments. This paved the way for the high volume manufacturing (HVM), and hence the considerable drop in price of the LED chip [2].

LEDs emitting in the deep UV range (200nm – 280nm, also known as UV-C range) are useful for applications like sterilization, water and air purification, ozone treatment, and vitamin synthesis that require UV-C light treatment [4][5]. The conventional sources for UV-C applications are high and low pressure gas discharge sources like mercury, xenon, and excimer lamps. Some of the downsides of these sources are high power consumption, low lifetime of few thousand hours, warm up time, and not being eco-friendly [6]. As a result, in some countries the new regulations have been issued to limit the usage of these sources and promote the use of LEDs instead [7].

Today, the optical performance of visible range illumination LEDs (EQE up to 80% with lifetime above 50000 hours) is acceptable to cope with the optical energy requirements of most applications. However, the optical performance of UV-C LEDs (EQE up 10 % with lifetime above 10000 hours) is considerably low compared to the conventional sources [8] [9] .

The performance of an LED can be characterized in terms of its power efficiency, so called wall plug efficiency (WPE), which is the ratio of the illuminated optical power to the supplied electrical power supplied both in watts. Another indication for the LED performance is in terms of light generation

known as external quantum efficiency (EQE), which is the ratio of the number of photons released per second into free space and the number of electrons supplied per second [8]. The concept of EQE is explained further in appendix 8.1.

An approach for optimizing the UV-C LED's EQE is through the use of better reflective metals such as aluminum for contact pads [10]. Moreover, a dedicated UV-C LED packaging solution can improve the light output and assist the bean in shaping/focusing. This can play an important role in directing the light towards the intended target as will be seen in the following sections. Finally, the junction temperature of the LED can be reduced with an optimized package that can better conduct the heat towards the heat sink.

1.1 Motivation

Due to the low efficiency of the UV-C LEDs, most of the supplied energy is dissipated as heat. This excessive heat at the junction of the LEDs affects the optical performance negatively over the operation time of the LEDs [11]. Hence lifetime is under threat for the already low optical power UV-C LEDs. Moreover, the effective thermal conductivity and contact resistance at the package interfaces are of high importance for their lifetime. Heat generated by an LED can be dissipated through conduction, convection, and radiation. Transfer through conduction can be controlled via the bonding with package. Flip chip LED (FC-LED) architecture has the advantage of good heat transfer that allows high current and therefore high optical power of the LED [12]. Some of the heat generated from an LED can be conducted through this contact area and the effectivity of conduction depends on the packaging architecture and materials' thermal properties.

Metal lead frames such as aluminum and ceramics like aluminum nitride (AlN) can be used as submounts for the FC-LEDs. But the high mismatch of thermal expansion (CTE) between metals ($23x10^{-6}/^{o}C$ for Al) and LED base materials ($3\text{-}6x10^{-6}/^{o}C$ for AlGaN and GaN) can cause cracks in LED base materials [13]. Whereas, AlN has CTE ($4\text{-}6x10^{-6}/^{o}C$) closer to the semiconductor materials in LEDs and is already being used as submount for few UV-C LEDs. However AlN is relatively expensive and this will make it an undesired factor for the future when low-cost high-volume of UV-C LEDs are a demand in the market [2].

Wafer level silicon packaging has been recognized as a high volume and low cost packaging solution for LEDs [13]. Silicon's low CTE of $3x10^{-6}/^{o}C$ and high thermal conductivity of 149 W/mK make it a good choice as a packaging material. The prominent use of silicon in fabrication of electronic products facilitates system level integration of LEDs with power drivers, sensors, reflectors, vias, etc. The die-

sizes of flip chips can be less than 1 mm^2 with complex anode-cathode patterns different for each manufacturer and hence the submounts need to be printed with a matching bonding pattern to ensure maximum contact. This is possible with existing silicon wafer processing and when combined with integrated electronics, it enables fabrication of packages for smart applications.

Reflectors can be incorporated into the silicon wafers to improve the optical power received by the targets by redirection of light from sidewalls of an LED with reflective metal coating such as aluminum. Aluminum is a very good reflector of UV-C radiation [14] [15] and is also one of the most used metals in silicon wafer processing. Therefore exploring the incorporation of aluminum as reflector could improve the beam focusing/ shaping from the LED.

Wire bonding is a common interconnect method used today for submount's connection to the next level of a package due to its low cost. However its disadvantages include a) low robustness, b) high bonding pitch, c) limiting current and die density, d) reliability issues etc., [16]. Also, it most importantly limits the further processing of silicon substrate wafer in a fabrication environment. Through silicon via (TSV) technology is a popular solution for interconnects which facilitates both thermal and electrical paths for the operation of LED. TSVs also help in miniaturization of packages. Metals such as copper can be used for the conduction by complete or incomplete filling of vias which could be achieved through plating, sputtering, and evaporation [17]. To ensure maximum thermal conduction, the vias need to be fully filled which is possible by electroplating of a sputtered seed metal layer. However, the cost and time of processing of plating could be very high depending on the dimensions of the vias [17]. Furthermore, the chemicals involved in plating often need to be disposed of with care for the environment. Hence there is a need for new methods to fill the vias with minimal processing cost and time. One such ways to fill would be with metallic nano materials (MNP) which is introduced in this work.

1.2 Objectives

Overall, this work aims to contribute to the optical improvement of the packaging technology of UV-C LEDs by studying new silicon wafer-level LED packaging and integration methods. This work attempts to establish packaging technologies consisting two types of chip-to-substrate bonding: a) Gold stud bumping and b) Gold-Tin soldering. Both flows are aimed for high volume production, low cost, and good light extraction by reducing the packaging levels. Highlights of the objectives are:

- Introducing a new way to fill the TSVs in silicon microfabrication environment
- Establish and compare the technical challenges in 3D-monolithic and dual wafer flows for packaging UV-C LEDs

- Improve the optical performance of the LEDs by redirecting the light from sidewalls
- Analyze the electrical, optical, and thermal performance of the packages
- Demonstrate the high productivity and low cost of silicon wafer-level packaging

1.3 Outline of the thesis

This thesis focusses primarily on presenting the design, fabrication, and characterization of a wafer level package for UV-C FC-LEDs the performances according to the set objectives. Brief introductions to key processes, measurement methods, and attributes of materials are given wherever necessary. Overall, this dissertation is organized into 9 chapters.

In chapter 2, a brief introduction to the industrial standard packaging technology platforms like lead frame, chip on board, and wafer level packaging is provided. The state of the art concept designs of 3D wafer level packaging with an overview on a recent implementation by a fellow researcher is also provided. Recently developed TSV interconnections achieved by DRIE/KOH etching and plating are presented. Finally, the properties of metal nano pastes (MNPs) and aluminum pertaining to their use in this research are described.

Chapter 3 summarizes the background information on the key process steps for silicon microfabrication used for our UV-C packages. It starts with the physical properties of a silicon wafer concerning the fabrication such as the planes, size, and doping type. The key processes in fabrication related to this research including lithography, deposition, and etching are also explained with the help of schematics.

In chapter 4, two package designs for UV-C FC-LEDs are proposed. The concept designs for two types of packages in both monolithic and dual wafer flows are described. Each flow for a final 3x3 mm^2 package is explained step by step with 3D schematics designed using COMSOL multiphysics.

In chapter 5, elaborates on the fabrication of the designed packages. First, the operational specifications and the geometry of the UV-C LED chips as per the supplier's data are summarized. Then the fabrication of the packages, based on the concept design from chapter 4 and the basic fabrication knowledge, is demonstrated. The SEM, microscopic, and full-scale images of the dies are used to present the implementation of the design along with the fabrication flow.

In chapter 6, the measurement results are discussed. The current vs voltage, optical, and thermal performance characterization studies of the packages are presented. The optical performance is studied without and with reflector cups using integrating sphere and goniometer measurements.

Finally, chapter 7 concludes this thesis by a short discussion over the challenges encountered during our research, process observations, and results in the previous chapters. It also proposes some ideas for future work aimed to improve the established flows of working with MNPs and to have a better protection from environment.

As supplementary explanation, we include chapter 8 as appendix. Here, more of the fundamentals needed to understand processes, recipes; process observations, and bottlenecks are presented as appendices. This section also describes some of the challenges and process adjustments.

In chapter 9, the referenced documents are listed.

2 LED PACKAGING REVIEW

Because UV-C LEDs emit higher energy light than visible LEDs, packaging solutions are more limited. Also, since most of the energy is converted into heat, it is important to adapt the most suitable packaging architecture for effective thermal dissipation. This chapter reviews and introduces the existing architectures used in the industry, the latest research in using TSV interconnects, and properties of few materials used for packaging in this research.

2.1 LED Packaging technology

A package for an LED facilitates the electrical connection to the LED through the electrical paths in its architecture, a transparent window for the light to escape, and a thermal path. Early packages came with LEDs sitting in a reflector cup that is also an electrical terminal (anode/cathode) and the LEDs' connection is completed by wire bonding to a different isolated terminal. The thermal resistance was not under serious scrutiny for the applications at the time. As the LEDs evolved into use for high power, high reliability, and longer lifetime requirements of applications, the thermal resistance (Rth) was under scrutiny. Thermal resistance is a measure of how effectively the package can conduct the heat from the LED to the heat sink. The lower the thermal resistance the better. The figure 1 shows the evolution of thermal resistance in LED packages since 1970s until the last decade.

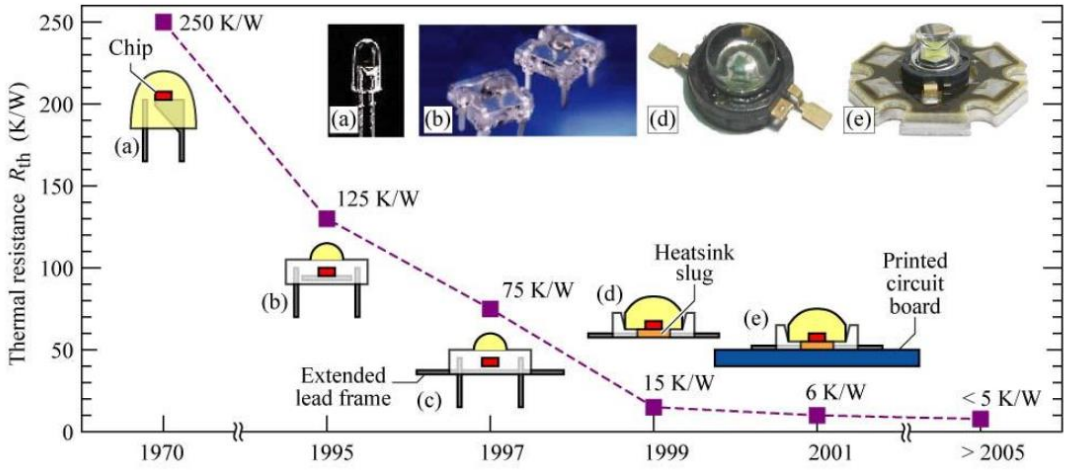


Figure 1: Thermal resistance of LED packages: (a) 5mm (b) low-profile (c) low-profile with extended lead frame (d) heat-sink slug (e) heat sink slug mounted on printed circuit board (PCB) [18] [5].

When high thermal power is required to be dissipated, a copper heat slug is placed under the LED's submount for better conduction as shown figure 1-d.

2.1.1 Lead frame packages

One of the solutions for effective thermal conductivity in high power applications is the LUXEON LED package developed in 1998. It was developed by Lumileds with a technique known as Lead frame plastic (LFP) that uses a metal slug like copper underneath the submount of the LED as shown in figure 2. This technique has later been incorporated in LED packages from organizations such as Osram and Seoul semiconductor. A schematic of the cross-section of an LFP package is shown in figure 2.

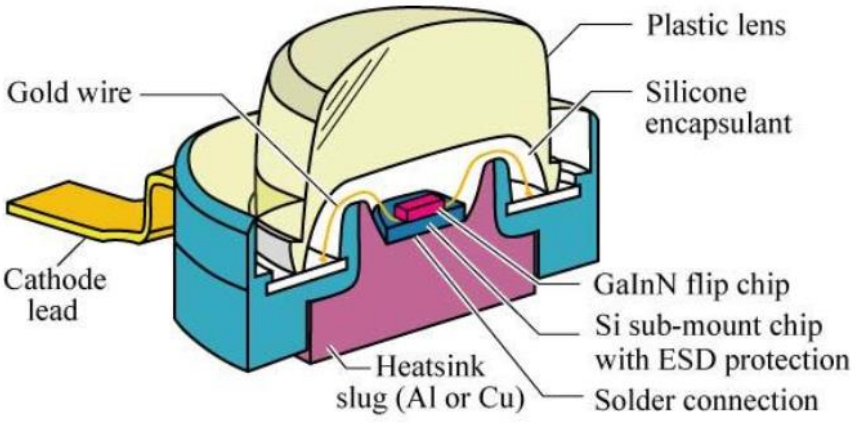


Figure 2: Cross-section of an LFP package [5], [18]

Improvements have led the LFP packages such as 'LUXEON K2' to achieve R_{th} as low as 5 k/W and let the LED to operate at a junction temperature of 150^{o}C, LEDs with forward currents up to 1.5A [19]. This is 50% higher than the earlier LUXEON package.

2.1.2 Chip on board packages

A compact architecture that reduces density of packaging is the 'chip on board' (CoB) [19]. CoB eliminates the heat slug from LFP and has the LED directly bonded to the PCB. This allows for a better thermal path by reducing the resistance stack and reduction in assembly materials that also reduces the cost when compared to LFP packages [19]. Despite the advantages, high density heat flux and CTE mismatch of PCB with the chip are a concern for CoB design [20]. A schematic of the cross section of a CoB is shown in Figure 3. An LED die is glued to the board with the electrical contacts facing upwards. Once the gold wires are bonded, the die is encapsulated and thus finishing the assembly of a CoB package.

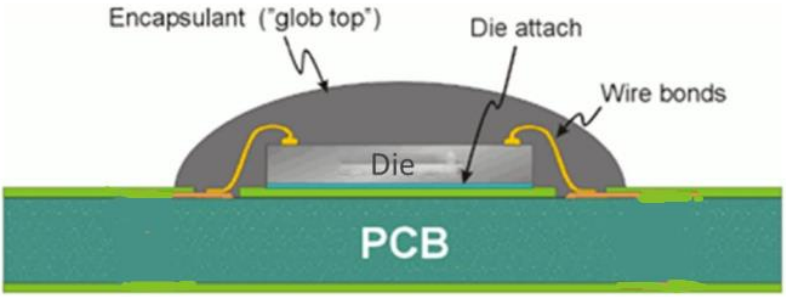


Figure 3: A Chip on board package [5][21]

2.1.3 Thermal resistance of LFP and CoB packages

A thermal resistance (R_{th}) network is the system of thermal resistances of materials in the package ordered in the hierarchy of heat flow. The total resistance of a network is just the sum of all the resistances of individual materials and their interface resistance with the neighboring material in the next level, starting with the junction of the LED and ending with the environment as shown in figure 4. The interface resistances remain the bottle necks for the heat conduction [22].

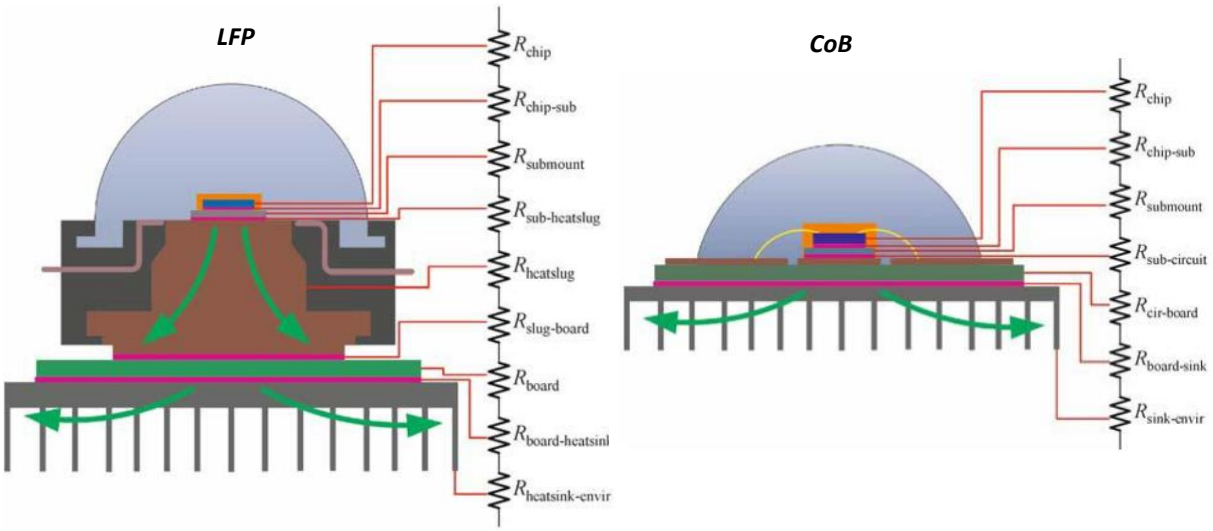


Figure 4: R_{th} network of LFP and CoB packages [22]

From figure 4 it can be deduced that the CoB package can have lower system thermal resistance than an LFP package, given the same materials and dimensions at the common levels of the packaging network.

2.2 Sate of the art 3D LED packages in silicon wafer level packaging

Existing state of the art packages combine concepts of TSVs, minimizing thermal resistance, light redirection, and integrating elements of smart design such as sensors and drivers [23]. A concept design is shown in figure 5.

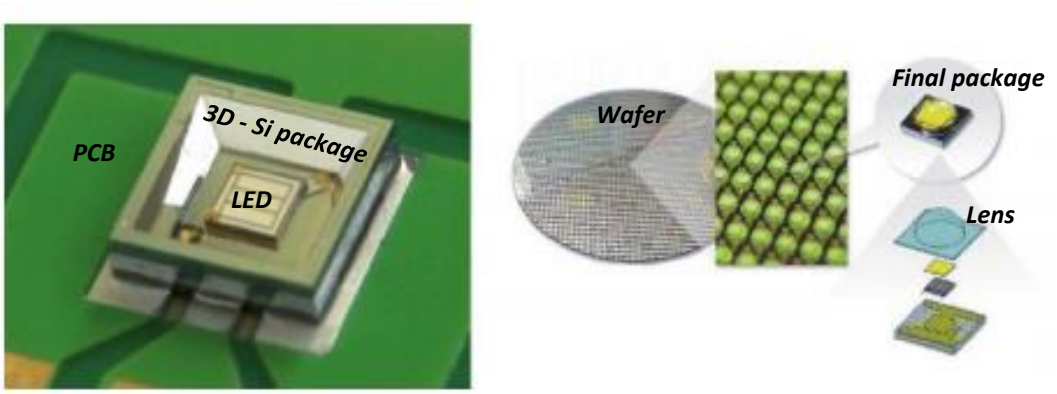
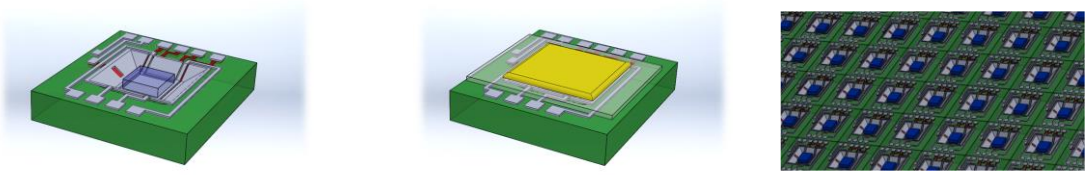


Figure 5:Design concept of state of the art LED packages in wafer level [23]

Z. Kolahdouz et al. [24], have implemented state of the art 3D wafer level packages for blue LEDs in TU Delft. The chips are glued to the silicon substrate for thermal contact and the electrical connection is established via 3D lithographic defied wire bonding. The packages combine 3D microfabrication, light redirection, current drivers, optical, and temperature sensors. The packages require complex BiCMOS mask flows with advanced 3D lithography. The design concept as provided by Zahra is shown in Figure 6. Figure 6-a is the state of the art design used for implementing an individual 3D package for blue LED, Figure 6-b is the same package with a remote phosphor plate to extract white light, and Figure 6-c is the processed packages on a wafer scale.



a) LED chip placement and bonding

b) Remote phosphor plate

c) Wafrer level 3D packaging

Figure 6: Concept design of state of the art 3D silicon packaging for blue LEDs (Zahra et al. [24]*)*

2.3 Merits of wafer level packages

A bottleneck for FC-LED attachment directly on PCB is the CTE mismatch between PCB and the chip. Elger et al. [20] have evaluated the architectures based on the new wafer level packaged LEDs (WLP-

LEDs) and benchmarked them with standard CoB modules based on ceramic and lead frame packages. The analysis has concluded that WLP-LEDs have better thermal performance than ceramic LED packages.

The thermo-mechanical stability of the FC-LEDs on IMS boards was investigated by temperature cycle tests. In each cycle, the temperature shock was induced at a high and a low temperature for 1 hour with 50% duty cycle. After 1000 cycles, 5% of the samples failed as a result of the increase in thermal resistance by 18 K/W. The cause was identified as the solder joint crack from CTE mismatch which is visible in the cross-section shown in Figure 7. A failed wafer's cross section shows visible cracks of solder. Hence the authors came to a conclusion that WLP-LEDs are the best choice for thermal design in high density applications. Relying on this study, silicon wafer package thermal performance estimation is left out of the scope of this work and the research is invested in thermal performance analysis and achieving the main objectives.

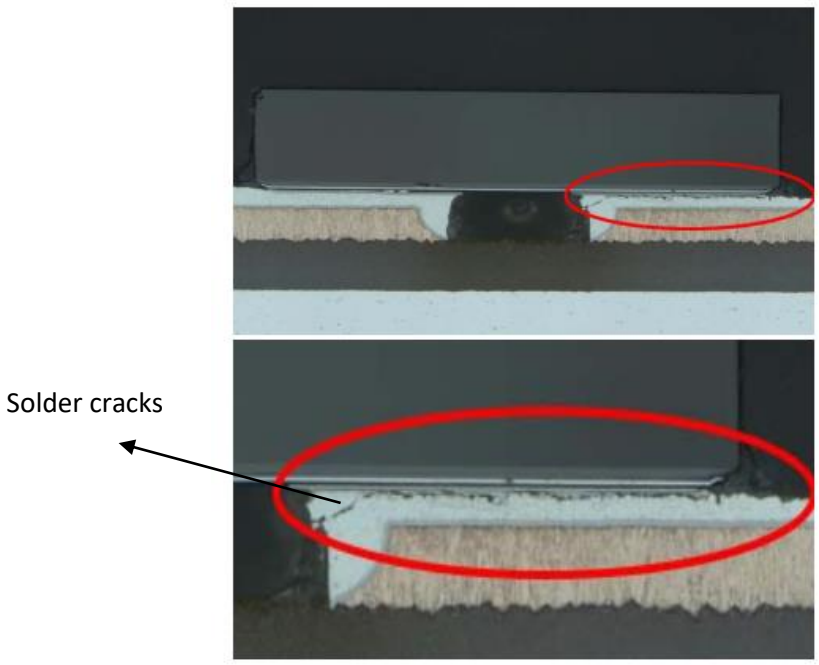


Figure 7: Cross-section of an FC-LED on IMS board with cracked solder joint after 1000 cycles of temperature stress [20]

2.4 Silicon packaging of LEDs with through silicon vias

By using dry and wet etching, flip chip LEDs can be packaged with TSV interconnects on silicon wafers. The electrical interconnection will be established from top to the bottom of the wafer through metals in the TSV. Sputtering and/or plating are commonly used today for establishing the interconnect vias. Rong Zhang et.al have developed LED packages with copper plated TSV for FC-LEDs attached with

bumping [25]. The concept design of the cross section is shown in Figure 8. The package is built for a stud bumped FC-LED.

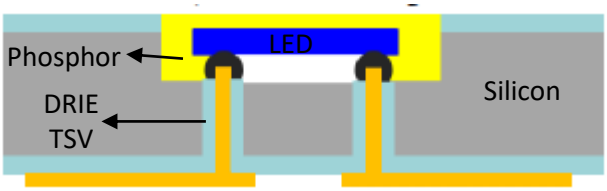


Figure 8: LED package with vertical TSV interconnects using DRIE and plating [25]

Similarly, Zhicheng et.al have used 'KOH etching' and plating to establish TSV interconnects to achieve a wafer level packages for LEDs [26]. The authors have mentioned time and cost as the major areas for improvement. The cross section is shown in Figure 9. The package is designed for a high power vertical LED chip.

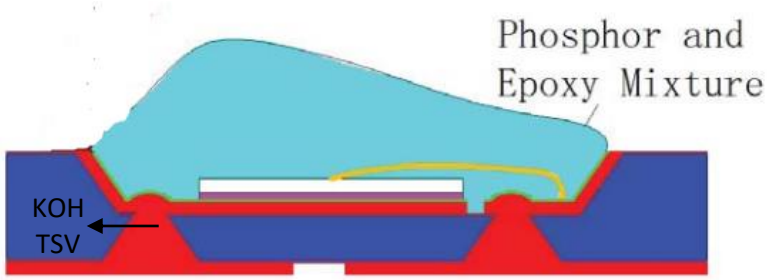


Figure 9: TSV interconnects achieved using KOH etching and plating [26]

2.5 Metal Nano pastes as TSV interconnects in packaging

Lead-free solders such as SAC (typically tin, silver, and copper) are predominantly used in today's microelectronic packaging. But they are not reliable as interconnects in ICs and there is a need to find intrinsic materials composed of just one metal [27]. One of the existing options are the metal nano pastes (MNP) which have been investigated to be used as solder material for fine pitch interconnects. Metal pastes of silver and copper are commercially available in the market. However silver pastes are much more expensive than copper pastes. These pastes are nano particles of metals with solvents preventing them from oxidation, and once sintered (heating at temperatures much less than the bulk counterparts of the metals) will leave the metal in the original shape (with some loss of mass) of the deposited paste[28].

The oxidation of the metal once sintered was proved not to occur $100^{o}C$ [28]. In this research, the 'DuPont Solamet PV416' silver nano paste and the 'Intrinsiq Materials CPN-1000P' are used. The silver paste is designed for use as a front-side conductor in CIGS and other thin film solar cell applications. It

has a sheet resistance of 8-12 mΩ/sq/25 µm and fuses between 130-180^{o}C. The copper paste has a sheet resistance of 40-60 mΩ/sq/5 µm and fuses between 225- 250^{o}C.

2.6 Aluminum reflector in packages for UV-C LEDs

LED chips can emit light from the side walls as shown in Figure 7 and since the UV-C LEDs' optical performance is not at the desired levels yet, it is crucial to extract as much light as possible in the direction of the target. In traditional visible LEDs, silicone is molded around the chip to better shape the emission pattern [18]. However, energy of the UV-C radiation is so high that it makes the silicone brittle over time, thus there is need for UV-C compatible silicone. From figure 8, aluminum is a material with reflectivity of more than 92% in the UV-C region [15] and it can be used to redirect the light towards a target with reflection rather than transmission like traditional silicone. Additionally, aluminum being one of the most commonly used metal in silicon fabrication is an advantage for integration of reflectors in UV-C packages. It can be patterned on the silicon package with the help of lithography [24]. Figure 10 shows the side wall emission of the UV-C LED used in this work.

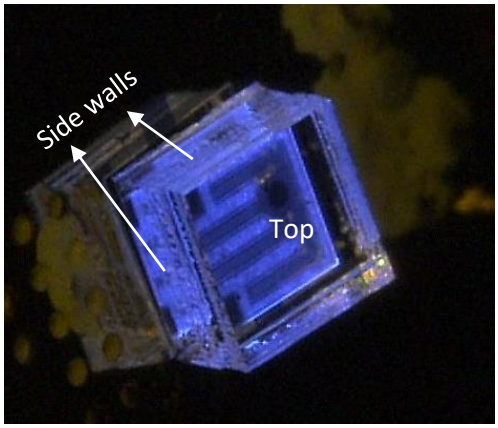


Figure 10: LED emitting light from sidewalls

Aluminum reflectance in percentage over wavelengths of 200 - 1000 nm is shown in Figure 11. As it can be seen, it stays constant from 200 nm to 500 nm and it reaches a lowest reflectance of 86.8 % at 820 nm and again reflects most of the radiation in RF and Microwave regions.

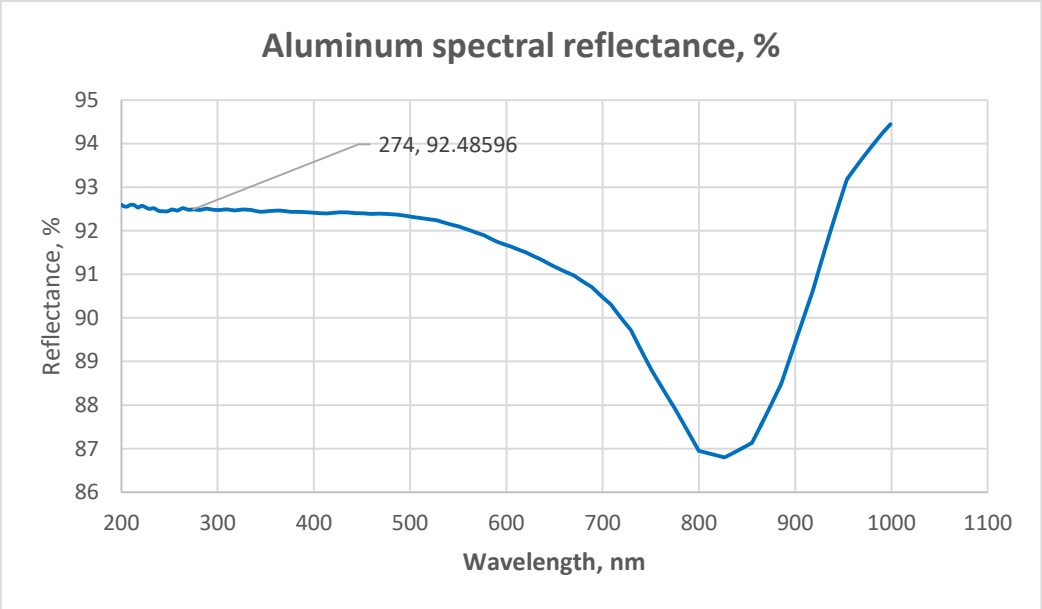


Figure 11: Aluminum's 92% Spectral reflectance in the wavelength range of the UV-C LEDs [15]

2.7 Summary

In summary, the junction temperature of an LED depends strongly on the package architecture and the resistance network with the lowest R_{th} is more suitable for optimal thermal conductivity, in consequence CoB is more suitable than LFP for UV-C LEDs. Additionally, CoB packaging with silicon submounts allows for low cost and high volume manufacturing with addition of materials like aluminum for light redirection.

Introduction to key processes in UV-C LED Si WLP

In this chapter we briefly discuss some key silicon microfabrication processes involved in this work performed at Else Kooi laboratory in Delft University of Technology.

3.1 Silicon wafer properties

For decades, high purity crystalline silicon wafers have been used as carriers on which integrated circuits are made. Silicon wafers are thin (often less than 1mm thick) circular slices of semiconductor material. Very large scale integration (VLSI) of circuits is today possible with the advancements in patterning to print fine structures. Whereas high volume manufacturing (HVM) is made possible with repetitions of identical circuits disconnected from each other spread over an entire wafer and each identical section is called as a 'die'.

Silicon has a regular face-centered diamond-cubic crystal (which is anisotropic) structure. It is least dense in (100) plane and most dense in (111) plane [29]. This anisotropic property gives it different mechanical properties in different planes. Figure 12 shows the lattice structure of silicon with lattice constant 'a' and different densities in different planes. Plane (111) in Figure 12-c has the highest density of atoms while plane (100) in Figure 12-(a) has the lowest.

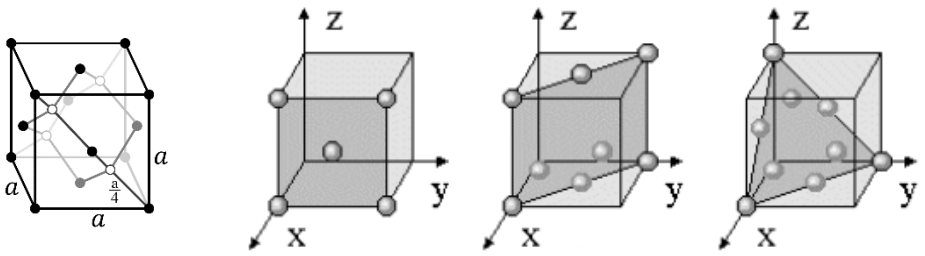


Figure 12: Silicon lattice structure and crystal planes [29]

Once silicon is grown in bulk, it is sliced into wafers in different planes and most commonly available wafers are in (100) plane. The wafers come with 'flats', a primary flat and a shorter secondary flat whose relative positions indicate the doping and the plane of the wafers. The

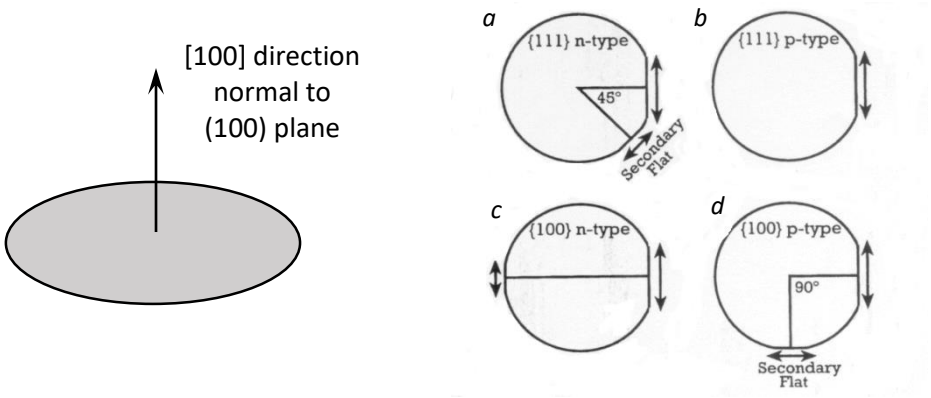


Figure 13: Orientation of growth plane of silicon wafer and types of wafers [30]

The types of silicon wafers used in this work are: 525 µm thick single side polished n-type (figure 13-c) and 300 µm thick double side polished (DSP) p-type (d). Both are in (100) plane and 4 inch in diameter. The die size on both types of wafers is 6mm x 6mm. In order to build a functioning circuit a combination of deposition, patterning, etching, and modification of electrical properties is needed. Different varieties of deposition, etching, and patterning are used in this work which the main principles are elaborated in the following.

3.2 Thin film deposition technology

Deposition is a process which grows or transfers a material onto the wafer. Most widely known process for depositing insulating layers like silicon nitride (Si_3N_4, often known as nitride) and silicon dioxide (SiO_2, often known as oxide) is chemical vapor deposition (CVD). Extremely thin layers of films can be deposited with CVD and is often controllable to an accuracy of few nanometers. Low pressure CVD (LPCVD) and plasma enhanced CVD (PECVD) are variations of the CVD process for high (generally > 500^oC) and low (generally 350^oC-500^oC) temperature depositions respectively. LPCVD nitride is commonly used as an insulator and chemical barrier in silicon processing due to its high resistivity (10^{16} Ω-cm) and extremely low etch rates to many chemicals used in semiconductor processing. PECVD nitride or oxide can be used for insulation when wafers contain materials that can't be subjected to high temperature stresses (for example metal layers). However PECVD films suffer from disadvantages including higher non-uniformity, higher reactivity to chemicals, lower electrical resistivity, and inferior dielectric properties.

Whereas physical vapor deposition (PVD) is a well-known process used for deposition of metals in vacuum such as aluminum, copper, and gold. It differs from CVD by not subjecting the wafer to high temperatures (often less than 100^oC) and by using vapor of the material to be deposited on the wafer. PVD allows a wafer to have multiple materials deposited on top of each other in a single process cycle

(for ex: chromium and gold). Sputtering and evaporation are two of the most commonly known PVD processes for metal deposition in today's processing industry. The schematic of a silicon wafer with oxide deposited is shown as an example in figure 14.

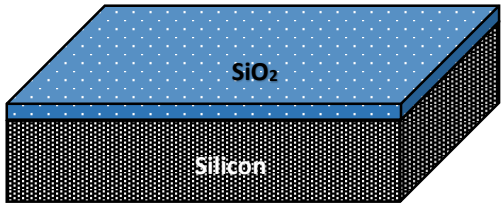


Figure 14: Example of oxide deposited on top of silicon

3.3 lithography defined patterns

A deposited material often needs to be patterned into fine structures according to the process design with the help of etching or lift off in selected areas. The fine patterns can be imprinted with the help of a process known as photolithography. It typically has 3 steps: coating, exposing, and developing.

3.3.1 Coating

First a light sensitive chemical called photoresist is coated on top of the said material with automated spin coating machines or spray coating machines. Depending on the type of resist, when exposed to the right amount of UV light it hardens and becomes relatively chemically inactive for few chemicals or plasma which otherwise would remove the resist much faster hence giving the protection to whatever material is underneath it for longer periods of time. When treated with the right chemicals, positive photoresist is removed in the areas exposed with UV light and vice versa for negative photoresist. A schematic of a coated resisted to pattern the oxide is shown in figure 15.

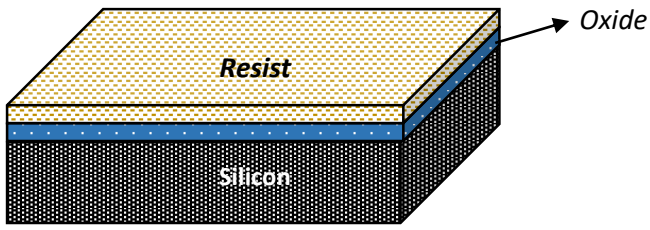


Figure 15: Schematic of resist coating

Adhesion of a resist to the wafer surface is improved by evaporating a chemical named hexamethyldisilazane (HMDS) onto a surface prior to coating. The adhesion is made even stronger with

increased viscosity by baking the resist at high temperatures typically in the range of 90°C - 115°C for few minutes. The automated spin coating machines normally perform the HMDS and resist coating, baking steps depending on the pre-defined recipes. The thickness and uniformity of the photoresist depends on the choice of resist and spinning profile defined in the recipes. Spin coating is used for wafers with flat surfaces. Whereas spray coating is often used for wafers with non-flat surfaces, cavities, or holes.

3.3.2 Exposure

After coating and baking, the resist is exposed with UV light with the help of a photomask which allows light through a pre-defined pattern that has to be printed on the photoresist. The exposure is chosen such that the resist reacts throughout its thickness. The schematic of exposure with an example pattern is shown in figure 16.

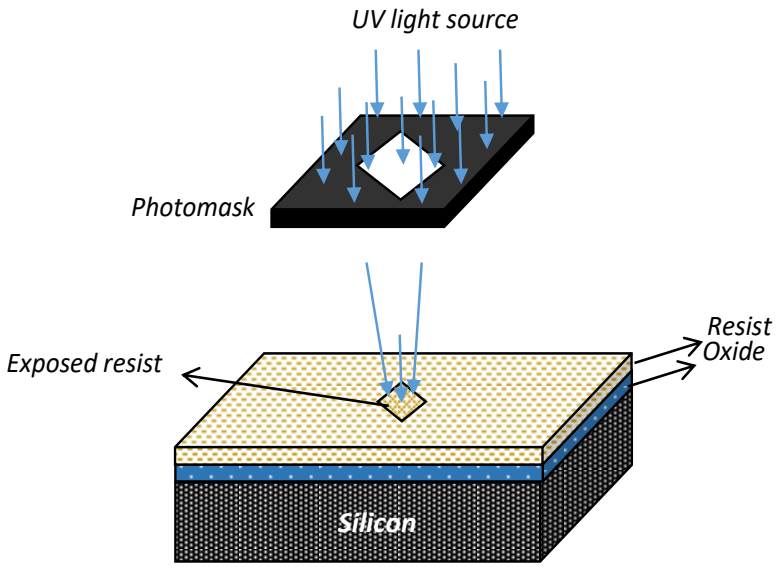


Figure 16: Schematic of UV Exposure of a sample pattern with photopmask

The exposure is done by a machine called 'stepper'. It aligns the wafer and the photomask to a high degree of accuracy and exposes the areas of the wafer according to the software. The reacted regions can be washed away in a developing solution. The size of the printed patterns on the wafer are scaled down by a factor of the size of the patterns on the photomask. The stepper used in this work scales down the features by a factor of 5.

3.3.3 Development

After exposure, the wafer is sent for development in a solution referred to as 'the developer'. During development, the exposed part is dissolved while the unexposed part stays if it is positive resist (vice versa for negative resist). The developer needs to be chosen according to the type of resist, for example AZ-400K (diluted) and MF-322 are used in this work. The wafer after development is shown in figure 17.

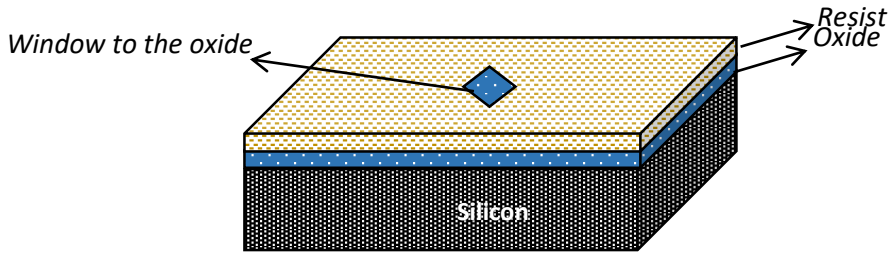


Figure 17: Schematic of a developed pattern forpositive photoresist

In the case of negative photoresist, the resist would remain in the exposed area while the rest dissolves away.

3.4 Etching

Once the windows to the material to be etched are open, the wafer can proceed to dry or wet etching. The time of etching will depend on the etch rates. Once the etching is finished, the resist needs to be stripped and sent for a cleaning step (normally involves acid like HNO_3). After the cleaning, a wafer is ready for the next process step. The etched oxide is shown in figure 18.

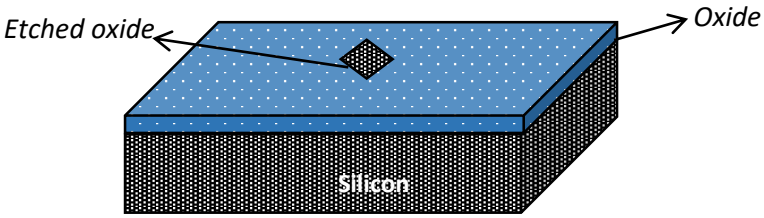


Figure 18: Schematic of the wafer after etching cycle (incl. stripping the resist)

For example the next step could be to use the oxide as the mask layer and etch the silicon through the oxide window. Wet etching or dry etching can be used depending on the required profile of the material after etching. Different profiles of etching exist: anisotropic and isotropic.

When a material is attacked by an etchant, as shown in figure 19,it can be removed anisotropically (uniformly in vertical direction, figure 19-a) or partially anisotropic (selected planes, figure 190b) or isotropically (uniformly in all directions, figure 19-c).

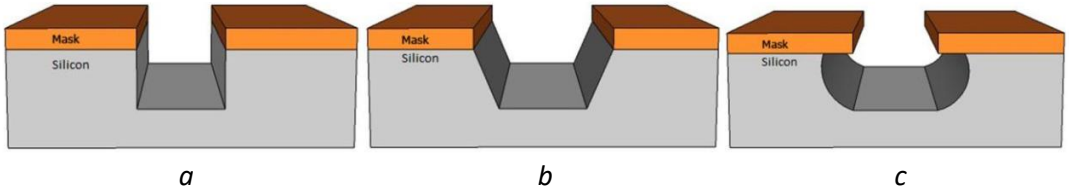


Figure 19: Etching profiles a) completely anisotropic b) partially anisotropic c) isotropic

Generally, fully anisotropic profile can be achieved just with dry etching and isotropic profiles can be achieved just with wet etching, whereas partially anisotropic profiles can be achieved with both dry and wet etching.

3.4.1 Wet etching and dry etching

Wet etching is a material removal process that uses liquid chemicals to remove materials from a wafer when it is put in the etching batch. The etching is a result of chemical reactions between the etchant and the material on the wafer. The key steps include transport the reactants to the target surface, oxidation of the surface, and transport the products from the surface. This process repeats and the key ingredients of a wet etchant bath are: oxidizer (e.g. H_2O_2, HNO_3), acid/base (e.g. H_2SO_4, NH_4OH), and dillutent media to transport reactants/products (e.g. H_2O, CH_3COOH). In some cases the etch rate of a material can be accelerated by increasing the temperature of the bath, therefore temperature enhanced etching is quite often used in the processing industry.

Dry etching uses bombardment of ions or etching vapors to etch the material on the wafer in vacuum. A high energy bombardment raises the temperature of the wafer and hence the wafer is often placed on a cooling chuck. Dry etching etches the atoms of a material unprotected by the mask at a faster rate that it does the atoms of the mask. If the etching is performed by ions it is called physical dry etching, whereas if the etching is performed by chemical reaction between the etchant gasses and the target material it is called chemical dry etching. In this work we use a special case of physical dry etching called reactive ion etching (RIE) for etching nitride and oxide of few nano meters. And for etching deep structures (>100um) in silicon a combination of both physical and chemical dry etching called deep reactive ion etching (DRIE) is used. DRIE etching is explained in detail in appendix 8.3.1 DRIE of silicon

3.5 Summary

In summary, we introduced and discussed the microfabrication technology related to this work available at the EKL laboratory. In chapter 4 we design the UV-LED packages which can be fabricated using the process steps discussed in this chapter.

4 PACKAGE DESIGN

In this chapter we design the silicon packages for two UV-C LEDs based on the established knowledge of the silicon microfabrication from the previous chapter. The design approach is explained with the aid of 3D structures of the package created with COMSOL multiphysics.

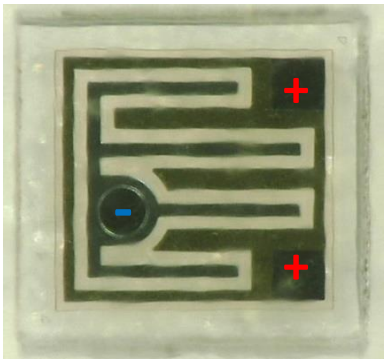
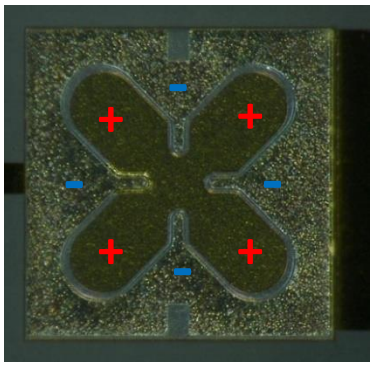
Two types of flows are designed for two LEDs (say, LED-A and LED-B): Monolithic and dual wafer flows. Monolithic package is used to package one LED. Whereas, dual wafer flow is used to package two LEDs with just the interconnect pattern step being the difference. Therefore at the end of this chapter, there will be three different packages designed, two of which are for one LED.

4.1 Package requirements and target LED specifications

The packages were designed for two different UV-C LEDs[1]. Both LEDs are manufactured in flip-chip architecture with isolation-oxide layer in the cathode-anode separation areas. Both LEDs have gold contact pads where LED-A is designed for gold stud bumping (Au bump) and LED-B is designed for gold-tin (Au-Sn) soldering.

The attributes with average values and the microscopic images of both the LEDs are summarized in table 1.

Table 1: Attributes of LED- A and LED-B

Attribute	**LED-A**	**LED-B**
Image of the FC - UV-C LED chip		
Chip architecture	Flip chip	Flip chip
Contact pads	Gold finish	Gold finish
Avg. Optical power, mW	17	10
Avg. Thickness, µm	400	100

[1] The commercial names of the suppliers are undisclosed

Avg. Size (length x width), um^2	780 x 750	690 x 680
Avg. Wavelength, nm	277	272
Avg. Current, mA	100	150
Avg. Voltage, V	6.4	10
Substrate bonding type	Gold bump	Gold – tin (80-20) solder
Package type	Dual wafer	Monolithic and dual wafer

Multiple packages were designed in pursuit of better light extraction, new cost-effective way of via filling, HVM, low-cost, low resistance 3D-TSV interconnects, decreased levels of packaging materials, establishing a chip specific flow for monolithic wafer-level packaging and common flow of packaging for multiple FC-LEDs. Photolithography is a well-established fabrication technique for patterning with high throughput and when established in an industrial environment with dedicated equipment, cost per chip could be low in HVM production. However the capital cost of research and educational facilities are quite high and the operating hours of the cleanroom facility imply the operational costs.

Usually, number of litho steps correlates to the time spent in a research cleanroom environment and hence the processing costs also depend on number of litho steps. This is one of the reasons for the choice of two different process flows: a monolithic package for LED-B with 7 litho steps and a common dual wafer flow for LED-A and LED-B with 4 and 5 litho steps respectively. With manual adjustments on the backside of the wafer it was possible to bring the dual-wafer flow litho steps even further to 3 and 4 respectively as will be seen in the next chapter.

The following sections will introduce the design of both flows starting with the monolithic design.

4.2 The Monolithic packaging concept design for LED-B

This flow is designed for a package in a single wafer with processing on both sides. The since the size of the chip is 100um, the 300um thick double side polished (DSP) 100 p-type (boron) wafers are chosen for implementation. Each package is 3 mm x 3 mm x 0.3 mm in size with the LED to be bonded on the bottom of the cavities. The final design of a single monolithic 3 mm x 3mm package is shown in the figure 20 .

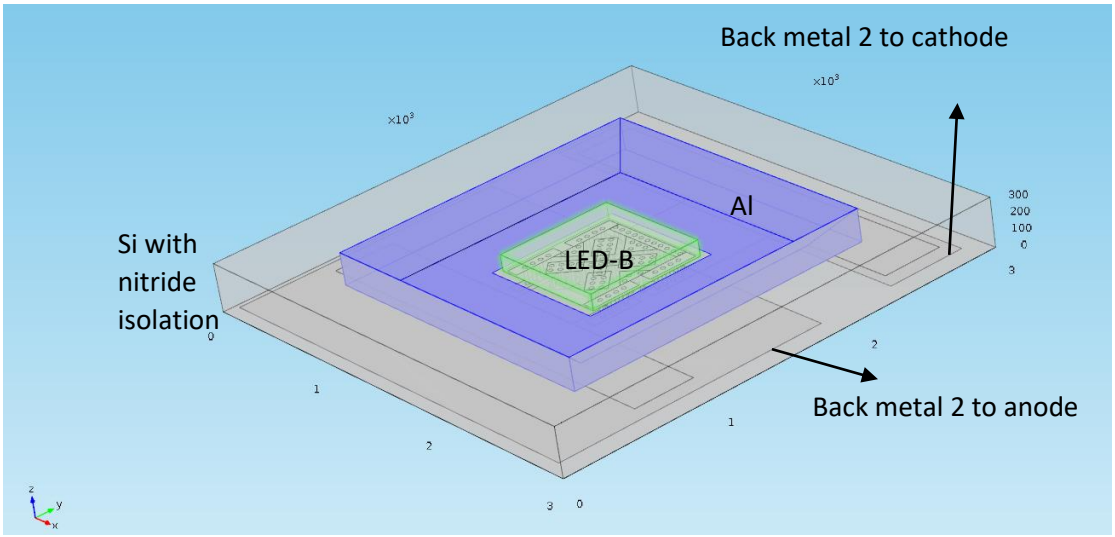


Figure 20: The Monolithic design of a single 3 mm x 3 mm package for LED-B

Note: all the axes are in micrometers.

Going through the design, let's follow the main steps one by one. We start with double side polished Si wafer and made the zero layer and alignment markers on both sides. The design steps are as follows.

4.2.1 LPCVD nitride depostion

A 4" diameter wafer is covered with 200nm of nitride in 'Tempress systems' LPCVD furnace which takes 28.5 minutes to deposit from ammonia (NH_3) and dichlorosilane (SiH_2Cl_2) at a temperature of 700^oC-800^oC.

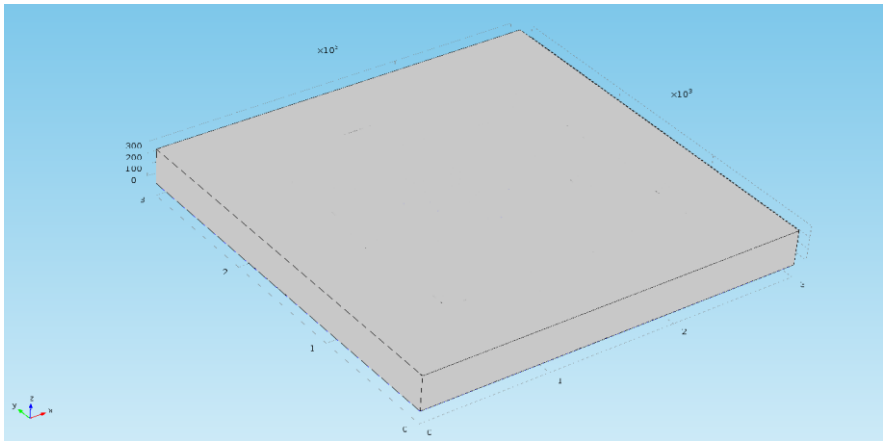


Figure 21: A 300 µm thick 3 mm x 3 mm silicon substrate covered with 200nm of nitride

4.2.2 Cavities - KOH etching

The deposited nitride is used as the mask and it is patterned in 2 mm x 2 mm open squares with lithography and dry RIE etching. Then the wafer is sent to KOH etching in a 33.33% (kg/liter) KOH bath which anisotropically etches the wafer in <100> directions at 1.6 µm/min in a 54.7^{o} angle with <111> directions. The wafer is taken out of the KOH bath when the etching reaches 200 µm deep as shown in the concept design in Figure 22.

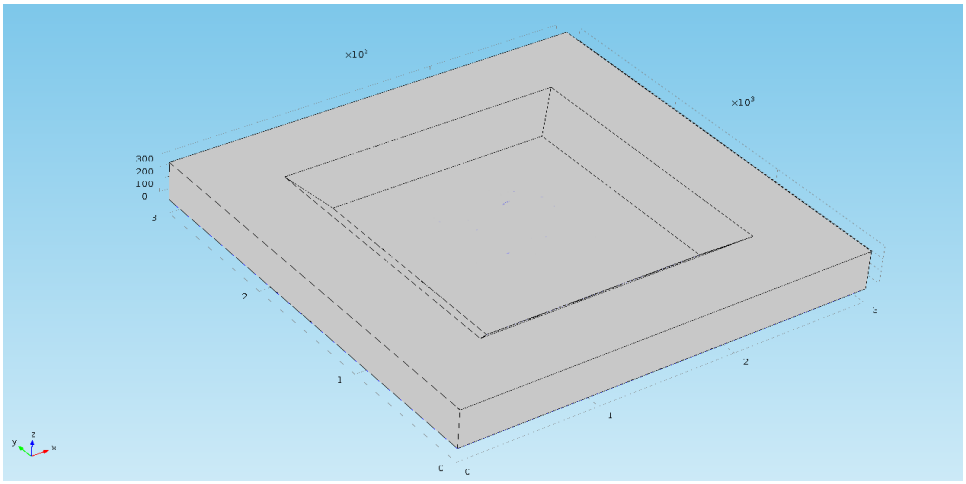


Figure 22: 3mm x 3mm substrate after KOH etching leaves 100 µm at the bottom of the cavity

4.2.3 Etching via pattern – DRIE

After the cavities are etched, the nitride on the wafer is cleaned and is sent for PECVD oxide deposition on the backside. The oxide is patterned with the via pattern performed on 'Drytek Triode 384T' RIE etcher using resist as the mask. Then this patterned oxide is used as a hard mask for etching silicon using 'rapier omega i2L' DRIE etcher for the depth of 100 µm where the vias through to the cavity on the other side. The side view with isometric view inset is shown in Figure23.

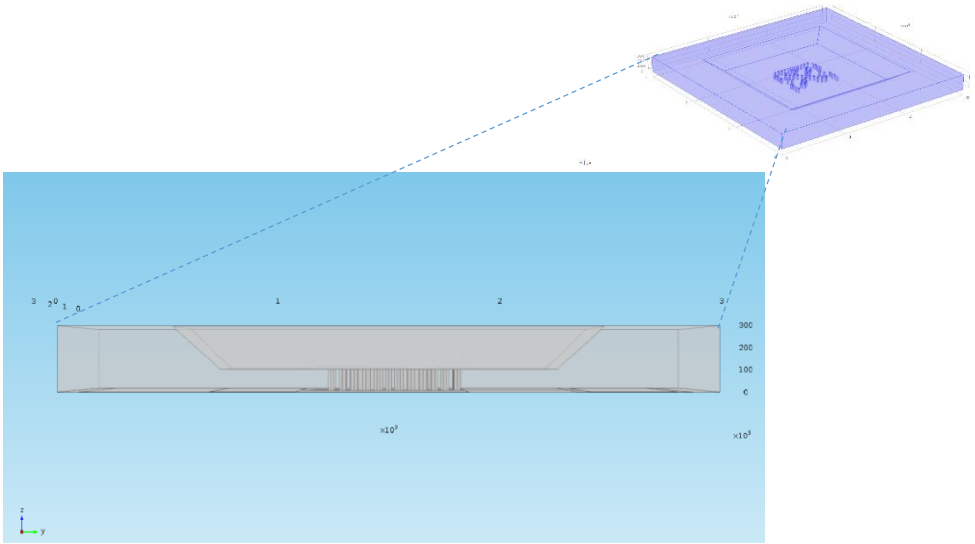


Figure 23: Substrate after etching vias using DRIE

The resist and polymers on wafer are long-stripped in 'Tepla Plasma 300' plasma etcher for 30 minutes and then the wafer is sent to the standard HNO3 cleaning before going to the next step.

4.2.4 Aluminum reflector – sputtering and etching

To fabricate the reflector for UV-C radiation on the cavity walls, 300nm thick AlSi is sputtered on the top side of the wafer using 'Trikon sigma' sputtering machine. Next, spray coated resist is patterned at the bottom of the cavity using the stepper with the focus shift of 199 to uncover the AlSi for etching. After developing, it is etched at the bottom of the bottom of the cavity with wet etchant PES for 2 minutes. Then to etch the poly silicon away, it is sent to poly-etch for 30 seconds before dissolving the resist away in acetone and sent to standard cleaning. Figure 24 shows aluminum patterned as reflector.

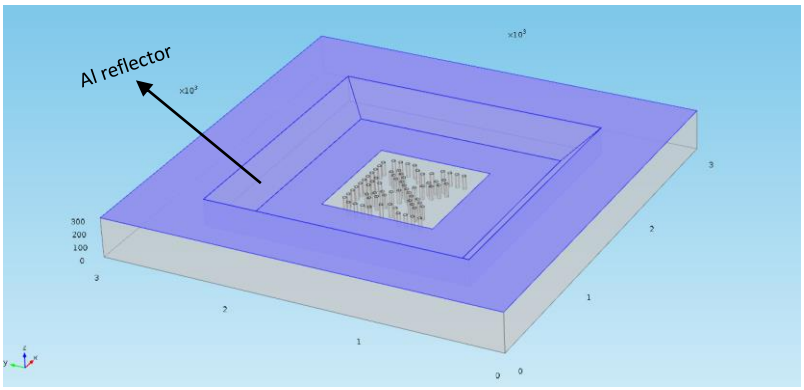


Figure 24: Aluminum reflector after etching

4.2.5 Filling the vias

The nano copper paste is used to fill the vias manually by applying puddles of paste with a syringe on top of vias from one side and vacuum from the other with the help of a vacuum chuck. Once the vias are filled, the puddles are wiped off using isopropanol (IPA) and a hard rubber. If the wiping is not clear, the wafers are spray coated with resist before applying the metal nano paste. So the paste residues on top of the resist will be washed away once treated with acetone after a soft bake. If photo resist is used, then the wafer is soft baked in an oven for an hour at 75^{o}C in vacuum and presence of nitrogen gas (N_2). After the soft bake, the wafer is cleaned with acetone and taken back to the oven for a hard bake at 250^{o}C for 2 hours in vacuum and presence of nitrogen gas (N_2), this step is called 'sintering' where the solvents evaporate and the nano metal particles fuse together.

4.2.6 Back metal 1 with pads away from the chip area – Sputtering and etching

When the vias are filled and sintered the anode and cathode vias are still on the same level and are not ready to be soldered onto a PCB. This is because the anode and cathode vias are too close to each other and they need to be separated for easy soldering on the PCB. So, copper is sputtered on the back and etched such that two separate contact pads are connected to anode vias and cathode vias. The design of metal 1 after patterning is shown in Figure 25 .

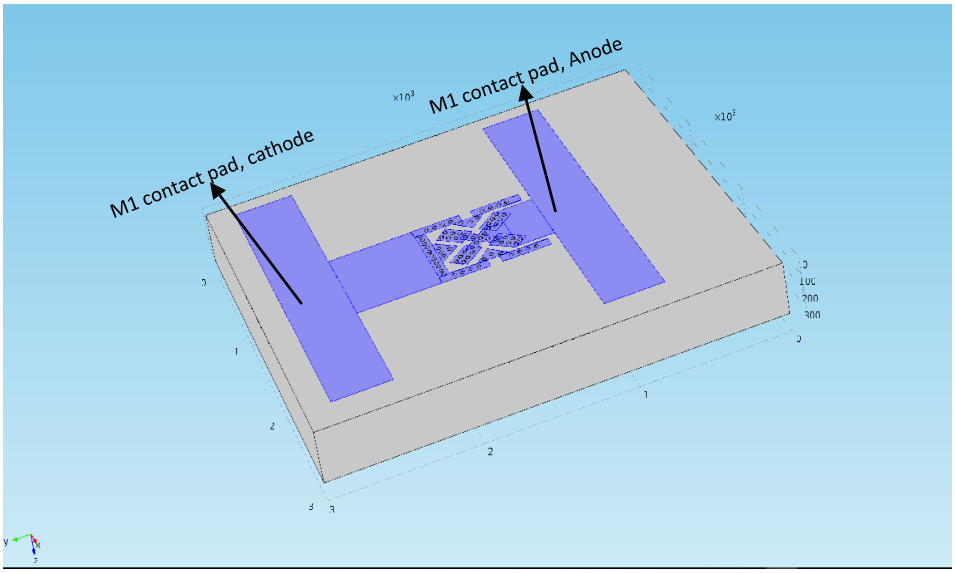


Figure 25: Back Metal 1 - Copper pads of metal 1 (M1) connecting anode vias and cathode vias

4.2.7 Isolationoxide on top of M1 – PECVD and etching

A 500nm of TEOS oxide layer, using 'Novellous concept 1' PECVD machine is deposited on the back side of the wafer and opened on just the contact pads of metal 1 so that metal 2 with a larger area can be deposited on the back side which makes contact with metal 1 though the contact openings in oxide. The Figure 26 shows the schematic of the package after patterning the contact openings (CO) oxide (in green) deposition on top of back metal 1 (in blue).

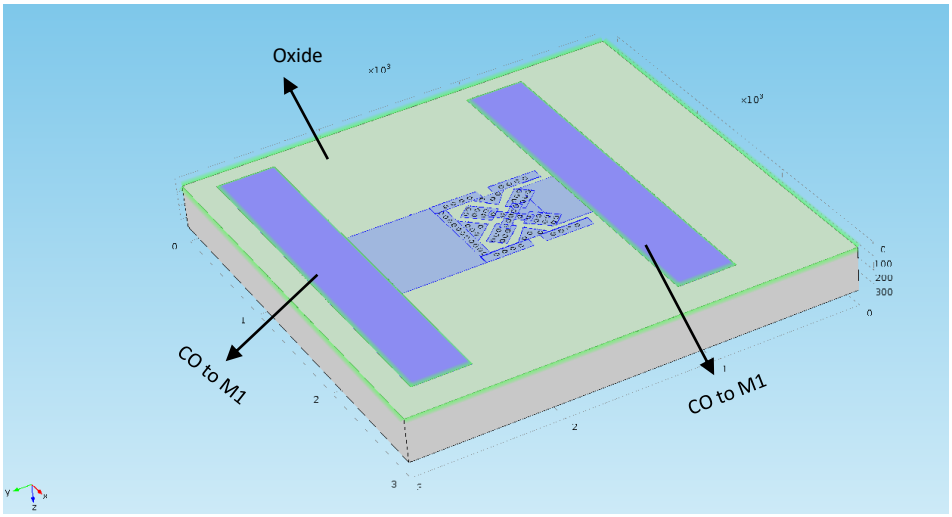


Figure 26: Contact openings (CO) through oxide to Metal 1

BHF (1:7) is used to etch contact openings through the oxide which etches the oxide isotropically at 160 nm/min.

4.2.8 Back Metal 2 – evaporation and lift off

Back side is patterned with negative photoresist for lift-off of gold (Metal 2). First a 20 nm think chromium is evaporated for better adhesion of Gold to oxide and copper. Evaporation of chromium is followed by evaporation of 300nm think gold. The evaporation is done in 'Balzers BAE 370 Cr/Au' evaporator. Then the wafer is taken for lift off in n-methyl-2- pyrrolidone (NMP, heated to 70^{o}C). Here the materials deposited on top of resist will be lifted off while the metals deposited on the wafer surface stay. The 3d schematic of the back metal 2 (in blue) on top of oxide (in green) is shown in figure 27.

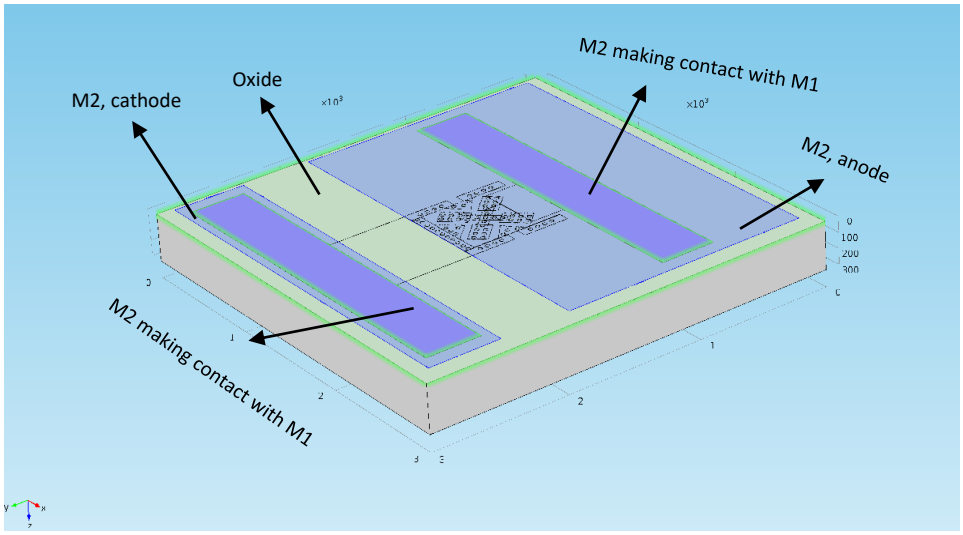


Figure 27: Metal 2 (Gold) contacting M1, after lift off

4.2.9 Solder on top of vias – sputtering and liftoff

Back side processing is finished and there is one last step before dicing and attaching the chips to the individual 3 mm x 3mm packages i.e. depositing the Au-Sn (80-20) eutectic solder on top of the vias through sputtering on the front side for the chip bonding. This is a lift off process like the last step (M2). Once the solder is deposited, a lift off is performed and the wafer is ready to be diced into 3 mm x 3 mm packages which look like the schematic shown in figure 28 .

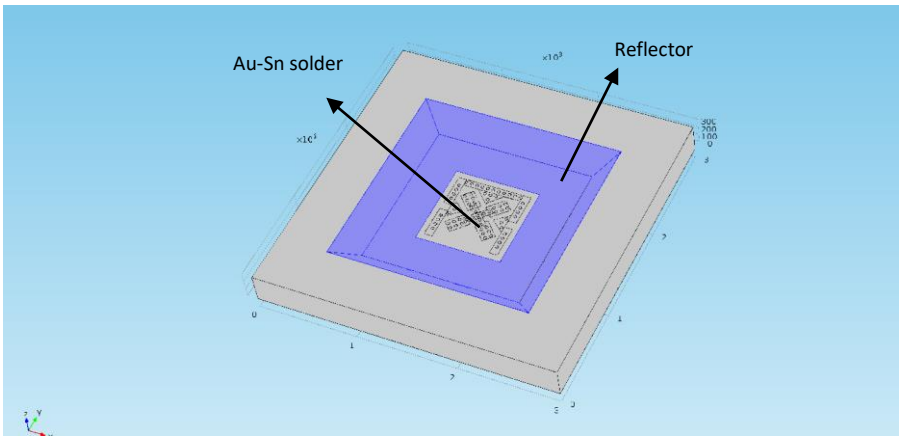


Figure 28: Final processing step Au-Sn (80-20) solder deposited on top of vias with lift-off

4.2.10 Chip bonding

The final step in completing the package is to bond the chip to the substrate. When the Au-Sn composition is 80% - 20% the eutectic melting point drops to 278^{o}C. Considering the thermal capacitance of the package, the substrate must be heated on a hot plate to a slightly higher temperature than 278^{o}C for the solder to have 278^{o}C. When the melting point is reached, the chip is held in place on the solder by a vacuum nozzle which forms the bond while the hot plate's temperature ramps down. The nozzle leaves the chip when the substrate temperature falls down to a pre-determined level, which leaves the chip bonded to the substrate.

Now the package is ready to be soldered on to a PCB with solder pads matching the structure of the back M2. The figure 29 shows the finished package of monolithic flow.

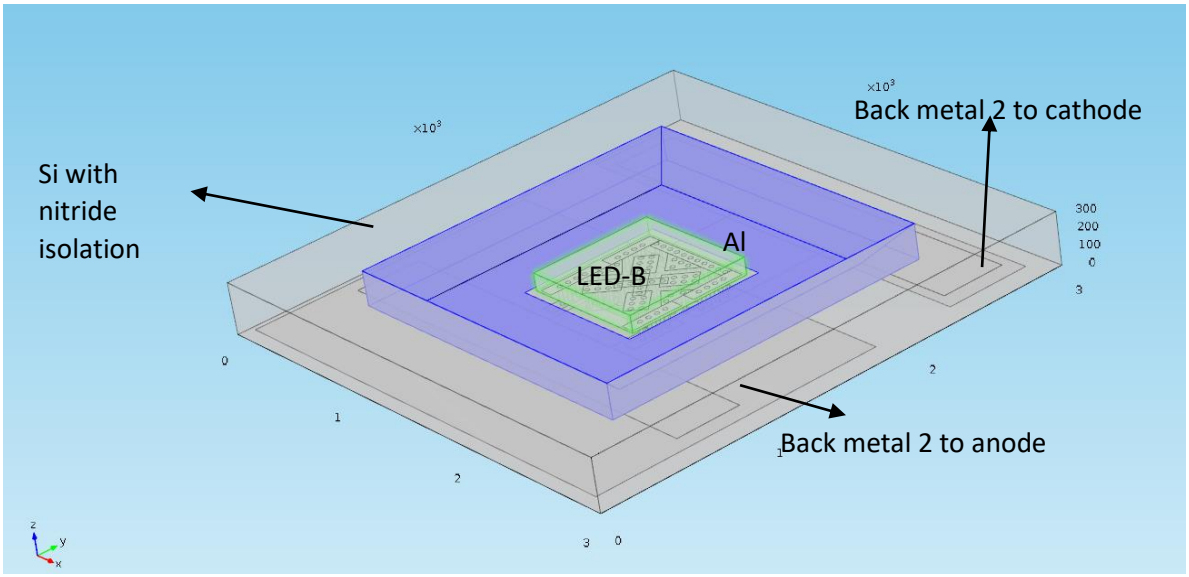


Figure 29: Packaged LED ready for soldering on PCB

4.3 Dual wafer packaging concept design for LED-A and LED-B

This flow requires processing on two wafers, the top and the bottom wafer. The top wafer is for fabricating reflector cups and needs just one litho step, whilst the bottom wafer is the substrate for the chips and it requires 3 litho steps for LED-A and 4 steps for LED-B out. The final concept design is shown in figure 30.

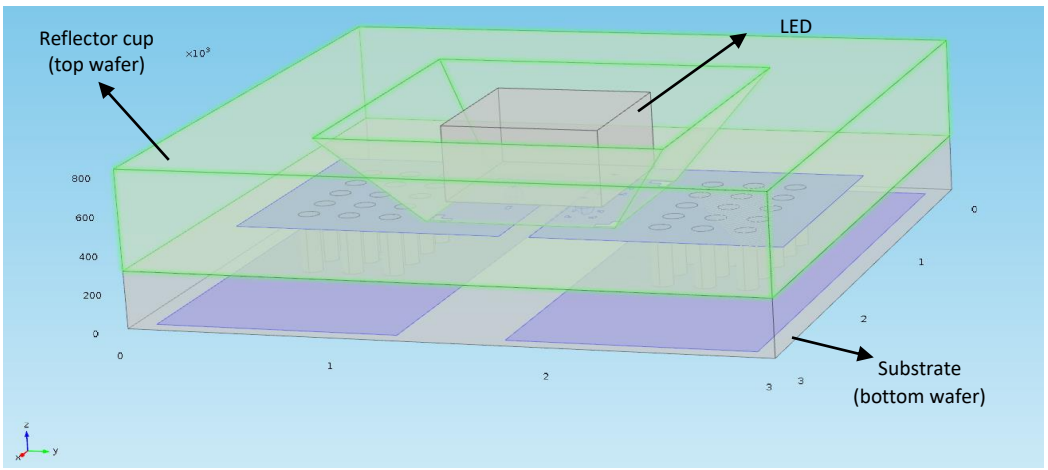


Figure 30: Dual wafer package

Merits of this process when compared to monolithic packaging are:

1. the incredible reduction in process time therefore cost of ownership and cost per die,
2. establishing a common packaging platform for different types FC-LEDs,

3. less materials involved on the package therefore less variables contributing to process variations,
4. easier to reverse/course-correct the process flow,
5. easier to identify and analyze the bottlenecks,
6. the prospects of automated production for HVM,
7. less chance of contamination of cleanroom equipment

4.3.1 The top wafer – reflector cup

The reflector cup is for both LED-A and LED-B and one of the chips is 400 µm thick, hence the reflector cup is designed with 525um thick wafers in order for it to be able to encapsulate both chips. The only lithography step is to perform KOH etching. After this the wafer is insulated with nitride and AlSi is deposited from the top. After dicing, the individual reflector cups are ready to be attached to the submounts with chips.

KOH etching and reflector sputtering

A 525 µm thick p-type wafer is sent to the 'Tempress systems' furnace for 200nm of LPCVD nitride deposition. Then with lithography we pattern the openings on resist and the nitride is etched in 1650 µm x 1650 µm squares with RIE etching by the machine 'Drytek triode 384T'. Then the resist is stripped and the wafer is cleaned with standard HNO_3 cleaning line. The wafer is then sent to KOH etching in the KOH bath with nitride as the mask and the etching is performed where the nitride is open until the wafer is etched through completely.

Then the wafer is sent through the HNO_3 cleaning line before 200 nm LPCVD nitride is deposited once again for the side wall insulation of the cavities. Then 'Trikon Sigma 204' sputtering machine is used to sputter AlSi (99% Al and 1%Si) as reflector material. Figure 31 shows the completed reflector cup.

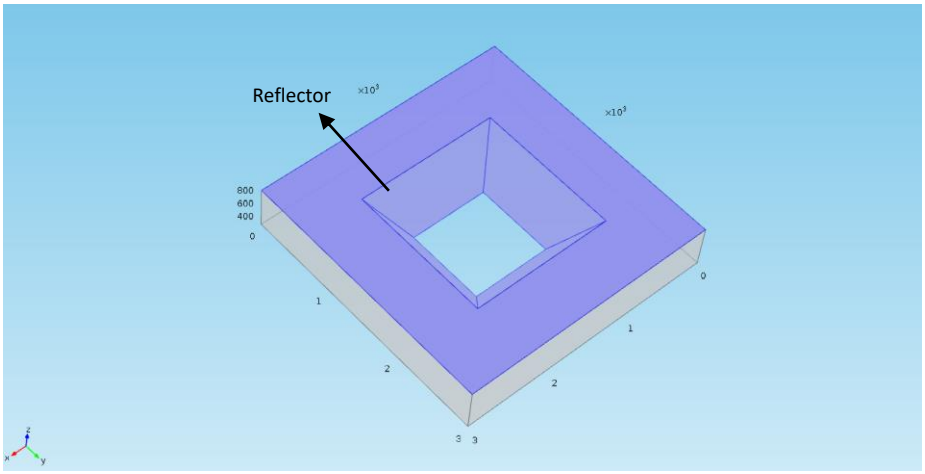


Figure 31: Reflector cup with sputtered aluminum

4.3.2 The submount design – bottom wafer

The submount's fabrication includes: vias, via filling, contact metal from vias to the chip on the front side, contact metal to the PCB on the back side.

4.3.2.1 Etching vias - DRIE

The dual wafer design allows the electrical path to be far from the chip rather than underneath it like in the monolithic design. This is achieved by the placement of the vias far away from the chip. This reduces the backside processing to just 1 step. When the puddles are placed far from each other the back side processing is reduced to even zero since there is contact already established from the metal paste puddles when the back side is used to solder to a PCB.

The anode and cathode vias are each a 3x5 matrix of 100 µm diameter vias. The etching is performed by 'rapier omega i2L' DRIE etcher used to etch the vias with. A 3 µm of TEOS oxide deposited by 'Novellous concept1' is used as mask for etching the vias for 550 loops. The oxide mask is pattered with lithography and opened with RIE etching by 'Drytek Triode 384T'. Since the via etching is done through the entire thickness of the wafer, the plasma can go through the wafer and hit the wafer holder of the DRIE machine. To prevent this, a 2 µm thick PECVD oxide is deposited on the other side of the wafer to protect the wafer holder of the DRIE machine.

Once the etching is finished, the polymers are long-stripped in 'Tepla Plasma 300' plasma etcher for 30 minutes and the wafer is sent to the standard HNO_3 cleaning line. Next, the oxide and nitride are removed with BHF and boiling 85% nitric acid respectively before sent to the standard HNO_3 cleaning line. The insulation for the walls and the wafer is provided by 200nm of LVPCVD nitride

deposition in 'Tempress systems' furnace. Figure 32 shows a 3 mm x 3 mm submount with vias etched and isolated with 200 nm of LPCVD nitride.

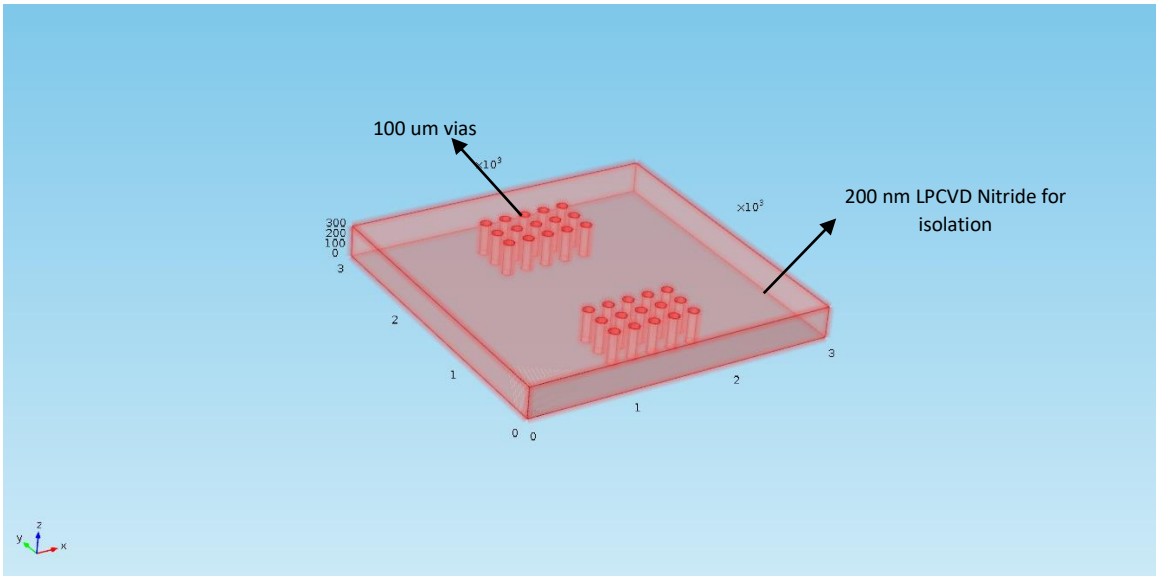


Figure 32: Vias etched and insulated with nitride

4.3.2.2 Via filling and sintering

The vias are filled with the metal nano paste by carefully placing puddles of paste on top of the vias and applying vacuum from the other side. Once the filling is finished, the wafer is sintered where the solvents of the paste are evaporated and the nano particles of the paste are fused together. This is done in a vacuum oven vacuum with nitrogen gas at 250^{o}C for 2 hours. The puddles are not wiped as this could be used for direct soldering on to PCB and thus eliminating another litho step for depositing metal on the backside.

4.3.2.3 Gold deposition for LED A

The gold is deposited in preparation for gold bumping for chip bonding. First, the wafer is spray coated with negative photoresist (NLOF 2070) and exposed in the pattern of required gold pattern. After developing with the developer (MF322) to open the resist, the wafer is ready for evaporation of gold. The same steps used in evaporation of gold in monolithic flow are also used here. The 3D schematic of the package with gold pattern on the 3 mm x 3mm substrate is shown in figure 33.

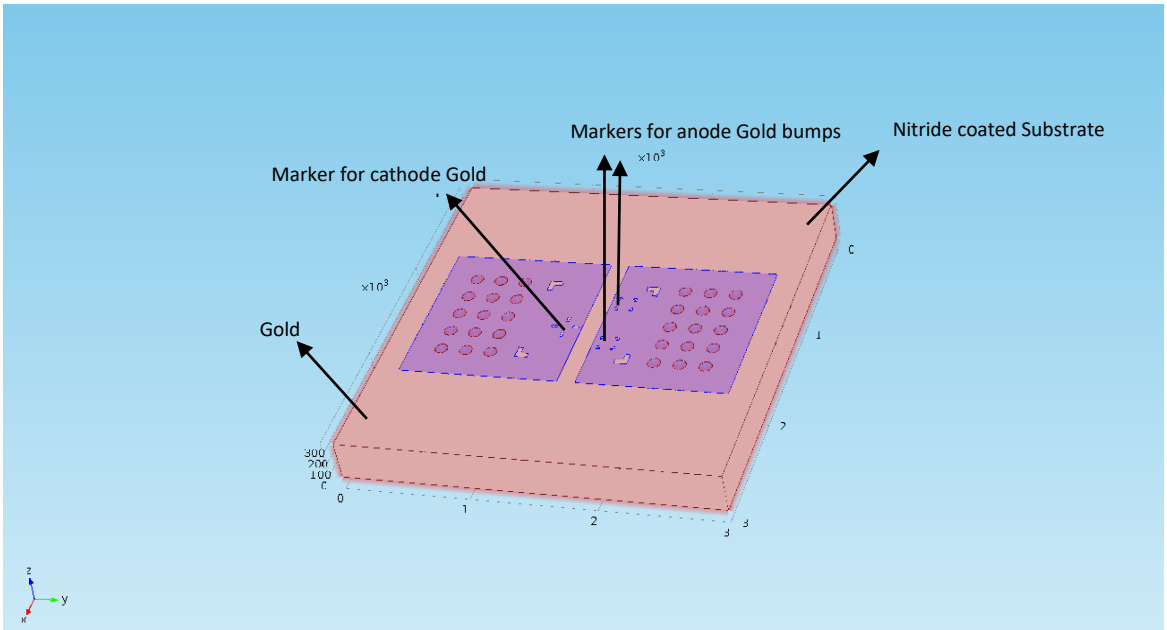


Figure 33: LED-A's gold pattern (last processing step for LED-A)

4.3.2.3 Solder deposition for LED-B

The same steps are followed for gold deposition for LED-B as well with the exception of the change in pattern of gold which is in the exposure part of lithography.

A solder material is required for bonding this particular type of LED. Gold-tin (80-20) eutectic solder is the choice for its advantages and it is deposited by sputtering. It is needed only on the chip bonding area which is at the center. However, since the sputtering is performed everywhere on the wafer and the unrequired deposition is just lifted-off in NMP, the same pattern used for gold can be used for Gold-Tin solder as well. Thereby eliminating the need for another litho step for patterning solder just at the chip bonding area. The schematic of the substrate with solder pattern for LED-B is shown in figure 34.

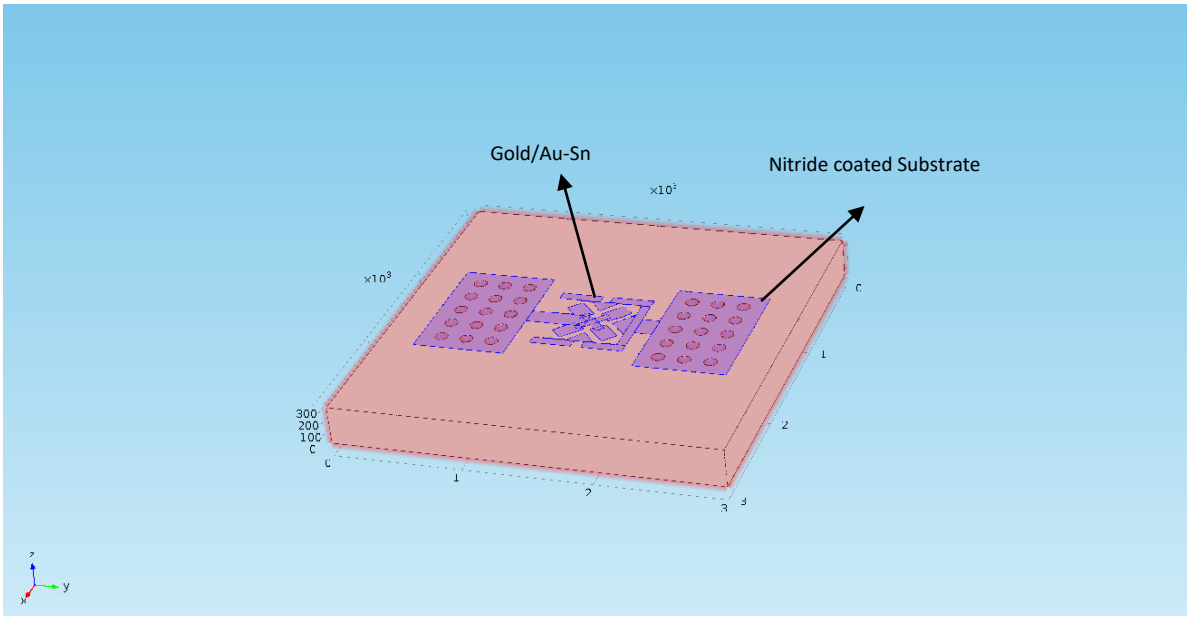


Figure 34: LED's Gold/Gold-Tin pattern

4.3.2.4 Back metal (optional)

The metal nano paste puddles on the back provide enough contact for soldering the package on PCB. Therefore another step for metal deposition is not needed. This ends the processing of the package, and the wafer can be diced and the chips can be bonded. The schematic of puddles after via filling is shown in the figure 35.

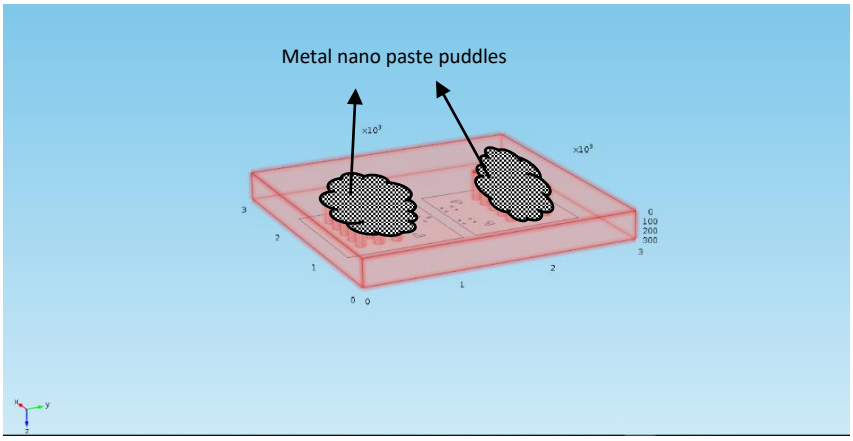


Figure 35: Puddles of paste eliminating the need for metal pattern

However, if the puddles are found not to be of almost the same thickness (height), the substrate will be unlevelled when facing upwards and the chip bonding could prove to be difficult in obtaining a levelled chip bonding. In this case, the puddles need to be wiped off after via filling and before

sintering, and another metal needs to be patterned on the back side with an extra litho step. The metal can be evaporated or sputtered. The back metal after patterning is shown in figure 36 .

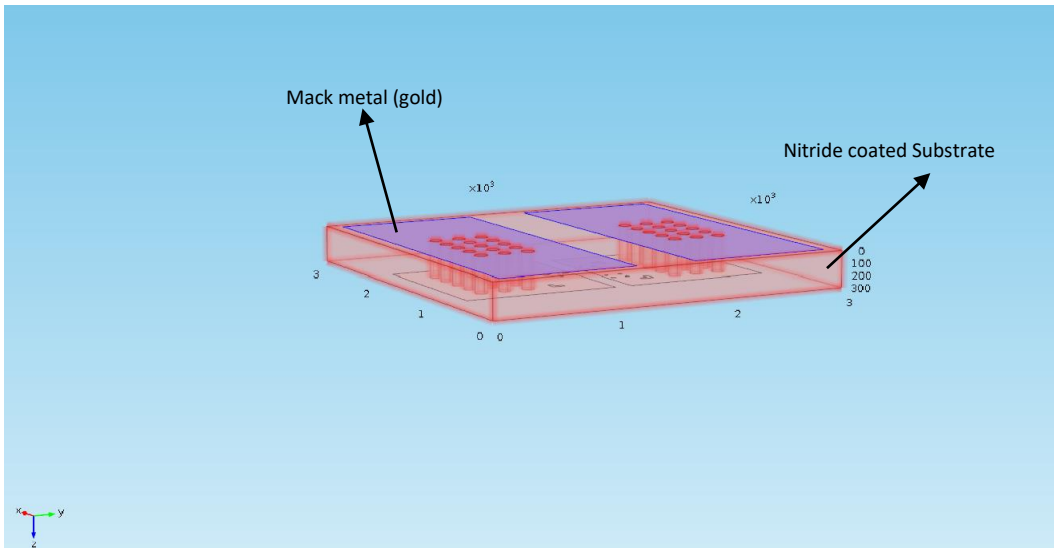


Figure 36: Back metal deposited with an extra litho step in case the puddles are a problem

4.3.2.5 Bonding LED-A to the substrate

LED-A is designed for bonding via stud-bumping. The bond pads on the chip are 100 µm in size (2 rectangular pads for anode and 1 spherical pad for cathode). The 3 bumps are placed at the markers and the chip is ultrasonically bonded with the submount using 'Finetech ultrasonic module' bonder. The schematic of the placement of the Au bumps is shown in the figure 37.

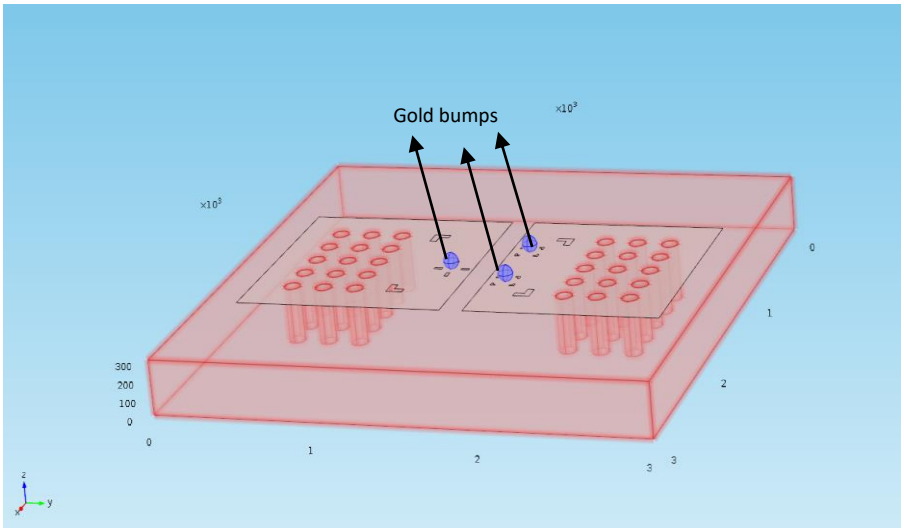


Figure 37: Gold bumps for bonding LED-A

The last step is to attach the reflector cup with glue as shown in figure 38.

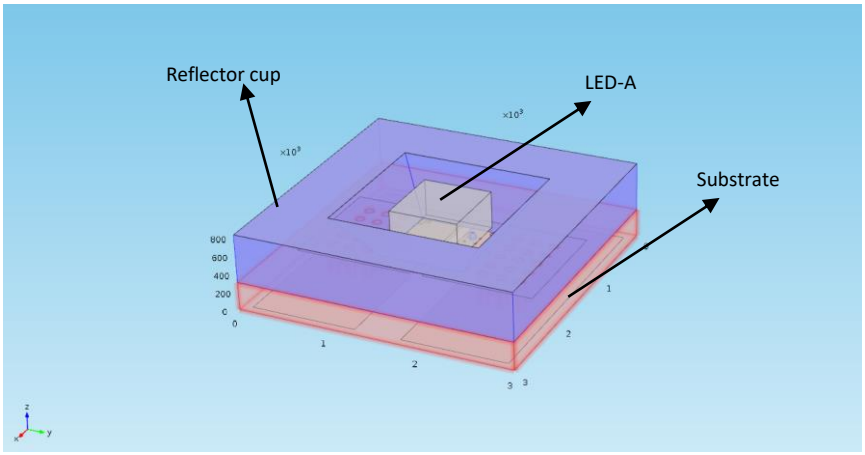


Figure 38: A complete LED-A package

4.3.2.6 Bonding LED-B

The bonding of LED-B is the same as the method in monolithic bonding. And the reflector cup is attached to finish the package.

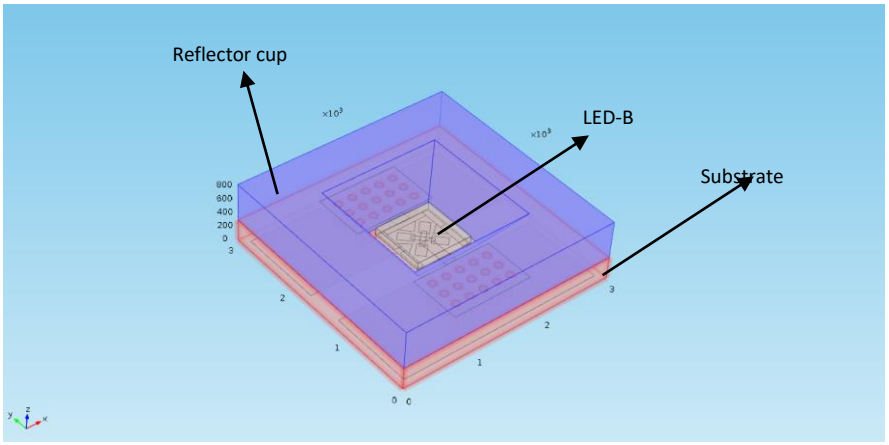


Figure 39: A finished package of LED-B

4.4 Summary

We have developed the concept design for the 3 mm x 3 mm packages and visualized the package using COMSOL multiphysics as it goes through changes in microfabrication to become a finished product. In the next chapter we implement the design at EKL in TU Delft and bond the chips at Philips research at High tech campus, Eindhoven.

The overview of the processing steps are provided in the table 2.

Table 2: Summary of the monolithoc and dual wafer flows:

Monolithic flow	**Dual wafer flow**
Etch vias and isolate with LPVD nitride – back	Reflector cup - Etch cavities and deposit AlSi
Etch reflector cavities - front	Submount – Etch vias and isolate with nitride
Deposit and pattern the AlSi - front	Submount – Fill the vias and sinter, back
Fill the vias and sinter	Submount – Deposit and pattern metal, front
Deposit and pattern back Metal 1 (M1) - back	Dice and chip bonding
Isolation oxide and pattern CO on M1 - back	Attach the reflector cup and the submount
Back metal M2 on oxide – back	
Solder deposition and lift off - front	
Dice and chip bonding	

5 PACKAGE FABRICATION

In this chapter, the actual fabrication process is described in detail with visible aids of SEM, microscopic, and full-scale images of wafer as it goes through each step of the fabrication, and images of the equipment used for the processes. First the mask design and the progress of each flow is given.

The fabrication was performed in 'EKL laboratory in Delft University of Technology'. The fabrication flows were adjusted according to the regulations and the equipment local to EKL. The process recipes for most equipment have been standardized and require just variation in few variables like time, number loops, exposure energy, power, cooling limit, endpoint detection, etc.

When the fabrication is complete, the wafer was diced into 3 mm x 3mm packages and taken to Philips lighting research, Eindhoven for Au bumping, attaching the chips and reflector cups. Characterization of the finished products was also done at Philips.

5.1 Monolithic wafer processing for LED-B

5.1.1 The MASK design for 3D processing

The standard 3x3 (9 images) image format of EKL laboratory is used to design the mask. The image structures are designed in 'L-Edit 11.0' software. The structure sizes needed on the wafer are the sizes used in the software as well. Each image corresponding to a lithography step is designed in a 6 mm x6 mm boundary (die size) format and each image is created with a different design layer. All 9 images are added to a single cell in a 3x3 matrix format enclosed in a 20 mm x 20 mm boundary with 1 mm spacing between every image. Once all the layers are generated the design is converted to a monochrome file by assigning all the layers a single graphic database system (GDS) number. The design is exported into a GDSII file and sent for printing on a mask (reticle).

The reticle is a 6" x 6" x 0.120" quartz glass with chrome film printed in the patterns 5 times the size of the structures on the GDS file. The chrome film is opaque to the UV light and the features in the GDSII file are the patterns with no chrome. So the patterns (black) in the GDSII file are the patterns where the reticle is transparent.

Since each die is 6 mm x 6 mm and the package is 3 mm x 3 mm in size, each die can incorporate 4 packages in a 2x2 matrix. Thus, every image on the mask has 4 similar structures each corresponding

to a single package as can be seen in the 9 image mask showed in figure 40. So, after the wafer is processed, every die can be diced into 4 packages.

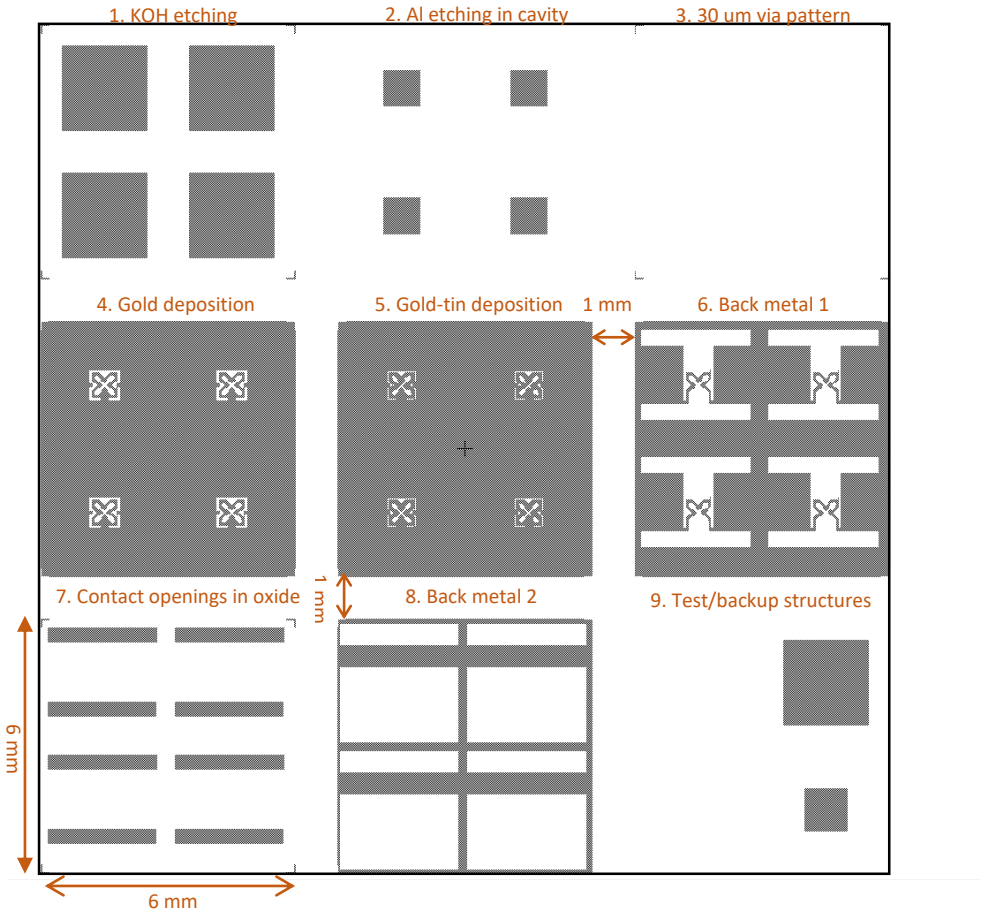


Figure 40: The GDSII file of monolithic flow (where, each image = 4 packages & black = tramsparency on mask)

5.1.2 Wafers and zero layers

The wafers chosen to fabricate the packages are '4" diameter & 300 µm thick' which are supplied by 'OKMETIC' to the EKL. This flow requires processing on both sides hence DSP wafers are chosen. These wafers are bare silicon and before the processing starts they are sent through the standard HNO3 cleaning.

When multiple lithography steps are performed on a wafer it is important to have an accurate alignment of wafer and mask every single time an exposure is performed as this is the defining step for matching the relative position of structures from different litho steps. In order to obtain this, before the fabrication of a device is begun, the 'alignment markers' are etched on the wafer. The local terminology for this step is 'Zero Layer'. The standard process is to coat 1.4 µm of resist in 'EVG 120 coater-developer' with a standard recipe. After coating, the wafer is aligned based on the primary flat

and exposed using an 'ASML PAS 5500/80 wafer stepper' using a default mask always loaded in the machine. The alignment markers re placed at 14 different points close to the edges of the wafer. Later the wafer is taken for development in the 'EVG 120 coater-developer' where the exposed parts are developed to expose bare silicon thus ending the first litho step.

Next, the exposed silicon is etched 120 nm deep in 'Trikon Omega 201' plasma etcher with a standard recipe. After etching the resist is stripped in 'Tepla Plasma 300' plasma etcher for 2 minutes with endpoint detection. Then this cycle is finished with standard non-metal HNO_3 cleaning.

The same process is repeated for alignment markers on other side, but this time the markers are placed by aligning the wafer using the markers already present on the other side. After the repeated cycle, the wafer is ready for fabrication.

5.1.3 Etching Vias – DRIE

According to the concept design, the cavities are etched before the vias are etched. However, the cavities make the wafer mechanically weaker and are more susceptible for breakage in via etching flow. Hence the die pitch is reduced to 37 dies per wafer with a die present alternatively in every direction as shown in figure 41 and the vias are etched first then and taken for KOH etching.

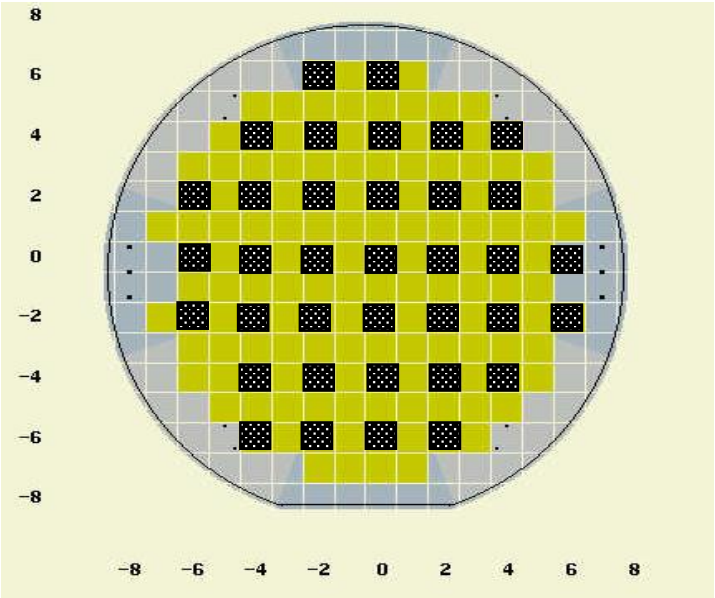


Figure 41: Alternative dies chosen for exposure to reduce the mechanical weakness

For etching the vias, 1.5 µm of PECVD TEOS oxide is deposited 'on side B' as the mask at 350^{o}C with 'Novellous Concept 1' machine. This oxide is patterned with ø30 µm via pattern on the 'image 3' of

mask using lithography. Then the oxide is etched with 'Drytek Triode 384T' at (500 nm/min). To account for non-uniformity of etching over wafer area, over-etch is always used. In this case a total time of 3.5 minutes is used (0.5 minute of over etch). The thickness of oxide is checked using 'LEITZ MP-SP' film thickness measurement machine to make sure the oxide is open to bare silicon.

Once the bare silicon is exposed in the via pattern, the silicon is etched with 'Rapier Omega i2L DRIE etcher' for 225 cycles (100 µm deep). Over-etch is used here as well. The via pattern is printed on the wafer as shown in figure 42-a. One of the wafers is sliced along the 100 plane to check the via depth as shown in figure 42-b and confirm that etch cycles are sufficient. Then the resist and polymers are long stripped for 30 minutes in Tepla and the wafer is sent through the standard non-metal HNO_3 cleaning. Then the oxide is removed with BHF (1:7). Now the wafer can go for the next step in the flow: KOH etching. The top view and the cross section of the vias are shown in the figures.

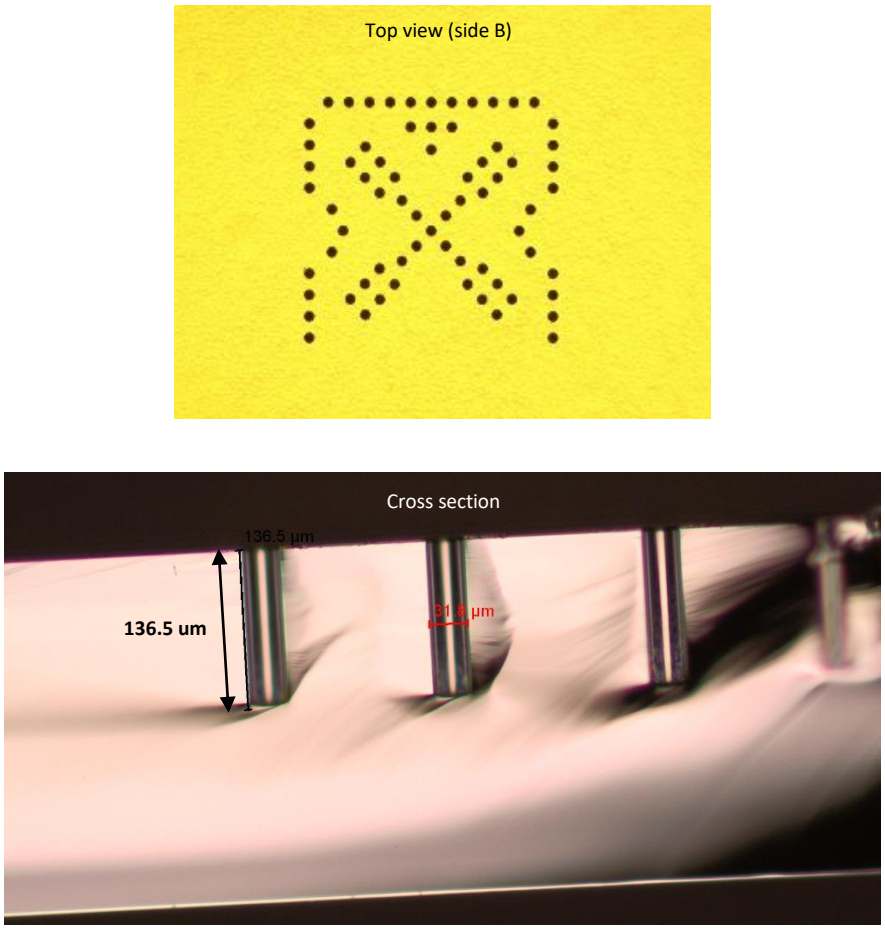


Figure 42: Package after etching vias a) The ø30 µm pattern b) an example of cross section of vias at one of the dies

5.1.4: Cavities for reflector cup

The wafer is first sent through the standard non-metal HNO_3 cleaning line before sent to LPCVD tube of 'Tempress systems' furnace where it is coated with 200 nm LPCVD nitride (for 28.5 min) which is a

mask for silicon during KOH etching. Since this is LPCVD nitride, it also deposits on the walls of the vias and this obstructs the KOH solution from flowing into the vias once the vias are reached while etching from the other side. This wall protection is essential to maintain the integrity of vias' physical separation. The nitride walls are shown in the SEM images in figure 43-b,c.

The nitride on the front side is patterned with image 1 on reticle in litho and etched with Drytek (300 nm/min) with 30 sec over etch. The resist is stripped and the wafer is sent through the standard non-metal HNO_3 cleaning line before going to the KOH bath.

The 33% KOH bath is maintained at 85°C and wafer is left in the batch for 125 min (200 µm deep, etch rate of 1.6 µm/min). The cavity depth is measured with 'Dektak 8' profiler to make sure the 200 µm depth is reached and the cavity looks like figure 43-a. If it didn't, the wafer can go back to the batch until it does. Once this is achieved the nitride has to be wiped off completely to be able to fill the vias.

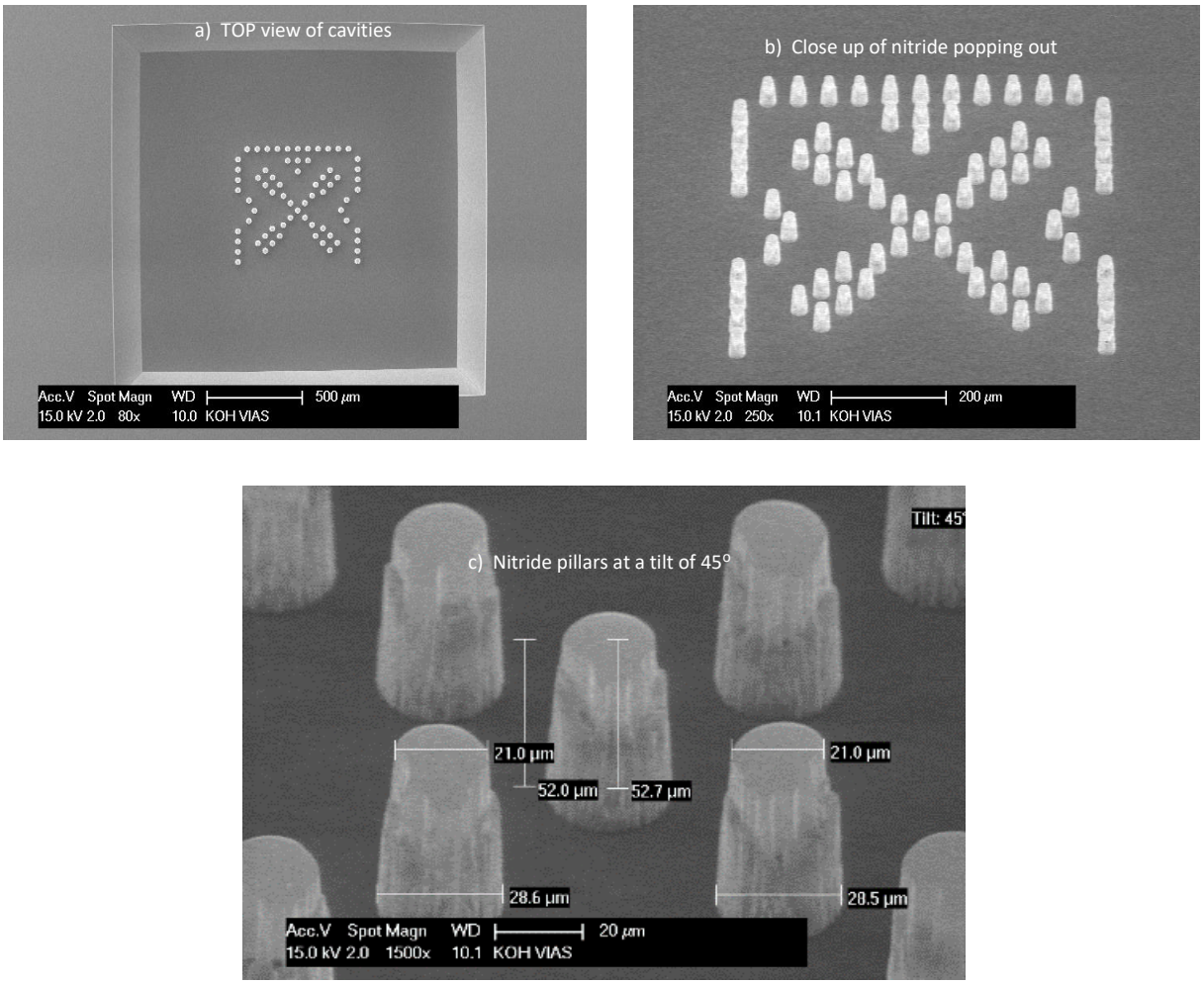


Figure 43: SEM images of a) the cavities after 200 µm of KOH etching, b) Close up, and c) Nitride pillars

From figures 43-b and 49-c, it must be noted that just 200 nm of nitride was able to mechanically stand with no cracks, proving how reliable LPCVD nitride thin film is even in 30 µm diameter and 100 µm depth vias.

5.1.5 Isolation of vias – LPCVD nitride

The nitride is cleaned completely in boiling phosphoric acid (157^{o}C @ 85% conc.) since the pillars block the path to fill the vias. The nitride is deposited again to have the isolation layer of vias the wafer is first sent through the standard non-metal HNO_3 cleaning line before going to LPCVD tube of 'Tempress systems' furnace where it is coated with 200 nm LPCVD nitride. The wafer after nitride is shown .

5.1.6 Reflector pattern in cavities – 3D processing of Aluminum (front side – Side A)

The reflector material is deposited on the front side with sputtering. 300 nm of AlSi (99%Al and 1% Si) is sputtered at 350^{o}C in the 'Trikon Sigma 204' sputtering machine with AlSi target.

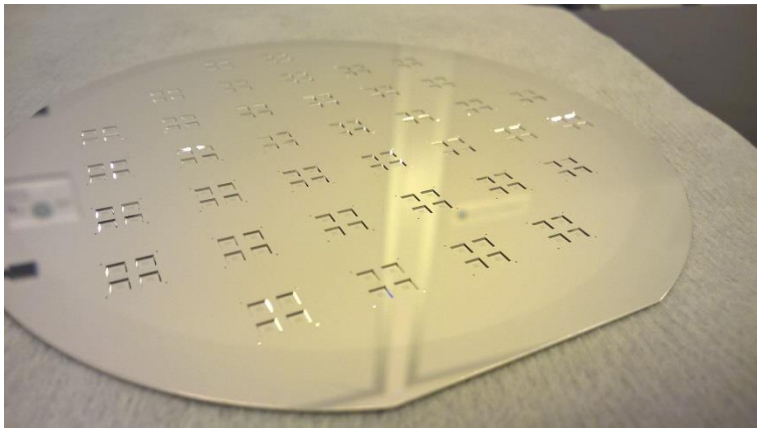


Figure 44: Wafer after sputtering reflector material

The reflector material is patterned with wet etching. Spray coating is used to deposit resist uniformly at the bottom of the cavities. The 'EVG 101 spraycoater' machine, shown in figure 45, sprays resist in layers at a slow rate while the wafer spins and the spray nozzle moves hovering over the wafer at varying speeds depending on the position of the wafer. The thickness of the resist depend on the spin speed, spray rate (micro liter per second – ul/s), pressure etc.

To obtain 6 µm thick resist, 8 layers of AZ-9260 resist is spray coated on the wafers 'twice' at 1000 mbar pressure and 2 ul/second spray rate with baking (@ 115^{o}C) steps after each spray(for 3 min after 1st and 5 min after 2nd) – *Recipe provided by Zahra* [24].

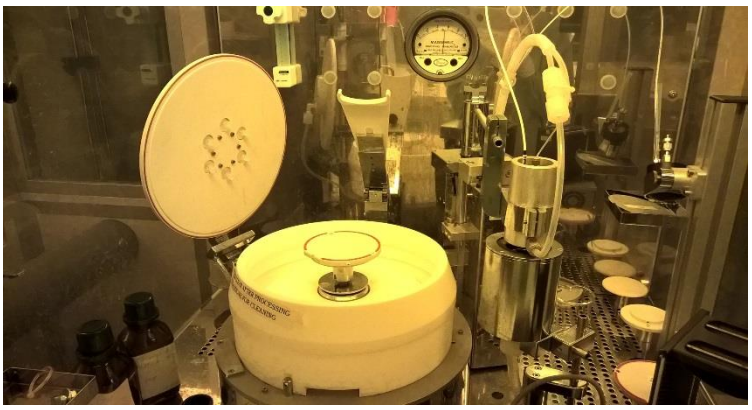


Figure 45: EVG 101 Spraycoater module for 3D processing

After coating and waiting for 30 minutes, the wafer is attached to a carrier wafer and exposed with an energy of 800mJ/cm^2 at a focus depth of 199 µm using the image 2 of the reticle. Then after waiting for 30 minutes the wafer is developed in AZ-400K (diluted: 1 part AZ-400K and 2 parts DI water) for 2 minutes.

After development, the aluminum is etched at the bottom of the cavity with PES solution at 35^{o}C (3 minutes incl. over etch) and the poly silicon is etched for 45 seconds using poly etch bath. Then the resist is stripped in acetone for 1 minute and rinsed in DI water before it is dried. The microscope images of a die and a chip are shown in figures 46-a and 46-b.

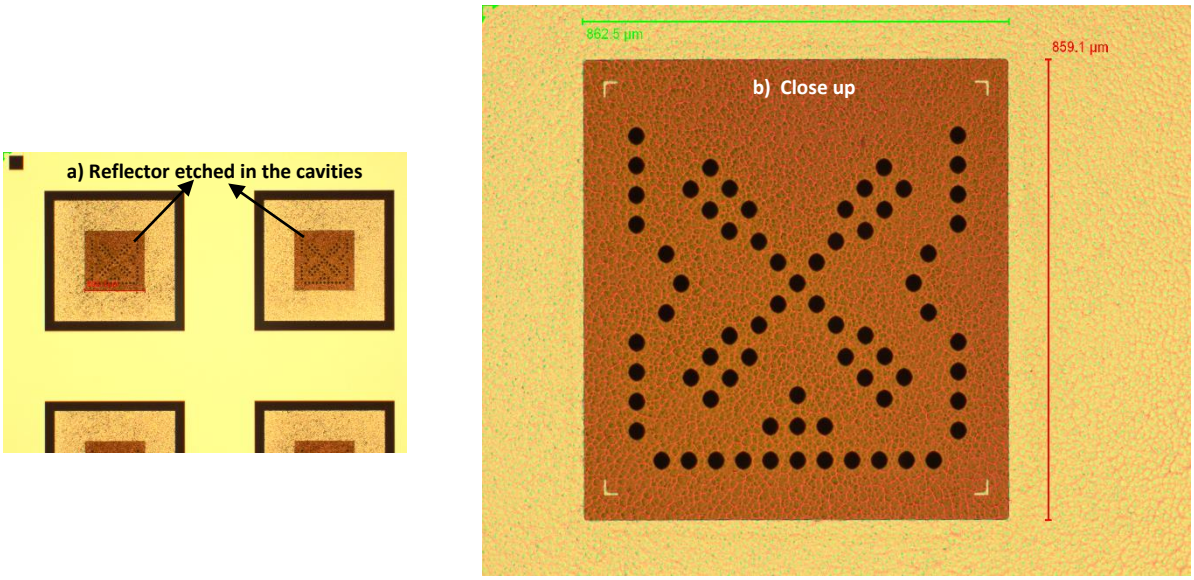


Figure 46: Microscope images after reflector is etched in cavities a) of a die b) close up to a single chip

Finally, the wafer is sent to the through the standard 'green-metal' HNO_3 cleaning line before the vias are filled with copper MNP.

5.1.7 Filling the vias – Copper MNP with vacuum

Copper paste (CPN – 1000P) from 'Intrinsiq materials' is obtained and filled in a syringe. This paste is manually and carefully placed on each via set on the back side (side B) as puddles as shown in figure 47. This paste can be wiped away with IPA as mentioned in the technical data sheet from the supplier. However this doesn't ensure a complete residue-free surface. To reduce the residues, a layer of photoresist is spray coated before the pate is deposited so after the soft bake the residues can float away along with the resist when dipped in acetone.

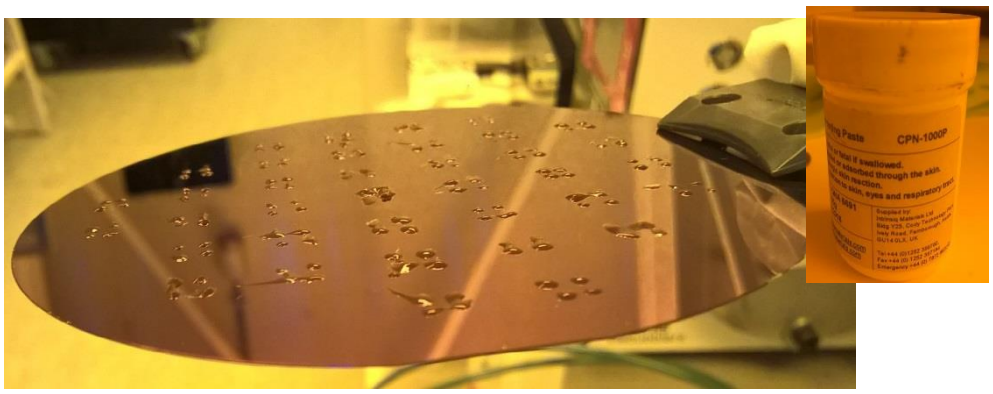


Figure 47: Paste placed on each set of vias with a syringe (inset: bottle containing the paste)

The wafer is placed on a vacuum chuck as shown in figure 48, and slowly the vacuum valve is turned. It should be turned just enough to not break the wafer. Extreme care is required in turning the valve for it could break the wafers very easily. This mainly due to the cavities that have weakened the wafer.

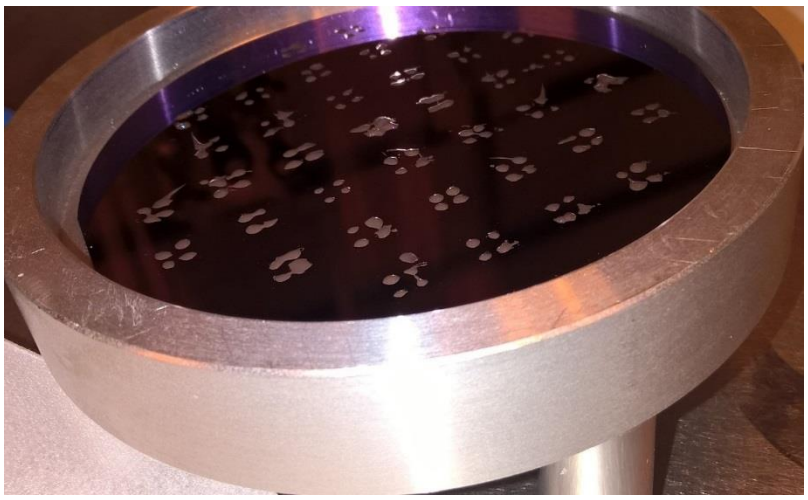


Figure 48: Wafer on the chuck while vacuum is applied from

The wafer is consistently checked for signs of paste visible on the other side (Side A). Once the paste is seen to be coming out the wafer on the other side the wafer, it is set on the cleanroom grade tissue papers and the puddles are wiped with IPA and a hard rubber. The cleanliness of the surface depends on the manual parameters and it is not consistent throughout the wafer.

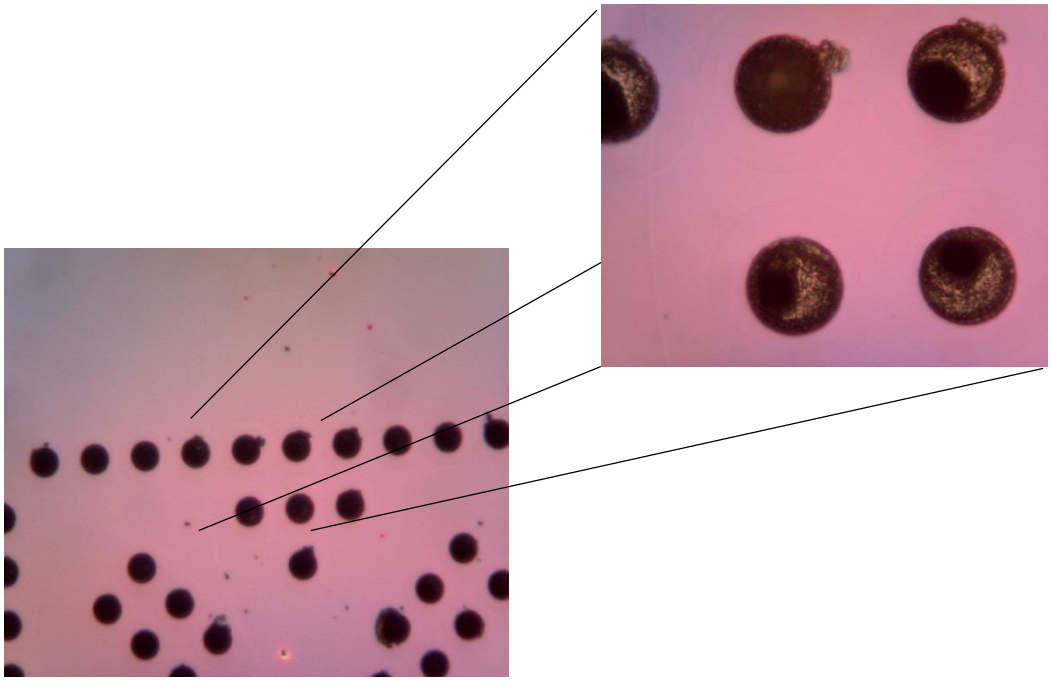


Figure 49: Image after an acceptable wiping and soft baking on back side (Side B)

Then it is taken for soft baking in vacuum at 75^{o}C in the 'Hereaus vacuum oven' for an hour in the presence of nitrogen gas (200 mbar). Then the wafer is dipped in acetone for 2 minutes and rinsed with DI water.

Then the wafer is sent back to the oven for a hard bake in vacuum at 250^{o}C for 2 hours in the presence of nitrogen gas (200 mbar). Then the wafer is let to cool down in vacuum until the temperature drops to approx. 70^{o}C. The wafer is inspected for residues as shown in *figure 48* above. The nano copper particles are inspected for their contact to the surface with SEM imaging as shown in *figure 50.a and 50.b* . The gap to the surface is found to be in the order of few micro meters and since this surface will be sputtered with gold-tin solder, the electrical contact will be established.

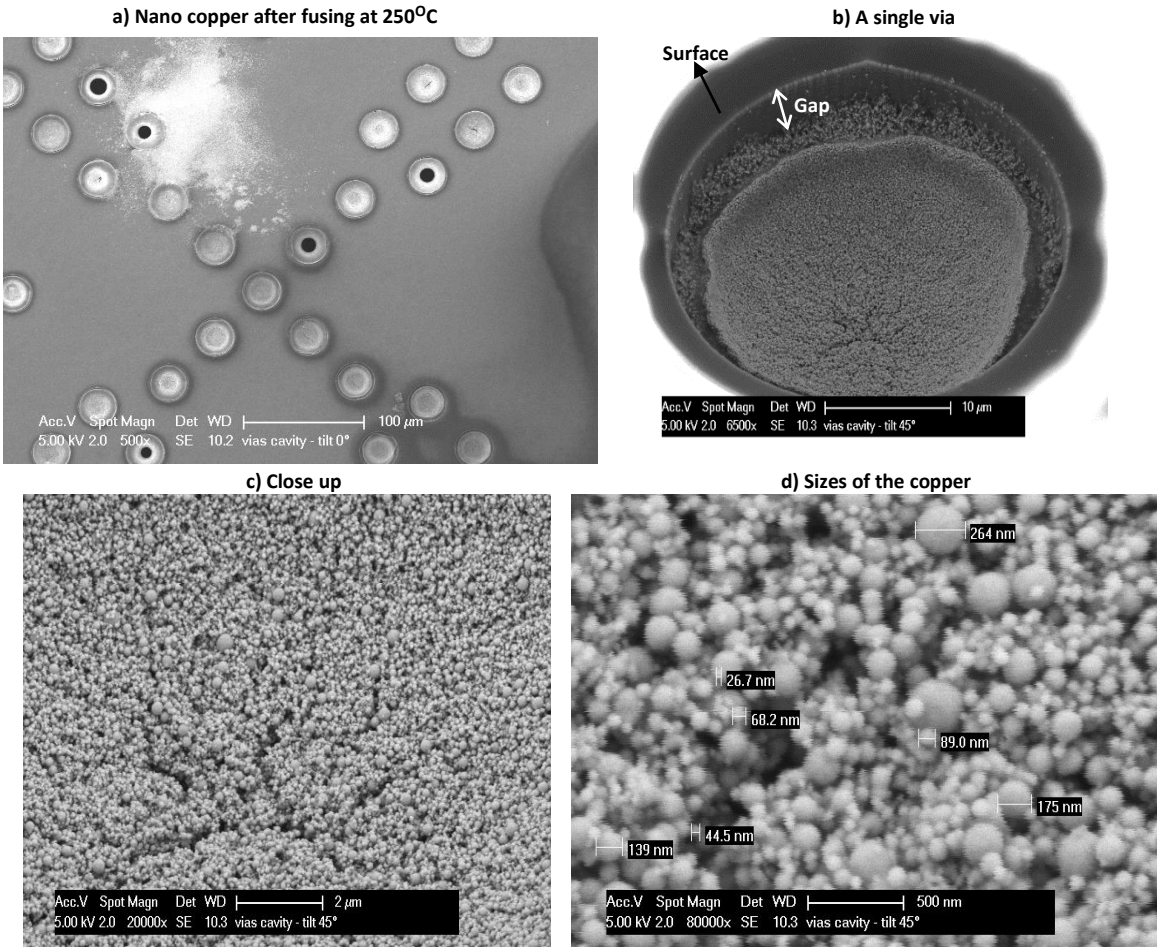


Figure 50: SEM images of the via filling in cavity: a) vias filled, b) Single via, c) close up, d) size of nano- copper

The *figures 50.c and 50.d* above also reveal that the cracks are introduced at the surface of the vias and the size of fused copper is in the range of 25 nm - 265 nm.

5.1.8 Anode and cathode separation with back metal 1 (Cu sputtering) – side B

300 nm of copper is sputtered at 25°C on the back side of the wafer in the 'Trikon Sigma 204' sputtering machine. Carrier wafers are used to prevent contamination to the machine. The back side is spray coated with photoresist and it is patterned with image 6 of the reticle in the stepper (contaminated carrier wafers are used). After developing in AZ 400K, the wafer is coated with resist on the front side, baked with proximity heating, and then taken for etching in copper etchant.

After 9 minutes, the copper unmasked by the photoresist is etched away. This disconnects the copper connecting anode via group and the copper connecting cathode via group as shown in 51. The resist is cleaned with acetone and the wafer can proceed to next step: the insulation layer (before M2 is deposited).

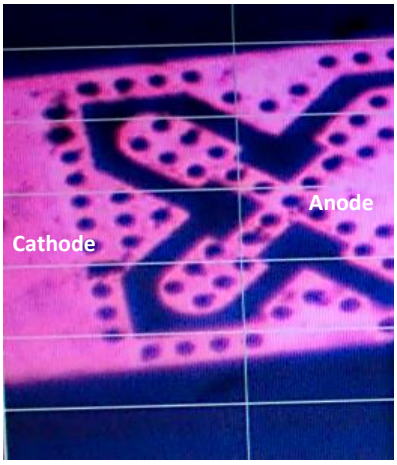


Figure 51: Close up of M1 on the wafer (inset: the whole design)

5.1.9 Insulation layer and contact openings to back metal 1 (PECVD TEOS oxide) – Side B

A 500nm of TEOS oxide is used as insulation layer and contact openings are made for M2 to make contact with M1. As per contamination regulations, a special metal carrier is used for transporting the wafer inside. The deposition is successful for just one wafer due to machine, more on the process bottle neck is explained in appendix 8.4 BOTLENECK - Issue of repeatability. The process is continued with the wafer with the successful deposition of oxide. It is patterned with spray coating, exposure, and development. Then it is taken to BHF (1:7) bath. The wafer is taken out after 5 minutes (incl. over etch). The resist is removed with acetone and the wafer is rinsed in DI water. The depth is measured first with Dektak profiler to confirm all the oxide is etched away. The profiler pointer starts scanning on top of oxide and moves towards the contact opening where the oxide is etched away thereby exposing M1. The step showed 500 nm of step after reaching the edge of contact opening as shown in figure 52.

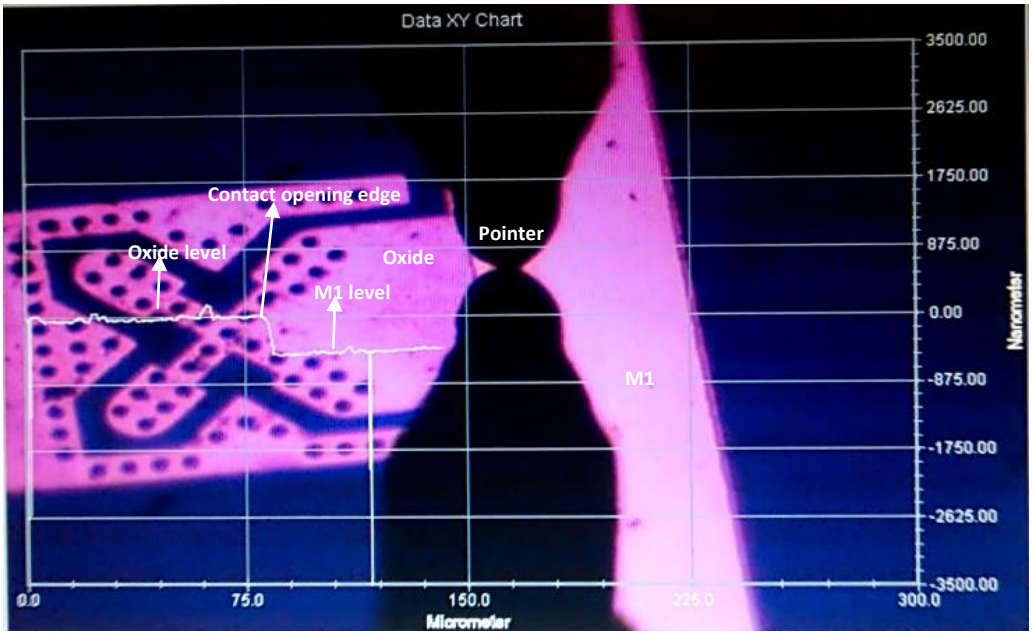


Figure 52: Contact openings in oxide (Note: The graph is related to the pointer's physical location, not the image behind the graph)

5.1.10 Back metal 2 (Gold evaporation - liftoff) – Side B

The final process step on the back side is to deposit pattern metal 2 with a liftoff process where the resist is patterned first, then the metal is deposited, and the resist lifted off which also takes away the metal deposited on top of it. The NLOF 2070 negative resist is spray coated with the same recipe as a spray coated positive resist except the baking temperature is 100^{o}C. The exposure energy is 100 mJ/cm^2 and image 8 on the reticle is used. After developing a crosslink bake is performed which is at 115^{o}C for 2 minutes. The wafer is developed for 4 minutes and taken for gold evaporation. 20nm of chromium is deposited as an adhesion layer then 300nm of gold is evaporated on to the wafer using 'Balzers TPG 300 Cr/Au evaporator'. Finally, the resist is lifted off, as shown in figure 53-b, in a beaker filled with NMP (70^{o}C) using a 'Branson 2200' ultrasonic bath as shown in figure 53-a.

a) Ultrasonic bath

b) Gold while lifting off in ultrasonic batch

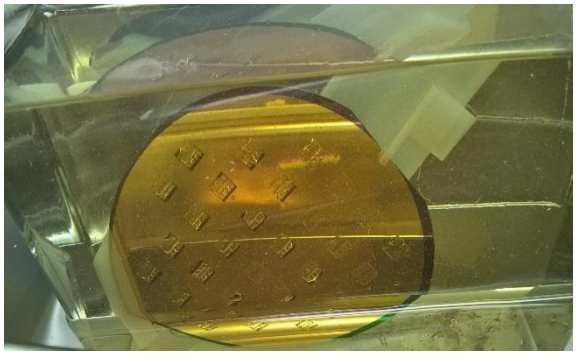


Figure 53: Metal 2- Lift off of gold a) the ultrasonic bath, b) gold while lifting off in ultrasonic batch

5.1.11 Solder deposition

The reflector step was sacrificed as the last wafer the wafer broke into 2 pieces of a large one (left) and a small one (right) while drying the wafer in a spin dryer. The process is saved by attaching the two pieces together on a dummy wafer and the correct exposure is achieved by correcting for the individual alignment markers on the left side and right side. The left part is considered the important due to its larger size hence larger number of dies. The reticle is aligned with the left the part of the wafer and exposed. The right part was shifted and the tilt is accounted for in the job description by relatively shifting the die positions. The patterns were accurate, as shown in figure 54, for left part and for most of right dies. The discoloring is explained in appendix 8.6 Process observation: Aluminum residues from BHF etching of oxide.

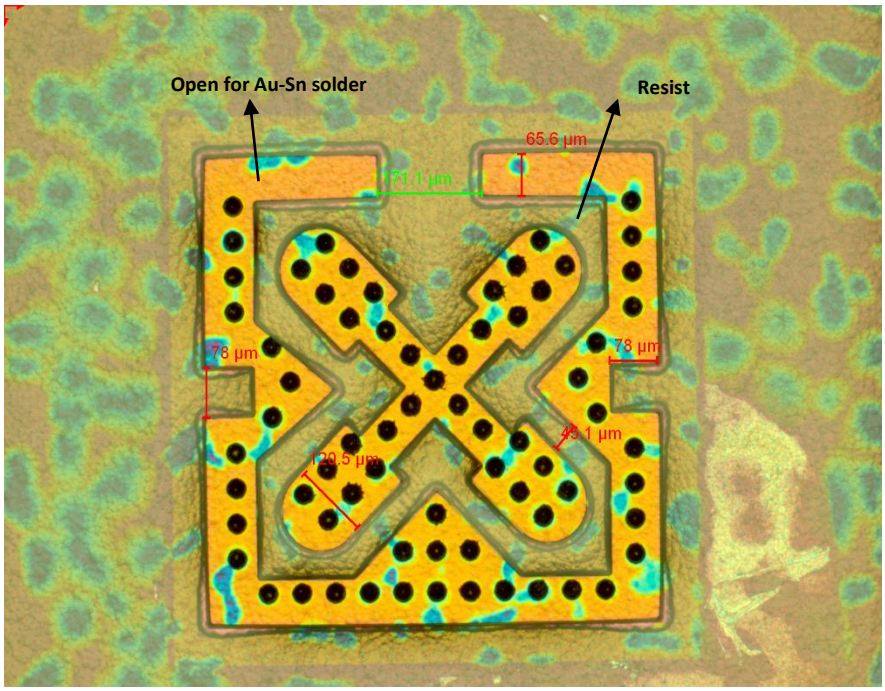


Figure 54: Correct patterning on the broken wafer

5.2 Dual wafer flow

5.2.1 Mask design

The mask is designed for 2 different packages built on a common plat form. This design involves two (100) type wafers: top n-type wafer and bottom p-type wafer. The top wafer (525 µm thick) is for a reflector cup designed for both LEDs. Whereas the bottom wafer (300 µm thick DSP) is the substrate

for bonding the chip. The via pattern and isolation is the same for both LEDs. LED-A has one extra step: gold deposition. Whereas LED-B has two extra steps: Aluminum and gold/gold-tin. The back metal is not needed unless the paste is required to be wiped clean on the back. The figure of GDSII image is shown in figure 55 as it was sent for print on the reticle.

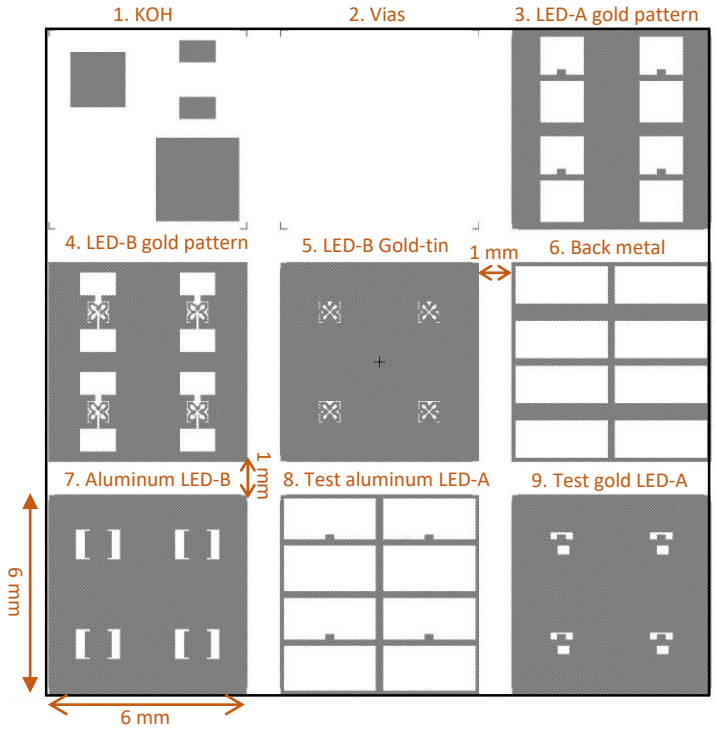


Figure 55: GDSII image of dual wafer package flow

5.2.2 Reflector cup – top wafer

5.2.2.1 Reflector cup etching - with LPCVD nitride mask

Since there is no other litho step there's no need for alignment markers. The wafer is sent through the standard non-metal HNO_3 cleaning line and coated with 200 nm of LPCVD nitride. Then the nitride is patterned with lithography using 'image 1' on the reticle and dry etching. The resist is stripped and the wafer is sent through the standard non-metal HNO_3 cleaning line.

The wafer is etched (@ 1.6 µm/min) in the KOH bath for 330 minutes once the holes are visible, the wafer is sent through the standard non-metal HNO_3 cleaning line and the nitride is removed with boiling phosphoric acid. Finally the wafer is sent through the standard non-metal HNO_3 cleaning line before depositing 200 nm of isolation LPCVD nitride. The figure 56 shows wafer after etching.

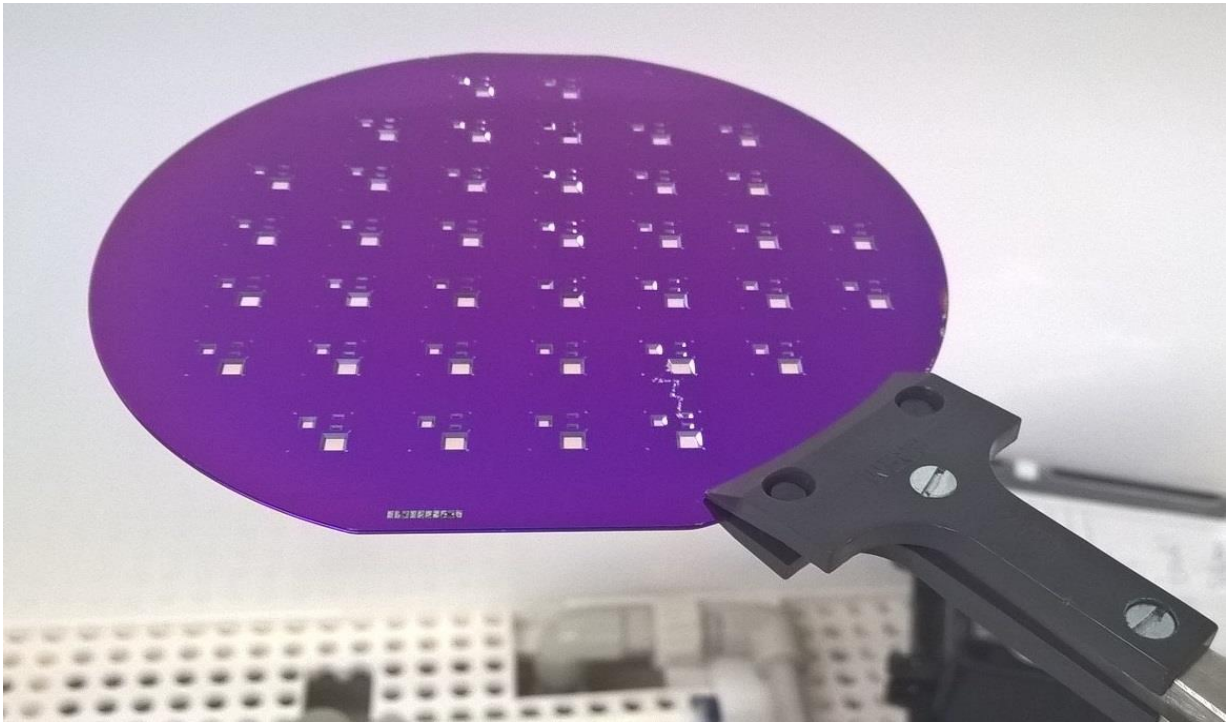


Figure 56: Top wafer after etching cavities with KOH

5.2.2.2 Reflector material deposition (AlSi sputtering) and dicing

Once the wafer is covered with nitride it is sputtered with 300 nm of AlSi @ 350^{o}C in 'Trikon Sigma 201' sputtering machine. The wafer is ready to be diced. The dicing blade may leave rough stains from the particles flying so the wafers are often coated with resist and then taken for dicing. Here, a die on the edge of the wafer as reference and the wafer is diced in x and y directions with 3 mm pitch. This dices the wafer into 3 mm x 3 mm packages. Once the dicing is finished the dies are cleaned with acetone. The figure 57-a shows the wafer as it is undergoing dicing process. Figure 57-b shows the diced wafer that are ready to go into acetone to wash away the resist and be ready for gluing onto substrates.

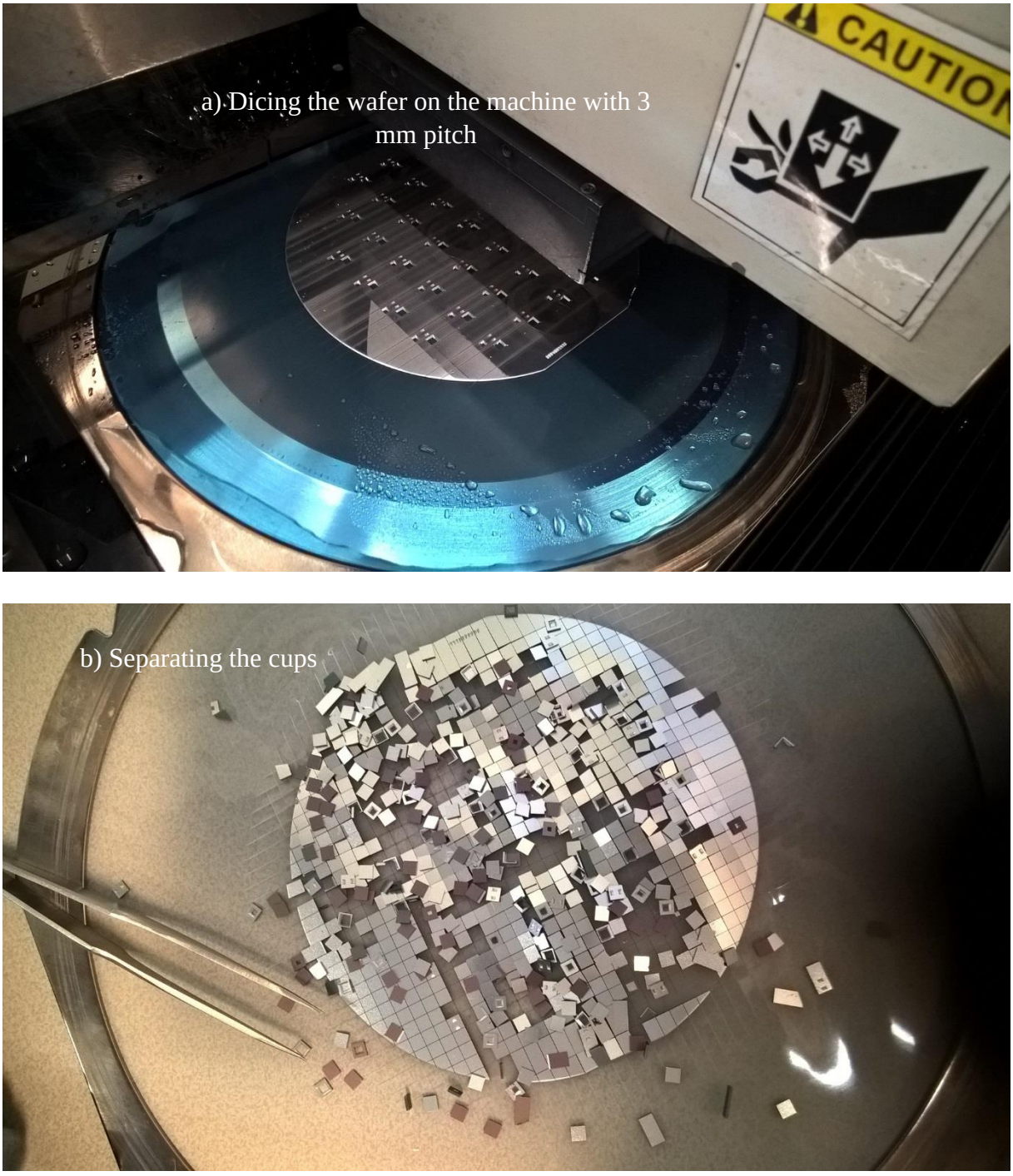


Figure 57: a) Dicing the wafer on the machine with 3 mm pitch, b) Separating the cups

5.2.3 Substrate – bottom wafer

5.2.3.1 Etching vias - LED-A and LED-B

The 300 µm DSP wafer is sent through the standard non-metal HNO_3 cleaning line before going to the PECVD TEOS deposition. Both sides of the wafer are coated with oxide (3 µm on one side and 1.5 µm on the other). The 3 µm oxide is used as the mask to etch the vias. The Image 2 is used to pattern the oxide with lithography and dry RIE etching. Then the vias are etched with dry DRIE etching for 550 cycles. The figure 58 shows the microscopic image of a 6 mm x 6 mm die with etched TSVs.

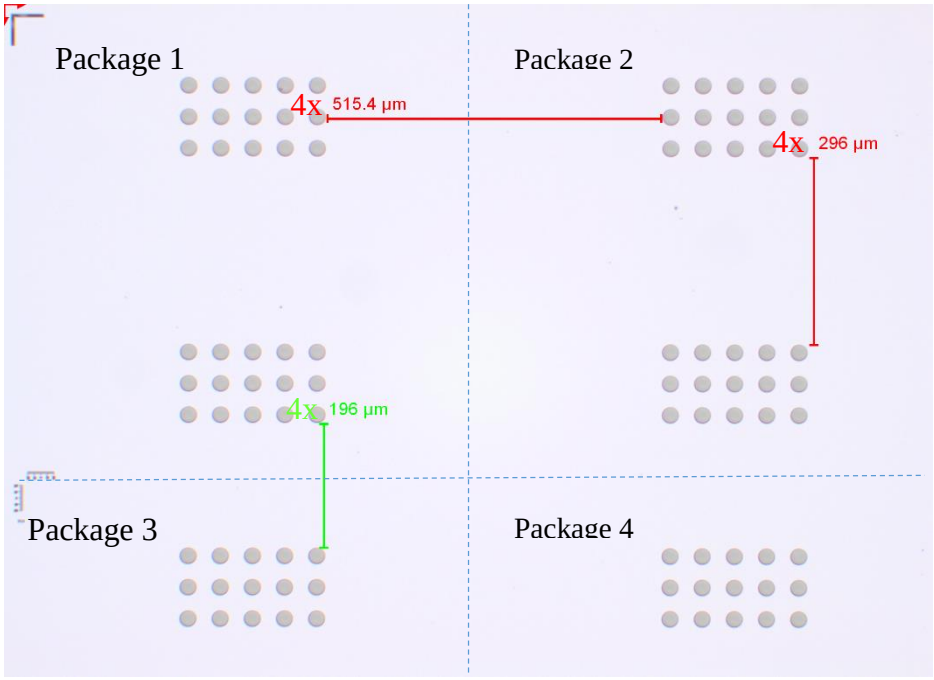


Figure 58: The etched 100 µm through silicon vias in a die

Once the vias are etched through, the oxide is cleaned in BHF (1:7) and sent through the standard non-metal HNO_3 cleaning line before a 200 nm of LPCVD nitride is deposited for isolation of vias.

5.2.3.2 Aluminum - LED-B

Since the LED chip is smaller than LED-A there will be a bit more space left on the bonding surface around the chip and to ensure maximum reflection, aluminum is sputtered and patterned in the space around the bonding area of the chip using 'image 7' as shown in the figure 59 .

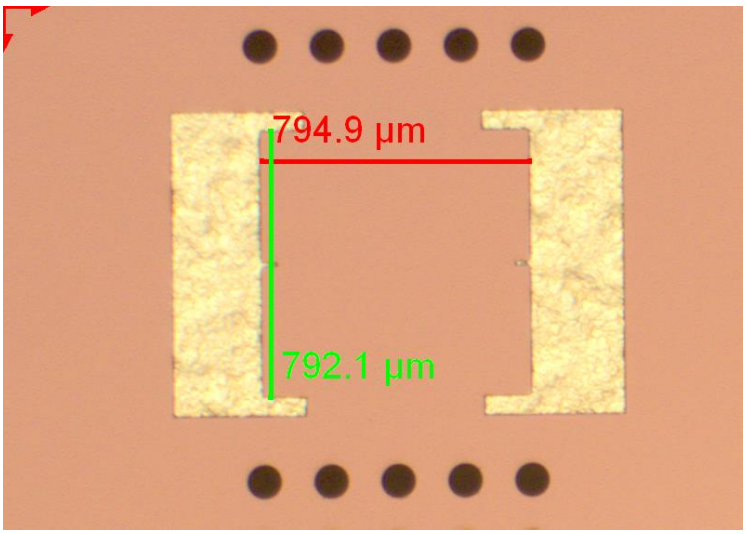


Figure 59: Reflector on substrate for LED-B

5.2.3.3 Filling vias (Copper or Silver) – LED-A and LED-B

The vias are filled with nano silver paste 'DuPont™ Solamet® PV146' as shown . This paste is originally designed for screen printing conductor in thin film solar applications. The puddles are placed carefully on top of the vias and vacuum is applied. Then the wafer is sintered at 250°C in the vacuum oven for 2 hours. The side of the puddles as shown in the figure 60 becomes the side that'll be soldered onto PCB.

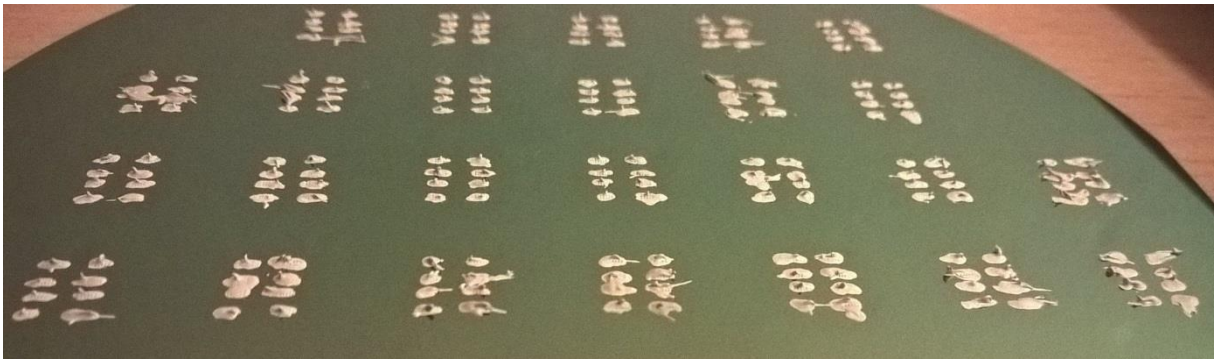


Figure 60: Nano silver paste placed on vias and sintered after filling the vias with vacuum

5.2.3.4 Solder deposition for LED-B (last process step)

Gold interconnects are patterned with the established liftoff process as shown in figure 61. After depositing gold, the same step can be used for Au-Sn (80-20) solder deposition as well. And then the lift can be performed with NMP at 70°C in an ultrasonic bath.

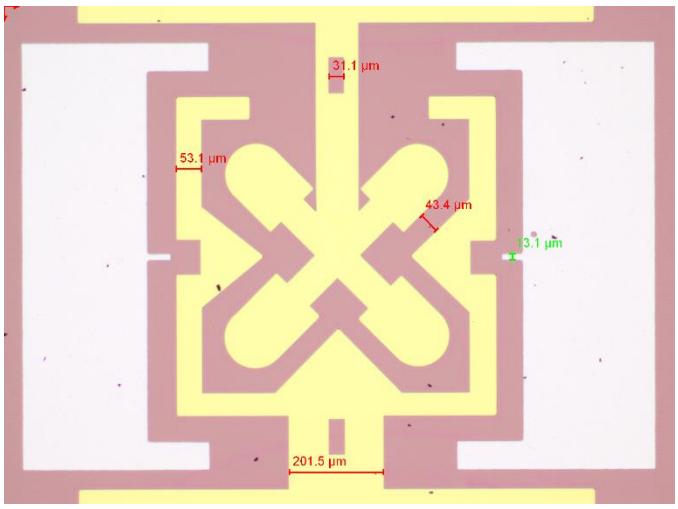


Figure 61: 300nm of Au deposited for LED-B

5.2.3.5 Gold deposition for LED-A (last processing step for LED-A)

300 nm of gold (with 20 nm of chromium as adhesion layer) is evaporated on the flat side of the wafer with the patterned negative resist like shown in figure 62. 'Image 3' is used for this and the liftoff is performed using NMP at 70^{o}C in the ultrasonic bath.

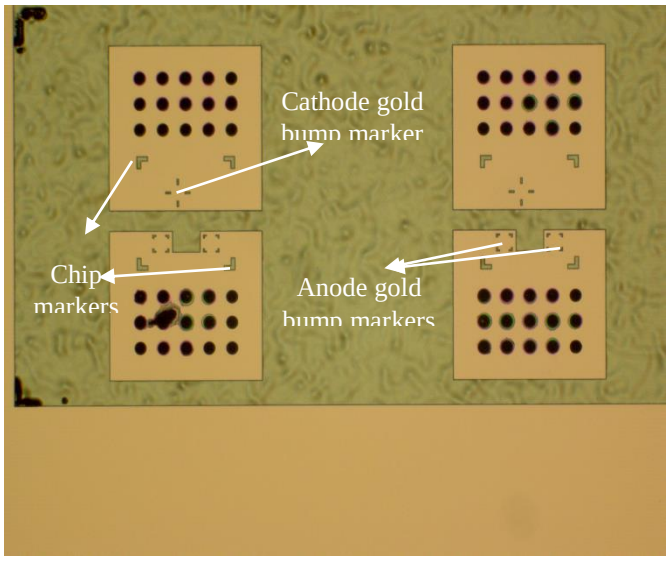


Figure 62: Negative resist pattern for gold deposition

After gold, liftoff the wafer is checked for conductivity from front side to backside with a multimeter. Not all dies were conducting with the least resistance some are not conducting at all. This could be due to the lack of proper contact between the gold and nano silver. This problem is easily tackled with dispensing small amounts of nano-silver with dispenser tools as shown in *figure 63*. The wafer is sintered at 250^{o}C for 2 hours to evaporate the solvents. After this, every randomly selected sample via

section was shorted from top to the corresponding area on the bottom. Therefore the silver paste dispense significantly improved the yield.

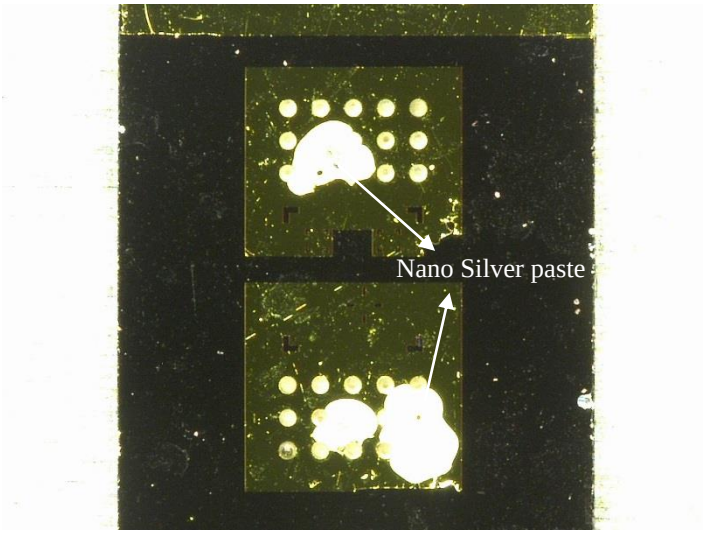


Figure 63: Nano Ag paste deposited on the vias to ensure the least resistive contact to gold and maximum yield of the wafer

The wafer is coated with resist, baked, and finally diced in to 3 mm x 3mm packages which after dipped in acetone to clean the resist are ready for soldering onto a PCB. The dicing was not yielding as the non-uniformity in silver puddles thickness has caused the wafer to break in some areas and thus many of the dies were lost as shown in the figure 64 . The remaining dies are still more than enough in number to perform the final step of packaging at Philips.

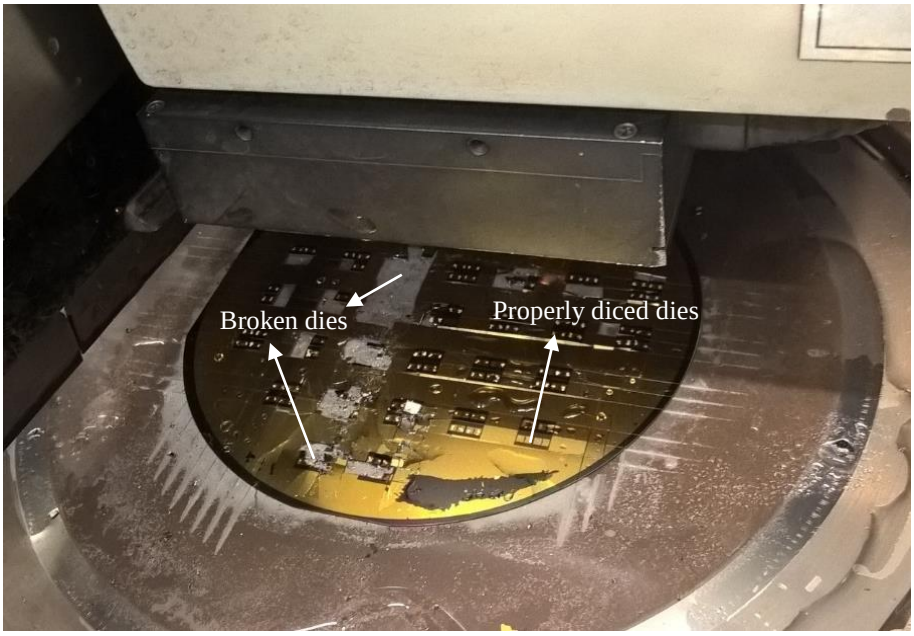


Figure 64: the irregularity of silver puddles caused the dicing to be imperfect

5.3 Oxidation of copper paste

The copper was found to be oxidizing and the repeat of monolithic flow with another paste (Ag) is at the time not achievable EKL due to the PECVD machine issue discussed in *appendix 8.4 BOTLENECK - Issue of repeatability.* A solution to reduce the oxide [28][31] was implemented. The wafer was kept in the vacuum environment of H2 and N2 gasses at 260^{o}C for 10 minutes using 'Axitron black magic'. The oxide was reduced but the uncertainty of the possibility of oxidation in further processing has resulted in a choice to not pursue this until further study of this paste.

The LED-B samples from the dual flow were not taken further due to the high cost of the deposition and as the lack of packages from monolithic flow samples increases cost per package in dual flow substantially. The functionality is proven of the MNP for filling vias and the flow is functioning, the copper paste due to its porosity and oxidation it is uncertain as to how it, even after reduction, will act in the presence of the other chemicals if it enhances or stays the same. Therefore it was decided to not pursue the LED-B solder deposition.

5.4 Chip bonding (Gold bumping and soldering) – LED-A

The diced 3 mm x 3 mm packages are taken to the LED lab in Philips Lighting - HTC 44, Eindhoven for bonding the chips with gold bumping.

The silicon submounts are first checked for their resistance and the resistance for almost all the packages remained after dicing is minimum (i.e. less than the multimeter limit of 0.3 ohms). A single via's resistance was measured to be approx. 0.6 ohms. Therefore due to the parallel configuration of vias, the resistance falls down considerably. The resistance is much low even if some of the vias out of every 15 are not filled.

The 3 mm x 3 mm submounts are mounted onto insulated metal substrate (IMS) and copper (Cu-AlN-Cu) PCBs with copper contact pads. The Hysol's 'ECCOBOND CE3103WLV' electrically conductive lead-free paste was deposited on the two copper pads and the submount is carefully placed and pressed normal to the plane. To make a solid solder, the PCB is heated for 3 minutes at 150^{o}C on a hot plate. Any excess glue may cause leakage/short path parallel to LED and will affect the performance of the final product, this will be seen in the results section '*6.1 I-V characteristics'.*

5.4.1 LED bonding with Au bumping - pre optimization

The gold wire bonding machine from 'Micronnect', shown in figure 65, is used as the gold bumper here. The bumps are created by placing the nozzle at the same point twice and it ultrasonically bonds a tiny wire bump twice at the same point. The bumps are roughly the size of 90 µm.

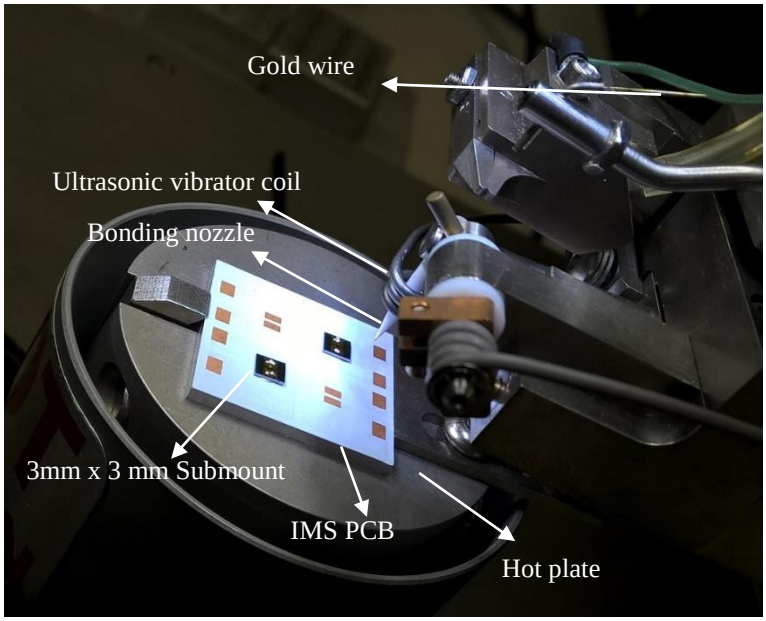


Figure 65: Image of the Micronnect bonding nozzle ready to bump the submount soldered to PCB

Since this is originally a wire bonding tool, when the bump is released a tail tends to follow at the end of each wire cut (shown in figure 66-a). This tail needs to be cut manually with a razor blade like shown in figure 66-b. This process once repeated with all 3 bumps is shown in the figure 66-c.

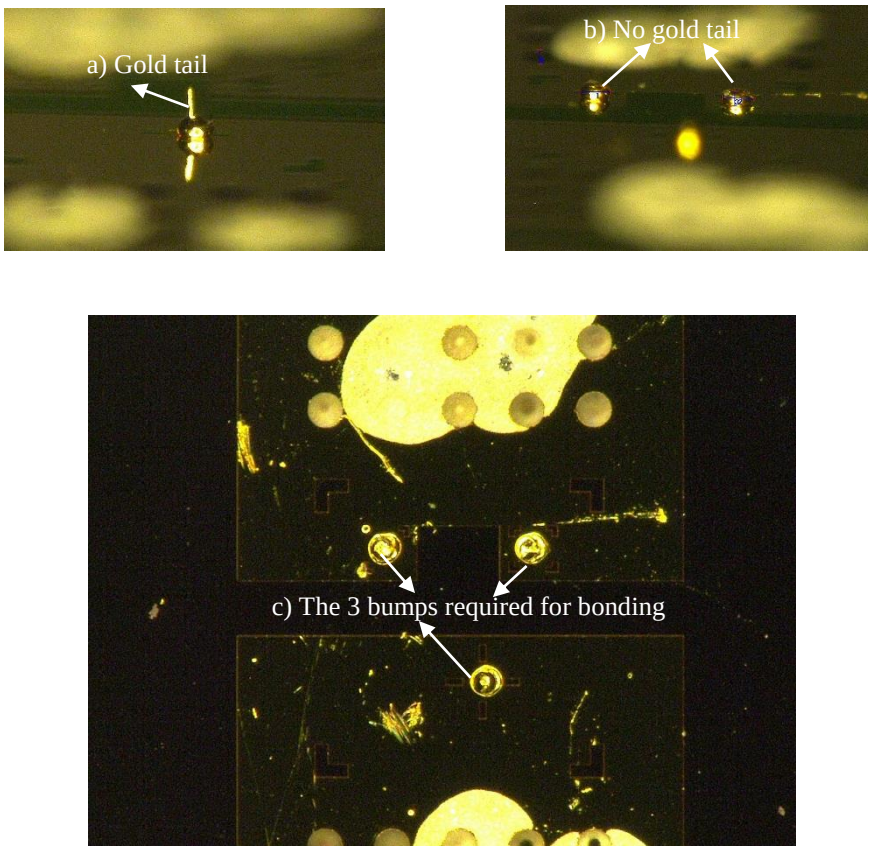


Figure 66: Au bumping: a) Gold tail b) after trimming the tail c) The 3 bumps requried for bonding

Once the bumps are placed, the submount and the LED are moved to the 'Finetech flip chip bonder' machine. The ultrasonic module had to be optimized since it was never used before. This machine has vacuum assisted pick and place nozzle which brings down the chip and ultrasonically bonds the chip as shown in figure 67.

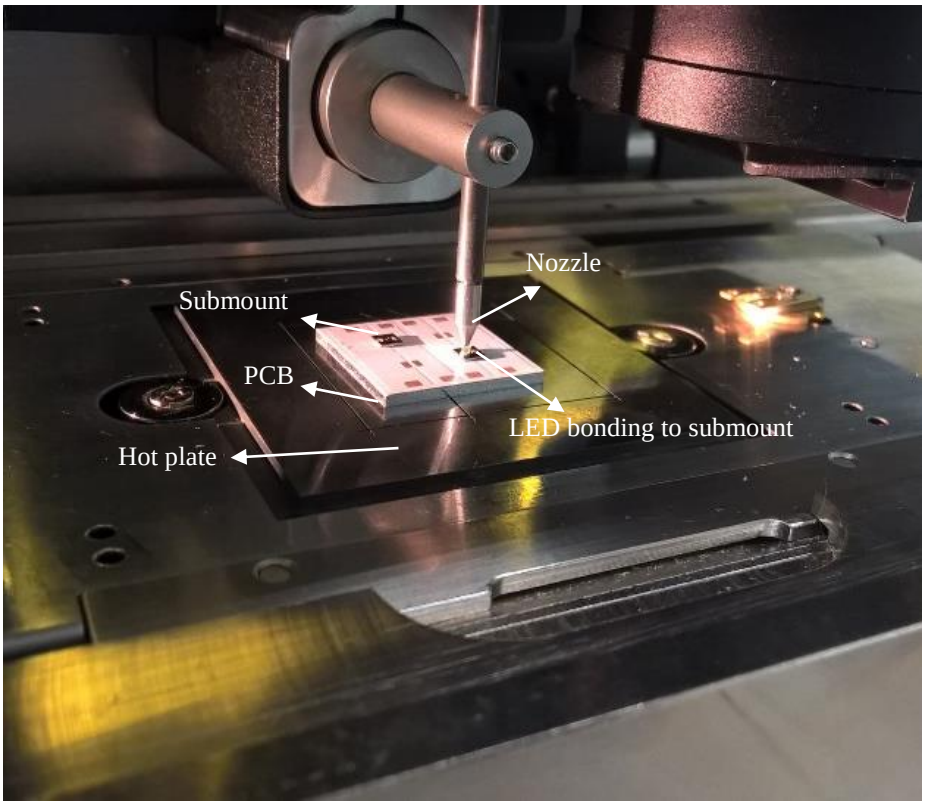


Figure 67: Finetech's vacuum nozzle bonding the chip to submount

First some experiments were done to optimize the bonding and the first bonding was performed with an ultrasonic power of 700 mW for half a second, when the hot plate was ramped up to 120^{o}C. The first two chips were electrically bonded but thermal contact was poor due to the tilt in the submount caused by the silver. Due to this tilt, the bonding left the chip with some tilt a shown in figure 68 .

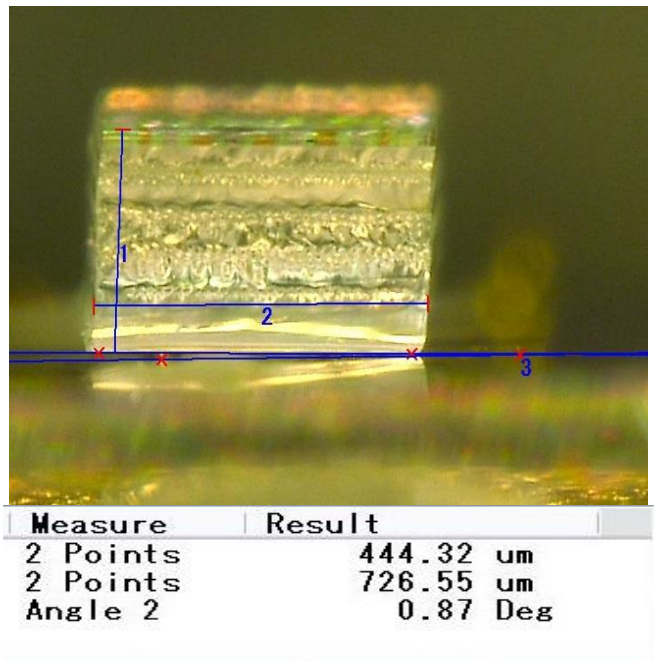


Figure 68: Tilted chip

To reduce the tilt, the silver puddles on the back (figure 69-a) have been scraped off as shown in figure 69-b and the submount is soldered onto PCB.

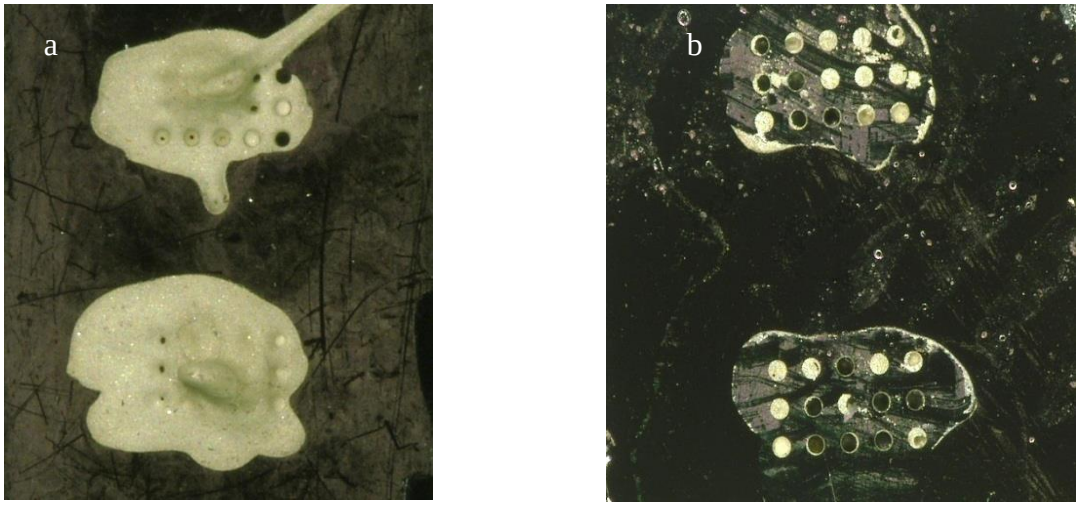


Figure 69: a) uneven silver thickness causing the tilt, b) flattened by scraping with a razor blade

This certainly improved the thermal contact but the tilt is not completely solved. The reason is found to be that the nozzle itself is tilted hence a new nozzle had to be installed. Before it is changed, effort is put into finding another way to solve the thermal contact issue: with SAC solder.

5.4.2 Chip bonding with SAC solder

The ‘ALPHA OM-338-PT‘ is a lead free solder from ‘Alpha assembly solutions’. It is a composition of Sn, Ag, and Cu in 96.5%, 3%, and 0.5% respective ratio. In this experiment the solder is applied in two different ways: i) on the submount in place of Au bumps (in figure 70) and ii) on the pads of the LED chip.

The flux covering the solder reflows between anode and cathode surface areas. However, the solder is not wettable to nitride so it is restricted to the boundaries of gold. The substrate is heated to 260^{o}C so the solder is molten and it starts to spread, allowing the chip to have a larger area in contact with the substrate and thereby better heat conduction. However, the solder also needs to make maximum contact with the anode and cathode contact pads of the chip for the LED to have optimal electrical performance. IV and thermal resistance characteristics will reveal the effectiveness of ‘solder on substrate’ type chip bonding.

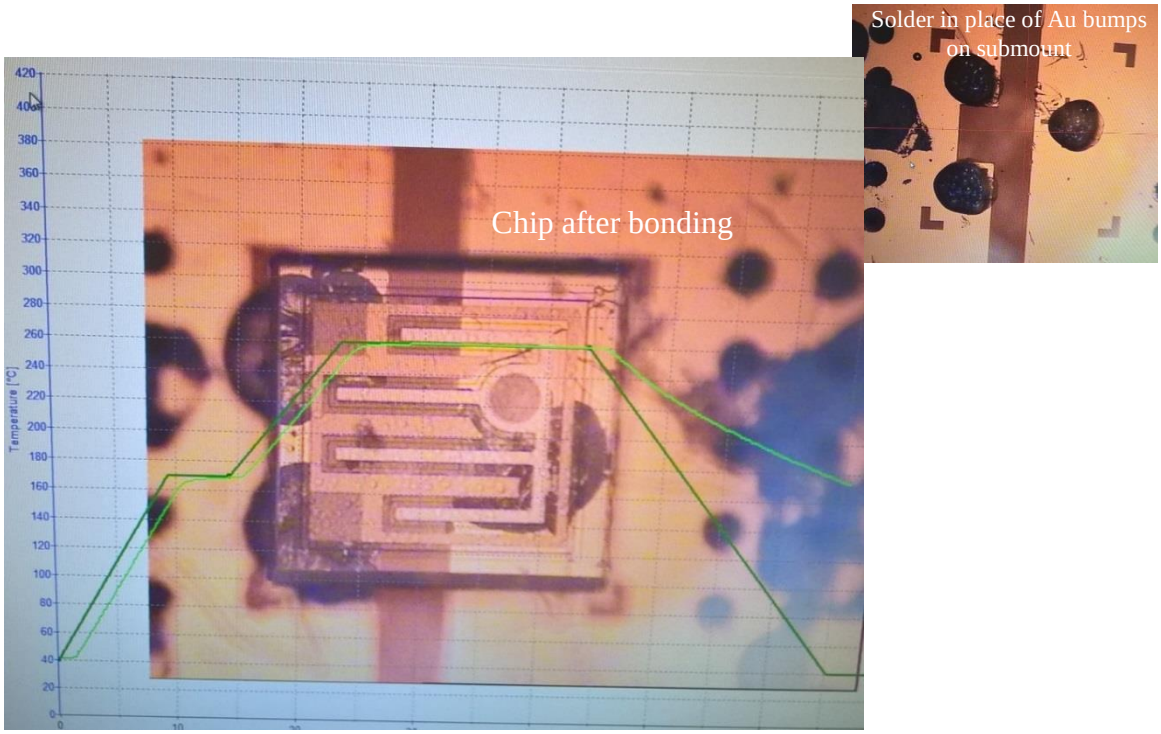


Figure 70: LED being bonded to the submount with solder (inset: solder on submount before chip is bonded)

One more way to use solder in bonding the chip is when the solder is deposited on the contact pads of the chip and then it is brought into contact with the substrate, the chip can be placed anywhere as gold on the substrate is in a large area and the contact pads are already covered with solder (figure 71). The nozzle pick and place is not needed as the chip can be placed manually using a microscope right after the solder is applied on contact pad.

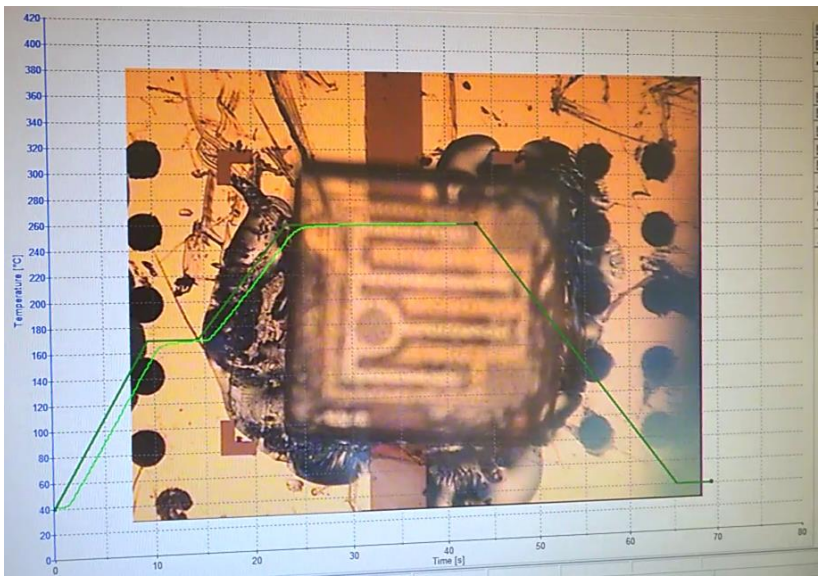


Figure 71: Chip bonding with solder on chip's contact pads

5.4.3 Au bump ultrasonic chip bonding with the new nozzle and process parameters

A new nozzle with a flat tip is used and the ultrasonic power is 500 mW for 300 milli seconds. The hot plate is heated to 120^{o}C. Now since the tilt is reduced, a better thermal performance is expected of this. The figure 72-a shows an illuminated LED in reduced ambient light and figure 72-b shows the LEDs in darkness.

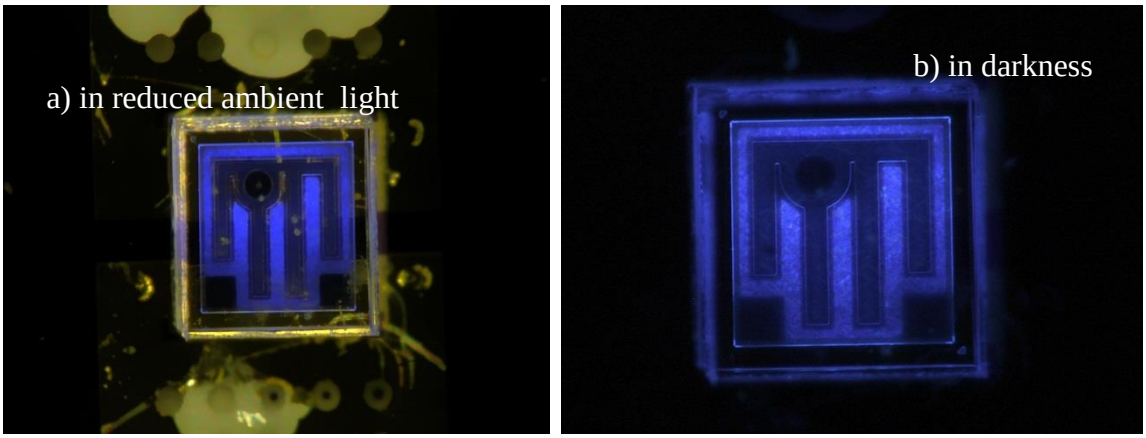


Figure 72: Without reflector cups a) in reduced ambient light b) In darkness

5.5 Attaching reflector cup to the submount

Reflector cups are attached for few packages (figure 73-a) after radiation pattern, optical power measurements were done to observe the improvement. When 100mA of current is pushed the light emission from the chip looks like the one shown in figure 73-b .

Note: *The UV-C radiation is not visible to the naked eye, the blue light is from the radiative recombination of electron-hole pairs at intermediate energy levels. This can be referred in the emission spectrum of the LEDs shown in the results section.*

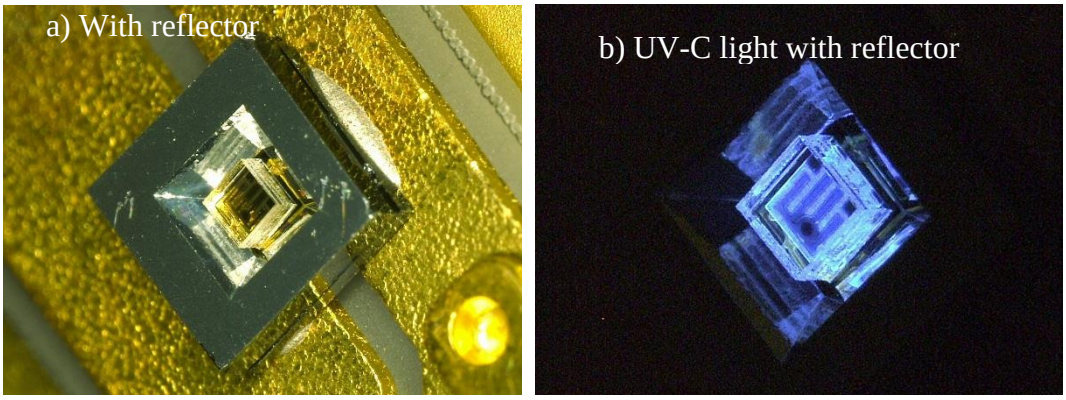


Figure 73: An LED-A package emitting UV-C light at 100mA: a) in ambient light b) In darkness

Summary

The packages using monolithic and dual wafer flows have been processed. The dual wafer flow is clearly easier to implement, cost effective, and highly productive. Due to copper oxidation the Cu-MNP interconnecting material is replaced with Ag-MNP and the dual wafer flow for LED-A was resumed. The monolithic flow was withheld due to the repeatability problems discussed in appendix 8.4 BOTLENECK - Issue of repeatability. The monolithic flow will work with a change in the MNP material to silver and with a PECVD machine which can allow (or better handle) wafers with materials like copper, silver, and gold. LED-B packaging in dual wafer flow was also withheld due to the low quantity of samples and a very high cost of sputtering of Au-Sn solder per package. The overview of the packaging status is presented in Table 3.

	LED-A	**LED-B**	
Flow	Dual wafer	Monolithic	Dual wafer
Packaging Status	Complete (10 packages)	Withheld	Withheld
Comments	MNP changed to silver	Cu MNP oxidation. Too late to change to silver MNP due to irrepeatability	Cost of Au-Sn solder per package too high due to lack of monolithic packages

Table 3: Summary of the packages at the end of processing

In total 10 LED-A chips are completely packaged in dual wafer flow, where:

- 3 packages with chips bonded with solder are soldered on IMS PCBs
- 4 packages with chips bonded after Au-bumping optimization are soldered on copper PCBs
- 3 packages with chips bonded before Au-bump optimization are soldered on copper PCBs

The packages are characterized in their IV, optical, thermal, emission pattern performances in the next chapter: MEASUREMENTS and CHARACTERIZATION.

6 MEASUREMENTS and CHARACTERIZATION

In this chapter the packaged samples are measured to analyze their electrical, optical and thermal performances. The electrical characteristics reveal the resistance and leakage characteristics of the packaged samples. The optical measurements can be used to trace the change in optical power, radiation pattern without and with reflector cup. The thermal transient measurements reveal thermal resistances of individual elements in the resistance network of the packages.

The samples are labelled as follows:

- O1, O2, O3, and O4 for denoting the 4 optimized Au-bumped chips on Cu PCBs
- S0, S1, and S2 for denoting the 3 Au-bumped chips before optimization on Cu PCBs
- IMS4, IMS5, and IMS6 for denoting the 3 solder bonded chips on IMS PCBs (with 5 having the solder on submount)

6.1 I-V characteristics

An LED package ideally should have minimum leakage and resistance. I-V characteristics will reveal some of the package attributes. The LEDs have been probed by the supplier and the average voltage at their operation current 100 mA has been indicated as 6.4 volts with variation of 0.5 volts. Addition of the package should add less or no voltage to this 6.4 volts when 100mA is supplied. The I-V characteristics have been measured with Keithley 2400 connected to LABVIEW environment via GPIB (IEEE-488) cable. The parameters are set to: 0.1A current limit, 50 mV voltage step, and 0 V - 9 V of voltage range.

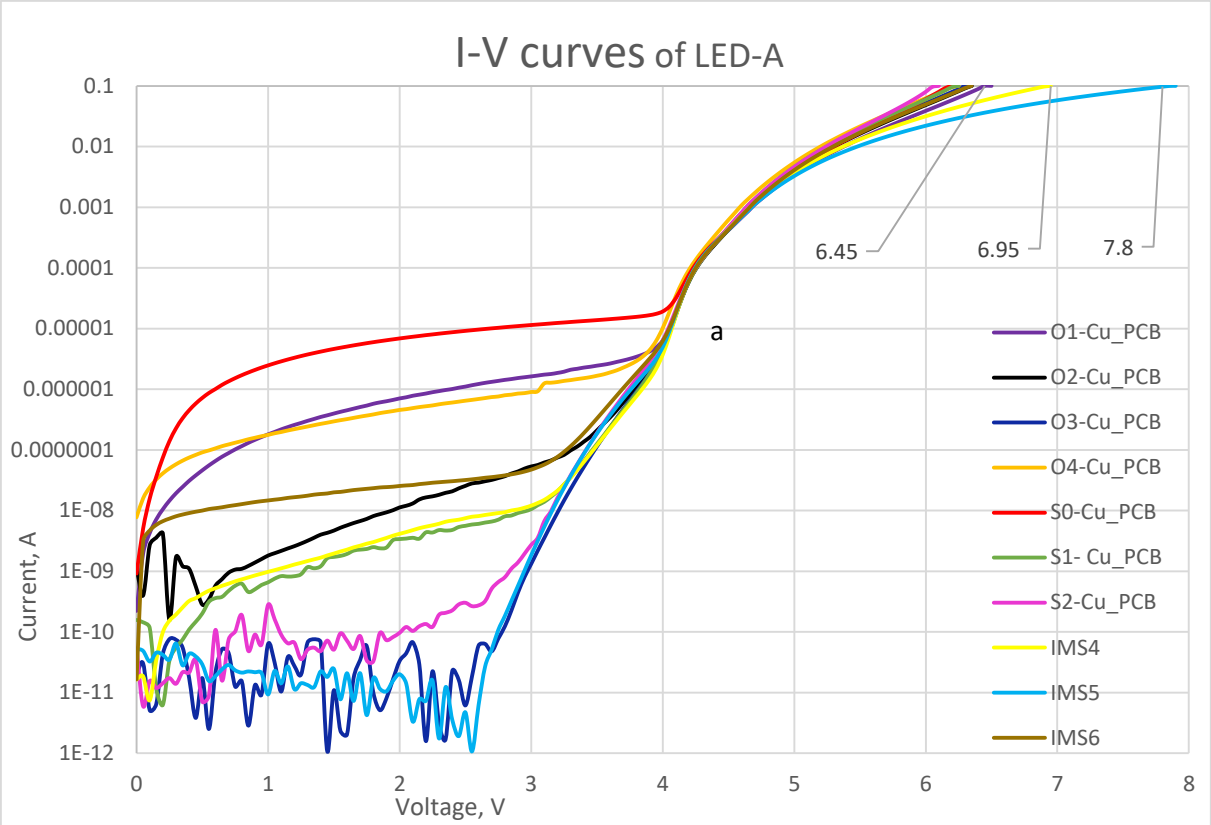


Figure 74: I-V characteristics of all 10 samples of LED-A measured with a compliance of 100 mA

From the above plot (*Figure 74*) it can be inferred that the leakage is in the range of 10 uA and 10 pA. Given the space between anode and cathode of the submount is 0.5 mm, the leakages are expected as the solder was manually dispensed on to the PCB and the submount is manually attached. The pressure applied with hands has caused to move the submounts in the order of microns and hence the minimal contact from the solder spread is causing this leakage.

The voltage at 100 mA for Au-bumped packages are in the range of the supplier's data. However the solder attached-chips are ones with high voltage at 100mA with the highest being 7.8 volts. This is due to the insufficient contact of the SAC solder to the anode/cathode contact pads of the chip. The mass of molten solder flows away when the chip is physically pressed against the submount and the solidification of the mass while cooling down causes the solder to contract and hence the increase in resistance.

6.2 Optical characteristics

The optical power of the LED is measured with integrating sphere and the radiation pattern was measured with a goniometer. The average power mentioned by the supplier is 17mW. 4 packages were already attached with the reflector cup before the measurements to have some completed and

functioning packages and be sent for tests at different departments. The remaining 6 packages went through measurements and tests before and after the reflector cup attachment.

6.2.1 Integrating sphere for studying spectral distribution of optical power

Integrating sphere has the advantage of measuring the optical power over a wavelength range in one measurement run at a rate as low as 1 second per nano meter. After entering from the opening slit, the light intensity reduces from multiple internal reflections. The low intensity light leaves through the exit slit to the spectroradiometer where the power is measured with the help of a monochromator, cooled PMT detector, and control electronics.

The LED is put as close as possible to the opening of the 6-inch diameter 'OL IS-670 integrating sphere', this is also pointed in Figure 75. The light entering the slit bounces off the reflective coating on the interior of the sphere and fraction of the light enters the 'OL 756 Portable UV-VIS Spectroradiometer' from Gooch & Housego [32], as shown in the inset of Figure 75, is used to measure the optical power. An opaque shield is placed in the line of sight of the opening and the exit slit to prevent the influence of the intense light. For these LEDs, the optical power peak is expected around 274 nm. Therefore, the wavelength sweep is chosen for the range: 240 nm – 340nm with a step of 1 nm.

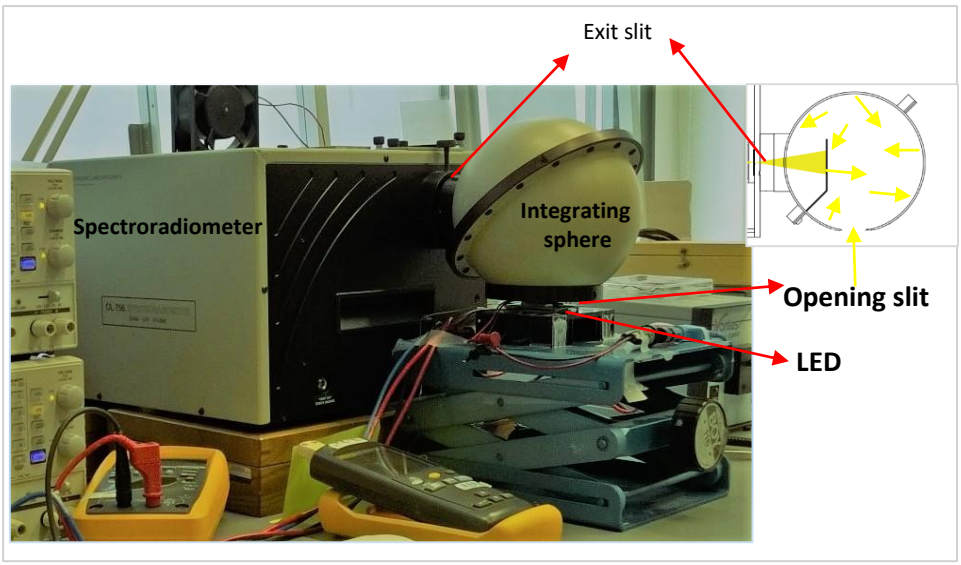


Figure 75: The integrating sphere used for measuring optical power in watts(inset: interior of the sphere)

The measured spectral distribution is then converted to an excel sheet and the data can be used for further studies. An example distribution of a sample with and without reflector cup is shown in Figure 76 .

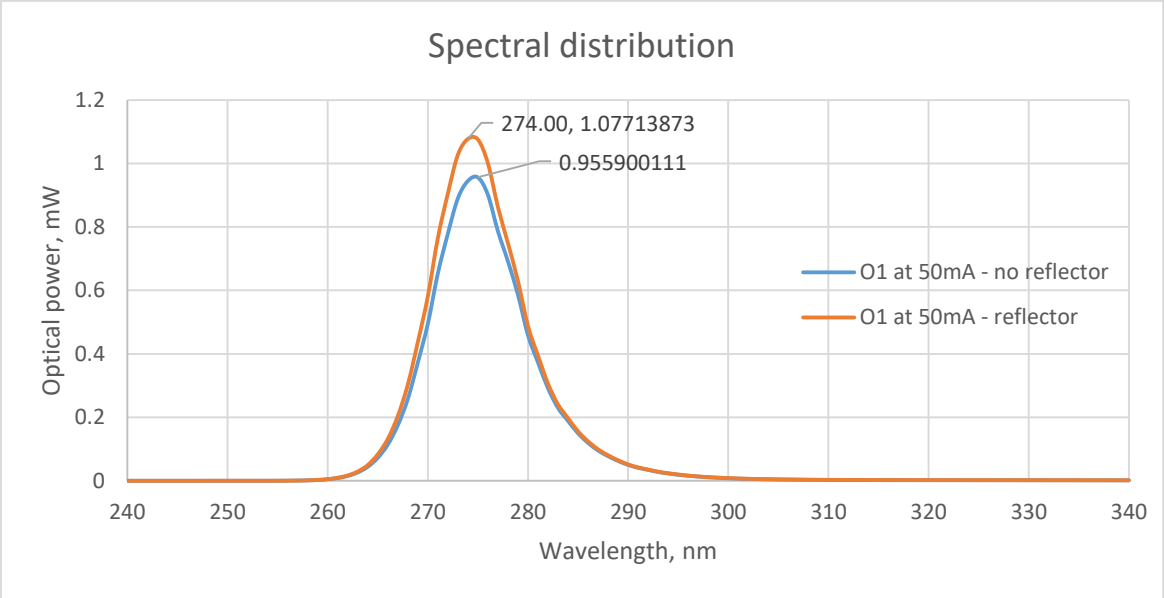


Figure 76: Example spectral distribution of O1 with and without reflector

The above plot (Figure 76) clearly shows the increased optical power distribution over wavelengths. The integrated power is measured at 50 mA instead of 100 mA as the flux was reaching the limit of the sphere for most of the samples at 100mA. The limit wasn't reached at 100mA for some of the samples and the summary is shown in the Table 4 .

Sample	No reflector		With Reflector		Increase. %
	Power @ 50mA, mW	Power @ 100mA, mW(if measured)	Power @ 50mA, mW	Power @ 100mA, mW(if measured)	
O1	11.16	19.04	12.46	overload	**11.648**
O2	11.88	Overload	12.31	overload	**3.619**
O3	-	-	14.54	overload	-
O4	-	-	13.63	overload	-
S0	-	-	10.69	overload	-
S1	12.578	Overload	11.703	overload	**11.703**
S2	-	-	12.229	18.151	-
IMS4	10.99	Overload	12.138	overload	**10.446**
IMS5	9.82	16.28	11.08	overload	**12.831**
IMS6	10.84	overload	12.225	overload	**12.776**
Average increase, %					10.504

Table 4: Optical power of all the samples (6 samples were measured also without reflector)

Note: *It must be pointed out that the spectroradiometer's measurement is dependent on the radiation pattern of the light emitted from the package. This is because the amount of light that exits through the exit slit of the sphere is influenced by the pattern of the light that enters the sphere. Therefore the spectroradiometer measurements are useful for studying the spectral distribution of optical power but not the change in optical power as a result of change in radiation pattern. For example the integrating sphere is reliable for relative measurements such as in tracing optical power degradation over an LED's lifetime; where the radiation pattern is not critically changed. A different measurement technique is needed to really understand the optical power associated with the radiation pattern change. This is where a goniophotometer is extremely useful.*

6.2.2 Goniophotometer for determining spatial radiation patterns

The goniophotometer has the advantage of measuring the spatial distributions of luminous intensity in spherical co-ordinates (r, θ, ϕ) commonly called: radius, theta, phi. The radius kept constant while the theta and phi are varied over the spatial distribution. The 'LEDGON goniophotometer' from 'Instrument Systems', shown in the Figure 77 , is used for determining spatial radiation patterns. Theta is varied from -90° to +90° in 2.5° steps with every phi. While phi is varied from 0° to 180° in steps of 22.5 °. Consequently a total of 577 measurement points are considered. The radial intensity (mW/Sr) at each point is calculated in the range of 200 nm - 400 nm.

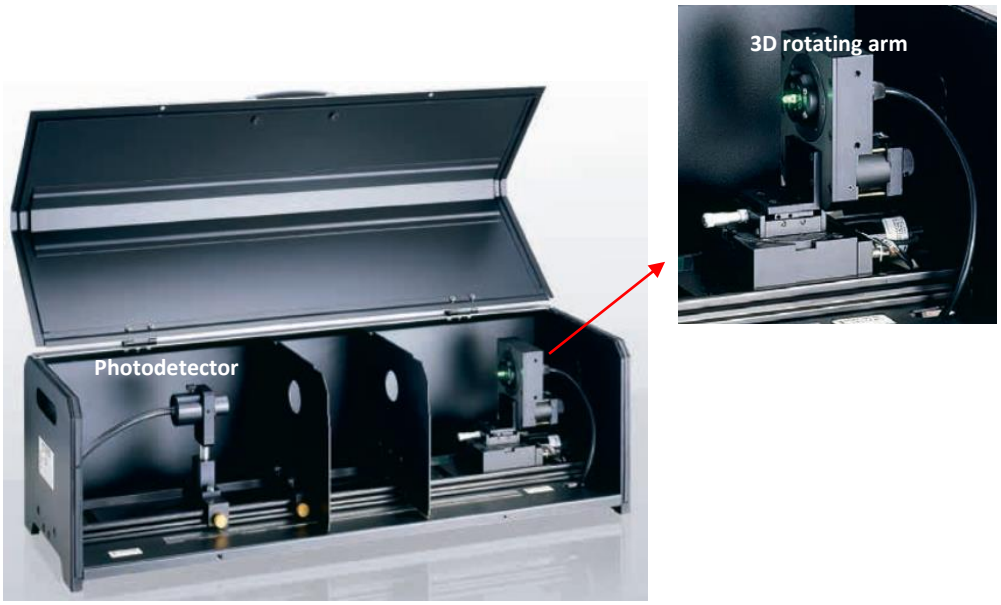


Figure 77: The goniophotometer setup used for measuring spatial radiation patterns (inset: the arm that rotates the LED)

The LED is operated at 50 mA and is fixed on a 3D rotating arm, as shown in inset of the Figure 77, at a reference point from the detector before the measurement begins. The photo detector is rigid while the 3D arm rotates the sample according to the parameters in the operating software. The figure 76 is the graphical representation of the radiant intensity (mW/Sr) along theta of a sample (IMS 4 here) for every phi. There are 8 phis, hence 8 data series. The data is achieved without and with reflector for the same sample.

The advantage of looking at the raw data in this graphical form is that it is easier to spot the differences common to all the graphs at once. Now, let us discuss the area marked as 'x' on the plots in Figure 78-a and b. Besides the change of shape to a more focused beam, the interesting detail is that "the radiant intensity is going towards zero as the plot reaches -90^o and +90^o with reflector". However, "the radiant intensity is reaching approx. 0.3 mW/Sr at -90^o and +90^o when there's no reflector. This is the region where the light could be absorbed by the materials on the substrate like gold (less than 40% reflectance for UV-C) and nitride. The sample's optical power (W) after attaching the reflector was 99.8 % of the power of the same sample without the reflector. There, if the sidewall emission hitting the substrate is considered to be mostly absorbed, it was found that adding the reflector has 6% gain in light which was redirected into the focused beam.

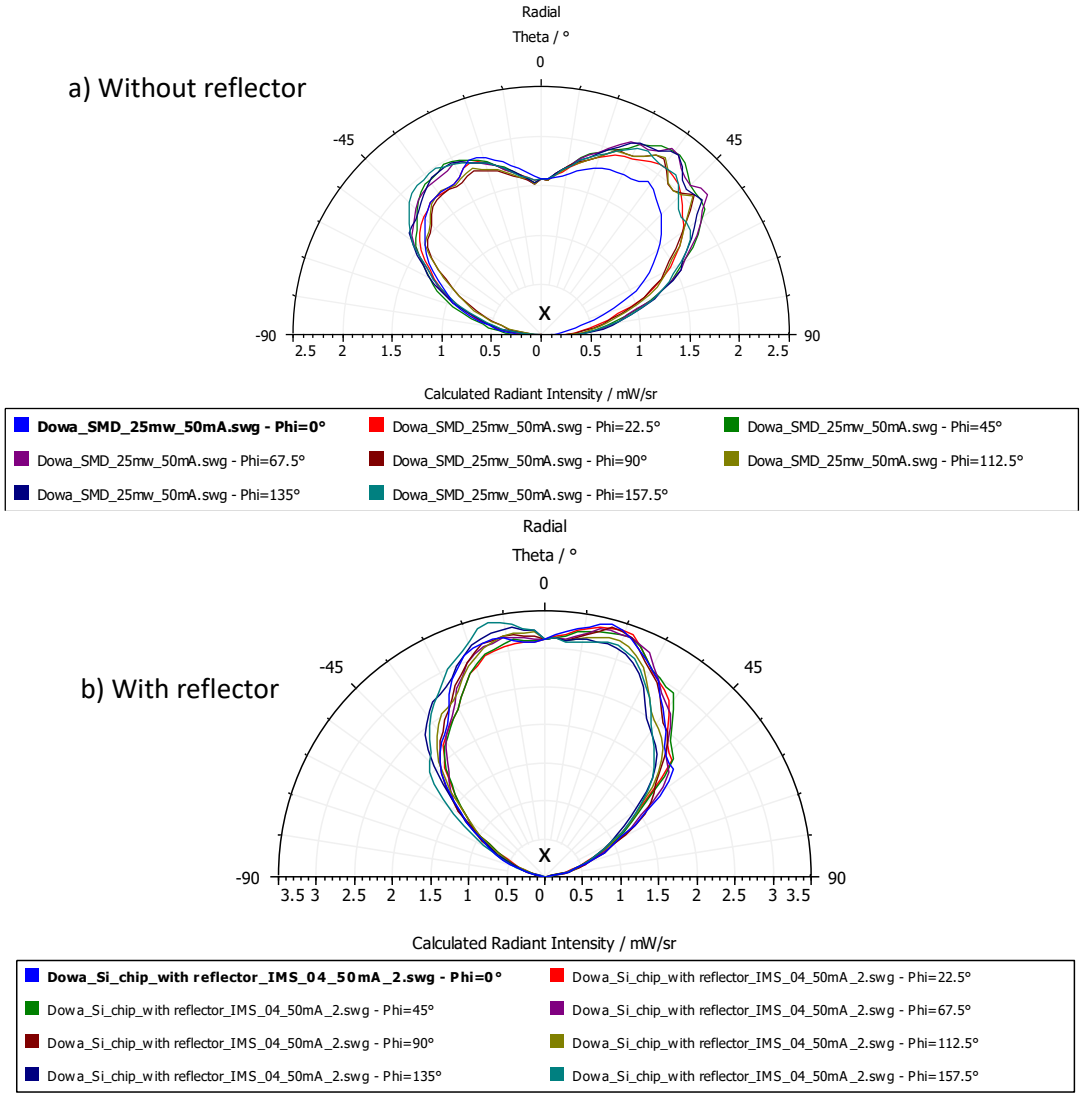


Figure 78: Radiant intensity in theta a) without, b) with reflector

The intensity could be color coded and could be visually presented from top and isometric views as shown in Figure 79-a and b. A quick glance at the isometric views will reveal that:

- with a reflector cup the beam is focused better with uniform shape around the center axis of the LED,
- with a reflector cup, the peak intensity has increased from 2.282 mW/Sr to 3.456 mW/Sr, and
- the intensity is evenly spread around the axis when a reflector is present

In conclusion, with the reflector the light is more intense and focused with almost no loss of light.

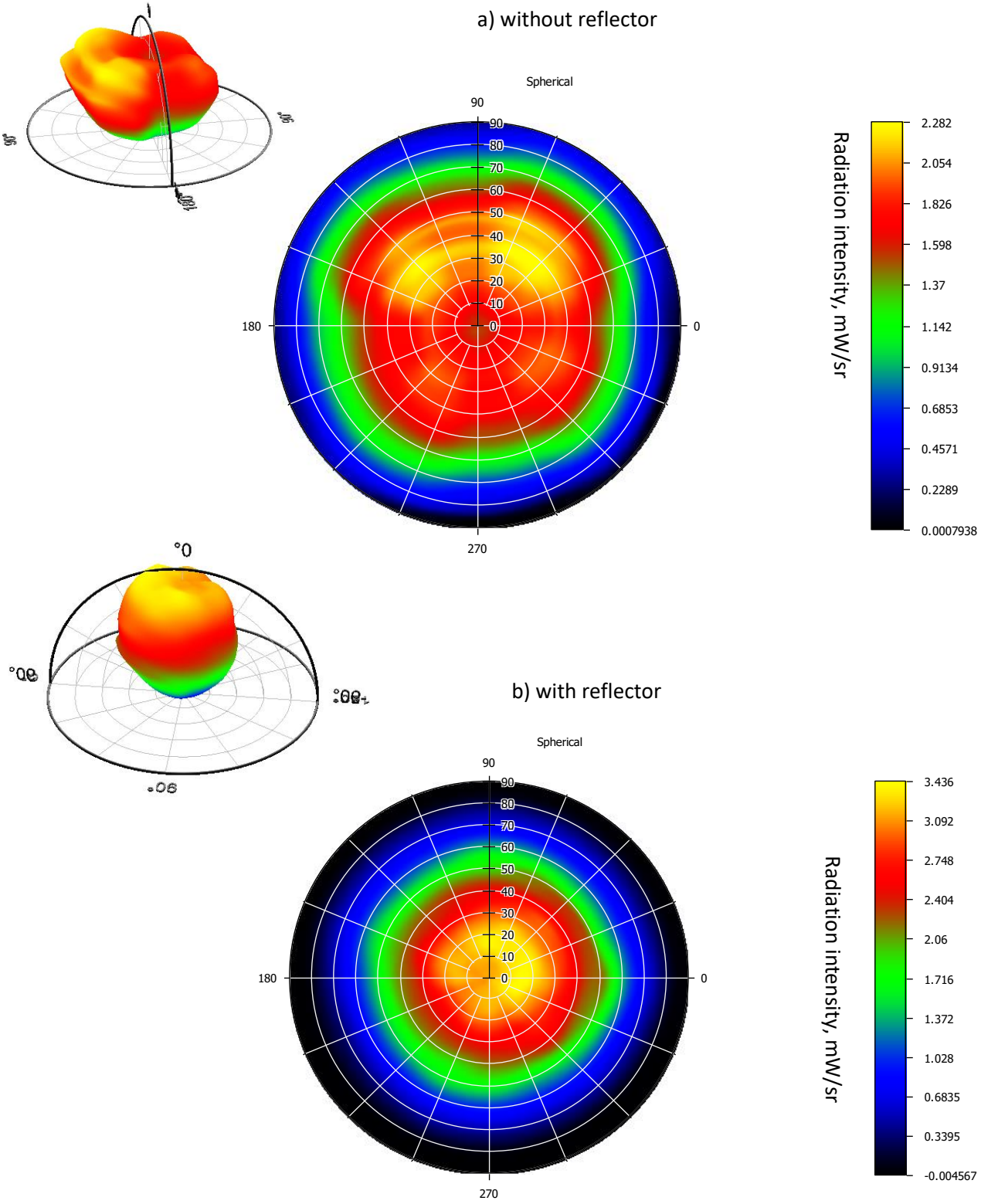


Figure 79: Radiation intensity as seen in isometric and top view a) without reflector and b) with reflector

6.3 Thermal transient characteristics

Good thermal performance of a package is of crucial importance to prevent an LED's junction from excessive heating. Higher temperature may damage the PN junction, increase the forward the voltage, cause wavelength shift, and ultimately may even lead to failure [22]. Thermal dissipation is a serious issue with high power LEDs or in this case: UV-C LEDs with extremely low quantum efficiencies since the electrical power not converted into optical power is dissipated as heat [18]. The knowledge of thermal performance of the LEDs used in this thesis is even more important because of the low physical contact area of the LED to the environment.

The electrical and optical performances of the packages are well characterized. In order to characterize the performance as well, a good modelling of all the levels in the package from junction to the heat sink, namely: LED, submount, PCB is needed. A steady state thermal analysis gives the lump sum of the thermal resistance of the entire package. But a transient thermal analysis can reveal the thermal performance details of intermediate levels of the package. This is achieved by extracting the 'structure functions' from a thermal transient graph of a package [33].

6.3.1 Extracting structural information

The simplest model of a package consists of its thermal resistance (R_{th}, in Kelvin/Watt) and thermal capacitance (C_{th}, Watt.Second/Kelvin). When a power (P in Watt) is applied to the package, the steady state temperature difference across the package is simply '$P*R_{th}$'. But the steady state is achieved after the package experiences a transient increase in temperature. The temperature will rise exponentially with a time constant, $\tau = R_{th}*C_{th}$. Real world packages are complex structures with many stacks of materials and hence contain more than one time constant. Hence there's a need to simplify the interpretation of structural information from a transient graph.

One of the models used for extracting structural information is through the RC models in 'Cauer canonic' form. Where each material's RC structure is placed in a ladder network of the package as shown in Figure 80. It is difficult to interpret in a one dimensional ladder a most packages today have multiple contacts with a material and thus requiring a complex accurate modeling. A solution for easier interpretation is the graphical representation called cumulative structure function (CSF)

The ***cumulative structure function*** (CSF) is the map of the conduction path. It is a graph of sum of cumulative thermal resistances vs sum of cumulative thermal capacitances from junction of an LED to the ambient as shown in the Figure 80 . The differential of capacitance with resistance indicates the interface material details with a peak, this is known as differential structure function (DSF).

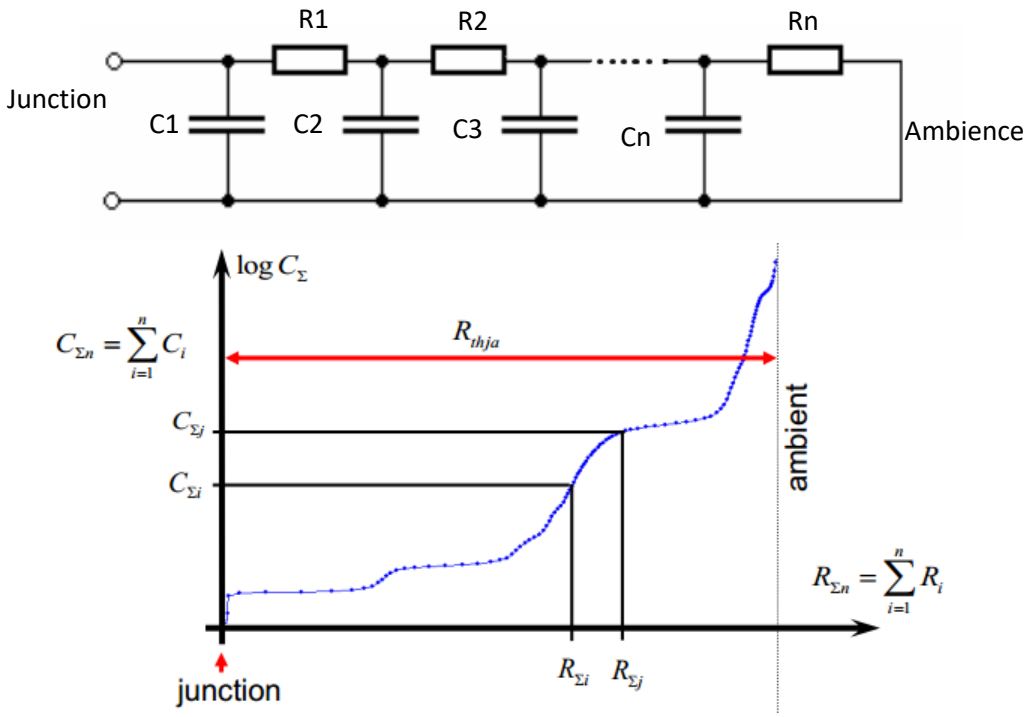


Figure 80: Example of thermal RC ladder and its graphical interpretation with CSF [33]

6.3.2 The thermal transient measurement with Mentor Graphics T3Ster®

The packages are tested for their thermal performance in the T3Ster® advanced transient temperature measurement system with the cooling plate, as shown in Figure 81, and the ambient environment which is set to 25°C. The software can analyze 4 LEDs at once. The samples were driven at 100 mA and the software estimates the temperature from voltage based on the boltzman relations in semiconductor physics thoery [18]. When an LED's junction temperature raises from operation, naturally the voltage falls down, thus requiring lower input power. By definition, the ratio of their change (dT/dP) is the thermal resistance of the package. The thermal capacitance is estimated from the time constant values from the thermal transient data measure by the system.

Since the CSF is a cumulative (addition of all previous values) it has a positive slope for any material. It is flat when it encounters the inerface. The slope of CSF can change if there is a change of material or for the same maerial but with a different size. And since the DSF is the differential of CSF, the DSF shows 'spikes' only at the edge of an interface.

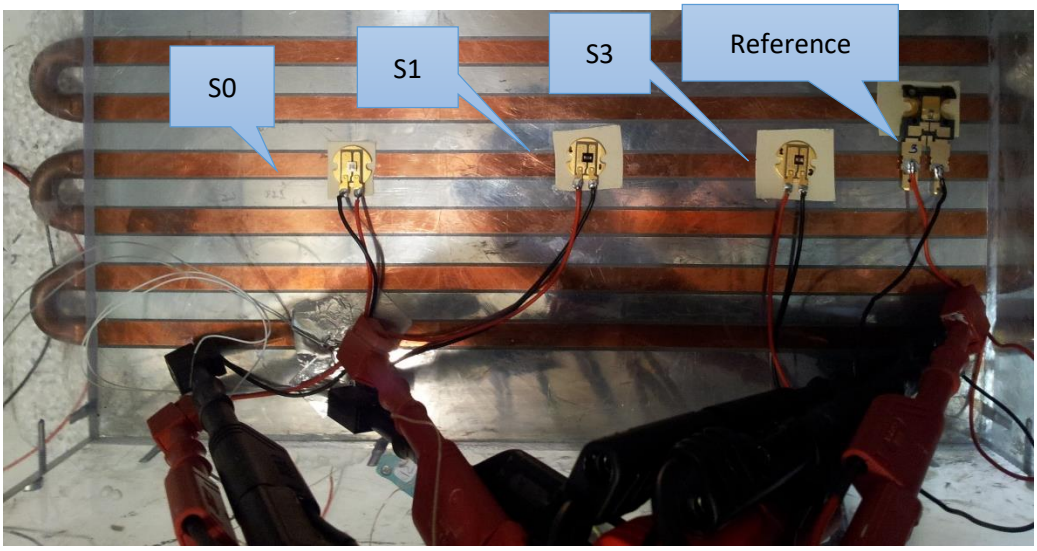


Figure 81: 4 LED s on the cooling plate for T3Ster

Different thermal characteristics were expected from the various combinations of: bonding methods, optimization parameters, and PCBs. The range of change however is found to be large. Bonding is identified as the major cause for such high range as shown in Figure 82. A reference sample (Ref. on AlN on copper slug) from the supplier which is Au-bumped on AlN substrate which is glued to a copper slug is used as a reference for comparing the performance.

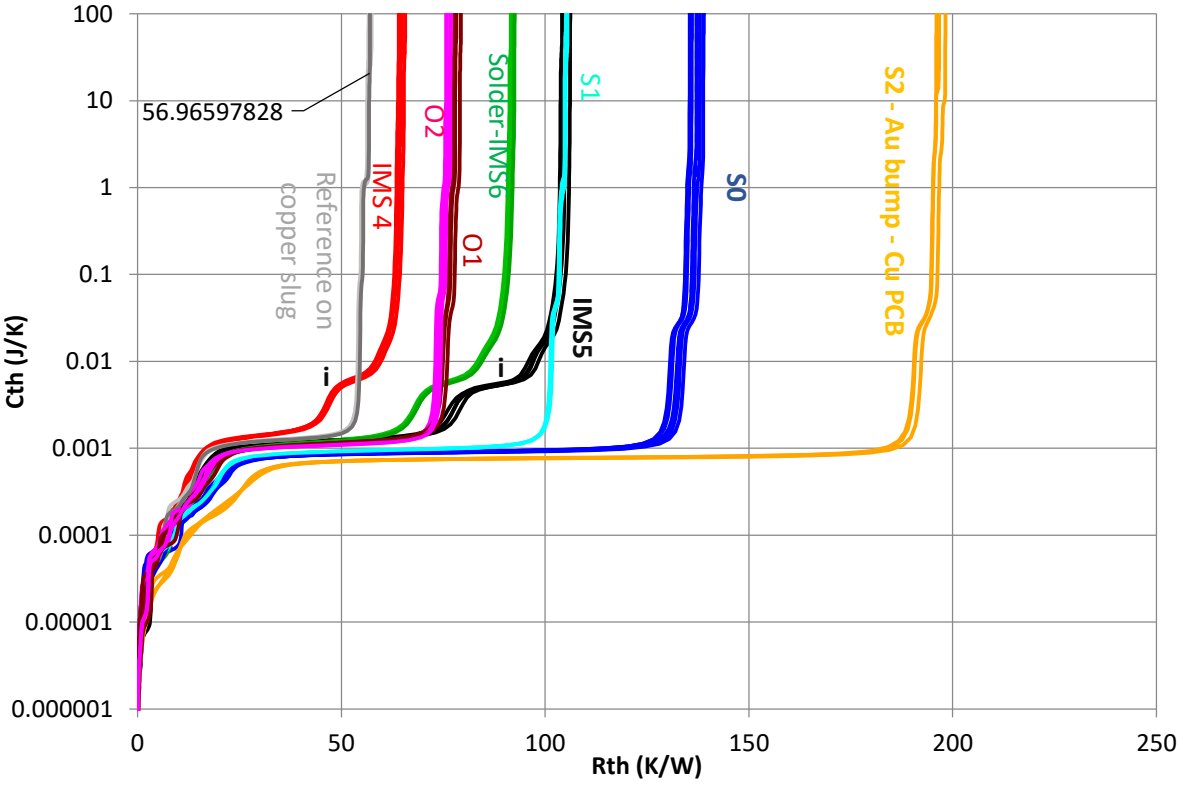


Figure 82: The CSF of all the samples measured

Observations from the CSF plot in Figure 82:

i) Gold bonding has shown most variation in thermal resistance i.e. between O1/O2 and S2. This is due to the optimization time required to fully use the machine for the first time and change the parts to get the best out of the machine.

ii) The insulator material on IMS boards acts as an interface material It also has some additional R_{th} and C_{th} as pointed out with 'i' in the plot area. This could be due to Aluminum having a higher heat capacity than copper (approx. 3 times that of Cu). Also, the insulator on IMS has a high thermal capacitance.

iii) The reference (in grey) and optimized samples (O2 in pink and O1 in brown) perform quite similar until the thermal resistance of the reference sample, then the thermal resistance near silicon interface adds around 16 K/W. This could be due to the improper bonding of the submount, or improper filing of the vias.

iv) The above plot reveals that soldering the chips with SAC has the better average thermal performance. This is because the solder reflow allows the chip to be in physical contact with the submount. However they also require higher average input electrical power at the operating point of 100mA to give the same optical power.

6.4 Summary

All the packages are successfully characterized in terms of electrical, optical, and thermal performances. By confirming the leakage characteristics in few samples, manual soldering of the submounts is advised to be handled more carefully. With the help of right measuring tools the merits of the reflector cup were established. Electrical and optical targets set were met, however thermal performance still needs to be improved. More research in standardizing a flow for final steps such as chip bonding, and soldering etc., would enhance the thermal performance.

7 CONCLUSION and FUTURE WORK

7.1 Conclusion

The UV-C LEDs have a huge potential for market in the near future. And packaging is going to play an important role in their lifetime and reliability performance. These light sources have very low efficiencies but progress is seen every year. The packaging materials chosen would have to be resistant to degradation from the high energy of the radiation emitted. A package with the least thermal resistance, best optical directivity towards the target, least electrical resistance, and best facilitates integration of smart electronics is ideal. The packaging method with low cost and high productivity is desired. This work has explored these highlights with silicon wafer as substrate and fabricating a package in two flows: a) Monolithic, and b) Dual wafer.

The major merits of the dual wafer flow are: the cost and the time of production. The flows have been compared in terms of the litho steps. At the final process step of solder deposition for chip bonding, the monolithic flow has been discarded due to the uncertainty of the behavior of the nano metal paste's oxidation and resistance in presence of chemicals that the wafer would come into contact after this process step. The packages from the dual wafer flow have been used to successfully bond the chips with gold bumping. The following are the highlights of the results:

- A new cost effective way of establishing interconnection in TSV technology has been introduced
- The light from the sidewalls has been redirected with no loss, hence this packaging assists the UV-C LEDs in being better suited for target oriented applications like water purification, DNA and protein analysis, and short range stealth communications in battlefield
- All of the samples show optical characteristics matching with the target data
- Two types of flip chip bonding have been successfully tested: Gold-bumping and soldering with SAC
- The thermal resistance can be improved by the effectiveness of the chip bonding of the submount and the silicon submount bonding to the PCB could be optimized
- The best thermal performance was from a soldered chip which also has the worst electrical resistance
- The thermal performance of the samples with optimized stud-bumping was the second best and it also has great electrical characteristics

- The leakage currents were 10 uA in sub-threshold voltage regions and vary depending on the perfection of soldering of submount to the PCB
- All the gold-bumped samples have I-V operating points (@ 100 mA) matching with the target data

The height difference of puddles on the back of the submounts will cause the submount to tilt and this proved to be a bottleneck, as the chip bonding will not be level due to the tilt. The problem was solved with the scraping of the puddles with a razor blade.

The monolithic flow can be repeated in a different laboratory where samples with copper can be processed. However the dual wafer process is a better choice for easy production and for lesser packaging levels requiring improvement.

7.2 Future work

7.2.1) Encapsulation

The chips are still not protected from the environment. An encapsulating material with high transparency to UV-C radiation and tens of thousands of duration with can be used to shield the chip. Companies like Schott have developed a new UV-C compatible silicone which doesn't get brittle over time as normal silicone does. This special silicone could be used here.

7.2.2) Chemical mechanical polishing

Instead of using a razor blade for scraping the puddles, a CMP leveling would remove the puddles uniformly on an entire wafer.

7.2.3) Optimization of chip bonding

The chip bonding proved to be the bottleneck for thermal performance and this can be performed with standard gold bumps rather than bumps from a wire bonding machine and bonding with a standard bonding machine.

8 APPENDIX

8.1 External quantum efficiency (EQE)

An LED can have an EQE of unity if: A) every electron injected into an LED generates an electron-hole pair required for recombination, and B) every generated pair recombines radiatively in the active region to generate photon, and C) every generated photon is extracted into free space. An efficiency drop at any point in the above steps causes EQE to drop unity. So, the EQE can be defined as product of efficiencies at all the above steps as shown in equation 8-a.

$$\eta_{EQE} = \eta_{inj} * \eta_{rad} * \eta_{LEE} \quad \text{(8-a)}$$

Where, η_{inj} is the injection efficiency,

η_{rad} is the radiative efficiency, and

η_{LEE} is the light extraction efficiency

The injection and radiative efficiencies depend on the heterostructure design and the threading dislocation density (TDD). Hence η_{inj} and η_{rad} together constitute to the internal quantum efficiency (η_{IQE}), which accounts for the photons generated in the device. Extracting the light generated into free space depends on the geometry of the active region and the light absorptivity of the LED materials such as the substrate and the metal contact pads on anode and cathode. Hence equation 1-a can be modified as the product of internal quantum and light extraction efficiencies.

$$\eta_{EQE} = \eta_{IQE} * \eta_{LEE} \quad \text{(8-b)}$$

Currently, the commercially available UV-A LEDs (400nm) have EQEs as high as 60% [34]. The EQEs fall with decrease in wavelengths The EQE for a UV-C LED is as high as 15% [35] with most commercial LEDs having EQE's less than 10%. The main reasons for such low EQEs of UV-C LEDs are identified as TDD of AlGaN, low hole concentration of p-AlGaN, and high absorption of p-GaN metal contact layers [5]. EQE can be improved with manufacturing of LED chip and continuous improvements have been reported over the past few years by using buffer layers over the substrate for lower TDD [35].

8.2 Etchants used in wet etching

i) KOH etching for silicon cavities

Silicon can be etched using wet or dry etching, but wet etching is easier, cheaper, and least parameter dependent. The reactivity of silicon in presence of hydroxides is the basis of using KOH etching. This is an orientation dependent etching (ODE) from the mixture of potassium hydroxide (KOH) and deionized

water (DI water). A 33.33% KOH solution (Kg/L) is used at 85^{o}C to etch silicon at an etch rate of 1.6 µm/min in the [100] direction. The etching is partially anisotropic due to the high selectivity of the (100) plane over the (111) plane ($S_{<100>:<111>}$=400:1) in silicon. A cross section of the profile is shown .

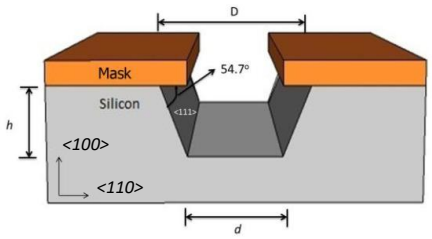


Figure 83: KOH etching profile

The longer the etching is allowed to proceed, the deeper it etches with 54.7^{o} (the angle between (100) and (111) planes) from the edge of the mask window with a constant etch rate. The dimensions are related with the following simple trigonometric equation.

$$d = D - \frac{2h}{\tan(54.7)} \quad (1)$$

From the above figure and equation it can be seen that the mask opening (D) defines the landing space (d) for a given height (h). Similarly, if the wafer's thickness is the same as the height (h), there will be a hole with the size of 'd'. These concepts are used in this work to make reflector cups and integrated reflector cavities.

Both LPCVD nitride and oxide can be used as masks although oxide etches faster. PECVD nitride and oxide masks are weak in the presence of hydroxides therefore they are not preferred. It should also be noted that aluminum is also etched with a high etch rate in KOH.

ii) PES 77-19-04 for etching Aluminum/1%Si (AlSi)

AlSi wet etching is performed by 'PES' which is 77:19:4 ratio mix of phosphoric acid (H_3PO_4), nitric acid (HNO_3), and acetic acid (CH_3COOH) respectively. It is maintained at a temperature of 35^{o}C and it etches AlSi at an approximate rate of 140nm/min. Photoresist can be used as a mask and the feature sizes depend on the mask features printed with photolithography. The process of etching is as follows: HNO_3 oxidizes aluminum to aluminum oxide (Al_2O_3) which is dissolved in H_3PO_4.

iii) BHF (1:7) for etching oxide

Buffered hydrofluoric acid (BHF) is HF with parts of ammonium fluoride (NH_4F). Generally just HF is enough to etch oxide but it is extremely aggressive and the control over the pH and the etch rate is lost. Consequently to achieve a better control over the pH and the etch rate, HF is buffered with NH_4F. In this case it is 1 part HF to 7 parts NH_4F. The etch rate of the PECVD TEOS oxide used in this work is approximately 160nm/min and the chemical reaction between HF and oxide gives water and hexafluorosilicic acid (H_2SiF_6) as follows.

$$SiO_2 + 6HF \rightarrow H_2SiF_6 + 2H_2O \quad (2)$$

iv) 85% H_3PO4 (157°C) for etching nitride

Phosphoric acid (H3PO4) at its boiling point is an effective option for etching nitride. The boiling point of H_3PO_4 varies inversely with concentration of water in the bath. To have an acceptable etch rate of approx. 100nm/min, the 85% H_3PO4 bath is heated to the boiling point of 157°C while maintaining the level of water with the help of a feedback sensing system. The wet etch rate of nitride is not crucial for this work as it is used to clean all the nitride off the wafer and therefore control over the etch rate is not necessary. The chemical reaction is as follows.

$$Si_3N_4 + 4H_3PO_4 \xrightarrow{157C} Si_3(PO_4)_4 + 4NH_3 \quad (3)$$

v) $Na_2S_2O_8$ and H_2SO_4 for etching copper

Etching of bulk copper needs to be extremely controllable because as the bulk copper used in this work is only about 300 nm thick. For this, an oxidizer like sodium peroxydisulfate ($Na_2S_2O_8$) and reducer like sulfuric acid (H_2SO_4) when mixed and diluted in water can etch copper at very low rate. 10 grams of $Na_2S_2O_8$ and 2.5 ml of 99% H_2SO_4 mixed in 1000 ml of DI water can isotropically etch bulk copper at approx. 30 nm/minute.

8.3 RIE etching

The wafer is placed on a wafer platter with voltage opposite in opposite polarity to the plasma charge and the potential difference draws the plasma towards the wafer. Upon reaching the material surface the ions react chemically, but can also knock off (sputter) the atoms with their kinetic energy. This type of etching is highly anisotropic and the profile depends on the gasses, RF power, pressure etc.

The 'Drytek Triode 384T' plasma etcher is used to etch oxide and nitride with photoresist as the mask. The main gasses are hexafluoroethane (C_2F_6) and fluroform (CHF_3) for etching oxide with an RF power of 300W. Whereas C_2F_6 is the main gas for etching nitride with an RF power of 250W.

8.3.1 DRIE of silicon

Etching deep structures like vias with high anisotropy with RIE is achieved with a special case of RIE called DRIE. This process combines chemical and physical dry etching. Even though RIE is well directed etching the chemical nature still introduces some isotropy which may make deep structures with high aspect ratio (depth/diameter) difficult to achieve. A solution for this process is given by a DRIE process called 'bosch' process which uses a combination of physical and chemical dry etching.

It has a loop of 3 basic steps: deposit passivation layer, physically break the passivation layer at the bottom, and chemically etch silicon before depositing passivation layer for next etch. This loop repeats and the number of loops define the depth etched once the recipe is selected.

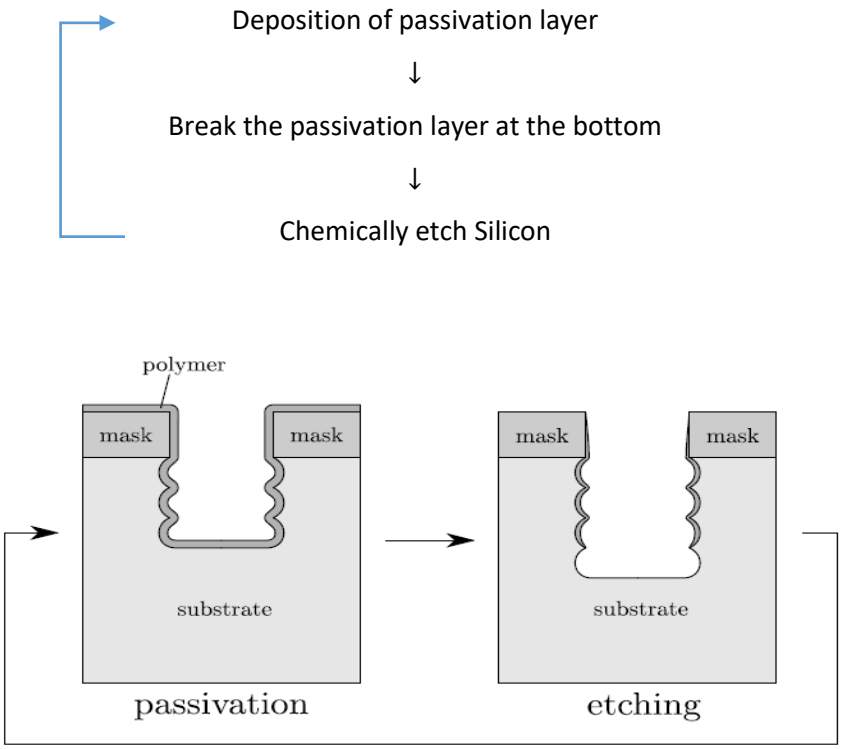


Figure 84: DRIE of silicon – bosch process

The depth of etch depends on aspect ratio, for instance a 100um diameter trench is etched faster than a 30um diameter trench for the same depth. The 'rapier sigma' is used to etch TSVs in this work with a depth rate of 1.5 µm/loop.

8.4 BOTLENECK - Issue of repeatability

The metal carrier is a special carrier specific to the 'Novellous Concept 1 PECVD machine'. The repeatability of the deposition with the contaminated wafers is a bottleneck to this process. Only one wafer came out with successful deposition without any problems in wafer transport. The others were dropped while transporting between the deposition chambers or caused machine interrupt in collecting the wafer back. Despite this, metal carrier is used persistently in hope for another success deposition and the wafer shifted in deposition chamber 3 and the fingers of the carrier arm have bent the carrier wafer. The fingers didn't break, if they had, there would've been a need for replacing the fingers which the EKL didn't possess at the time and the time. A new wafer carrier could be made but it would not solve the original issue of repeatability. If the fingers broke this time, the machine would need to be shut down. Since this is a shared research laboratory it would've interrupted the work of fellow users.

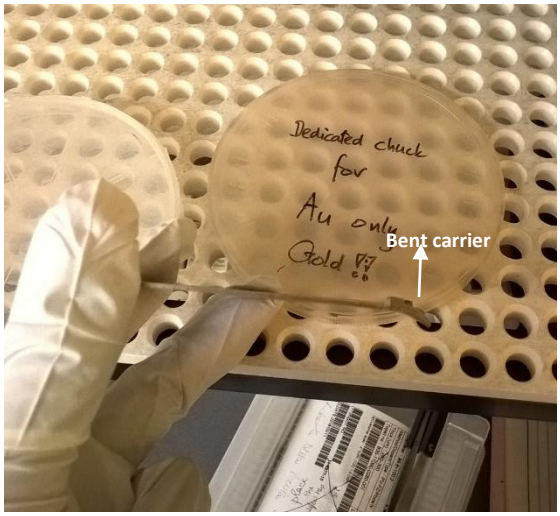


Figure 85:Metal wafer carrier bent by the PECVD machine arm

8.5 Process correction: reflector material etched away while developing

While developing the resist for contact openings, aluminum was found to be slowly etched. The reason was found to be the hydroxide content in the AZ-400K developer. The previous developments have been etching the 300 nm of aluminum and the aluminum was 'visibly' etched at the oxide patterning step. To verify this, another wafer from previous step was put in AZ-400K and the aluminum etching repeated as shown .

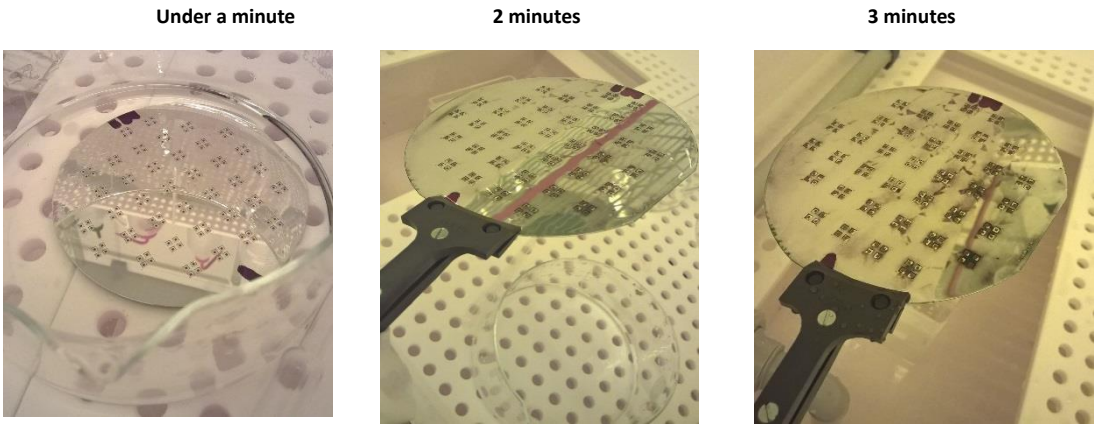


Figure 86: AZ 400K developer etching aluminum over time: a) under 1 min, b) 2 minutes, c) 3 minutes

Solution: The aluminum can be deposited again before the last step (gold-tin) with uses MF322 for development and NMP for lift-off. However this time, the aluminum should be evaporated, as sputtering will raise temperatures and will affect the resist. The same image (image 2) can be used again for lift off.

8.6 Process observation: Aluminum residues from BHF etching of oxide

The aluminum is etched away by BHF while oxide etching and it spread aluminum residues in and it gives a different look. A microscope image is shown .

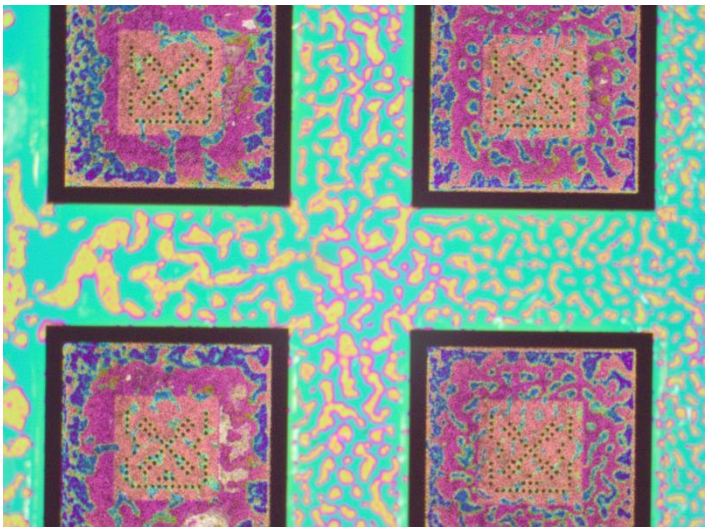


Figure 87: Aluminum residues from BHF etching of oxide

8.7 30 µm Via filling cross section

The m.onolithic wafer was sent for cross-section inspection as it was not used further.

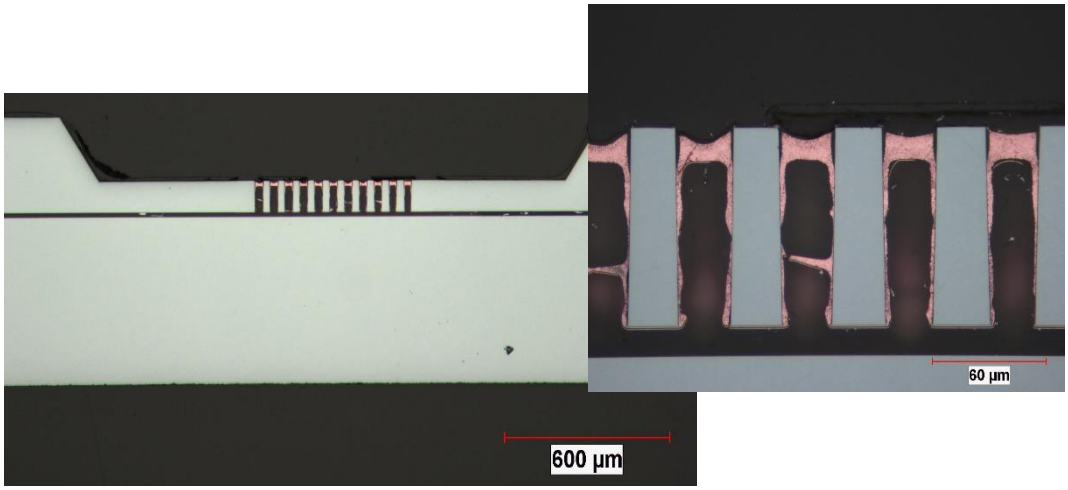


Figure 88: Cu vias cross section

8.8 Via filling and Resistance of TSVs with silver MNP

The via filling with nano silver is not uniform across the wafer. There is overfilling in some area, and underfilling in some.

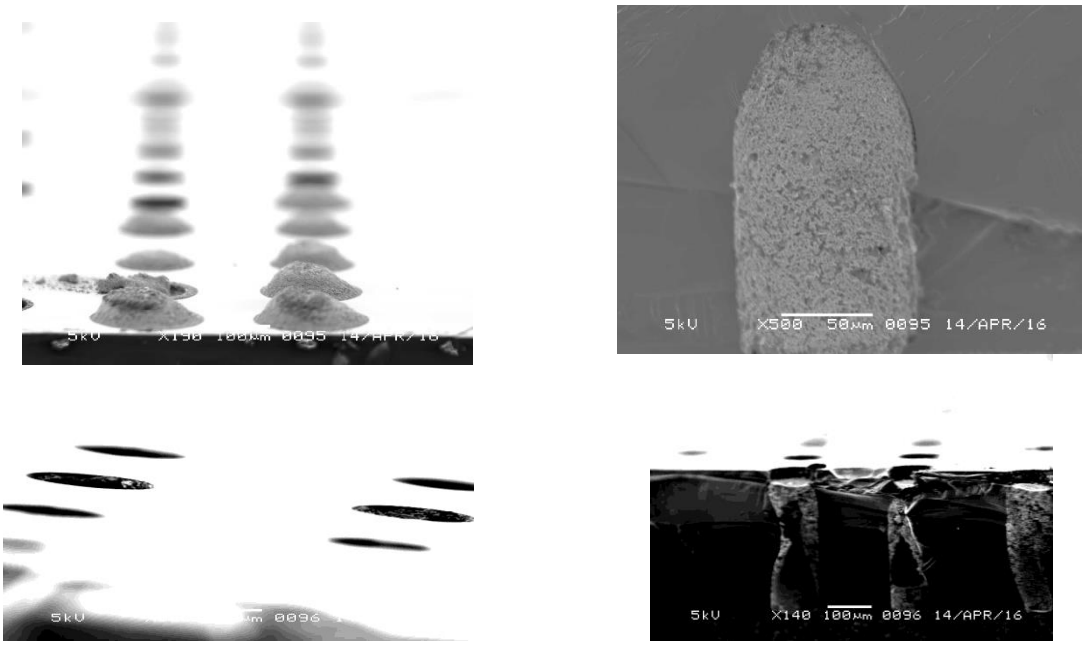


Figure 89: SEM images of over filled and under filled vias with their cross sectins respectively

Resistance is measured with 4 point probe station. Current was measured for a forced voltage from -150 mV to 150 mV and the current was sensed. The data is divided to get resistance in ohms. The least resistance was found to be 0.6 ohms in an over-filled via, the highest being 2 ohms in an under-filled via. Please refer to Figure 90 .

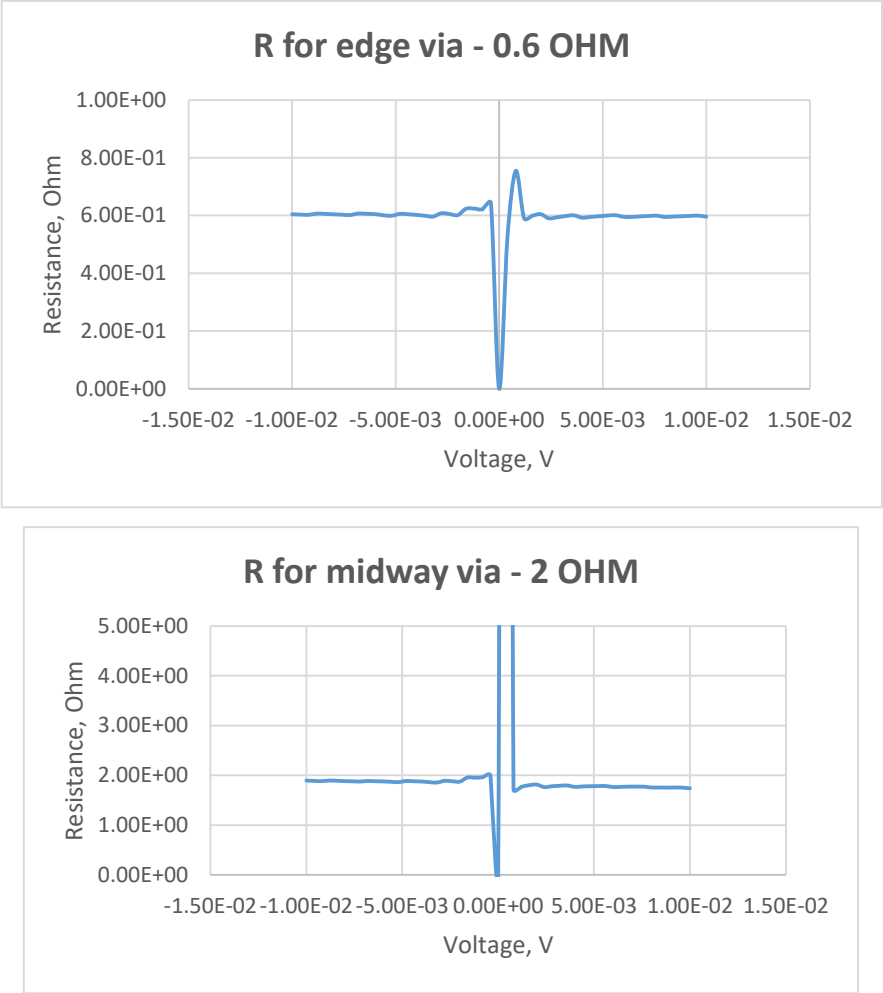


Figure 90: Resistances of fully and underfilled vias

*

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