5G mm-Wave Downconverter

Architecture for the Antenna Dome System

by

R. A. Coesoij

to obtain the degree of Master of Science
at the Delft University of Technology,
to be defended publicly on Thursday June 25th, 2021 at 9:30 AM.

Student number:	4318765	
Project duration:	January 30, 2020 – June 24, 2021	
Thesis committee:	Prof. dr. M. Spirito,	TU Delft, supervisor
	prof. dr. L. C. N. de Vreede,	TU Delft
	dr. F. Sebastiano,	TU Delft

An electronic version of this thesis is available at `http://repository.tudelft.nl/`.

TU Delft

Abstract

The commercialization of millimeter wave frequencies for the 5G New Radio standard requires time and cost effective testing equipment. Antennas and radios are integrated due to the decreasing wavelengths and over-the-air test methods require system characterization. The ADome developed at the TU Delft is designed to perform fast far-field beam-pattern measurements for 5G FR-2 UE antennas by using a powermeter distributed over several nodes.

To improve the system capabilities of the ADome, this work researches the capabilities of retrieving signal information by downconverting the modulated signal to an intermediate frequency (IF). Maintaining amplitude and phase information is used to evaluate the signal quality performance of the antenna-under-test (AUT), quantified by the Error Vector Magnitude (EVM). Two main topics are identified for a downconverting node.

Firstly, the distribution of the Local Oscillator (LO) will be discussed. A power budget is considered for generating the LO signal taking into account high-frequency losses. An implementation with a local multiplier is preferred for driving the downconversion stage. Secondly, the design of a downconversion mixer using a single-balanced passive topology in NXP's Qubic4Xi technology is proposed for the system. The topology is chosen for reduced-complexity and low conversion loss and noise figure.

To conclude, the mixer performance is evaluated using an EVM testbench in Advanced Design System simulator (ADS) to evaluate the EVM performance of the setup. A 5G NR related modulation (e.g. 64-QAM) is generated and corrupted through path loss and non-ideal mixer components. The resulting EVM performance is compared to related measurement setups and systems in literature to evaluate the performance of the test-system.

R. A. Coesoij
Delft, June 2021

Contents

1

Introduction

The mobile telecommunication industry for commercial applications has developed the 5G New Radio (NR) standard [1] to enable higher bandwidth data transfer and lower latency time amongst other features. The clear market-trend and future forecast expectation for the increased user bandwidth requirements can be seen in Figure 1.1. In [2] the limitation of current networks due to latency is described for applications requiring latency predictability such as industrial or medical control driven from the cloud. The current networks are lacking due to latency times in the order of 10 to 100 milliseconds or longer.

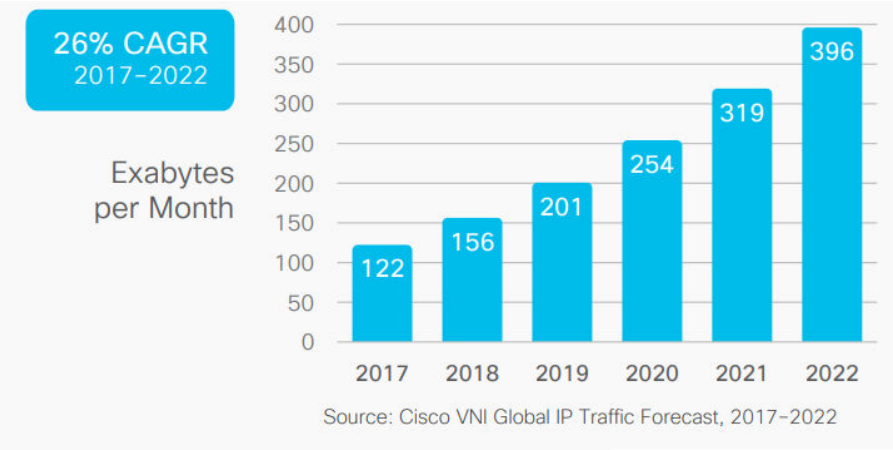


Figure 1.1: The commercial growth of 5G applications from 2018-2020.

Among the variations introduced by 5G NR a key difference, compared to previous generations, is the extensive usage of the mm-wave spectrum. Namely, the frequency range FR-2 operating between 24.25GHz and 40 GHz. The higher carrier frequencies enables up to 400-1200 MHz of signal bandwidth, which is expected to facilitate the data requirements to support the mobile communications, automotive and Internet of Things industries. These aimed requirements include peak data rates up to 10 Gbps and latency time of 1 ms [2].

The frequency up-scaling of 5G NR, with the consequent increase of the path loss and the reduced energy from scatterers, imposes also a radical change in the development of 5G systems. This challenge has been currently tackled by the development of higher re-configurability in the radiation interface of these systems which allows to implement line of sight communication. Across the various implementations of this extra functionality is the usage of phased array systems which allows to electronically steer the main antenna panel radiation beam. The introduction of re-configurability of the radiation pattern that can be generated by these system introduced more challenges in the characterization and testing phase.

1.1. Testing Challenges for 5G Systems

In this section, the scope of the thesis is introduced by starting with testing challenges including over-the-air (OTA) testing, requirements on the electromagnetic wave propagation and link characterization. Furthermore, a brief introduction is given on previous related work to the thesis, namely the Antenna Dome (ADome). The chapter concludes with the research question and the organization of the thesis.

1.1.1. OTA Antenna characterization

The use of mm-wave systems requires beamforming to overcome the high path loss to keep a reasonable signal-to-noise (SNR) ratio. Additionally, efficiency is increased since the energy is focused in a narrow beam. Interference is minimized allowing for higher spatial multiplexing and reuse of spectrum [2]. The beamforming technique is used to create sharp beams of RF energy with low sidelobes. An array of transceivers with weighted amplitude and phase is used to create the desired radiation pattern. By controlling the phase at each antenna, interference is put into use to steer the beam in a certain direction for both transmit (TX) and receive (RX) mode.

Characterization of phased arrays using conventional conducted measurements becomes increasingly difficult due to the large amount of antennas. Consequently, the high integration of the antenna and the transceiver chip makes it increasing difficult for using connectors or probing points to perform conducted measurements. An example of integration of the antenna module and transceiver is seen in Figure 1.2.

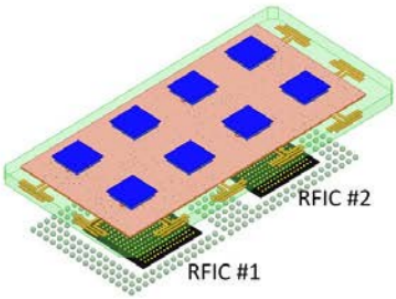


Figure 1.2: Implementation of a phased array antenna and beamforming modules for UE applications [3]

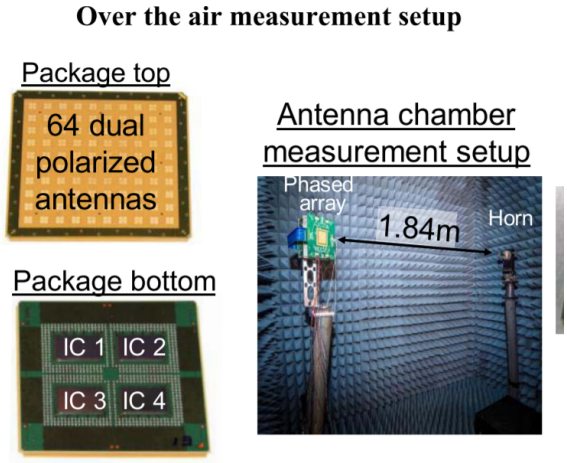


Figure 1.3: Package of a 64 element phased array antenna using four transceiver ICs. The antenna is characterized over-the-air in a anechoic chamber as seen on the right[4].

The alternative for characterizing the antenna-under-test (AUT) is by over-the-air (OTA) testing. An example of an OTA test setup is shown in Figure 1.3. The AUT operates at 28 GHz using a 64-element array with a size of 70mm x 70mm. The distance between the AUT and measurement horn is 1.84m to ensure far-field conditions. The radiation pattern is measured using two motors controlling the azimuth and elevation angles of the AUT. Properties of interest include the maximum Effective Isotropic Radiated Power (EIRP) and the radiation pattern specified by the beam widths, side-levels and notches between the main and side-lobes. Before introducing additional characterization parameters of interest the properties of EM wave properties is discussed in the next section. This will provide insight on the distances set from the AUT and the impact on signal power losses.

1.1.2. Radiation fields

An antenna can either transmit or receive electromagnetic (EM) waves. The radiation mechanism of the antenna is based on the acceleration of electric charge. Time-varying currents in the antenna generate an electric field, in turn creating a magnetic field. The antenna is also considered as converting an EM-wave propagating on a transmission-line, into a plane-wave in free-space [5]. However, at smaller distances from the radiating element the plane-wave approximation cannot be made due to the spherical propagation characteristics of an EM-wave. This phenomenon is shown in Figure 1.4 where three areas describe how the EM-wave develops with respect to distance from the antenna.

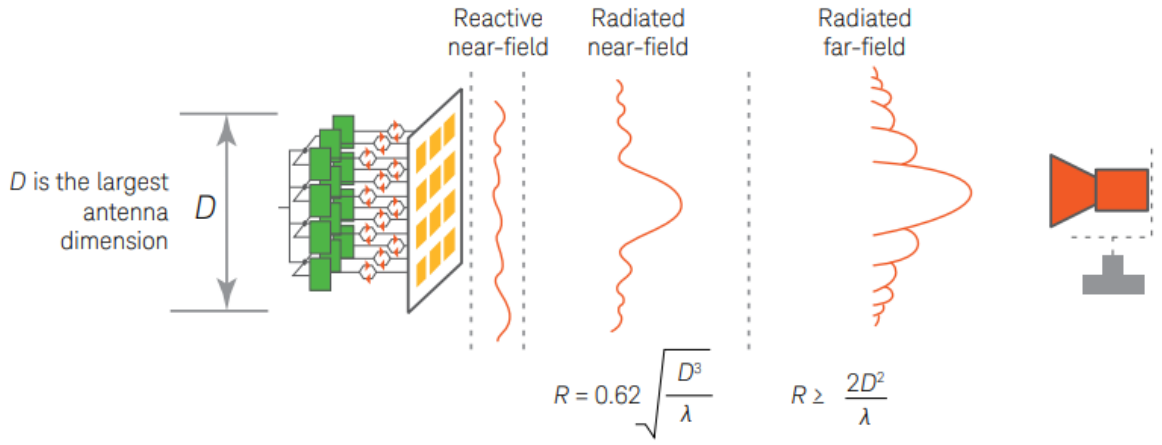


Figure 1.4: Illustration of radiation fields with respect to the distance[6].

A distinction is made between *near-field* (NF) and *far-field* (FF) regions between the radiating and receiving element. In general, no precise boundary is defined between NF and FF. However an approximation can be made by defining the Fraunhofer distance, where "the spherical wave front radiated by an antenna becomes a close approximation to the ideal planar phase front of a plane wave." [[5], p.661]. The Fraunhofer distance is described as:

$$R_{ff} = \frac{2D^2}{\lambda} \tag{1.1}$$

With D the maximum dimension of the radiating element.

Measurements can be performed in the near-field, using near field to far field transformations (NF-FFT) implemented with software or hardware [7]. However, these approaches are considered out of the scope of this work. Therefore, in this thesis the distance for far-field conditions is set as a specification. The distance set by the FF distance influences the signal-power attenuation between the link. The Free Space Path Loss (FSPL is derived from Friis Transmission equation [5] and defines the power loss in a line-of-sight path.

$$FSPL|_{dB} = 20log_{10}\frac{4\pi f d}{c} \tag{1.2}$$

The FSPL is proportional to the frequency 'f' and distance 'd', assuming the antennas are lossless. Now the impact on far-field conditions set by the distance to the AUT are known, we will elaborate on additional characterization parameters where we left off in the previous section.

Link characterization

The main motivation for introducing 5G mm-wave systems and the implementation of phased array antennas is to enhance data requirements to comply with the demand. This is done by characterization of the link of the system. An example of a study on 5G mm-wave antenna systems is the 8x8 array presented in [8]. The system includes 2x2 transmit/receive (TRX) beamformer chips connecting to patch arrays. Sixteen chips were integrated to form a 64-element phased array antenna operating between 28-32 GHz. The paper presents over-the-air measurements to evaluate the performance of the array. First of all the radiation patterns are characterized and verified. Another important measurement of the antenna is the signal quality of the link, using the EVM metric.

The over-the-air measurement was performed at a link distance of 300 meters. The designed 8x8 array were positioned both at the TX and RX side. An arbitrary waveform generator (AWG) generated a 16/64-QAM signal at an IF of 6GHz. At both sides mixers have been implemented to upconvert to a frequency of 29 GHz, using an LO at 23 GHz. The reported performance at a data rate of 12 Gbps is an EVM of 10.6% using 16-QAM and at 9 Gbps an EVM of 5.6% using 64-QAM. The receiver SNR was found to be 24-22 dB at a 2-3 GHz modulation bandwidth. It is important to note that the measurement system must be able achieve performance better than the tested devices to measure its performance. These numbers represent the state-of-the art performance and provide guidelines for the measurement system.

1.2. Antenna Dome

From the previous analysis it is shown that 5G mm-wave systems are characterized OTA for radiation pattern and quality of the link. Most test setups in literature rely on OTA setups using a single receiving antenna and a moving AUT, or vice versa. This section introduces the concept of the ADome and its trade-offs compared with the conventional test setups.

The performance of 5G mm-wave antennas require to be evaluated on a large scale in a fast and cost-effective method. Existing solutions for measuring link performance make use of a motorized setup for scanning the beam pattern of a phased array creating a 3D image. This method is time consuming and requires expensive measurement equipment. The proposed solution of the Antenna Dome (ADome) is able to compete in terms of time and cost. A proof of concept is introduced in [9] measuring the beam-pattern in a semi-spherical measurement setup using several power detectors placed in a dome configuration. The real-time measurement in combination with a low-cost solution makes this a viable competitor, compared to existing implementations.

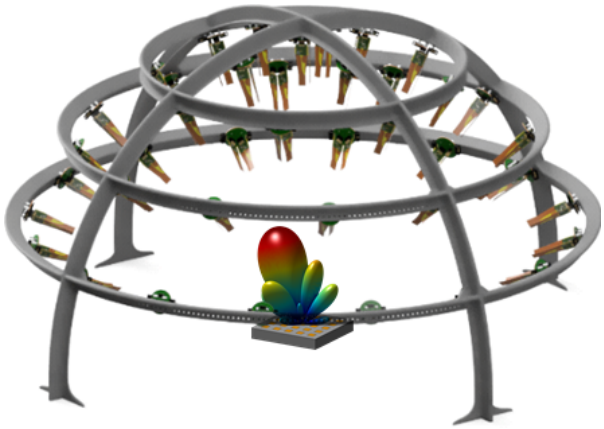


Figure 1.5: The ADome concept [9]

The idea of the Antenna Dome (ADome) is to place multiple power sensing nodes on a semi-spherical surface. The system is able to characterize the beamforming capabilities of an AUT, by implementing multiple nodes across the structure. Consequently, the need for a scanning arm is removed and the nodes capture the data points at once, the user is therefore able to retrieve data from the setup in real-time. The ADome is designed for FR-2 antennas which are to be placed in the center of the dome to be tested. A continuous wave can be applied to the AUT for the dome to sense the power radiated by the antenna. Each single sensing node consists of two Vivaldi antennas, polarized for either the electric (E) or magnetic (H) fields. The power received by the antenna is processed by an off-the-shelf power meter and fed to an ADC. Each node is connected to the other node passing the data using serial communication up to a single microcontroller. The microcontroller passes the data to a PC where the data is processed for visualization. A 3D-mockup of the system is shown in 1.5. The sensors are mounted on 3D printed parts which are reconfigurable, which gives room for flexibility on the size of the structure.

1.2.1. Vivaldi Antenna

The gain of the developed antenna is important for the work in this thesis and is shown in Figure 1.6. The figure shows the simulated and measured values which range between the 12 and 15 dB across the 24 - 40 GHz frequency range.

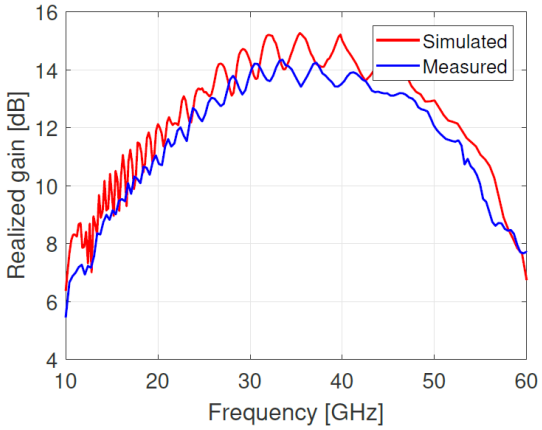
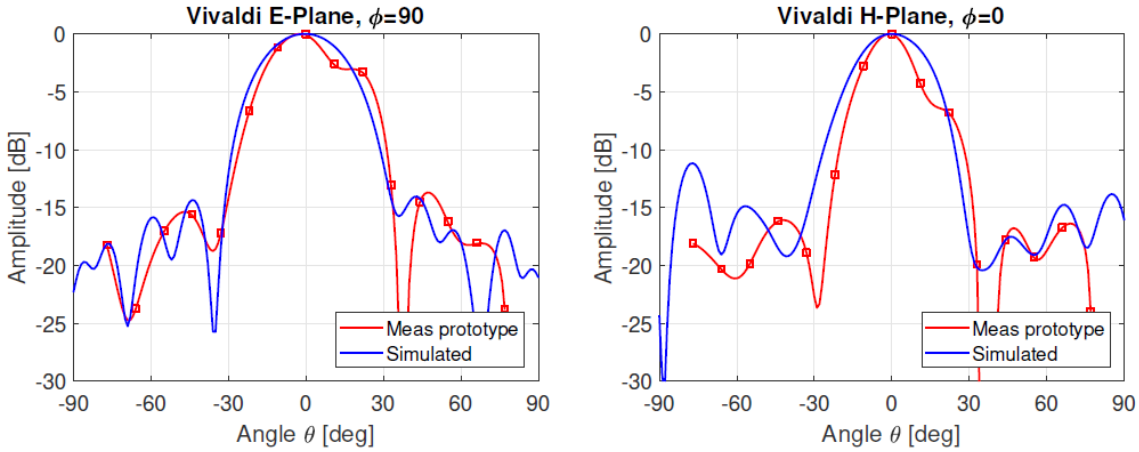


Figure 1.6: The gain of the developed Vivaldi antenna in [9] achieving a maximum of 14 dB at 32 GHz.

To verify the antenna performance, a standard gain horn antenna and a Vivaldi antenna were placed under a simplified dome structure whilst rotating the AUT. The measurement results of a standalone Vivaldi antenna is shown in Figure 1.7.



(c) The measured E-plane of a standalone Vivaldi antenna board, compared to the datasheet specification of a similar horn.

(d) The measured H-plane of a standalone Vivaldi antenna board, compared to the datasheet specification of a similar horn.

Figure 1.7: Vivaldi antenna pattern polarization simulations and measurements [9]

Both the vertical and horizontal polarized antennas measurement results largely agree with the simulated results. The accuracy of the measurement lack in the regions with large slopes, possibly caused by assuming the polarizations are located in a single point, whilst the vertical and horizontal antennas have a slight offset due to practical implementation purposes. This part concludes the introduction of the previous work and the research question will be formulated next.

1.3. Research Question

The real-time antenna characterization system presented in [9] is part of previous work in line of this project. To further extend the measurement capabilities of the system, this work will focus on other characterizations metrics of the AUT. Another key metric to evaluate is the signal quality performance of the AUT. The developed sensor node is able to measure the absolute power of the AUT, suitable for the radiation pattern measurements. However, for measuring signal quality the RF signal needs to be demodulated. Therefore, the main goal of this work is to research the implementation of such a downconverting node to measure the EVM of an AUT. The research question is formulated as follows:

"How to design and implement hardware for the ADome to enable EVM measurement and the possibilities of optimizing on-chip "

1.4. Organization of Thesis

The thesis is organized as follows. Chapter 2 is dedicated to the system analysis with respect to the ADome. Concepts are introduced such as the link budget, the LO distribution, mixer fundamentals, a proposed topology and it concludes with a set of system specifications. Chapter 3 describes the proposed mixer implementation, aimed for in this work. The design is built up from defining the technology and its constraints. Then a design is proposed for achieving the performance with the proposed topology. The mixer is implemented in the technology considering layout constraints. The chapter concludes with a discussion on interfacing directly to the antenna. Chapter 4 is dedicated to results acquired from simulations. Post-layout mixer simulations are presented, discussed and compared. Chapter 5 concludes with a discussion on the presented work and concludes with suggestions on future work.

2

System analysis

In this chapter, the receiver module to enable EVM measurement for the ADome is analysed from a system perspective. Critical components in the system are compared in terms of cost and power. Furthermore, system specifications are derived from these analyses. The last section describes the mixer figure of merits and topologies.

Extending the ADome measurement capabilities by retaining the phase information of the modulated signal, requires analysis into the TX/RX link. The AUT is considered a black box since the performance of the AUT needs to be evaluated using the ADome. However, it is useful to identify each component and its error sources in the link before concentrating solely on the receive chain.

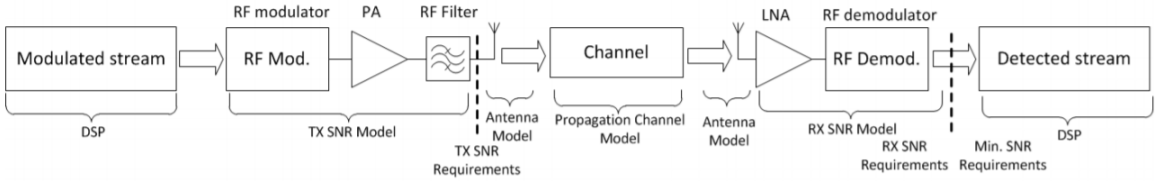


Figure 2.1: Communication system model used in [10] for analyzing 5G RF system performance.

A functional block diagram of the TX/RX link is shown in Figure 2.1. The signal is processed from left to right, starting at the transmitter side. First a digital signal processor (DSP) processes the signal and generates an I and Q component bit stream. For 5G NR the maximum signal bandwidth is specified up to 400 MHz according to 3GPP TS38.810 [1].

The RF modulator is implemented for several functions. The main function is to convert the digital signal from the DSP into an analog signal. A QAM signal is generated by modulating with both in-phase (I) and quadrature (Q) inputs. Lastly, the I and Q components are up converted to the desired radio frequency and combined to form a single complex modulated signal. This results in a bitstream being represented in a symbol, consisting of $log_2(M)$ bits, depending on modulation type (M-QAM).

Next, the Power Amplifier (PA) provides gain to the RF signal such that the radiated power from the antenna is sensed at the receiver. The power amplifier is designed by trading off linearity versus power, while maximizing the component efficiency (i.e., DC to RF power conversion). The linearity of the PA is essential to achieve the acquired EVM performance of the TX, since the signal is both amplitude and phase modulated.

The RF signal is radiated by the TX antenna and propagates through a channel to the RX antenna. To characterize the output power of the transmitter using a single definition, the Effective Isotropic Radiated Power (EIRP) is used. This expression for the power includes the gain of the antenna G_t, as well as the transmit power generated by the PA, P_t [5].

$$EIRP = P_t G_t \tag{2.1}$$

This expression will be used in the link budget for the power received at the RX antenna. A similar process as performed at the transmitter side is now performed at the receiver in an opposite order to convert the RF modulated signal into a digital bit stream. The RF signal is first amplified in a low noise fashion, down-converted, filtered, digitized and finally processed.

2.1. Concepts

An introduction is given on the concepts used throughout this work. Starting with concepts relating to physical phenomena regarding EM waves and digital modulation techniques. The last concept to be discussed is the distribution of the LO-signal. The section is concluded with concepts specific to the mixer circuit-design.

2.1.1. Modulation and errors

A radio link is designed for exchanging information between the receiver (RX) and transmitter (TX). At the TX side, the baseband processor represents the information in a binary representation, which will be referred to as the bit-stream. The bandwidth of the baseband signal for FR-2 NR is specified up to 400 MHz. The bitstream is then processed into the required modulation. For 5G NR signals this is specified in by the 3GPP standard. The TS38.101 [1] standard specifies the following modulation techniques for 5G NR: BPSK, 16-QAM, 64-QAM and 256-QAM. Binary Phase Shift Keying (BPSK) and Quadrature Amplitude Modulation (QAM) are variants of modulating the phase and amplitude of the signal.

The constellation diagram is constructed by an In-Phase (I) and Quadrature (Q) axis. Mapping points in the diagram result in a signal that is modulated both in amplitude and phase. Information is coded in bits, where each point in the constellation diagram represents a symbol. For example, with 16-QAM a symbol contains 4-bits and represents a single point in the constellation diagram.

Errors due to non-idealities between the TX and RX are quantified by comparing the ideal signal vector with the received vector. The Error Vector Magnitude (EVM) is defined by measuring the vector between the ideal and measured constellation point. An illustration of the error vector is shown in Figure 2.2.

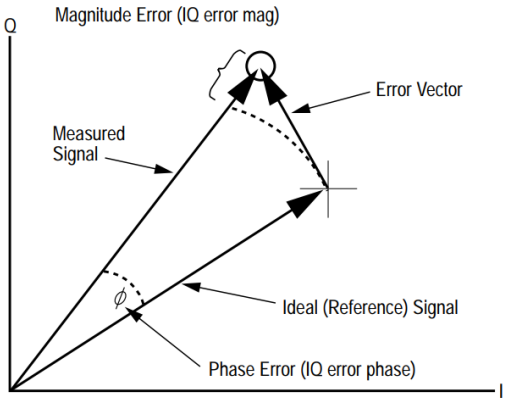


Figure 2.2: Illustration of the Error Vector Magnitude [11]

Modulation type	Average EVM Level (%)
Pi/2 BPSK	*30*
QPSK	*17.5*
16 QAM	*12.5*
64 QAM	*8.0*

Table 2.1: EVM 5G NR Specification [1] Table 6.4.2.1-1

In typical measured constellation plots, a 'cloud' of points around the ideal point can be identified. All the resulting error vectors can be averaged to derive a single metric for the Error Vector Magnitude. In a recent paper [12] two commonly used definitions, EVM_{max} and EVM_{RMS} . In this work the latter definition is used in eq. 2.2

$$EVM_{RMS} = \frac{\sqrt{\frac{1}{N}\sum_{i=1}^{N}|S_{ideal,i} - S_{meas,i}|^2}}{\sqrt{\frac{1}{M}\sum_{i=1}^{N}|S_{ideal,i}|^2}} \tag{2.2}$$

The signal-to-noise ratio (SNR) is directly related to the EVM. Both metrics express noise relative to the ideal signal as shown in eq. 2.3

$$SNR_{dB} = 20log_{10}(\frac{1}{EVM}) \tag{2.3}$$

In 5G systems, as in any telecommunication system, the minimum requirements for EVM are given by the standard. For each modulation scheme an EVM requirement is given, according to their complexity in the constellation diagram. Increasing the number of constellation points require a more stringent EVM performance. An overview of the required EVM performance is given in Table 2.1.

2.1.2. Receiver chain

The previously introduced relationship between EVM and SNR has impact on the design of the RX chain. We now concentrate on the RX section in Figure 2.1 and analyze its influence on the SNR of the link. Therefore, the goal of this section is to introduce concepts that influence the gain, noise figure and linearity performance of the RX chain.

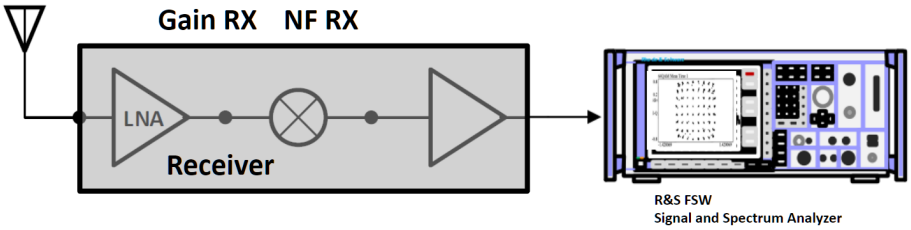


Figure 2.3: Conventional down-converting receiver chain

The first concept to be discussed is the conventional receiver chain as shown in Figure 2.3. Each stage is again described from left to right, including the antenna, low noise amplifier (LNA), filtering, buffering and an ADC or network analyzer.

- The role of the **LNA** is to amplify the relatively low input RF powers and minimize the added generated noise of latter stages according to Friis' formula [13].
- The **Mixer** translates the signal to a lower frequency, to lower the speed requirements of the following stages.
- The **IF amplifier** can be implemented using Automatic Gain Control (AGC) for increasing the dynamic range of the receiver chain.

To evaluate the quality of the link, each component in the chain are attributed three performance parameters: Gain, Noise Figure and Linearity. Linearity is represented using the Third-Order-Intercept point, which will be treated for a mixer in a following section. The performance of the entire receiver in terms of noise figure and gain can be evaluated using Friis equation.

$$NF_{tot} = 1 + (NF_{LNA} - 1) + \frac{NF_{Mixer} - 1}{A_{LNA}} + \frac{NF_{AMP} - 1}{A_{LNA} A_{Mixer}} \tag{2.4}$$

The linearity of the receiver chain in terms of IP3 is expressed as:

$$\frac{1}{A_{IP3}^2} = \frac{1}{A_{IP3,LNA}^2} + \frac{\alpha_{LNA}^2}{A_{IP3,Mixer}^2} + \frac{\alpha_{LNA}^2 \beta_{Mixer}^2}{A_{IP3,AMP}^2} \tag{2.5}$$

In addition to general system specifications, the effect of cascaded noise and linearity effect is taken into account when constructing the link budget. The specific receiver architecture requires an introduction into frequency planning and will be introduced next.

Homo/Hetero-dyne receivers

Two main receiver architectures can be distinguished to demodulate the RF signal. The heterodyne receiver first translates the signal to an Intermediate Frequency (IF) and eventually to baseband using two down converting stages. The problem of this topology is the image frequency, desensitizing the wanted signal if a blocker is present or causing increased noise figure at the IF due to the presence of noise at the image which folds back to the IF. With no image rejection in place this will result in a 3 dB increase of noise figure. The influence of the image frequency on the noise figure of a two-stage RX chain is expressed by eq. 2.6 from [14].

$$F_{total} = F_{1R} + F_{1I}\frac{G_{1I}G_{2I}}{G_{1R}G_{2R}} + \frac{F_{2R} - 1 - \frac{G_{2I}}{G_{2R}}}{G_{1R}} \tag{2.6}$$

With the subscripts $1/2$ denoting the stage and I/R denoting the Image or RF signal. Taking the image gain of the mixer to zero $G_{2I} = 0$, results in the standard Friis equation 2.4. When no image suppression is applied we have $G_{1I} = G_{1R}$, $G_{2I} = G_{2R}$,$F_{1I} = F_{1R}$ and the expression reduces to eq. 2.7.

$$F_{total} = 2F_{1R} + \frac{F_{2R} - 2}{G_{1R}} \tag{2.7}$$

The influence of gain stages before the mixer on image suppression is shown in 2.6. For a noiseless mixer the minimum single sideband noise figure is 3 dB, we have for eq. 2.7 $F_{2R} = 2$ and the total noise including image noise folding onto the IF is increased by 3dB.

The homodyne receiver employs a single down converting stage and directly output the wanted I and Q signals. This is known as the IQ-demodulator or the image rejection mixer. This implementation eliminates the afore mentioned increased noise figure by the image frequency and additionally provides blocker suppression. However, two main reasons are formulated why the preference of this work is the homodyne receiver topology.

First of all, demodulating the IQ to baseband at the sensing node requires a high-speed DAC. Achieving Nyquist rates for 1200 MHz signals, requires power intensive DACs at the nodes which are considered not feasible. Processing large bandwidth signals outside of the antenna is the preferred method in this work. Another option is to feed the I and Q baseband signals out of the antenna dome. However, this requires identical coax lines to ensure the IQ imbalance is minimal. Secondly, demodulating at the sensing node requires receiver phase recovery circuitry. Errors in the angular accuracy of the carrier recovery denoted by θ_e result in crosstalk between the I and Q signals. An elaborate discussion on error terms for IQ-demodulators is described in [15].

To conclude, two main reasons were mentioned on the disadvantages of the homodyne receiver topology with regard to the antenna dome. Therefore, this work focuses on the heterodyne principle taking into account the noise folding of the image frequencies. No interferers are assumed since the measurements are performed in a controlled environment. However, care must be taken if the image generated by the mixer is reflected at the antenna and is again mixed to the desired IF.

Next, the link budget for the proposed system will be discussed in depth.

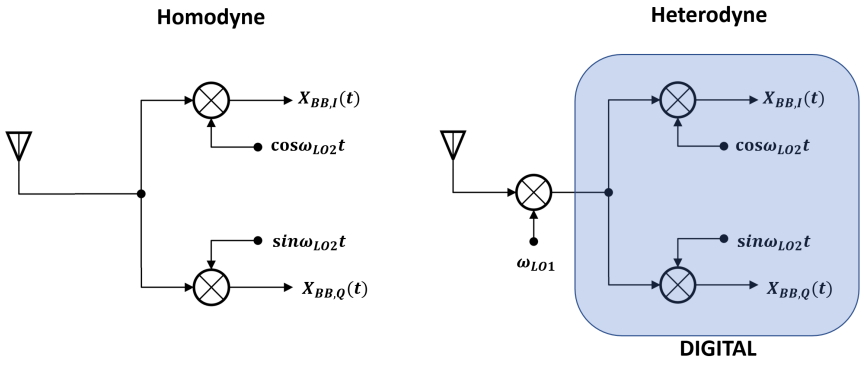


Figure 2.4: Homodyne and Heterodyne I/Q Receiver Architectures considered for the ADome

2.1.3. Link budget

The gain, noise figure and linearity requirements are specified by treating the RX chain as a black box. A link budget is used to determine the influence of the individual components, contributing to gains, losses and noise figure. An overview of expected losses and gains from TX to RX is represented in Figure 2.5.

UE Parameters	3GPP TS 38.101
Min peak EIRP	20.6 dBm
Max EIRP	43 dBm
Min EIRP for EVM	-13 dBm

Table 2.2: The 3GPP 5G NR specified power levels [1] Table 6.2.1.0

The 3GPP standard sets specifications in terms of output power levels for the transmitting device. A distinction is made between four power classes in the User Equipment (UE) category. Among these are Fixed wireless access (1), Vehicular(2), Handheld (3) and High power non-handheld (4). Table 2.2 indicate UE output powers expected to be tested in the ADome system. In state of the art literature a range between 35 and 55 dBm EIRP for phased array antennas was found [9]. The work presented in [4] reports an EIRP of 54 dBm, requiring a far-field distance of 1.84m. In this work we assume a maximum EIRP 43 dBm as specified by the standard. In addition to the expected path losses this creates an overview of the expected powers of the TX.

Path Loss	24 GHz	40 GHz
0.5m	54 dB	59 dB
2.0m	66 dB	71 dB

Table 2.3: Path losses with corresponding distances

Table 2.3 shows the expected path losses for two dome sizes, namely 0.5 and 2 meters. Additionally the lower and upper extreme of the FR-2 band are also included. This shows the expected range of path losses due to dome size and operating frequency for the receiver chain.

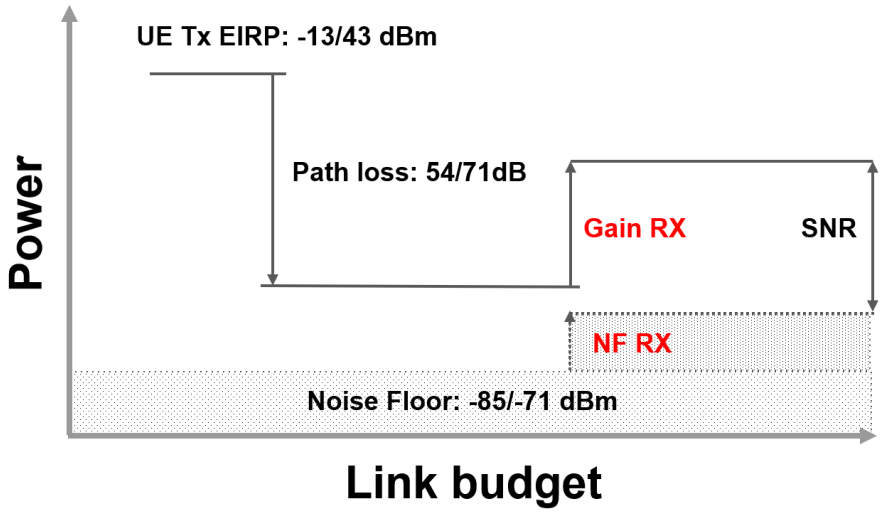


Figure 2.5: Conventional down-converting receiver chain

To conclude, a graphical representation of the previously found values are shown in Figure 2.5. The specifications sets a range for minimum and maximum power (EIRP) transmitted. Additionally, the dome size and operating frequency sets the expected path loss. The next section will investigate the impact of the proposed mixer on the link budget.

The previous developed link budget is a simplified illustration of the power flow through the chain. The receiver can be considered as a single block, with Gain and Noise Figure specifications. In this part we specify these two figures and implement the necessary components to meet the SNR requirements. The Noise Figure allowed for the entire receiver chain is determined using the following relation [10].

$$SNR(dB) = P_{RX}(dBm) - (10log_{10}(kT_0B + NF) \tag{2.8}$$

With P_{RX} the received power in dBm, kT the thermal noise set by the Boltzmann constant and the temperature, the signal bandwidth B and the minimum SNR (SNR_{min}). The thermal noise of the receiver is set to room temperature resulting in $-174dBm/Hz$. The minimum SNR required, is set by the used modulation described in the Table 2.1.

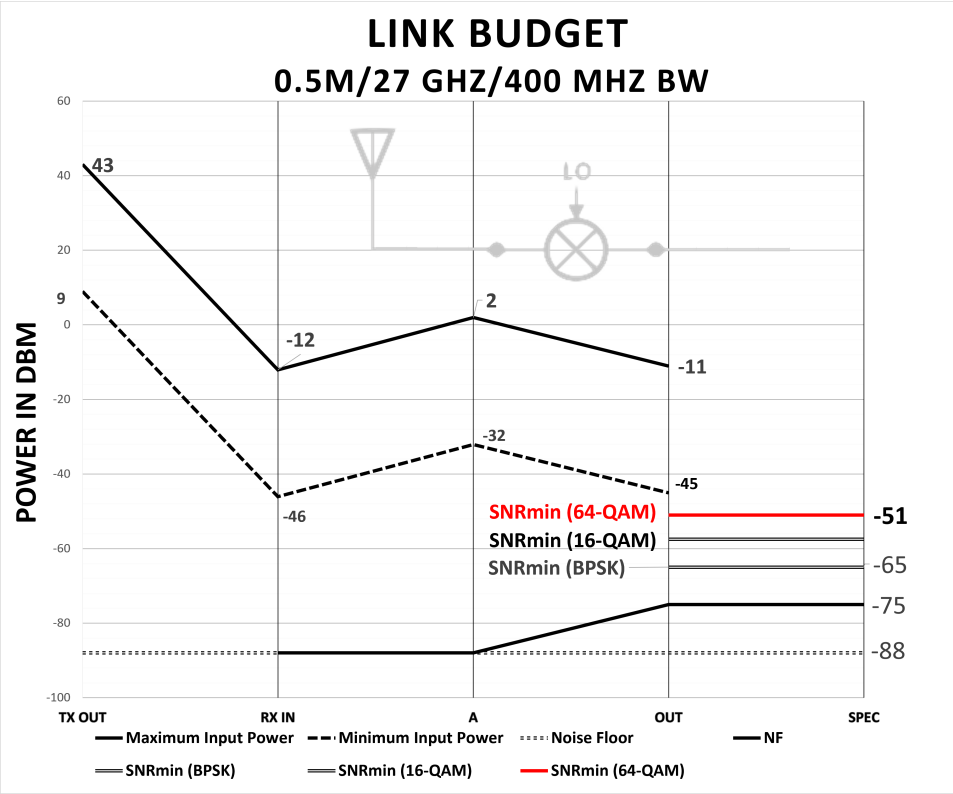


Figure 2.6: Link-budget implemented for an antenna and mixer receiver chain. Considering a signal bandwidth of 400 MHz and a path loss corresponding to a distance to 0.5m at 27 GHz. The RX antenna provides 13.5 dB of gain whilst the mixer introduces 12 dB conversion loss and 12 dB NF. The minimum SNR levels on the right-hand side are based on the EVM percentage values specified in the standard and analyzed in 2.1.

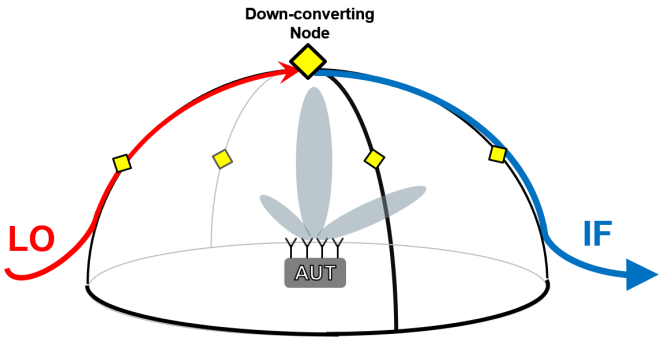
In this work a passive mixer-only implementation topology is pursued. We take as a reference the HMC774A mixer and analyze the performance in the link budget. At 27 GHz with 400 MHz BW the mixer is able to meet the following performance based on maximum and minimum EIRP. As shown in 2.6, a maximum EIRP of 43 dBm from Table 2.2 results in 1 dBm at the input of the mixer. A minimum EIRP of 9 dBm meets the SNR_{min} requirements for a 64-QAM signal. Worth noting is the noise added by the signal analyzer. For example the R&S FSW analyzer having a typical DANL of -169 dBm adding $(DANL - (10log_{10}(kT))) = 5dB$ noise figure to the link. Additionally, cable losses ranging from 1-3 dB need to be taken into account, and image noise folding of 3dB. Therefore, the minimum EIRP for 64-QAM demodulation is expected around 9 dBm, including 6 dB headroom. Simulations are performed on this matter and are discussed in Section 4.2.

2.2. Local Oscillator Distribution

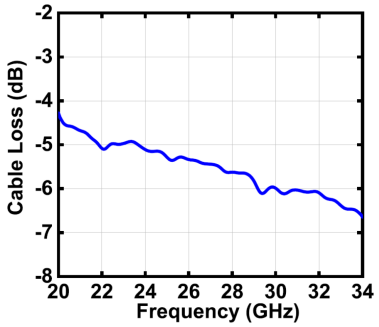
In the previous section, using a detailed link analysis tuned to the specific case of the Antenna Dome we have identified that a mixer-first receiver can be used to succesfully characterize 5G AUTs. While the conventional nodes in the ADome work as a scalar detector, thus not requiring any high frequency distribution, the EVM sensing node will need to receive an LO signal to realize the frequency translation. From a system prospective it is useful to elaborate on the way this LO distribution, to the (few) EVM sensing nodes scattered over the Dome skeleton, is performed.

One of the main issues of high frequency measurements are the power losses. For example, the calibration challenges shown in Figure 2.7b show the cable losses in the frequency range of interest. A dome with a radius of $r = 0.5m$ with a sensing node placed on the broadside requires a minimum cable length of $0.8m$ to reach the node in the dome. Also, the distance from the generator to the dome needs to be accounted for which resulting in cable lengths between 1-2m.

The second factor part of this analysis, is the cost of the implementation. The idea is to implement five sensing nodes, one placed on the broadside and the other four equally spaced from each other lower on the dome. Each sensing node requiring a high frequency LO for down-conversion.



(a) Illustration on the implementation of several down-converting nodes for the ADome system.



(b) Calibration challenges for a 21-33 GHz carrier aggregration EVM measurement in [16]. Figure extracted from the paper representing measurement cable losses

Figure 2.7: Considerations for the LO distribution for the ADome

2.2.1. Case Studies

Three implementations are considered for supplying the high frequency LO signal to the mixer block. The approach is similar to the method presented in [17] for mm-wave receivers, since similar factors are to be accounted for. Two extremes are described which include internal generation and external generation of the LO signal. The third case is considered a hybrid variant of the extremes. All of the cases account for mainly two factors, power budget, cost and complexity of the implementation. This section is concluded by a discussion the three cases and a preferred form of implementation.

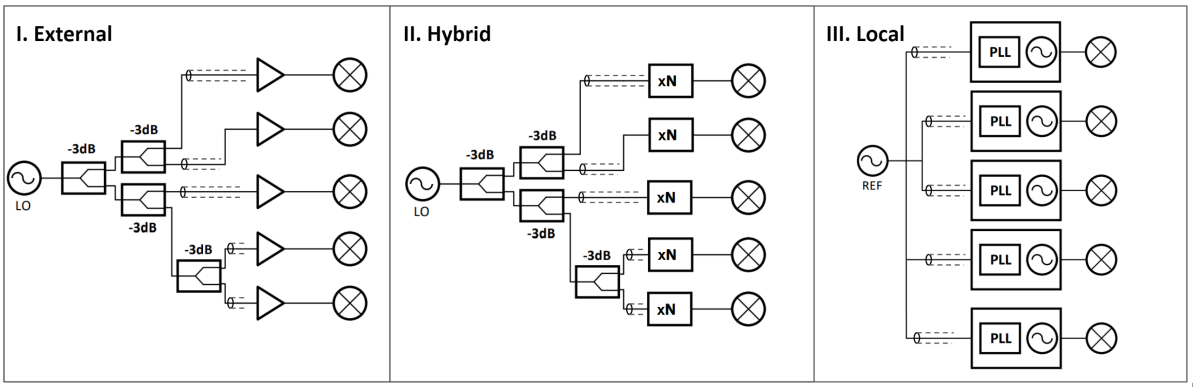


Figure 2.8: Three LO distribution implementations: I: External generation, II: Hybrid generation, III: Internal generation.

For each implementation **I.**,**II.** and **III.** a brief summary and case are described.

- I. External generation: The high-frequency LO signal is distributed from outside of the measurement setup. A signal generator with frequency generation capabilities up to 40 GHz is needed using this implementation. The phase noise performance of the generator is $\mathscr{L}_{Gen}(100kHz) = -98dBc/Hz$ and $\mathscr{L}_{Gen}(100kHz) = -108dBc/Hz$ between 20 - 40 GHz depending on the configuration. The LO signal is then applied to a power divider, splitting the power to the several downconverting nodes. This is implemented using 4 splitters as shown in Figure 2.8. This will result in an decrease in power per node, the buffers can provide 20 dB of gain between 24GHz and 40GHz with a maximum output power of 14 dBm.

Case I.	**Component**	**Specification**	**Pout**	**Gain**	**Amount**	**Unit Price**	**Total**
Signal Generator	Keysight E8257D	24 GHz - 40 GHz	15 dBm	-	**1**		
Splitter	EP2KA+	1.5dB excess loss	1.5dBm	-13.5dB	4	$30	$120
Buffer	HMC-AUH256	(17.5G-41G)	19dBm	+17.5dB	5	~90$	$450
Coax	RF-COAX	fmax 40G	15dBm	-4dB	5	$300	$1500
TOTAL			**14dBm**		**9**		**$2370**

Table 2.4: Case 1: External generation implementation using off-the-shelf components

- II. Hybrid generation: With a 2x multiplier at the sensing node, a frequency between 12-20 GHz is distributed by the signal generator. The phase noise performance of the generator is $\mathscr{L}_{Gen}(100kHz) = -104dBc/Hz$ and $\mathscr{L}_{Gen}(100kHz) = -145dBc/Hz$ between 10 - 20 GHz depending on the configuration. First of all, the signal generator is able a higher output power at lower frequencies. Also, the excess loss of the splitter is 0.8 dB, which is 0.7 dB lower compared with the previous case. Coax cables losses are typically lower.

Case II.	**Component**	**Spec.**	**Pout**	**Gain**	**Amount**	**Unit price**	**Total**
Signal generator	Keysight E8257D	@(12G-20G)	21dBm (max)		1	-	-
Splitter	EP2KA+	0.8dB excess loss	9.6dBm	-11.4dB	4	$30	$120
Coax	RF-COAX	fmax 20G	3.6dBm	-3dB	5	$150	$750
Multiplier	HMC598	active x2 Pin: 0 to 6dBm;	15 dBm	+15dB	5	$40	$200
TOTAL			**15 dBm**		**15**		**$1060**

Table 2.5: Case 2: Hybrid generation implementation using off-the-shelf components

- III. Internal generation: The high-frequency signal is generated at the node locally. This requires voltage controlled oscillators (VCO) and phase-locked-loops (PLL) to achieve a stable frequency. The datasheet of the PLL reports a phase noise performance of $\mathscr{L}_{Gen}(100kHz) = -100dBc/Hz$ at 24 GHz. The main advantage of the PLL is the local generation on the sensing node. However, the output power of the ADF4371 of -7dBm is low for driving a mixer and can be compensated using buffers e.g. CMD275P4, chosen for its low phase noise performance.

Implementation III.	**Component**	**Spec.**	**Pout**	**Gain**	**Amount**	**Unit price**	**Total**
VCO+PLL	ADF4371	(62.5M - 32G)	-7 dBm	-	5	$275	$1375
Reference	100MHz XCO	100MHz	-	-	5	$2	$10
Buffer	CMD275P4	(DC-26.5G)	3dBm	10dB	5	~150$	$750
Multiplier	HMC598	active x2 Pin: 0 to 6dBm;	Pout:15 dBm	5dB	5	$40	$200
TOTAL			**15dBm**		**12**		**$2335**

Table 2.6: Case 1: Local generation implementation using off-the-shelf components

All three implementation result in roughly the same output power for driving the LO port of the mixer. This value is set as a design specifications for the design of the mixer. The implementations differ the most in cost. Implementation (I) requires an high frequency signal generator and high frequency cables, which are costly for low-loss performance. The cost of implementation (III) is dominated by the PLL with integrated VCOs, a drawback of this implementation is the need for a multiplier, degrading the phase noise performance. Implementation (II) is preferred using frequency multipliers and relatively lower cost and lower loss cables. The next section will discuss a specific implementation and its considerations.

2.2.2. LO distribution

After determining an application specific RX chain for the ADome, the implementation of distributing the LO signal to the mixer needs to be addressed. From the case studies on LO distribution, the Hybrid implementation (II) is preferred due to cost, power-loss and implementation trade-offs. The multiplication factor of the node is chosen according to component availability. In this case for multiplying up to 40GHz, the *HMC598* Active Multiplier is used to generate the required LO frequencies for downconversion. The off-the-shelf multiplier datasheet reveals an three stage implementation of the multiplier. It consists of an input buffer stage, a 2x multiplying stage and an output buffer.
The input power of the multiplier for optimal performance is specified between -2 to 6 dBm. An LO signal generator with output power of 15 dBm including 20 GHz cable losses will suffice. The active multiplier provides gain, to achieve a maximum output power of 15 dBm. The specified output power is able to drive a passive mixer.

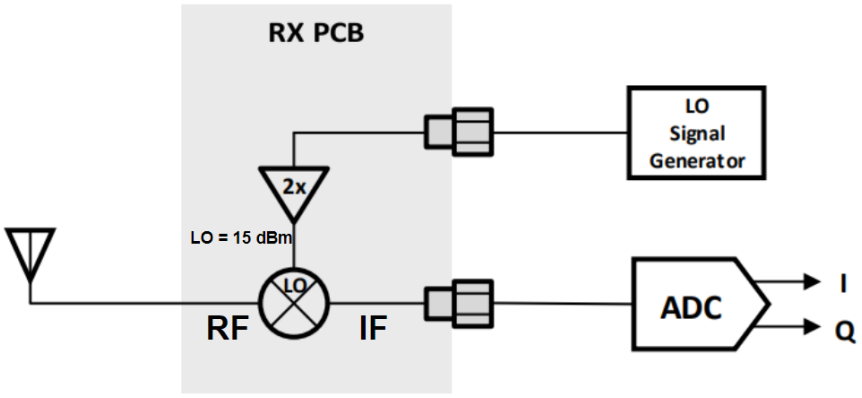


Figure 2.9: LO distribution components

A block diagram of the preferred implementation is shown in Figure 2.9, excluding bias networks. The antenna is connected to the mixer and the IF output of the mixer is connected to an ADC by an coax cable. The LO signal is generated between 12-20 GHz at the signal generator and distributed to the node using a coax cable up to 20 GHz. The implementation would benefit in terms of losses with a higher multiplication factor of the multiplier. However, due to component availability this was not an option. An overview of the components relevant parameters is given in the table below.

HMC598 Active Multiplier		
	Input RF Range	**11 - 23 GHz**
	Input Drive	**0 to 6 dBm**
	LO output power	**15 dBm**
HMC774A Mixer		
	Frequency Range (RF)	**22-40 GHz**
	Conversion gain	**-13 dB**
	Noise Figure	**<13 dB**
	P1dB	**12 dB**
	IIP3/IIP2	**20dBm/40dBm**

The HMC774A mixer is an off-the-shelf double-balanced passive mixer used in the link budget to compare the achievable performance of the down-converting node. The Conversion gain and Noise Figure specifications are typical values but vary across input RF range. The linearity specifications P1dB and IIP3/IIP2 are conform the performance of a passive mixer.

2.3. Influence of LO Noise

The link analysis developed until now assumed an ideal LO signal supplied to the mixer. In reality, the LO adds amplitude and phase noise to the overall system noise figure. The AM noise in the upper and lower band mix with the LO and convert to the IF. The PM noise is transferred directly from the LO to IF with the same relative level in dBc/Hz [14]. In this section we study the effects of the proposed implementation using a single mixer and an active multiplier.

2.3.1. LO AM noise

The effect of the LO AM noise on the mixer noise figure is two-fold. The first one arises from the sidebands and will be denoted as $N_{LORF,AM}$ in eq.2.9.

$$N_{LORF,AM} = \frac{G_{LO}F_{LO}}{G_{1-2R}}\left(\frac{(G_{2R}G_{LR})_{LSB}}{2} + \frac{(G_{2R}G_{LR})_{USB}}{2}\right) \tag{2.9}$$

From this expression the influence of the receiver chain and isolation of the mixer are derived. The cumulative gain and noise figure of the LO chain G_{LO} and F_{LO} are suppressed by stages before and include the mixer gain G_{1-2R}. Additionally, the LO-RF isolation of the mixer G_{LR} further suppresses the effect of the LO AM Noise added to the mixer noise figure. The factor G_{2R} is the conversion gain of the mixer, which attenuates the LO AM noise in case of conversion losses.

Another contribution is the LO AM noise directly appearing at the IF port $N_{LOIF,AM} = \frac{G_{LO}F_{LO}G_{LI}}{G1-2R}$. Combining the two expressions result in a general expression for the noise figure increase due to LO AM noise. This is shown in eq. 2.10

$$N_{LO,AM} = \frac{G_{LO}F_{LO}}{G_{1-2R}}\left(\frac{(G_{2R}G_{LR})_{LSB}}{2} + \frac{(G_{2R}G_{LR})_{USB}}{2}\right) + \frac{G_{LO}F_{LO}G_{LI}}{G_{1-2R}} \tag{2.10}$$

2.3.2. LO PM noise

Phase noise is expressed relative to the carrier at a certain offset in dBc/Hz at an offset frequency f_m in Hz. The phase noise directly adds to the noise figure at a specific frequency. It is important to choose the IF at a frequency where the thermal noise dominates instead of the phase noise, largely deteriorating the SNR of the system. In system phase noise analysis it is important to identify the contributions of each component in the chain and minimize its influence to achieve the specification, as follows.

We analyze the proposed implementation using the signal generator and active multiplier on phase noise performance. The E8257D is available in multiple options with respect to phase noise performance according to the datasheet. In this example, we use for the signal generator a particular option with a specified phase noise of $\mathscr{L}_{Gen}(100kHz) = -104dBc/Hz$. The multiplication factor of the multiplier with $M = 2$ adds $20 * log(M)$ dB to the generator phase noise, resulting in $\mathscr{L}_{Gen}(100kHz) = -98dBc/Hz$. Taking for the the SSB phase noise of an active multiplier $\mathscr{L}_{Mult}(100kHz) = -128dBc/Hz$. From this comparison we can conclude the signal generator is limiting the phase noise performance. To ensure the thermal noise dominates in the band of interest we either increase the IF, or increase phase noise performance of the generator to improve the SNR.

2.4. Mixer Fundamentals

In this section the mathematical nature of mixing is discussed which is the basis of down converting a signal. The next section describe performance parameters on which mixers can be evaluated. Then, an overview of existing mixer topologies are given and their trade-offs are discussed.

Before a mathematical description of the mixing process is developed, we investigate the matter using illustrations. The mixing process is illustrated best in the frequency-domain. Considering the frequency of interest at ω_{RF} and a second frequency the Local Oscillator at ω_{LO}. Applying these separate frequencies components to the mixer will result in a frequency translation of the desired signal ω_{RF} to a higher and lower frequency. These resulting frequencies are called the Intermediate Frequencies (IF) and are either sum or the difference between the RF and LO frequencies.

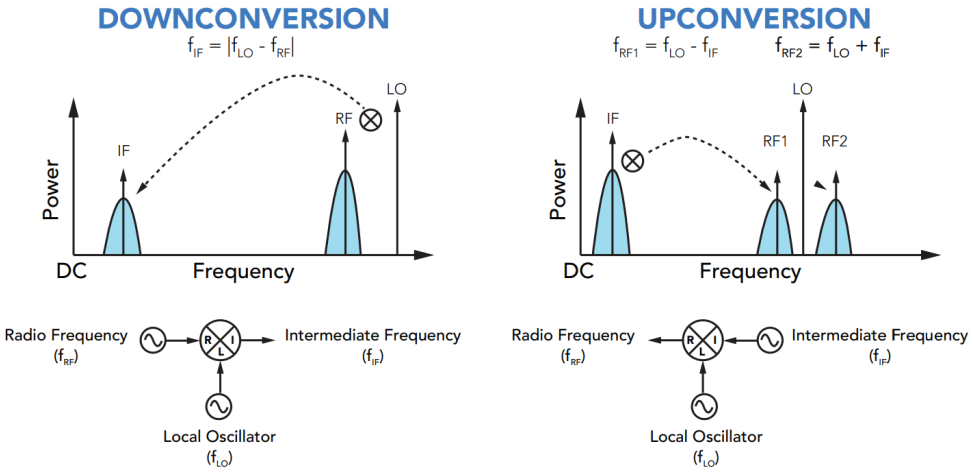


Figure 2.10: Upconverting and downconverting mixer operation figure retrieved from [18]

Figure 2.10 illustrates the mixing concept. The mixer is illustrated as a three terminal device, with two inputs and an output. For a down converting mixer the RF and LO signals are regarded as the input, whilst the IF is the output. The frequency of interest is located at the difference between the RF and LO frequencies.

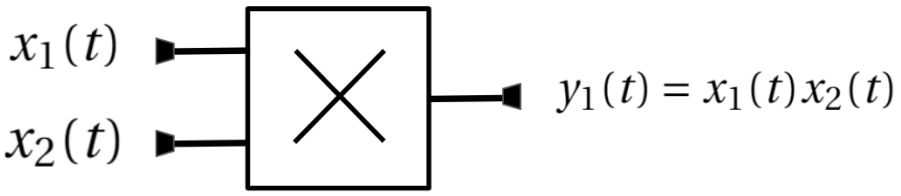


Figure 2.11: Block diagram of a multiplier with inputs x_1 and x_2 resulting in the output y_1

The mixing operation is performed by the multiplication of two signals, using $x_1(t) = A_1 cos(\omega_1)$ and $x_2(t) = A_2 cos(\omega_2)$. We can write the multiplication as:

$$y_1(t) = x_1(t)x_2(t) = A_1 cos(\omega_1) A_2 cos(\omega_2) = \frac{1}{2}[cos(\omega_1 - \omega_2) + cos(\omega_1 + \omega_2)] \tag{2.11}$$

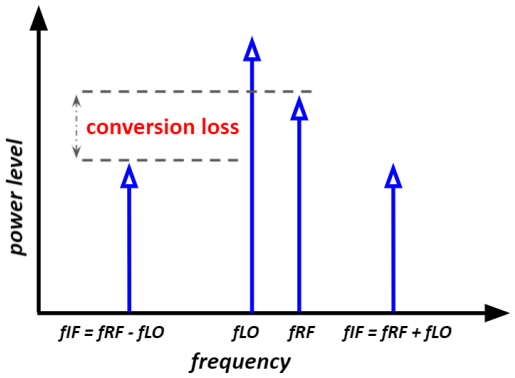
The sum and difference frequencies arise when the trigonometric identities are applied for multiplying two cosines with non-equal arguments: $cosAcosB = cos(A-B) + cos(A+B)$.

2.4.1. Mixer Figure of Merits

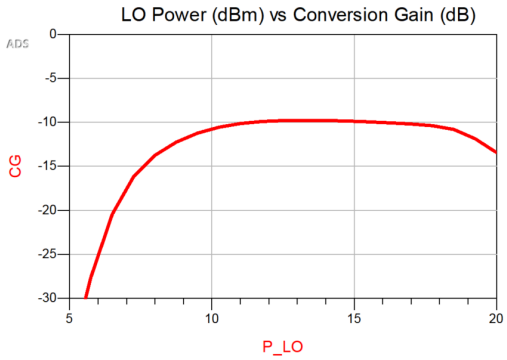
Now that the mixing concept has been introduced, it is needed to develop parameters which determine how well suited a given mixer topology is for a certain application. The performance of a mixer is expressed in four main concepts. The conversion gain describes the efficiency of translating the input frequency to a desired frequency. The noise figure parameter expresses the noise added by the mixer to the chain. Port isolation describe the signal feedthrough between the ports. Lastly, linearity describe the tolerance of the mixer to large signals. Each concept will be discussed on the impact it has on the system and its relationship to mixer design based on [18].

Conversion gain

The mixing operation ideally generates the sum and difference frequency components, as shown in 2.12a. For a downconverter, the intermediate frequency (IF) component is considered the difference between the RF and LO frequencies. The ratio between the input RF and output IF power is the conversion efficiency. A IF power lower than the input RF results in a conversion loss which is normal for passive mixers. Active mixers provide gain and can therefore gain the IF product, resulting in conversion gain.



(a) Frequency spectrum illustrating the conversion loss between the input f_{RF} and down-converted output f_{IF}



(b) Simulating conversion loss versus LO power of a single ideal diode

Figure 2.12: The concept of conversion gain illustrated in the frequency spectrum and the influence of the LO drive.

$$Conversion\ gain|_{dB} = 10log_{10}(\frac{P_{IF}}{P_{RF}}) \tag{2.12}$$

Conversion efficiency directly impacts the system link budget and therefore the signal quality at the output of the system. The required SNR and DR at the output of the mixer for detecting the specified modulation schemes in Section 2.1.1 is achieved by choosing the appropriate mixing device and topology.

The conversion gain performance is often plotted against LO pumping power for optimal performance of the mixer as shown in Figure 2.12b. Another method of evaluating the conversion gain is versus RF frequency, for a wideband mixer the conversion gain is ideally constant over the specified frequency range. The frequency selectivity of mixers is mainly determined by the use of hybrids or baluns for driving the mixing devices.

Noise Figure

Noise in a signal chain can be referred to the in- and output, since a two-port in the chain provides signal gain and loss. The noise figure (NF) metric is the ratio between the in and output SNR.

$$NF = \frac{SNR_{in}}{SNR_{out}} \tag{2.13}$$

Two definitions for mixer noise figure are used, *Double Side-Band* (DSB) and *Single Side-Band* (SSB) Noise Figure. The DSB NF is half the power of the SSB NF.

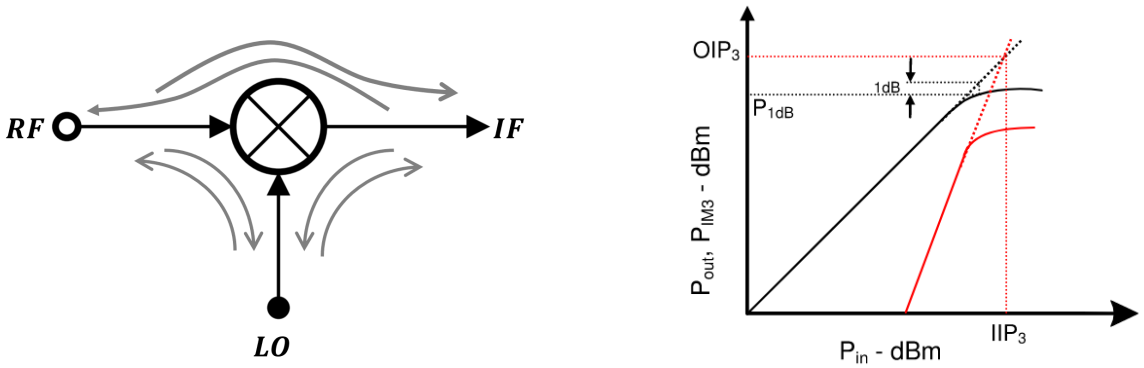
Assuming an ideal noiseless mixer, the following relation holds:

$$NF_{DSB} = 0dB \tag{2.14}$$

$$NF_{SSB} = 3dB \tag{2.15}$$

Implementing the noise figure in the link budget gives a clear overview of the added noise by the component in the chain. Noise performance directly impacts the system link budget and therefore the signal quality at the output of the system.

Noise sources in passive mixers originate from thermal and shot -noise. The former due to losses in the circuit modeled by resistances, which are part of non-ideal reactive components, interconnects and the losses in a nonlinear device. Lastly, shot noise is caused by energy changes in carriers when crossing a junction. This phemomena occurs in semiconductor components such as diodes, BJTs and FETs.



(a) Port feedthrough between mixer ports:[13]

(b) Intermodulation and compression [19]

Figure 2.13: Illustrations of port isolation and linearity concepts of a mixer.

Port Isolation

Port isolation or coupling is defined as the amount of power that leaks from one port to another. Generally three cases of port isolation are defined for a mixer: LO-to-RF, LO-to-IF and RF-to-IF. Isolation is improved by balanced topologies or the use of hybrids junctions. Typical values reported [18] are in the range of 20-30 dB of isolation.

The LO-to-RF isolation has impact on the signal to noise ratio of the system as was shown in the analysis of LO phase noise. Interference caused by poor LO-RF isolation on other components of the circuit, such as the antenna of amplifier could be problematic. The LO-IF isolation has impact on the RF signal path in terms of LO phase noise directly appearing at the IF output. Additionally, a large LO signal on the IF line can also desensitize following stages. For downconverters this issue is solved by implementing a balanced topology using hybrids or by filtering the high frequency LO. The latter requires an LO much larger than the IF, to obtain the required attenuation. The RF-IF isolation is the isolation of the RF signal leaking to the IF port. The RF and IF are considered small-signal compared with the LO and are therefore less of a problem. However, it can indicate the balance of the mixer, resulting in low conversion losses.

Gain compression

Nonlinear devices operate at a certain bias point and can be approximated by a linear function. Input levels exceeding the small-signal behaviour, shift the operating point away from the linear approximation. In active RF applications providing gain this is defined as gain compression. The input level at which the gain deviates 1 dB from the linear approximation is named the 1-dB compression point P_{1dB}. This metric is used to specify largest input RF power level the circuit is able tolerate. When the mixer enters into compression, this causes higher conversion loss and intermodulation tones. This will in turn degrade the SNR of the system. The P_{1dB} is typically 4-7 dB below the LO drive of the mixer. Compression of the mixer can be improved by using higher turn on diodes.

Intermodulation

Another source of nonlinearity is intermodulation. This effect can be analyzed by two-tone excitation of the system, the concept is shown in 2.14 for low-side LO injection. Figure 2.13b shows input-output characteristic for a non-linear system. The black line represents the fundamental component, compressing for larger input powers. The red line represents the power of the intermodulation component. The intersection of the fundamental and IM3 component is called the Intermodulation Intercept Point (IIP). The IMD3 component is considered the most dominating component and is defined as the third order intercept point (TOI). A high TOI refers to a highly linear device.

Typical $IIP3$ levels occur above the LO drive level, however this is dependent on the mixer type and topology. High performance passive mixers designed to operate as switching mixers often have superior IIP3 performance between 20 - 30 dBm.

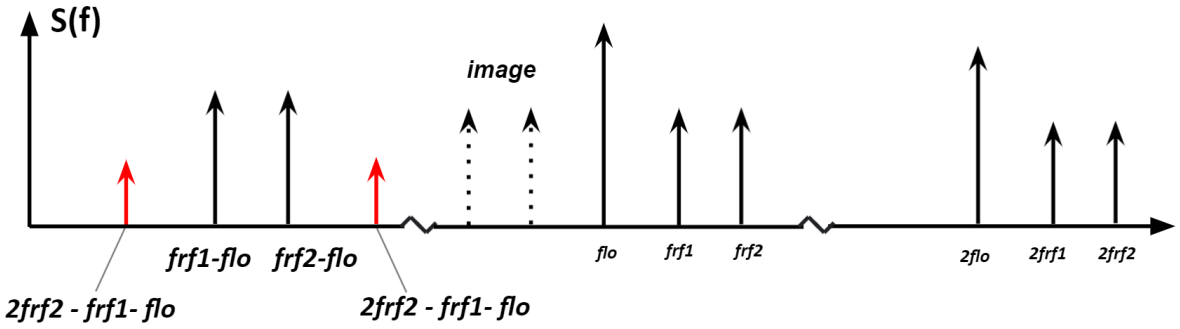


Figure 2.14: Low-side LO injection and frequency components of interest for determining the third-order intercept point. Red arrows are the 3rd order IMD products.

2.4.2. Mixer topology considerations

The introduction to the system and mixer concepts described in the previous section, provide the necessary background to evaluate existing mixer topologies. Three main points are considered important for the implementation of the down-converting nodes. Firstly, the number of sensing nodes is considered limited due to the large signal bandwidth demodulation requirements mentioned in 1 and the according ADC requirements. Secondly, to span the entire FR-2 band, the node requires wide-band performance in terms of conversion losses and noise figure. Lastly, the link budget between the TX and RX determine the EVM performance of the TX signal quality measurement which is treated in Section 2.1.3. Figure 2.7a shows an illustration of the dome with 5 down-converter nodes for measuring the signal quality of the AUT.

A multitude of mixer topologies is reported in literature in the frequency band of interest. A well-known topology is the active Gilbert Cell mixer. A folded double-balanced variant in 28nm CMOS operating at 33 GHz has been reported in [20]. The achieved performance is a CG of -12 dB and a NF of 11 dB. The implemented balun mainly influenced the difference between simulated and measurement results, for example a simulated CG of -10dB and measured at -16dB at an IF of 10 GHz. A comparison between the performance of CMOS and SiGe double-balanced Gilbert mixers is made in [21], the SiGe technology with an $f_T = 200GHz$ achieves a CG of $10.5dB$ and a $NF_{DSB} = 4.7dB$. However the linearity of the mixer is limited by achieving a $P_{1dB} = -7.2dBm$ and an $IIP3 = -0.8dBm$, similar performance is found in [22], which is compared in Table 2.7 to the passive mixers discussed next..

The analysis on the link budget in section 2.1.3 allows for implementation of a passive mixer-only in terms for a range of expected EIRP levels and noise figure. The passive resistive topology used in mostly CMOS, where the device functions as a switch is less favourable to be implemented using HBT devices. Therefore this work narrows its scope to passive diode implementations using the HBT as a diode-connected device.

Parameter	Bao '20 [22]	Simulation	Issakov '10 [23]	Zhongpu '15 [24]	**Design goals**
Technology	CMOS HLMC 40nm	-	SiGe:C	-	**SiGe:C** $250um$
Device	CMOS	Diode	HBT	Diode	**HBT**
Topology	Double Balanced Gilbert Cell with DCI	Single Diode	Single-balanced	Double-balanced	**Single-balanced**
frf (GHz)	24-30	26	22-39	25-40	**24-40**
fif (GHz)	1	1	0.1	DC - 5	**1**
CG (dB)	16	-9	-8	-9	**>-12 dB**
NF	9.65	12	>10 dB	9	**<12 dB**
Pin,1dB	-11	9	-1.5	11	**>0 dBm**
IIP3 (dBm)	-	17	8.8	-	**>5**
LO (dBm)	-4	15	3	>10	**15**

Table 2.7: Performance comparison of an active and three passive diode mixers. Simulation results of the single-diode was found [25] and verified with simulations in ADS.

Table 2.7 gives an overview of three passive diode topologies and an active mixer topology. From this literature search design goals have been formulated and the single-balanced passive diode technology will be analyzed in-depth in the following section.

2.4.3. Single-Balanced Diode Mixer

The single-balanced topology is first analyzed by orienting the diodes as shown in Figure 2.15. The orientation of the diodes must be opposite as is determined by analyzing the conductance waveforms through the diode, as in [19] and [26]. To analyze this more in-depth we consider the case when the RF is applied to out-of-phase and the LO in-phase. The diodes are pumped out-of-phase due to the LO, whilst the RF voltage is also applied out-of-phase. This results in the IF appearing in-phase at the output. This concept is illustrated in Figure 2.15 by the arrows. The same mode of operation holds when the roles of the RF and LO are reversed.

Orienting the diodes in the same direction, for example the cathodes connecting to the hybrid, requires an hybrid at the IF since the IF appears out-of-phase. Additionally, connecting two diodes in the same orientation result in a non-balanced structure, causing the circuit not to reject LO noise or spurious responses [25].

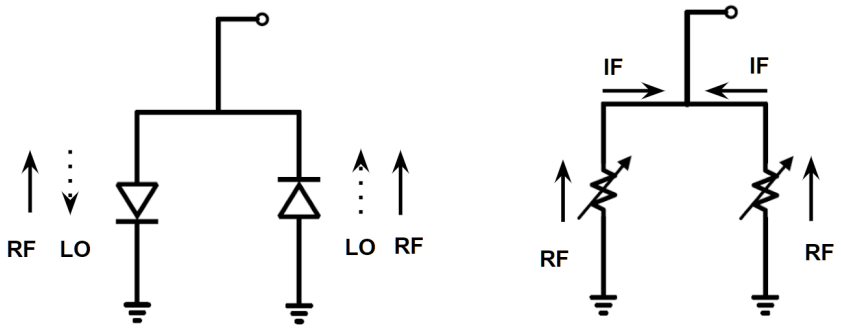


Figure 2.15: Diode orientation for the Single-Balanced Mixer [25] [26]

Balanced diode mixers are found to be implemented using Schottky diodes due to their fast switching characteristics. Unfortunately, no Schottky diodes are available in the provided technology. However, the technology does provide access to high performance heterojunction bipolar transistors (HBT). For this reason, the HBTs are diode-connected to function as mixing devices.

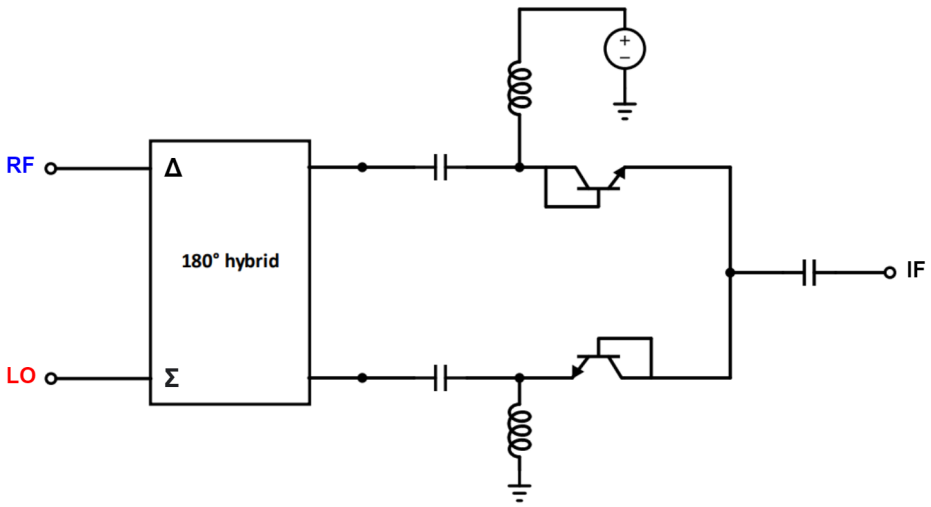


Figure 2.16: Passive Single-Balanced mixer concept

Now that the role of the mixing devices are known the rest of the circuit shown in 2.16 is explained. The capacitors function as DC blocking capacitors. The DC voltage source provide bias and the corresponding inductors close to the device ensure a DC current to flow through the device. If no DC path is available through the diodes, the mixer will not work [27]. Lastly, the 180-degree hybrid combines the RF and LO signal to be applied to the mixing devices as was discussed previously.

The advantages of the single-balanced topology with respect to the single diode implementation are [25]:

1. Isolation between the LO and RF/IF port, 2. Rejection of spurious responses, 3. Suppression of LO noise and spurious signals and minimization of filters . Drawbacks of the topology are decreased conversion performance and larger required LO drive power. Additionally, due to a single balanced structure only a single port (RF or LO) is isolated at the IF.

It was shown in Chapter 2 that the single-balanced topology has shown favourable performance for the ADome application. However, implementing the 180°-hybrid using a rat-race coupler limits the broadband performance of the circuit due to the delta port. Additionally the rat-race will also introduce losses which affect the noise figure of the mixer. Ideally, the lossy components are minimized in the structure whilst maintaining the functionality of the circuit. The single-balanced topology and its variants are discussed in [19]. One of the variants include leaving out the hybrid. Therefore to gain more insight 180°-hybrid, its functionalities are discussed in the next section.

The 180 degree hybrid coupler is a four port device with two separate inputs and two outputs. The main functions of the hybrid is power dividing when applied to one of the inputs, or a 180-degree phase shift when applied to the other input and isolation between ports. The ideal scattering matrix for a 180-degree coupler is defined as:

$$[S_{180}] = \frac{1}{\sqrt{2}} \begin{bmatrix} 0 & 1 & 1 & 0 \\ 1 & 0 & 0 & -1 \\ 1 & 0 & 0 & 1 \\ 0 & -1 & 1 & 0 \end{bmatrix}$$

The balanced topology is implemented by a four-port hybrid coupler connected to two single-ended mixers. The 180-degree hybrid can be implemented by a rat-race coupler providing a balanced signal at the output ports when the input is applied to the delta port. Exciting the sigma-port will result in a power division at the output ports. Two fundamental characteristics of the structures can be derived from the previous analysis. An input applied at port 4 result in a balanced output between 1 and 2. When applied to port 3 this results in an in-phase output at port 1 and 2.

Studies have been been conducted on reducing the size of the rat-race hybrid [23] and also achieve wideband performance using the Marchand balun [28]. Both reduced size and wideband performance are favourable for the ADome downconverter. Ideally, the Vivaldi antenna would function as a balanced structure and is able to excite the receiver by a balanced signal. In that case, it would be favourable to omit the balun in terms of losses and noise. The LO signal is the applied to a common node between two equal impedances to achieve the power division to the diodes. A similar implementation for the RF signal is shown in [29], for a passive balanced diode mixer.

2.5. System specifications

An overview of the developed system requirements is shown in Table 2.8.

Requirements for downconversion	Low performance	High performance
Operating band (f)*	**24.25 GHz**	**40 GHz**
Effective Isotropic Radiated Power (EIRP)*	**20.6 dBm (Power Class 3 n260)**	**55 dBm (Power Class 1)**
Signal quality (EVM)*	**30%**	**8%**
EVM uncertainty*	**-1%**	**+1%**
Maximum signal bandwidth*	**50 MHz**	**400 MHz**
Carrier aggregated bandwidth (BW)*	**400 MHz**	**1200 MHz**
Minimum far-field distance (d)	**0.5 m**	**2m**
Free Space Path Loss (FSPL)	**54 dB @ 24GHz/0.5m**	**71 dB @ 40GHz/2m**
LO power	**10 dBm**	**15 dBm**

Table 2.8: System performance for ADome downconverter. *requirements set by the 3GPP standard for New Radio User Equipment devices

. The requirement for the FSPL was developed in the previous section for various dome sizes and operating frequencies, which affect the maximum antenna aperture to be measured. Lastly, the LO power was derived from available off-the-shelf components. A power-budget was developed and it can be concluded that all implementation can deliver up to 15 dBm of LO power by implementing a buffer on the sensing node.

3

Mixer Implementation

This chapter describes the implementation of a single-balanced passive diode mixer in the NXP SiGe technology technology. Starting with a description of the technology and its considerations. Furthermore, a single diode-connected HBT is studied using small and large signal analysis. The proposed approach is needed for the design and simulation of the mixer. In section 3.2, the circuit operation is analyzed and simulated. In the last section of this chapter, the implementation of the layout of the mixer core is discussed.

3.1. Technology

The SiGe BiCMOS Qubic4Xi technology enables a design with HBT devices with an f_T up to 180GHz. The technology provides six metal layers, connecting the external environment of the die to the substrate where the devices are situated. Each metal layer and via has its own properties in terms of conductance, maximum current and dimensions. The structures to build the circuit are designed conform these requirements and evaluated using EM simulations in Advanced Design Systems (ADS) Momentum simulator. The latter simulation provide insight into parasitics influencing the behaviour of the circuit. Before implementing a preferred mixing topology, the behaviour of the device must be analyzed which is treated in the next section.

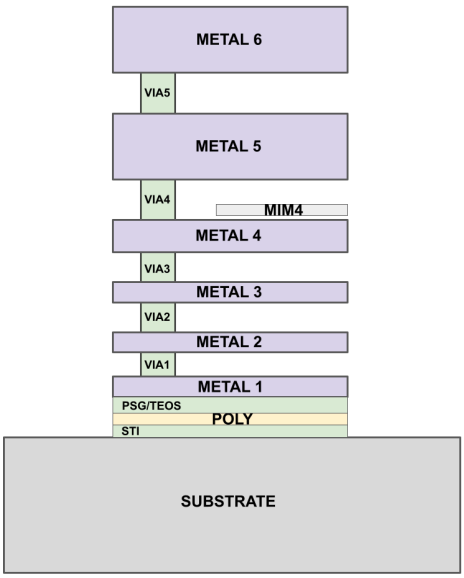


Figure 3.1: Metal layer stack of the NXP Qubic4Xi technology

3.1.1. Device analysis

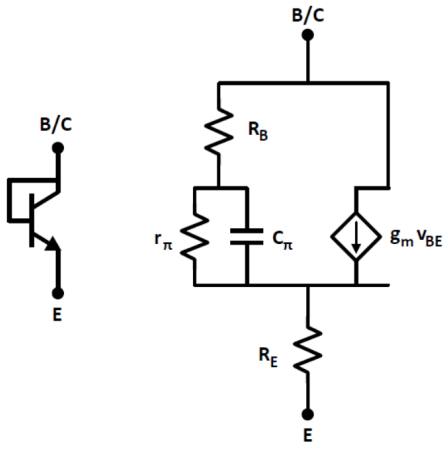


Figure 3.2: Small signal model diode-connected BJT

Impedance matching the device to interfacing circuits is critical to ensure optimal power transfer. In this section the input impedance of the device is determined using analytical models for small-signals. Large signal analysis is essential for designing the mixer and is treated in the next section. The impedance of the first-order small signal model of the transistor at the base/collector terminal is derived as:

$$Z_{in} = R_E + R_B + \frac{1 - g_m R_B}{g_m + \frac{1}{r_\pi || \frac{1}{sc_\pi}}} = R_E + R_B + \frac{\frac{1}{g_m} - R_B}{1 + \frac{1}{g_m (r_\pi || \frac{1}{sc_\pi})}} \tag{3.1}$$

The real part of the input impedance of the diode-connected HBT is dominated by the emitter and base resistances. Increasing the transconductance of the device g_m minimizes the influence of the resistance R_B. Taking g_m to infinity the expression reduces to $Z_{in} = R_E$. Two design choices can be made for increasing the transconductance. Firstly, by increasing the base-emitter voltage V_{BE}, however this is limited by the breakdown voltage and the available supply. Secondly, by sizing the device which in turn also increases the capacitance. The impact of these design variables on mixing performance will be discussed after the large signal analysis of the device.

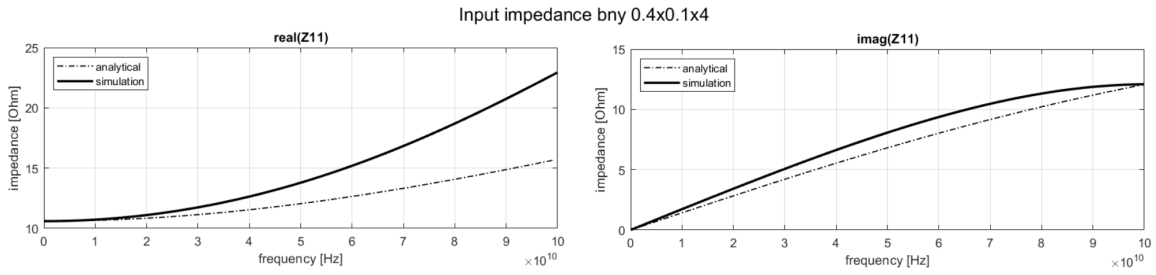


Figure 3.3: Analytical and simulated device input impedance

To verify the analytical derivation of the input impedance, a S-parameter simulation is performed in the technology and compared with the analytical formula. An S-parameter analysis between 1kHz - 100 GHz is performed using a diode-connected 'bny' transistor (W=0.4um/L=0.1um/number of Emitters=4). The bias voltage is set to 800 mV. The DC operating points provide small signal parameters for the analytical expression and is compared with the simulated values.

The analytical approximation of the real impedance starts to deviate above 10% for frequencies larger than 40 GHz. The imaginary part of the impedance stays within the 10% margin over the entire simulated frequency range.

The differences can be explained by the oversimplified model which does not take into account several device parasitics, nevertheless the accuracy in the design frequency range allows to use the analytical numbers as a start point and conduct the optimization for device sizing based on the simple model.

Large signal analysis

The large signal LO pumping the mixing devices needs to be taken into account since, the quiescent bias point of the device using small-signal analysis is changed by the LO drive and will alter the device response. The input impedance of the device is determined using large signal s-parameter analysis. For this, the periodic s-parameter *PSP* analysis is used in the Virtuoso simulator.

An appropriate match is achieved by simulating the large signal behaviour of the device. The LO signal is in the order of $10-15dBm$. The small-signal RF source is set at $-20dBm$. The Virtuoso simulator provides periodic s-parameter simulations using the *PSP* analysis mode. Using this analysis, it is possible to assign two frequencies at PORT0, namely the LO and RF signal. An S-parameter analysis across the RF band is performed, to obtain the input impedance of the device.

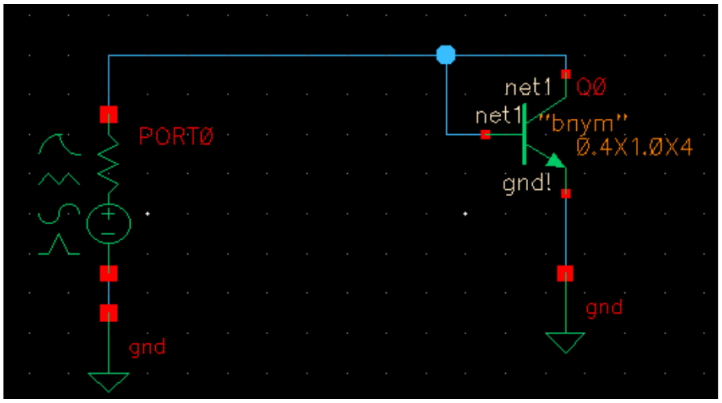
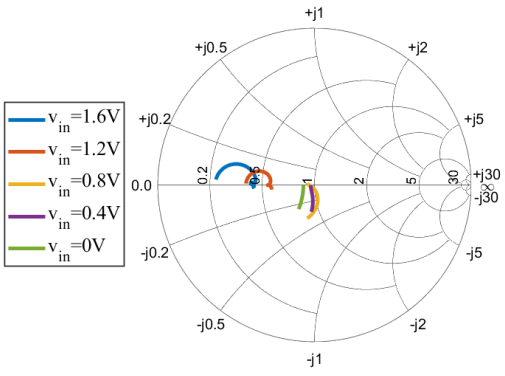
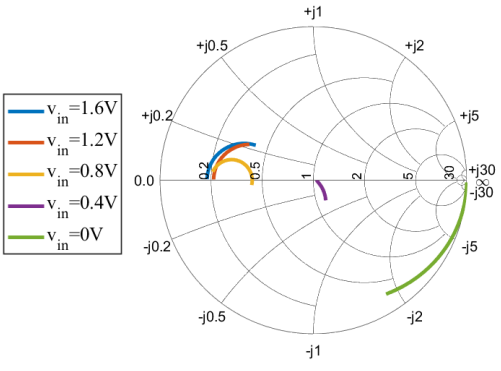


Figure 3.4: Simulation setup of the diode-connected HBT using PSP analysis for large signal excitation. PORT0 is set to a DC = 800 mV and RF and LO powers of -20 dBm and 15 dBm respectively.

The difference between simulating the diode with small-signal and large-signal S11-parameters is shown in Figure 3.5. For a zero DC bias, the green curve in Figure 3.5a takes into account the pumping LO signal. The green curve in Figure 3.5b corresponds with the values found in the analytical of a small-signal diode. The overall characteristic of the S-parameter simulations are identical, however the large signal analysis also takes into account a certain offset due to the LO signal.



(a) Large-signal S-parameter vs bias with v_{in} the DC voltage



(b) Small-signal S-parameter vs bias with v_{in} the DC voltage

Figure 3.5: Comparison between the S-parameters using either SP analysis or PSP analysis for the diode-connected HBT.

Also shown, is the influence of the DC biasing on the input impedance of the device. Looking again at the PSP analysis, a DC bias of 0.8V with the corresponding dimension of the transistor ends up in the center of the Smith Chart, making it more practical to achieve a wide-band match. By having a good analysis and simulation tool, the next step is to start with the considerations of sizing the device providing the input impedance matching network.

3.1.2. Single-diode mixer analysis

The design approach of the balanced mixer starts with the design of a single diode mixer. First an optimal device has to be chosen and its corresponding network. Device sizing, matching and the biasing of the device play a role for minimizing conversion loss of the circuit. Therefore, this section will focus on these three aspects, before combining the two single diode mixers to form the balanced mixer. The first step for implementing a diode mixer is to analyze the impedances at the terminals of the device.

Device sizing

The provided technology allows for designing with different dimensions of the bipolar transistor. To comply with the provided device models, the following preset parameters were used to determine optimum device sizing.

Width (in um)	Length (in um)	Number of Emitters
0.4	1.0	2 (min)
0.5	1.5	20 (max)
	2.3	

Table 3.1: Preset values for 'bny' device

The conversion loss degradation factor δ of a diode mixer is defined as [25].

$$\delta = 1 + \frac{R_S}{Z_S} + \frac{Z_S f_{RF}^2}{R_S f_c^2} \tag{3.2}$$

with series resistance R_S and source impedance Z_S both evaluated at f_{RF}. The cutoff frequency f_c of a diode is related to the series resistance and junction capacitance of a diode.

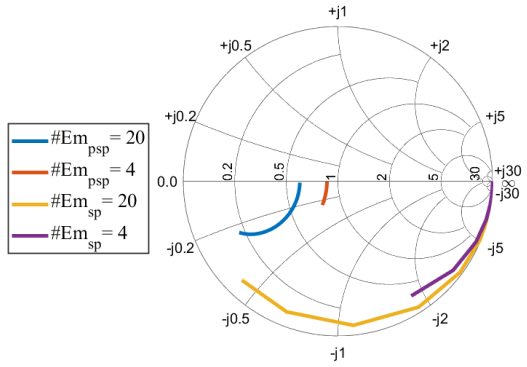
$$f_c = \frac{1}{2\pi R_s C_{j0}} \tag{3.3}$$

Minimizing the degradation factor can be achieved by making a trade-off in device sizing. Either increasing the size of the device to reduce R_S which results in a larger junction capacitance. This in turn will reduce the cutoff frequency of the device.

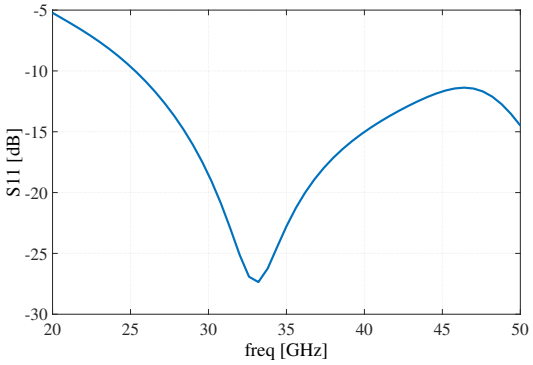
In our case, the emitter width and length are kept minimum to minimize the emitter capacitance. The drawback of having a larger base-emitter and emitter resistances is compensated by the fact that the input impedance of the device is close to the center of the Smith chart, as shown in Figure 3.6a. The remaining design parameter is increasing the number of emitters, allowing for a higher current through the transistor. The effect of increasing the number of emitters from 4 to 20 is shown in Figure 3.6a for emitter widths and lengths of = $0.4\mu m$ and L = $0.1\mu m$, respectively. The real part of the impedance decreases for higher number of emitters. The diode size is set to 0.4x1.0x4, the large signal S11 parameters are close to the center of the Smith Chart. Whilst this does not minimize the series resistance of the device, it is possible to achieve a relative simple wideband matching network across the 24-40 GHz frequency range. This is shown in Figure 3.6. The conversion losses are expected to be acceptable for the given application.

A pi-network using L-C-L configuration is used for matching a single diode as shown in Figure 3.7. The "LO" and "Bias" nodes are considered ac-ground and the "HBT" node connect to the base/collector of the bipolar transistor. Capacitor $C0$ functions as DC-block and inductor $L0$ as a DC-feed. The LO is applied to inductor $L1$.

The resulting values for the device size, bias, LO pump level, and passive components is shown in Table 3.2. The resulting matching network achieves a $|S11| < -8dB$. The S11 performance at 24 GHz is non-optimal and will be taken into consideration when implementing the non-ideal components.



(a) Influence of increasing the number of emitters of the device on the S11-parameter, for large signal (psp) and small signal (sp)



(b) S11-parameter simulation of a single matched 0.4x.1.0x4 'bnym' diode

Figure 3.6: Analysis of device sizing and the resulting S11 of the matched device.

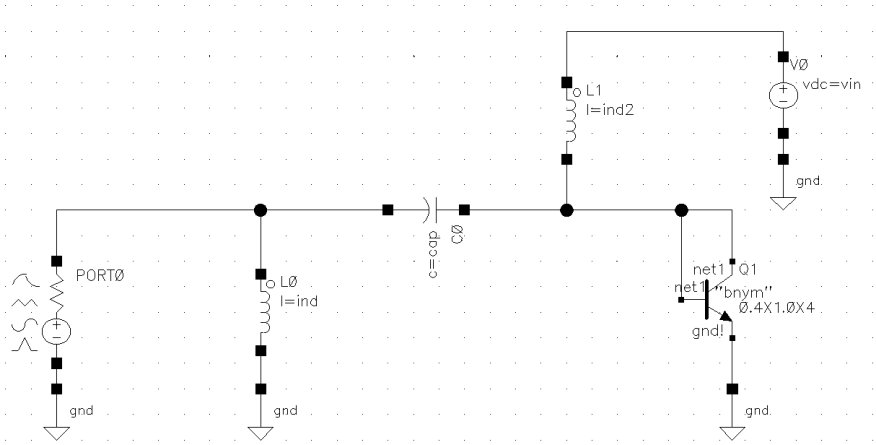


Figure 3.7: Ideal matching network

Parameter	Value
DC bias	**800 mV**
LO Pump Power	**15 dBm**
Inductor (L0)	**270 pH, 330 pH**
Capacitor (C0)	**120 fF**

Table 3.2: The obtained values for matching a single-diode to a 50Ω source impedance.

3.2. Single-balanced mixer design

The previous section analyzed the matching of a single-diode, taking into account large-signal effects which are involved during mixing operation. The single-balanced topology is preferred as was discussed at the start of the mixer design. Therefore, in this section the design is progressed by incorporating the matching networks for the single diodes to form the balanced configuration.
As shown in Figure 3.8, the primary winding of a conventional transformer 180-degree hybrid is excluded from the design since the signal is assumed driven differential from the antenna. Similar implementations of connecting a balanced RF signal to a passive balanced diode mixer can be found in [19]. First we analyze the operation of the circuit more in-depth.

The common node of the inductors L1 and L2 function as a center-tap for the LO signal. Serving the purpose to function as the in-phase power divider of the LO. The inductances of L1 and L2 are chosen equal. Furthermore, the DC blocking capacitances C1 and C2 and bias feed inductors L3 and L4 are used for matching the mixing devices. The node connecting L1 and L2 is used to feed the LO signal to the mixer diodes.

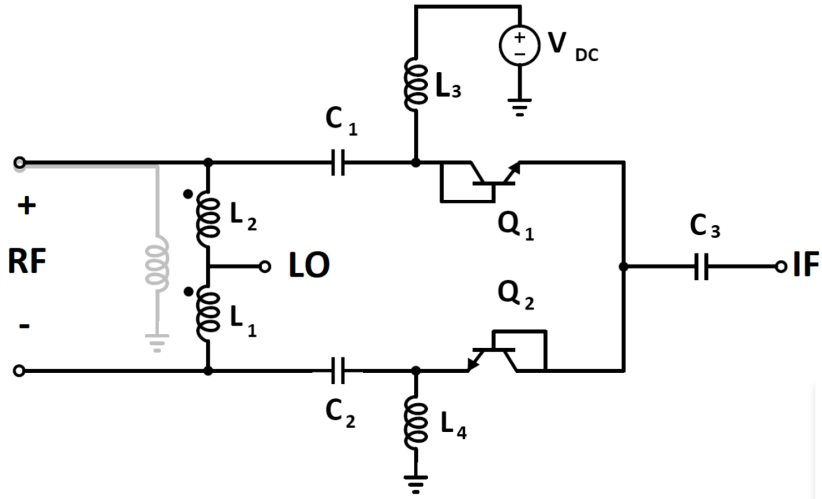


Figure 3.8: Transformer-less balanced mixer

Furthermore, the RF signal is applied differential across the inductors L0 and L1. The capacitance C3 at the IF node functions as a DC blocking capacitance, ensuring the DC path through the mixing devices.

A mixer testbench is created to efficiently switch between levels of implementation. In this case, ideal passive components and technology device models are used to evaluate the performance of the mixer. The input RF source is connected to an ideal balun to feed the circuit with a differential signal. The impedance of the source is set to 100Ω, assuming both positive and negative RF lines are 50Ω lines. Therefore, the mixer input is loaded with a 100Ω differential impedance. Each diode will then see 50Ω as was designed for in the previous section.

To evaluate the balanced mixer topology, the insertion loss and conversion gain of the structure are simulated. The component values for the single-diode match are optimized to the values $L1 = 400pH$, $C1 = 110fF$,$L1 = 300pH$. To provide 50Ω to the single diodes, the single-ended source impedance is set to $R_s = 100\Omega$ and converted to a balanced signal by an ideal balun. The resulting s-parameter simulation is

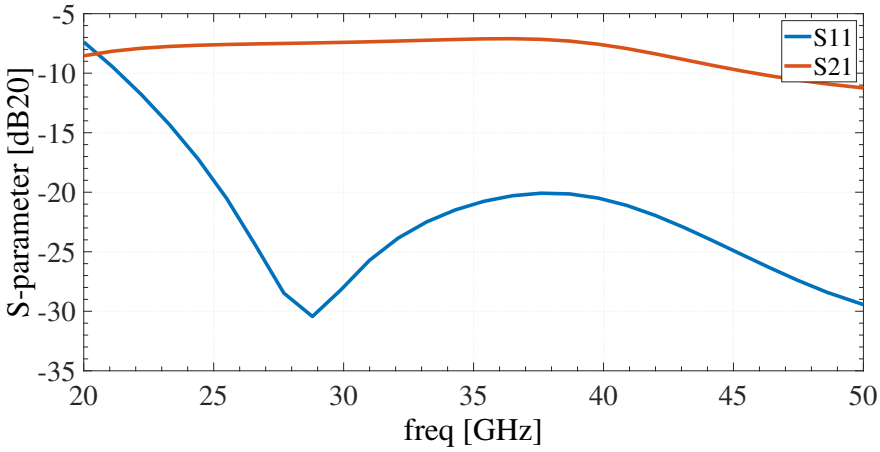


Figure 3.9: Resulting S11 and S21 large-signal S-parameter simulation

shown in Figure 3.9. The achieved performance is shown in terms of |S11| <-17 dB and |S21| <-8 dB, in the 24GHz - 40 GHz band. From this it is concluded that an appropriate match is achieved using ideal passive components whilst using the device models. The next step of the implementation of the circuit is to include library and EM models achieve to get a more realistic behaviour of the circuit.

3.3. Layout

In this section the design of the mixer circuit is progressed for layout implementation. During layout, the design has to account for design rules in terms of electromigration, line spacing and orientation, and the layer stack including the available vias. First, a description is given on the implementation of the interconnects from the device to the upper metal layers. Then, a simulation method is discussed for the inductors. Lastly, the transmission lines connecting the mixer-core to the outer pads are designed.

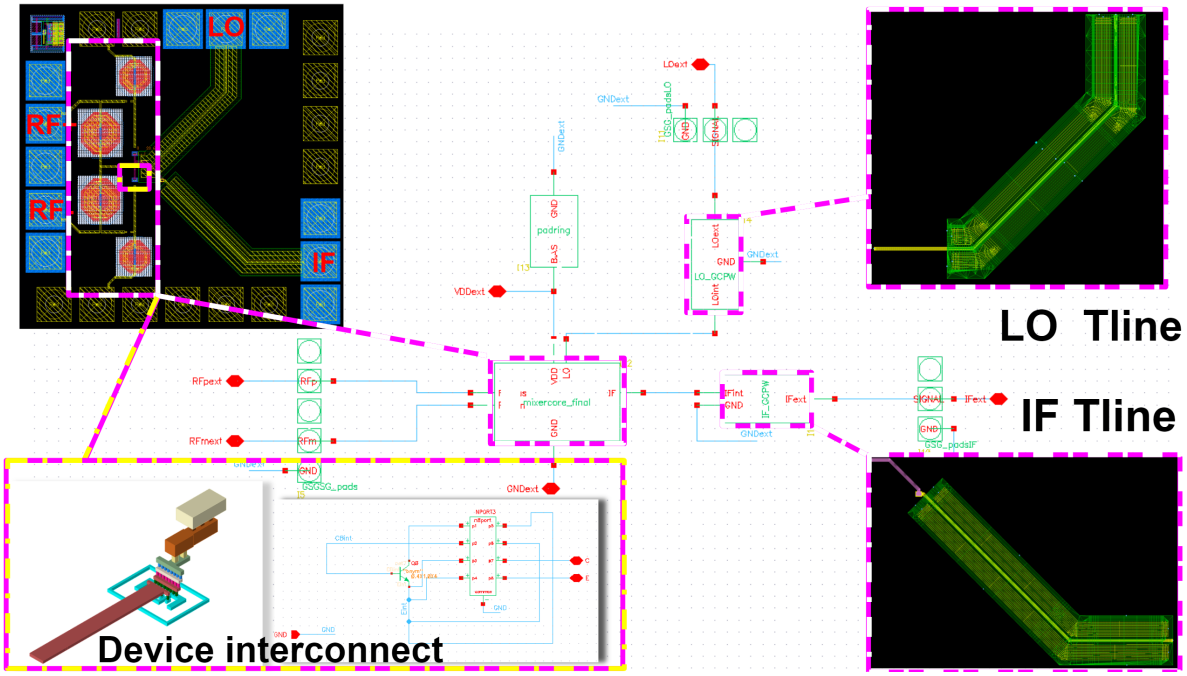


Figure 3.10: Overview of the simulation setup and its sub-components

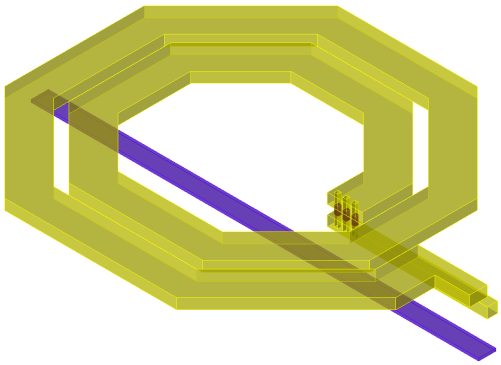
Shown in Figure 3.10 are the mixer components that have been considered for the layout. In the top-left corner the layout of the mixer-core is shown. Included in the simulation are the effects of the bondpads, LO and IF transmission lines and interconnects. The metals from the top to the bottom layers, connecting the device are shown in the lower left-hand corner. The results of the EM simulation are then incorporated in the simulation as shown. A similar method is for the other EM simulations. The mixer-core contains the matching network and is discussed next.

3.3.1. Matching network inductors

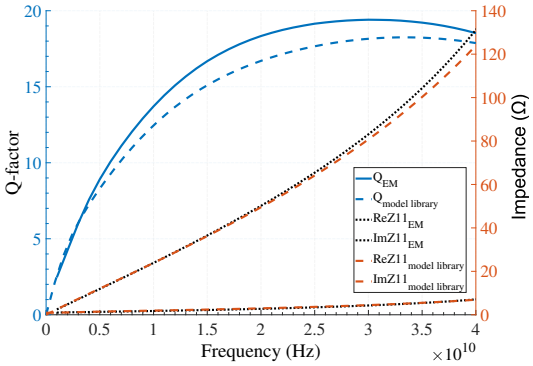
The matching network is implemented using inductors and capacitors. These components are available in the technology library. In this section, the parasitics of the library inductor component are evaluated using Momentum EM simulations. An inductor of $0.4nH$ is considered for this analysis, shown in Figure 3.11a. A one-port S-parameter simulation is performed and the corresponding z11-parameters are evaluated to determine the quality factor of the component. The quality factor is defined as the ratio between then imaginary and real part of the z11 parameter:

$$Q = \frac{Im(Z_{11})}{Re(Z11)} \tag{3.4}$$

The higher the Q-factor the more it approaches the behaviour of the ideal component. The Q-factor degrades due to the losses originating from the losses in the metal. The strategy to gain insight in the performance of the model library is to EM simulate the component and comparing the performance.



(a) Simulated 0.4 nH inductor



(b) Momentum and Virtuoso simulation comparison between Momentum (EM) and Virtuoso (model library)

Figure 3.11: Inductor performance comparison between the EM simulation and the model library.

The EM results are compared with the model library in Figure 3.11b. The Q-factor retrieved from the EM simulations deviate less than 10% within the band of interest compared with the model library. The model library achieving lower Q-factor seems to account for more non-idealities of the inductor, it is assumed the library component models the correct behaviour of the inductor. Therefore, to speed up simulation times the remaining EM simulations will be limited to the interconnect lines and the transmission lines, which will be discussed in the following section.

3.3.2. LO and IF Transmission Lines

The next part of the design considers the transmission lines for the LO and IF signal, connecting the mixer-core to their corresponding bondpads. The LO signal is applied at the common node of the inductors branching into the differential RF ports. Additionally, the IF signal is tapped at the common node between the two BJTs. Essential for the choice of transmission lines is low-losses at the design frequency. For implementations purposes, the two signals are connected to the pads using Grounded Co-planar Waveguide (GCPW) transmission lines. These lines are implemented due to relative low complexity and -loss features.

The strategy for designing the lines is three-fold. Initially, the appropriate dimensions of the line need to be determined. This will result in the desired characteristic impedance of the line, namely 50Ω. Then it is needed to route the components as desired and find an optimum implementation. The positions of the LO and IF pads were chosen north-east and east-south, respectively as shown in Figure 3.10. The main reason for this is to reduce the influence of coupling between the two lines. This is done by increasing the distance between the lines and placing them orthogonal with respect to each other.

The line dimensions for metal 6 are designed by importing the technology layer map and its characteristics into ADS 'Controlled Impedance Line Designer' using metal 5 as the ground-reference. The line dimensions for a 50Ω GCPW are tabulated below.

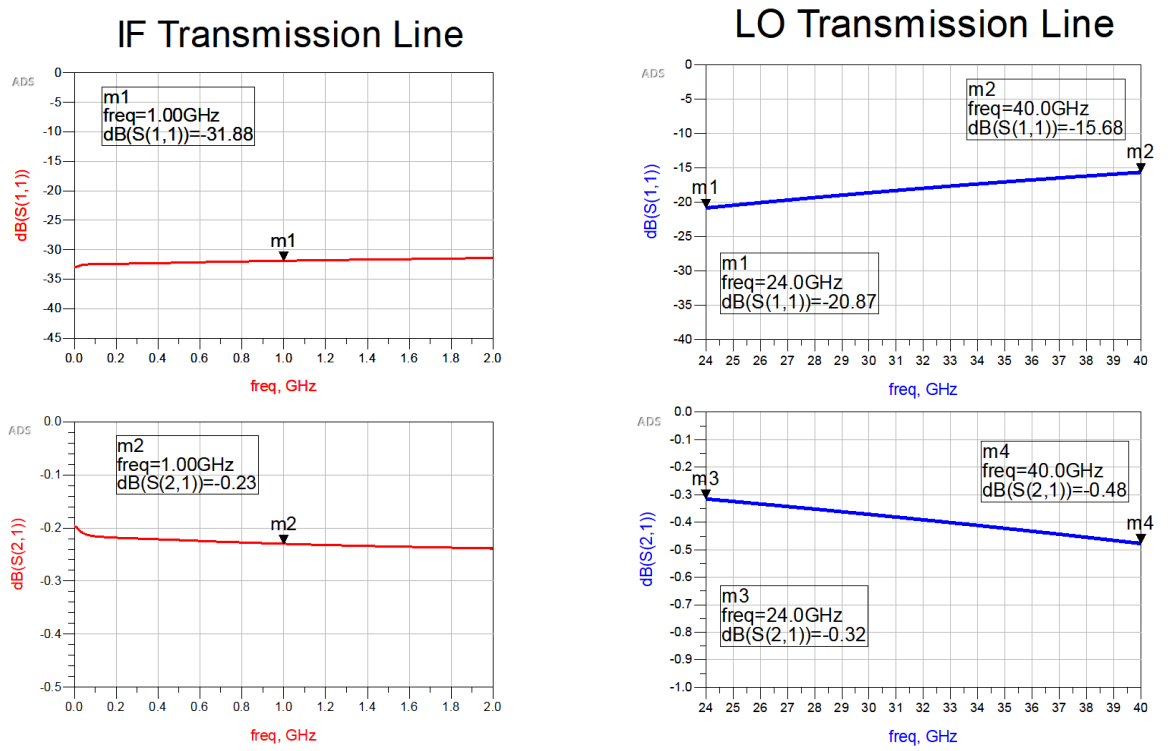
Dimension in μm	Height (h)	Width (W)	Thickness (T)	Gap (S)
	10.7	5	3.055	4

The height and thickness are determined by the technology and is specified in the substrate definition. The width and gap are free to design with, but also limited by the DRC rules specified by the technology. The structure is implemented in Cadence and EM simulated using Momentum. For simulation purposes the ground plane for the GCPW is simplified by partially including it in the EM simulation.

The implementation of the LO line is shown in the top-right corner of Figure 3.10. The ground planes on the bottom and on the top surrounding the signal line are implemented with sheets of metals for simulation purposes. Two-port S-parameter simulation reveal the performance of the LO line in Figure 3.12b.

The achieved |S11| of -21 dB at 24 GHz and -16 dB at 40 GHz are considered sufficient for achieving wideband performance since this accounts for 2.5% of the power being reflected at 40 GHz, for a 50 ohm load. Ideally, the S11 is constant and more flat across the frequency band since now a difference of 10 dB is seen across the band of interest. The losses in the line are in the order of -0.3dB at 24 dB and -0.46dB at 40 GHz with a 0.16dB difference between the limits of the band of interest. The deviation in losses across the band is 0.1 dB and is assumed to have minimal impact on the wideband performance of the mixer.

To conclude, the implementation of the LO line resulted in a large deviation for the input match of the LO potentially influencing the power delivered to the mixer-core and therefore the performance of the mixer. The line exhibit low-losses as was expected due to the GCPW structure and show sufficient low losses at 40 GHz.



(a) The transmission line connecting the devices to the output IF pad.

(b) The transmission line connecting the LO to the mixer circuit.

Figure 3.12: Simulated S21 and S11 result of the LO and IF lines introduced at the start of this section.

The IF line is implemented with a similar method as the LO line, the key difference is the lower design frequency of the line. The design frequency of the IF at 1 GHz with a maximum bandwidth of 400 MHz poses less stringent requirements compared with the LO line. The results are shown in Figure 3.12a. The |S11| is -32 dB achieving a relatively good performance, compared with the LO line at its design frequency. Secondly, the achieved losses are -0.23dB which is considered to have minimal effect on the mixer performance.

Worth noting is the difference at 1 GHz for both the IF and LO lines, where the seems to perform better. The reason for this is the connection between the IF GCPW and the diodes. The separate devices are connected together via metal 2 which is a thinner metal compared with the upper metal layers. The IF GCPW is situated in layer 6, which needs the implementation of a via. The design of the connection between the metal 6 of the IF line and the devices will be treated next.

The section of the line connecting the device to the upper IF line is shown in Figure 3.14. The line is routed in this way, since the LO line is routed in M6 above the diodes toward the inductors.

To verify the behaviour of the accuracy of the EM simulation including the via. The results are then compared with an ideal simulation. This is shown in the right hand sight of Figure 3.14. It must be noted that the ideal simulation does not include the via, therefore better performance in terms of input reflection and return losses are expected for the ideal simulation.

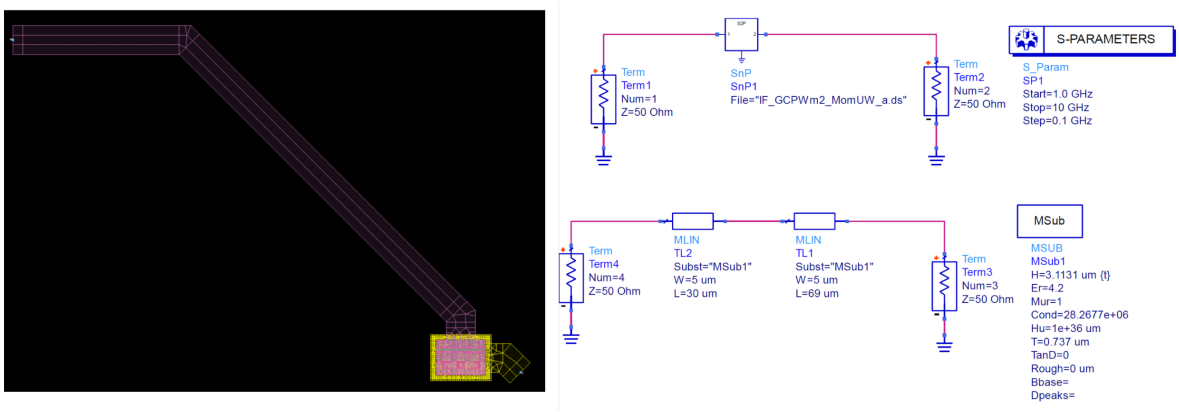


Figure 3.13: Simulation setup between the EM simulated line, including via and the ideal simulation using MLIN components and the definition of the substrate

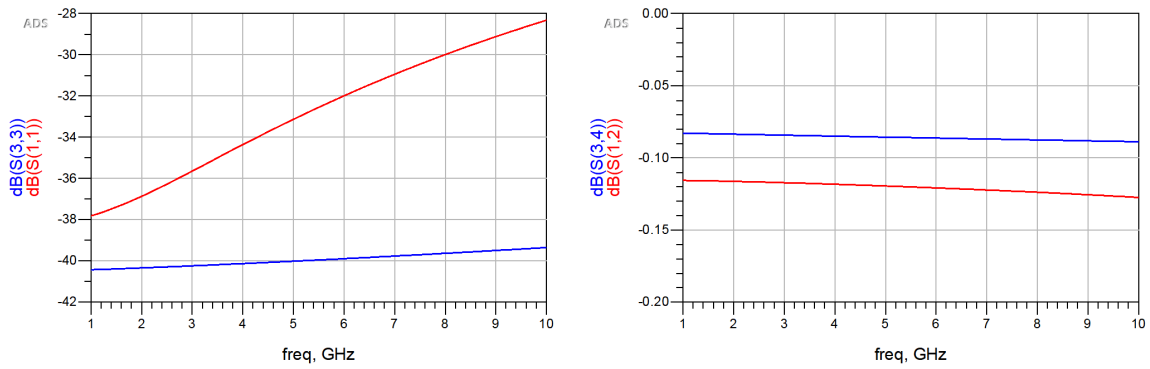


Figure 3.14: Comparison between EM simulated line in metal 2 (S11,S21) and an ideal MLIN simulation (S33, S34). The results for the return loss differ at 1 GHz by less than 3 dB, the insertion loss differs <0.05dB.

The comparison is shown in Figure 3.14. The difference between the |S33| and |S11| at 1 GHz is approximately 3 dB, which is accounted to the via. At higher frequencies the effect of the via becomes larger and the difference is increased to 12 dB. The effect of the via is therefore noticeable in the EM simulation.

The difference in losses between the ideal and EM simulated values are smaller. In the order of 0.04 dB. The absolute numbers reveal not much, however these losses contributes -0.1dB of the total loss of -0.2dB to the losses of the entire IF line at 1 GHz, as can be seen in Figure 3.12a. Also, in this case the EM simulations are verified by the ideal case. To conclude, the connection between metal 2 and metal 6 accounts for a large part of the entire line loss, which has been verified comparing the ideal case with the EM simulations.

3.4. Differential input considerations

The motivation for applying a differential RF was to connect a balanced antenna directly to the input of the mixer, providing the out-of-phase signal without the need for a unbalanced-to-balanced conversion. This would in turn minimize the losses in the circuit.

In this part, we address the assumption of applying a balanced signal at the mixer input terminals by analyzing a simple dipole. This analysis is put in place to identify the common and differential loading conditions to provide to the circuit simulator. In literature the effect of common-mode and differential-modes on a balanced has described in [30]. Where the antenna reflects most common-mode (CM) signals and provides a match for differential-mode signals (DM). To verify this, a simplified balanced structure similar to the Vivaldi antenna is analysed. A dipole antenna is a balanced structure and can be analysed for both DM and CM excitation. Using mixed-mode S-parameter analysis, the common and differential modes of the antenna are analyzed. Mixed mode S-parameters are defined for a 2-port network using the following relations:

$$S_{cc1} = (S_{11} + S_{12} + S_{22} + S_{21})/2 \tag{3.5}$$

$$S_{dd1} = (S_{11} - S_{12} + S_{22} - S_{21})/2 \tag{3.6}$$

The subscript "cc" and "dd" refer to either CM or DM S-parameters. An ideal dipole structure is EM simulated using ADS momentum and analysed using the method described above. The s-parameter data is retrieved from the EM simulation and used for the mixed-mode analysis. The simulated simple dipole and mixed-mode analysis results are shown in Figure 3.15 and Figure 3.16.

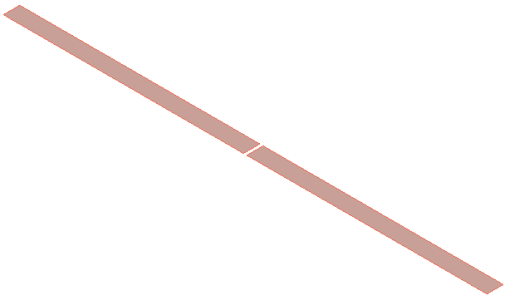


Figure 3.15: Simple Dipole EM simulation

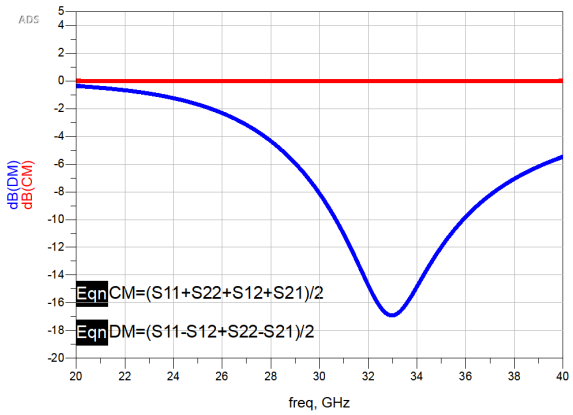


Figure 3.16: DM and CM S11 of the simple dipole

This analysis shows that an ideal dipole reflects all common-mode or unbalanced signals, since the input reflection coefficient equals zero for the common mode. For simulating this behaviour, an ideal balun is connected to a RF source. Consequently, it is assumed the input of the mixer is driven by a balanced signal. It should be mentioned that a practical implementation results in less reflection of the common-mode. Non-ideal effects can be simulated by introducing gain or phase imbalances, however this is dependent on the design of the receiving antenna. The impact on system performance is determined in Chapter 4. Now that we have considered the common-mode being rejected by the balanced antenna, it is still possible for the LO to radiate through one of the antenna lines as a monopole. The monopole antenna length would be half the length of the dipole, equal to $\lambda/4$ and radiate at the frequency of the LO. Therefore, some form of isolation between the antenna and mixer would be needed to mitigate the this effect, such as an isolator or a hybrid. This in turn will increase the losses in the chain. Another option would be to implement a LNA, in the ideal case for a wide frequency range and not limiting the linearity of the system. In the next part the mixer-only implementation will be discussed with respect to the Vivaldi antenna.

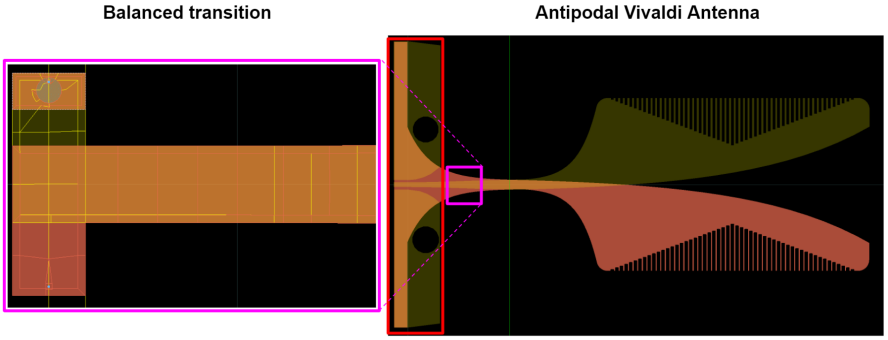


Figure 3.17: Illustrative transition needed for the Vivaldi antenna developed in[9] to feed the differential mixer. The original balanced-to-unbalanced transition is shown marked by the red box. The purple box indicates where the balanced could be converted to two planar balanced lines onto one side of the PCB

In the specific case of the ADome, an antipodal Vivaldi antenna is used. Fundamentally, the Vivaldi antenna is a balanced structure and the same principles hold as for the simple dipole case. The antipodal variant however provides a planar transition to single-ended. This is achieved by using a conductive plane on the top and bottom of the PCB. By referring one of these planes to ground, the balanced to single-ended conversion is achieved by a coplanar to microstrip transition as explained in [9]. The implication of this for the differential mixer is that an off-chip transition is needed to integrate the mixer with the Vivaldi antenna. An example of such an implementation is shown in Figure 3.17, in-depth implication of the antenna performance, are not considered in this work. However, the imbalance induced by such a structure and its impact will be discussed briefly.

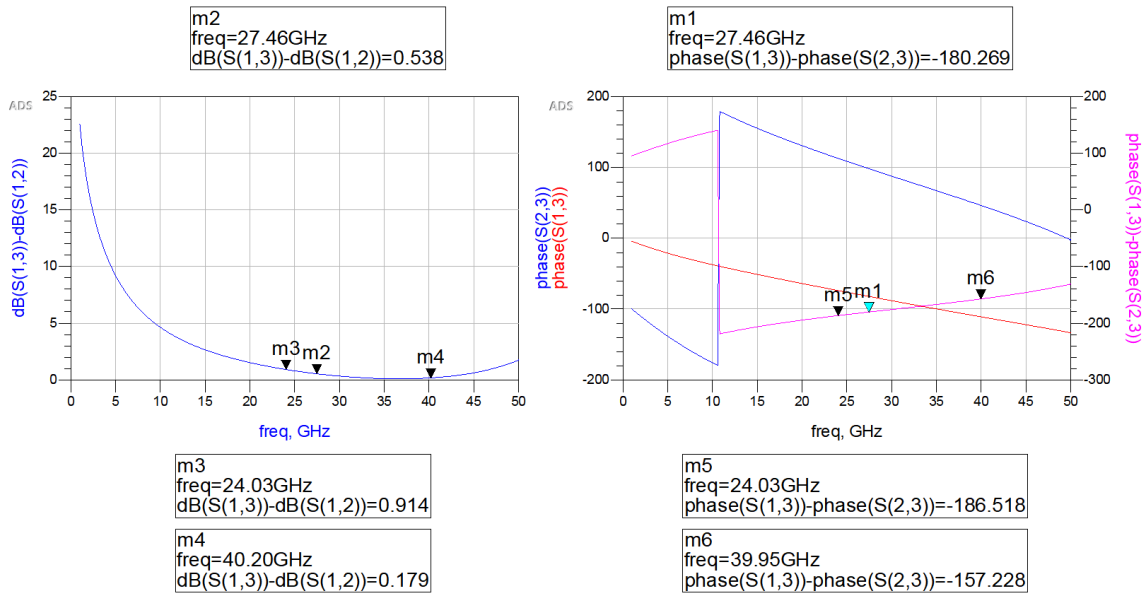


Figure 3.18: Simulation results of ideal coupled lines, using the dimensions of the lines towards the transition of the Vivaldi antenna.

For deriving guideline numbers on the expected gain and phase imbalances, an ideal simulation is performed for the balanced line excluding the transition to study the effects of imbalance. This includes the section surrounded by the pink box up until the green line in Figure 3.17. Figure 3.18 are the resulting simulated imbalances. The line provides a 180 degrees out-of phase signal at 27.46 GHz as shown by marker 1. The corresponding amplitude imbalance is 0.538 dB. The phase imbalance between 24 and 40 GHz is 13 degrees maximum for this simulated line. Important to note is that adding the transition will add more imbalances. However, these figures give reasonable insight for the expected imbalances.

4

Mixer evaluation for the ADome application

4.1. Mixer simulations

In this section, simulation results are presented of the previously introduced mixer design. The design is focused on mainly four performance indicators, namely conversion gain, noise, isolation and linearity performance of the mixer. The metal layers connecting the model components are EM simulated in the Momentum environment. The devices inductors and capacitors are incorporated in the simulation using the corresponding model libraries.

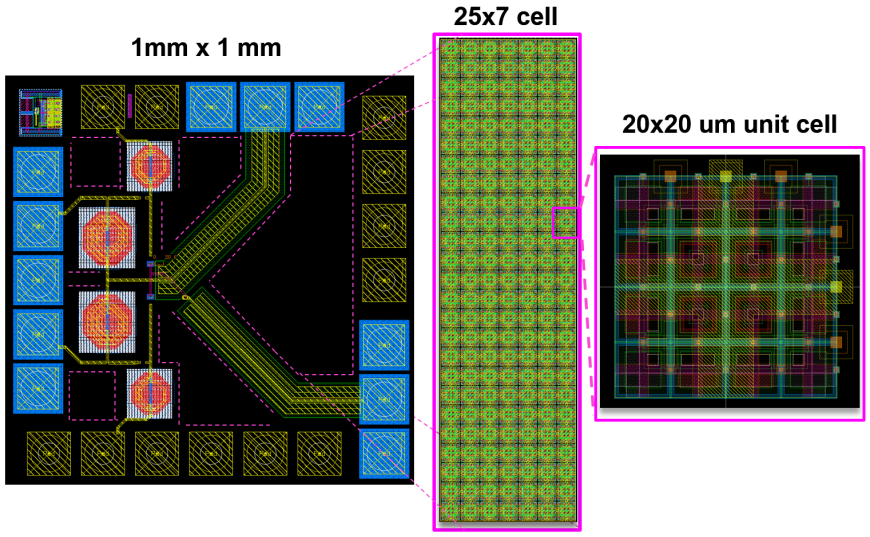


Figure 4.1: Simulated mixer core and marked areas in purple needing to fulfill density requirements before fabrication. A magnified version of the metal structure cells to achieve the requirements are shown as well.

The layout includes RF and ground -pads and Electro-Static Discharge (ESD) protection. The implemented components of the circuit comply to DRC and LVS rules, except for the IF and LO transmission line ground planes which violate the metal density rules. This can be seen in Figure 4.1 Therefore, the implementation and analysis of the effects of the ground plane fulfilling density requirements of the chip are excluded from this analysis. To conclude, this section provides post-layout results of the proposed mixer-core. The area of the chip including pads is 1mm x 1mm.

4.1.1. Conversion gain and Noise Figure

The post-layout simulation results using PSP analysis are shown in Figure 4.2. Compared with the ideal component implementation, the |S11| has increased by $2.5dB$ to $-12.5dB$ at 24 GHz. At 40 GHz the $S_{11} = -13.5dB$ resulting in a difference compared with the the ideal simulation of $7dB$. This effect can be accounted to the losses of the interconnect and the matching components. The conversion gain performance is approximately 1 dB less, compared with ideal components.The S22 is defined in the simulation as the output reflection coefficient at 1 GHz. Inside the band of interest a reasonable match is found with $S22 < -15dB$. Less favourable performance of the circuit is shown for the LO port with a return loss of 3 dB between 30-35 GHz, this is part due to the LO line which was designed for 50 ohm loading conditions, however this is not the case.

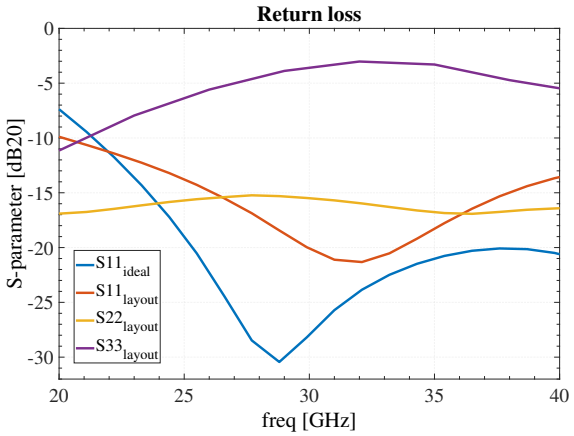


Figure 4.2: Return loss including EM simulations

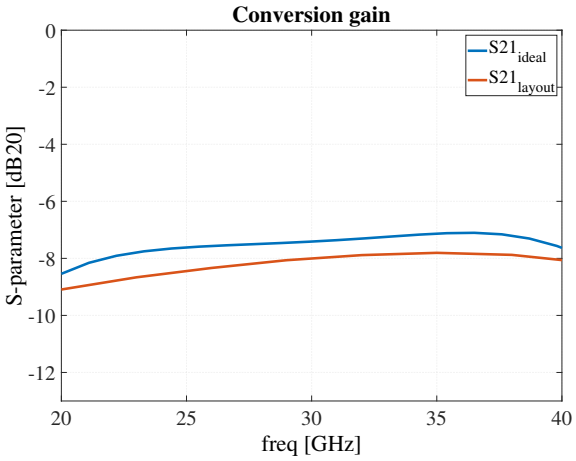


Figure 4.3: Conversion gain for the post-layout simulations

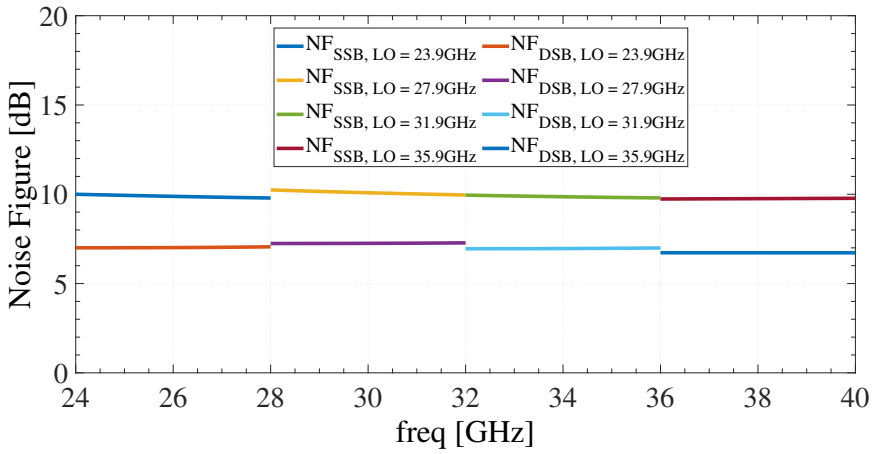


Figure 4.4: Single and double -sided Noise Figure of the mixer

The PSP analysis was used for determining the noise figure of the circuit. Both the Single and the Double sideband NF are shown in Figure 4.4. The achieved single-sideband noise figure for the implementation is between 10 dB between $f = 24GHz$ and $f = 40GHz$. The jumps seen in the figure can be explained by describing the simulation procedure. For this simulation, the LO was varied to maintain a maximum IF frequency of 4 GHz. Taking for example the LO at 23.9 GHz and sweeping the RF between 24 and 28 GHz resulting in an IF between 0.1 GHz and 4 GHz. The difference between the DSB NF and SSB is 3dB as expected.

4.1.2. Isolation

Leakage between the RF, LO and IF ports and its influences have been described in the previous chapter. Using the PSP-analysis it is possible to analysis frequencies at the respective ports. For example, at the IF output port an S-parameter is analysis is run at the IF (1GHz) and at the RF (24-40GHz). This enables the possibility to examine the isolation between the ports. The layout simulation results are shown in Figure 4.5.

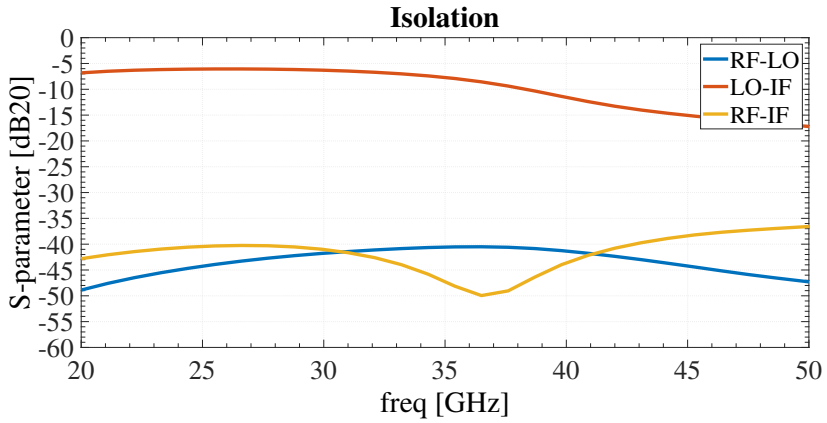


Figure 4.5: Isolation between the RF, LO and IF ports. The LO appears at the output significantly, since no ac ground for the RF frequency is applied to the output port.

The RF signal is attenuated by more than 40 dB at both the LO and IF ports. This is expected since the RF signal appears both out of phase at these respective ports. The RF-IF performance is due to the balanced structure of the circuit. It should be addressed that the ideal balun used for this simulation largely influences the RF-LO isolation performance. Additionally, no coupling between the RF lines and the inductors near the LO are taken into the account, since the components were EM simulated separately. The LO is attenuated worst-case by -6 dB at the IF port, which is also expected since the LO is applied in-phase across the diodes. It is possible to reduce the LO component at the IF-port by providing an ac-ground at the respective frequency, using either a shunt capacitor or a band pass filter.

To conclude, the biggest improvement of the isolation of the mixer is to be achieved for the LO-IF path, since this could potentially saturate the following stages. To conclude, the simulation results of the RF-IF and LO-IF isolation of the mixer are within expectations, care must be taken for interpreting the result of the RF-LO isolation.

4.1.3. Linearity

In order to simulate the linearity of the mixer, harmonic balance simulations are performed. In specific the QPSS and QPAC analysis, allowing for evaluating intermodulation performance of the mixer. It is possible in the simulator to define the harmonics of interest. For the compression point this is the IF frequency. For the intermodulation analysis, this include the third-order harmonic components appearing near the IF. The input RF power is swept and the resulting powers at the previously defined harmonics are evaluated in the QPAC and QPSS simulations. The simulations are performed using $f_{RF1} = 33.1GHz$, $f_{RF2} = 33.2GHz$ and $f_{LO} = 31GHz$. A tone spacing of 200 MHz is chosen which is in line with the expected signal bandwidths. The bias at the diodes is set to $v_{dc} = 1.6V$ and LO drive to $P_{LO} = 15dBm$. The resulting 1-dB compression point of the mixer is $P_{1dB} \approx 1.8dBm$ and third order intermodulation $IIP3 \approx 18dBm$ which are derived from Figure 4.6.

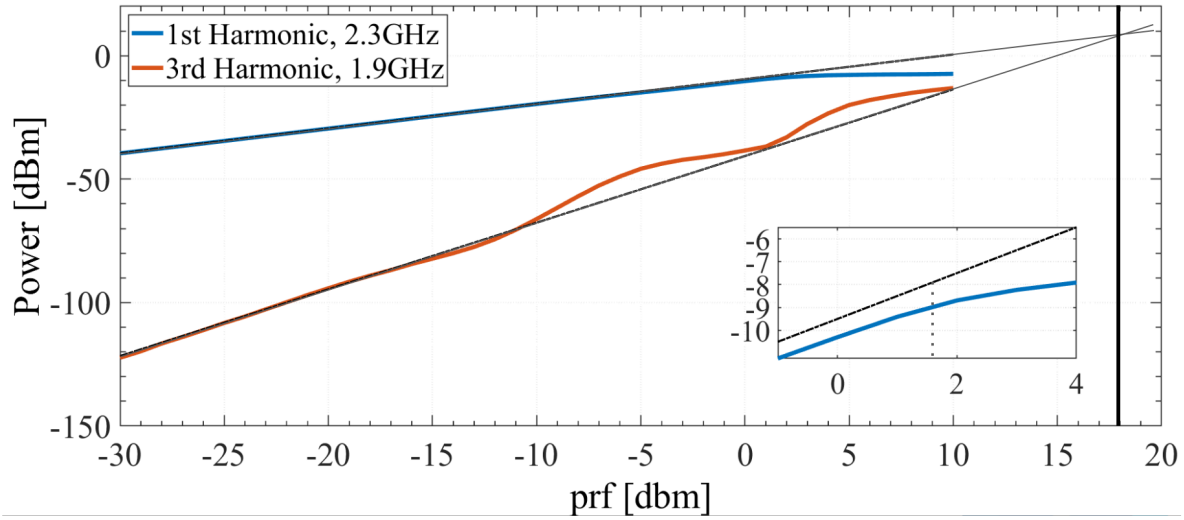


Figure 4.6: First and Third harmonic simulation results, the subplot represents zoom of the 1st harmonic and extrapolated lines. From this the compression point and intercept point are identified

The difference between the LO drive and P_{1dB} is 13 dBm, which is considered a performance drawback of this mixer. Whereas typical passive diode mixers achieve a P_{1dB} within 4-7dB of the LO drive [18]. The $IIP3$ of the simulated mixer is 3 dB higher compared with the LO drive level. This is typical for these mixers , which are able to achieve $IIP3$ performance up to 3 dB higher than the drive level. Both effects of the difference between the LO drive level and the $IIP3$/ P_{1dB} performance can be accounted to the use of a DC bias to minimize conversion losses.

A comparison of the mixer with similar topology and technology mixer implementations is shown in Table 4.1. The difference between LO drive and P_{1dB} also range within the 4-7 dB for these reported mixers. Comparing the absolute numbers of the implemented with literature, the IIP3 is over performing whilst the P_{1dB} is considered achieving good performance at 32 GHz.

4.1.4. Performance comparison

To conclude, a comparison is made between similar mixer topologies found in literature. The tabulated performance of the mixer in this work is based on simulated values. The referred works all include values obtained by measurement of the fabricated circuits in their respective processes.

Parameter	[23]	[31]	[29]	[28]	This work
Technology	SiGe:C/0.35 um	SiGe:C	GaAs/0.15um	TSMC 0.13um	SiGe/0.25um
Device	HBT	BJT	Schottky	CMOS	HBT
Topology	Passive Single-Balanced	Passive Double-Balanced	Passive Single-Balanced	Passive Single-Balanced	Passive Single-Balanced
f_{RF} (GHz)	22-39	77	46-78	45-73	24-40
f_{IF} (GHz)	0.1	-	1	4.5	1
Loss (dB)	8 @ 24 GHz	-0.3	10	-15	9
NF	>10 dB	12.55	-	-	10.5
$P_{in,1dB}$	-1.5	-2.2	-	-2	1.8
IIP3 (dBm)	8.8	-	-	-	18
LO (dBm)	3	0 & 2	12.5	5	15

Table 4.1: Performance comparison between similar passive mixer topologies

4.2. Link EVM simulations

In this section, the system performance is evaluated including the proposed mixer. This is done to verify the assumptions made in previous chapters, such as the requirements derived from the link budget and mixer performance. To do so, a test-bench is setup to evaluate the link performance. The performance of the link is evaluated as follows.

First a comparison is made with an existing measurement setup found in literature [16]. This is chosen to evaluate the performance of the mixer and the link in a realistic scenario. Secondly, the proposed mixer is compared with a similar technology mixer to evaluate its performance.

Three important conclusions can be drawn using the simulation setup. First of all, the SNR requirements analyzed by the link budget are verified by analyzing the achievable $EVM_{\%RMS}$ of the link without non-idealities of the TX mixer and the baseband generator. Ideally, the EVM performance is lower than the AUT such that the system is capable of measuring the errors made, a 1% EVM error is taken into account as was specified in Table 2.8. Secondly, by sweeping the EIRP of the AUT in the simulation two boundaries are identified which are set by the mixer. The first one being the noise added by the mixer when the linearity of the mixer limits the performance of the link. Thirdly, these two boundaries define the dynamic range in which the link can operate and can characterize the AUT for its EVM performance.

One last thing thing to note are the components to model the mixers. The mixer from literature will be modeled using the CG, NF and TOI parameters. Whilst the Qubic mixer will be implemented using the mixer circuit in ADS, including the Mextram device model, non-ideal passives and transmission lines. Important to note is that this simulation do not include cable losses which are present in the practical setup. The implication of this, is an optimistic simulated performance of the link. However, these simulation provide insight in the performance of the link.

4.2.1. Comparison with measurement from in literature

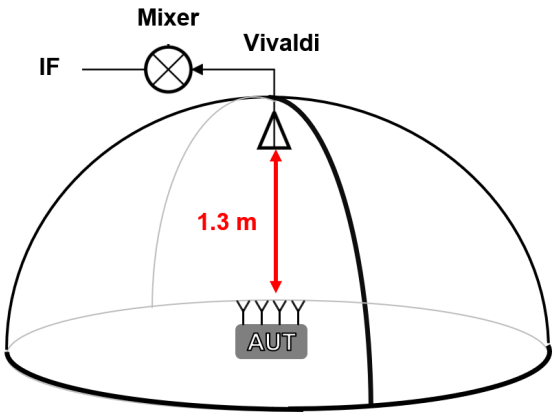


Figure 4.7: Illustration of simulation setup, to compare reported AUT in [16] with proposed mixer

Used as a reference for this simulation is the measurement setup reported in [16]. The performance is then compared using the ADome setup including the proposed mixer, however to keep consistency the path loss is kept equal as shown in Figure 4.7. The reported measurement is performed using a wideband 8x8 transceiver array measured in the TX mode. A waveform generator is connected to an amplifier, attenuator and fed to the array. At the RX side, a horn antenna receives the signal and the output is fed through an amplifier into a 63 GHz scope. The EIRP is swept between -4 and 51 dBm to evaluate the EVM RMS performance of the AUT. The measurement data compared with the designed mixer is shown in Figure 4.8.
The simulation test-bench is setup identical to the reported measurement, using equal path lengths and operating frequency. Using an identical setup in the simulation environment allows us to compare the proposed mixer with the AUT performance reported in the paper.

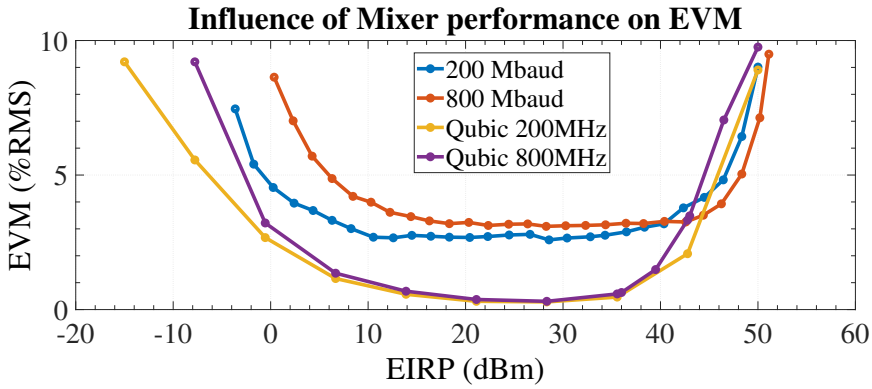


Figure 4.8: Qubic mixer implemented with the MEXTRAM model evaluated at 200 and 800 MHz signal bandwidth and compared with the performance found in [16]

For a 200 MHz signal bandwidth the measurement reaches an EVM of 5% at EIRP = 0 dBm, whilst at 800 MHz this is achieved at EIRP = 2dBm. This is due to the increased noise floor of the larger bandwidth signal. The Qubic mixer shows favourable performance for the lower power levels in this application. A similar noise characteristic is seen at lower power levels. However the impact of the linearity of the mixer is less favourable in terms of the upper limit of the dynamic range of the measurement. Where the original measurement shifts up in dynamic range, the Qubic mixer is performing worse at higher signal bandwidths. A solution to this issue is to attenuate the incoming signal by for example increasing the size of the dome, or by using an attenuator.

4.2.2. Comparison with a similar technology

In this section a SiGe:C bipolar single-balanced passive mixer from literature is taken as a reference [23]. This mixer is chosen since it gives a fair comparison in terms of technology and topology implementation.

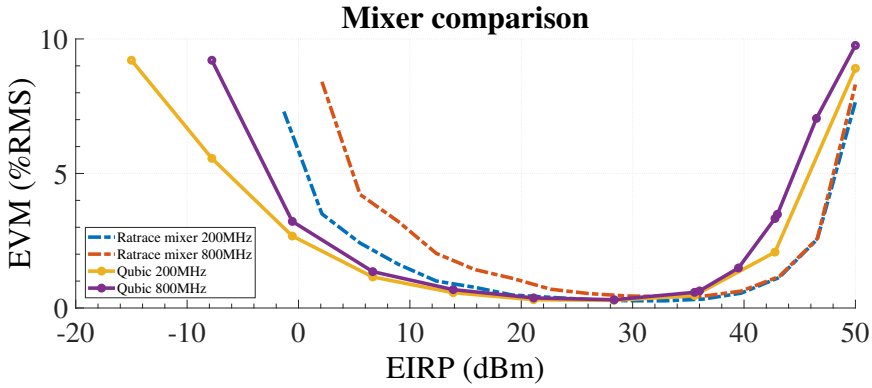


Figure 4.9: Qubic mixer implemented with the MEXTRAM model evaluated at 200 and 800 MHz signal bandwidth and compared with the performance found in [23]

Using the same simulation setup as before, the results of the comparison is shown in Figure 4.9. For EIRP levels between 0 dBm and 10 dBm the mixers have similar performance for both the 200 and 800 MHz cases. However, for EIRP levels < 10 dBm a deviation of 2% EVM_{RMS} is found between the two mixers. The Qubic mixer having of lower conversion losses and noise figure is seen in this range. For EIRP levels >33 dBm where linearity dominates, the Qubic mixer is at a disadvantage when measuring 800 MHz of signal bandwidth. A reason for this could be that the linearity simulations of the standalone Qubic mixer were too optimistic. Another explanation which could limit the performance in this simulation, is a deviation between the Mextram device model in ADS and the model used in the technology library.

4.2.3. Effect of Amplitude and Phase imbalance

The mixer performance has been primarily evaluated assuming the RF is balanced. This choice was made to minimize the influence of losses at the input of the mixer. From a practical point-of-view most antennas provide a single-ended output for connecting to the PCB or single-ended devices. This is also the case for the Vivaldi antenna, which is a balanced structure using a coplanar-to-microstrip transition to provide a single-ended output. The transition fundamentally functions as a balun.

The performance of the balun is quantified by amplitude and phase imbalance, due to non-idealities of the structure. Maximum values for amplitude imbalance is 1 dB and phase imbalance is 15 degrees as was found in literature [32], which are in line with the values found at the end of Chapter 3. These worst-case numbers are used to evaluate the effect on the performance of the system.

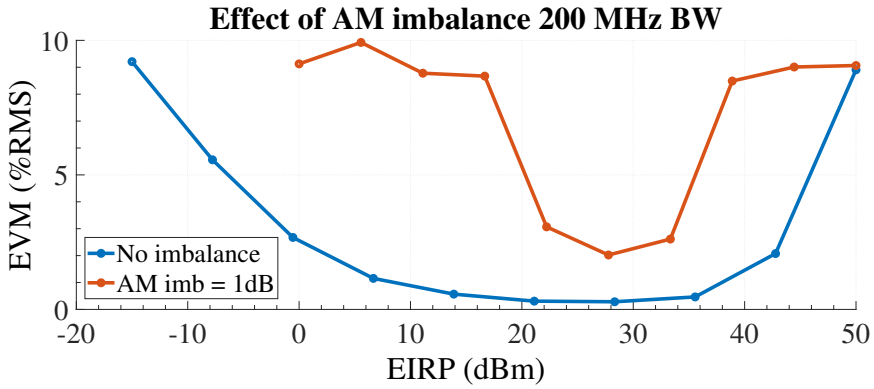


Figure 4.10: Amplitude imbalance influence on the EVM performance of the mixer, the ideal balun has been replaced with a transformer with amplitude imbalance whilst providing the correct input impedance.

The effect of the imbalance is simulated similar to previous analyses. The impact of 1 dB amplitude imbalance is significant for this implementation. An EVM<5% is achieved for input powers $20 \leq P_{in} \leq 33dBm$. Comparing with the previous achieved performance the dynamic range is reduced from 58 dBm to 13 dBm, which is a substantial performance decrease due to 1 dB of amplitude imbalance. This could by resolved by implementing a balun on-chip to ensure low amplitude imbalances. Ideally, across the entire frequency band of interest, this accompanied with adding complexity to the design.

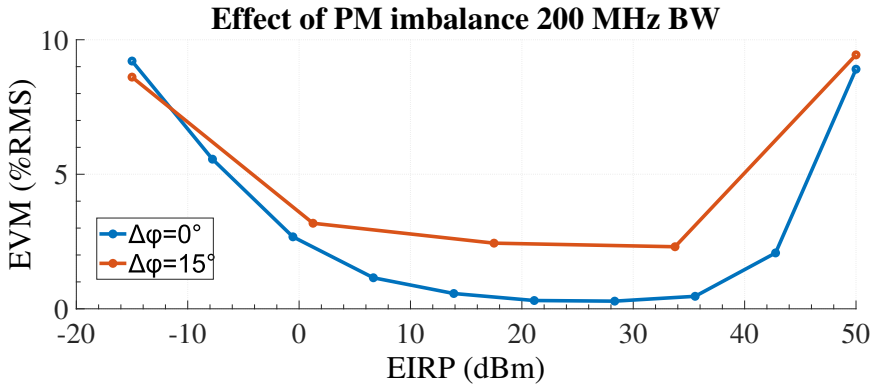


Figure 4.11: Phase imbalance influence on the EVM performance of the mixer, phase shifting components are placed before the diodes with 15 degrees phase difference.

Ideally, the phase difference of the RF applied to the two diodes are 180 degrees out of phase. In this simulation the influence of a phase difference less than 180 degrees is shown. By introducing a phase difference of in total 15 degrees, the maximum difference in EVM performance is 2% between the two cases.

5
Discussion

5.1. Conclusion

This thesis includes research on how to design and implement hardware for the ADome, to enable EVM measurements and the possibilities of optimizing on-chip. In Chapter 2, a hybrid LO distribution topology was chosen including a multiplier and buffer. Two other implementations have been analyzed and were considered less favourable in terms of power and cost budget. The LO distribution analysis resulted in preferring the demodulation in the digital domain and choosing for a heterodyne downconversion. Additionally, guideline numbers for the LO pumping power for the downconverting stage were specified.

In Chapter 3, the design of a single-balanced passive diode mixer in NXP's Qubic4Xi technology is proposed. The mixer is designed to operate between 24 and 40 GHz with a LO drive power of 15 dBm. The device sizing, bias, layout of components and transmission lines are discussed. Furthermore, the impact of connecting the mixer directly to the antenna are discussed.

Chapter 4 presents the post-layout performance of the mixer, achieving a maximum conversion loss of -8.5 dB and SSB noise figure of 10 dB across the band. Good RF-LO and RF-IF isolation of <-40dB is found, partly due to the mixer being simulated using an ideal balun at the input. The LO-IF isolation of -6dB across the band was expected and need to be accounted for when interfacing with e.g. an IF amplifier. This issue could be resolved by implementing a band-pass filter at the output of the mixer, either on-chip or off-chip. Additionally, the phase noise originating from the LO chain is not suppressed by the LO-IF isolation and will have impact on the RX chain.

The lack of a proper LO match deteriorates the mixer performance. This will have significant impact on the LO distribution topology, requiring more power to drive the mixer. Lastly, the linearity of the mixer can be summarized with a P1dB of 2 dB and IIP3 of 18dB. The compression point of the mixer limits the measurement capabilities of the antenna dome for AUTs with higher EIRP levels. The consequences of this are discussed in the last part of Chapter 4.

Performance of the proposed mixer was evaluated using a measurement example in state-of-the-art literature. The guidelines of operating frequency, link distance, and EIRP values were used. A comparison is made between a mixer found in literature with a similar topology and technology and the proposed topology. The mixer from literature has been simulated with simplified performance parameters, however the characteristics of the mixer are identified. The proposed mixer is simulated with device model and passives and show favourable performance for the ADome. Factors such as cables losses and other non-idealities further diminish the performance of the mixer in the system and should be accounted for in further analysis. The impact of imbalance is shown using the same test-bench. Performance of the mixer is deteriorated significantly for worst case scenarios of 1 dB and 15 degrees of amplitude/phase imbalance, respectively.

5.2. Future work

The goal of this work was to identify the critical components to enable EVM measurements for the ADome. However, for evaluating the analysis and implementation of the mixer the analyzed components have to be developed and tested to evaluate the overall performance. Three main subjects for future work are summarized as follows:

- **LO distribution:** The proposed hybrid implementation consisting of a 2x active multiplier can be integrated on a PCB with the mixer to evaluate the performance of the system. The initial analysis in this thesis gives a first impression of the preferred implementation and considerations. Higher integration could be achieved by implementing the active multiplier in the same technology as the mixer. However, this requires more component verification and increases the system complexity, due to the larger amount of sub-components. To illustrate, the off-the-shelf multiplier consisted of a LNA, multiplier and buffer on a single die.

- **Single-balanced passive mixer:** The performance of the mixer can be improved with respect to matching to the LO port, which has less favourable performance compared with other achieved metrics. The transmission line, which was now designed for a 50 ohm load, need to be designed for the impedance present at the LO node of the mixer-core. Optimally, the match would apply for the entire frequency band of interest with a flat response. This work focused on reducing losses by removing the hybrid, however this comes at the cost of LO to RF isolation. When interfacing the antenna directly to the mixer this will result in excitation of the antenna when it is considered as a monopole. Isolation between the mixer and antenna would resolve this issue.

  The mixer core including passive components, interconnects and device models have been included in the simulation results. However, before submitting for fabrication the mixer performance need to be reviewed after implementation of complete DRC. This include ground planes to ensure to comply with the density rules critical for production. The effect the ground plane implementation on circuit performance need to be EM simulated as well. Especially for the LO and IF transmission lines and the corresponding ground planes.

  Implementation of an off-chip or on-chip balun or hybrid is critical for maintaining the performance presented in this work. As was shown at the end of Chapter 4, the system performance is very sensitive for amplitude and phase imbalances and would therefore limit the performance of the setup.

  Lastly, to fully characterize the differential mixer performance, it has to be fabricated and measured. A differential probe setup is required since the mixer is designed with a differential input. Methods to measure conversion gain, noise figure, isolation and linearity need to be developed and investigated to fully characterize the mixer performance.

- **EVM measurements for the ADome:** The link budget analysis and related simulations can be verified using off-the-shelf components with equal performance as proposed in this work. This setup would include a down-converting node close to the antenna and the corresponding LO distribution components. Other factors such as cable losses and phase noise affect the performance of the link and require additional analysis. The requirements set in this thesis have been mainly focused on wide-band, high signal bandwidth requirements as given in the standard. Another option to enable EVM performance for the ADome would be to relax the requirements. For example, demodulation at a fixed frequency and power with a maximum signal bandwidth of 50 MHz could allow for higher integration at the sensing node.

Bibliography

[1] 3rd Generation Partnership Project (3GPP). "NR; Study on test methods". TR 38.810, 2020.

[2] G. Hueber and A.M. Niknejad. *Millimeter-Wave Circuits for 5G and Radar*. The Cambridge RF and Microwave Engineering Series. Cambridge University Press, 2019.

[3] J. D. Dunworth, A. Homayoun, B. H. Ku, Y. C. Ou, K. Chakraborty, G. Liu, T. Segoria, J. Lerdworatawee, J. W. Park, H. C. Park, H. Hedayati, D. Lu, P. Monat, K. Douglas, and V. Aparin. A 28ghz bulk-cmos dual-polarization phased-array transceiver with 24 channels for 5g user and basestation equipment. In *2018 IEEE International Solid - State Circuits Conference - (ISSCC)*, pages 70–72, 2018.

[4] B. Sadhu, Y. Tousi, J. Hallin, S. Sahl, S. K. Reynolds, Ö. Renström, K. Sjögren, O. Haapalahti, N. Mazor, B. Bokinge, G. Weibull, H. Bengtsson, A. Carlinger, E. Westesson, J. E. Thillberg, L. Rexberg, M. Yeck, X. Gu, M. Ferriss, D. Liu, D. Friedman, and A. Valdes-Garcia. A 28-ghz 32-element trx phased-array ic with concurrent dual-polarized operation and orthogonal phase and gain control for 5g communications. *IEEE Journal of Solid-State Circuits*, 52(12):3373–3391, 2017.

[5] David M. Pozar. *Microwave engineering*. Wiley, University of Massachusetts, 2011.

[6] Keysight. OTA Test for Millimeter-Wave 5G NR Devices and Systems White Paper, 2020.

[7] Benoît Derat, Corbett Rowell, and Adam Tankielun. Promises of near-field software and hardware transformations for 5g ota. In *2018 IEEE Conference on Antenna Measurements Applications (CAMA)*, pages 1–4, 2018.

[8] A. Nafe, M. Sayginer, K. Kibaroglu, and G. M. Rebeiz. 2 × 64-Element Dual-Polarized Dual-Beam Single-Aperture 28-GHz Phased Array With 2 × 30 Gb/s Links for 5G Polarization MIMO. *IEEE Transactions on Microwave Theory and Techniques*, 68(9):3872–3884, 2020.

[9] F.A. Musters. "Real-Time 3D Characterization of Antenna Systems". Master's thesis, Technische Universiteit Delft, the Netherlands, 2019.

[10] Tommi Tuovinen, Nuutti Tervo, and Aarno Pärssinen. Analyzing 5g rf system performance and relation to link budget for directive mimo. *IEEE Transactions on Antennas and Propagation*, 65(12):6636–6645, 2017.

[11] Keysight. Using Error Vector Magnitude Measurements to Analyze and Troubleshoot Vector-Modulated Signals, 2000. `https://literature.cdn.keysight.com/litweb/pdf/5965-2898E.pdf`.

[12] M. Vigilante, E. McCune, and P. Reynaert. "To EVM or Two EVMs?: An Answer to the Question". *IEEE Solid-State Circuits Magazine*, 9(3):36–39, 2017.

[13] Behzad Razavi. *RF Microelectronics (2nd Edition) (Prentice Hall Communications Engineering and Emerging Technologies Series)*. Prentice Hall Press, USA, 2nd edition, 2011.

[14] Bert Henderson. *Microwave Mixer Technology and Applications*. Artech House, 2013.

[15] Earl McCune. *Practical digital wireless signals*. Cambridge University Press, 2010.

[16] Yusheng Yin, Berktug Ustundag, Kerim Kibaroglu, Mustafa Sayginer, and Gabriel M. Rebeiz. Wideband 23.5–29.5-GHz Phased Arrays for Multistandard 5G Applications and Carrier Aggregation. *IEEE Transactions on Microwave Theory and Techniques*, 69(1):235–247, 2021.

[17] Greg LaCaille, Antonio Puglielli, Elad Alon, Borivoje Nikolic, and Ali Niknejad. Optimizing the LO Distribution Architecture of mm-Wave Massive MIMO Receivers, 2019.

[18] F. Marki. Mixer basics primer‘. Marki Microwave, Morgan Hill, CA„ 2010.

[19] Bert Henderson and Edmar Camargo. *Microwave Mixer Technology and Applications*. Artech House, 2013.

[20] Mahsa Keshavarz Hedayati, Abdolali Abdipour, Reza Sarraf Shirazi, Max J. Ammann, Matthias John, Cagri Cetintepe, and Robert Bogdan Staszewski. Challenges in on-chip antenna design and integration with rf receiver front-end circuitry in nanoscale cmos for 5g communication systems. *IEEE Access*, 7:43190–43204, 2019.

[21] Vadim Issakov, Herbert Knapp, Marc Tiebout, Andreas Thiede, Werner Simburger, and Linus Maurer. Comparison of 24 ghz low-noise mixers in cmos and sige:c technologies. In *2009 European Microwave Integrated Circuits Conference (EuMIC)*, pages 184–187, 2009.

[22] Rongsheng Bao, Shengyu Rao, Chunqi Shi, Jinghong Chen, Guangsheng Chen, and Runxi Zhang. A ka-band high-gain and wideband mmw down-conversion mixer for 5g communication applications. In *2020 IEEE 15th International Conference on Solid-State Integrated Circuit Technology (ICSICT)*, pages 1–3, 2020.

[23] V. Issakov, H. Knapp, M. Wojnowski, A. Thiede, and W. Simbuerger. "A 22-39 GHz passive mixer in SiGe:C bipolar technology". In *2010 IEEE MTT-S International Microwave Symposium*, pages 1–1, 2010.

[24] Li Zhongpu, Dai Xiu, Wei Liutai, Sun Jiawen, and Liu Jinxian. Design of a ka -band double balance mixer based on the marchand balun. In *2015 12th IEEE International Conference on Electronic Measurement Instruments (ICEMI)*, volume 02, pages 939–942, 2015.

[25] Stephen A. Maas. *Microwave Mixers*. Artech House, 1993.

[26] George D. Vendelin, Anthony M. Pavio, Ulrich L. Rohde, and Matthias Rudolph. *Microwave Circuit Design: Using Linear and Nonlinear Techniques*. John Wiley & Sons, Inc., second edition, 2005.

[27] Stephen A. Maas. *Nonlinear Microwave and RF Circuits*. Artech House Published, 2nd edition, 2003.

[28] C. Lien, C. Wang, C. Lin, P. Wu, K. Lin, and H. Wang. Analysis and Design of Reduced-Size Marchand Rat-Race Hybrid for Millimeter-Wave Compact Balanced Mixers in 130-nm CMOS Process. *IEEE Transactions on Microwave Theory and Techniques*, 57(8):1966–1977, 2009.

[29] Pei-Si Wu, Chin-Shen Lin, Tian-Wei Huang, Huei Wang, Yu-Chi Wang, and Chan-Shin Wu. A millimeter-wave ultra-compact broadband diode mixer using modified marchand balun. In *European Gallium Arsenide and Other Semiconductor Application Symposium, GAAS 2005*, pages 349–352, 2005.

[30] H. Hu, F. Chen, J. Qian, and Q. Chu. A Differential Filtering Microstrip Antenna Array With Intrinsic Common-Mode Rejection. *IEEE Transactions on Antennas and Propagation*, 65(12):7361–7365, 2017.

[31] H. J. Ng, M. Jahn, R. Feger, C. Wagner, and A. Stelzer. An efficient SiGe double-balanced mixer with a differential rat-race coupler. In *2013 European Microwave Conference*, pages 1551–1554, 2013.

[32] C. Marki and D. Jorgesen. *Balun Basics Primer*. Marki Microwave, Inc., 2014.