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M.Sc. THESIS

Wideband Class B Power Amplifier Topologies

by
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Abstract

Wireless communication has encountered a tremendous growth over the past few decades. The increased plurality in communication standards, characterized by the use of different operating frequencies and data rates, has translated into very tough specifications for the broadcasting base station power amplifier, in terms of efficiency, bandwidth and linearity. For this reason, currently many high efficiency power amplifier concepts are investigated for their suitability to handle the upcoming generations of wireless communication standards.

At this moment the Doherty power amplifier (DPA) is a popular concept, which gives good efficiency in the power back-off, making it a suitable choice when dealing with signals that have a high peak-to-average power ratio. To be efficient in power back-off operation, the Doherty power amplifier is composed out of two linear amplifiers with an impedance inverter as an output power combiner. Due to its high complexity, the traditional Doherty amplifier is limited for its RF bandwidth. In view of this, the objective of this thesis is to design a linear wideband class-B power amplifier cell which allows incorporation in the DPA. For this purpose an LDMOS based push-pull topology together with baluns (implemented by bondwires) at the input and output of the transistors has been adapted. The described topology helps to achieve an orthogonal relation between the fundamental path and its second harmonic, resulting in wideband high efficiency operation. The resulting amplifier provides an output power of 60 W with a power added efficiency greater than 48% over a relative bandwidth of 40% centered around $1.8GHz$.

Advisor: Dr.Ir. L.C.N. de Vreede, Microelectronics, TU Delft

Chairperson:

Member:

Member:

Member:

To my parents and grandparents

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1 Introduction

Motivation and Objective

Mankind has made tremendous progress in the field of mobile communication. The fact that life nowadays is difficult to imagine without mobile phones is a testament to this. This progress would not have been possible without the enormous developments in the supporting infrastructure required for wireless communication. Base stations are the most critical components in this supporting infrastructure. They facilitate the communication between cell phones and network providers. It has been forecasted that the cellular base station shipment will grow to 13.4 million units in 2013 [2]. Hence, a lot of research focus is now being placed on designing cost-effective and high performance base-stations. The block diagram of a typical base station is shown in Figure 1.1 as taken from [4].

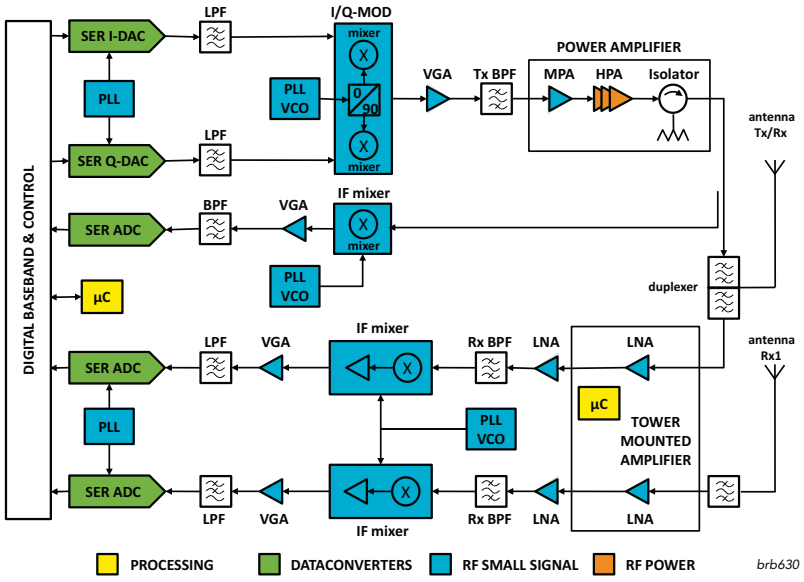

Figure 1.1: Block diagram of a base station transceiver system [4]

High power RF power amplifiers are an integral part of a base station transceiver system. They are used to amplify the transmit signals to the end users in the unit cell assigned to that base station. These transmit signals have a high power level in order to compensate

for the environmental losses in the transmit path. The performance in terms of efficiency, output power, operation bandwidth of a power amplifier and its cost are important drivers in base station design.

Currently, the fast growing wireless market is characterized by a plurality of various communication standards like GSM, W-CDMA, UMTS or WiMAX, which operate in different frequency bands (900 MHz, 1800 MHz, 2100 MHz, 3500 MHz, etc.) [17]. The modern communication standards utilize varying envelope signals with high peak to average ratios (PAR), e.g $> 10.5dB$ for W-CDMA, resulting in high linearity and efficiency requirements for the power amplifier [33]. High efficiency is also required for eco-friendly operation and to cut down cooling/operational costs. The high data rates in these various communication standards make both video bandwidth as well RF operating bandwidth important requirements in the design of a power amplifier. A power amplifier which can be designed to operate multi-band, multi-mode would decrease the number of power amplifier modules required to cover the entire application spectrum, resulting in a low-cost and area-efficient implementation of a base station unit.

The amplifier requirements for linearity, efficiency and bandwidth are key concerns in the wireless research community and are chosen as the topic of focus in this thesis. In view of this, Doherty amplifiers consisting of a main and peaking amplifier are currently adopted in base station applications to relax the efficiency penalty related to the high PAR of the signals, as it provides good efficiency at power back-off region [12]. The main and the peaking amplifier in this system are usually linear power amplifiers biased in class AB/class B configuration. It has been concluded in [20] [11] that these amplifiers cause bandwidth limitations of the whole system. To overcome this limitation, the objective of this thesis is to implement a wideband class B power amplifier cell (60 W) which can be utilized in a Doherty system. For this purpose, a push-pull topology is investigated and compared to the classical single-ended class B topology. Special attention is given to the practical implementation, which requires balun structures at the input and output to convert the single-ended signal to a differential signal and vice versa. These balun structures and the required matching networks are preferably included inside the package of the power device. Consequently, the use of bondwire structures is considered to achieve a low loss compact design implementation. All the design work and implementation has been done in collaboration with NXP semiconductors.

For the definition of various performance metrics like drain efficiency, power added efficiency (PAE) etc; one can refer to Appendix A.

Thesis Organization

The thesis is organized as follows:

- Chapter 2 introduces power amplifiers in two groups, namely the transconductance and switch-mode power amplifiers. A detailed analysis of the class B power amplifier is carried out, stating the loading conditions which are required for high

efficiency. It also introduces the class J power amplifier, which has different loading conditions than class B but an efficiency performance similar to the class B configuration.

- Chapter 3 analyses the bandwidth and efficiency for the class B/class J configurations. A load pull simulation is carried out to plot efficiency for different loading conditions at the fundamental and the 2^{nd} harmonic. A class J-class B-class J* continuum is observed in this plot providing high efficiency over a large impedance range, which gives rise to new possibilities for wideband operation. The implementation aspects are also discussed by analyzing the classical single-ended topology to find the maximum bandwidth it can provide. It is concluded that its bandwidth performance is limited due to the interaction in the circuit implementation between the fundamental and the 2^{nd} harmonic termination.

- Chapter 4 introduces the push-pull topology with baluns at the input and the output that helps in the orthogonalization of the fundamental (differential signal for the balun) and the 2^{nd} harmonic (common mode signal for the balun) signal path solving the issue of limited bandwidth. The transistors in this design are implemented using LDMOS devices from NXP semiconductors. The huge device parasitic capacitances of the active device are used to short the 2^{nd} harmonic while a model is developed for the balun whose parameters are designed to provide an optimum load at the fundamental over the operating frequency band. The design of the matching network is also described with focus not only on obtaining high bandwidth, but also to solve issues like stability. Also, a biasing scheme is introduced in this chapter to achieve low memory effects.

- Chapter 5 covers the implementation aspects of the various components described in Chapter 4, like the balun and the input and output matching networks. The implementation procedure is divided into two parts: the first part consists of an in-package design which includes the LDMOS die, the input and output balun, bias network and a pre-match; while the second part is an external PCB design on which the package lands, and which consists of transmission line type matching network continuing the pre-match network and the external decoupling for biasing. The above implementation results in a compact design. Two designs with differences in their input matching network are implemented based on the above concept. The simulation results are also provided for the same.

- Chapter 6 briefly introduces the Doherty power amplifier (DPA) concept. A basic simulation is carried out with ideal push-pull and single-ended topology replacing the main and peak amplifiers of a DPA to compare the bandwidth performance in the two cases.

- Chapter 7 presents the important conclusions drawn during the design of the power amplifier. A few possible recommendations and future work are also described in this chapter.