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# Influence of the Magnetic's Parasitic Capacitance in the switching of High-Voltage Cascode GaN HEMT

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***Abstract*— In this paper, the influence of the parasitic capacitance of a magnetic component (inductor or transformer) on the switching of 600V cascode GaN HEMT devices is investigated. An analytical switching model is used to analyse the influence and the results are verified by means of an experimental double pulse tester setup. Furthermore, the influence of replacing the diode of the switching cell with an active GaN HEMT switch is analysed in combination with the parasitic capacitance of the magnetic component.**

***Keywords*— Gallium Nitride (GaN) high electron mobility transistor (HEMT), cascode configuration, double-pulse tester (DPT), parasitic capacitance**

## I. INTRODUCTION

In the past few years, there has been a general trend in the area of power conversion to higher power densities while maintaining high efficiencies, mainly driven by reduced weight/space in applications like automotive, aircrafts [1], and microprocessors [2]. Advancements in power electronics have contributed towards the realization of that demand, by introducing lightweight, high-power density and highly efficient in harsh environment power electronics. The increase in power density of power electronic systems has been made feasible primarily by developments in the semiconductors field, namely by semiconductors that can operate at higher switching frequencies and generate less power loss. Another step towards higher power densities is to utilize appropriate circuit topologies, as they can reduce the stress upon the components and the cooling requirements.

For many years, silicon-based power devices have managed to monopolize the power electronics applications, but as the need for devices with higher voltage and switching frequency capability is growing, they start reaching a limit. Gallium Nitride (GaN) power semiconductors have emerged as a possible candidate to replace the silicon-based devices, by offering potential benefits for high frequency power conversion, due to their intrinsic material properties. Due to their material advantages, GaN features a wide bandgap, high electron mobility and high electron velocity, allowing devices to switch faster and with lower switching loss [3][4].

GaN HEMTs can be categorized, based on their physical structure, into normally-off (enhancement mode) and normally-on (depletion mode) device. Although the enhancement mode GaN HEMTs present the desirable feature of gate drive overprotection [9], their application is limited due to critical driving considerations [4]. On the other hand, in high voltage depletion mode GaN HEMTs, the driving circuit can operate in a voltage range between -30V to 2V and -5V is required to fully turn-on ensuring a sufficient safety-driving margin. However, as a normally-on device, it is conducting in the absence of applied voltage, which means that the driving circuit has to operate before the input voltage is applied on the devices.

In order to easily use a high-voltage depletion mode GaN transistor, a low voltage Si MOSFET is used to drive the high voltage GaN transistor, which is well known as a cascode structure (Fig. 1) and helps to generate a normally-off condition from a normally-on device [10]. The principle of this configuration is quite straightforward as only the low voltage Si MOSFET is actively controlled while its drain-source voltage acts as a control for the GaN HEMT. Specifically, the GaN HEMT's gate is connected to the Si MOSFET's source, causing its drain-source voltage to become the negative gate-source voltage of the GaN HEMT required to pinch off its channel. The cascode configuration makes the device compatible with standard Si drivers.

High-voltage 600V cascode GaN HEMT by Transphorm is currently supplied in two packages: the TO-220 and the PQFN 8x8 [5]. As the switching frequency is pushed up to the MHz range, the switching behavior of the device is not only influenced by the GaN die, but the device package's along with circuit's parasitic inductances will deteriorate the switching transitions eventually increasing the switching loss [6][7]. Moreover, the junction capacitance introduces significant loss under hard-switching conditions, especially in bridge configuration.

As the package and circuit parasitics set a limit on increasing the switching frequency in hard switching topologies with GaN converters, topologies where these parasitics are utilized, will be required at MHz switching frequency [8]. However, at very high switching frequencies, the parasitic elements like the self-capacitance of magnetic components, such as inductors and transformers, may have a substantial impact on the switching behavior of the devices.

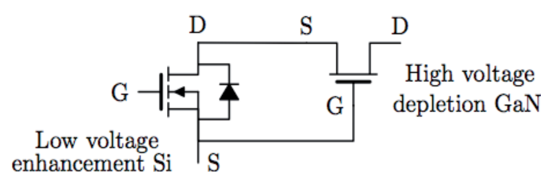


Fig. 1. GaN HEMT in cascode configuration

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This paper investigates the switching behavior of the high-voltage cascode GaN HEMT and the influence of the inductor's equivalent parasitic capacitance (EPC) on this behavior.

## II. Evaluation Of 600V GaN HEMT Switching Characteristics

The evaluation of the switching behavior and the influence of the inductor's EPC on this behavior will be made both theoretically by means of an analytical loss model and experimentally by a double-pulse tester (DPT). A 600V/17A GaN HEMT (TPH3006LS, 8x8PQFN package) from Transphorm is used as the device under test (DUT). The parameters of the device are shown in Table I. A SiC Schottky diode (C3D04060A) will be used as top switch.

TABLE I.
Parameters of TPH3006LS (Cascode GaN HEMT from Transphorm Inc)

| **Parameters** | **TPH3006LS** |
|---|---|
| $V_{ds_max}$ (V) | 600 |
| $R_{ds_on}$ (Ω) | 0.15 |
| $Q_g$ (nC) | 6.2 |
| $Q_{rr}$ (nC) | 54 |
| $Q_{o_tr}$ (pF)/$Q_{o_er}$ (pF) | 105/64 |

### A. Analytical loss model

The analytical model developed for the evaluation of the cascode GaN HEMT is based on the model proposed in [11]. This model includes the parasitic inductors of the device package and the circuit, and the parasitic capacitors of the devices and the load inductor. A typical diagram of the cascode GaN HEMT can be seen in Fig. 2, where inductances $L_g$, $L_d$, and $L_s$ represent the inductance of the package lead frames, and inductances $L_{int1}$, $L_{int2}$, and $L_{int3}$ represent the interconnections between the GaN die, the Si die and the lead frames. A PQFN package was used that eliminates the inductance $L_s$ [7] and $L_g$, $L_d$ are the inductors connecting the dies to the corresponding package pads. The parasitic inductors induced by the PCB are denoted as $L_{dr_loop}$ for the driving loop inductance and $L_{p_loop}$ for the power loop inductance.

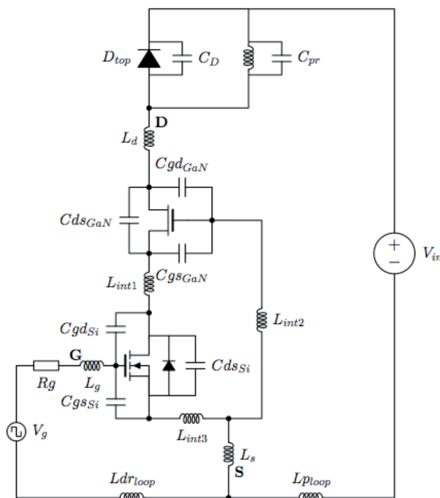


Fig. 2. Equivalent circuit to analyze the switching loss of the cascode GaN HEMT

The package and layout inductances are summarized in Table II.

TABLE II.
Parasitic inductance of package and PCB layout

| Package | | | | | Layout | |
|---|---|---|---|---|---|---|
| $L_g$ | $L_d$ | $L_{int1}$ | $L_{int2}$ | $L_{int3}$ | $L_{dr_loop}$ | $L_{p_loop}$ |
| 3nH | 1.2nH | 0.1nH | 0.15nH | 0.2nH | 8nH | 17nH |

Including the parasitic inductors of the package and circuit makes the mathematical calculations very complicated, thus the non-linearity of the parasitic capacitors of the DUT ($Cds_{GaN}$, $Cgd_{GaN}$) and the top diode ($C_D$) will be modeled with an assumption. An equivalent value for these capacitors is derived during each stage of the transitions based on the drain-source voltage range of the DUT. Moreover, the inductor's EPC ($C_{pr}$) is effectively in parallel with the $C_D$, as can be seen in Fig. 2, and it will be added to it as it is expected to have the same effect.

The stages for turn-on switching transition (Fig. 3) can be found in [11] and they are calculated as stated, except from stage V. During this stage, a part of the DUT current provides the inductor current $I_d$ and additional current charges the $C_D$ and $C_{pr}$. As the voltage across the diode starts to rise, the DUT's drain-source voltage ($V_{ds}$) decreases. In order to more accurately model this simultaneous change of these capacitors, stage V is divided into two sub-stages with the same equations but with different values of the capacitors. The first sub-stage is calculated from the total capacitive charge of the diode (8.5nC in the case of the used diode) that is contributed to the $I_d$. When the current reaches this value, the second sub-stage starts and different values for the parasitic capacitors are used, as the $V_{ds}$ will decrease to zero at the end of this stage. After the $V_{ds}$ reaches zero, the $C_D$ and the $C_{pr}$ will resonate with the parasitic inductances in the circuit and the current ringing period will begin (the equivalent circuit and equation of stage VI can be found in the Appendix). The stages are shown in Fig. 3 as the DUT is switching with 400V/5A, where the blue waveform is the drain-source voltage of the DUT and the green is the drain-current.

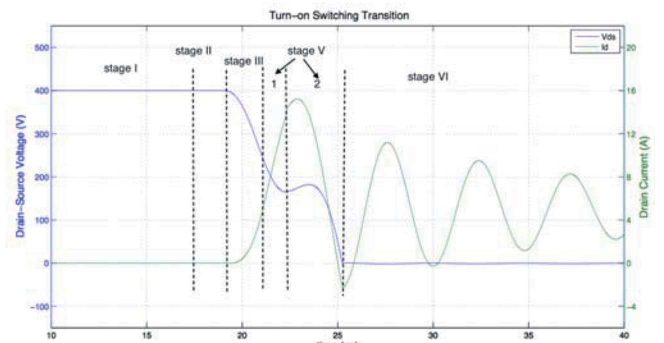


Fig. 3. Stages during turn-on switching transition

The stages for the turn-off switching transition can again be found [11] and calculated as stated, while the $C_{pr}$ is added to the $C_D$, where it is applicable. The waveforms are shown in Fig. 4 as the DUT is switching at the same conditions as during the turn-on. The channel current determines the stage III of the turn-off transition, thus is also shown (red waveform). Moreover, stage V is added in order to model

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the voltage and current ringing period (the equation used during stage V can be found in Appendix).

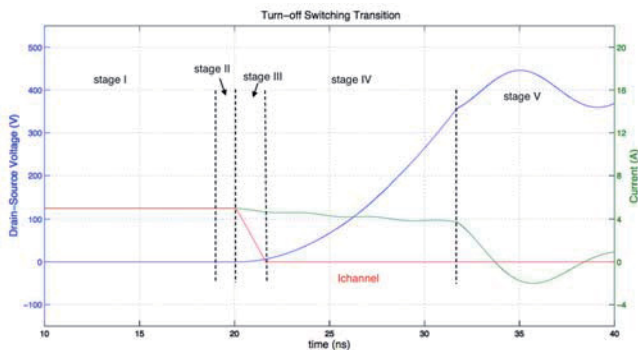


Fig. 4. Stages during turn-off switching transition

## B. *Test Setup for Switching Characterization*

The switching performance of the DUT is investigated experimentally with a DPT (Fig. 2), under clamped inductive load condition. Based on the results, a basis for the power converters' design can be provided, regarding the switching frequency, dead time, and efficiency estimation [12][13].

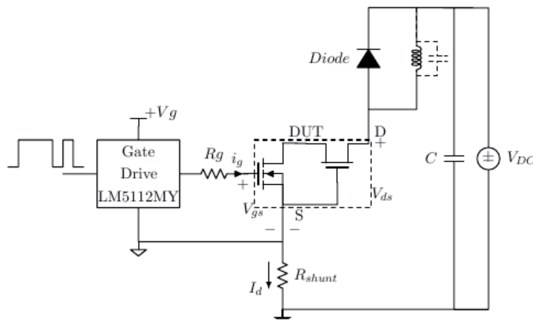


Fig. 5. Double pulse tester circuit schematic

The DPT circuit board was constructed on a four layer printed circuit board (PCB) integrating the dc bus, the switching phase leg, the gate drive circuit, the dc bus bulk aluminum electrolytic capacitors, the film and the ceramic capacitors, the DUT and the top switch, the measuring probes and the inductor into a single board (Fig. 3). The DUT is driven by a high-speed, high-current gate driver LM5112MY from Texas Instruments, with gate voltage from 0V to 10V. The TMS320F28069 Piccolo Microcontroller from Texas Instruments is used to control the circuit's operation by providing a double-pulse signal to the gate driver as shown in Fig. 2.

The inductive load was designed in such a way as to minimize its EPC. It is composed of two inductors, with one layer of windings and space between the turns achieving an EPC of 2pF.

In order to fully characterize the switching transition of the DUT, measurements of the gate voltage ($V_{gs}$), drain-source voltage ($V_{ds}$) and drain current ($I_d$) are needed, to determine the switching time, *di/dt*, *dv/dt* and switching losses of the device. However, the gathering of accurate measurements can be very challenging when measuring high frequency waveforms, due to the very fast current and voltage rates of change [14][15].

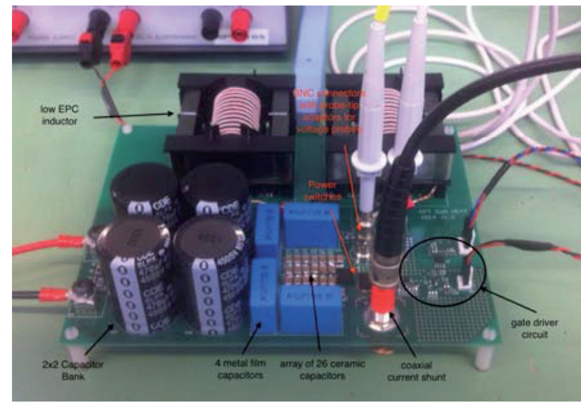


Fig. 6. Double pulse tester hardware

A 0.1Ω shunt resistor with a bandwidth of 2GHz (SSDN-10) manufactured by T&M Research is used to measure the $I_d$, while the $V_{gs}$ and $V_{ds}$ are measured with the Yokogawa 701939 600V, 500MHz, 10x passive probes. The voltage probes are connected to the test point trough a probe-tip adaptor and BNC connector. The probe-tip adaptor is placed in the BNC connector and allows the probe tip to get connected directly to the test point, while the outer barrel of the adaptor makes a direct and short ground contact. The three measurements share the common point of the DUT source terminal, which is also used as ground of the voltage probes. Thus, the $I_d$ needs to be flipped in the scope to get the correct waveform.

Considering that the GaN HEMT devices are characterized by high switching-speed capability, the challenges for switching characterization of the DUT primarily lies on the layout design of DPT board and precision measuring of the switching waveforms.

# III. Verification of the Analytical Model

The verification will be divided into two parts: first, the switching behavior of the GaN HEMT with no additional capacitance in parallel with the low EPC inductor is examined. Second, ceramic capacitors of 22pF, 56pF, 78pF, and 100pF will be soldered close to the inductor modeling inductors with bigger EPC, in order to investigate its influence on the GaN HEMT's switching behavior.

## A. *GaN HEMT switching behavior*

The DUT is subjected to switching conditions of 400V/5A. The waveforms are recorded for a time interval of 100ns and Fig. 7 shows the waveform comparison between the double-pulse tester and the calculated results of the developed analytical model for both turn-on and turn-off switching transitions.

It can be seen that the analytical model is able to match the experimental results on the voltage and current slope rates, and the main transition times. However, during the turn-on process, the $V_{ds}$ drops faster in the beginning and increases again to match the falling of the experimental waveform. This is caused due to the discrete values of the parasitic capacitances used in each stage of the transition modeling the non-linearity of these capacitances. For the same reason, there is a slight difference between the modelled and measured value of the current overshoot. Next, the oscillation frequencies and damping effects have been predicted reasonably well, but they present differences

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due to inaccurate high-frequency parasitic inductance and stray resistance of the circuit.

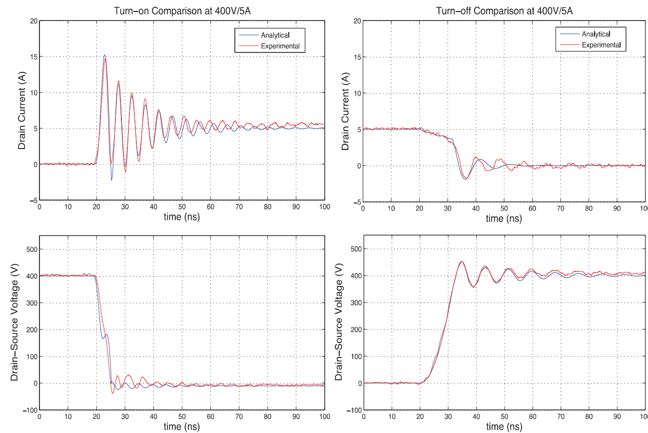


Fig. 7. Turn-on/off switching waveforms comparison at 400V/5A

Additionally, the energy dissipation during the turn-on/off transitions is calculated and compared in Fig. 8. The energy dissipation is calculated by integrating the product of the drain-source voltage and the drain current. However, it is important to note that integrating the $V_{ds}$ and the $I_d$ does not represent the real turn-on and turn-off loss. During turn-on process, the junction capacitance of the DUT ($C_{oss}$) is discharged through the channel of the device, causing the channel current to deviate from the drain current measured on the device terminals. During the turn-off process, this capacitance is being charged by drawing part of the load current, causing the channel current to be smaller than the drain current. Consequently, in a DPT, the turn-on loss derived from the waveforms is underestimated while the turn-off loss is overestimated. On the other hand, the sum of the turn-on and turn-off energy can be used to predict the switching loss in one switching cycle [14].

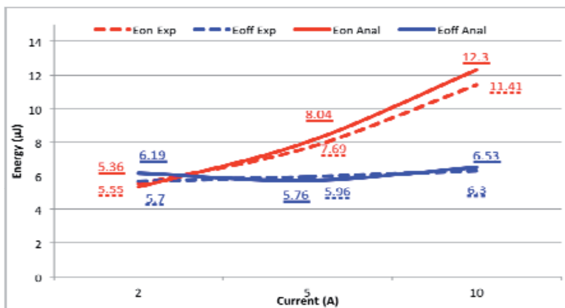


Fig. 8. Switching energy comparison between experimental & calculated results from the analytical model

During the turn-on switching transition, the $C_D$ is being charged, increasing the current overshoot of the DUT. When the charging process is over, the $I_d$ returns to the inductor's current with high di/dt, triggering oscillation to the circuit. As the DUT is already on, the oscillation is caused by the power loop inductance resonating with the $C_D$. According to Fig. 8, turn-on energy a strong function of the inductor's current. During turn-off switching transition, the $C_{oss}$ is being charged by drawing part of the inductor's current and the $V_{ds}$ increases. In the meantime, the $C_D$ is discharged by also drawing part of the inductor's current and the voltage across it drops to zero [14]. As the value $C_D$ is smaller than the $C_{oss}$, it is expected to discharge faster and the voltage across the diode to drop to zero before the drain-source voltage of the GaN HEMT increase to the dc bus voltage. This can be seen in Fig. 4 at the end of stage IV. At this moment, the value of the transistor's current will determine the remaining energy of the parasitic inductors [11] and it will eventually trigger oscillation to the circuit. The power loop inductance resonating with the $C_{oss}$ causes the oscillation, and since the $C_{oss}$ is bigger than the $C_D$ the oscillation frequency during turn-off is smaller. Next, the turn-off energy stays almost constant under different values of the inductor's current, due to the unique intrinsic current source mechanism of the GaN HEMT [6].

### *B. Influence of the inductor's EPC*

The waveforms are recorded for a time interval of 200ns and the same conditions. Fig. 9 shows the waveform comparison between the DPT and the calculated results of the developed analytical model for both turn-on and turn-off switching transitions for an EPC of 100pF.

It can be seen that the analytical model is able to match the experimental results on the voltage and current slope rates, especially during turn-off. The modelled drain current peak is however higher than the measured value. The current reaches a higher peak value and then drops faster to zero triggering oscillations to the circuit. This is caused because in the analytical model, the total capacitive charge of the top switch is used to calculate the peak value of the current and the value of the EPC is added to that charge.

Finally, the oscillation frequencies and damping effects are predicted reasonably well, however there are deviations due to inaccurate high-frequency parasitic inductance and stray resistance of the circuit. Despite the inaccuracies and the assumptions of the model, the switching energy calculated with the analytical model seems to match well the experimental results, as it is shown in Fig. 10.

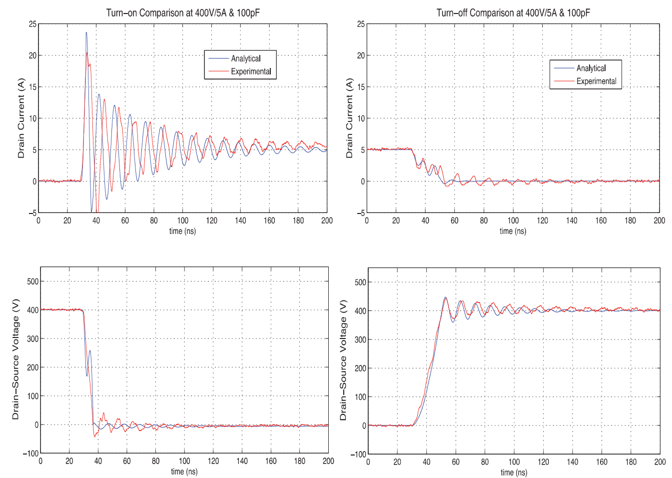


Fig. 9. Turn-on/off switching waveforms comparison at 400V/5A & EPC 100pF

The overshoot in the current during the turn-on process is created now by two capacitive current contributions: the capacitive current necessary for charging the $C_D$ and the other one is originated from the inductor's EPC. It is shown in Fig. 11 that as the value of the EPC increases so does its contribution the DUT's current overshoot. The drain current increases from 14.6A to 20.8A and the time required for

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drain-source voltage to drop to zero is increased from about 5ns to 7ns.

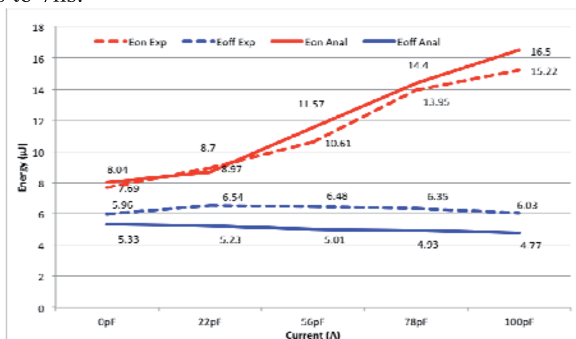


Fig. 10. Switching energy comparison between the experimental & calculated results from the analytical model as the EPC increases

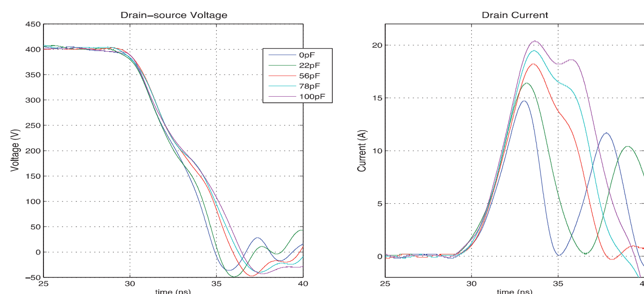


Fig. 11. Influence of the inductor's EPC on the turn-on switching transition

As the current overshoot increases, the Id returns to the inductor's value with a higher di/dt triggering oscillations to the circuit causing the envelop of the oscillation to increase (Fig. 9). Since the DUT is already on, the ringing current will be caused by the switching power loop inductance resonating with the $C_D$ in parallel with the inductor's EPC. Thus, the frequency of oscillations decreases as the EPC increases. During the turn-off transition, the inductor's EPC is in parallel with the $C_D$ and they are both getting discharged by drawing part of the inductor's current. Thus, the drain-source voltage increases slower, as the EPC increases.

## IV. Influence of the Top Switch Reverse Recovery

The DUT is subjected to the same switching conditions but the top switch is replaced by a cascode GaN HEMT. The gate resistance for this set of experiments is 14Ω for turn-on and 0Ω for the turn-off process and the waveforms are shown in Fig. 12.

In this case, the $Q_{rr}$ of the top device together with the charging of its junction capacitance ($C_{topGaN}$) increases the current overshoot of the DUT during the turn-on transition. Additionally, the $Q_{rr}$ of the top device increases the switching transition compared with the previous case. As the $C_{topGaN}$ is bigger than $C_D$, more time is required of its voltage to drop to zero during the turn-off transition. The Id is smaller and, thus, the remaining energy of the parasitic inductors causing no voltage overshoot and making the transition smoother than in the previous case.

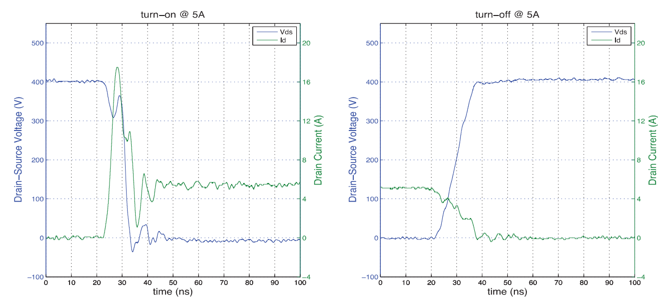


Fig. 12. Switching waveforms at 400V/5A with a GaN HEMT as a top switch

In order to compare the influence of the top switch on the DUT's switching behavior, the switching energies are defined and calculated based on the switching waveforms.

In the first case the turn-on energy is 7.69µJ and increases to 31.54µJ in the second case. The turn-off switching energy is 5.96µJ and 7.11µJ, respectively. It can be concluded that applying an applying an active switch with $Q_{rr}$ and bigger junction capacitance will eventually deteriorate the switching transition and significantly increase the turn-on switching loss which is dominant in the case of this cascode GaN device.

### *A. Influence of the inductor's EPC*

The influence of the inductor's EPC on the GaN HEMT's switching behavior is investigated again by soldering ceramic capacitors of 22pF, 56pF, 78pF, and 100pF close to the inductor load.

As the impact of the inductor's EPC is basically added to the one of the $C_{topGaN}$, the overshoot of the turn-on current will be caused by the reverse recovery effect, the charging process of the $C_{topGaN}$ and the current originated from the inductor's EPC. However, the $C_{topGaN}$ along with the inductor's EPC will start getting charged after the reverse recovery process is complete. This can be seen in Fig. 13, where the first peak of the current waveform is constant, so the $Q_{rr}$ controls it, while the second peak changed with the value of the EPC.

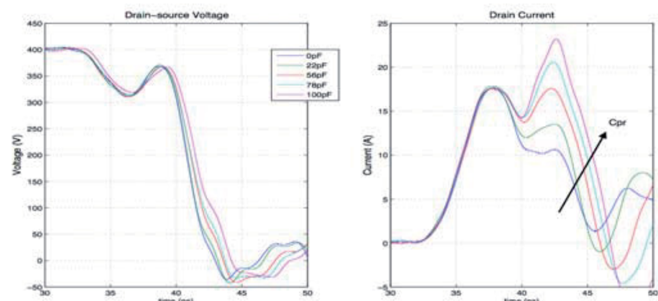


Fig. 13. Influence of the inductor's EPC on the turn-on switching transition

As the EPC's value increases so does the current overshoot. This causes the envelope of the oscillations to increase but the frequency of the oscillation to decrease, as discussed in the previous case. The turn-off process is not significantly influenced, but for the same reason as mentioned in the previous case, the voltage increases slower as the EPC increases.

In order to better understand the influence of the inductor's EPC on the switching behavior of the DUT, the energy dissipated during the turn-on/off switching transitions is calculated and presented in Fig. 14.

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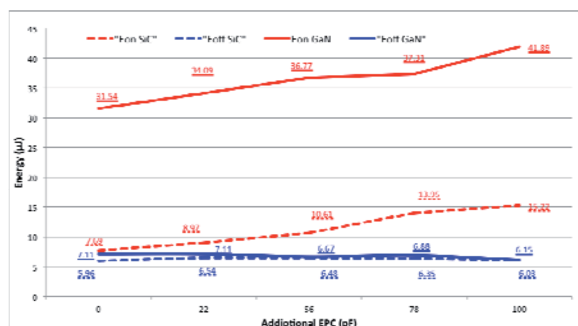



Fig. 14. Comparison of the dissipated energies during the switching transitions for both examined cases

During the turn-on transition, the inductor's EPC constitutes another capacitive contribution to the drain current's overshoot. Therefore, as the inductor's EPC increases, so the does the current overshoot and the switching transition. The combination of these two causes the turn-on switching energy to increase with the increase of the EPC. On the other hand, the turn-off transition does not change significantly and this can be verified by the calculated dissipated energy.

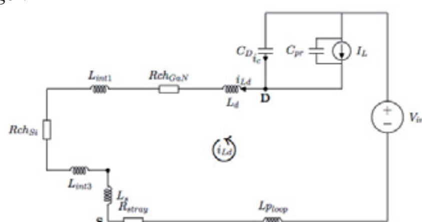
## V. CONCLUSION

This paper investigates the influence of the parasitic capacitance of the magnetic components (inductors or transformers in a dc/dc converter) on the switching performance of the high-voltage 600V cascode GaN HEMT. This is done by means of an analytical loss model that includes the parasitic inductances of the device package and the circuit and the parasitic capacitors of the devices and the load inductor. It is shown that even a small value of 100pF could significantly deteriorate the switching behavior of the DUT while in practical applications this value can be in the order of several hundred pF or more. Thus, the impact of the magnetics' EPC should be carefully taken into consideration by the circuit designers when working with these otherwise fast switching devices. The waveforms are presented during the turn-on/off switching transitions and the accuracy of the developed model is verified experimentally by a double-pulse tester.

Furthermore, it is shown that applying an active switch with reverse recovery charge and bigger junction capacitance will deteriorate the switching transition and significantly increase the turn-on switching loss. Moreover, the increased value of the inductor's EPC, not only will double the turn-on switching loss in the case of SiC Schottky diode and by about a third for the case of the GaN HEMT, but it will also cause the transistor's current to oscillate after the device is fully on.

## APPENDIX

*Turn-on: stage VI*



$$(L_{int1} + L_{int3} + Ld + Ls + Lp_{loop})\frac{di_{Ld}}{dt} + (Rch_{Si} + Rch_{GaN} + R_{stray})i_{Ld} + \frac{1}{(C_D + C_{pr})} \cdot \int (i_{Ld} - I_L)dt = V_{in}$$

*Turn-off: stage V*

$$(Ld + Ls + Lp_{loop})\frac{di_{Ld}}{dt} + (Rch_{Si} + Rch_{GaN} + R_{stray})i_{Ld} + \frac{1}{C_{ringing}} \cdot \int (i_{Ld})dt = V_{in}$$

,where $C_{ringing}$ is the $Cds_{GaN} + Cds_{Si} + Cgd_{Si} + C_{pr}$.

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