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3.4 An Ultrasound-Powering TX with Standing-Wave Peak Tracking Employing Adiabatic Power Sensing Achieving 82% Power-Tracking Accuracy and <90ms Settling Time for Brain Implants

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Abstract

An ultrasound powering TX ASIC for brain implants with autonomous on-chip standing-wave peak tracking for RX power (PDL) regulation is presented. With a proposed adiabatic power-sensing scheme, the TX consumes 43µW for power tracking, and the system achieves a settling time of <90ms while using the standing-wave peak-tracking FSM. The TX can achieve PDL improvement of up to 2.7× with a power-tracking accuracy of 82%.

State-of-the-art intracortical brain-computer interfaces rely on implants on the cortex surface to achieve selective neural recording and stimulation [9]. Wireless powering replaces wires penetrating the dura (a membrane above the cortex), thus enabling safe and long-term sub-dural implantation (Fig. 3.4.1). To increase the powering-link efficiency, two-stage approaches involving a relay cranial implant have recently been presented [1,6], with ultrasound (US) serving as the "trans-dural" wireless powering modality thanks to its low attenuation in tissue, relaxed safety limits on power density and beam-steering capabilities. For trans-dural powering, the distance (d) between the cranial and subdural implants is up to 1cm (Fig. 3.4.1), while the implant diameter (D) should not exceed several mm to minimize the invasiveness of skull-opening surgery. Transducers with resonant frequencies in the MHz range are preferred [6], since their higher TX pressure sensitivity (kPa/V) maximizes power delivered to the load (PDL) over the small powering distance. Thus, d can be smaller than the Rayleigh distance $D^2/(4\lambda)$, meaning that the RX can be in the US near field (Fresnel zone). Acoustic reflections in this region create "standing waves", maximizing PDL at distances approximately equal to integer multiples of $\lambda/2$ and making it dependent on both distance and frequency. However, distance variations can occur during the implantation surgery but also due to the vibrations caused by breathing, heartbeat or head movements. Displacements by heartbeat of around 100mm [7] are close to the distance between peak and valley of the US standing wave of 4 to 4.5MHz, varying PDL by more than 2×. With a fixed ultrasound driver frequency (f_D), RX power is unregulated against such displacements [1], since the frequencies corresponding to the peak of the standing wave are shifted when the distance changes. Thus, there is a need to tune f_D and ensure operation at the peak of the standing wave for maximum PDL. This process is standing wave peak (SWP) tracking and can be characterized by the power-tracking accuracy, meaning how close to the optimal value PDL is regulated with varying distance. Within the narrowband f_D tuning range for SWP tracking, the transducer's pressure sensitivity remains unchanged and PDL varies only due to the standing waves. SWP tracking could be achieved with a global feedback loop as in [2,3], with PDL monitoring on the subdural implant and a wireless uplink of the feedback data to the power TX where it would be used for f_D tuning. However, such an approach increases complexity and power consumption on the subdural implant since it requires PDL monitoring as well as a dedicated driver circuit and transducer for the uplink of the power feedback [2,3]. Also, the wireless feedback does not allow for fast f_D settling (<100ms) needed to compensate for displacements caused by fast movements such as the heartbeat. To overcome these limitations, this work proposes a local TX f_D tuning loop for fast and autonomous SWP tracking that maximizes and regulates PDL with a high tracking accuracy and low power.

For near-field US powering, the medium acts as a lossy acoustic transmission line, with a change in frequency affecting the equivalent impedance seen by the TX (ZTX). PZT transducers with a resonant frequency at 4.3MHz are chosen as a trade-off between pressure sensitivity and attenuation in tissue. The standing-wave effect adds a magnitude and phase modulation on top of the ZTX profile. Thus, complex ZTX sensing has been used as the TX local feedback signal for f_D tuning [4]. Since voltage mode drivers are preferred for driving US transducers thanks to their power efficiency [13], ZTX sensing conventionally requires current sensing, with high resolution and low phase distortion necessary to accurately measure ZTX and maximize PDL. However, direct current sensing with a resistor in the power path [4] large enough to output a voltage signal $V(I)$ with high SNR leads to significant TX power loss, while bulky off-chip current sensing components exceed the cranial implant form factor constraints [5]. Alternatively, integrated current sensors with TIA [11] have constraints on the amplifier BW and power consumption for low phase distortion at high US frequencies. However, around resonance, ZTX is dominated by a resistive part [10] and PDL sensing can be simplified to active power monitoring. To enable low-power and high-accuracy power-tracking for 4.3MHz US without the constraints of ZTX sensing, an adiabatic power-sensing scheme is proposed.

The TX system architecture is shown in Fig. 3.4.2 (bottom left), with the full system comprised of an adiabatic driver with a V_{DD} of 4.8V and an f_D tuning loop. In this work, a 5-level adiabatic driver is adopted (Fig. 3.4.2 top left), with 3 capacitors connected to the intermediate nodes V2, V3, V4 and switches S1-S5 turning on and off sequentially, driving the US link with a 5-level 4.3MHz periodic waveform. Inside the f_D tuning loop, an ADC samples V3 from the adiabatic driver and provides the digitized voltage value V_p to a "SWP tracking FSM". Based on V_p, the FSM determines the frequency control word (FCW) that serves as the input of a frequency locked loop (FLL). Based on the FCW value, the FLL controls the frequency of a 12-phase DCO that provides the driving signals for S1-S5 in the 4-to-5MHz region.

In the adiabatic power-sensing scheme, the capacitors of the adiabatic TX are used as power-tracking elements. In adiabatic drivers [1,6], these capacitors serve to recycle part of the charge that would be dissipated by the load and thus improve driving efficiency of US transducers. At steady state in each US period, in the first half cycle the capacitors sequentially charge the US link load, while in the second half cycle there is sequential charge transfer from the load to the capacitors. With on-chip capacitors in the same range as the load capacitance, the voltage across these capacitors will vary due to the charge transfer. The voltages are decreased during the charging phase of the TX output (VTX) and increased during the discharging phase of VTX, with the example of V3 varying between $V3_L$ and $V3_H$ (Fig. 3.4.2 top right). For two US frequencies f_A and f_B, if $V3_L$ at f_B is lower than $V3_L$ at f_A, it means that at f_B there is a larger charge transfer between the cap of node V3 and the US link. This corresponds to a higher absolute value of output current ITX while the US link is connected to V3. Since the US link load is approximately resistive, this translates to higher PDL. Thus, V3 is monitored in the adiabatic power sensing scheme, and the system settles to the f_D of minimum $V3_L$ which maximizes PDL. In this way, direct PDL tracking with a high tracking accuracy can be achieved at TX with simple voltage sampling. For sampling, a S/H and 8b SAR-ADC running at 125S/s are used. For proper closed-loop operation, $V3_L$ should be sampled when it has settled so the S&H switch opens in sync with S5 opening, once every SWP tracking FSM cycle of 8ms. The adiabatic power sensing has negligible power consumption (43µW) and requires no current sensing or external components.

Prior art [4] performs f_D tuning for SWP tracking with a blind frequency sweep. This results in long f_D settling time (seconds) and the system cannot compensate for fast movements or heartrate vibrations and requires power consuming and long-latency memory access to store all sensing values. The proposed f_D tuning loop, instead, is fully autonomous, achieves frequency settling in <90ms and without accessing memory, thanks to the proposed SWP tracking FSM, as shown in Fig. 3.4.3. The FSM uses a differential approach and a pair of frequencies f_1 and f_2 that differ by a fixed amount df. df is selected to be in the same range as the frequency difference between consecutive peak and valley of the standing wave, that for trans-dural US powering at 4.3MHz is in the range of 40 to 60kHz, and thus df is set to 64kHz. Depending on the sampled voltage difference ΔVp between f_1 and f_2, the FCW is updated accordingly, and the pair of f_1 and f_2 moves across the spectrum with a step of df_2 until ΔV_p is smaller than a pre-defined value lim (i.e., $\Delta V_p < lim$). Then an extra operation is performed to check if V_p is smaller than the value at f_2 at the middle frequency of f_1 and f_2. This is an indication of a local minimum of V_p, and the FSM locks the FCW at this f_D, maximizing PDL. This continues until there is a new distance change and a voltage difference is detected to update the loop. Compared to conventional MPPT algorithms like hill climbing [12], the SWP tracking FSM takes advantage of the well-known periodicity of the power over frequency due to the standing wave and achieves power tracking with a higher gain (Fig. 3.4.3 right). Parameters df, df_2 and lim are programmable to allow for a wide range of US f_D and powering distances. df_2 is set to 4kHz as a tradeoff between tracking accuracy and settling speed.

With the use of the FLL, the FSM accurately sets the DCO frequency by setting the FCW. FLL adopts a 4kHz reference clock to allow a df_2 step of 4kHz. A 12-phase differential DCO is implemented to create driving signals for the adiabatic driver switches S2-S4 with duration $T_D/12$, where T_D is the US period. A leakage-based delay cell is used [8] as well as supply independent current bias with a self-start-up capability. DCO f_D tuning is achieved with resistor tuning of the current bias. The FLL tunes the DCO's 6b resistor fine bank, targeting a resolution of 2kHz to ensure a low frequency error. The fine bank range is designed to be 120kHz to ensure loop settling by having at least 2 standing-wave peaks within this range. The 4b coarse bank value is programmable, with a coarse resolution of 60kHz so that it is smaller than the fine bank range and a coarse range of 1MHz to compensate for DCO PVT variations and allow for the use of 4-to-5MHz transducers.

The chip was fabricated in 65nm CMOS, and the micrograph is shown in Fig. 3.4.7. Acoustic measurements are performed in water with all 64 TX units driving a single 6×6mm² PZT

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transducer, with a 6×6mm² RX PZT connected to a 50Ω load. By sweeping f_D and monitoring the digitized $V3_L$ and the RX AC voltage, the correlation of $V3_L$ with PDL is demonstrated (Fig. 3.4.4), validating the adiabatic power sensing scheme. The FLL can be settled within 8ms (Fig. 3.4.4). The closed-loop operation shows that the SWP tracking FSM tunes f_D in <90ms, and PDL is improved up to 2.7×(Fig. 3.4.5). PDL can be regulated to more than 82% of the maximum open loop value, when varying the powering distance but also when varying the initial f_D of the loop. Figure 3.4.6 summarizes the performance and compares it with state-of-the-art US drivers. Autonomous on-chip SWP tracking is performed on the TX with high PDL improvement and power-tracking accuracy while settling >50× faster than [4] and consuming only 43μW for SWP tracking, most of which is due to FLL operation.

Acknowledgement:
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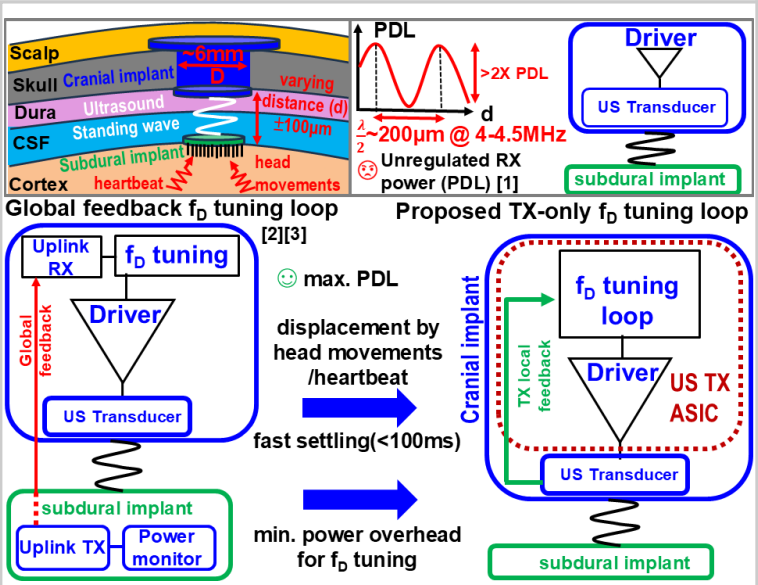


Figure 3.4.1: Simplified block diagram and concept illustration of the proposed trans-dural powering system with standing wave peak tracking.

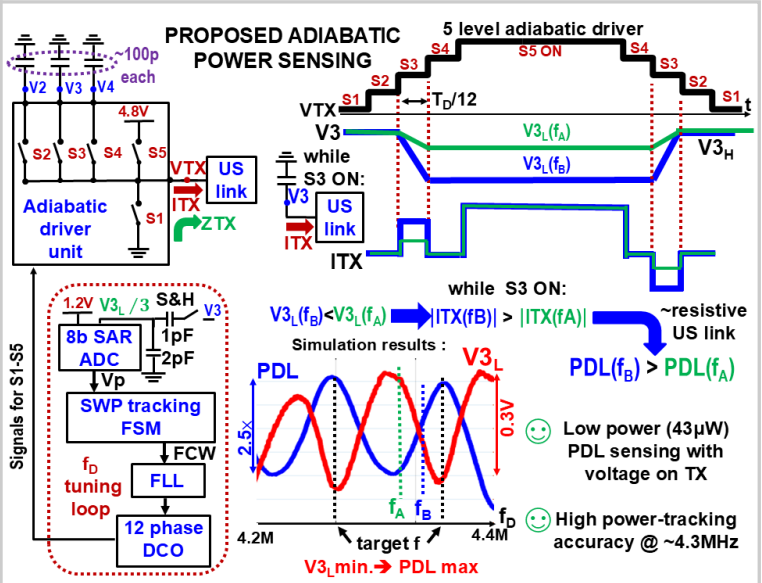


Figure 3.4.2: Simplified TX block diagram and concept illustration of the adiabatic power sensing.

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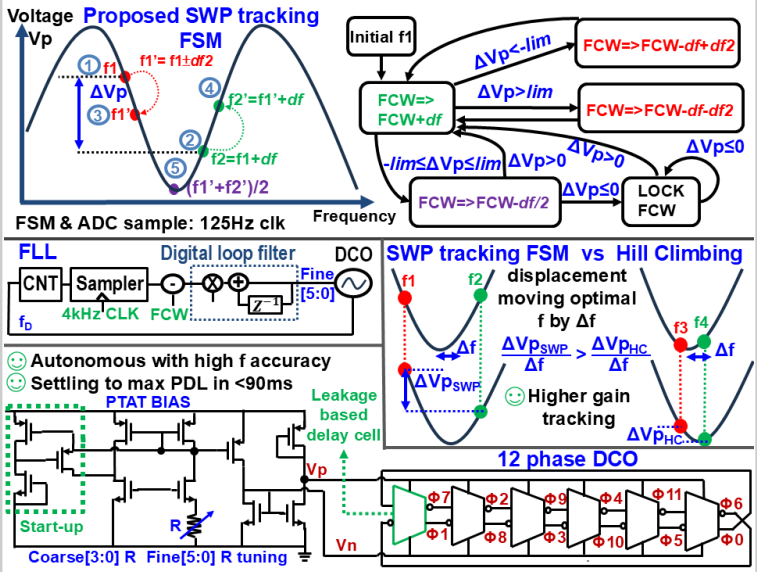


Figure 3.4.3: Simplified schematic of the frequency-tuning loop and concept illustration of the SWP tracking FSM.

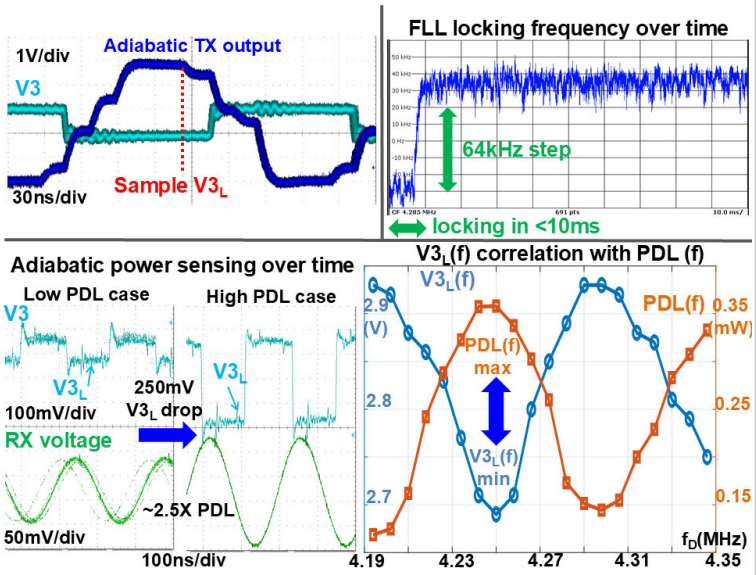


Figure 3.4.4: Measured TX output, voltage V3 to be sampled, FLL operation and acoustic measurements showing the correlation between sampled V3($V3_L$) and PDL.

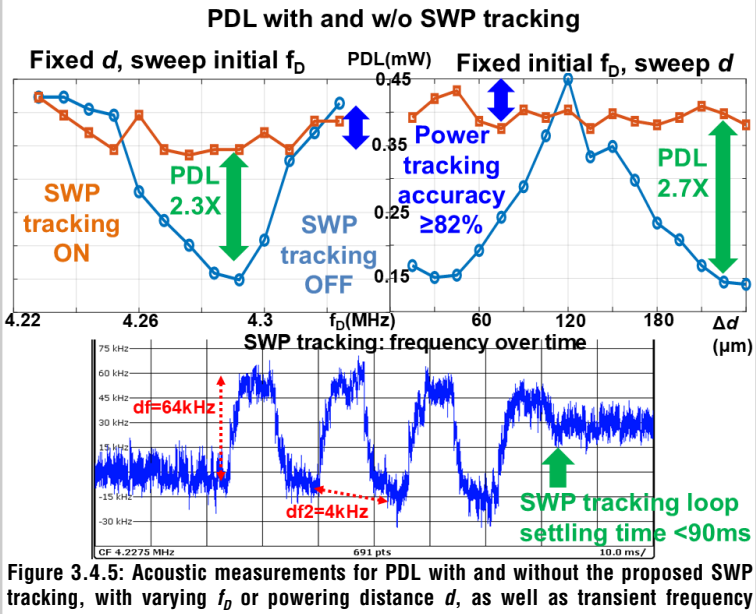


Figure 3.4.5: Acoustic measurements for PDL with and without the proposed SWP tracking, with varying f_D or powering distance d, as well as transient frequency measurement.

	This work	[4]Vihvelin, TBIOCAS'15	[2] Wang, TBioCAS'24	[3] Shmilovitz TBME' 13	[1] So, ISSCC'24	[6] Gourdouparis ISSCC' 24
CMOS process	65nm	Discrete	180nm	180nm	180nm BCD	65nm
Frequency	4.3MHz	1.3MHz	1MHz	720kHz	850kHz	7.8MHz
Autonomous closed-loop power regulation	YES	YES	YES	YES	NO	NO
Data link required for power regulation	NO	NO	YES	YES	-	-
Standing wave peak (SWP) tracking	YES	YES	NO	NO	NO	NO
On-chip SWP tracking	**YES**	NO	NO	NO	NO	NO
PDL improvement by SWP tracking	Up to 2.7X	Up to 2.5X	-	-	-	-
Power-tracking accuracy	**82%**	80%	-	-	-	-
Power loss for SWP tracking	**43μW**	Large (series R losses)[A]	-	-	-	-
settling time	**<90ms**	>5sec	-	-	-	-

[A]Estimated to be in the mW range, sensing R=209 Ω in series with transducer of 100-1K Ω under several Volts of supply.

Figure 3.4.6: Summary and comparison table of state-of-the-art ultrasound powering systems with power regulation.

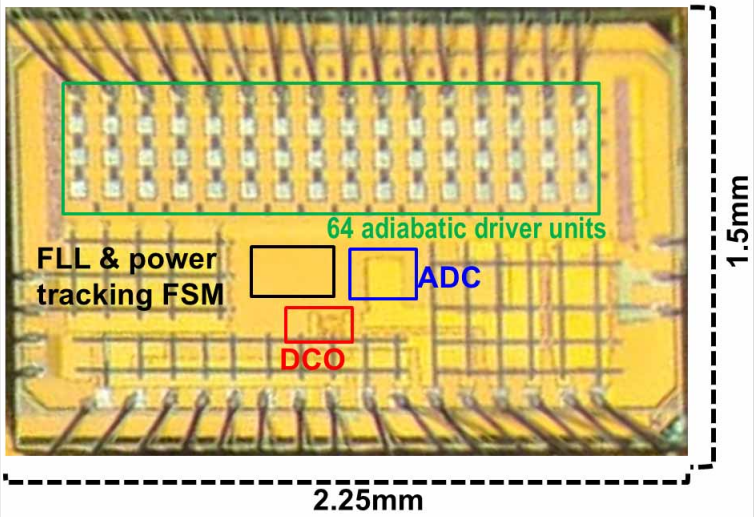


Figure 3.4.7: Chip micrograph.

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