Delft University of Technology
Faculty of Electrical Engineering, Mathematics and Computer Sciences
Laboratory of Electronic Components, Technology and Materials
DIMES Technology Centre

Foldable 3D Wafer Level SSL Package Using Flexible Interconnect

MASTER THESIS
ELECTRICAL ENGINEERING

AUTHOR:
Robert Sokolovskij
robert.sokolovskij@gmail.com

SUPERVISOR:
Prof. G.Q. Zhang
G.Q.Zhang@tudelft.nl

Delft, The Netherlands
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TU Delft Delft University of Technology

Delft Institute of Microsystems and Nanoelectronics
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Abstract

Solid State Lighting (SSL) is on track to replace conventional incandescent and fluorescent sources for general lighting. Even though it offers many benefits, the high initial device costs are still a major hindrance for many consumers. Packaging can account for up to half of the total device price, offering high potential for cost reduction. In this thesis, novel silicon wafer level packaging (WLP) concept and development platform are presented. The proposed packaging platform consists of silicon chips connected with neutral bending plane based flexible interconnect. Each chip contains an etched reflector cavity with wire bonded LED. The polyimide encapsulated flexible interconnects offer the benefit of folding the package into a 3D geometric shape. The space around the reflector cavity could be used to integrate active components and the backside – for passive components of the SSL driver circuit. The design, fabrication and characterization of the package is presented. A novel method to interconnect the front and backside of the chips is also incorporated into the process flow. After fabrication, packages are completed by adding LEDs, applying phosphor color conversion and release from substrate, followed by characterization of electrical, mechanical, thermal and optical performance. The developed packaging platform offers potential for future functional expansion by means of heterogeneous integration, possibly leading to a smart WLP package for SSL.

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List of Abbreviations

3D	3 dimensional
ALD	Atomic layer deposition
AR	Aspect ratio
ARDE	Aspect ratio dependent etching
BCB	Benzocyclobutene
BEOL	Back-end-of-line
BHF	Buffered hydrofluoric acid
BOE	Buffered oxide etch
CAD	Computer-aided design
CC	Correlation coefficient
CCT	Correlated color temperature
CMOS	Complementary metal-oxide-semiconductor
CMP	Chemical-mechanical polishing
CoB	Chip-on-board
CRI	Color rendering index
CTE	Coefficient of thermal expansion
DBC	Direct-bond-copper
DC	Direct current
DF	Dissipation factor
DI	Deionized water
DRIE	Deep reactive-ion etching
DSP	Double-side polished
DUT	Device under test
EBR	Edge bead removal
EM	Electromigration
EPD	Electrophoretic deposition
ESD	Electrostatic discharge
EUV	Extreme ultraviolet
F2R	Flex-to-Rigid
FEM	Finite element modeling
FEOL	Front-end-of-line
FM	Failure modes
FPP	Four point probe
GaAs	Gallium arsenide

GaN	Gallium nitride
HB-LED	High brightness light emitting diode
HF	Hydrofluoric acid
HNA	Isotropic Si etchant (HF:HNO_3:AcOH)
HNO_3	Nitric acid
I/O	Input/output
IC	Integrated circuit
ICP	Inductively coupled plasma
IPA	Isopropyl alcohol
IR	Infrared
KOH	Potassium hydroxide
LED	Light emitting diode
LPCVD	Low pressure chemical vapor deposition
LTO	Low temperature oxide
MEMS	Micro-electro-mechanical systems
MIM	Metal-insulator-metal
MMC	Metal matrix composite
MOCVD	Metalorganic chemical vapor deposition
MSM	Metal-semiconductor-metal
MtM	More-than-Moore
MTTF	Mean-time-to-failure
NMP	N-Methyl-2-pyrrolidone
NP	Neural plane
PA	Polyamide
PCB	Printed circuit board
PDMS	Polydimethylsiloxane
PE ALD	Plasma enhanced atomic layer deposition
PECVD	Plasma enhanced chemical vapor deposition
PES	Aluminum etchant (phosphoric acid - acetic acid - nitric acid)
PI	Polyimide
PIP	Polysilicon-insulator-polysilicon
RDL	Redistribution layer
RF	Radio frequency
RPM	Revolutions per minute
RTA	Rapid thermal anneal
SAM	Scanning acoustic microscopy
SiC	Silicon carbide
SiP	System-in-package
SMD	Surface-mount device
SMT	Surface-mount technology
SMU	Source/monitor unit
SoC	System-on-chip

SOI	Silicon on insulator
SPD	Spectral power distribution
SSL	Solid state lighting
TCC	Temperature coefficient of capacitance
TE	Thermoelectric
TFT	Thin film transistor
TMA	Trimethylaluminum
TMAH	Tetramethylammonium hydroxide
TSV	Through silicon (strata) via
UV	Ultraviolet
VCC	Voltage coefficient of capacitance
WL-CSP	Wafer level chip scale packaging
WLP	Wafer level packaging
YAG	Yttrium aluminum garnet

Chapter 1

Introduction

Since its invention, the light emitting diode (LED) has gradually established itself as the main light source for a broad range of applications. It is extensively used in many consumer electronics devices for indicator lights, portable light sources (flashlights), switches, information displays and automotive applications. First reports of electroluminescence date back to 1907, when H. J. Round published his observations that silicon carbide (SiC) crystals emitted light with voltage applied. Unfortunately his explanation of the observed phenomenon was inaccurate. The invention of the first visible LED is mostly credited to Nick Holonyak, Jr. in 1962 [1], though Oleg Losev reported electroluminescence of silicon carbide diodes 35 years earlier [2]. Despite the arguable origins, LED indicators of various sizes, colors and brightness levels can nowadays be found in virtually every electronics device.

Solid state lighting (SSL) is the application of LEDs for various illumination purposes. It introduces many benefits over conventional incandescent and fluorescent light sources, such as low power consumption, higher efficiency, absence of hazardous materials (mercury vapour, lead), exceptionally long lifetimes [3] and novel applications of lighting, however LED chips can only emit a narrow band of wavelengths, that is, monochromatic light of a single color. The color of emitted light is related to the band-gap of the semiconductor device, which in turn is dependent on material composite (e.g. GaN, GaAs, AlGaIn etc.). Therefore, certain wavelengths of the visible spectrum need to be combined so as to stimulate the perception of white light in the human eye.

High quality white light generation is only one of the main challenges associated with the design of SSL bulbs or luminaires. Other aspects include the design of power supply (driver) circuitry, optics, heat dissipation, demand for increasing light output and extremely long lifetime of the entire product. So the LED die is only a small part of the entire system. The costs of manufacturing SSL light sources are substantially higher than conventional light bulbs. According to a recent report [4], packaging of LEDs accounts for up to 50 % of the total device cost. On the other hand, it suggests high potential for overall price reduction if novel approaches are further developed.

A promising approach to reduce the costs associated with LED packaging is to integrate them in functional silicon based packages during processing compatible with back-end-of-line (BEOL) fabrication steps. This method is known as wafer level packaging or WLP. The purpose of this research is to design and fabricate a novel SSL package prototype on a silicon

wafer with integrated additional functionality that includes utilization of flexible interconnects to form 3D substrates, light reflector cavities with integrated LEDs and passive IC components, thereby demonstrating a heterogeneous integration approach for SSL applications.

This introductory chapter will first briefly cover the known device packaging and integration approaches for the IC (integrated circuit) industry. Then the issues with LED adaptation for SSL applications are presented as well as an overview of conventional packaging technologies for LEDs. Finally, a review of WLP is given followed by the motivation for the proposed 3D design.

1.1 Integration and Packaging

For almost 5 decades, Moore's law [5] has been the main guideline for the continued increase of functionality per unit silicon chip area. Ongoing feature size reduction approximately every two years (22 nm at time of writing), allows for the increase in transistor count per silicon area and therefore increases device performance and functionality with lower power consumption and heat generation. Reduction of the chip size on a Si wafer also yielded continuous decrease in manufacturing costs, since more devices could be fabricated on the same wafer. With every new node, lithographic scaling had to handle a growing amount of challenges to keep up with Moore's law. It has been recently reported [6] that sub 32 nm technologies will no longer possess the benefit of cost reduction due to increasing processing and extreme ultraviolet (EUV) equipment complexity. To continue the trend for more functionality per Si area new integration concepts known as More than Moore (MtM) [7] are gaining R&D momentum.

The MtM approach aims at combining several semiconductor technologies on a single chip, as depicted in fig. 1.1. Two directions are shown: digital circuitry will continue to follow

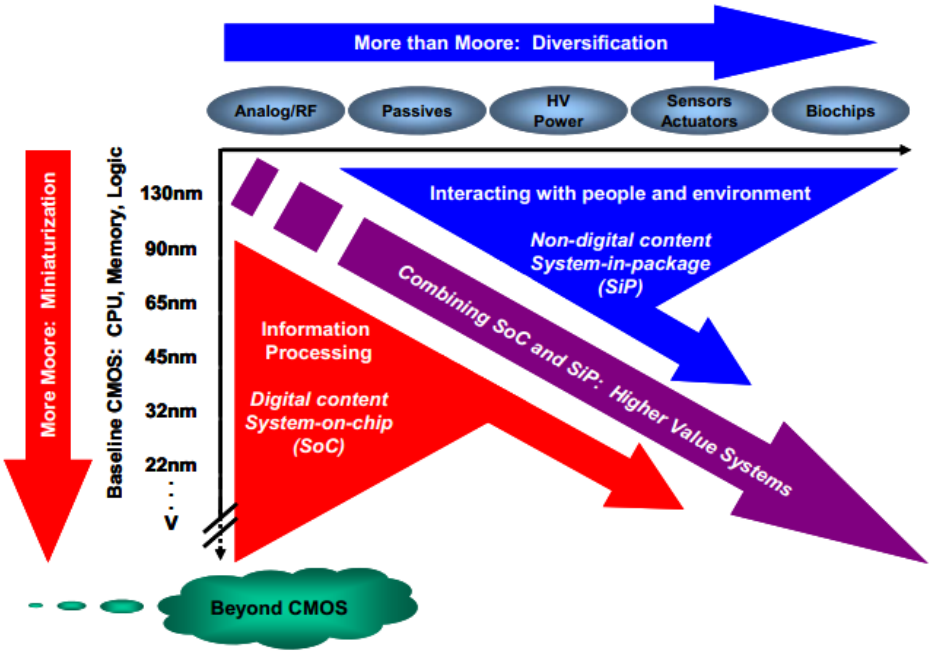


Figure 1.1: Combining Moore's law and More than Moore integration [7].

the lithographic scaling trends but additional functionally will be added to the same system by adding analog, RF or passive components. Integrated MEMS sensors would allow the to interact with the environment and the user. Such multifunctional systems on a chip (SoC) or in package (SiP) are applied in high end (consumer and industrial) applications.

Incorporation of additional functionality without increasing the floor plan area of the chip is a challenging task. Integrated circuits are usually considered as 2D, planar devices. Adding analog, sensing and other functions as well as passive components to a digital chip will significantly increase the 2D area of the die. Such an approach to heterogeneous integration could have an inverse effect on MtM, since the functionality per chip area would actually reduce as well as result in serious final device yield issues. An alternative and highly promising path towards MtM is by implementing 3D heterogeneous integration.

3D integration is based on utilizing the vertical dimension of the chip, without altering the planar area, by stacking multiple technologies on top of each other, forming a single SiP. Such ultimate design concept incorporating not only different functions but also new materials is presented in fig. 1.2. [8]. The enabling technologies driving 3D stacking and packaging

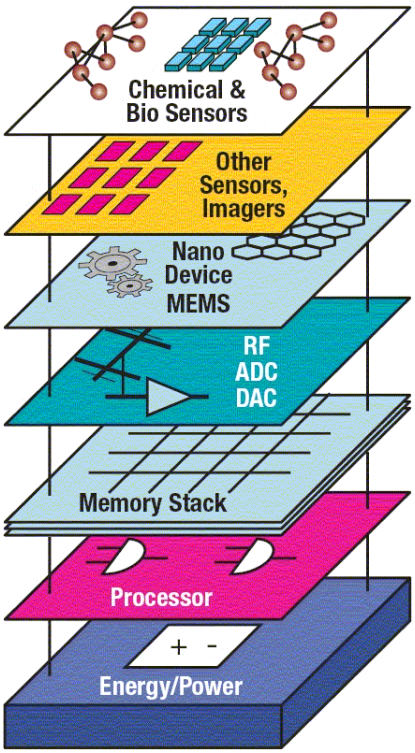


Figure 1.2: Functionality stacking for 3D integarion [8].

research are [9]:

- Through silicon (or strata) via TSV interconnections
- Wafer thinning
- Wafer alignment and bonding

These technologies can be further diversified in terms of various integration approaches, compatibility with other fabrication processes, intended applications and manufacturing costs.

A brief overview of the aforementioned technologies for 3D integration is given in appendix A.

Wafer level packaging (WLP) is essential for heterogeneous SiP integration. It enables the advancement of 3D heterogeneous integration for SIPs based on MtM. The term WLP defines technologies and design options to perform as many packaging steps of processed dies directly on the wafer as possible, prior to chip dicing and separation. WLP offers benefits in package miniaturization, increased processing throughput by packaging high numbers of devices in parallel, integration of additional functionally and overall cost reduction. It has been successfully applied for analog and digital IC chips, power IC, MEMS devices and passive components packaging.

Miniaturization of integrated circuit packages is possible by employing wafer level chip scale packaging (WL-CSP) technology. As the name suggests, these packages have dimensions that must not exceed 1.2×(chip size) and preferably should be 1:1 with the chip. With the continuation of Moore's law, it has been observed that cost per transistor is decreasing with process node downscaling and increased wafer size, since more functionality is added per Si area or chip size is reduced, while the fabrication costs remain the same. At the same time, the price of single chip packaging was increasing with every node, since more chips with higher I/O counts had to be packaged and tested. Contrarily, WL-CSP package costs go down with smaller nodes, as more chips can be packaged in parallel with shrinking die sizes [27]. In addition to increased throughput, WLP of IC chips allows to perform testing and burn-in procedures before die separation which leads to manufacturing cost reduction. IC chips are designed with bondpads on the edges of the die. The bondpad pitch is continuously decreasing as the die size is reduced and number of I/O goes up. To accommodate all required connections from chip to PCB, redistribution layers (RDL) are incorporated into the WL-CSP. Redistribution process starts with chip surface passivation using photosensitive polymers like benzocyclobutene (BCB) or polyimide (PI). Then metalization is performed by sputtering or evaporation. The metal layer is patterned to form an array layout of metal pads from the peripheral chip pads, allowing to substantially increase the pitch. Lastly, solder bumps are formed on the redistributed array by electro or electro-less plating or other methods [28] and A wafer level flip-chip package is complete.

WLP for micro-electro-mechanical systems (MEMS) differs from IC chip scale packaging. The main purpose of MEMS WLP is to provide encapsulation and electrical connection for micro-machined devices before wafer dicing. MEMS devices need to be packaged without molding materials because they have moving parts. Glass wafers with cavities for electrical interconnections are bonded to device wafers by anodic bonding (appendix A), to secure the chips from mechanical damage during further processing. CTE mismatch between Si and glass can damage certain sensitive devices. To avoid CTE mismatch Si wafers can be used for device sealing. Direct Si-Si bonding would damage the fabricated devices due to high process temperatures (appendix A), therefore bonding by intermediate layers, such as frit glass, solder, metal or polymer is employed. MEMS resonators, vacuum or IR sensors require vacuum packaging. For such applications, sealing with anodic bonding is done in vacuum and special getter films are deposited inside the device cavity to adsorb oxygen generated at the Si-glass interface. WLP by wafer bonding provides an inexpensive and robust packaging

solution for MEMS devices before chip dicing to prevent contamination with Si particles. Since MEMS can only be tested after chip separation, cost reduction and yield improvements are achievable with the WLP approach [29].

1.2 LEDs for General Lighting

LEDs are essentially p-n junction diodes. Under forward bias voltage, light is generated by emitting photons during radiative recombination of electrons and holes in direct band-gap semiconductor materials e.g. III-V compounds. The band-gap of a semiconductor is related to the wavelength of emitted light through the well-known Planck's relation [10]:

$$E_g = h\nu = h\frac{c}{\lambda} \tag{1.1}$$

where E_g is the semiconductor band-gap, h=6.62617 $\times$ 10^{-34} J·s – Planck's constant, c – speed of light, ν and λ – frequency and wavelength of a photon. Even though the operation principal of LED is similar to a diode for electronics applications, there are numerous additional parameters that define the performance of LEDs in terms of optical and electrical performance.

An important quantitative parameter of a white light source is the color rendering index (CRI). Color rendering is an effect that a light source has on the appearance of objects, when compared to a reference source. Poor color rendering leads to objects appearing discolored and unnatural [11]. CRI is determined by comparing the colors of 14 Munsell samples illuminated by the source under test and the reference illuminant. A CRI value R_i for each sample is then calculated by:

$$R_i = 100 - 4.6\Delta E_i \tag{1.2}$$

where ΔE – color difference between test and reference source. From eq. (1.2) it is evident that R_i can even have a negative value if color differences are very high. The average value of the first 8 samples is then calculated and gives the general color rendering index R_a which is usually quoted by the manufacturers of SSL. In general CRI < 80 is suitable for outdoor lighting, CRI > 80 used for indoor lighting and CRI > 90 is considered as sufficient for demanding applications, such as lighting for hospital operating rooms or art exhibitions. Unfortunately, there is an inherent trade-off between CRI and efficiency of SSL sources that needs to be taken into account when designing luminaires for various applications.

Because of wavelength dependence on the material band-gap, LEDs can only emit light of a single color. White light is a mixture of wavelengths of the whole visible electromagnetic spectrum and therefore it is not possible to produce white light with just a bare LED chip without employing color conversion techniques to stimulate the perception of white light in a human eye. Two approaches are used to produce white LED light for SSL applications: multi-chip combination and wavelength conversion [3, 12].

Our eyes see white light if three types of cones, located in the retina, are stimulated with similar intensity [13]. It is possible to mimic such stimulation by mixing two complementary, yellow and blue, color LEDs with appropriate power ratios. This dichromatic approach yields the highest luminous efficacy, but the CRI is lower than 20, unsuitable for lighting applications. Adding a red LED to the first two (trichromatic source) significantly improves the CRI > 80

at the expense of efficacy, but is suitable for general lighting. Reports on tetrachromatic multi-chip white light sources claim CRI of 95, at 6500 K CCT by selecting LED chips with appropriate peak emission wavelengths [14].

Wavelength converters are special materials that use high energy blue or UV photons (corresponding to the shortest wavelength) and down-convert part of these photons into lower energy (longer wavelength) photons. Most commonly used converter materials are phosphors, others include semiconductor converters and dyes [13]. When a blue photon excites (often called "optical pumping") yellow phosphor a photon, with wavelength in the wide middle range of the visible spectrum, is emitted. Extensively used yellow phosphors are based on yttrium aluminum garnets (YAG), doped with rare earth elements, YAG:Ce – used for SSL. By tuning the percentage of absorbed and transmitted light it is possible to obtain white light with correlated color temperature (CCT) in a range of 4000 K–8000 K, well suited for portable or outdoor lighting applications [15]. To improve the quantum efficiency and CRI of the source, various combinations of LED and phosphors have been investigated. Similarly to multi-chip designs, these are classified as dichromatic, using one LED and 1–2 phosphors [16], trichromatic and tetrachromatic, combining 1–2 LEDs with 1–4 phosphors [13].

Figures of merit for optical and electrical characterization of LEDs are summarized according to LED related literature [13] in table 1.1.

Table 1.1: Photometric, radiometric and quantum performance measures for LEDs [13].

Figure of merit	**Explanation**	**Measure unit**
Luminous flux	Light power of source as perceived by the human eye	lm
Luminous efficacy	Luminous flux per optical unit power	lm/W
Luminous efficiency (Source luminous efficacy)	Luminous flux per input electrical unit power	lm/W
Luminous intensity efficiency	Luminous flux per sr per input electrical unit power	cd/W
Luminance	Luminous flux per sr per chip unit area	cd/m^2
Power efficiency	Optical output power per input electrical unit power	%
Internal quantum efficiency	Photons emitted in active region per electrons injected	%
External quantum efficiency	Photons emitted from LED per electrons injected	%
Extraction efficiency	Escape probability of photons emitted in active region	%

So far, only issues regarding the LED chip were discussed. A complete solid state lighting system is segmented into 6 levels of the value chain, LED chip being level 0 [17]. A summary of functions at each level is presented below [18]:

0. *LED die.* Semiconductor diode, emitting light by electroluminescence.
1. *LED packaging.* Providing electrical connection, encapsulation, mechanical support and heat dissipation. Phosphor layer formation for white light generation.
2. *Multi LED assembly.* Smaller LED packages are placed and interconnected on PCBs enabling higher luminous output and improved thermal management. Also used for white light generation with phosphors and multicolor chips.
3. *LED module.* Interconnection and housing of driver circuitry to convert grid AC power to DC power for LED assembly. Additional functionally is often added: dimming, smart control.
4. *Luminaire.* Complete and sealed housing of final product. Two distinct approaches exist: *1. Retrofit* bulbs compatible with existing sockets and fixtures. *2. Beyond retrofit* whole systems integrated in custom housings with extremely long lifetime without need for replacement bulbs.
5. *Lighting system.* Complex system of many luminaires with control, monitoring, programming and sensing functions, as well as power consumption profiling and failure detection. Applied for large scale projects: street, building or city lighting.

Because of system complexity, designing and manufacturing SSL luminaires demands close attention at every value chain level in order meet the reliability and lifetime requirements exceeding 50000 hours. More than 30 failure modes (FM) have been identified for SSL, with the list still expanding [19]. For comparison, compact fluorescent bulbs only have 7 identified failure modes. For a brief overview, FMs can be categorized into optical, mechanical, thermal and electrical domains. Optical reliability deals with the light quality degradation, lumen depreciation, phosphor cracking and yellowing over the operational period of the device.

Mechanical reliability deals with defects in assembly, thermal stress, corrosion, delamination, cracks etc. of packages, modules and luminaries. Thermal stability is crucial for longevity of SSL systems. Increasing forward current is a way to increase luminous output, however this results in an increased junction temperature, that negatively affects lifetime as well causes shifts in emission spectrum peak. Ambient temperature inside the luminaire also plays an important role on reliability and is related to mechanical device stability mentioned earlier as well as electrical performance of power converters.

Power converters are the link between the input power source and the optical part of the luminaire. Typical driver circuit consists of three parts: control, switching and energy storage [20]. Studies have shown that the low power control circuitry that manages the switching frequency and determines the duty cycle of the converter is least prone to malfunction. Switching transistors and ceramic or electrolytic capacitors are regarded as the weak points of the circuit. These devices are more sensitive to thermal cycling and fail prematurely if are operated at elevated temperatures [20].

In addition to SSL specific failure modes, the electronics and interconnects also need to be validated in terms of electronics reliability. Failures due to electromigration, Joule heating, current crowding, and solder failure have to be considered.

Adapting the LED technology for general purpose lighting bulbs or luminaires, introduces a wide range of design, manufacturing, integration and reliability challenges, requiring multi-disciplinary knowledge from various fields of research and engineering. Since SSL sources are required to meet stringent lifetime specifications, simulations and accelerated test methods are used to predict time to failure. Studies aimed at testing time reductions are of great interest for SSL industry [21]. Components need to be tested individually first, then as a complete device. Tests involving multiple stress scenarios at once are carried out [17] and only after complete validation a product can be put on the market.

1.3 Functions of LED Packaging

The main functions of any electronics package are chip protection and insulation, input/output signal interconnection, power distribution and heat dissipation. Packages for SSL applications also contain phosphors for color conversion and optics to provide high color quality and light extraction efficiency.

The requirements for LED packaging arise from the targeted application. With increasing power of the device, more advanced packaging solutions are required to effectively dissipate heat generated by the LED chip. Heat dissipation performance is commonly characterized by thermal resistance of a package. Thermal resistance $R\theta$ is a property that defines how a material or body resists the flow of heat. In LED packaging applications thermal resistance is commonly measured between the semiconductor junction and the thermal pad, used for attachment to a heat dissipation structure (e.g. heatsink):

$$R\theta = \frac{T_J - T_C}{P} \tag{1.3}$$

Where T_J and T_C are junction and thermal pad temperatures respectively, P – thermal power dissipation of the chip. The development of LED packages in terms of thermal resistance reduction is presented in appendix B.

Light extraction, CCT control and light pattern formation are equality important aspects of packaging design for lighting applications. Low power LEDs are typically encapsulated using epoxy resins. Input power higher than 1W causes photo-thermal degradation of epoxy encapsulant due to increased junction temperatures and higher voltages. Degradation of encapsulant results in lifetime reduction caused by yellowing discoloration and cracking of the lens [22]. Silicones are more suitable for high power SSL applications, because they exhibit improved thermal stability, low shrinkage, low moisture absorption, variable Young's modulus, high optical transmittance for UV and visible spectrum and tunable refractive index [22, 23]. According to Snell's law (as described in appendix B), tuning of refractive index allows to maximize light extraction by reducing internal reflections between chip-encapsulant and encapsulant-air interfaces.

Silicone and phosphor mixtures are used to cover the surface of LED chips for down-

conversion based white light generation. Chips are first attached inside reflective cups and the phosphor-silicone compound is dispensed. There are 3 main methods to form phosphor layers:

- Freely dispensed coating
- Conformal coating
- Remote coating

A summarized description of these techniques is given in appendix C.

Designers of LED packages also have to take into account light beam collection and shaping. Materials used to form lenses need to have high transmittance in the visible spectrum range as well as be able to withstand thermal cycling and UV exposure. Glass has excellent properties for optical applications, but because of high cost and limited integration possibilities, is not commonly used. Various plastics with adequate optical properties are instead utilized for miniaturized LED optics molding.

LED optical system is often divided into primary and secondary optics. Primary optical elements are placed inside the package, in close proximity to the chip. An example of primary optics component is the reflector cup. Varying the depth and sidewall angle allows radiative pattern shaping. The reflector cup is coated with highly reflective material, like aluminum or silver. In addition to reflectivity, surface roughness of the reflector influences light extraction efficiency. Textured or diffusive reflectors extract more light as it is effectively scattered at varying angles, thereby reducing the number of total internal reflections and light trapping between the sidewalls [3]. The encapsulant material is also part of primary optics system. By shaping the top surface, where it interfaces with air, radiative patterns are formed as well as light extraction efficiency is enhanced.

Secondary optics are typically included for light pattern formation and additional mechanical support. Extra lenses and reflectors can be added and in certain cases phosphor coatings are placed on secondary lenses for maximizing light extraction with scattered photon extraction (SPE) method as described by [26].

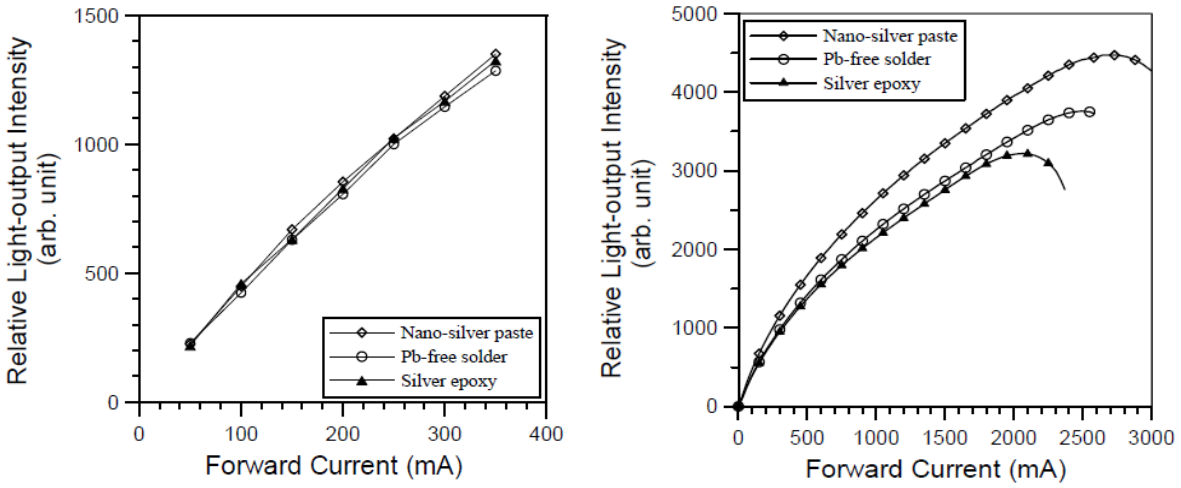
1.4 LED Wafer Level Packaging

Silicon based wafer level packaging is the next tier in component integration for power LEDs, succeeding CoB technology. Solid state lighting industry is still trailing behind in terms of WLP adaptation, but substantial research efforts are aimed at this technology for next generation lighting solutions. Because this work focuses on a novel WLP design for SSL applications, existing state-of-the-art designs will be reviewed.

Application of silicon microfabrication processing enables multiple package formation on the entire wafer followed my LED chip placement and attachment using exiting pick-and-place and die attach technologies with increased precision leading to overall yield improvements. A basic WLP package consists of a single chip attached to the Si wafer surface and encapsulated with silicone. Metal interconnects are formed and routed for wire bonding to the PCB. An improved approach is to route the interconnects to the backside of the substrate for flip-chip mounting with solder. Deep reactive-ion etching DRIE and copper TSVs are used for vertical connections [30]. These designs have no light reflectors hence the emission field is only defined by the LED chip, which results in a wide angle pattern. Integrated micro-reflectors are

fabricated by etching cavities in the substrate by DRIE or wet etching. Wet KOH or TMAH etch forms tapered cavities with 54.74° angle with respect to the top surface. These cavities are then lined with a thin reflective layer of metal for efficient light extraction. Simulations carried out for cavity optimization show that the taper angle as well as depth influence the light extraction efficiency of the package. It has been reported by Tsou and Huang [31] that for 1.8 mm×1.8 mm surface area and 525 µm deep cavity optimum taper angle is 53° – close to the wet etch angle. Modifying the sidewall angle is possible with DRIE etching by tuning the process conditions. Angle variation is achievable by altering the O_2 percentage of the $SF_6 + O_2$ gas mixture inside the plasma chamber, the chamber pressure, DC bias of the electrodes and substrate temperature [32, 33]. DRIE demands higher equipment costs but permits more processing flexibility, especially for designs incompatible with wet etching.

Most of LED WLP designs utilize the etched reflector cavities. Chips, placed inside these cavities by pick-and-place techniques, require reliable attachment and electrical interconnections. Proper attachment is done using adhesives like silicone or epoxy, re-flow soldering or sintering. The most suitable methods depend on the kind of chip used. Polymer based non-conductive adhesives provide reliable chip-attach for wire bond, flip-chip or vertical structure (one contact on top and one on bottom) LEDs, but suffer from low thermal conductivity. Electrically conductive die-attach materials have higher thermal conductivities and can be directly used for wire bond type chips. Wang et al. [34] investigated how different conductive die-attach materials influence the performance of high power GaN blue LEDs mounted on direct-bond-copper (DBC) alumina PCBs. The studied materials were silver epoxy (10 W/m·K), lead-free solder (50 W/m·K) and nano-silver paste (200 W/m·K). Experimental results have shown that for low supplied current levels there was no significant difference in light output, which means that the heat generated by the LEDs could be efficiently transfered through the tested mounting interfaces to the DBC board (fig. 1.3(a)). Increasing the current



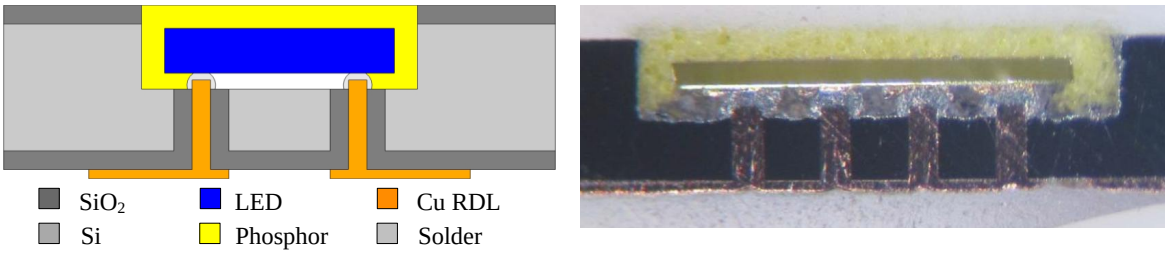
(a) Low current (b) High current

Figure 1.3: Relative light intensity of LEDs attached using three different materials at (a) low and (b) high supplied current values [34].

to higher levels resulted in greater temperature differences between the LED and substrate which indicates that heat transfer was insufficient. Best results were obtained using nano-silver,

while chips mounted with silver epoxy burned at 2.5 A fig. 1.3(b).

Flip-chip LEDs require the mounting interface to be patterned to expose the solder pads and avoid short circuits. Precisely patterning the bottom of a cavity is challenging, because of the need for lithographic exposure with proximity. A method to pattern the chip attachment and interconnection from the wafer backside was demonstrated in a WLP design by Zhang et al. [35]. The presented design fabrication starts with blind via etching at the backside and LED cavity etching at the from side using DRIE. The vias are then filled using same approach as for TSVs – electroplating. The front cavity is further etched with KOH until the copper pillars are exposed followed by BOE (buffered oxide etch) to remove the cavity passivation from the pillar tips. At this point the backside is still covered with a layer of copper, which is then covered in photoresist and electrodes are attached for solder platting. Solder is plated on the Cu pillar tips without any masking as there are no other conductive layers on the front-side. Solder is re-flown followed by the RDL formation using backside copper layer. LEDs are mounted and re-flow attached to the Cu pillars. Small amount of epoxy is dispensed inside the cavity and pre-cured with UV light, followed by phosphor powder printing with a squeegee blade and final curring to bind the epoxy and powder. The schematic of the finalized package as well as a cross-section image are presented in fig. 1.4. Such a design approach effectively combines the LED attachment and interconnection, but does not include a tapered cavity with reflective sidewalls, resulting in reduced light extraction efficiency.



(a) Schematic representation (b) Fabricated device cross-section

Figure 1.4: Flip-chip WLP with Cu pillars and RDL [35].

Alternative approaches for flip-chip mounting and RDL formation were proposed by [31, 36]. Solder was chosen instead of Cu to fill the through holes and form the RDL patterns. Wet etching was used by [31] to form both the reflector and backside via cavities, followed by thermal oxide isolation and nickel evaporation in the vias. Solder balls or paste were placed inside the cavities with micro-gripper or squeegee respectively, followed by re-flow to fill the vias with solder and form protruding bumps for LED mounting and RDL formation. The resistance of resulting vias was less than 5 Ω. Reflector cavity was not metalized by Tsou and Huang [31], whereas Chen et al. reports [36] on a wafer level package designed with metal reflectors, TSVs and cavity sealing by glass wafer bonding. The bottom of the reflective cavity was patterned to avoid shorts and the chip was mounted with adhesive prior to TSV etching. Glass wafer was bonded to seal the cavities and provide support to the Si wafer. The backside of the Si wafer was then thinned and TSVs, aligned to the LED contacts, were etched by DRIE. Polymer cavity passivation was carried out and laser drilling method was used to open the cavities and LED pads for metal sputtering and solder platting. Some of the glass sealant

wafers were coated with phosphor before bonding, forming a remote phosphor based WLP package directly applicable for SSL [36].

After mounting and interconnection, LED chips are encapsulated to complete a wafer level package. Various approaches are being developed to fill the reflector cavities with silicone and phosphor mixtures and form micro lenses for every package on the wafer with high throughput.

A method for conformal phosphor coating, based on injection molding, was developed and incorporated into a WLP process flow [37]. The package includes copper TSVs that are partially filled to reduce thermal stress. After vertical structure LEDs are attached and wire bonded, a mold is fixed and phosphor mixture is injected from one side. The phosphor is evenly coated on the chip due to capillary effect, followed by currying and mold removal. Unlike screen printing, this technique does not damage the wire bond leads during phosphor application and is suitable for all types of LED dyes. A separate wafer is etched with hemispherical cavities,which are filled with silicone, and is used as a mold to form an array of micro-lenses. The device wafer is flipped face-down and placed on the mold wafer. Once the silicone is partially cured the mold is removed. The polymer continues to cure and flows into additional TSV trenches (fig. 1.5), added to improve the shear strength of the lenses, due to poor adhesion of silicone to Si.

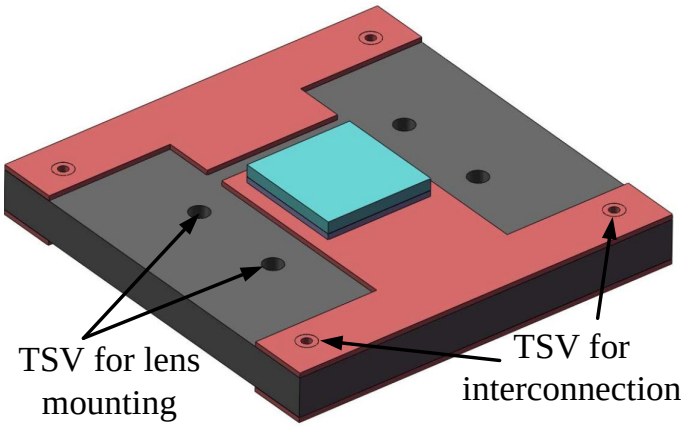


Figure 1.5: Wafer level package with TSVs for electrical connections and micro-lens attachment.

A moldless encapsulation method for LED arrays on a Si wafer was developed by Zhang and Lee [38]. UV curable epoxy was used as the encapsulation and lens material. Analysis of how the epoxy spreads on the wafer coated with low temperature oxide (LTO) was carried out. A syringe with precisely controlled injection volume was used to dispense the epoxy using the glob-top method, i.e. conformal dispense of viscous encapsulant at pre-defined areas for mechanical protection of devices. The obtained results indicated that freely dispensed epoxy, even when accelerated UV curing was applied, spreads too rapidly and a hemispherical lens, which, according to ray-tracing simulations [37], would result in maximum light extraction efficiency, cannot be formed. The maximum contact angle between the polymer and Si substrate with UV curring was 56.5° (fig. 1.6), where as angle of more than 80° is needed to form a hemisphere. Free flow constraining structures were designed around the encapsulation area to limit the spread of epoxy and increase the height to length ratio (H/L) of dome shaped

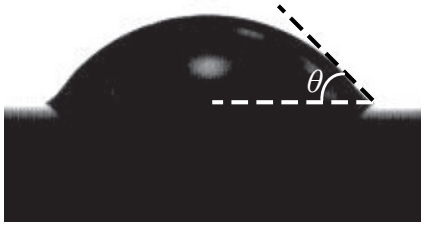


Figure 1.6: Highest achieved contact angle of freely dispensed epoxy after UV curing θ=56.5° [38].

lens. Two variants of constraining structures were evaluated, namely squares of varying area outlined with single and double line trenches, as shown in fig. 1.7. The best results obtained were H/L=0.42 for single line and H/L=0.52 for double line, which indicates that an hemisperical lens (H/L=0.5) can be obtained with moldless glob-top dispense method employing flow-constrain structures.

(a) Single line constrain (b) Double line constrain

Figure 1.7: Epoxy flow constraining structures: (a) single line, (b) double line [38].

An advantage of silicon based packaging is that additional functionality or devices can be directly integrated using standard silicon processing technology. Liu et al. demonstrated a thermoelectric (TE) device based on the Peltier effect, integrated into a Si LED package [39]. The heat removing structure was sandwiched between two Si wafers. The LED chip was placed on the cold side of the TE device and the hot side attached to a heatsink. Measurement results demonstrated that such active cooling method allowed to maintain the LED junction temperature at levels close to ambient temperature. In the proposed package the device and LED were connected in series to have the same driving current. Even though the TE cooling consumes additional power, it was determined that, compared to a package without TE device, the luminous efficacy of the device was 70% and 11% higher at 100 mA and 350 mA respectively.

Sensor integration into the SSL module would allow to monitor the performance of the LED chip. In case, the chip starts to overheat brightness reduces and a shift in peak color occurs, that can be detected using a photo-sensor. Kim and Lee [40] designed a metal-semiconductor-metal (MSM) photo-sensor integrated on a thin polysilicon membrane. The sensor was placed on the top corner of the integrated micro-reflector cavity with the polysilicon membrane overhanging above the cavity. A portion of light emitted from the LED would

then be absorbed by the sensor and generate a photo-current. A design with sensors on the membrane and on the surface of the Si wafer was made to compare the amount of generated photo-current in the MSM sensor (fig. 1.8). The amount of light falling on the membrane sensor was substantially higher, leading to an increasing amount of photo-current generation with increase in LED driving current. The surface mounted photo-sensor absorbs only a small portion of emitted light and a change in photo-current is difficult to detect. Measurement results for both sensors are presented in fig. 1.9. By integrating sensors and a feedback network to the driving circuitry accurate monitoring and control of chip performance is possible by altering the supplied current.

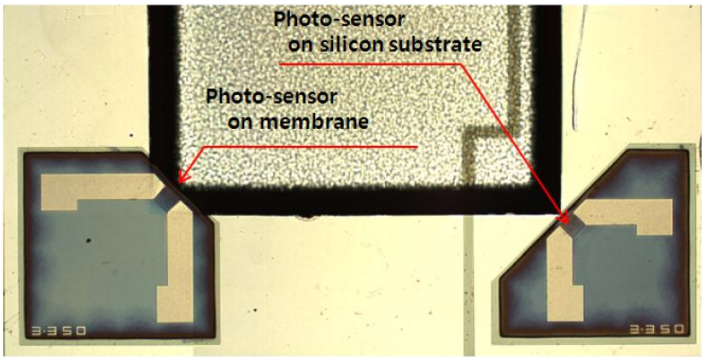


Figure 1.8: Top view of MSM sensors on Poly-Si membrane and Si surface.

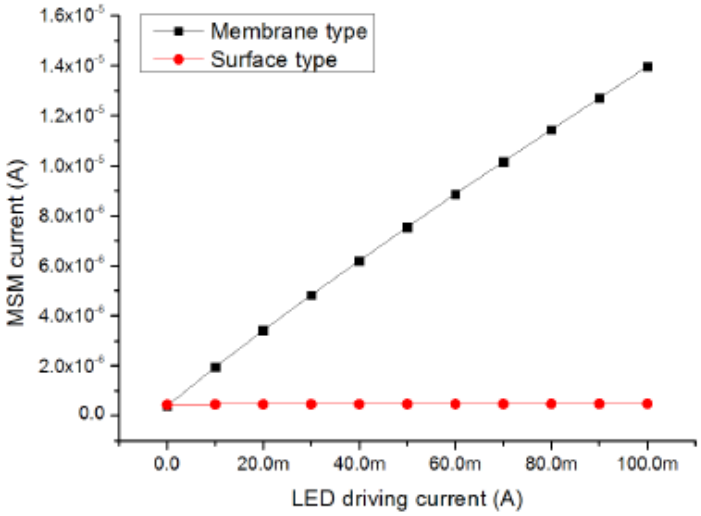


Figure 1.9: Photo-current generated by MSM sensors fabricated on poly-Si membrane and Si surface with increasing LED driving current.

To sum up the overview of current WLP technologies for SSL, a conclusion is made that silicon based packaging is a viable replacement of current LED packaging methods. Combining the reviewed technologies will allow to develop completely functional and compact form factor SSL modules with integrated circuitry, sensors and optical components. Such devices will follow the More-than-Moore heterogeneous integration concepts and evolve to low cost smart packages for high reliability lighting modules.

1.5 Proposed 3D WLP Design and Motivation

Generally the term 3D WLP is used to describe packages that utilize vertical (TSV) interconnections, redistribution and interposer layers. These packages are still only as thick as the substrate wafer, essentially flat. In lighting applications, wafer level packaged LED chips would be singulated and individually placed on multi-led assembles. LED assemblies are designed to meet specific luminaire applications, some of them having all the LED chips facing one direction for unidirectional lighting, while others form omni-directional designs for uniform light distribution without complex secondary optics, as shown in fig. 1.10. In this

(a) Unidirectional (b) Omni-directional

Figure 1.10: LED luminaires with (a) unidirectional [41] and (b) omni-directional [42] assemblies.

work, novel multi-chip WLP concept is introduced, which allows to form packages with 3D geometry and shape them into assemblies with omni-directional light emission. Si is used as substrate material to from packages with reflector cavities. Aluminum lines and bonding pads are added to interconnect packages together to form assembles. Geometrical shaping is achieved by adding flexible hinges with embedded interconnects followed by release of the formed packages by backside DRIE etching, forming rigid silicon islands with flexible joints (fig. 1.11).

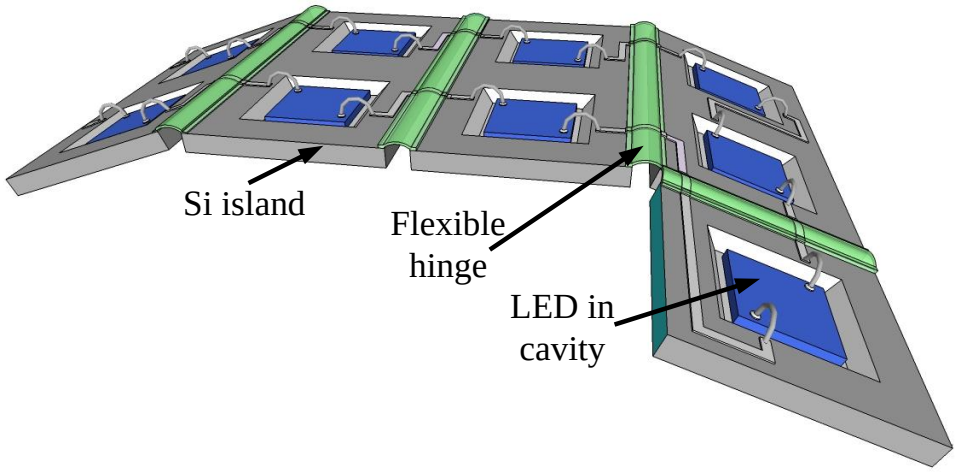


Figure 1.11: Silicon based flexible WLP package concept.

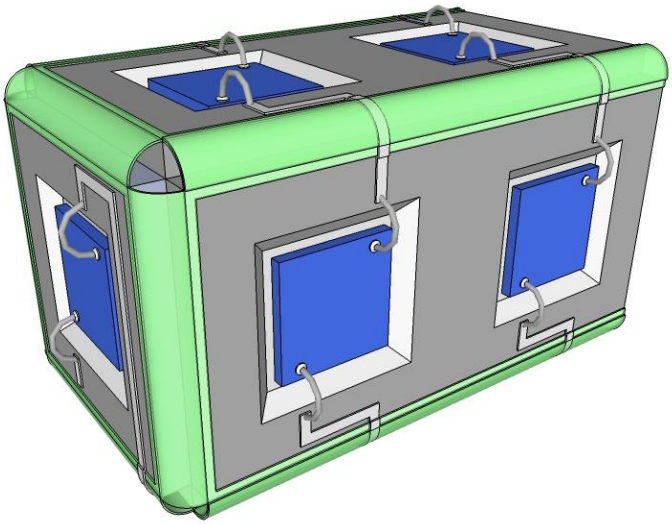


Figure 1.12: Flexible WLP design folded to form a cuboid.

To demonstrate the compatibility of the proposed design with standard microfabrication technology, metal-insulator-metal (MIM) capacitors are integrated on the backside of the formed islands. Embedded capacitors can be used to replace their discrete counterparts in the LED driver circuitry. A method to interconnect the front-to-back side of the Si package through the chip periphery, based on foldable interconnect is also added to the package design. The finalized device is released from the substrate wafer and folded around a heatsink to form the desired shape. A design with 5 islands, forming a cuboid with the bottom sidewall left open, as shown in fig. 1.12, was chosen. Dimensions of the package were based on the current version of the G4 1W LED Capsule from Philips Lighting [43]. The proposed WLP design effectively merges the 1st and 2nd levels of the SSL value chain (ref. to page 7), thereby offering potential manufacturing cost reductions. A detailed description of the flexible WLP design and fabrication process will follow in subsequent chapters of this work. Each design aspect and integrated components will be presented separately followed by the complete process flow and final device characterization. The last chapter will summarize the work and achieved results and present suggestions for further development of the proposed concept.

Chapter 2

Flexible Interconnect Integration

2.1 Introduction

The proposed WLP requires flexible hinges with embedded interconnect for folding into the 3D geometry and providing power to every LED chip. In this chapter, the latest existing methods to form flexible/stretchable chips are reviewed. Then the design of the package is presented, that incorporates neutral bending plane based flexible interconnects encapsulated in polyimide. A method to connect the front-side to the backside of the chips is incorporated into the processing flow. The complete flow is discussed in detail, introducing the associated challenges and chosen solutions.

2.2 Current State of the Art

Development of electronic components and devices that can withstand cyclic stress, strain and deformation without functionality degradation has gained increasing research interest in the last decade. These devices fall under a broad category of flexible and stretchable electronics engineering. A growing number of applications for such circuits has been demonstrated, ranging from flexible displays and sensors to miniaturized medical instruments and energy storage systems [44]. These devices require reliable interconnects that would withstand repeated mechanical deformation to comply with various form factors and while operating within required specifications.

Organic semiconductor materials are widely applied for large area flexible electronics. The benefit arises from the ability to deposit these materials on low cost substrates such as glass, plastic or metal foil using high throughput methods like ink-jet and roll-to-roll printing. Typical applications are in manufacturing of organic LEDs, flat and curved displays, flexible thin-film solar cells and thin film transistors (TFT). The main disadvantage of organic semiconductors is their inferior electrical properties (carrier mobility, resistivity), in comparison to inorganic semiconductors [45].

High performance chips are fabricated on rigid Si wafers. Integration of these devices for use in flexible electronics presents a challenging task with various approaches being developed. Silicon wafers are extremely rigid, hard and brittle with Young's modulus values from 130 GPa to 170 GPa for the $\langle 100 \rangle$ and $\langle 110 \rangle$ crystal orientations respectively [46]. Thin

Si films (<300 nm) are known to exhibit size effect, which causes the Young's modulus to monotonically reduce with decreasing layer thickness [47]. This property as well as the reduced strain in thin layers has been utilized for flexible, thin Si based circuits, that can be transfered onto flexible substrates or curved surfaces. A transfer method for such silicon micro-structures, using a polydimethylsiloxane (PDMS) elastomer stamp, was presented in [48]. Thin structures, fabricated on silicon-on-insulator (SOI) wafers, are partially released by etching the buried oxide layer with HF. The soft stamp is pressed against the substrate and forms a conformal contact with the structures. The adhesion between an elastomer and a solid is peel rate dependent, thus, with sufficient peel velocity, the structures are transfered onto the stamp. To transfer the pattern onto another substrate the stamp is brought in contact and peeled slowly. In this case the adhesion is higher between the structures and the substrate resulting in efficient pattern transfer. Figure 2.1 shows arrays of thin Si bars transfered onto a spherical surface with radius of 1 cm, without delamination or cracking. A comprehensive study on

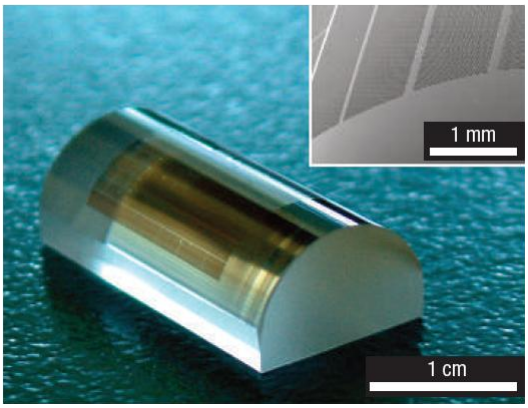
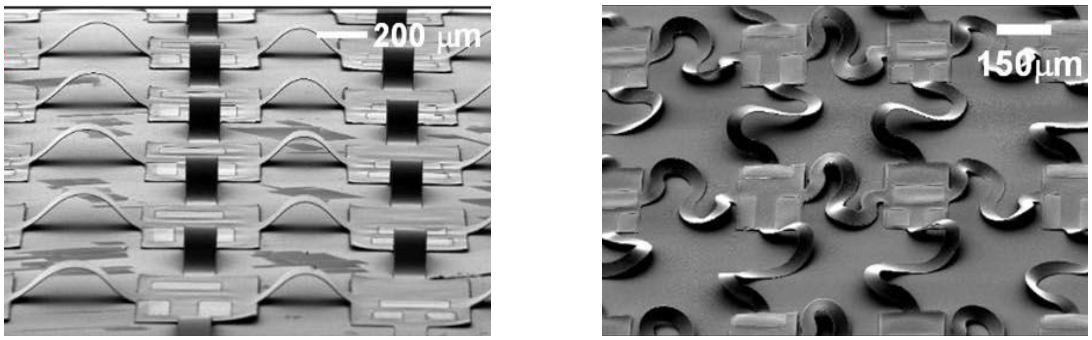


Figure 2.1: Thin silicon structures on spherical surface, applied by transfer printing [48]

the thin silicon deformation that demonstrates the relations between thickness and bending radius as well as observed failure mechanisms has been conducted by Park et al. [49]. Transfer printing of thin silicon islands, joined with out-of-plane flexible interconnects onto pre-strained stretchable PDMS substrates, yields the formation of flexible and stretchable inorganic circuits, as demonstrated in [50]. After releasing the strained substrate arc-shaped non-planar ribbons are formed, as shown in fig. 2.2(a). The arrays could stretch and twist in multiple directions



(a) Arc-shaped interconnects (b) Serpentine interconnects

Figure 2.2: Thin silicon structures with flexible interconnects on prestrained substrates: (a) acr-shaped interconnect (b) serpentine interconnect [50]

and strain of 11%, (with prestrain of 17%) was reported for the entire mesh. Replacing the arc with a serpentine layout (fig. 2.2(b)) with high substrate prestrain of 90% resulted in 100% elongation (system strain). Simulation and experimental results indicated that higher prestrain improves the system stretchability and increases the active component density due to shorter interconnect lengths. Thin Si and substrate transfer procedures pose a number of processing challenges. For many applications it is sufficient to employ flexibility and stretchability only at the interconnect, keeping the active devices on rigid Si. A common attribute of such designs is wafer segmentation by etching through the entire substrate, to form rigid islands with integrated components. The islands are held together by flexible or stretchable joints with embedded interconnects. High levels of flexibility have been demonstrated by placing the metal lines in between two layers of encapsulation material of equal thickness. Observing from the cross-section of the formed structure, the metal is located at the center. When bending is applied, one surface experiences tensile strain while the opposite side – compressive strain. It is known from mechanical beam bending theory, that at the center the tensile and compressive strains compensate each other therefore the stress at the center of the beam is approaching zero. This is known as the neural plane (NP). Flexible micro-cables have been successfully implemented, by placing the metal layer in the NP, for an implantable neural probe array [51]. Polyimide (Pyralin PI 2611) was chosen as the flexible substrate. A 5 µm thick layer was spin-coated and cured at 350 °C on a Si wafer covered with a thin Ti layer without using an adhesion promoter to enable easy release of the cable from the substrate wafer after processing is complete. Interconnects were formed by evaporating a 1 µm Cr/Au/Cr stack and lift-off patterning. The second PI layer of equal thickness was then applied and cured. The cables were patterned using RIE etching and then manually released by pealing with tweezers. The completed cable consisted of 30 interconnects with dimensions 20000 × 100 × 1 µm (L × W × H) and 150 µm pitch, which demonstrates the possibility to fabricate high densitity flexible interconnects. The cable was then subjected to electrical and mechanical characterization and demonstrated high data transmission rates with proper isolation between the signal lines. Fatigue testing showed that the wire can withstand cyclic deformation which is necessary for implantation of neural probes in the human brain.

Stretchable interconnects have also been demonstrated by utilizing the NP. In this case PDMS is used as encapsulation material due to it's elastic properties. To accommodate the applied strains, interconnects with meandering shapes were designed. Gonzalez et al. [52] presented a study relating the shape of copper interconnects to strain distribution and the possible elongation that the interconnects can withstand. Three meander shapes were investigated: elliptical, "U" shape and horseshoe. Finite element modeling (FEM) results have shown that when deformation of 20% was applied, the horseshoe meander exhibited the smallest amount of stress, 40% less in comparison to the elliptical. A scale factor was defined that shows that with a constant meander radius to interconnect width ratio (R/W) (fig. 2.3) the equivalent plastic strain of the interconnects remains unchanged. With increasing scale factor plastic strain reduces, so it was concluded than wide meandering lines should be split into equally spaced parallel tracks with minimized widths to achieve maximum stretchability. An improvement from 20% to 100% elongation was observed when a wide line was split into

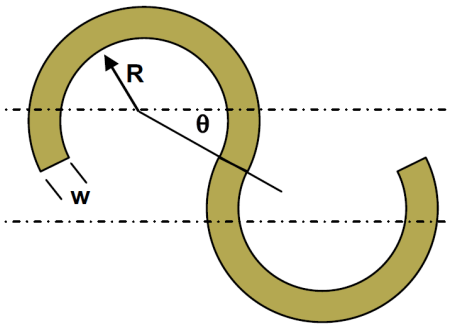


Figure 2.3: Horseshoe meander shape: R – inner diameter, W – line width, θ – joining angle [48]

four lines of reduced width (from 60 µm to 15 µm). Finally, higher elongation was obtained for horseshoe designs with higher joining angles θ.

The horseshoe type meandering interconnects possess high single-stretch strain. During cyclic stretching, these interconnects failed after only 85 stretch cycles of 30% elongation [53]. In addition, delamination was observed between the metal lines and PDMS encapsulation [54], that presents a risk of premature failure. To increase the overall reliability of meandering interconnects a double encapsulation approach was investigated by [55]. In this case, horseshoe Cu tracks were first encapsulated in polyimide, before molding with PDMS, as shown in fig. 2.4. The experimental results revealed that the maximum elongation increased to 250%.

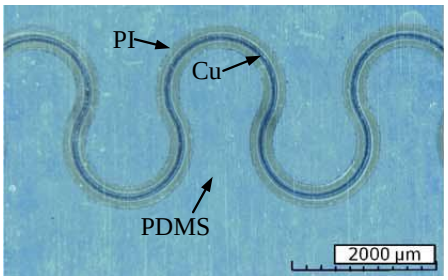


Figure 2.4: PI-enhanced stretchable interconnects [55]

A substantial improvement in the number of stretching to failure cycles (from 85 to 40000 at 30% elongation) was achieved. Delamination between PDMS and PI was observed at 65% stretching, however no interfacial delamination was observed between PI and metal, indicating that interconnects are reliably insulated by PI.

Liquid alloy materials have also been investigated for applications in flexible/stretchable interconnects. Alloys of eutectic gallium indium (EGaIn), injected into elastic hollow fibers or molds can achieve elongation levels exceeding 700% [56]. A common characteristic of this type of interconnects is the increase in resistance with stretching as the length of the conductor increases while the cross-sectional area reduces. The resistance variation can be minimized by using a diamond-shaped rather than a straight-line conductor design, because the channel length variation is reduced [57]. A functioning LED, connected to liquid-alloy diamond-shaped interconnects, encapsulated in PDMS, is shown in fig. 2.5. The device was subjected to stretching, bending and torsional twisting and still maintained proper operation.

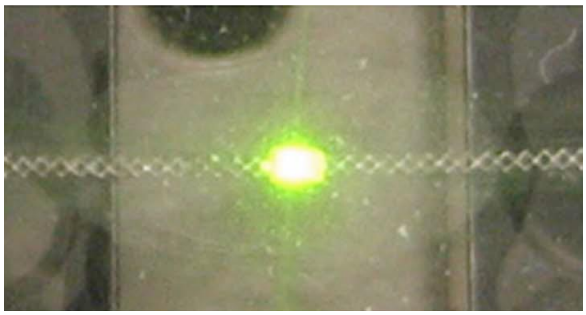


Figure 2.5: PDMS encapsulated LED with EGaIn diamond-shaped interconnects [57].

2.3 Flexible Interconnect Design

The main focus of this work was to design and fabricate a flexible Si based wafer level package for SSL applications. Various approaches were reviewed as evident from section 2.2. The package would consist of rigid Si islands with LEDs integrated inside reflector cavities. The LEDs should be connected in series to form wafer level LED assembles. The fabricated devices would be released form the substrate and folded into a 3D geometry. The design choices were weighed with regard to the following considerations:

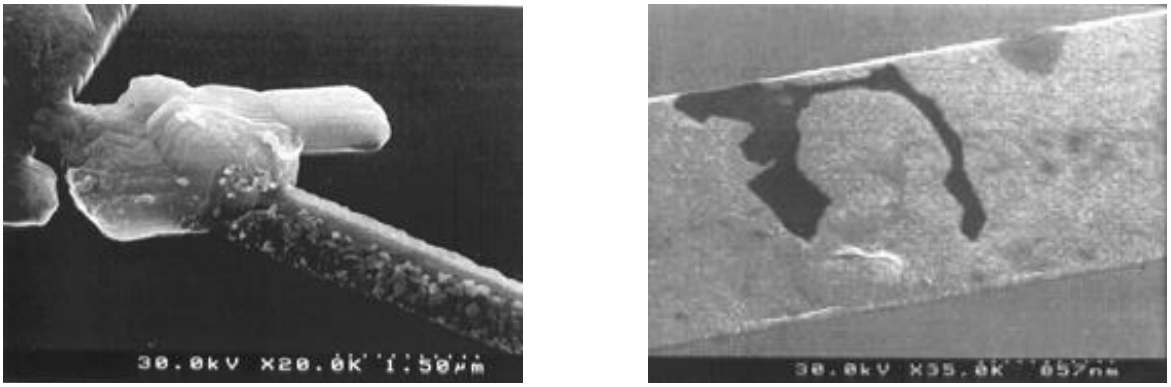
- Current-carrying capability
- Mechanical bendability
- Compatibility with standard CMOS processing
- Compatibility with MEMS processing
- Reduction of overall process complexity

Current carrying capability of a conductor is largely determined by the electrical resistance of the chosen metal and physical dimensions. Resistance of a uniform conductor can be calculated as:

$$R = \rho \frac{l}{A} \tag{2.1}$$

where ρ – electrical resistivity, l and A – length and cross-sectional area. Pure aluminum was used for the interconnects, because of package cost considerations, compatibility with the processing sequence and low electrical resistivity ($2.7\,\mu\Omega\cdot$cm). Interconnects were designed to withstand possible failures due to electromigration (EM) during the entire operational lifetime of the LEDs. Electromigration is the effect of material transfer caused by electric field. When DC current flows through the conductor some of the free electron momentum is transfered to the metal ions, causing transfer of material in the direction of current flow. This effect causes buildup of metal atoms that form hillocks as well as voids at the grain boundaries of the metals [58]. Hillocks can result in short circuits between densely spaced lines, where as voids cause local resistance increases leading to complete line failure. An example showing aluminum film degradation caused by EM is shown in fig. 2.6. To estimate the mean time to failure (MTTF) of metal interconnects in integrated circuits, an empirical model, that takes electromigration into account, was developed by J. R. Black [59]:

$$MTTF = \frac{A}{J^n} \exp\left(\frac{E_a}{kT}\right) \tag{2.2}$$



(a) Hillocks (b) Voids

Figure 2.6: Interconnect defects caused by electromigration [58]

where A – constant related to the cross-sectional area of the interconnect, J – electric current density, n – scaling factor, E_a – activation energy (0.7 eV for Al), k – Boltzmann's constant (1.38×10^{-23} J/K), T – absolute temperature. Interconnects integrated on Si can withstand higher current densities without melting than electrical wires, since the thermal conductivity of Si is high. To increase the lifetime of interconnects current densities must be kept below critical values. Elevated operating temperature of the device will also lead to reduced MTTF. Since LED junction temperatures can reach above 100 °C and generated heat is dissipated across the whole silicon island, the interconnect temperature will raise accordingly. At areas were the flexible hinges are formed, the metal lines are encapsulated between two layers of polyimide and the underlying silicon is etched away. FEM simulations were carried out to investigate how encapsulation of Al interconnects between layers of polyimide will influence the temperature of the interconnects [60]. The simulated geometry is shown in figure fig. 2.7. Joule heating, generated by current flowing through the Al interconnects was considered as

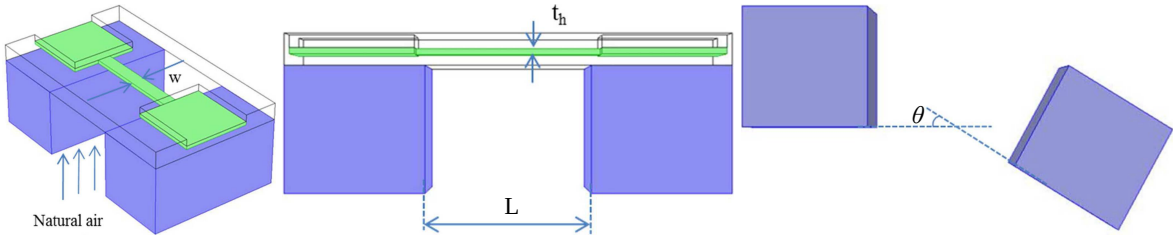


Figure 2.7: Geometry for FEM simulations of flexible interconnect[60].

the only heat source and natural convection and thermal radiation were used as heat transfer mechanics. To meet the lifetime requirements, MTTF of 25000 h was chosen as a minimum value. The maximum temperature difference between the package and ambient could not exceed 65 °C. The width of the hinge (L) and cross-sectional area (S=$t_h W$) were chosen as variables for the encapsulated metal lines. The influence of bending angle on the package temperature was also evaluated. With all the mentioned constrains in mind, simulations were performed and a design rule was derived indicating that in order to meet the current requirement of 700 mA for high power LEDs at a 90° hinge bending angle the ratio L/S should be less than 2. In the fabricated package, the L/S=1.5 was chosen for the interconnects, with

dimensions of $900 \times 300 \times 2\,\mu m$ ($L \times W \times t_h$).

In the proposed package design, flexible interconnects are implemented to connect the LED chips in series and to form a flexible front-to-backside connections for components that are integrated on the backside of the chips. The front-side layout of the package is presented in fig. 2.8 with labels indicating each of the design components. The purpose of these components

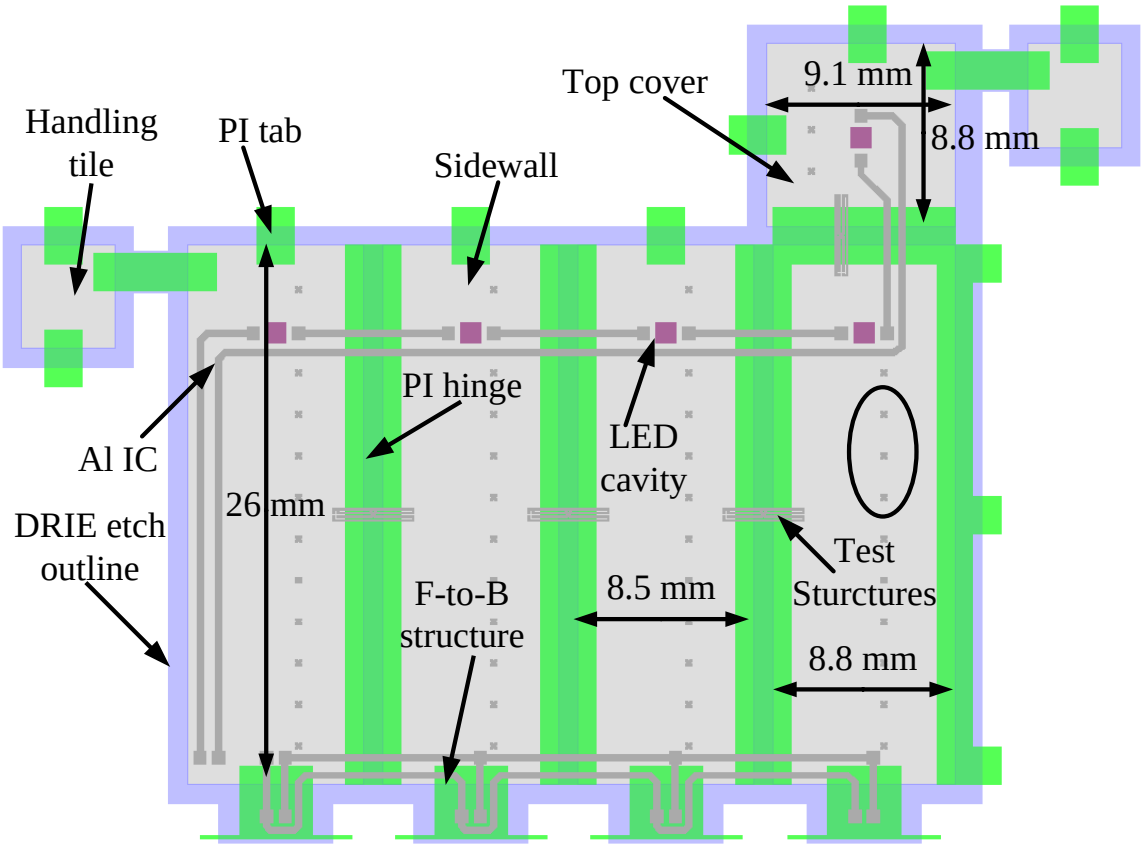


Figure 2.8: Front-side layout of proposed WLP design.

will now be discussed:

- *Handling tile.* An dummy piece of Si used to ease handling of fabricated devices using tweezers. It can be pealed off or cut with a blade after final device mounting.
- *Polyimide tab.* After processing is complete these tabs prevent the devices from falling out of the wafer. They are cut with a fine blade in subsequent post-processing steps when the structures need to be released.
- *DRIE etch outline.* Outline of area were the Si is etched from the backside for device release form the wafer.
- *Al interconnect.* Provides power for series connected LEDs on every sidewall of the package. The dimensions of interconnects and bonding pads are shown in fig. 2.9. Multiple combinations of line width and thickness were considered to have the required cross-sectional area. The thickness of $2\,\mu m$ was chosen to minimize the stress of encapsulated line, due to offset form the neutral plane. A 45° angle bend design was implemented to minimize the effect of current crowding [58].
- *Polyimide hinge.* The flexible part between the rigid Si sidewalls. The minimum width of the hinge (hypotenuse) to form a right angle between two Si islands with wafer

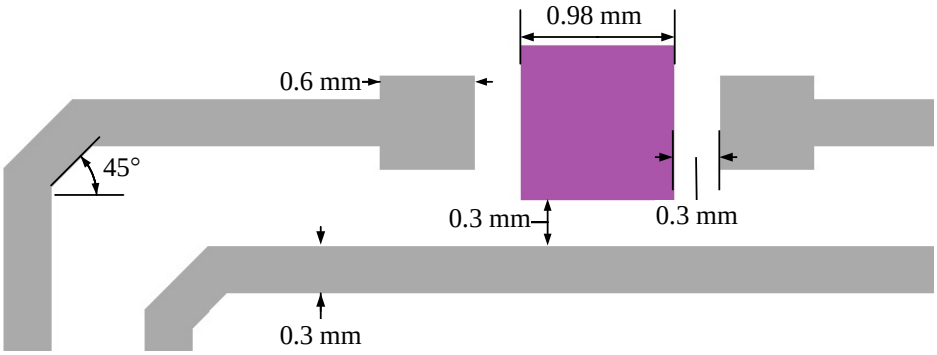


Figure 2.9: Dimensions of package interconnects and LED cavities.

thickness of 520 µm is $\sqrt{520^2 + 520^2} \approx 735$ µm. The width of 900 µm was designed to avoid stretching and form an arc-shaped bend, as shown schematically in fig. 2.10.

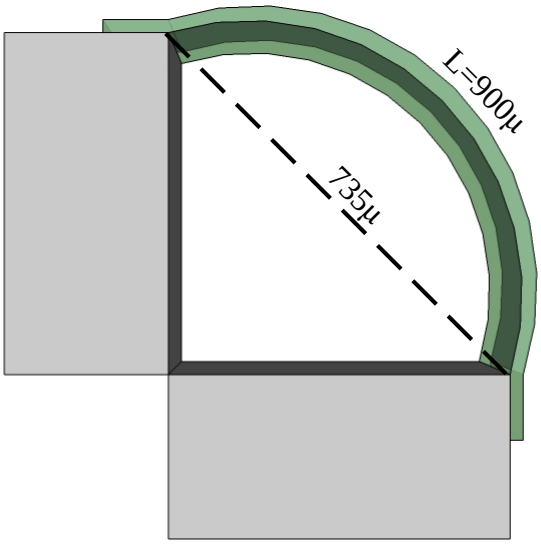


Figure 2.10: Schematic representation of right angle bend with arc-shaped polyimide hinge.

- *Front-to-back interconnect structure*. Al lines designed to overhang over the edge of the chip and encapsulated in polyimide with exposed contact pads fig. 2.11. The end of the structure is released from the wafer during through wafer backside etching. The

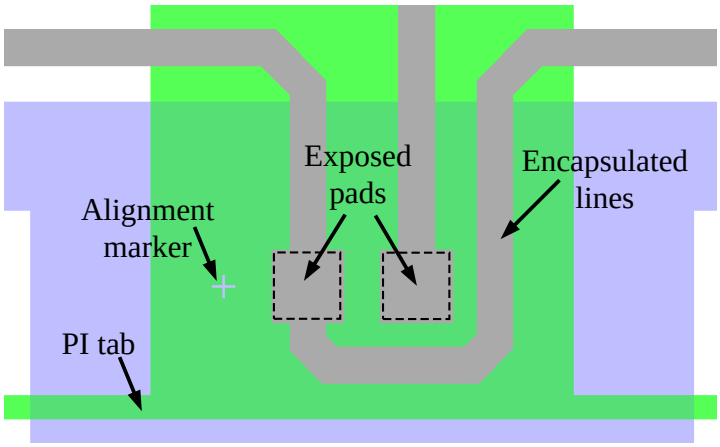
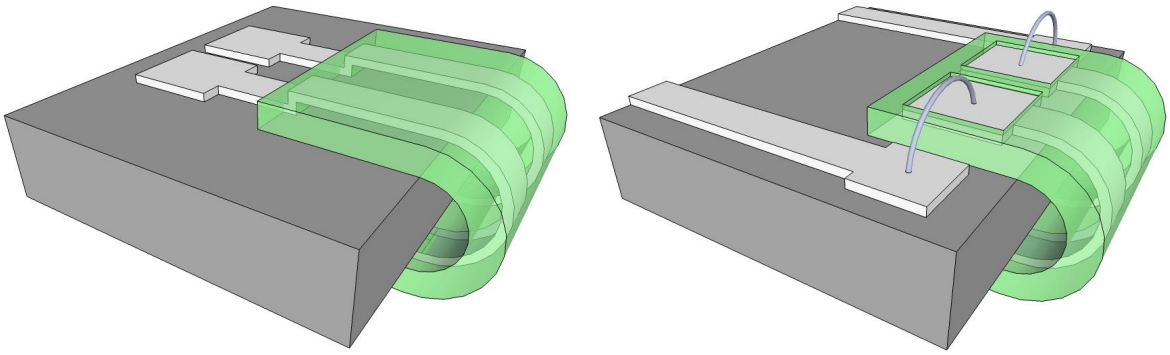


Figure 2.11: Polyimide based front-to-back interconnect structure.

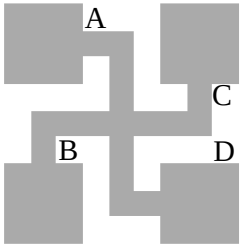
released structure can now be folded to the backside of the chip using a precision micro-manipulator. An alignment marker is added to aid with the placement of this PI strip on the backside. After folding, the bottom of PI layer is glued to the Si and the exposed contact pads are wire bonded to designated pads on the backside, as demonstrated in fig. 2.12. Such an interconnect desing proves a alternative to TSV based interconnect which requires additional complex processing steps. The proposed structure does not require additional lithographic steps and is integrated during flexible hinge and interconnect fabrication.



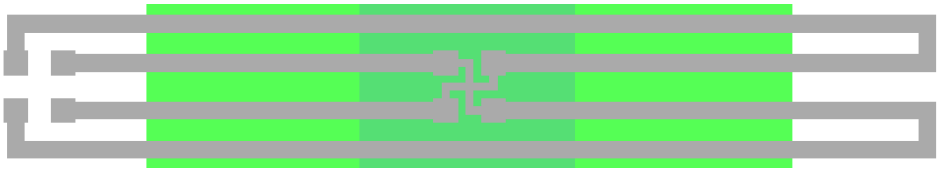
(a) Front-side view (b) Backside view

Figure 2.12: Schematic representation of front-to-back interconnection

- *LED cavity.* A tapered sidewall cavity etched in the Si substrate, used for housing the LED chips. The cavity is coated with a thin layer of Al and is used as a reflector to improve light extraction efficiency and directionality. The design aspects and integration process of LED cavities are discussed in chapter 4.
- *Electrical test structures.* Sheet resistance structures were added to the interconnect mask design (fig. 2.13). Sheet resistance ($R_s = \rho/t$) is the ratio between material resistivity (ρ) and layer thickness (t). The measurement is performed using the four



(a) Greek cross structure



(b) Greek cross structure encapsulated in PI hinge

Figure 2.13: Greek cross structures for sheet resistance measurements.

point probe (FPP) method. The layout of these structures is often referred to as the Greek cross structure [61]. A design with elongated traces was used for measurements

of resistance in the flexible bend (fig. 2.13(b)).The measurement is performed by forcing a current (I) between points A-B and measuring the voltage drop (V) across points C-D. Sheet resistance is calculated using the van der Pauw formula:

$$R_s = \left(\frac{V}{I}\right)\frac{\pi}{\ln 2} \tag{2.3}$$

By measuring R_s, the thickness of the deposited layer can be extracted since electrical resistivities of commonly used metals are known. The metal sputtering uniformity can therefore be evaluated by measuring sheet resistance at various points across the wafer.

- *Sidewalls and top cover.* The sidewall dimensions were chosen to be slightly smaller than the current G4 1W LED Capsule form Philips Lighting [43]. The last sidewall and top cover dimensions are larger to form an overlap with the edges of the other sidewalls for preventing adhesive leakage due to limited alignment precision during package folding.

A package design with 50% smaller physical dimensions was also added for demonstration purposes. This package does not include backside components nor front-to-back interconnections, but retains the same cross-sectional area of the interconnects as the full size design. A complete 4 inch wafer front-side layout is shown in fig. 2.14, which contains 2 full size and 2 half size packages. Package design and layout were realized using L-Edit v15.15 physical

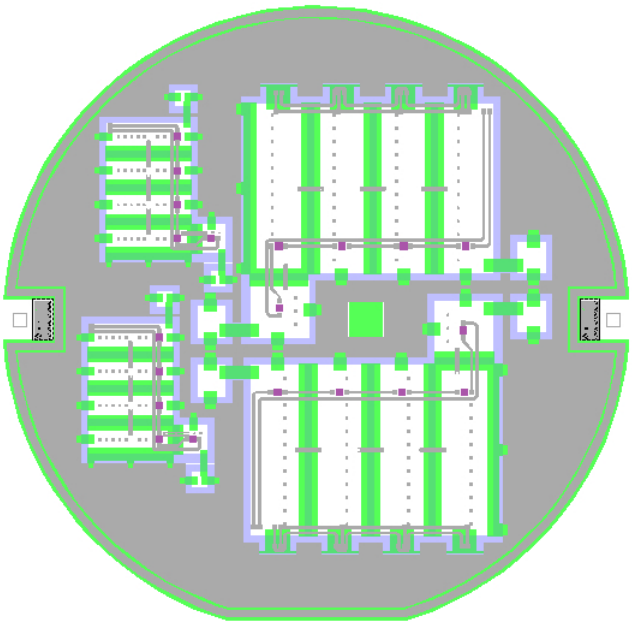


Figure 2.14: Full wafer front-side design layout.

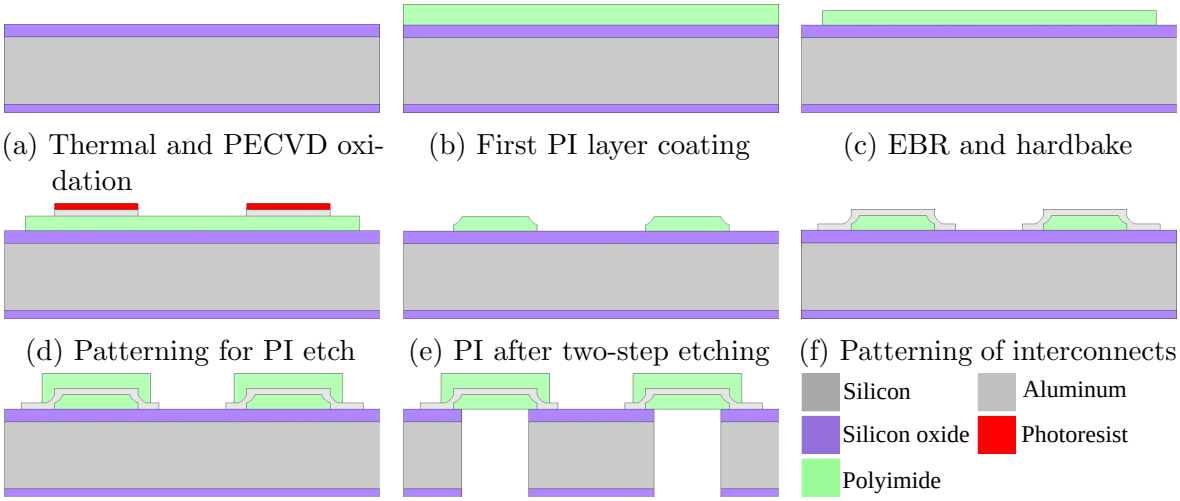
layout editor, by Tanner EDA. Mask fabrication was done in Dimes Technology Centre (DTC) of Delft University of Technology.

2.4 Flexible Interconnect Fabrication

Package fabrication was based on the Flex-to-Rigid (F2R) platform, designed for ultra-flexible medical sensor processing [62]. F2R was developed in collaboration between TU Delft and Philips Research. In this process polyimide is used to encapsulate aluminum interconnect

in the neutral bending plane. Some modifications were made to the processing sequence to incorporate additional features in the design.

Fabrication was carried out at the DTC class 100 cleanroom. 4 inch double-side polished (DSP) p-type Si wafers of 520 µm thickness were used as the substrate material. The process started with growing 300 nm of wet thermal silicon oxide (SiO_2) at 1000 °C on both sides of the wafer. This layer was used as an isolation layer for the backside integrated capacitors and part of the etch stopping layer for through wafer DRIE etching. An additional 1 µm of oxide was deposited at 400 °C by plasma enhanced chemical vapor deposition (PECVD) on the front-side to finalize the etch stop layer as shown in fig. 2.15(a). Then a layer of polyimide



(a) Thermal and PECVD oxidation (b) First PI layer coating (c) EBR and hardbake

(d) Patterning for PI etch (e) PI after two-step etching (f) Patterning of interconnects

(g) Patterning second PI layer (h) Backside DRIE

Figure 2.15: Flexible interconnect fabrication process.

was spin-coated. Durimide 100 Series 115A PI from Fujifilm was used. This material has Young's modulus of 3.3 GPa, CTE=32 × 10^{-6} K^{-1} and is self-priming for better adhesion to the substrate [63]. Wafers were cleaned in oxygen plasma for 5 min prior to applying the PI. A thin layer of adhesion promoter VM-652 from HD MicroSystems was spin-coated to further improve the adhesion to the substrate. PI was manually dispensed in the center of the wafer and spin-coated on a single wafer coating system fig. 2.15(b). The layer thickness is determined by the RPM as shown in fig. 2.16. With spin-speed of 1000 RPM layer thickness

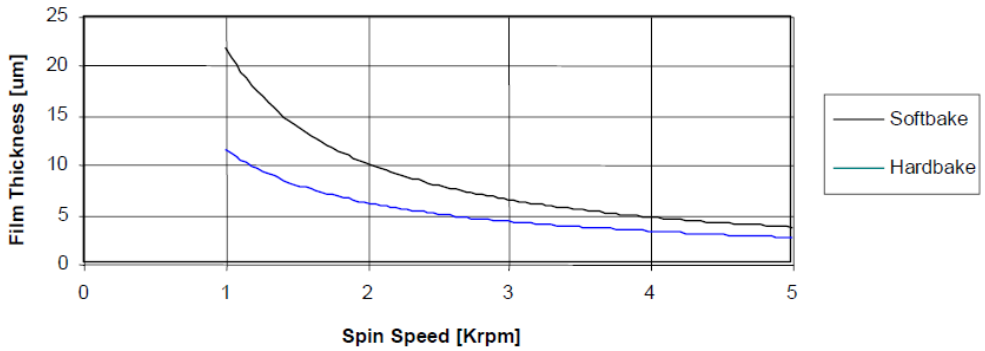


Figure 2.16: PI 115A spin curve [63].

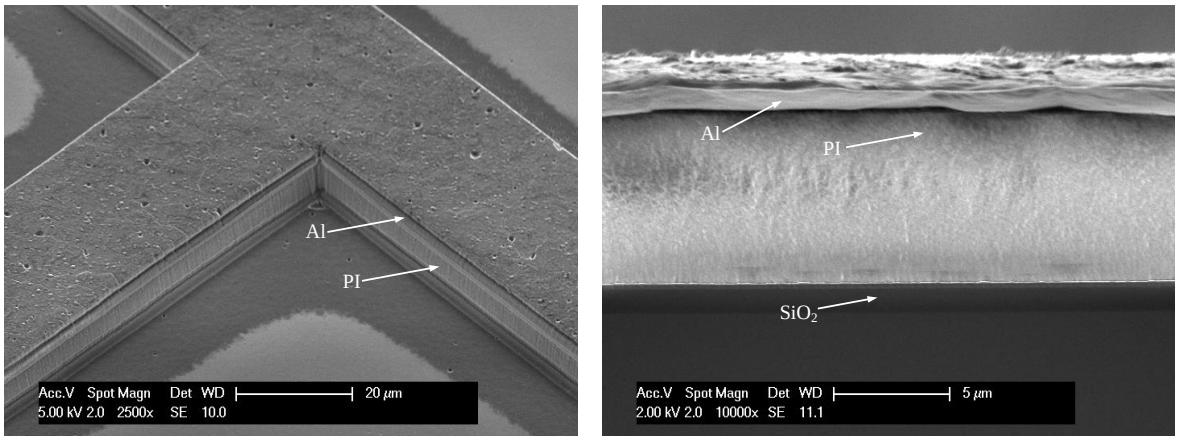
of approximately 13 µm was obtained. The layer was then softbaked on a hotplate at 120 °C

for 6 min. Edge bead removal (EBR) and backside clean are required to avoid contamination of equipment with PI during further processing steps. 3 µm of positive photoresist was spin-coated and exposed on a full wafer aligner using an EBR mask (a circle with diameter few millimeters smaller that the wafer). The exposed photoresist is developed and PI is etched using a 2.5% TMAH solution for 12 min with periodic agitation. It is recommended to carefully inspect the the resist coating after exposure, for the presence of small pinholes or bubbles. These will result in circular imperfections etched in PI during EBR. It was observed that number of resist coverage defects is reduced by applying a thicker resist layer (3 µm) due to its higher viscosity. After EBR the remaining resist is stripped with acetone and wafers are cleaned with isopropyl alcohol (IPA) fig. 2.15(c). Hardbake of the PI was carried out in a vacuum oven at 400 °C for 2 h in N_2 ambient at 200 mbar and cooled to room temperature without pressurizing the oven to avoid PI oxidation. The prolonged curing time is needed to minimize the out-gassing of the polymer during the following high temperature processing steps. The final PI layer thickness after hardbake is approximately 9 µm.

After the first PI layer is processed two approaches to form interconnects are possible:

1. Pattern interconnect directly on PI.
2. Pattern first PI layer prior to interconnect processing.

In the first case Al is sputtered on the first PI layer and interconnects are patterned. Using this approach the interconnects are on PI everywhere across the wafer. A second PI layer can be applied (same process as for first layer) and the metal is encapsulated. Both PI layers are patterned simultaneously by RIE. Midway through the PI etch process Al lines are exposed and act as a mask layer for the PI underneath, resulting in interconnects formed on a layer of PI as shown fig. 2.17. This method allows to reduce processing complexity since



(a) Al on PI tilted 45° (b) Al on PI cross-section

Figure 2.17: Al interconnects on polyimide.

one lithography and one etching step are avoided. It is used to fabricate flexible cables or other encapsulated structures than can be peeled off from the substrate wafer [51]. Two main drawbacks of fabricating interconnects on top of a soft, insulating PI layer are inadequate heat dissipation and delamination. Poor thermal conductivity of PI will reduce the maximum current density the interconnect can handle without burning due to Joule heating. After fabricating the first test samples, problems occurred when attempting to wire bond LEDs

to the fabricated interconnects. When ultrasonic energy was applied to the bonding surface, delamination of Al was observed on multiple samples and no successful bonds were achieved, rendering such an approach not suitable for this work. An example of Al delamination is shown in fig. 2.18.

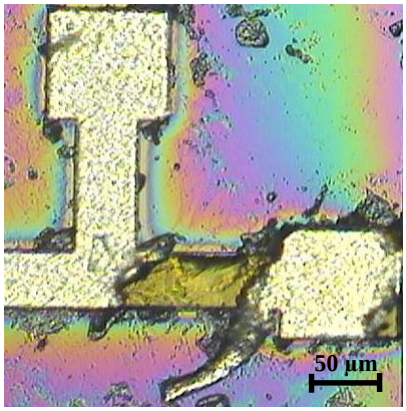


Figure 2.18: Interconnect delamination from PI.

The second approach requires the first polyimide layer to be patterned before Al sputtering and was used to fabricate the final version of the LED package. A hard masking layer is needed to pattern PI, as oxygen plasma is used for etching which would also etch the photoresist mask. SiO_2 and Al are suitable masking materials for PI etching and both were used during the process flow. A 250 nm layer of Al was sputtered and patterned with the PI mask (fig. 2.15(d)). There is no need to remove the photoresist layer, as it will be etched together with PI. Polyimide was etched in two steps to improve the step coverage of spin-coated photoresist for the subsequent interconnect patterning. The PI is firstly etched isotropically in pure O_2 plasma using a barrel-type etcher (TEPLA IPC 9200), commonly used for photoresist stripping, and then anisotropically in inductively coupled plasma (ICP) RIE reactor (Trikon Omega 201). The two step etch method was presented by Mimoun et al. [64]. It was observed that when PI 115A was fully etched isotropically in pure O_2 there were some Si rich residues left over on the wafer which originate form the adhesion promoter inside the PI and VM-652 applied before PI spinning. Same sort of residues were observed during etching tests conducted in this work. By adding a small amount of CF_4 (5%) to the iso-etching gas mixture no residues remained as fluorine is known to etch Si. Since the barrel etcher in DTC cleanroom does not have a CF_4 gas connection, the PI was etched isotropically for approx. 6 µm. The remaining PI was etched anisotropically in ICP-RIE with the plasma composition of 80% O_2, 13% H_2 and 7% CF_4. The resulting PI edge profile after the two-step etch is shown in fig. 2.19. The etching uniformity of the barrel etcher is very poor and the etch rate is non-linear and increases with raising chamber temperature. The isotropic etching was done in short time intervals of 1–2.5 min. After each step the wafers were rotated 180° to improve etching uniformity and the chamber was cooled to room temperature. Mapping of iso-etching depth across the wafer after multiple short intervals is shown in fig. 2.20, which indicates that the edges of the wafer are etched faster than the center.

After the two-step PI etching the masking layer was removed in wet Al etchant PES (mixture of phosphoric (H_3PO_4), acetic (AcOH) and nitric (HNO_3) acids, with ratios of

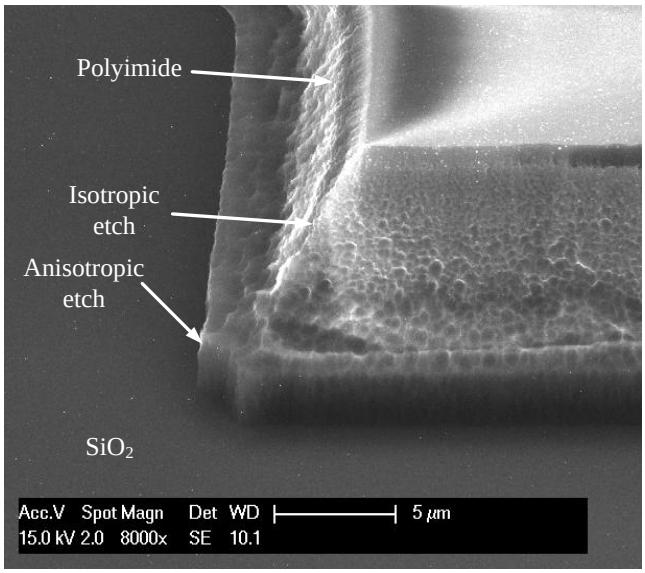


Figure 2.19: Polyimide edge profile after two-step plasma etching.

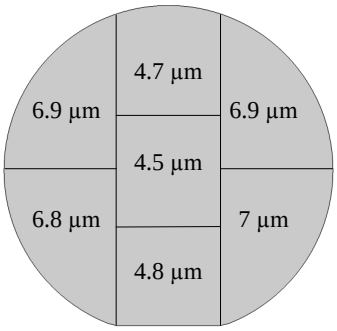


Figure 2.20: Non-uniformity of isotropic etching with barrel etcher.

77:19:4 respectively). The so called "wine glass" PI sidewall profile is formed (fig. 2.15(e)). Afterwards a 2 µm layer of Al was conformally sputtered and wet etching was again used to pattern the interconnects. It was decided to use wet etching due to obtained testing results and designed package characteristics. The minimum feature size of the metal mask was 30 µm so there was no risk of delamination due to isotropic undercut. During the first fabrication test run it was determined, that, after plasma etching of Al, the photoresist masking layer gets heavily cross-linked and wet stripping with acetone or N-Methyl-2-pyrrolidone (NMP) does not completely remove it. Using NMP showed better results, however there was a noticeable amount of resist flake residues across the wafer. To fully remove the cross-linked resist, an oxygen plasma clean using short process steps (similar to iso-etch of PI) would be required which would result in non-uniformly etched surface of the underlying PI. Another reason to use wet etching was the thinning of spin-coated photoresist at the crest of the PI structures as seen in fig. 2.21. In case plasma etching were to be used, the thin resist would be etched exposing the metal line, resulting in partial or full gaps in the interconnect lines.

From fig. 2.21 it is evident that there is a buildup of resist at the base of the slope. The photo-sensitive material used for Al patterning was SPR3017M [65], which is a positive-tone, dyed resist with intended layer thickness up to approximately 3 µm. Due to the addition of highly absorbing dye, thicker resist layers cannot be fully penetrated by UV light. In our case,

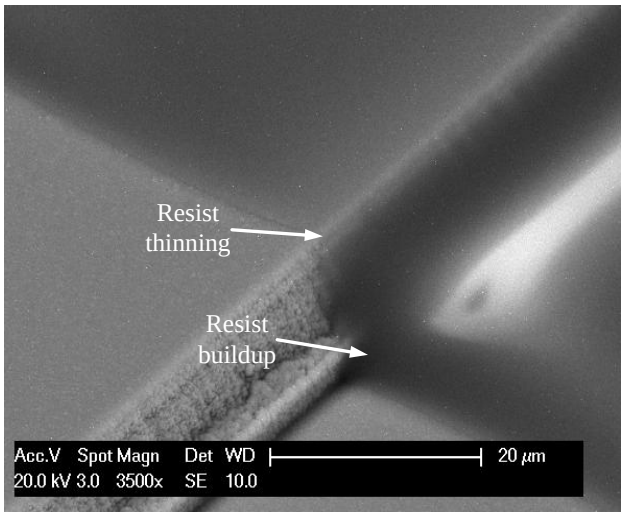
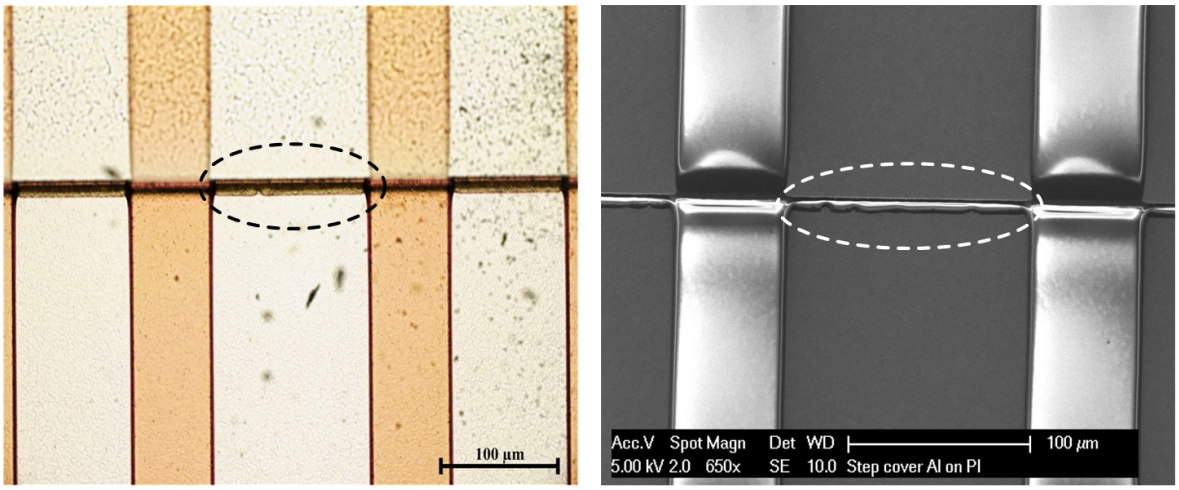


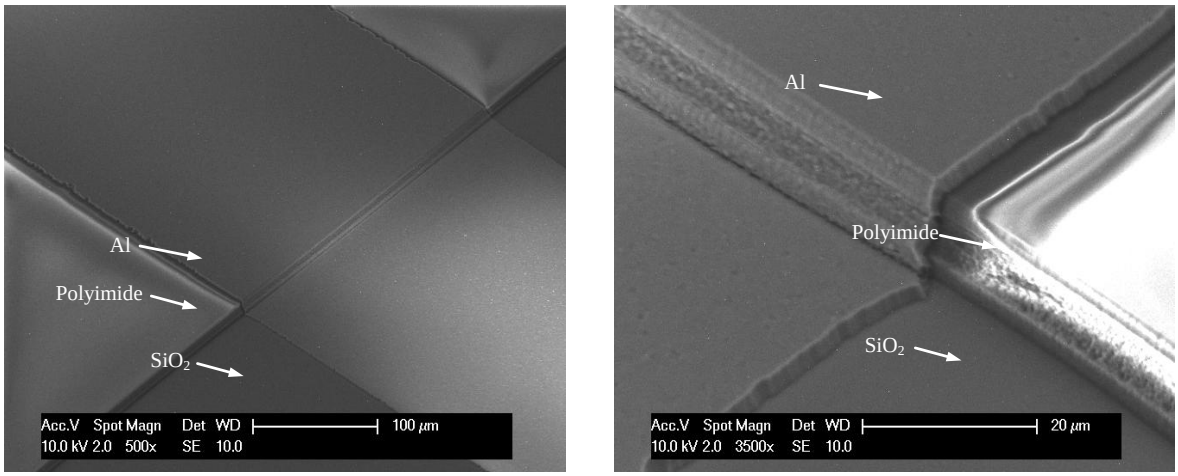
Figure 2.21: Step coverage of 3 µm photoresist indicating the non-uniform layer thickness along the PI slope.



(a) Optical view (b) SEM view

Figure 2.22: Resist remainder at the base of PI slope after single exposure and development.

the resist layer thickness at the base of the slope exceeded the maximum value. As a result, a thin layer of unexposed resist layer remained after development (fig. 2.22). The remaining resist masks the Al during wet etching causing short-circuits of the interconnects. In [64] negative resist was used for metal patterning. Short circuits are avoided when using negative resist as the unexposed areas are developed away. However, to fully expose the pattern, higher energy dose is needed to avoid undercuts at buildup areas. As a results, cross-linking would once again cause problems during wet stripping. A double exposure method, known as "optical drilling" was utilized to properly pattern the positive resist for Al etching. A two cycle optical drill was performed, consisting of exposure and development without any baking steps. Best results were obtained with increasing the necessary nominal exposure dose by 10% and dividing it into two equal parts for the exposures. After the last development step the material buildup is fully developed and the resist is baked at 120 °C for 1 h to improve the adhesion during wet etching. After 17 min of PES etching the interconnects were formed without any notching at the PI slope regions (fig. 2.23).



(a) Al line on Si and PI

(b) Zoom-in of Al on PI slope

Figure 2.23: Patterned interconnects on PI slope.

After the metal layer was patterned the second layer of polyimide was spin-coated using the same procedure as for the first. The PI was patterned only anisotropically using ICP-RIE and the flexible hinges were formed (fig. 2.15(g)). The final step in the fabrication of silicon islands connected with bendable interconnects is DRIE through the wafer from the backside. 6 µm of PECVD SiO_2 were used as a masking layer and the etching was carried out in the SPTS Omega Rapier i2L DRIE etcher. An example of a flexible test chip fabricated based on F2R process is shown fig. 2.24.

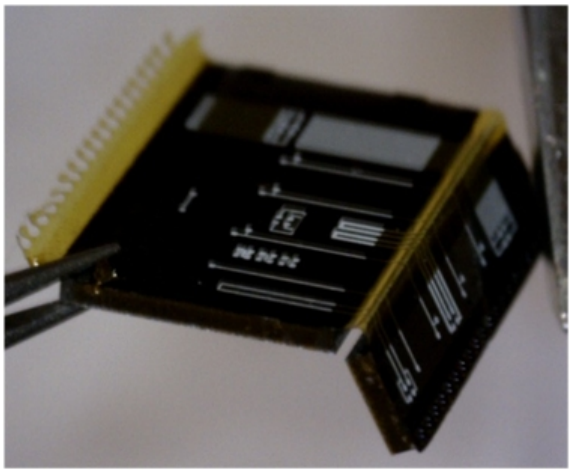


Figure 2.24: Flexible test chip.

2.5 Chapter Summary

This chapter was dedicated to flexible and stretchable interconnect and electronics. First, an overview of current state of the art in this field was presented and notable examples were reviewed. The next sections focused on the design and fabrication of flexible interconnect that is an essential part of the 3D SSL WLP. Package layout was presented and each component described individually. Fabrication steps were discussed in detail including challenges that were encountered. The following chapters will focus on the remaining parts of the package design and complete processing sequence.

Chapter 3

Embedded Capacitor Integration

3.1 Introduction

Typical SSL packages employ discrete passive components for the assembly of LED driver circuitry. These individually packaged components are mounted on PCBs using surface mount technology (SMT) (e.g. ceramic capacitors) or through hole mounting (e.g. electrolytic capacitors). This chapter demonstrates the integration possibilities of embedded capacitors in the designed wafer level package. Standard semiconductor processing is employed to fabricate and interconnect these components directly on the silicon substrate. Metal-insulator-metal (MIM) capacitors with horizontal parallel plate type structure and aluminum electrodes are integrated on the backside of each sidewall of the proposed package, using BEOL compatible processes.

3.2 Current State of the Art

The design of integrated capacitors depends on the intended application. The general classifications of capacitor functions in integrated circuits are [66]: filtering, A/D conversion, termination, decoupling, energy storage. Common capacitor structures are MOS (metal-oxide-semiconductor), PIP (polysilicon-insulator-polysilicon) and MIM (metal-insulator-metal). MOS is the integral part of any MOSFET device and has variable capacitance, dependent on the bias voltage and operation frequency. PIP capacitors use degenerately doped polysilicon for the electrode plates and therefore can tolerate high temperature processing (LPCVD). The polysilicon does however exhibit depletion effects which cause voltage dependencies of capacitance and has larger sheet resistance in comparison to standard metal electrodes. In this work the MIM capacitor structure with Al electrodes was chosen.

The development of MIM capacitors is governed by ITRS, with the roadmap of requirements currently presented up to the year 2026 [7]. The parameters that characterize MIM capacitors are as follows:

- *Capacitance density.* The capacitance per unit area:

$$C = \frac{k\epsilon_0}{t} A = C'A \tag{3.1}$$

where C – capacitace in farads, k – relative dielectric permittivity, ϵ_0 – electric constant ($\epsilon_0 \approx 8.85 \times 10^{-12}\,\mathrm{F/m}$), t – thickness of dielectric layer, C' – capacitance density. It is evident that there are two approaches to increase the capacitance density - using a dielectric with higher permittivity or reducing the layer thickness.

- *Voltage linearity.* Indicates the variation of capacitance with applied voltage. This variation is defined by voltage coefficient of capacitance (VCC), which is extracted from the C-V measurement results by fitting the characteristic equation [67]:

$$C(V) = C_0(\alpha V^2 + \beta V + 1) \tag{3.2}$$

where C_0 – zero bias capacitance, α and β – quadratic and linear VCC respectively. A typical C-V curve of a MIM device is shown in fig. 3.1.

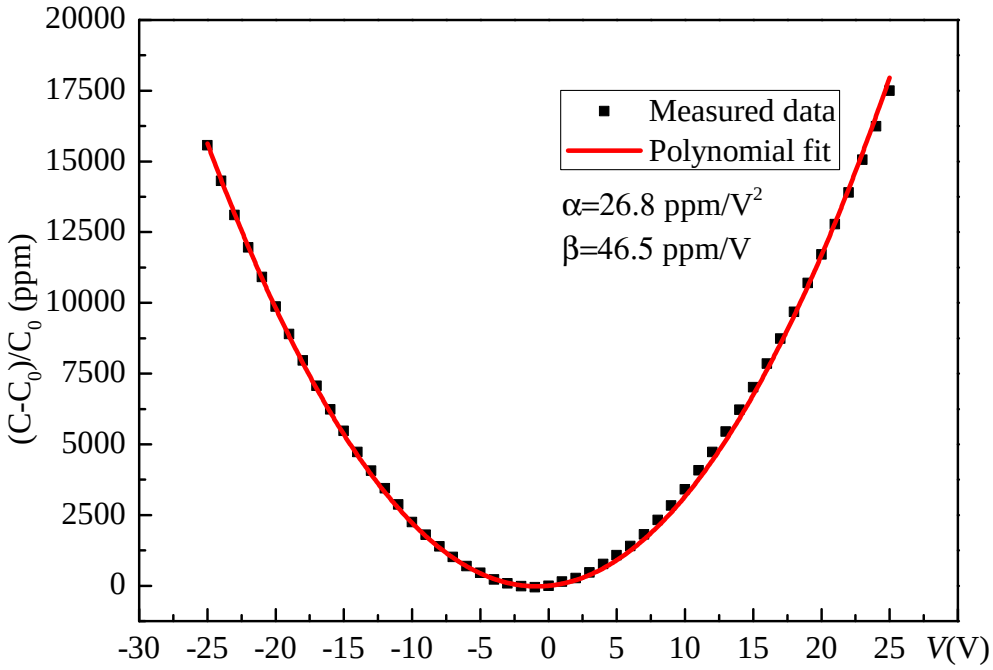


Figure 3.1: C-V characteristic of MIM capacitor with 95 nm Al_2O_3 dielectric layer. The VCC parameters are extracted by fitting eq. (3.2).

- *Temperature coefficient of capacitance (TCC).* The variation in capacitance value with temperature is an important parameter to consider since most of the integrated components operate at varying thermal conditions [68]. In case of SSL applications, the luminaire temperature gradually increases when lights are switched on and the component design needs to account for that. TCC is usually expressed in ppm/°C:

$$TCC = \frac{10^6}{C}\frac{dC}{dT} \tag{3.3}$$

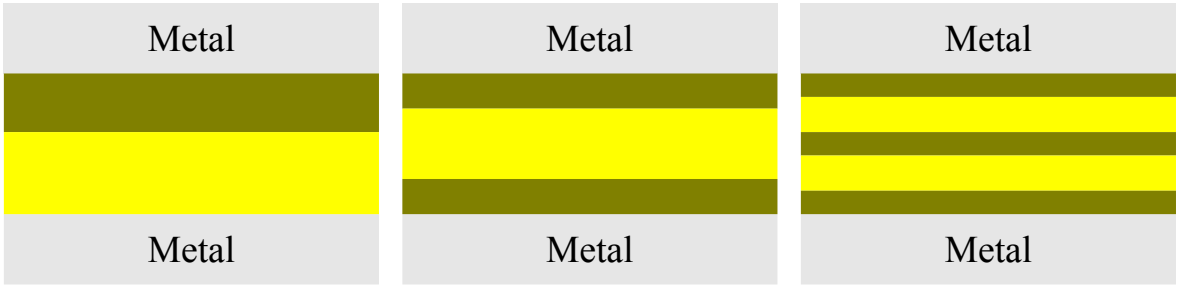
- *Leakage current density.* Low leakage current is an indicator of dielectric layer quality. Typically leakage current density (J) is measured at the supply voltage level. ITRS requirement for RF applications is $J < 1 \times 10^{-8}\,\mathrm{A/cm^2}$.
- *Quality factor (Q).* A measure of energy loss due to heat dissipation in an oscillating

system. In case of capacitors, energy losses occur in the dielectric layer as well as due to non-zero plate resistance. In publications, sometimes the dissipation factor (DF) or loss tangent ($\tan\delta$) is cited, which is the reciprocal of Q.

For a long time SiO_2 ($k = 3.9$) has been the industry standard dielectric material for integrated capacitors and increasing the capacitance density was achieved by thinning the layer. However with thinner layers the leakage current raises to no longer acceptable levels. The demand for higher capacitance densities of $10\,nF/mm^2$, with VCC<$100\,ppm/V^2$ requires dielectric materials with high permittivities (see appendix D for a list of dielectric materials investigated for MIM applications). Aluminum oxide (Al_2O_3), with $k = 9$, has been demonstrated as promising replacement for SiO_2 [69]. Hafnium oxide HfO_2 ($k = 25$) has also been successfully applied for high density capacitors [70]. A wide range of binary metal oxides have been investigated for MIM applications, including rare earth materials (e.g. La_2O_3 [71], Sm_2O_3 [72], Eu_2O_3 [73]). The required capacitance densities have been achieved and exceeded by more than 150% ($28\,nF/mm^2$) by employing TiO_2 dielectric with $k = 65$. Meeting the specifications for voltage linearity in combination with the reported C' values by simply using a single binary oxide layer has not been achieved to date. Leakage current specifications are also difficult to meet, as high-k dielectrics tend to have lower band-gap energies, resulting in higher charge leakage between the metal-insulator junctions [74].

MIM capacitors fabricated with ternary oxide dielectrics have also been extensively reported. These films are formed by combining two binary oxides. The material combinations are formed such that one would have a high dielectric permittivity and the other would suppress leakage and VCC. A typical example is a combination of HfO_2 and Al_2O_3 [67]. It was demonstrated that by varying the material compositions trade-offs between capacitance densities and VCC or leakage currents could be achieved. Compositions with more than two metal oxides, like $BaSm_2Ti_4O_{12}$ [75] were also investigated. In this case, negative α coefficient values were obtained, that are common for SiO_2, but have not been reported for most of the binary metal oxides.

Dielectric layer stacking is another highly investigated method to alter the properties of MIM devices. Possible stacking approaches, according to [76], are show in fig. 3.2. Combining



(a) Stacked structure (b) Sandwich structure (c) Laminate structure

Figure 3.2: Approaches to dielectric layer stacking.

a higher and lower permittivity film allows to reduce leakage currents as well as VCC. The capacitance density is slightly decreased due to higher overall layer thickness and lower effective k value of the stacked layers in comparison to mono-layer structures. The equivalent

capacitance (C_{eq}) can be calculated using the equation for capacitors in series:

$$\frac{1}{C_{eq}} = \sum_{i=1}^{n} \frac{1}{C_i} \tag{3.4}$$

where C_i is the capacitance of each dielectric layer in the stack, obtained using eq. (3.1). Stacked layers (fig. 3.2(a)) exhibit asymmetric C-V and leakage current characteristics, because the energy barrier highs between the dielectric and metal layers differ at the top and bottom interfaces [76, 77]. To overcome these non-linearities the sandwich (fig. 3.2(b)) structures are fabricated. The higher k layer is placed between two layers with lower k and higher band-gap. This way the barrier hight for both metal-insulation interfaces is the same, unless top and bottom electrodes are fabricated using different conductors. A further improvement to dielectric stacking is the laminate structure, where the higher permittivity layer is not continuous but is sub-divided by low-k inserts, fig. 3.2(c). It has been reported that laminate structures with 5 or more layers effectively reduce the leakage currents and VCC without decreasing the capacitance density. Highly investigated sandwich and laminate structures are made up of hafnium and aluminum oxides [78, 79]. Another promising k-stacking approach is to combine materials with positive and negative VCC coefficients. SiO_2 is known to have negative α values. When combined with a metal oxide (e.g. HfO_2 or TiO_2) capacitors with enhanced voltage linearity and high capacitance density can be achieved. The canceling effect has been demonstrated for MIM capacitors that meet the ITRS requirements for both $C' = 11.2\,\mathrm{nF/mm^2}$ and $\alpha = 30\,\mathrm{ppm/V^2}$ [80]. The improved performance of stacked MIM structures, in comparison to single layers, comes at the expense of increased processing complexity, due to alternating layer depositions.

Energy storage capacitors are allowed to have less stringent requirements for VCC, leakage current and high frequency loss tangent. The main challenge lies in forming structures with extremely high capacitance densities above $100\,\mathrm{nF/mm^2}$. Ferroelectric materials with very high dielectric permittivities [66] are a promising solution. MIM capacitors using ferroelectric $PbZrTiO_3$ (PZT) thin films [81] have been demonstrated. A capacitance density of $105\,\mathrm{nF/mm^2}$ has been obtained with a two layer stacked capacitor structure connected in parallel (fig. 3.3). Each layer was 270 nm thick with very high dielectric permitivity k=1600

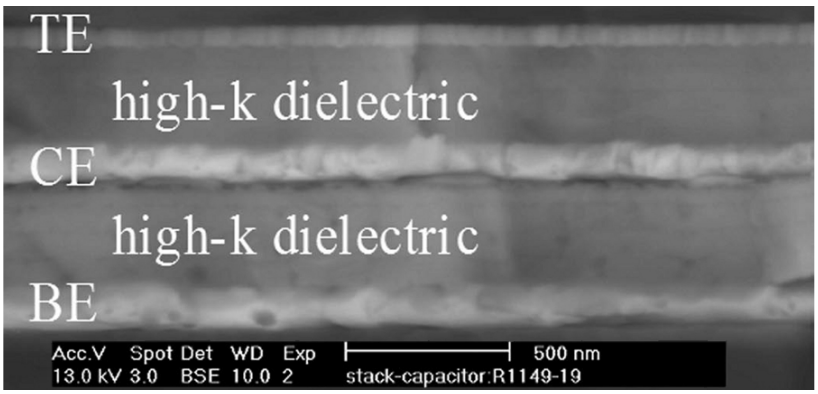
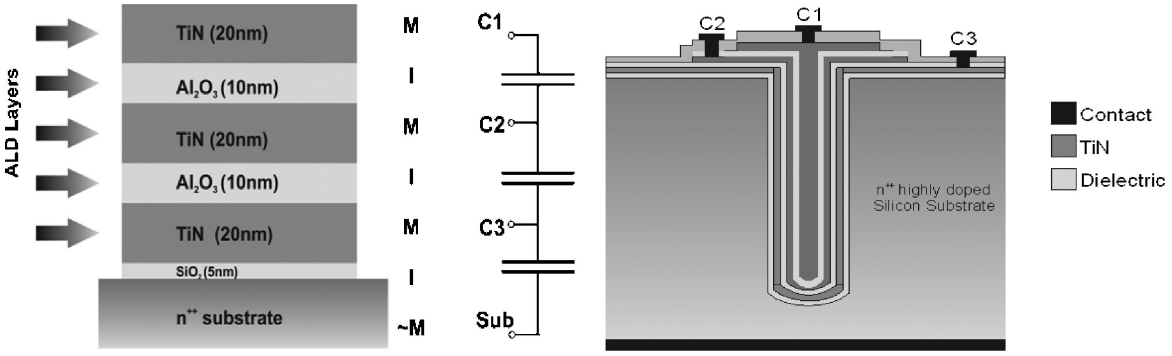


Figure 3.3: A parallel capacitor stack, with CE being the shared plate. MIMIM structure.

and breakdown voltage of 90 V. $BaSrTiO_3$ films with k=420 have been employed for tunable

MIM capacitors [82]. Ferroelectric materials are not as widely used as paraelectrics for integrated capacitors due a number of reasons. First of all, ferroelectrics exhibit non-linear dielectric constant variations with temperature and bias voltage [82]. Secondly, the fabrication of ferroelectic materials is based on the sol-gel process. It is solution based process that involves spin coating on the substrates. Spin-coating has a limited control of layer thickness for thin, uniform layers. Finally, these solutions need to undergo rapid thermal anneal (RTA) treatments at temperatures that are above 400 °C, making the process incompatible with standard BEOL.

High density MIM capacitors can be fabricated using the more easily obtainable binary metal oxides by increasing the effective area of the capacitors, while the lateral area remains unchanged. The effective surface area of these components can be substantially increased by etching high aspect ratio (AR) trenches in the silicon substrate, forming 3D MIM devices. These trenches are then lined with alternating metal-insulator layers. Capacitance densities of 440 nF/mm^2 combined with 6 V breakdown voltage, using the structure shown in fig. 3.4, were reported [83]. In this case, macro-pore arrays with aspect ratio of 20 were DRIE



(a) MIMIMIM layer stacking (b) Cross-sectional view

Figure 3.4: 3D MIM trench capacitor: (a) the schematic of the stacked structure. Highly doped substrate wafer is used as bottom electrode. (b) Cross-section schematic.

etched. Titanium nitride TiN was used for the capacitor plates and Al_2O_3 for the dielectric layers. Breakdown voltages obtained were the same as for planar versions, indicating excellent dielectric layer conformality inside the etched trenches. The main challenges related to the fabrication of 3D capacitors are the etching of high aspect ratio trenches and the conformal deposition of conductive and dielectric layers. Highly conformal layers are obtainable by atomic layer deposition (ALD). ALD is a two-cycle self-limiting CVD process. Special precursor gases are sequentially injected into the reaction chamber. The first gas coats the substrate with a monolayer of material by chemisorption. Once the surface is saturated the excess gas is purged from the chamber and the second gas is injected, which reacts with the layer of the first precursor and a layer of the desired material is formed. The second gas is then pumped out of the chamber and the cycle can be repeated many times to obtain highly uniform thin-film layers [84]. The main drawback of ALD is the slow deposition rate due to the self-limiting nature of the process. Some examples of layers that can be deposited with ALD: conductors – Co, Cu, Ni, Ru, Pt, TiN, W [85]; dielectrics – Al_2O_3, AlN, HfO_2, LaO_2, TiO_2, Ta_2O_5, TaN, ZrO_2, [86]. 3D trench capacitors have been successfully commercialized by a spin-off company

of NXP Semiconductors, IPDiA. An investigation of the material and processing requirements to integrate a high density energy storage capacitor in the 3D WLP package is presented at the end of this chapter.

3.3 Embedded Capacitor Design

The driver circuit design of the G4 1W LED capsule is assembled from separate components on a PCB and discrete capacitors – ceramic and electrolytic. Planar MIM capacitors were integrated at the backside of each sidewall of the proposed package to demonstrate how discrete components could be replaced by their embedded counterparts.

The targeted breakdown voltage of the capacitors was 25 V, which is the rated voltage of the 68 µF electrolytic capacitor of the G4 circuit [87]. For the dielectic material thermal ALD Al_2O_3 was used and the electrodes were Al. The layout of the capacitors in the package design is shown fig. 3.5. Only two lithography steps were required to fabricate the capacitors.

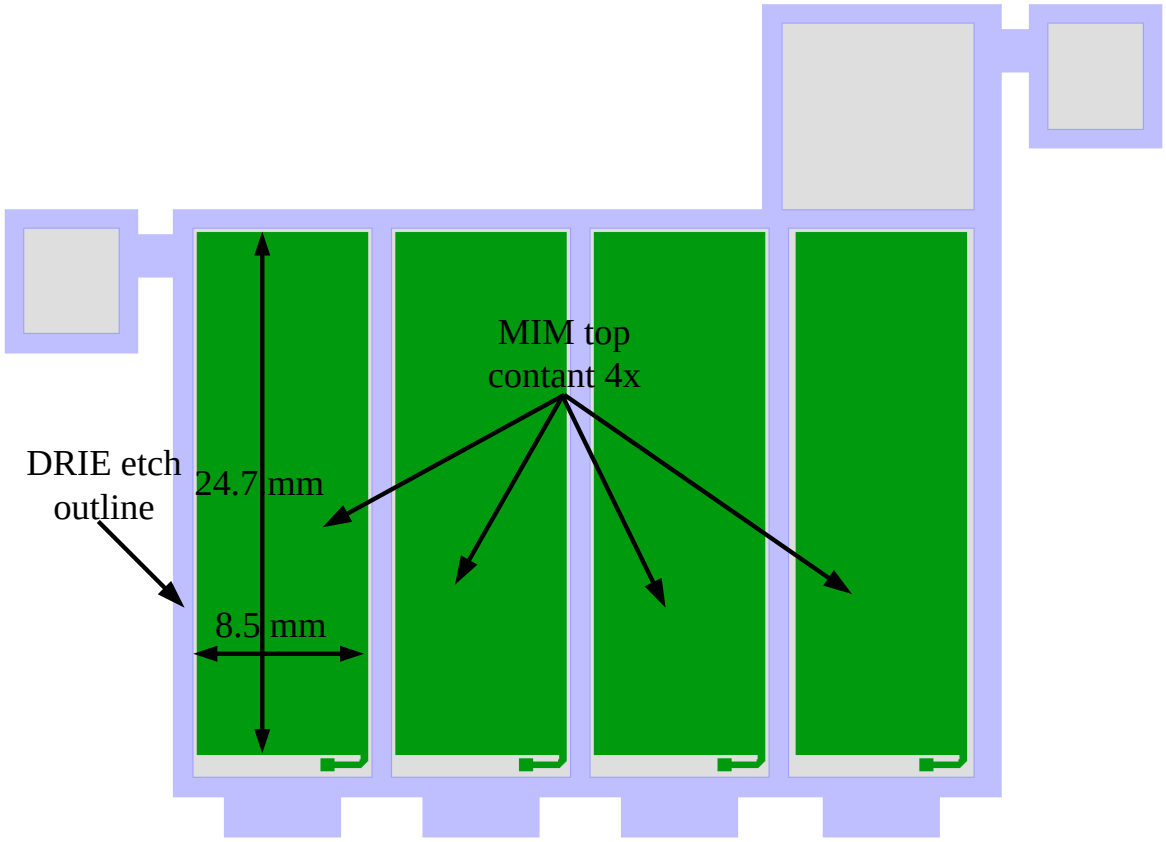


Figure 3.5: Backside layout of proposed WLP design, showing the dimensions of MIM capacitors.

Only the dielectric layer and top plate with bond pads was patterned. Spacings were left between the DRIE outline and the top plate border to avoid possible damage during though wafer etching (fig. 3.6). The bottom plate was patterned together with DRIE outline. All four capacitors can be connected in parallel using the front-to-back structure discussed in section 2.3. The surface area of one capacitor including bondpad connection was 200.97 mm^2.

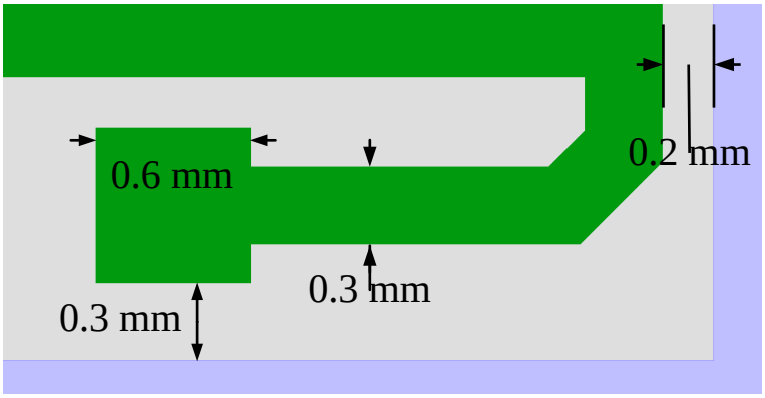


Figure 3.6: Dimensions and spacings on the edge of capacitor plate.

3.4 Embedded Capacitor Fabrication

The MIM capacitors were fabricated on the backside of 4 inch double-side polished Si wafers with 300 nm of thermally grown wet SiO_2 at 1000 °C (fig. 3.7(a)). 2 µm of Al were sputtered

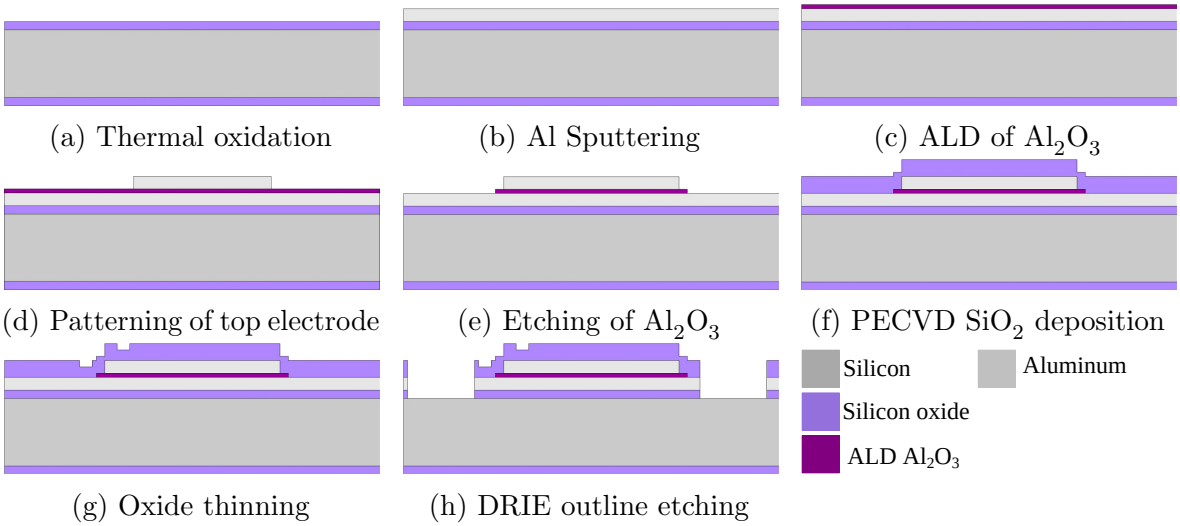


Figure 3.7: MIM capacitor fabrication process.

at 25 °C to be used as the bottom electrode (fig. 3.7(b)). Al_2O_3 was then deposited using ALD directly on the unpatterned bottom electrode (fig. 3.7(c)), using thermal ALD reactor ASM F-120 SAT. The precursors used for Al_2O_3 deposition were trimethylaluminum (TMA) and H_2O. The resulting reaction is:

$$\underset{\text{TMA}}{2\,Al(CH_3)_3} + 3\,H_2O \longrightarrow Al_2O_3 + 3\,CH_4 \tag{3.5}$$

Deposition was carried out at 300 °C chamber temperature. The layer growth rate was determined to be 0.94 Å/cycle. After 455 cycles the estimated average layer thickness was 43 nm. Then 2 µm Al layer was sputtered and patterned to form the top electrode. A special Al RIE etching recipe was made, that uses endpoint detection and isotropic overetch step to selectively land on the thin Al_2O_3 layer, as shown in fig. 3.7(d). The top plate was patterned again using negative photoresist with some offsets to make an Al_2O_3 outline around the top

plate. The dielectric layer was then etched, this time using a RIE recipe with start point detection to land on the bottom Al electrode without significant overetch (fig. 3.7(e)). At this stage the capacitors are fabricated and need to be protected from damage during other processing steps of the WLP. 6 µm of PECVD SIO_2 were deposited on top of the capacitors at 400 °C (fig. 3.7(f)). This layer serves not only as protection for the capacitor but also as the etching mask for the though wafer DRIE. The oxide layer was then patterned with contact openings mask and thinned by approximately 1.2 µm as shown in fig. 3.7(g). The SiO_2 layer was then patterned again with the backside though wafer DRIE mask. 6 µm of positive photoresist were used as a masking layer because multiple etching steps were required to land on the Si substrate. First, the wafers were placed in the oxide etcher with fluorine based recipes to etch the top oxide masking layer. The following step was to etch 2 µm of Al in the chlorine based ICR-RIE system and hence pattern the bottom electrode of the capacitors. The etching was then finalized with a short step in the oxide etcher again to remove the underlying layer of 300 nm thermal oxide. The resulting patterned wafer backside after etching and photoresist removal is shown fig. 3.7(h). At this stage the backside processing was suspended with capacitors still fully covered with PECVD SiO_2. The contact openings are only exposed after performing the backside wafer etching. The complete process flow to fabricate the WLP will be discussed in chapter 4.

3.5 Theoretical Estimations for High C' MIM Integration

This section will cover the theoretical estimations as well as preliminary experimental tests to integrate a high density MIM capacitor as a replacement for the discrete energy storage component. Electrolytic capacitors are bulky and occupy a lot of space on the PCB. In case of the G4 capsule, the PCB is shown in fig. 3.8. It is clearly evident that the electrolytic

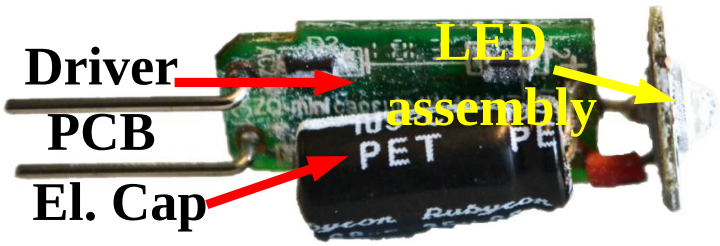


Figure 3.8: Philips G4 capsule PCB layout.

capacitor is the biggest component of this LED module and takes up 5.5% of the entire volume of the bulb. The specifications of these electrolytic capacitors are summarized in table 3.1. Integrating such a large capacitance value combined with high breakdown voltage on Si with limited surface area is very challenging. Calculations were made to determine possible design space options to integrate a 3D trench capacitor. The available planar surface area was chosen to be the same as for the backside capacitors, i.e., $4 \times 200.07\,mm^2$. The relationship between the breakdown electric field E_{bd} and the dielectric constant needs to be taken into consideration to find the optimum combination between layer thickness and breakdown. This relationship has been investigated and an approximate dependency of $E_{bd} \sim k^{(-1/2)}$ has been

Table 3.1: Specifications of electrolytic capacitor used in G4 capsule [87].

Capacitance	68 µF
Rated voltage	25 V
Max leakage current	17 µA
$\tan\delta$	0.14
Ripple current, at 100 kHz, 105 °C	450 mA (r.m.s)
Dimensions: ϕD×L	5×11 mm

reported. Jain and Rymaszewski [88] have proposed an equation based on the best obtained fit of experimentally reported results:

$$E_{bd} = 20/k^{(1/2)} \tag{3.6}$$

where E_{bd} is expressed in MV/cm. McPherson et al. [89] reported a similar E_{bd} vs. k relation, based on a thermochemical model:

$$E_{bd} = 35/k^{(0.64)} \tag{3.7}$$

The reduction of the breakdown field strength in high-k dielectrics was attributed to the increase of the local electric field between the dipole atoms E_{loc}, which is expressed as:

$$E_{loc} = [(2+k)/3]E \tag{3.8}$$

Where E – applied external electric field. The higher local field reduces the bond strength of polar molecules, causing breakage of bonds and formation of conductive paths in the dielectric layer. Both relations (eq. 3.6 and 3.7) are plotted for a range of k values in fig. 3.9, showing close agreement between the models, especially for k >20.

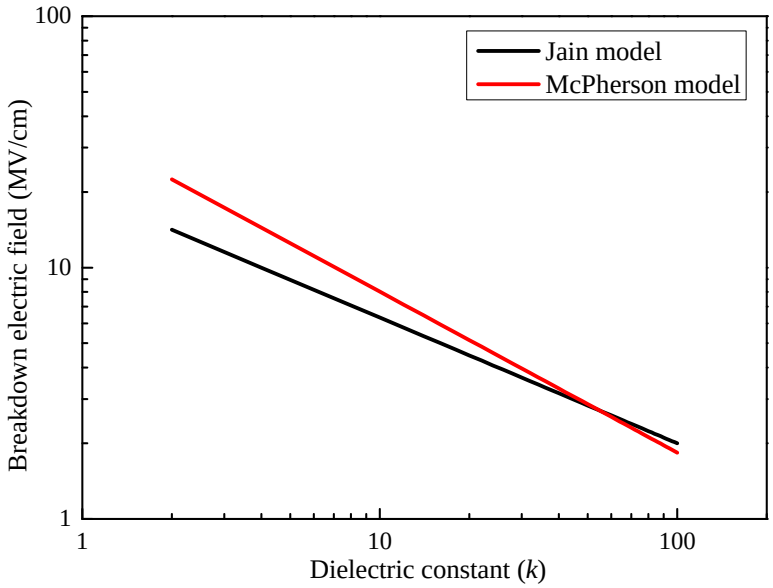


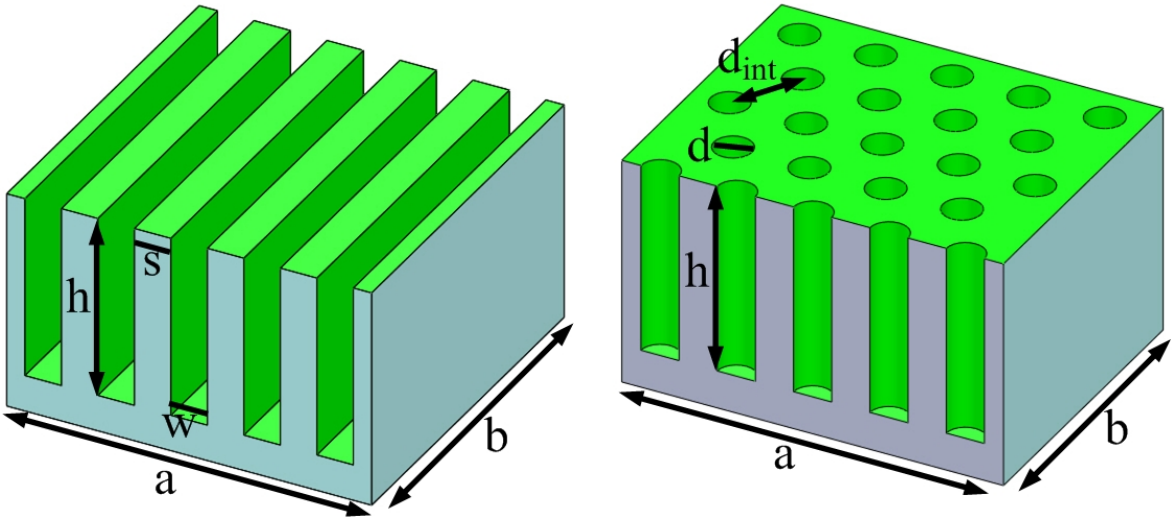
Figure 3.9: Models predicting the breakdown strength of dielectric materials as a function of k [88, 89] on a log-log scale.

Using equations 3.1 and 3.6, breakdown voltage (V_{bd}) can be expressed in terms of k and dielectric layer thickness (t):

$$V_{bd} = \frac{1.77k^{1/2}}{C'} \tag{3.9}$$

$$V_{bd} = \frac{59.5t^{1/2}}{C'^{1/2}} \tag{3.10}$$

where V is in volts, C' – µF/cm^2 and t – µm. The required capacitance density to integrate 68 µF into 800.28 mm^2 area is 8.5 µF/cm^2. From the above equations it can be derived that such a large capacitance density combined with 25 V breakdown would require a 1.5 µm thick dielectric layer with $k = 14413.5$. To achieve the required capacitance density with more conventional binary dielectric materials, the effective capacitor area needs to be increased. Etching the substrate to form arrays of high aspect ratio features would result in substantial increases of effective area, while the planar area remains unchanged thereby lowering the needed C'. Two commonly used trench designs are shown in fig. 3.10.



(a) Trenched structure (b) Porous structure

Figure 3.10: Schematics of surfaces with high AR structures: (a) trenched, (b) porous. The effective area is highlighted in green.

The total capacitance of a design with an array of parallel trenches (fig. 3.10(a)) can be calculated using the equation:

$$C = C'A\left(1 + 2\frac{h}{w+s}\right) \tag{3.11}$$

It is evident that the capacitance is expressed as the planar value × area multiplier. The multiplier is $1 + 2(h/(w+s))$, where h – depth of trench, w – trench width and s – distance between trenches. The number of trenches, needed to fill the predefined area A, is $n = a/(w+s)$. The structure in fig. 3.10(b) is made up of arrays of macro-pores, in a hexagonal arrangement. According to the theory of circle packing, that describes the arrangement of non-overlapping circles on a given surface [90], the highest density of equally sized circles is achieved using the hexagonal arrangement. Therefore the hexagonal layout would result in the highest increase

in effective surface area. To determine the area increase it is necessary to calculate the number of the equally spaced pores. The method to calculate the pores is as follows:

1. Knowing the interpore distance (pitch) d_{int}, tangent circles are drawn from the center of each pore, with diameter equal to $D = d_{int}$, as shown in fig. 3.11.

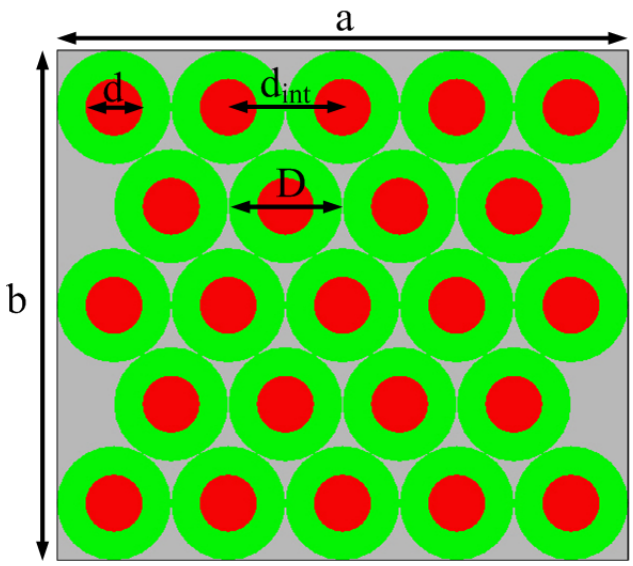


Figure 3.11: Hexagon pore layout. Red circles are the pores, green – tangent circles with $D = d_{int}$.

2. The number of circles in the first and any subsequent odd row is $m_o = a/D$, while every even row contains one circle less.
3. The total number of rows, n, is determined from the relation:

$$b \geq d_{int}\left(1 + (n-1)\frac{\sqrt{3}}{2}\right) \tag{3.12}$$

   by finding the largest integer n, for which the inequation still holds.
4. If n is an even number, the total number of pores, m_{tot}, is:

$$m_{tot} = \frac{n}{2}(2m_o - 1) \tag{3.13}$$

   and, if n is odd:

$$m_{tot} = \frac{n+1}{2}m_o + \frac{n-1}{2}(m_o - 1) \tag{3.14}$$

5. After the total number of pores is calculated, the pore density can be defined as $\phi = m_{tot}/A$.
6. The total capacitance of the porous capacitor can now be expressed similarly to the trench capacitor, in terms of planar area × multiplier:

$$C = C'A(1 + \phi h(\pi d)) \tag{3.15}$$

   where d is the pore diameter, h – pore height.

To compare the gain in area between the two 3D capacitor designs, the area multipliers

are plotted in fig. 3.12 as functions of aspect ration (h/w or h/d), with $d = w = s$ and $d_{int} = w + s$. The increases in area are similar, while the porous design has the advantage of being more mechanically robust. The dielectric constant and layer thickness, required to obtain 68 µF, are plotted as a function of the area multiplier in fig. 3.13.

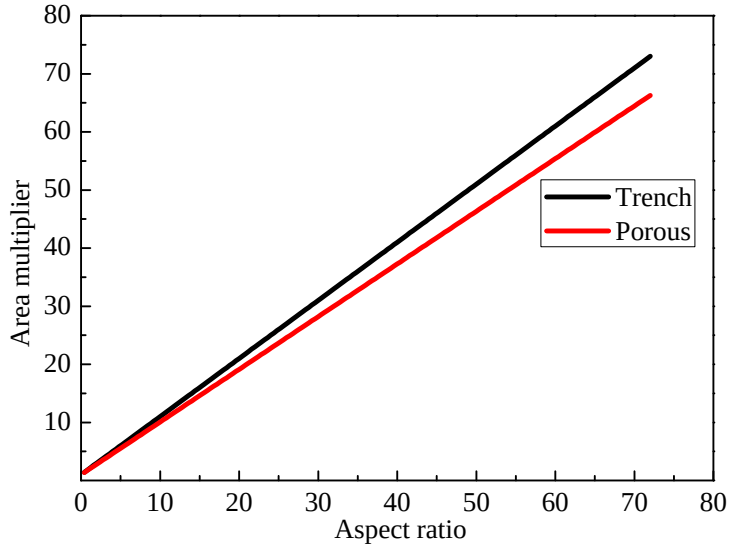


Figure 3.12: Comparison of area gain from increasing the structure AR for porous and trench designs.

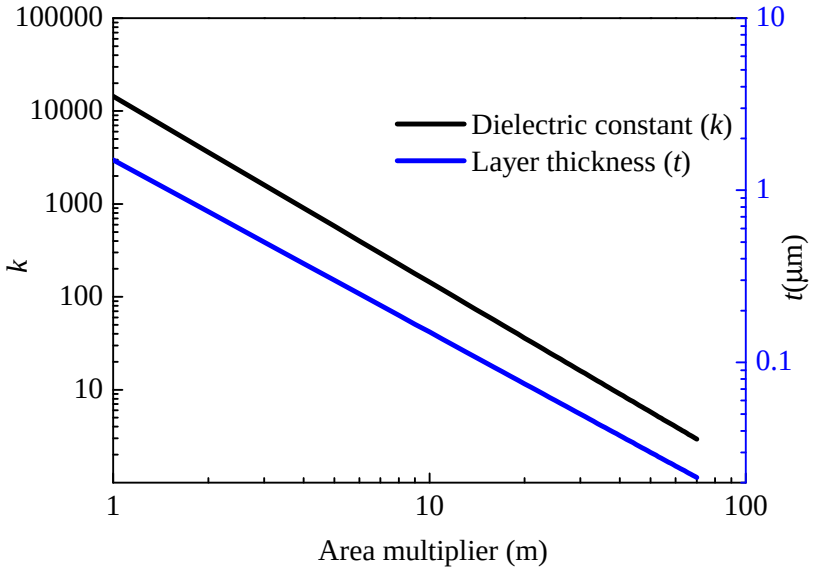


Figure 3.13: Dielectric constant and layer thickness (right axis) required to integrate 68 µF as functions of area multiplier.

The typical k values of highly investigated binary metal oxides are in a range of 3∼100, which corresponds to the area multiplier range of 70∼12. There are certain fabrication constrains regarding high area multiplier values that need to be taken into account. Etching of high aspect ratio (h/w) trenches with minimized pitch ($w + s$) is limited by the capabilities of the DRIE process. Reducing the spacing between structures can result in sidewall collapse due to characteristic scalloping and undercutting of the masking layer during DRIE. Aspect ratio dependent etching (ARDE) is also a well know property of the Bosch process. ARDE is caused

by the reduction of etching species at the bottom of the structure with increasing AR, due to collisions with trench sidewalls. The effectiveness of removing the polymer passivation also decreases causing narrowing of the etched structure until the sidewalls completely coincide. Aspect ratios up to 30 are achievable with standard Bosch process [91] by properly configuring the etch recipes. Etching tests for high AR trenches were carried out using an existing recipe, designed for etching with low sidewall scalloping, in a Alcatel Adixen AMS100 reactor. The results are shown in fig. 3.14. The designed width of the trenches was 2.5 µm and the AR=37.

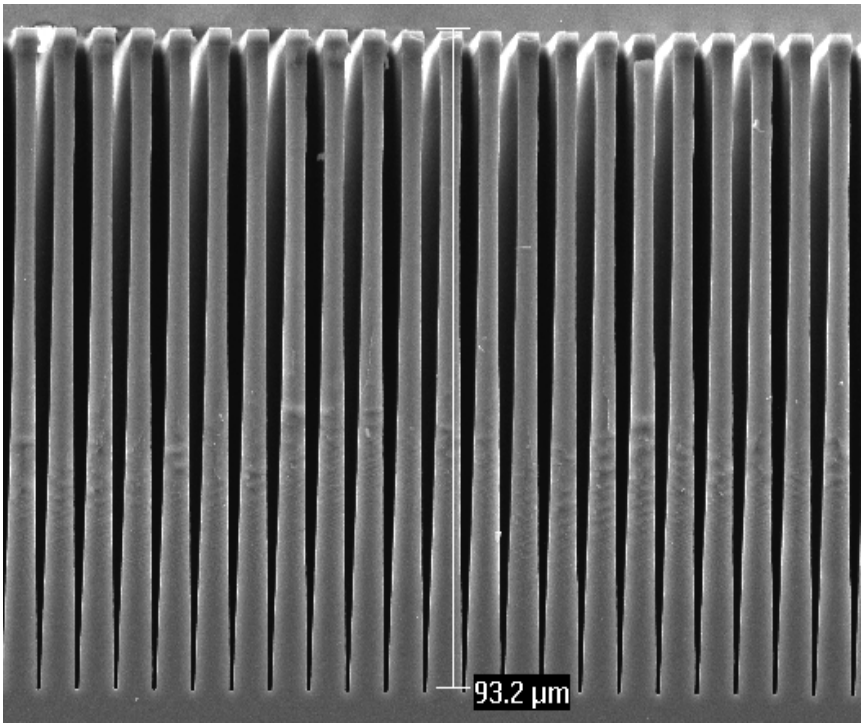
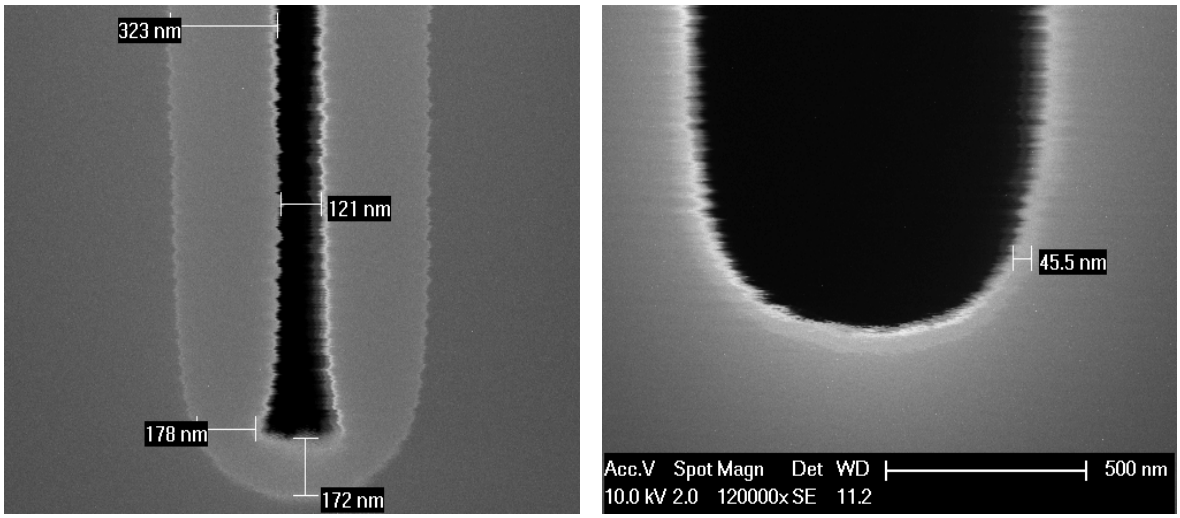


Figure 3.14: Effects of ARDE during high AR trench etching.



(a) Thermal oxidation (b) ALD Al_2O_3

Figure 3.15: Lining of high AR trenches with: (a) thermal SiO_2, (b) ALD Al_2O_3. In (b) the image is distorted due to high magnification but the contrast difference is still visible.

No significant undercutting under the masking layer was observed. The effects of ARDE are noticeable after reaching the AR of 20. At the bottom of the trench, width reduced by 75 % to 620 nm. After etching, the trenches were lined with thermal SiO_2 or ALD AL_2O_3 to determine whether conformal dielectric layers can be deposited in such structures as shown in fig. 3.15. In both cases conformal coatings were obtained. The ALD layer thickness was difficult to measure due to limited magnification of the scanning electron microscope, but the contrast difference is visible, indicating a continuous layer.

The possible design space to integrate a high value capacitor with required breakdown voltage, using the 3D trench approach, can now be summarized in terms of practically obtainable area multiplier, required layer thickness and the resulting breakdown electric field for a range of dielectric materials (fig. 3.16). The proposed design space calculations were

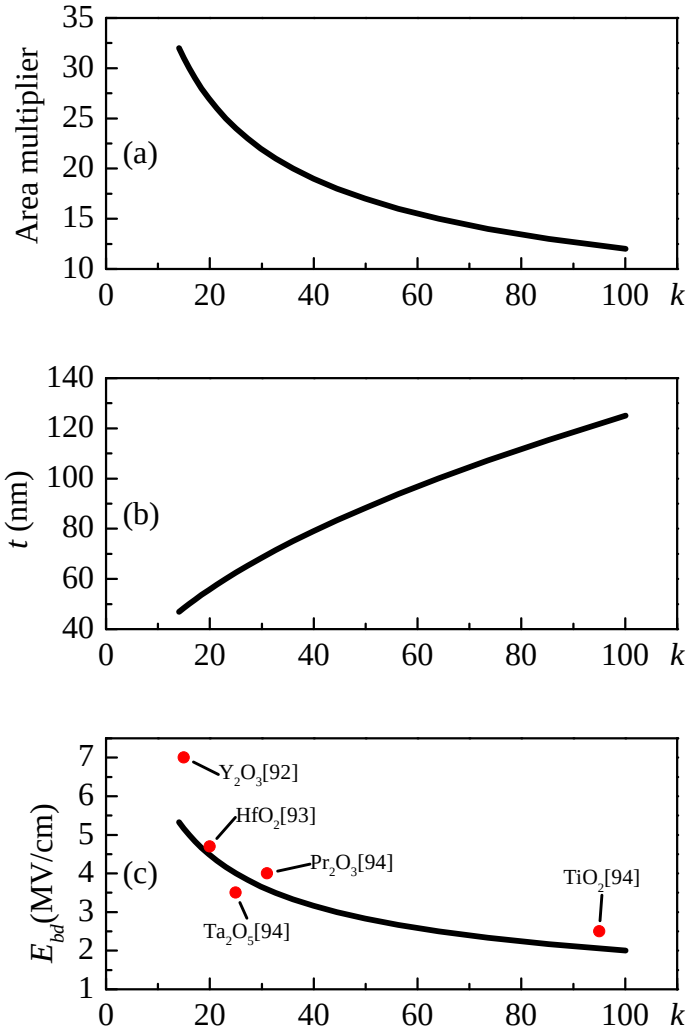


Figure 3.16: Design space requirements to integrate a 68 µF, 25 V 3D capacitor in terms of (a) effective area, (b) layer thickness, (c) breakdown strength. Experimental results reported in [92, 93, 94] are added to (c) indicating the validity of the $E_{bd} \sim k^{(-1/2)}$ model.

done for a MIM structure with a single dielectric layer. An alternative design approach is to stack multiple layers to form MIMIM with a common middle plate (as in shown fig. 3.3) or even MIMIMIM [83] structures. Layer stacking introduces more fabrication complexity, but

enables the application of lower k, but more stable and highly researched materials such as Al_2O_3 or Si_3N_4. Other design flexibility options of stacked layers could be the reduction of planar area, reduction of trench aspect ratio or increase of breakdown voltage to have higher reliability margins.

HfO_2 and Ta_2O_5 are promising candidate materials for a single layer 3D MIM capacitor, whereas Al_2O_3 is well suited for a two layer design. The porous layout results in a comparable area multiplier to the parallel trench design and increasing the pore diameter would allow to surpass it without compromising the structural integrity of the component.

3.6 Chapter Summary

Because silicon is used as substrate material for the 3D WLP package, additional components can be readily integrated. To demonstrate component integration possibilities it was decided to add a MIM capacitor on the wafer backside. Therefore this chapter began with an overview of current advances in MIM capacitor integration. Design parameters and requirements were then presented and dielectric material options were reviewed. A process flow for MIM capacitor integration at the wafer backside was presented in detail. Finally, an investigation on the possibilities to integrate high capacitance density 3D capacitors for energy storage applications was carried out. A design space for a range of available dielectric materials was presented, taking into account the micro-fabrication constrains such as ARDE and ALD uniformity inside high AR structures.

Chapter 4

Package Fabrication and Assembly

4.1 Introduction

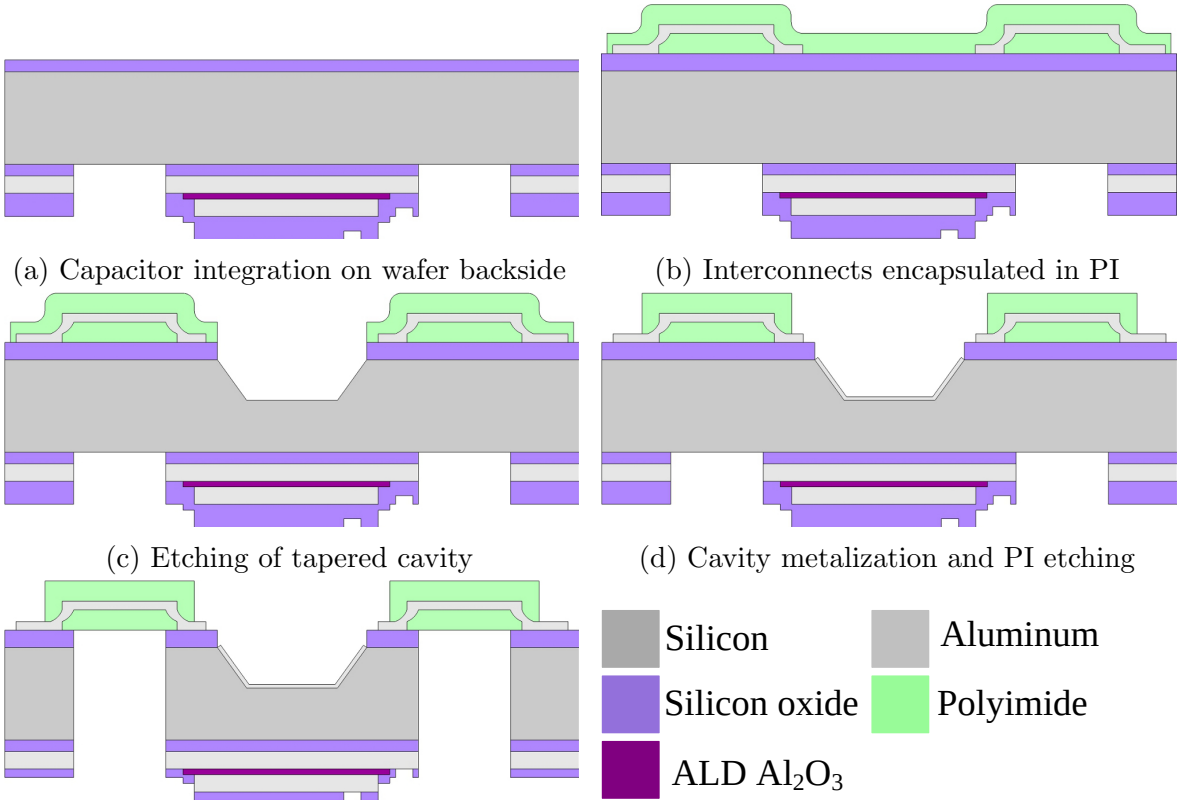
Design and fabrication of the two main structural elements of the proposed 3D SSL package were covered individually in chapters 2 and 3. This chapter will cover the entire fabrication sequence, in the order that it was performed. The integration of a LED reflector cavity will be discussed in detail. The post-fabrication package assembly, release from the substrate and folding into a 3D shape will also be presented.

4.2 Integrated Process Flow

The fabrication of the proposed 3D WLP package can be divided into 3 main parts:

- Backside capacitor integration (chapter 3).
- Flexible interconnect fabrication (chapter 2).
- Reflector cavity integration.

Processing started by growing 300 nm of thermal SiO_2 on both sides off DSP 4 inch p-type wafers. Next followed the capacitor fabrication on the backside. Fully patterned capacitors were then covered with a 6 µm of PECVD SiO_2, that acts as a protective layer during further processing and as a DRIE hard mask (fig. 4.1(a)). Then the front-side processing began by spin-coating the first layer of polyimide on 1.3 µm (300 nm thermal + 1 µm PECVD) of SiO_2, followed by hardbaking and patterning. Aluminum layer of 2 µm thickness was then sputtered, lithographically patterned and wet etched in PES, using positive photoresist as a mask. The formed interconnects were then encapsulated in a second layer of PI, as shown in fig. 4.1(b). At this stage, the reflector cavities need to be etched. A 6 µm layer of PECVD SiO_2, deposited at 350 °C, was used as a masking layer for this process. To pattern the oxide mask in the fluorine based etcher, 3 µm of photoresist were required. The patterned oxide acts as a mask to etch PI, the underlying 1.3 µm oxide layer and silicon. A DRIE etcher was used for the tapered cavity etching, with continuous SF_6 gas flow without multiplexing with C_4F_8, unlike in the standard Bosch process. After etching for 32 min 200 µm deep cavities were formed. The remaining oxide mask was removed using BHF, with the backside of the wafer protected by 3 µm of photoresist. The resulting structure is shown in fig. 4.1(c). Typically tapered cavities are formed using wet chemical etching (KOH, TMAH), however these chemistries



(a) Capacitor integration on wafer backside

(b) Interconnects encapsulated in PI

(c) Etching of tapered cavity

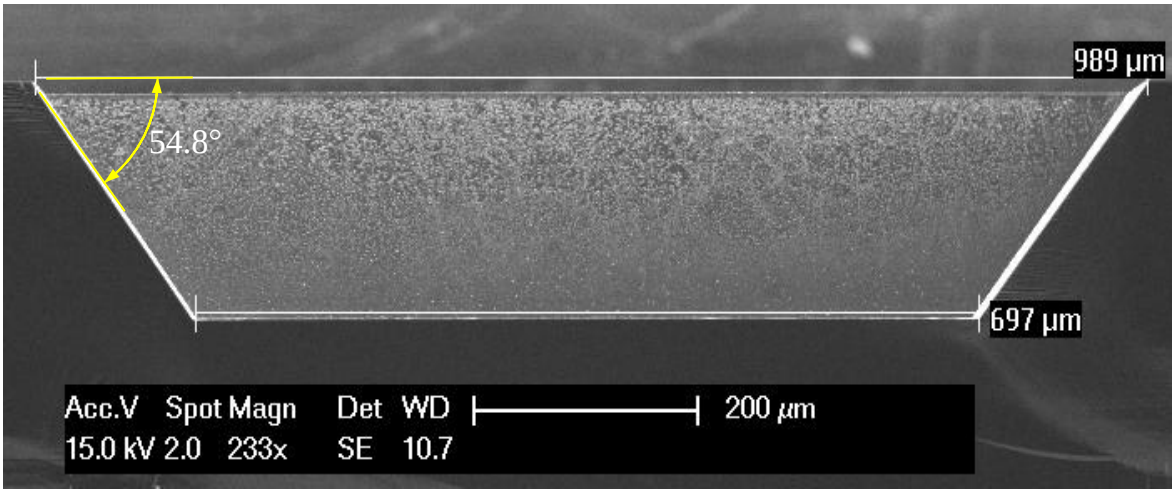
(d) Cavity metalization and PI etching

(e) Cavity metalization and PI etching

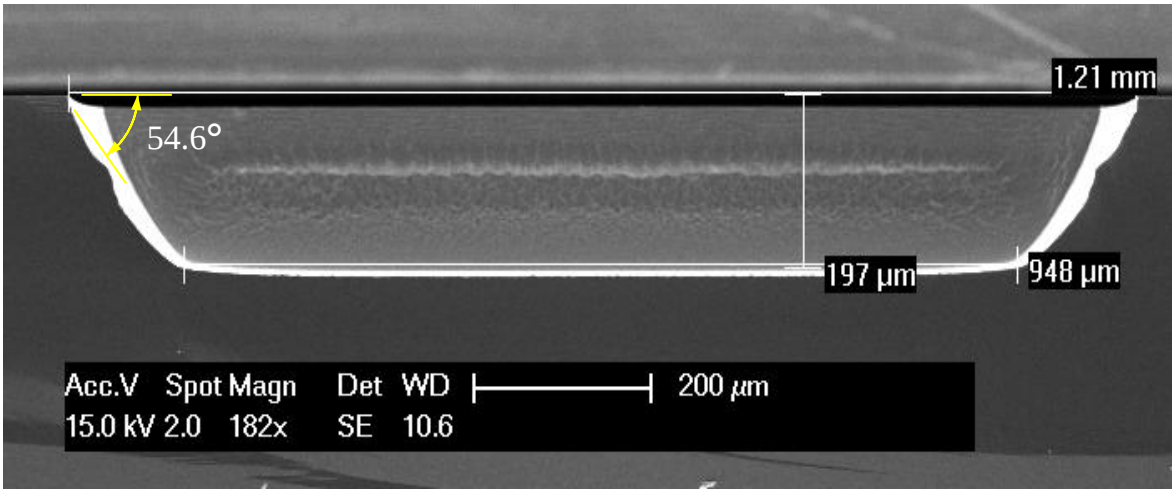
Figure 4.1: Processing flow of 3D WLP package.

also etch aluminum and organic layers like PI. Consequently, the integration of wet etching into the proposed fabrication flow would require pinhole free, conformal protective layers on both sides of the wafer as well as an additional lithography step, in order to cover the edges of the layer stack, which are exposed during etching to reach the Si. A comparison between wet etched and DRIE tapered cavities was made. Two test wafers were patterned with the reflector cavity mask (openings of 0.98 mm×0.98 mm). One wafer was etched in 33% KOH at 85 °C and the other – using the DRIE etcher. Cross-sections of the resultant cavities are shown in fig. 4.2. The KOH cavities have a smooth surface and form an inverted trapezoid, whereas plasma etched cavities have rounded edges and the sidewalls are rough. The taper angle in both cases is almost identical. A rough surface can act as a diffusive reflector and scatter light out of the cavity more efficiently [3]. Due to undercutting of the masking layer the DRIE cavity expanded by more than 230 nm, while the KOH cavity retained the patterned dimensions.

The cavities then had to be lined with a reflective coating layer to enhance light extraction. Aluminum was chosen as the reflector coating because of its high reflectivity (95% [13]) and compatibility with the process flow. 250 nm of Al were sputtered and patterned with the cavity mask using spray-coated negative resist to cover the Al inside the cavities. After development the wafers were spray-coated with positive resist and patterned again with the PI mask. This mask was etched in the chlorine based RIE etcher and a hard mask pattern to etch the PI was formed while the cavities remained metalized. After anisotropic PI etching, the metal interconnects were exposed, the cavities remained metalized, however the Al masking



(a) Cross-section of KOH etched cavity



(b) Cross-section of DRIE etched cavity

Figure 4.2: Comparison of reflector cavities: (a) KOH etched, (b) DRIE etched.

layer still remained. This layer could just be removed by a short dip in PES, but since the cavity metalization has the same thickness, it needs to be covered. To selectively remove the masking layer, the PI mask pattern was inverted using negative resist. After development, resist remained everywhere except for on the PI pattern and hence could be removed in PES. The resist was then stripped using NMP. Chemical removal of negative resist does cause challenges, as some resist flakes remained after 20 min in NMP with continuous stirring at 70 °C and needed to be cleaned with soft cotton tips. The formed structure is shown in fig. 4.1(d). After resist removal the front-side processing was completed.

The last step in the package fabrication was through wafer etching from the backside. The newly purchased SPTS Omega Rapier i2L DRIE system was used. Due to the formed PI structures, the wafer front-side was no longer flat. This topography caused increased helium leakage inside the chamber of the etcher and the process would not start. He is used as a cooling interface for the wafers and the pressure is monitored. If the pressure is lower than the preset value the flow is increased up to the maximum allowed level. Therefore it was necessary to reduce the required He pressure to start the etching process of the wafers. Lowering the pressure could cause cooling inadequacy, however no overheating or masking

layer deterioration was observed. Only 3 µm of SiO_2 were consumed by the etching process, yielding a superior selectivity of 268 for the new DRIE system. The remaining SiO_2 layer was etched to expose the capacitor contacts and the finalized structure is shown in fig. 4.1(e). Five photolithography masks were required to fabricate the WLP. Some of the masks were used more than once during processing. A summarized flow chart of the entire fabrication process is given in fig. 4.3 and a completed wafer with 4 structures is shown in fig. 4.4.

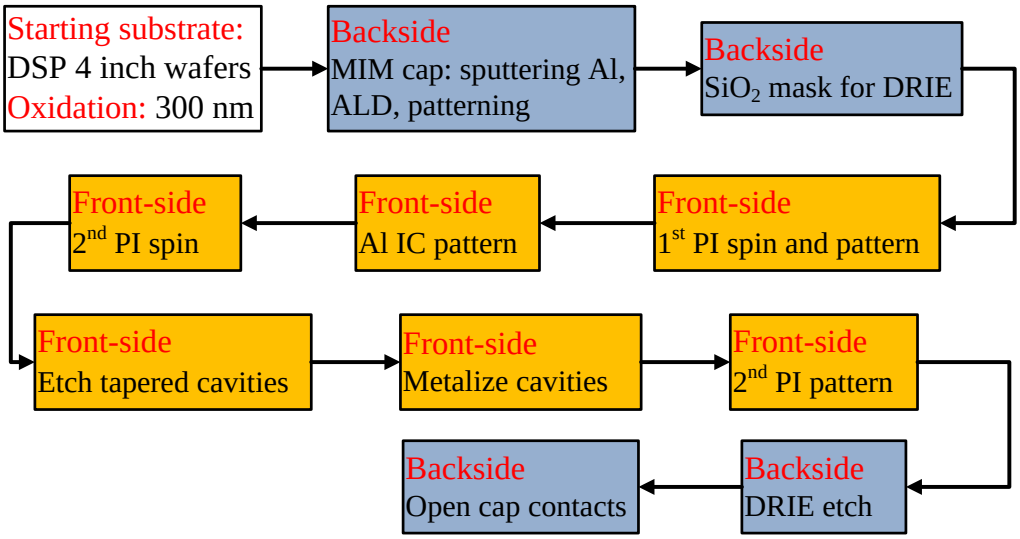


Figure 4.3: Schematic diagram of the 3D WLP fabrication flow.

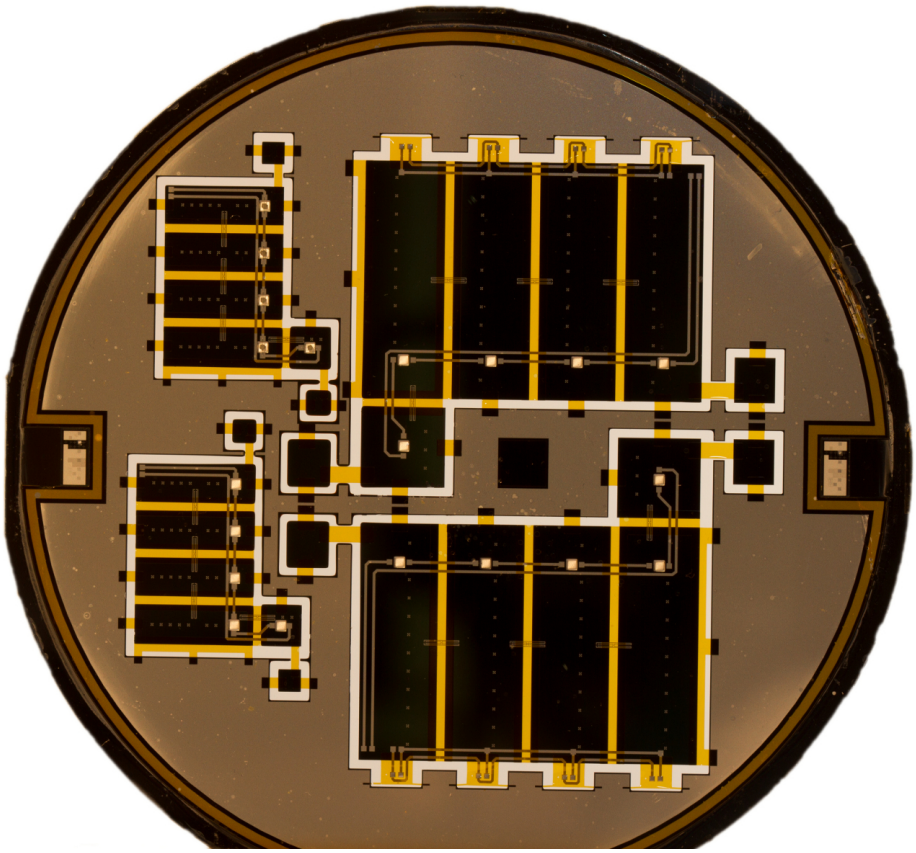


Figure 4.4: Fully fabricated packages on Si wafer.

4.3 Post-Fabrication Assembly

After package fabrication, LEDs need to be placed in the cavities and connected by wire bonding. Phosphor was used to convert the color of light, packages were then released from the wafer and folded around an assembly structure.

LED Mounting

Blue LED chips from Cree were used as light sources. The specifications of these chips are summarized in table 4.1. The LEDs were placed inside the cavities by pick-and-place and

Table 4.1: Specifications of the LEDs used in this work [95].

Part number	TR5050
Forward voltage (V_f)	3 V
Forward current (I_f)	120 mA
Material	InGaN on SiC
Dimensions (L × W × H)	500 × 500 × 175 µm
Color	Blue (450 nm)
Max. junction temp.	150 °C
Bond pad metal	Gold (Au)

attached using silver paste, because of its superior thermal conductivity. Wire bonding with Al wires (d = 32 µm) was utilized to connect 5 chips in series to the Al bond pads of the package. The connections were tested by applying current with probe needles, as shown in fig. 4.5.

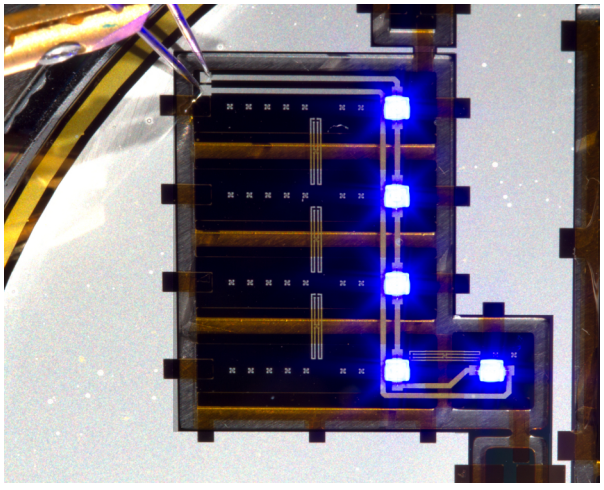
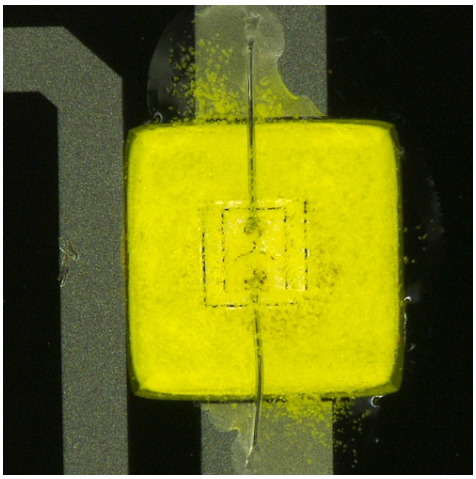


Figure 4.5: Current supplied to wire bonded LEDs.

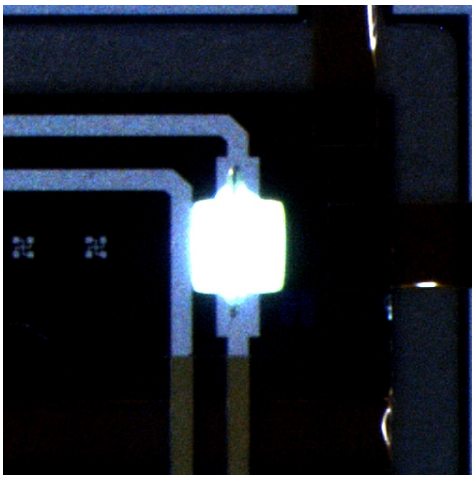
Phosphor Based Color Conversion

A mixture of yellow phosphor and silicone was prepared to demonstrate light conversion on the wafer level. The silicone used was a two-part OE-6650 Resin from Dow Corning, mixed with a A:B=1:3 ratio. Yellow phosphor, Philips YAG U822 d50 (particle size 10 µm), was added to silicone with ratio 15:85 and mixed using a speedmixer to break up the phosphor particle clusters. The substance was dispensed inside the reflector cavities using glob-top method with

multiple dispense cycles and visual inspection of color change after every cycle. The cavities allow to confine the mixture to the proximity of the chip and prevent overflow. The silicone was curred on a hotplate for 30 min at 150 °C. The LED cavity, filled with phosphor is shown in fig. 4.6(a) and color of light after conversion in fig. 4.6(b). Measured optical parameters are discussed in chapter 5.



(a) LED cavity filled with phosphor



(b) Light color after conversion

Figure 4.6: LED cavity filled with phosphor mixture (a). Light color (b).

Release from Substrate and Folding

After LED mounting and color conversion, the packages were released from the wafer and folded into a 3D geometry. The wafers were placed under a microscope with a long free working distance and individual packages were separated from the wafer by cutting all the PI tabs out of the wafer with a sharp, fine blade. The released flexible package is shown in fig. 4.7.

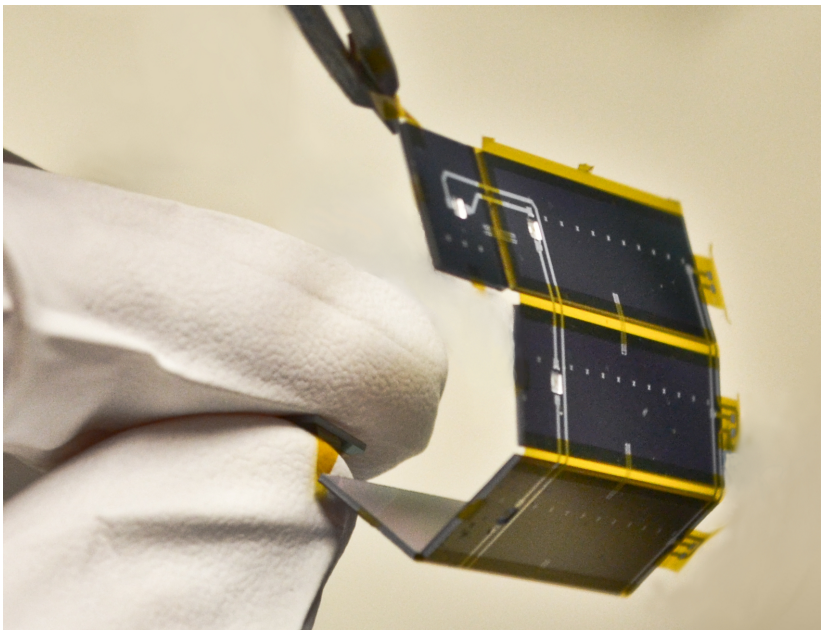
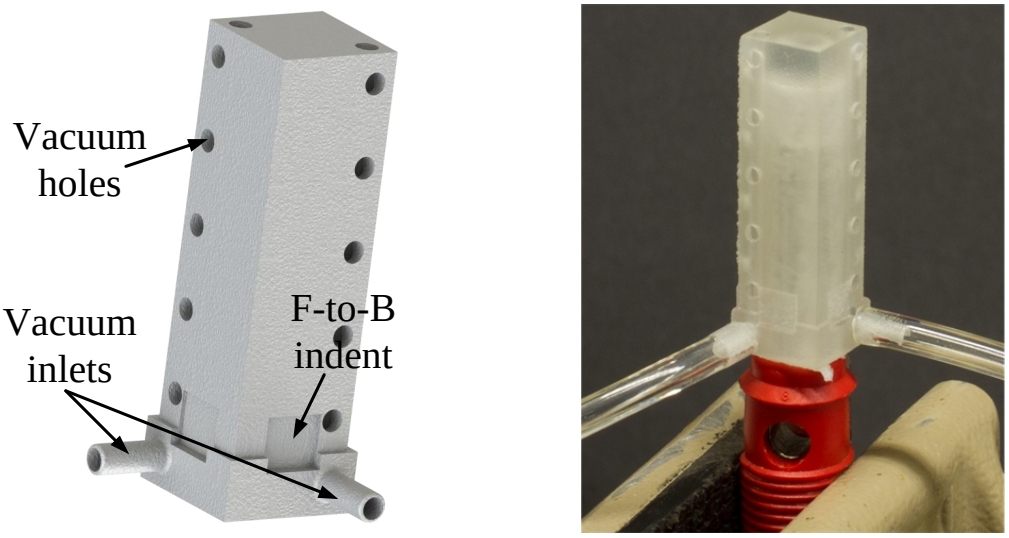


Figure 4.7: Flexible package released from wafer.

An assembly structure was designed for folding the packages into a cuboid. Solidworks 2013 3D CAD software was used to design the block shown in fig. 4.8(a). The dimensions of

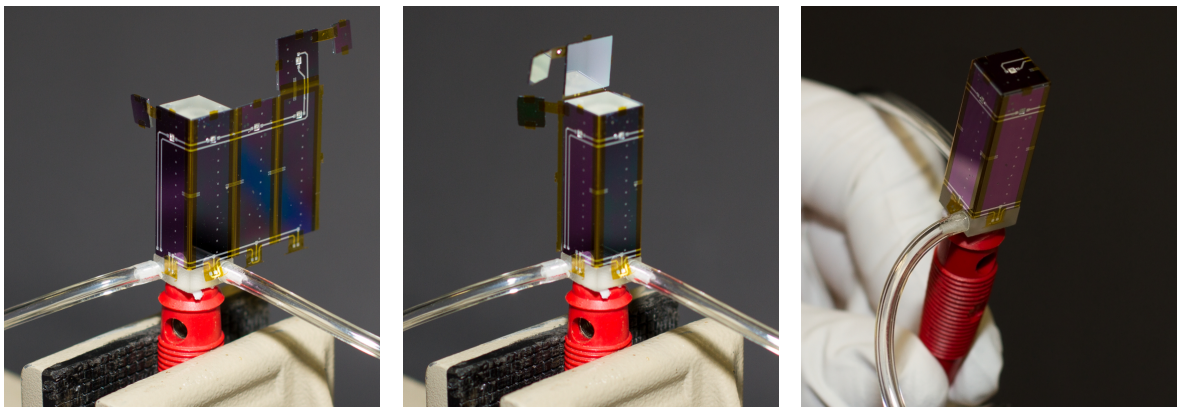


(a) 3D rendering of the folding structure. (b) Plastic 3D printed folding structure.

Figure 4.8: Package folding structure: 3D rendering (a), fabricated by 3D printing (b).

the sidewalls were made equal to the larger version of the package. Two vacuum inlets were added to the slightly wider base part of the structure. Every sidewall had 5 vacuum holes (2 on the top), to assist with package folding while the extruded edges at the base helped with alignment before folding. Indentations were added at positions were the folded front-to-back structure would be. The assembly structure was fabricated by 3D printing, from PA 2200 plastic and is shown in fig. 4.8(b). The fabricated structure also had a round cavity at the bottom, that was used to clamp the block during assembly.

Package folding started with securing the block in a vice to prevent it from moving. Suction was applied through the vacuum inlets. The package was brought in contact starting with the left-most sidewall and edges were aligned. When the first two sidewalls were attached, the vacuum clamping was strong enough to hold the structure without support, as demonstrated in fig. 4.9(a). The remaining sidewalls were then easy to fold without misalignment fig. 4.9(b).



(a) Half-folded package. (b) Sidewalls folded. (c) Fully folded, handling tiles removed.

Figure 4.9: Flexible package folding procedure.

The wrapping was finalized by folding the top and peeling off the handling tiles fig. 4.9(c). The interconnect integrity was tested by applying power to the package fig. 4.10.

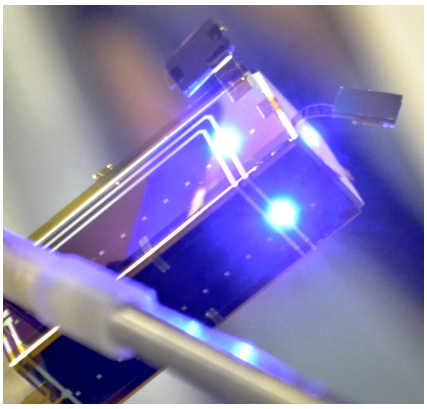


Figure 4.10: Power applied to folded package.

Front-to-Back Interconnection

The novel method for connecting the front-side of the chip to the back was used as possible alternative for TSVs (refer to page 24). After the chips were released from the wafer the polyimide encapsulated Al lines were freely overhanging at the bottom edges (fig. 4.11). These

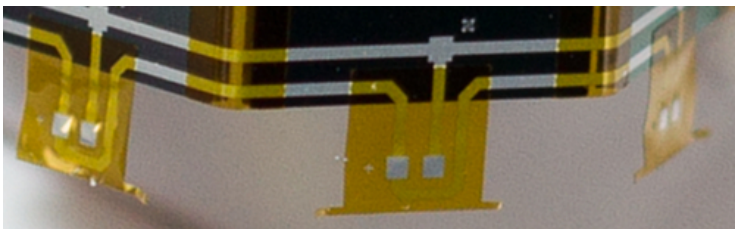


Figure 4.11: Front-to-back structures after chip release.

flaps did not curl or bend downwards as the bending stiffness was high enough to keep the structures coplanar to the chip surface.

The chips were placed face down and structures were bent over to the backside using fine tip tweezers. Quick drying, two-part epoxy was used to glue the structures to the chip at room temperature. The initial proposed method of interconnecting the bond pads by wire bonding (ref. to page 25) was not successful due to the soft underlying PI and glue layers. The wire boding station tip would only make indentations to the Al pad surface without forming a bond. An alternative method, using conductive silver paste, was employed by syringe dispensing of conductive paths between the pads, as shown in fig. 4.12. The conductive paste was curred

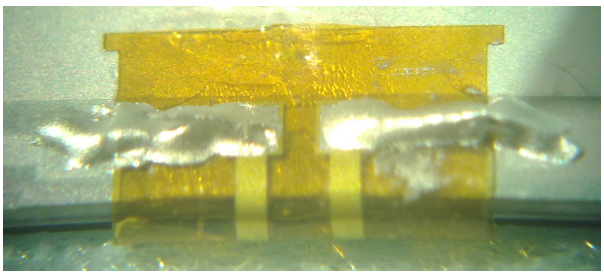


Figure 4.12: Glued and connected flexible front-to-back structure.

in an oven at 125 °C for 2 h. Solder paste could be used as alternative conductive material. Interconnect continuity was validated by $I - V$ measurements, demonstrating linear (ohmic) relationship (fig. 4.13).

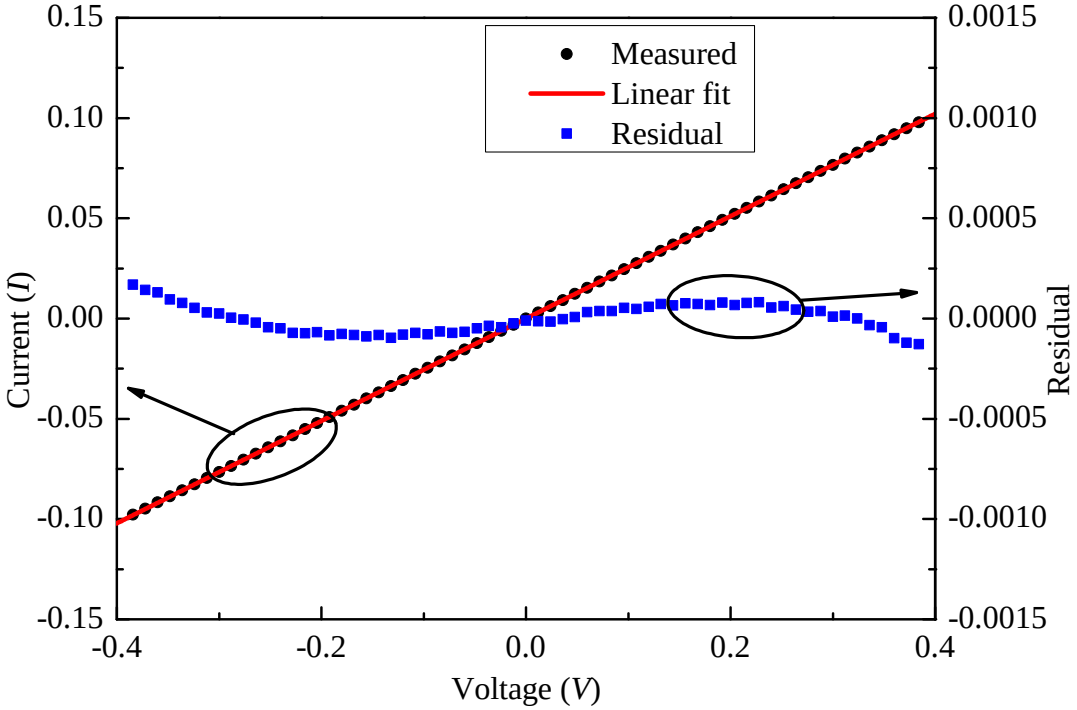


Figure 4.13: Continuity validation of the flexible front-to-back interconnection structure by $I - V$ sweep. Linear fitting with correlation coefficient=1 was obtained.

4.4 Chapter Summary

In this chapter the flexible 3D wafer level package fabrication and assembly was covered. The processing sequence was presented in the order as it was carried out with detailed description of the steps necessary to integrate the reflector cavities. Because tapered cavities were obtained by plasma etching rather then by conventional wet KOH etching, cross sectional comparison of obtained structures was performed. The remainder of this chapter focused on the post-fabrication assembly of the 3D WLP. It started with mounting and wire bonding of blue LED chips inside the cavities. Afterwards phosphor based color conversion was demonstrated on wafer level. Packages were then released from the substrate by cutting the PI tabs with a fine blade. The released structures were folded around a 3D printed assembly structure. Vacuum was used to clamp the folded package during assembly. Lastly, the novel structure to connect devices on the backside of the wafer to the front-side was demonstrated. The interconnect was folded over the edge of the chip, glued by a non-conductive epoxy and interconnected to the backside by dispensing silver paste to form conductive tracks. The connection continuity was validated by voltage sweeps, showing linear $I - V$ characteristics.

Chapter 5

Packaging Characterization

5.1 Introduction

This chapter will cover the post-processing characterization of the fabricated flexible package ant its components. Cyclic mechanical bending that was conducted to determine the durability and electrical performance of the flexible, neutral bending plane based interconnects will be presented. Then the investigation of embedded capacitors will follow with respect to electrical characterization of dielectric layer properties, as well as component yield challenges that arose. The thermal performance of the package, tested by thermographic imaging, will also be presented. Finally, optical measurements will be summarized and discussed.

5.2 Interconnect Bending Tests

Mechanical bending tests were performed to investigate how flexible interconnects can withstand cyclic bending during package fabrication and assembly. Previously reported results demonstrated the possibility to bend Al interconnects, embedded in polyimide, to a radius of 300 µm without any changes in resistance [96]. The influence of multiple bending cycles on interconnect degradation was not mentioned, however.

A custom test setup was constructed to perform automated bending tests. An Al bending block was designed in Solidworks CAD and fabricated by precision milling. The 3D image of the bending structure is shown in fig. 5.1. One edge of the structure had slopes with 5

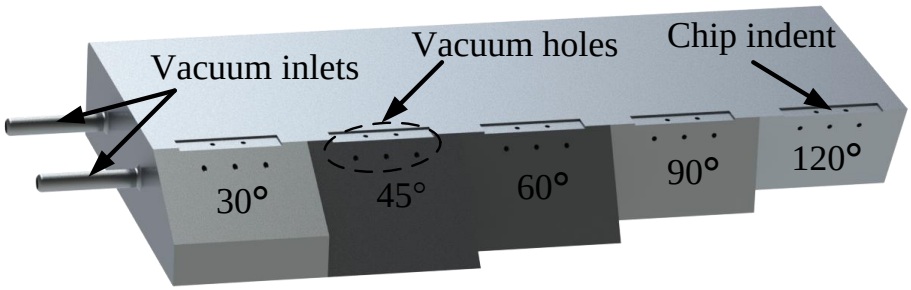
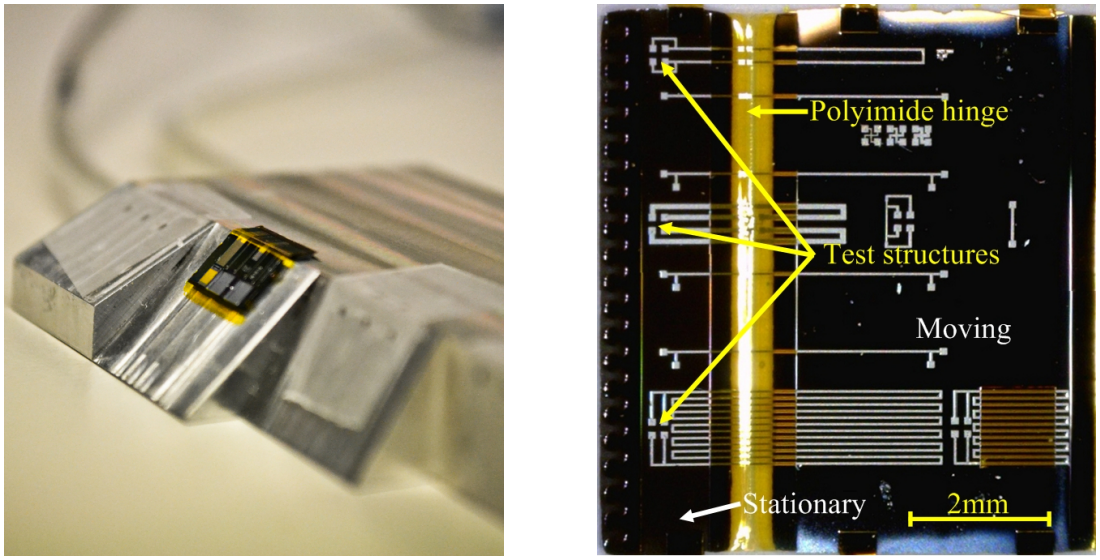


Figure 5.1: 3D rendering of the bending test structure, with indicated bend angles.

different angles. Chips were placed on these slopes and aligned to the shallow indentation.

Two separate vacuum inlets were added to the block. One was used to clamp the horizontal stationary part of the chip where the probe needles would be placed and the other – to hold the bent part in place during measurement. A directed nitrogen stream was used to apply bending without physical contact. A test chip mounted on the bending block and clamped with vacuum is shown in fig. 5.2(a) and top view, showing details of the chip, in fig. 5.2(b). It is



(a) Test chip on bending block.

(b) Test chip for bending tests.

Figure 5.2: Test chip mounted on bending block (a). Detailed view of the test chip (b).

separated into two parts by a flexible hinge, with the narrower part used for probing, whereas the wider part would be periodically bent and released. Four-point resistance measurements (described on page 25) were conducted on the test structures that connected the two segments and thus went through the flexible hinge and the bending axis. The complete testing setup used is demonstrated in fig. 5.3. It consisted of the bending block, adjustable nitrogen nozzle

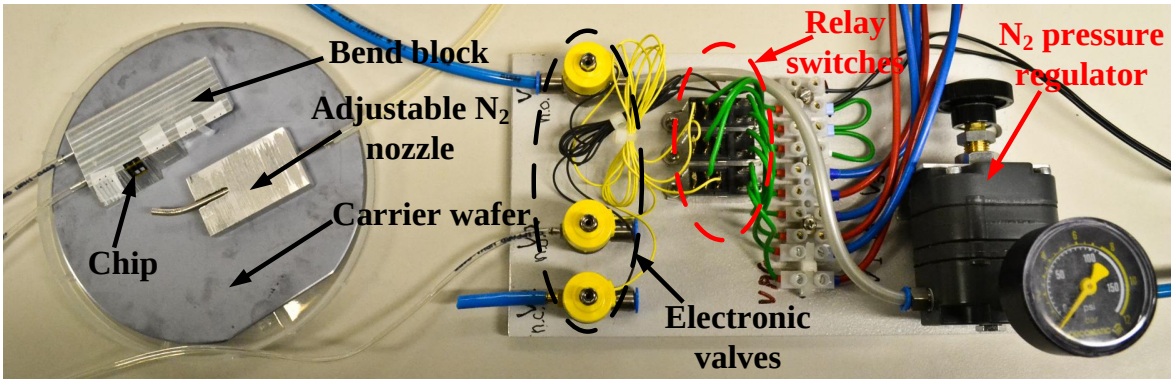


Figure 5.3: Bending test sequence.

and control board for the vacuum and N_2 switching. The block and nozzle were taped to a 6 inch unpolished carrier wafer that was used to securely clamp the blocks on the chuck of the probe station. The blocks were then moved into the measurement chamber and the chips were probed. The control board consisted of electronic valves that were regulated by switching relays. These relays were controlled directly by the source monitor unit. A pressure regulator

was used to adjust the N_2 flow necessary to bend the chip. A diagram of the measurement sequence is shown fig. 5.4.

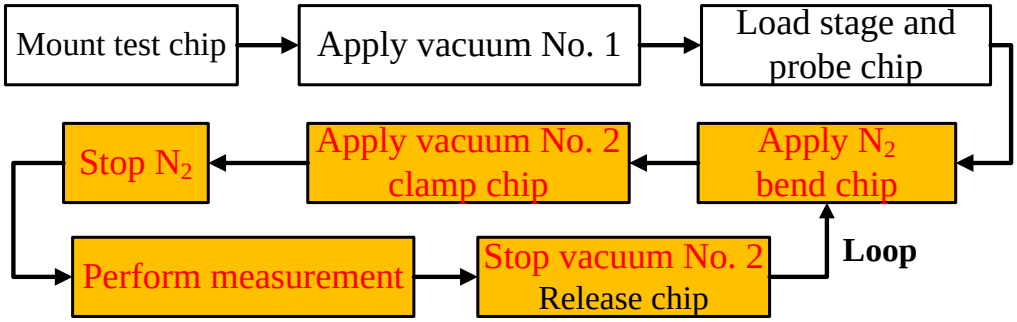
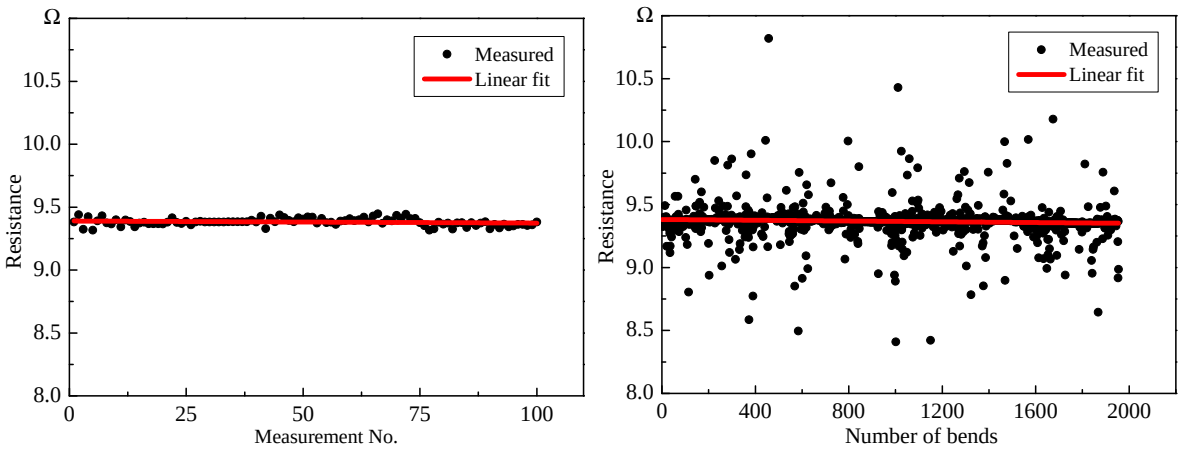


Figure 5.4: Measurement process of the bending test.

Current sweeps in the range of −10 mA to 10 mA, with 2 mA increments were performed and voltage drop was measured. The resistance value was extracted from the slope of the linear fitting of V-I plots. The most accurate measurements were obtained using the longest winding structure (bottom of test chip), due of the higher voltage drop across it. Only results with correlation coefficients (CC)>0.98 were accepted. The testing started by measuring the resistance 100 times before bending. These measurements were used as initial reference and the results are shown in fig. 5.5(a). The average measured value was $R = 9.38\,\Omega$. The chip was



(a) Resistance measurements before bending. (b) Bending test results after 2000 cycles of 90 degree bends.

Figure 5.5: Flexible chip bending tests: pre-bending reference values (a), results after 2000 bending cycles of 90° (b).

then mounted on the test block and automated bending together with resistance measurement was conducted. No change in resistance value was observed after 2000 cycles of 90° bends, fig. 5.5(b). Due to a large number of measurements there was some scatter of measured values, making it difficult to estimate the changes in resistance. By performing linear regression of results, it was observed that the slope of the fit was almost 0, indicating that the resistance was not increasing. Therefore, it can be stated that there was no degradation in electrical performance of the flexible interconnect after 2000 bending cycles.

5.3 Embedded Capacitor Characterization

To investigate the properties of available ALD metal oxide layers, test capacitors were fabricated using the same processing steps as described in section 3.4. A lithography mask with an array of 1.8×1.8 mm squares was used to pattern the capacitor plates. The first investigated layer was Al_2O_3 deposited by thermal ALD, with layer thickness of approx. 95 nm. Additionally, 43 nm plasma enhanced (PE) ALD layers of Al_2O_3 and HfO_2 were investigated. PEALD was performed in an Oxford Instruments FlexAl reactor. Both processes were executed at 300 °C, using TMA as Al_2O_3 precursor and tetrakis(ethylmethylamino)hafnium (TEMAH) for HfO_2. *C-V* and *I-V* measurements were carried out using HP 4284A precision LCR meter and Agilent E5270B source/measurement unit respectively. The capacitance linearity characteristics are shown in fig. 5.6. The measured values were fitted with the capacitor

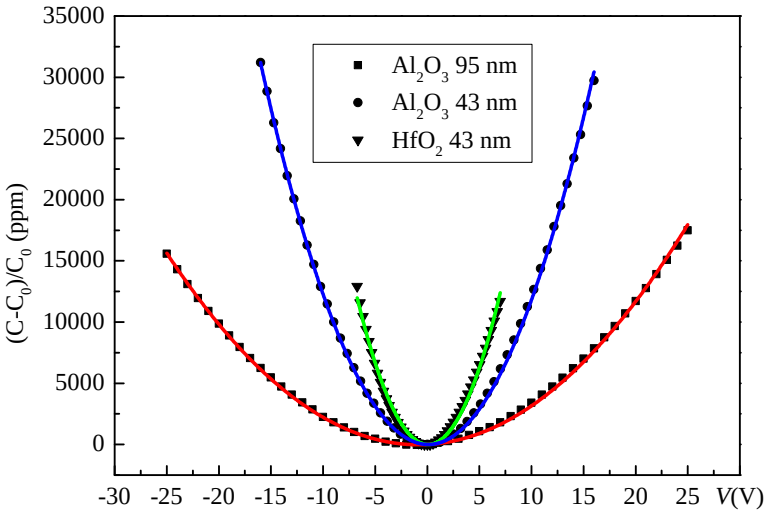


Figure 5.6: *C-V* of thermal and PEALD Al_2O_3 and HfO_2 MIM capacitors.

linearity equation 3.2 to extract the VCC coefficients. Dielectric breakdown strength of the fabricated passives was determined from *I-V*. The onset of dielectric breakdown occurs when there is a sudden increase in leakage current (up to SMU compliance value) at a small bias voltage increment, as shown in fig. 5.7, causing irreversible damage to the component. Characteristic parameters of the tested dielectrics are summarized in table 5.1.All the layers were as-deposited, without implementing any thermal annealing or passivation steps, that were reported to improve the dielectric properties [97]. Thermal Al_2O_3 layer had values most closely matching to reported in literature for both k and E_{bd}.

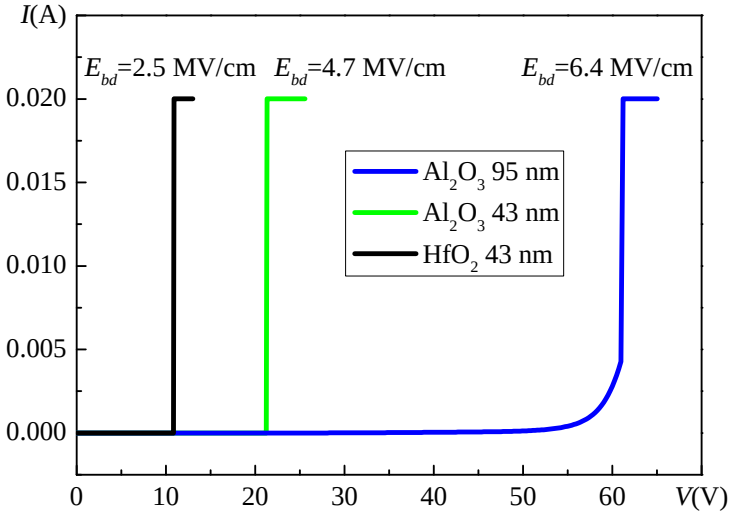


Figure 5.7: Dielectric breakdown of thermal and PE ALD Al_2O_3 and HfO_2 MIM capacitors.

Table 5.1: Measured capacitor parameters. Dielectric constant values were compared to reported in literature and E_{bd} – to predicted by the $E_{bd} \sim k^{(-1/2)}$ model [88].

	ALD Al_2O_3	**PEALD Al_2O_3**	**PEALD HfO_2**
α **(ppm/V^2)**	26.8	120.3	258.7
β **(ppm/V)**	46.5	-23.5	-42.2
k **meas.**	9.2	9.1	19.7
k **from [93, 98]**	8∼10	8∼10	20∼25
E_{bd} **meas. (MV/cm)**	6.4	4.7	2.5
E_{bd} **from eq. (3.6) (MV/cm)**	6.6	6.6	4.2

Thermal ALD Al_2O_3 was further characterized in terms of performance at elevated temperatures, as typical SSL components operate at temperatures above the ambient value. Capacitance was measured with increasing temperatures and the results are shown in fig. 5.8. The $TCC = 268\,\text{ppm/°C}$ was extracted from the slope of the linear regression fitting line.

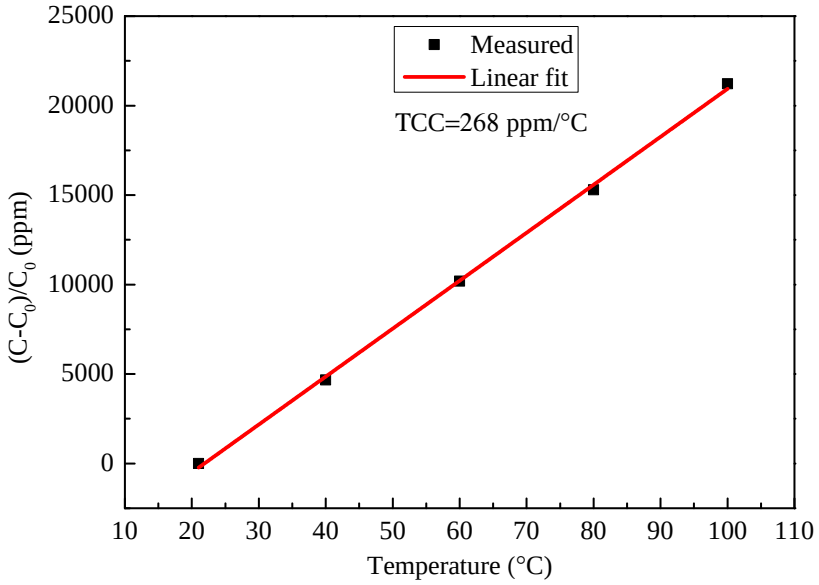


Figure 5.8: Temperature dependency of normalized capacitance. CC=0.99.

Breakdown characteristics with increasing temperature were also investigated. It was observed that breakdown field strength was stable up to 85 °C. At higher temperatures E_{bd} started to gradually deteriorate, as demonstrated in fig. 5.9. The decrease in breakdown electric field

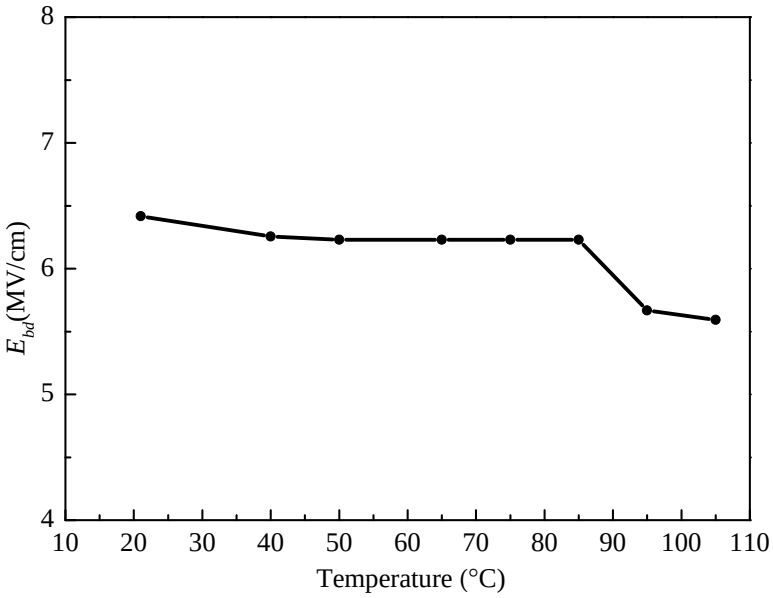


Figure 5.9: Temperature dependency of dielectric breakdown.

is attributed to the increase in leakage current at elevated temperatures. Leakage current is dependent on the charge carrier transport mechanism through the dielectric layer. At lower electric fields, electrical conduction is based on Schottky (thermionic) emission whereas at higher electric fields the conduction mechanism is dominated by Poole–Frenkel emission [99], leading to noticeable increase in leakage current. With increasing temperature the transition in conduction mechanism occurs at lower bias voltage levels causing the reduction of dielectric field strength [100].

MIM capacitor Yield Investigation

The backside of the fully fabricated WLP had integrated MIM capacitors on each sidewall. After performing C-V measurements on 12 structures, it was, unfortunately, discovered that there were no functional structures. The failure mode in all cases was short circuiting between top and bottom plates. These results prompted yield investigations on wafers with the test capacitors. Here, yield is defined as the ratio of operational devices to the total number of measured devices and assuming uniform defect densities. Calculation results are summarized in table 5.2. With reduction of dielectric layer thickness, it was observed that the yield of test

Table 5.2: Yield estimations for test MIM capacitors. t – layer thickness, Y – yield, D_0 – defect density.

	ALD Al_2O_3	**PEALD Al_2O_3**	**PEALD HfO_2**
$\boldsymbol{t}$ **(nm)**	95	43	43
$\boldsymbol{Y}$ **(%)**	95.6	81.1	82.3
$\boldsymbol{D_0}$ **(defects/mm^2)**	0.014	0.065	0.06

capacitors has reduced by up to 14.5 %. The defect density was calculated using eq. (5.1), assuming Poisson distribution of defects [101].

$$Y = \exp\left(-D_0 A\right) \tag{5.1}$$

Where A – area of test capacitor. The calculations suggest that a component with area of 200.97 mm^2 and dielectric layer thickness of 43 nm could have more than 13 defects. These results could explain why no working large area MIM capacitors were obtained. Since yield reduced with decreasing the ALD layer thickness, it is believed that the failure mechanism was short circuits due to pinholes in the layers which during processing were considered to be completely conformal. It has been reported that for thin layers (2 nm) of ALD Al_2O_3 the effectives of nucleation on the deposition surface [102] influences the pinhole density. For layers above 10 nm the main cause for defects is attributed to the presence of particles on the wafer surface that cause micro-masking. It is highly probable that surface contamination caused pinholes in our case, as depositions were performed outside class 100 environment. It was also observed that some particles fall on the wafer from the chamber walls, which is not cleaned after every deposition. Lowest defect density for ALD Al_2O_3 on a metal surface (Cu) was 0.08 defects/mm^2, for t=25 nm [103]. This value is comparable to defect density of MIM test structures (table 5.2).

5.4 Package Thermal Performance

The ability of the package to dissipate excess heat was evaluated by performing thermal imaging. Heat distribution was monitored using FLIR A655SC infrared camera. Chips were placed on a steel chuck, used as a heatsink, and 120 mA current was applied. The package was monitored for at least 20 min, which was sufficient to reach a stabilized temperature value. A thermogram of the top side wall (smallest area) is shown in fig. 5.10. The maximum temperature on the surface of the LED chip reached only 35 °C, or 10 °C higher than ambient. Heat was uniformly distributed across the surface of the chip, without hot-spots. A piece of cardboard, which is a poor thermal conductor (0.21 W/m·K), was placed under the chip and the measurements were repeated. As expected, in this case, the chip temperatures were substantially higher (fig. 5.11), as heat dissipation by means of conduction was strongly diminished. Convection and radiation were not sufficient to transfer heat away from the device, leading to LED surface temperature increase to 78 °C. The PI layers appear warmer that than the LED chip, whereas the Al interconnect seems cooler, because of the difference in emissivity values of materials.

The obtained thermal imaging results indicate that the fabricated device can effectively transfer heat away from the LED chip. A heatsink still needs to be used however, as the amount of generated heat cannot be dissipated by means of free air convection and thermal radiation alone.

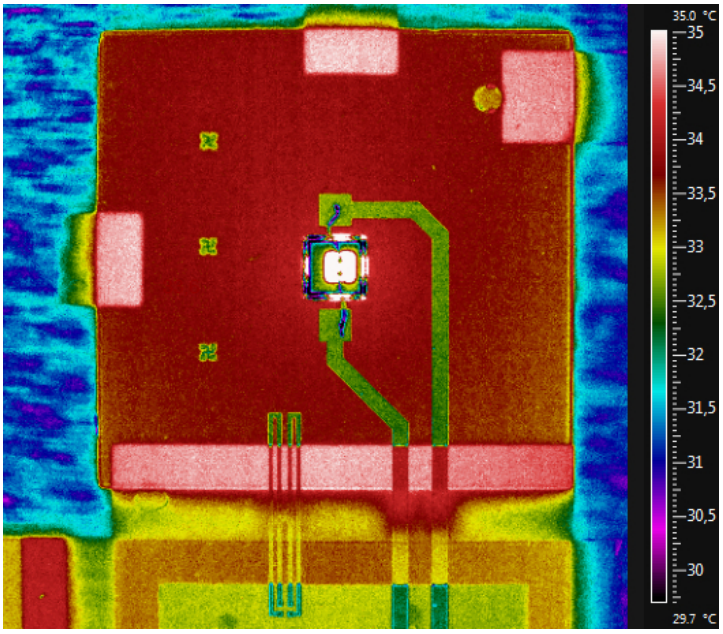


Figure 5.10: Thermal image of WLP on metal chuck after 20 min.

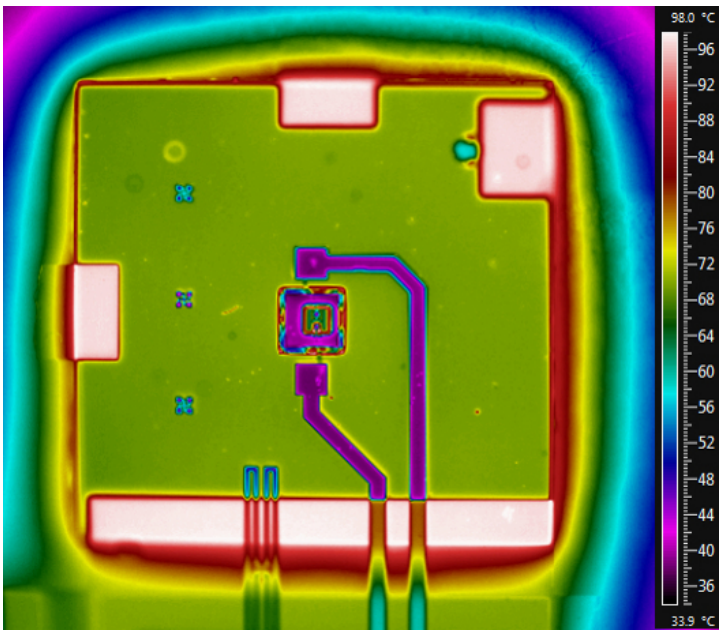


Figure 5.11: Thermal image of WLP on thermal insulator (cardboard) after 20 min.

5.5 Device Optical Performance

An integrating sphere with a diameter of 0.5 m was used to perform the optical measurements. The total spectral power was measured and the relevant parameters were automatically extracted using the proprietary software used for optical characterization, developed by Philips Lighting. The device under test (DUT) was placed on a heatsink with temperature control, connected to a pulsed power supply and loaded inside the sphere. Calibration was carried out before starting the measurements to compensate for light absorption by the chip. Measurements were performed in pulsed voltage mode to avoid heating of the LED chip. Junction temperature was ramped via the heatsink and monitored using a thermocouple.

Typical spectral power distribution (SPD) of a commercially available while light LED is shown in fig. 5.12. For comparison, the SPD obtained from the measurements of the DUT

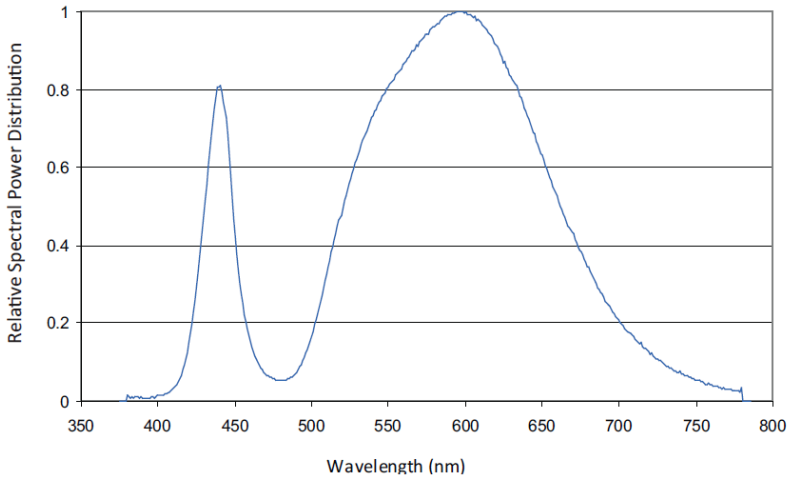


Figure 5.12: Relative SPD of while LED with CCT=3000 K [104] at 25 °C.

with applied phosphor based color conversion, as described on page 53, is shown in fig. 5.13. It is evident that the fabricated device had the peak power component in the blue region with

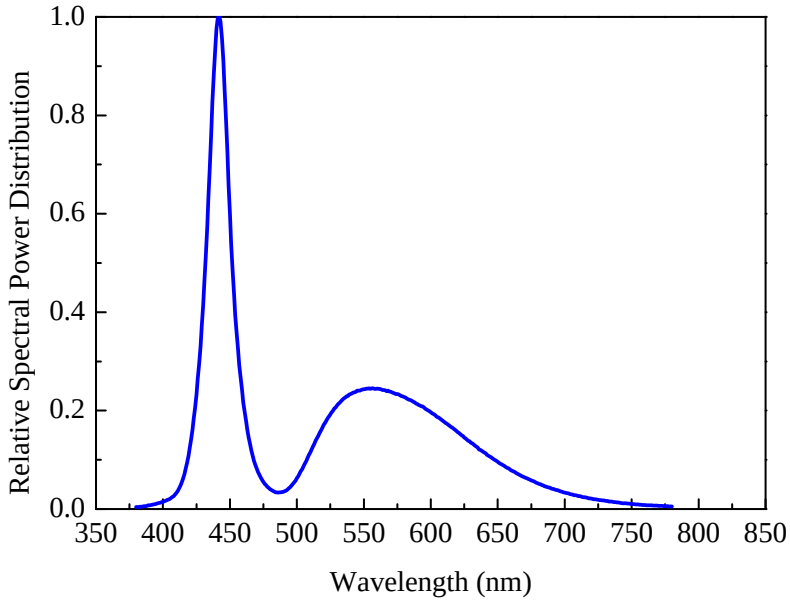


Figure 5.13: Relative SPD of fabricated WLP at 25 °C after color conversion.

less power in the wide yellow-green region, whereas for the commercial LED, peak power was obtained in yellow-green region of the visible spectrum. It can be stated that the phosphor concentration and layer thickness were insufficient to convert the necessary amount of blue photons to yellow, leading to a pale blue light with CCT=13800 K, compared to warm white with CCT=3000 K of the commercial LED. The CCT can be corrected by increasing the phosphor to silicone ratio of the encapsulation mixture.

Luminous flux (Φ_{lum}) of the device was measured as a function of temperature (fig. 5.14). The highest measured lumen output was 92 lm, at 25 °C and I_f=120 mA. The light intensity reduced by 14 % when the device temperature was raised from 25 °C to 100 °C, which is

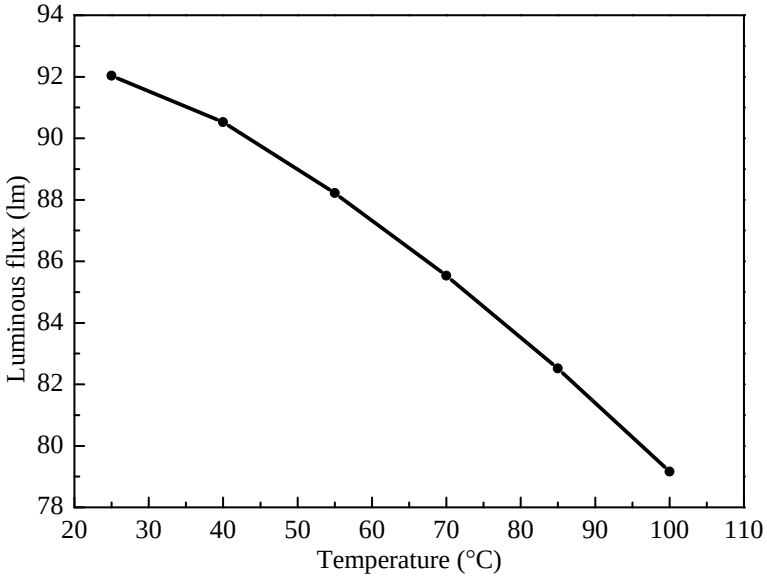


Figure 5.14: Luminous flux of the device as a function of temperature.

consistent with the LED manufacturer's specifications [95]. Due to the pronounced peak of blue light in the output spectrum the the achieved color rendering index was rather low CRI=70, not suitable for indoor applications.

5.6 Chapter Summary

Electrical, thermal and optical characterization of the fabricated 3D wafer level package was covered in this chapter. Flexible interconnects were tested by cyclic bending on a custom made testing setup. No deterioration of electrical conductance was observed after 2000 bending and release cycles. Al_2O_3 and HfO_2 dielectric layers, grown by ALD, were characterized as candidates for MIM capacitor fabrication. Dielectric constants, breakdown voltages, linearity coefficients and thermal robustness were determined from these measurements. The ability of silicon based packages to dissipate large amounts of heat generated by LED chips was studied by thermal imaging. Uniform heat distribution was observed across the surface of the package without any hot-spot formations. It was concluded that heatsinks are still required, if these devices were to operate below 85 °C. Finally, optical parameters were extracted by performing spectral power measurements using an integrating sphere. Luminous flux depreciation with temperature was determined. CCT, SPD and CRI were compared to a commercially available packaged white LED.

Chapter 6

Conclusions and Future Outlook

6.1 Results and Conclusions

The further expansion of SSL sources into the general purpose illumination market demands continuous cost reduction without trade-offs in terms of light output, reliability, quality and lifetime of the final product. As reported by [4], packaging can account for up to 50 % of the final device cost. This indicates that there is high potential to cut down costs by developing and implementing novel packaging solutions on a large production scale. In general, cost reduction in SSL can be achieved by utilizing cheaper materials and components combined with high throughput and mature fabrication and assembly processes. Often compromises between the amount of light output and quality, thermal management, reliability, power consumption or lifetime need to be made, that are governed by the intended application of the SSL product and competitive price. Design spaces, that are optimized with respect to aforementioned requirements, are being extensively developed by means of numerical calculations, FEM simulations, measurements and lifetime estimations to assist product development [105].

Wafer level packaging is a promising approach for cost reduction, as devices can be packaged directly on the wafer, rather than individually. The focus of this Master's project was to develop a novel wafer level based packaging platform for SSL applications. This package would be fabricated on Si substrate and consists of multiple LEDs, placed inside individual reflector cavities. The package would be segmented into Si islands and electrically connected with flexible interconnects by employing a modified rigid-flexible-rigid process [62]. In addition, upon release from the substrate wafer, the package would be folded into a 3D shape compliant with form factor constrains of miniature luminaires, thereby forming a wafer level LED assembly. To achieve these goals, a design, comparable to the G4 LED Capsule [43] was made, a fabrication process flow developed and implemented in a class 100 cleanroom environment. The processing involved numerous challenges as discussed in the previous chapters, however demonstration devices were successfully fabricated and the main goals achieved with promising results as summarized below:

- **Developed back-end-of-line compatible process flow for flexible Si based WLP**. The fabricated package consisted of the following structural elements:
  - **Rigid Si sidewalls and top cover, joined by flexible hinges**. Results in

cuboid (fig. 4.9) form factor.

- **Flexible interconnects** based on neutral bending plane design between two layers of PI. Two approaches of interconnect placement on the rigid islands were investigated. By depositing Al directly on the non-patterned PI layer processing complexity is reduced, however wire bonding becomes challenging due to soft underlying layer and delamination. Patterning the PI layer before Al deposition results in interconnects formed directly on the wafer at the cost of additional processing complexity of patterning interconnect on PI slopes. Interconnect durability was confirmed by cyclic bending tests. No resistance increases were observed after 2000 bends.
- **Reflector cavities coated with Al**. Tapered sidewall profile allows to form directional light patterns as well as ease silicone dispensing by preventing material spread across the surface.
- **Front-to-backside flexible interconnects**. High flexibility was demonstrated by folding over the edge of the chip. Electrical interconnection was successfully made using silver paste. This method could be further developed as a viable candidate to replace wire bonding or TSVs for 3D stacking of chips with low to medium pitch, peripheral pad layout. The advantages of this method are: accurate, lithographically defined interconnect formation, electrical insulation of each metal track and higher durability compared to wire bonding.
- **Passive components on the backside**. Demonstrated compatible backside BEOL process for MIM capacitor integration. Unfortunately devices were not operational due to challenges related to pinholes in large area ALD films.

- **Demonstrated post-fabrication assembly on wafer level**. Blue LEDs were attached with thermally conductive silver paste and wire bonded to the fabricated flexible interconnects. Color conversion was demonstrated by glob-top dispensing phosphor-silicone mixtures inside reflector cavities. Devices were tested on a wafer, before release form substrate, by probing and applying current.

- **3D form factor**. Packages were removed from the substrate by cutting the support tabs. No wafer dicing was required as individual chips were formed by backside DRIE etching. Device folding using 3D printed structure with vacuum clamping was demonstrated. Similar folding can be done directly on a metal heatsink. Devices were still operational after folding.

- **Thermal and optical performance**. Uniform heat spreading and dissipation was observed by thermal imaging. A heatsink is still required to maintain components below 85 °C. Optical measurements revealed typical luminous flux degradation with temperature. Highest flux at room temperature was 92 lm at 120 mA. CCT was outside the range of white light but this can be solved by adding higher concentrations of phosphor into the encapsulation mixture.

6.2 Recommendations for Future Work

The main deliverable produced by this work is a platform developed for fabrication of flexible/foldable silicon packages and chips. Therefore proposed future work is mostly based on further improvement of the process as well as expansion of package functionally by monolithic/heterogeneous integration.

Recommendations for Process Improvement

- **Void free polyimide processing**. In this work PI was dispensed manually, by pouring directly from the container. An automated dynamic dispensing system is recommended for PI spin-coating. It would prevent excess material waste, improve layer thickness reproducibility and enable automated edge bead removal and backside rinse, eliminating the need for lithographically defined EBR. The main drawback of litho-defined EBR is pinhole formations in spin coated photoresist layers. These pinholes are difficult to detect and result in circular voids in the PI layer after wet etching in 2.5 % TMAH solution. Hardbaking with temperature ramp-rate (3 to 6 °C/min) control is recommended to avoid rapid solvent outgasing which can also cause voids.

- **Aluminum interconnect patterning**. Two main challenges arose when patterning Al on substrates that contain patterned PI layers. The first issue was cross-linked photoresist removal after Al plasma etching. The standard method of hardened resist removal is O_2 plasma ashing. It cannot be directly applied, as the plasma will also etch PI. In this work, wet Al etching was used to avoid resist cross-linking. Another method is 75 °C NMP resist stripping combined with short O_2 plasma steps. The best approach depends on the critical dimension and thickness of the Al line. The other challenging aspect was to pattern Al on the slopes of PI. The method used in this work was a two cycle exposure-development "optical drilling", described on page 31. The process of Al patterning on slopes should be further developed to avoid the double exposure method as it is time consuming and undercutting or notching of the photoresist can occur due to UV light reflection off the Al layer.

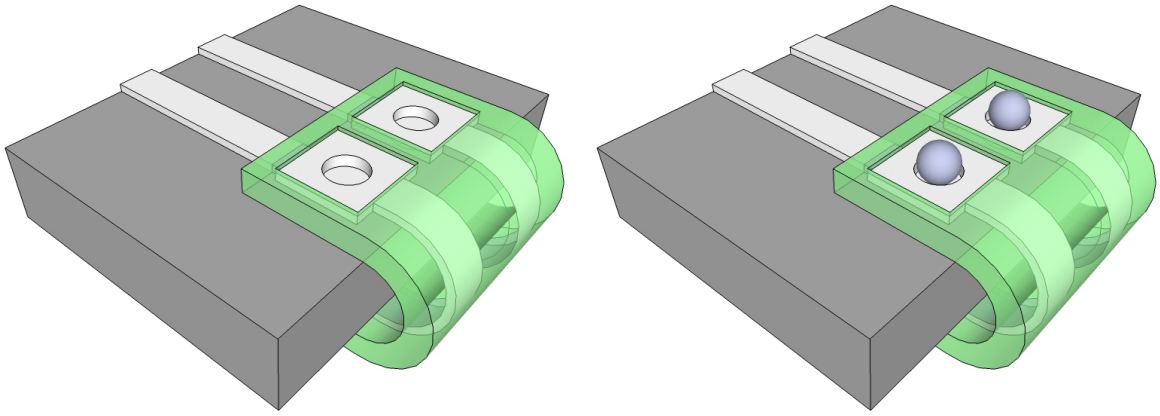
- **Reflector cavity metalization**. In this work the cavities were metalized by utilizing the same mask as for cavity etching by inverting the pattern with negative photoresist. It is recommended to avoid negative resist with PI processing as it is difficult to remove with chemical solvents. A dedicated cavity metalization mask combined with positive resist is the recommended option.

- **Chip Release and Assembly**. The fabricated chips need to be released from the substrate. Wafer dicing is not required so a method similar to metal punching could be employed to cut out the chips from silicon frames. Automation of package folding technique should also be developed.

Recommendations for Functionally Expansion

- **Electronics Integration**. The flexible interconnect fabrication is fully BEOL compatible. Active semiconductor components could be integrated on the substrate wafers. Driver circuitry components, including p-n diodes, power MOSFETs and rectifiers could be integrated monolithically or by pick-and-place assembly of bare die components.

- **Re-flow soldering compatible flexible front-to-back structure**. The structures shown in fig. 2.12 can be modified by making openings in the middle of the bondpad (fig. 6.1(a)). The PI would be etched and solder ball re-flow (fig. 6.1(b)) used to form electrical connection and provide adhesion.



(a) Backside view of bondpads with cavities (b) Backside view with solder balls in cavities

Figure 6.1: Schematic representation of front-to-back interconnection

- **Passive Component Integration**. Inductors, resistors and capacitors could also be integrated in the WLP package. Due to challenges of fabricating large surface area components, it is recommended to investigate the options for heterogeneous integration of passives e.g. packaged miniature form factor components, silicon based, bare die components (as produced by IPDiA). Parallel arrays of smaller area components could also be integrated with increased yield.

- **Cooling Design**. The Si based package demonstrated superior heat spreading capabilities. An appropriate cooling design still needs to be implemented for heat dissipation. An assembly structure for package folding and the heatsink could be combined.

- **Sensing Functionality**. Si based optical and thermal sensors could be integrated inside reflector cavities to monitor junction temperature and peak color shift of the LED chip. A feedback system could be used to adjust driving current in case component overheating is detected.

- **Wafer Level Optics**. Miniature lenses can be formed on wafer level by glob-top [38] or injection mounding [37].

Appendix A

Complementary Technologies for 3D integration

The emerging trend for 3D integration of various semiconductor technologies into a heterogeneous SiP is based on vertical stacking of individual chips. The continued development of such systems strongly depends on the following technologies: TSVs, wafer thinning and wafer bonding.

Through silicon vias

TSV, as the name suggests, is a vertical interconnection used for connecting the back of the wafer or die to the front. The application is not strictly defined for through silicon interconnection, so a more general term is through strata via [8]. TSVs are usually classified into 2 major categories:

I. TSVs fabricated during IC processing, further sub-divided into:
   - Front-end-of-line (FEOL) TSVs, fabricated before the first interconnects layer
   - Back-end-of-line (BEOL) TSVs, fabricated during metal interconnects processing

II. TSVs fabricated after IC processing (post BEOL TSV), further sub-divided into:
   - Via first i.e. vias processed before wafer bonding
   - Via last i.e. vias processed after wafer bonding

FEOL TSVs need to be compatible with high temperature processing. The conducting material used is highly doped polysilicon. The resistivity of phosphorus doped polysilicon (450 $\mu\Omega$·cm) is higher than that of metals, but is acceptable for certain applications [106]. BEOL TSVs are incorporated during IC metallization. The metals used are copper (Cu) or, less commonly, tungsten (W).

The post BEOL TSVs can be fabricated at a separate foundry as long as certain exclusion zones are designed in the device layout. Outsourcing TSV fabrication will reduce the equipment requirements for the IC foundry as well as introduce more flexibility for chip stacking. The post BEOL approach also allows the formation of TSVs before or after the 3D IC stacking to further optimize the complete chip assembly process.

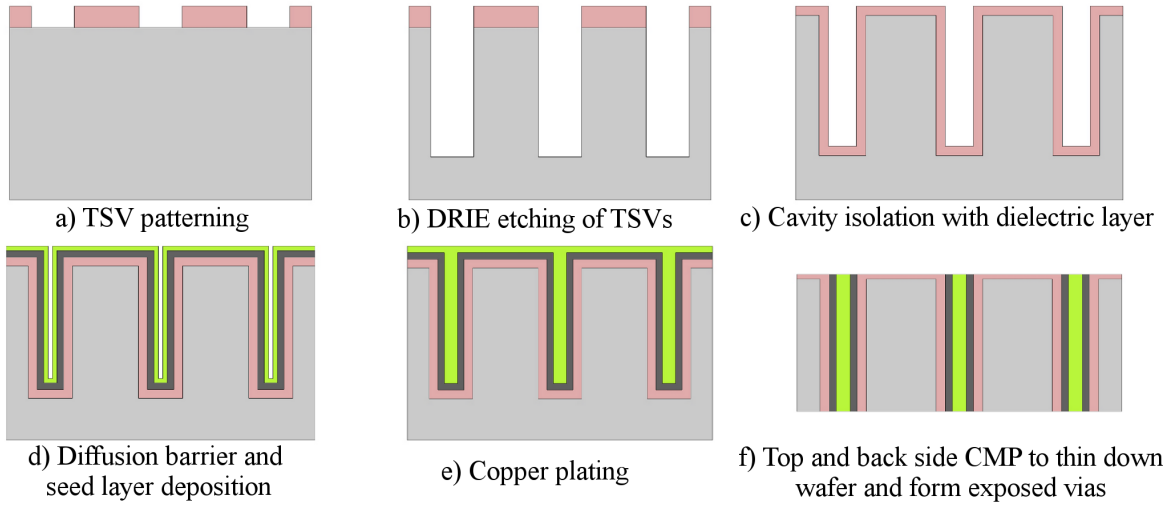


Figure A.1: TSV fabrication process flow.

A typical fabrication flow of cooper TSV is presented in fig. A.1. After the TSV layout is lithographically patterned (fig. A.1a) using a hard (SiO_2) or photoresist mask, vias are etched using deep reactive-ion etching (DRIE), Bosch process (fig. A.1b). When the cavities are etched, they need to be isolated with a thin layer of dielectric material as well as a TiN barrier layer (fig. A.1c-d) to prevent copper diffusion into silicon [107]. A thin seed layer of Cu is then deposited by physical vapour deposition (PVD) or metal-organic chemical vapour deposition (MOCVD) (fig. A.1e). After lining the trenches with the seed layer, void free copper filling is performed by electro or electro-less plating. Finally, the wafer is polished and thinned down from both sides to form separate TSVs that are now ready for interconnection (fig. A.1f).

Wafer thinning

Wafer thinning is needed when stacking dies to reduce the vertical footprint of the chips and reduce the resistance, delay and aspect ratios of TSVs. Heat dissipation is also improved by thinning the substrate [9]. There are several approaches and techniques for wafer thinning which will now be briefly discussed.

Depending on the application, wafers are thinned to at least 100 µm and up to below 10 µm [108]. Thinning begins with wafer grinding. The active side of the wafer is protected by special UV light sensitive tape. Grinding is performed in two stages: coarse grinding, to remove the bulk of the wafer thickness and fine grinding and to remove the damaged silicon layers from the previous step and reduce surface roughness. Coarse grinding damages the crystal surface of the wafer, introducing fractures and surface oxidation, which causes bowing towards the top active side of the wafer due to tensile stress. The following fine grinding is one of the steps to reduce the bow by removing the damaged surfaces and reducing roughness, but some of the stress still remains. After grinding, the surface is treated with chemical-mechanical polishing (CMP) to remove remaining surface defects and wafers are cleaned from residues using wet chemical cleaning solution.

Alternative approaches for wafer thinning are dry plasma etching or wet chemical etching. Plasma etching is similar the Bosch process, but without passivation steps, but still using

fluorine based chemistry (SF_6, CHF_3) [9]. An alternative is atmospheric downstream plasma etching using CF_4 [109]. Plasma etching ensures etching uniformity and less damage to the surface at the cost of slower etch rate and costly equipment. Wet etching is performed in a chemical bath or tank. Most used compounds are solutions of strong bases of potassium hydroxide (KOH) or tetramethylammonium hydroxide (TMAH). These exhibit Si crystal plane dependent anisotropic etching, so are not suitable for high aspect ratio structure formation. Isotropic Si etchant is HNA, a mixture of HF:HNO_3:AcOH. Wet etching suffers from even slower etch rates than plasma etch. If the front-side of the wafer is already patterned with interconnects special vacuum chucks are used to prevent contact with the etchants. Wet etching however is not limited by equipment batch sizes and is the cheapest solution.

Wafer bonding

To achieve a robust 3D stacking process, chips with different functionalities need to be reliably attached to each other. Whether wafer-to-wafer, chip-to-wafer or chip-to-chip assembly scheme is employed, bonding techniques are required for stable chip fusion. Accurate methods of alignment are necessary before the bonding process. Similarly to lithography alignment, marker structures at defined wafer locations are used to align the wafers to each other. For stacking two wafers, optical access to a set of markers on both wafers is required, when direct alignment method is used. Typical misalignment is $\pm 2\,\mu m$. The disadvantage of direct alignment is that the stack thickness is limited to two layers and the alignment markers need to be at the bonding interface or the accuracy will reduce due to optical effects such as diffraction or reflection. Wafers covered with non IR transparent layers, like Al, also cannot be directly aligned. As an alternative, indirect alignment method is then used. Wafers are aligned not to each other, but to external reference points – the microscope focus points. Once the first wafer is aligned, the microscope lenses are fixed, wafer is moved on the z-axis and the second wafer is aligned to the same focal points of the lenses. Finally, both wafers are moved onto the bonding chuck, but during this movement wafers can shift and misalignment occurs which is left uncorrected, leading to $\pm 5\,\mu m$ alignment errors [110]. More advanced indirect alignment approaches are used when sub micrometer tolerances are required, such as SmartView and 3D align [110, 111]. The former uses 2 pairs of lenses, for the top and bottom wafers, that are calibrated with respect to each other so the focal points are very accurate. The wafers are vacuum attached to horizontally moving stages in close proximity. After sequential alignment, both wafers are brought into contact. 3D align uses a modified stage and a periscope style mirror system to overlay top and bottom wafer alignment marks.

After alignment wafers are brought into contact and bonded using one of the following methods [112]:

- *Direct bonding.* Requires smooth wafer surface with roughness less than 10 Å. Surfaces are cleaned and hydrated, brought into contact starting with the centre point and surface attraction forces promote contact across the entire surface. It is critical that no particles or air is trapped at the interface. To complete the bond high temperature annealing is carried out at 800 °C–1000 °C. Direct bonding is generally carried out between Si−Si or SiO_2−SiO_2 surfaces [112].

- *Anodic bonding*. This method is widely used for bonding silicon wafers to glass wafers. The glass wafer is used as a transparent and hermetic sealant for sensors, microfluidic channels and other applications. The mechanism of anodic bonding consists of heating the substrates to temperatures of 400 °C–450 °C (BEOL compatible) and applying a high DC voltage of 400 V–1200 V. The strong electric field causes ion migration and irreversible high strength chemical bonds are created at the bonding interface [112].
- *Intermediate layer bonding*. Similar method to direct boning, however by covering the bonding surfaces with thin layers of silicides, silicates, solder, polymers, or metals it is possible to lower annealing temperatures. Cu−Cu is especially promising technology, because TSVs patterned during BEOL processing can be used as bonding pads, electrical interconnects and thermal conductors. Thermal compression bonding of Cu layers is based on inter-diffusion of copper atoms [113]. The process consists of surface preparation (bondpad formation, CMP, surface cleaning), applying compression force at temperatures of 350 °C to 400 °C and post bonding anneal at the same temperature in N_2 ambient. Polymer based bonding is a simple process for quick bonding at temperatures of 200 °C–250 °C, widely applicable for temporary bonding of thinned wafers onto carrier substrates.

Appendix B

Heat Dissipation in LED Packages

With increasing packaging densities and higher froward current levels the continuous improvement in heat dissipation of LED packages is essential. The improvements in thermal performance of LED packages over the last three decades is shown in fig. B.1 For applications

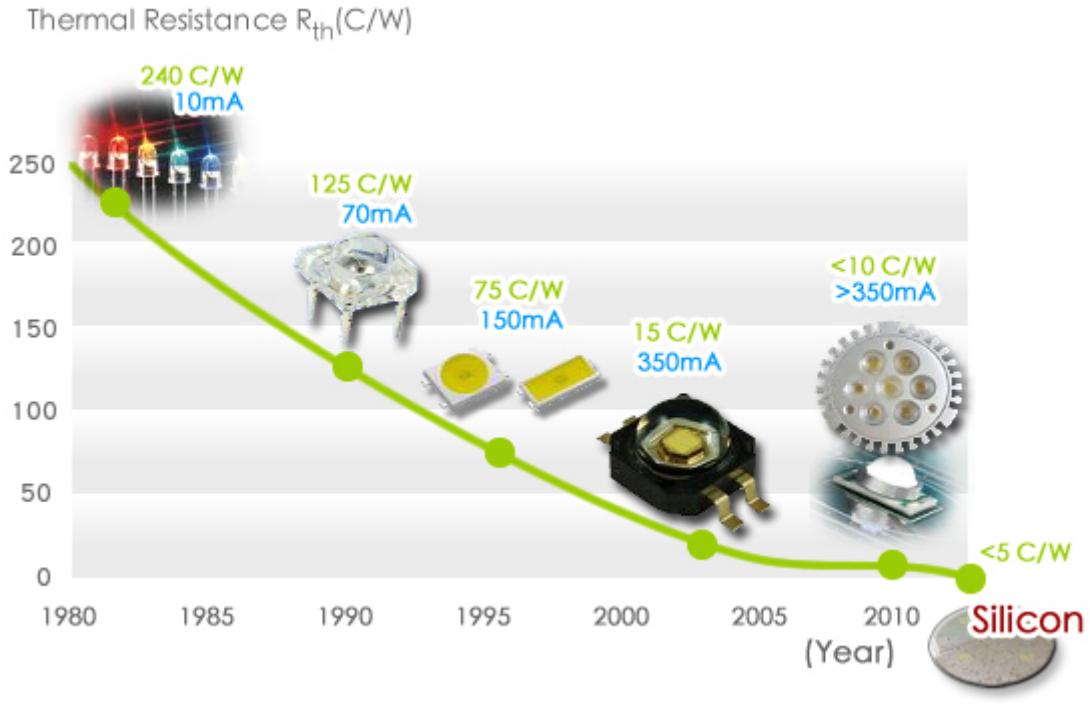


Figure B.1: Development of LED packages in terms of reduction in thermal resistance. (Source: http://www.viseratech.com)

such as indicator lights, with low power LEDs, commonly used packages are known as lead frame e.g. T1 (d=3 mm) T1-3/4 (d=5 mm). Such packages contain a single die, mounted inside a reflector cup and wire bonded to the contact leads as shown in fig. B.2. The chips are encapsulated using epoxy resin. The refractive index of the epoxy encapsulant is typically in 1.5–1.8 range which is closer to the refractive index of the LED (n_{GaN}=2.5), so more photons are able to escape from the chip, because the critical angle for total internal reflection is

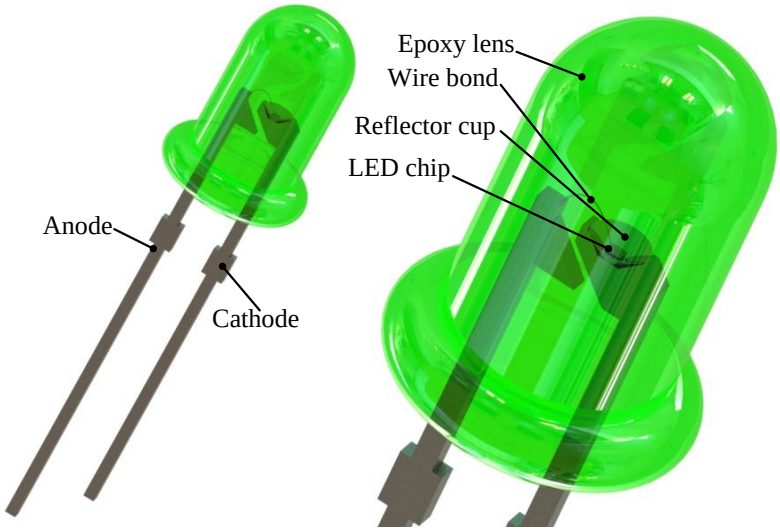


Figure B.2: Low power lead frame through-hole LED.

increased, according to Snell's law:

$$n_1 \sin\theta_1 = n_2 \sin\theta_2 \tag{B.1}$$

where n_1 and n_2 are the refractive indexes of two media, θ_1 and θ_2 are the angle of incidence and transmittance of light. When $n_1 > n_2$ for a certain incidence angle (θ_1), θ_2 can become 90°. This is known as the critical incidence angle (θ_{crit}) for total internal reflection:

$$\theta_{crit} = \arcsin\frac{n_2}{n_1} \tag{B.2}$$

Hence closely matched values of refractive index will broaden the light escape cones. The top of the encapsulant is dome shaped to prevent internal reflection at the boundary with air and also acts as a lens. Lead frame packages, mounted on PCBs using through-hole technology, dissipate most of the heat coming from the LED die through the cathode leg. Thermal resistance is approximately 250 K/W, which is too high for SSL applications with high brightness LEDs [114]. High power packages like the Barracuda from Lumileds were introduced to accommodate HB-LEDs for SSL applications. These packages come in various dimensions and shapes intended to accommodate a broad range of luminaire designs. Typical design of power packages consists of a flip-chip LED die mounted on a Si sub-mount, which contains ESD protection circuitry, commonly consisting of multiple p-n junction diodes or Zener diodes. The sub-mount is wire bonded to the SMD anode and cathode leads for electrical connection and the bottom is soldered to a metal slug to dissipate heat from the LED. The slug itself is soldered to a heatsink or metal core PCB to effectively spread the generated heat over a larger area. Chips are encapsulated with silicone and a plastic lens is put on top that also provides mechanical rigidity. A cross-section of power LED package is shown in fig. B.3. Such a single die package typically has thermal resistance of around 15 K/W and when mounted on a PCB this value would reduce to 6 K/W since heat flux effectively spreads across a larger area. [13]. Currently, high power LED packages can incorporate multiple chips

to achieve higher luminous flux. Products like Luxeon K from Philips Lumileds contain arrays of up to 24 LED chips with individual lenses. These arrays emit more than 3000 lm of light at CCT=5000 K and have thermal resistance of only 0.5 K/W [115].

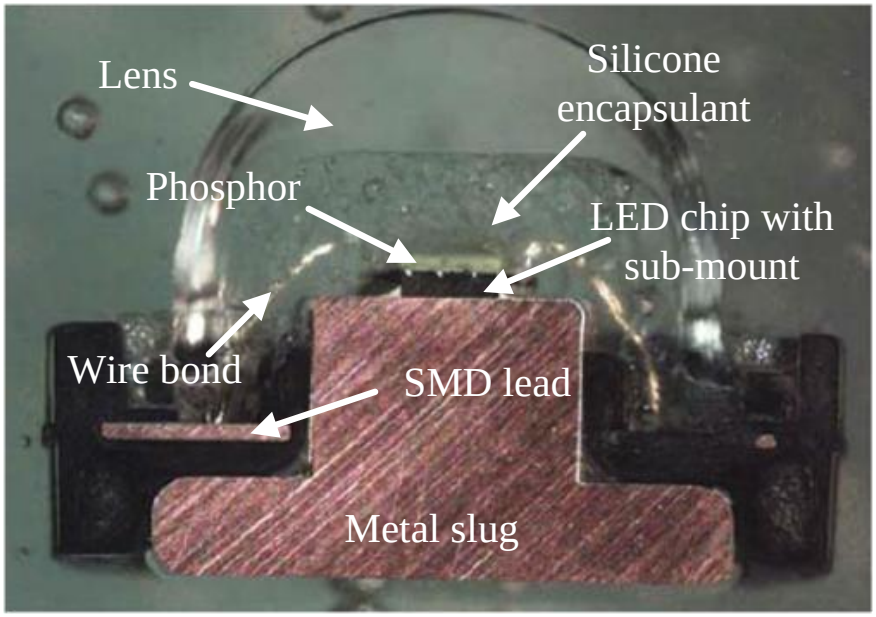


Figure B.3: Cross-section of HB LED package from Lumileds [22].

The packaging density of SSL packages is limited. In applications that require high luminous output and uniformity many LED chips with small light emitting surfaces need to be placed as close as possible to each other. Chip-on-board (CoB) is an emerging packaging technology for aforementioned functions. Currently available products report thermal resistance values as low as 0.22 K/W [116]. In this approach, LED dies with silicon sub-mounts are soldered directly on the printed circuit board (PCB) layer with low thermal resistance. Thermal path from chip to heatsink is reduced and there is no need for a metal slug to channel the heat flux, which allows for higher packaging density and package cost reduction. A range of options for the PCB selection are available depending on the required overall thermal power dissipation capability. Metal core PCB is a viable solution for CoB designs. Mounting chips directly on the top surface will not yield significant performance gains because the top dielectric layers of such PCBs are made from composites of epoxy mixed with inorganic powders, which have poor thermal conductivity in range of 2–10 W/m·K. Options to replace this dielectric layer with alumina (Al_2O_3), deposited by aerosol deposition, which has a higher thermal conductivity (27 W/m·K) have been reported [117]. An alternative option for CoB designs aimed at minimizing thermal resistance is to remove the surface dielectric entirely and solder LED chips directly to the electrically conductive layer. Thermal conductivity improvements can be achieved, but high density chip arrays with parallel connections can lead to increased current densities and charging of the metal substrate and heatsink, leading to reliability concerns due to electrostatic shock damage. These issues can be avoided by using die attach methods employing non conductive materials, at the expense of increasing $R\theta$. An even higher long term reliability concern arises from CTE (coefficient of thermal expansion) mismatch. Commonly used metals have CTE in a range of 16 to $24 \times 10^{-6}\,K^{-1}$, where as for Silicon it is

only $4 \times 10^{-6}\,\mathrm{K}^{-1}$. Thermal stress, induced during device operation at elevated temperature, can result in defects due to deformations, delamination at the interface and cracks [23, 118].

Ceramic substrates, despite having lower thermal conductivity than metals, are more suitable for LED packaging. Ceramics are insulators, which allows direct surface mounting of chips with thin layers of solder. The substrate can in turn be soldered to a metal heatsink which remains electrically isolated. Ceramics are well suited for HB-LED packaging because of their thermal-mechanical stability, CTE values comparable to GaN and Si along with options to form multi-layer packages. Al_2O_3 is an easy to manufacture low cost material for ceramic CoB substrates. Alumina has a rather low thermal conductivity, so other ceramics are being investigated as candidate substrates. AlN and BeO (beryllium oxide) are ceramic materials with high thermal conductivities of 175 W/m·K and 300 W/m·K respectively. AlN is however costly to manufacture and can cause reliability concerns because of brittleness of the material [119], whereas BeO is highly toxic and requires additional precautions during processing [120]. Aluminum silicon carbide (AlSiC) is a highly promising metal matrix composite (MMC) ceramic with thermal conductivity of 200 W/m·K, which is higher than pure Al, and CTE of only $7.4 \times 10^{-6}\,\mathrm{K}^{-1}$. Examples of cast AlSiC substrates for LED packaging have been successfully demonstrated by [121].

Appendix C

Phosphor Coating Methods for SSL

The conventional way of dispensing phosphor-silicone mixutes is by freely injecting the substance inside the reflector cup. This method has limited controllability over the layer thickness resulting in non-uniform distribution of phosphor across the surface of the chip, with buildups of thickness in the center and depletion at the edges (fig. C.1a). Because the

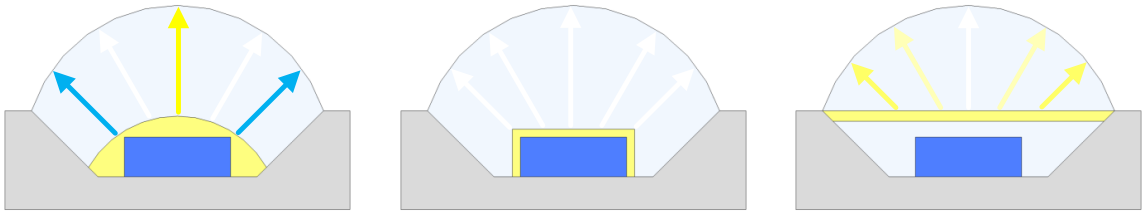


Figure C.1: Phosphor dispense methods: a) freely dispensed phosphor, b) conformal coating, c) remote coating. Color shifts for each method are also show.

proportions of absorbed and transmitted light directly depend on the phosphor layer thickness, noticeable shifts in CCT across the emission surface of the source are observed, varying from yellowish color in the center towards blue at the edges. The non-uniformity of the phosphor layer in the mixture is caused by the settling or sinking of the phosphor power to the bottom of silicone layer during curing. It was discovered that fumed silica acts as an anti-settling agent [23] and prevents phosphor particles from clumping, which in turn results in better thickness uniformity and reduced color shifts.

A conformal coating method (fig. C.1b) developed by Lumileds enables equal distribution of phosphor layers over the entire LED surface using electrophoretic deposition (EPD). The process uses charged phosphor particles dispensed in electrolyte solution. The substrate containing the LEDs is biased oppositely to phosphor particles and brought into the solution. Under applied electric field, particles move towards the substrate and form a conformal layer on the chip surface [24]. Only flip chip LEDs can be used for EPD because a flat top surface is needed. An alternative conformal coating method that uses pulsed spraying of silicone-phosphor mixtures allows usage of wire bond LEDs and is considered more environmentally friendly than EPD [25]. LED chips with conformal phosphor coatings produce high quality white light with no CCT variations across all viewing angles.

The first two discussed approaches are used to deposit phosphor in close proximity to the chip surface and are well suited for miniature and high density packaging applications. Phosphor layers typically back-scatter roughly half of the incoming light. With proximate phosphor distribution most of the back-scattered light is reabsorbed by the LED die and causes significant reductions in light extraction and can even cause localized heating of the chip, leading to overall drop in luminous efficacy. For this reason, a method to place the phosphor coating within a certain distance from the LED surface was introduced [26]. Remote phosphor coating (fig. C.1c) requires the LEDs to be in a reflector cup. It is filled with transparent encapsulant which is pre-cured first followed by silicone phosphor mixture at the top of the reflector. The probability for the back-scattered light to fall on the surface of the chip greatly reduces with distance between the chip and phosphor since most of the light is reflected back by the cup sidewalls [13]. The CCT distribution of emitted light is superior to that of conventional method, but is inferior to conformal coating, because the thickness of the remote phosphor is not entirely uniform and tends to be thicker at the center as the surface is slightly concave instead of being perfectly flat due to surface tension effects. An even higher increase in light extraction (above 60 % compared to conventional coating) efficiency as well as improved special color distribution can be achieved by placing the phosphor further from the reflector on the secondary optics of the system as reported by [26].

Appendix D

Dielectric Constants

Table D.1: Dielectric constants of selected materials for MIM applications.

Material	**Dielectric constant (k)**	**Ref.**
SiO_2	3.9	[66]
Si_3N_4	7-9	[66]
Al_2O_3	9	[66], this work
Y_2O_3	10-15	[92]
Sm_2O_3	19	[72]
HfO_2	19-25	[93], this work
Ta_2O_5	19-26	[94]
ZrO_2	23-29	[94]
La_2O_3	27	[94]
Pr_2O_3	31	[66]
SiC	40	[66]
TiO_2	30-115	[66]
$SrTiO_3$	95-170	[98]
BST	360-420	[82]
PZT	950-1600	[81]

List of Publications

Contributions to Conference Proceedings

1. P. Liu, J. Zhang, R. Sokolovskij, H. van Zeijl, B. Mimoun, and G.Q Zhang, "Geometric optimization of high performance interconnect of Rigid/Flexible/Rigid substrate for Wafer Level Packaging in Solid State Lighting applications by numerical simulations," in *Thermal, Mechanical and Multi-Physics Simulation and Experiments in Microelectronics and Microsystems (EuroSimE), 2013 14th International Conference on*, 2013, pp. 1-6.

2. H. Ye, H. van Zeijl, R. Sokolovskij, A.W.J Gielen, G.Q. Zhang, "Advanced LED package with temperature sensors and microfluidic cooling," *Electronic Components and Technology Conference (ECTC), 2013 IEEE 63rd*, vol., no., pp.1920,1925, 28-31 May 2013

Proposals for Intellectual Property Applications

1. R. Sokolovskij, P. Liu, H. van Zeijl, W. Van Driel, G.Q Zhang "3D wafer level package for solid state lighting applications", under review

2. R. Sokolovskij, P. Liu, H. van Zeijl, W. Van Driel, G.Q Zhang "Method for front-to-backside interconnection of silicon chips", under review

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