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DOI
10.1109/ECTC51687.2025.00126

Publication date
2025

Document Version
Final published version

Published in
Proceedings - IEEE 75th Electronic Components and Technology Conference, ECTC 2025

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***Abstract*—Accurate characterization and calculation of the interfacial stresses are of key importance for the optimization of the chip sintering process and the evaluation of the long-term reliability of the chip interconnect. In this study, the pioneering application of confocal Raman spectroscopy for the accurate, rapid, and nondestructive characterization of interfacial stresses at the interconnections of silicon carbide chips was undertaken. Silicon carbide chips (5mm*5mm) were mounted to active metal brazing substrates by pressure-assisted sintering using copper nanoparticles. Subsequently, finite element simulations were used to model the thermally induced deformation and stress in the SiC chip. The thermally induced warpage of the SiC chip was then measured using interferometry. Finally, confocal Raman spectroscopy was employed to measure the interface stress distribution at the SiC/sintered copper interface. The results showed that finite element simulations could not accurately assess the thermally induced deformation and stress in the SiC chip. The proposed method based on confocal Raman spectroscopy for testing chip interconnection interface stresses achieved an excellent balance between accuracy, non-contact measurement, and non-destructive testing. The residual stress at the backside interface of the SiC chip was concentrated in the central region of the chip, with compressive stress values ranging from -139 MPa to -165 MPa. Theoretically, this study provides a new framework for modeling and researching the reliability of electronic packaging interfaces.**

Keywords—SiC chip; Interface Stress; Confocal Raman Spectroscopy; Sintered Nano-Cu;

I. INTRODUCTION

Recent advancements in silicon carbide (SiC) devices have led to their widespread use in high-temperature, high-frequency, and high-power density applications, such as electric vehicles, renewable energy, grid conversion, and aerospace [1, 2]. Progress in material growth, device manufacturing, and packaging technologies has improved the reliability and cost-effectiveness of SiC power devices, accelerating their market adoption. However, packaging technologies still limit their reliability under high power density and operating temperatures. The die attachment process, crucial to packaging, directly affects thermal management and long-term stability [3]. Traditional solder materials, prone to interface diffusion and fatigue cracking at high temperatures, fail to meet the reliability and thermal conductivity needs of SiC devices. Sintered copper nanoparticles (Cu NPs), with their high thermal conductivity, melting point, and mechanical properties, offer an ideal solution, forming strong bonding interfaces that enhance thermal management and mechanical reliability, thus advancing high-performance power electronics packaging [4].

Despite the advantages of sintered Cu NPs in die attachment, the sintering process and other attachment technologies typically introduce residual interfacial stresses. These stresses arise from discrepancies in thermal expansion coefficients and internal stresses generated during sintering or cooling. Specifically, residual stresses accelerate the aging of the sintered joint and can lead to interface failure, severely impacting the performance and reliability of SiC power devices [5]. Therefore, controlling residual stresses during the die attachment process is critical for enhancing the performance and lifespan of SiC power devices [6].

2025 IEEE 75th Electronic Components and Technology Conference (ECTC) | 979-8-3315-3932-0/25/$31.00 ©2025 IEEE | DOI: 10.1109/ECTC51687.2025.00126

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DOI 10.1109/ECTC51687.2025.00126

Residual stress significantly impacts the performance and reliability of SiC power devices, and its distribution at the packaging interface is equally important. The spatial distribution of residual stress indicates the quality of the bond between the chip and substrate, particularly highlighting stress concentration areas that can lead to interface failure. By analyzing residual stress distribution, we can assess packaging integrity, predict failure modes, and optimize the attachment process [7]. Therefore, accurately measuring residual stress distribution not only provides insight into packaging quality but also aids in optimizing process parameters to enhance product reliability.

Common methods for detecting residual stress at interfaces include X-ray diffraction (XRD) [8, 9], ultrasonic testing [10], optical analysis [11], and electron backscatter diffraction (EBSD) [12]. XRD measures the displacement of diffraction peaks to infer internal residual stress, making it suitable for non-destructive internal measurements [8, 9]. However, its application is limited in complex multilayer interfaces, particularly in SiC chip packaging, where high hardness and brittleness of SiC affect measurement accuracy. Jiang et al. [10] effectively assessed residual stress in multilayer viscoelastic composites using acoustoelastic effects and electromechanical impedance spectroscopy. However, the high density and hardness of SiC limit ultrasonic wave penetration, reducing the accuracy of this method for internal interface stress analysis. EBSD, as demonstrated by Kartal et al. [12], can calculate multiaxial residual stress in high-temperature alloys, but its application is limited to surface measurements. Analyzing interface stress requires destructive methods, which alter the original internal stresses and introduce new processing stresses. Moreover, EBSD's detection area is limited, resulting in low efficiency. Optical stress analysis methods measure surface displacement or strain through interference effects and reconstruct the stress field using elastic theory [13, 14]. However, these methods overlook material defects between the test surface and target interface, which can affect residual stress at the interface. In conclusion, these techniques face challenges in terms of precision, efficiency, destructiveness, and testing depth when evaluating residual stress in SiC chip packaging.

In contrast, confocal Raman spectroscopy [15, 16], an emerging stress testing method, offers significant advantages. This technique analyzes the frequency shift of Raman scattered light within materials to non-destructively measure residual stress in small regions, providing high-precision information on stress distribution at both surface and sub-surface levels [15]. Its unique spatial resolution allows for the precise measurement of stress distribution at different material interfaces in SiC packaging. This method enables rapid, non-destructive characterization of residual stress at SiC chip interconnect interfaces, offering great industrial application potential.

In this study, pressure-assisted sintering of nano-copper was used to attach SiC chips to an Active Metal Brazing (AMB) substrate. SiC/sintered Nano-Cu Interface Stress was calculated and analyzed based on confocal Raman spectroscopy testing. The distribution characteristics and causes of residual stress at the SiC chip interface were discussed.

II. Pressure-Assisted Nano-Cu Sintering Die-Attach

In this study, HPE NYM-9122DA sintered nano-copper paste developed by Nayu Semiconductor Materials Co., Ltd was used. The schematic diagram of SiC die-attach process with pressure-assisted Nano-Cu sintering is shown in Fig. 1. First, an automatic printing device (EKRA Serio 400 Automatisierungssysteme GmbH) was employed to uniformly apply the nano-copper paste onto the AMB substrate. A custom screen with a thickness of 100 μm was used, and the primary printing parameters included a squeegee pressure of 30 N, printing speed of 30 mm/s, and release speed of 10 mm/s, ensuring uniformity and consistency in the paste layer thickness. Next, the printed samples were dried for 5 minutes in a nitrogen atmosphere at 120°C. Following this, a 5 mm × 5 mm 4H-SiC chip was mounted onto the dried copper paste surface using an automatic pick-and-place device. The samples were then subjected to a pressure-assisted sintering process using Boschman's Sinterstar Auto-F-XL-HC system, sintering for 3 minutes at a temperature of 250°C and a pressure of 20 MPa in a nitrogen atmosphere. Finally, the samples were removed from the sintering equipment and cooled to room temperature on a cooling platform.

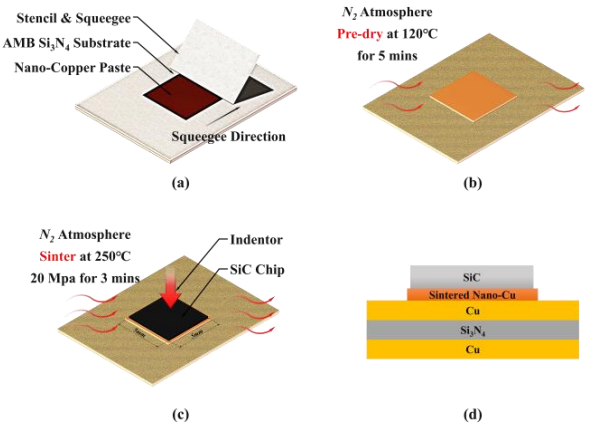

Fig. 1 Schematic diagram of SiC die-attach process with pressure-assisted Nano-Cu sintering

III. Finite Element Simulation

A 3D finite element model of a 4H-SiC die attached on AMB substrate with pressure-assisted Nano Cu sintering was constructed in ANSYS Workbench 2022R2. The geometric structure and contact relationships of the finite element model were set according to actual conditions. By default, there is no layered intimate contact in the packaging structure. The tangential and normal behaviors of the interface contact relationships were set to hard contact based on the penalty

function method. The material parameters assigned to the various layers of the packaging structure are shown in Table I [17]. The mechanical boundary condition consists of applying remote displacement constraints to the bottom surface of the AMB substrate. The thermal boundary condition involves a uniform temperature that linearly decreases from 250°C to 25°C. Based on the mechanical and thermal boundary conditions, thermodynamic simulations were performed to model the residual stress induced by the pressure-assisted sintering process of the SiC chip.

After cooling to room temperature, the surface deformation and the residual stress distribution at the bottom interface of the SiC chips for sample 1 and sample 2 are shown in Fig. 2 and Fig. 3, respectively. The simulation results show that there is warping on the surface of the chip, and the maximum relative warping is 7.483 μm located near the center of the chip. The residual stress distribution at the interface is symmetrically centered around the chip's center, with stress concentrating at the center and radiating outward, decreasing as it moves away from the center. The overall stress is compressive, with the maximum value located near the center of the chip at 139.68 MPa. Both the displacement at the chip's upper surface and the residual stress at the lower surface show an ideal continuous distribution in the simulation results.

TABLE I. MATERIAL PARAMETERS ASSIGNED TO THE VARIOUS LAYERS OF THE PACKAGING STRUCTURE [17].

Components	Materials	K (W/m·°C)	CTE (ppm/°C)	E (GPa)	ν
Chip	SiC	58.6	5.1	400	0.14
Die-attach	Sintered nano-Cu	390.0	17.3	13.2	0.34
AMB Substrate	Si_3N_4	70.0	31.0	49	0.38
	Copper	401.0	18.0	110	0.34

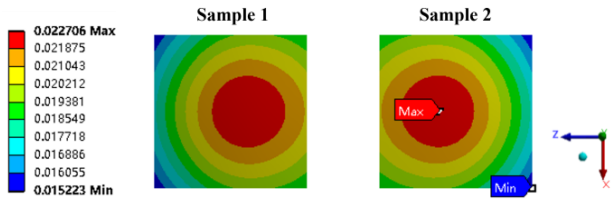

Fig. 2 Displacement distribution contour map at the upper surface of the 4H SiC chips (Sample 1 and Sample 2).

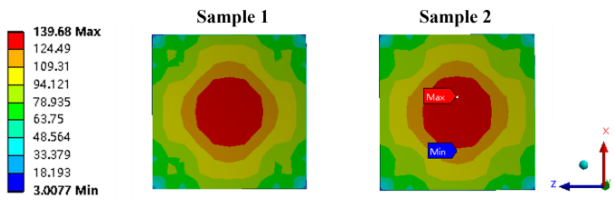

Fig. 3 Residual stress distribution contour map at the bottom surface of the 4H SiC chips (Sample 1 and Sample 2).

IV. WARPAGE MEASUREMENT OF THE SIC CHIP SURFACES

First, the warpage of the SiC chip surfaces for Sample 1 and Sample 2 was measured using the *S neox* system from SENSOFAR, which is based on confocal, interferometric, and multifocus methods. The warpage measurement results are shown in Fig. 4. The results indicate that the warpage is concentrated at the midpoints of the chip edges, while the lowest surface points are located at the chip corners. The maximum relative warpage of the top surfaces of Sample 1 and Sample 2 is 1.606 μm and 2.282 μm, respectively. This observation does not align with the finite element simulation results for the chip surface displacement (Fig. 2), highlighting that thermally induced deformation is not solely caused by the mismatch in the CTE between the material layers. Factors such as the surface morphology of the sintered layer caused by printing, micro-defects within the chip, and micro-cracks in the sintered nano-copper also influence the thermal-induced deformation during the chip sintering process. Additionally, the difference in warpage between sample 1 and sample 2 suggests a certain degree of instability in the sintering process, even under identical conditions.

In summary, the finite element simulation of thermally induced deformation, which only considers the mismatch of thermal expansion coefficients among the layers, is idealized and one-sided compared to real-world conditions. Furthermore, evaluating the residual stress at the chip bonding interface solely through finite element simulation is also partial and inaccurate. A rapid and accurate evaluation of the interface stress in SiC chips requires the use of a testing and computational framework based on confocal Raman spectroscopy.

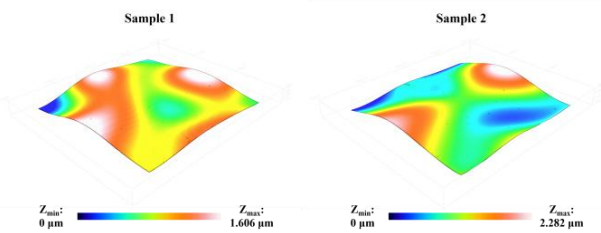

Fig. 4 Warpage measurement results of the SiC chip surfaces of Sample 1 and Sample 2.

V. CONFOCAL RAMAN ASSISTED SIC/SINTERED NANO-CU INTERFACE STRESS CHARACTERIZATION

A. Raman-Stress/Strain Theory

Raman spectroscopy is fundamentally based on the inelastic scattering of monochromatic laser light, where the vibrational and rotational energy levels of a material's molecules interact with incident photons to produce a distinct scattering signal. This signal, often termed a "spectral fingerprint," reflects specific vibrational modes and can be used to analyze a material's chemical composition and structural properties. When an external stress is applied to the material, the resulting lattice deformation alters the interatomic forces, leading to shifts in the Raman peak positions [18]. In particular, the stress-induced change in the frequency of a characteristic

Raman peak can be quantitatively related to the stress state in the crystal coordinate system, as expressed by

$$\omega_j = \omega_0 + \left(\frac{\partial \omega_j}{\partial \sigma_{ij}}\right)_{ij} \Delta\sigma_{ij} + \frac{1}{2}\left(\frac{\partial^2 \omega_j}{\partial \sigma_{ij}\partial \sigma_{kl}}\right)_{ijkl} \Delta\sigma_{ij}\Delta\sigma_{kl} + \cdots \tag{1}$$

where ω_0 is the Raman peak position of the sample in a stress-free state, ω_j is the Raman peak position after the material is subjected to stress, and σ_{ij} represents the stress field of the sample in the crystal coordinate system.

Because the relative shift of the Raman peak under stress is generally small compared to its intrinsic position, linear deformation potential theory is often employed to simplify the relationship between the Raman peak shift and residual stress. For 4H-SiC, which belongs to the P_{6mc} space group, the peak shift of a particular vibrational mode under stress can be further related to the internal strain[19]:

$$\Delta E = a\left(\varepsilon_{xx} + \varepsilon_{yy}\right) + b\varepsilon_{zz} \pm c\sqrt{\left(\varepsilon_{xx} - \varepsilon_{yy}\right)^2 + 4\varepsilon_{xy}^2} \tag{2}$$

where constants a, b, and c are the deformation potential constants corresponding to specific phonon modes of 4H-SiC. In modeling this relationship, we designate the crystal directions [1-100], [11-20], and [0001] as the X, Y, and Z axes, respectively.

According to generalized Hooke's law, the strain in the 4H-SiC crystal under a given stress can be derived as:

$$\begin{pmatrix} \varepsilon_{xx} \\ \varepsilon_{yy} \\ \varepsilon_{zz} \\ 2\varepsilon_{yz} \\ 2\varepsilon_{zx} \\ 2\varepsilon_{xy} \end{pmatrix} = \begin{pmatrix} s_{11} & s_{12} & s_{13} & & & \\ s_{12} & s_{11} & s_{13} & & & \\ s_{13} & s_{13} & s_{33} & & & \\ & & & s_{44} & & \\ & & & & s_{44} & \\ & & & & & s_{66} \end{pmatrix} \begin{pmatrix} \Delta\sigma_{xx} \\ \Delta\sigma_{yy} \\ \Delta\sigma_{zz} \\ \Delta\sigma_{yz} \\ \Delta\sigma_{zx} \\ \Delta\sigma_{xy} \end{pmatrix}$$
$$= \begin{pmatrix} s_{11}\Delta\sigma_{xx} + s_{12}\Delta\sigma_{yy} + s_{13}\Delta\sigma_{zz} \\ s_{12}\Delta\sigma_{xx} + s_{11}\Delta\sigma_{yy} + +s_{13}\Delta\sigma_{zz} \\ s_{13}\left(\Delta\sigma_{xx} + \Delta\sigma_{yy}\right) + +s_{33}\Delta\sigma_{zz} \\ s_{44}\Delta\sigma_{yz} \\ s_{44}\Delta\sigma_{zx} \\ s_{66}\Delta\sigma_{xy} \end{pmatrix} \tag{3}$$

Considering that the tested 4H-SiC chip is a thin square block of 5 mm × 5 mm × 0.2 mm, it can be regarded as being subjected to equibiaxial stress in the plane. Compared with the stress values in the X and Y directions, the stress in the Z direction can be ignored; and the shear stress component plane can also be ignored. Since the stress in the X and Y directions is equal, the corresponding Equation (2) can be further simplified to:

$$\Delta\omega_{E_2} = 2\left[a_{E_2}\left(s_{11} + s_{12}\right) + b_{E_2}s_{13}\right]\Delta\sigma \tag{4}$$

Since the main peak in the standard Raman spectrum of 4H-SiC is E_2(TO), in this experiment, we choose this peak to evaluate the residual stress inside the 4H-SiC chip after mounting to reduce the test error. The specific E_2(TO) Raman peak offset-stress relationship is expressed as:

$$\Delta\sigma\ (\mathrm{MPa}) = -323\Delta\omega_{\mathrm{obs}}\ (\mathrm{cm}^{-1}) \tag{5}$$

B. Interface stress characterization

Fig. 5 shows the Raman measurement setup for a 4H-SiC chip mounted on a sintered copper layer. In these experiments, the backscattering mode was employed to collect Raman signals, with the monochromatic laser beam incident along the [0001] crystal direction (i.e., the Z-axis) of the 4H-SiC. It is important to ensure that the laser beam remains perpendicular to the chip surface. The confocal mode was adopted to capture the stress state at the 4H-SiC/sintered copper interface more accurately during the sintering process. In this mode, the laser focal plane was positioned near the bottom surface of the 4H-SiC chip to maximize the Raman signal originating from the interface region.

To establish a stress-free reference, we measured the E_2(TO) peak position of the unmounted 4H-SiC sample. This reference peak, located at approximately 777 cm^{-1} (Fig. 6), aligns well with values reported in the literature. For clarity, positive stress values are defined as tensile stress and negative as compressive stress. By comparing the mounted chip's measured Raman peak positions to this stress-free reference, it becomes possible to quantify the induced residual stress stemming from the mounting process.

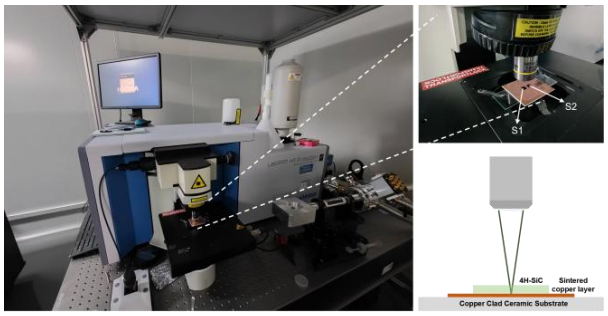

Fig. 5 Confocal Raman test setup for test sample

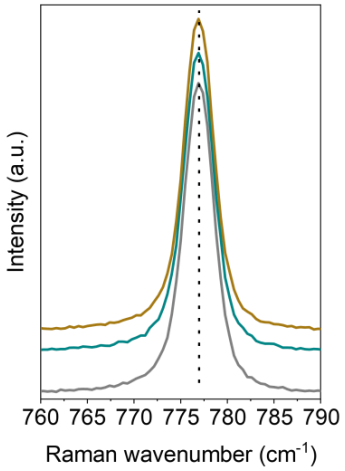

Fig. 6 E_2(TO) Raman peak position of 4H-SiC chip before die-attach.

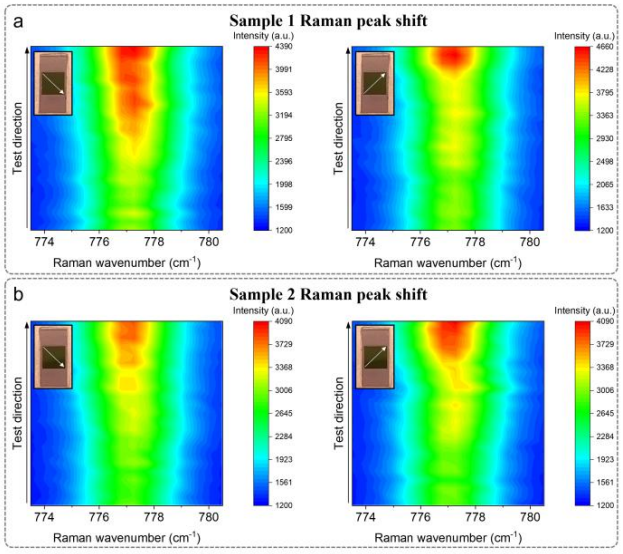

Fig. 7 The E_2(TO) peaks of the two chip samples shift along the diagonal direction. The arrows in the figure indicate the Raman test direction. (a) Sample 1 Raman peak shift. (b) Sample 2 Raman peak shift.

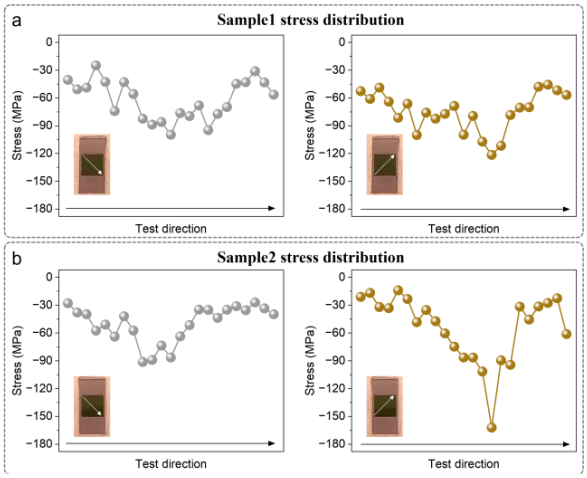

Fig. 8 Stress distribution in the diagonal direction of two samples. (a) Sample 1 stress distribution. (b) Sample 2 stress distribution.

TABLE II. THE E_2(TO) PEAK SHIFTS IN THE DIAGONAL DIRECTION OF THE TWO CHIP SAMPLES.

Sample	***Line Scan***	***Shift range (cm^{-1})***	***Average peak shift (cm^{-1})***
1	Line 1	0.08-0.31	0.19
	Line 2	0.14-0.38	0.23
2	Line 1	0.09-0.28	0.16
	Line 2	0.07-0.50	0.17

To more comprehensively elucidate the spatial distribution and evolution of residual stress at the 4H-SiC/sintered copper interface, linear Raman scans were conducted along both diagonals of the chip. As shown in Fig. 7, the E_2(TO) Raman peak position varies notably with scanning distance, while Table II summarizes the corresponding peak shifts in each diagonal direction. The distinct variations in peak position along these two diagonals reflect significant stress gradients, indicating that the sintering process imposes non-uniform thermomechanical loading on the chip. Furthermore, because multiple samples exhibit similar diagonal-based stress distributions, these stress gradients appear to be intrinsic to the interface rather than sporadic anomalies. From a mechanistic perspective, two key factors can contribute to the development of these stress gradients. First, the thermal expansion mismatch between 4H-SiC and the sintered copper layer drives differential stress accumulation as the assembly cools from the sintering temperature to room temperature. Regions along the diagonals—particularly those adjacent to the chip center—experience greater constraints on expansion or contraction, resulting in higher compressive stress magnitudes. Conversely, the corners and edges of the chip can more readily accommodate deformation, thus showing relatively lower stresses.

Using Equation (5) for stress inversion, the measured Raman shifts were translated into residual stress values, as shown in Fig. 8. Three major observations emerge:

(1) Stress concentration in the chip center. The highest residual stress values are located near the chip center. During the sintering process, this region undergoes the most pronounced effects of thermal expansion and contraction, culminating in a larger buildup of internal stress.

(2) Lower stress near edges and corners. Moving from the center toward the edges and corners, residual stress levels steadily decrease. This trend suggests an outward diffusion or relaxation of stress, driven by thermomechanical coupling effects, and leads to comparatively lower stress magnitudes near the perimeter.

(3) Influence of material mismatch. Substantial interface stress arises due to the markedly different coefficients of thermal expansion and elastic moduli of 4H-SiC and sintered copper. Such stress concentrations can significantly impact thermal management and mechanical reliability in subsequent device applications. Improved sintering processes can help alleviate excessive stress accumulation.

Overall, the linear Raman scan data provide a detailed spatial mapping of the stress state at the 4H-SiC/sintered copper interface. By integrating this non-destructive diagnostic technique with insights into the thermomechanical origins of stress gradients, a robust analytical framework can be established to refine sintering processes and enhance the reliability of 4H-SiC-based devices over the long term.

VI. CONCLUSION

This study presents an evaluation framework for residual stress at the SiC chip packaging interface based on confocal Raman spectroscopy, enabling non-destructive, accurate, and efficient residual stress testing. Additionally, a thermomechanical finite element simulation model for sintered

SiC chip attachment was constructed. The main conclusions are as follows:

(1) The thermally induced deformation and residual stress in the sintered SiC chip packaging are not solely caused by the mismatch in the coefficients of thermal expansion (CTE) between the layers of the packaging materials. Finite element simulations only consider the mismatch in thermal expansion coefficients between the layers, which is idealized and one-sided. Thermomechanical simulations are insufficient for accurately assessing the warpage and residual stress in SiC chips.

(2) After being attached to the AMB substrate using the pressure-assisted sintering process, the SiC chip exhibits a noticeable warpage. The maximum warpage occurs at the mid-point of the chip's edge, while the minimum warpage is observed at the chip's corners. The relative warpage for the top surface of sample 1 and sample 2 is 1.606 μm and 2.282 μm, respectively.

(3) The confocal Raman spectroscopy method enables non-destructive, accurate, and efficient evaluation of the residual stress at the SiC/sintered nano-Cu interface. Raman spectroscopy tests reveal significant compressive residual stress at the bottom interface of the SiC chip. The compressive stress is concentrated at the center of the chip, with the highest residual stress value near the center. Residual stress steadily decreases from the center toward the edges and corners. The linear Raman scan data provides a detailed spatial map of the stress state at the 4H-SiC/sintered copper interface.

ACKNOWLEDGMENT

This research was supported by the National Natural Science Foundation of China (grant number: 52275559).

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