DRIE and Bonding Assisted Low Cost MEMS Processing of In-plane HAR Inertial Sensors

V. Rajaraman, K.A.A. Makinwa and P.J. French

EI Laboratory, DIMES, Dept. of Microelectronics, Faculty EEMCS, Delft University of Technology, Mekelweg 4, 2628 CD Delft, The Netherlands, e-mail: v.rajaraman@tudelft.nl

We present a simple, flexible and low cost MEMS fabrication process, developed using deep reactive ion etching (DRIE) and wafer bonding technologies, for manufacturing in-plane high aspect ratio (HAR) inertial sensors. Among examples, the design and fabrication results of a two axis inertial device are presented. Fabricated device thickness ranged up to 140 µm and a HAR of 28 was obtained. Compared to the existing approaches reported in literature, the salient features of the presented process are: single-sided single-wafer processing using just two lithographic masks, capability to fabricate standalone MEMS as well as CMOS compatible MEMS post-processing via process variations, the use of plasma etching for wafer thinning that facilitates stictionless dry-release of MEMS, and its suitability for batch processing.

1. Introduction

HAR micromachining of silicon enabled by DRIE technology [1] has led to the development of low cost and high performance inertial microsensors for various applications in the automotive, consumer, medical, aerospace and defense systems. By effectively exploiting the vertical dimension, such sensors exhibit better mechanical properties due to the use of single crystal silicon, a thicker proof mass that reduces the mechanical noise and improves the sensitivity, smaller form-factor and a relatively larger output capacitance leading to a higher performance than the surface micromachined devices. This paper presents a simple MEMS process flow that has been used for fabricating various in-plane capacitive HAR inertial sensors such as accelerometers and gyroscopes. Also the design and simulation of a dual axis inertial device is described that is later fabricated using the presented technological approach.

2. Fabrication Process

The MEMS process flow, using two lithographic masks, for fabricating HAR capacitive inertial sensors is illustrated in Fig. 1. Microfabrication was performed on 100mm, 525 µm thick, low resistivity p-type silicon wafer with (100) orientation. At first, an oxide mask is deposited and patterned (Fig. 1a) in order to etch a 5 µm deep cavity (Fig. 1b) that defines the perimeter of the free-standing MEMS parts. The cavity etching can be performed by either wet etching with 25 wt% of TMAH at 85°C or dry etching (RIE). Later a 2 µm thick PECVD

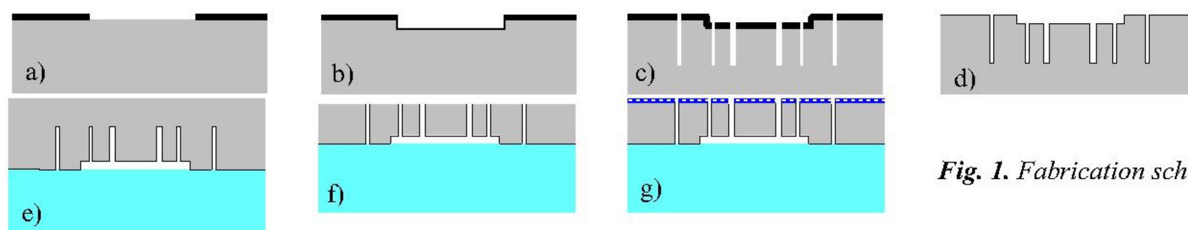

Fig. 1. Fabrication scheme

978-1-4244-2326-2/08/$25.00 ©2008 IEEE

oxide layer is deposited on the cavity region and the microstructure is patterned (Fig. 1c). This is followed by HAR micromachining of silicon using Bosch DRIE process to define the MEMS structure (Fig. 1c). During this step, isolation trenches are also etched around the MEMS structure to electrically isolate the different regions. The residual mask oxide is now removed in BHF (1:7) solution and the microstructures are passivated with an optional layer of 40 nm conformal oxide (Fig. 1d). The patterned device silicon wafer is now bonded face-down to a glass carrier substrate (Fig. 1e). Both, anodic bonding, for standalone MEMS fabrication, and adhesive bonding at low temperature with BCB [2], for CMOS compatible MEMS post-processing, are considered, respectively, aimed at achieving process flexibility. Anodic bonding was performed using a pyrex glass substrate in EV501 bonding equipment at 440°C and 700V. When using BCB bonding non-alkali containing AF45 glass substrate can be used that is CMOS compatible. Later the backside of the bonded silicon device wafer is thinned by timed etching in SF_6 plasma stopping on the oxide lined trench bottom (Fig. 1f). In the next step, the MEMS devices are dry-released without any stiction issue by RIE of trench oxide lining. Finally, a very thin layer of aluminium metal is sputter-coated onto the MEMS device for the electrical bond pads and to reduce the contact resistance of the device.

Table 1. *Bosch DRIE process parameters*

Process Parameters	MEMS Definition (Recipe A)	Silicon Thinning (Recipe B)
SF_6 Etch Gas Flow [sccm]	420	400
C_4F_8 Passivation Gas Flow [sccm]	280	20
SF_6 Etch Gas Step Time [sec]	5	7
C_4F_8 Passivation Gas Step Time [sec]	2	3
Plasma Power [Watts]	1500	2000

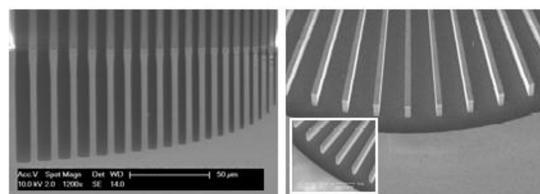

Fig. 2. *HAR microstructures etched with recipe A*

The Bosch DRIE process was performed at room temperature in AMS-100 ICP etch system and the optimized DRIE process parameters are presented in Table 1. Recipe A was used for etching the HAR microstructures, refer Fig. 2. An AR as high as 28 was obtained and the silicon etch rate was 2.7μm/min, the mask selectivity to oxide was 158:1 and the lateral undercut was better than 400 nm. Recipe B was used for thinning the device silicon wafer with an etch rate higher than that of recipe A. The developed process as such allows integration of the inertial MEMS devices with electronics as a two chip system.

2. Design and Simulation of a Dual Axis Inertial Device

A range of capacitive HAR inertial sensors could be fabricated using the abovementioned process. This section briefly describes the design and simulation of an example inertial device that was fabricated in the presented process. The structure of the dual axis inertial sensor is shown in Fig. 3. The device consists of a movable, in both x and y directions, proof mass sus--pended by four crab-leg beams that are anchored to the silicon substrate. Symmetry is preserved in the structure in order to improve the zero stability, linearity and cross-axis sensitivity. This inertial device can be used as a dual axis accelerometer or a gyroscope. When it is used as an accelerometer, an applied external force causes proof mass deflection that is detected as a capacitance change. When using the device as a gyroscope, a two dimensional driving mode

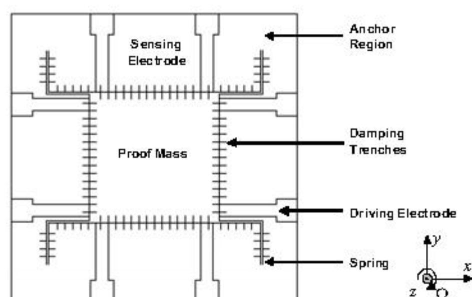

Fig. 3. *Schematic of a dual axis inertial sensor*

employing electrostatic driving and capacitive sensing is applied, described elsewhere [3]. The bulk micromachined inertial device is 140µm thick and the proof mass measuring 600x600μm^2 is suspended by four crab-leg springs, the length and the width of each fold being 200 µm and 3µm, respectively. An equal trench-gap design is used in the design to eliminate the aspect ratio dependent etching of the ICP DRIE process. A large gap is used between the proof mass and the electrodes and damping trenches are included to reduce the damping and achieve sufficient quality factor for device operation in an atmospheric environment. The FEM simulation done using COMSOL in Fig. 4 shows the displacement of the sensor structure due to an applied inertial force. The device parameters of the dual axis inertial device are summarized in table 2.

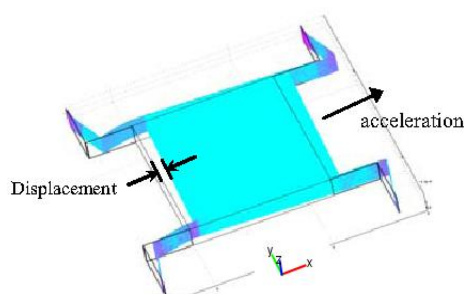

Fig. 4. *FEM simulation showing displacement of the sensor structure due to an inertial force applied in the x-direction*

Table 2. *Dual axis inertial sensor design parameters*

Mass, m	117 µg
Resonance frequency, f_0 *(from FEM)*	6.581 kHz
Electrode gap, d_0	5 µm
Sensitivity, S	6 nm/g; 0.1 fF/g
Damping ratio	56.79 x 10^{-3}
Sense capacitance per side, C_0	110 fF
Thermal noise, a_n	2.7 µg/$\sqrt{Hz}$
Pull-in voltage, V_P	100.02 V
Si Young's modulus (E)	170 GPa

4. Results and Discussion

Inertial devices such as lateral accelerometers and gyroscopes having a capacitive readout and electrostatic actuation, with different structural thicknesses, can be fabricated using the presented process. Fig. 5 presents the DRIE results of microstructures such as comb electrodes and unfolded and folded springs that are often used in inertial sensors. The fabrica-

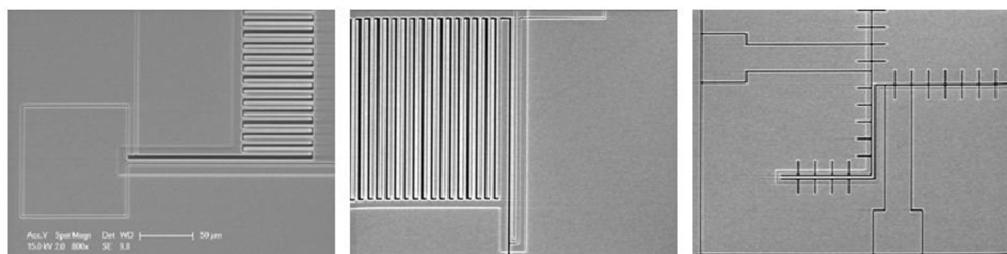

Fig. 5. *Detailed view of the comb electrodes and springs of various inertial sensors*

-tion results of the dual axis inertial device are presented in Fig. 6. The top and cross-sectional views of the DRIE etched HAR device is shown in Figs. 6 a and b. The trench gaps were 5 µm and the etch depth was 140 µm, resulting in an AR of 28. Fig. 6c shows the optical micrograph of an anodic bonded device viewed through the glass carrier substrate. Here, the light region indicates the unbonded area where movable MEMS parts are situated and the dark regions indicate the bonded area, where silicon wafer is bonded to the glass carrier substrate. The dry-released device obtained by stictionless plasma thinning of silicon is shown in Fig. 6d.

Inherent benefits of the process such as: the use of single crystal silicon, absence of release holes often found in SOI devices that results in a higher mass, insulating properties from the glass substrate providing lower parasitic capacitance, etc. aids the performance of inertial sensors. Compared to existing technological approaches, the salient features of the presented

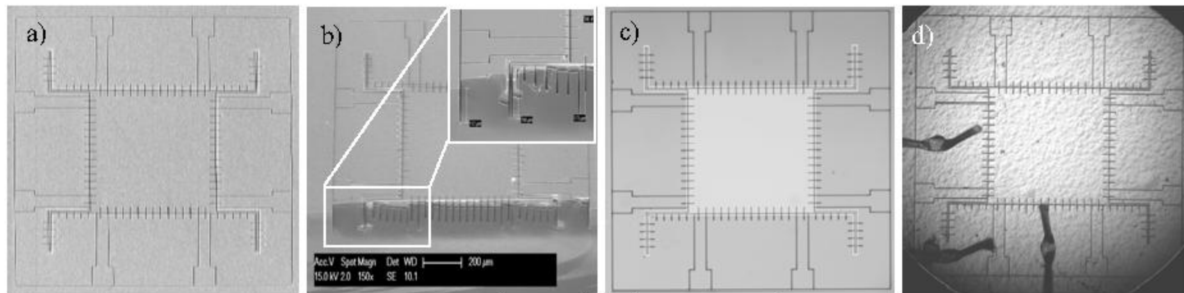

Fig. 6. *Fabricated dual axis inertial sensor*

process are: single-sided single-wafer processing using just two lithographic masks, capability to fabricate standalone MEMS as well as CMOS compatible MEMS post-processing via process variations, its suitability for batch processing, and the use of plasma etching for wafer thinning that facilitates stictionless dry-release of MEMS. Moreover, stictionless dry releasing of MEMS devices reduces the process complexity and improves the yield. Proposed process variations allow standalone MEMS fabrication as well as CMOS compatible MEMS post-processing. Furthermore, the integration of inertial MEMS devices besides CMOS circuitry on a single chip is possible by eliminating the oxide sidewall passivation step, by patterning metal interconnects between the isolated MEMS region and the CMOS circuitry on the glass wafer, and by performing low temperature adhesive wafer bonding with BCB. Similarly, it is also possible to integrate z-axis detection electrodes in the glass wafer for sensors requiring vertical movement detection.

5. Conclusion

A simple, potentially low cost HAR MEMS process flow using DRIE and wafer bonding technology was demonstrated. A wide range of HAR microstructures such as springs, beams, comb electrodes, capacitive structures, suspended structures, etc. that are often used in the design of MEMS inertial sensors can be fabricated in the developed process. Among other examples, the design and fabrication results of a dual axis inertial device were presented. Also other devices requiring HAR micromachining and electrostatic microactuators can potentially be fabricated using the presented process.

Acknowledgement

The authors would like to thank NXP Semiconductors, The Netherlands, for the financial support. Thanks are also due to Mr. G. Craciun for his assistance in this work, Mr. L. Pakula for helpful discussions and the staff of the Delft Institute of Microsystems and Nanoelectronics (DIMES) Technology Centre, TU Delft, for their support during device fabrication.

References

[1] F. Laermer and A. Schilp, Method of Anisotropically Etching Silicon, *U.S. Patent No. 5501893*, 1994.

[2] F. Niklaus, Adhesive Wafer Bonding for Microelectronic and Microelectromechanical Systems, *PhD Thesis*, Royal Institute of Technology, Sweden, 2002.

[3] H. Yang et. al, Two-dimensional Excitation Operation Mode and Phase Detection Scheme for Vibratory Gyroscopes, *J. Micromech. Microeng.*, **12**, pp. 193-197, 2002.