Analog Integrated Circuit and System Design for a Compact, Low-Power Cochlear Implant

Wannaya Ngamkham

Analog Integrated Circuit and System Design for a Compact, Low-Power Cochlear Implant

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Wannaya NGAMKHAM

Master of Electrical Engineering
Mahanakorn University of Technology
geboren te Nong Prue, Chonburi, Thailand

This dissertation has been approved by the

promotor: Prof.dr.ir. W.A. Serdijn
Prof.dr.ir. J.H.M. Frijns

Composition of the doctoral commitee:

Rector Magnificus	Delft University of Technology, chairman
Prof.dr.ir. W.A. Serdijn	Delft University of Technology (EWI), promotor
Prof.dr.ir. J.H.M. Frijns	Leiden University Medical Centre, promotor

Independent membes:

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Prof.dr.ir. P.J. French	Delft University of Technology (EWI)

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To my father Suthep Ngamkham

Summary

Cochlear Implants (CIs) are prosthetic devices that restore hearing in profoundly deaf patients by bypassing the damaged parts of the inner ear and directly stimulating the remaining auditory nerve fibers in the cochlea with electrical pulses. This thesis describs the electronic circuit design of various modules for application in CIs in order to save area, reduce power consumption and ultimately move towards a fully implantable CI.

To enhance the perception of tonal languages (such as Thai and Chinese) and music, an effort to realize the speech processor in a CI that imitates the inner hair cells and the auditory nerve behaviour more precisely should be made. According to recent physiological experiments, the envelope and phase of speech signals are required to enhance the perceptive capability of a CI implanted patient. The design of an analog complex gammatone filter is introduced in order to extract both envelope and phase information of the incoming speech signals as well as to emulate the basilar membrane behavior. A subthreshold $G_m - C$ circuit topology is selected in order to verify the feasibility of the complex gammatone filter at very low power operation.

Several speech encoding strategies like continuous time interleaved sampling (CIS), race-to-spike asynchronous interleaved sampling (AIS), phase-locking zero-crossing detection (PL-ZCD) and phase-locking peak-picking (PL-PP) are studied and compared in order to find a compact analog speech processor that allows for full implantation and is able to convey both time and frequency components of the incoming speech to a set of electrical pulse stimuli. A comparison of the input and reconstructed speech signals in terms of correlation factor and hardware complexity pointed out that a PL-PP strategy provides a compact solution for the CI electronic hardware design since this strategy does not require a high precision envelope detector. A subthreshold

CMOS peak-instant detector to be used in a PL-PP CI processor has been designed. Circuit simulations, using AMIS 0.35 μm technology, show that the proposed detector can be operated from a 1.2 V supply and consumes less than 1 μW static power for detecting a 5 kHz input signal. The output signal of the detector together with the input signal amplitude (the output of the band-pass of each channel) is expected to be used as control parameters in a stimulator for apical cochlear electrodes.

To design stimulators that are implanted inside the body, there are very strict requirements on the size and power consumption. Therefore, it is important to convey as much charge as possible into the tissue while using an as low as possible supply voltage to minimize power consumption. A novel method for maximizing the charge transfer for constant current neural stimulators has been presented. This concept requires a few additional current branches to form two feedback loops to increase the output resistance of a MOS current mirror circuit that requires only one effective drain-source voltage drop. The main benefit we achieve for neural stimulation is the larger amount of charge that can be conveyed to the stimulation electrode. In other words, for the same amount of charge required, the supply voltage can be reduced. Also, a compact programmable biphasic stimulator for cochlear implants has been designed by using the the above concept and implemented in AMS 0.18 μm high-voltage CMOS IC technology, using an active chip area of only 0.042 mm^2. Measurement results show that a proper charge balance of the anodic and cathodic stimulation phases is achieved and a dc blocking capacitor can be omitted. The resulting reduction in the required area enables many stimulation channels on a single die.

As the work laid out in this thesis produced only stand-alone modules, future work should focus on combining all these modules together to form an analog CI processor suitable for a fully implantable cochlear implant.

Samenvatting

Cochleaire Implantaten (CIs) zijn protheses die het gehoor herstellen bij volledig dove patienten door middel van het omzeilen van de beschadigde delen van het binnenoor en de overgebleven gehoorzenuwen in het slakkenhuis direct te stimuleren met elektrische pulsen. Dit proefschrift beschrijft het circuit ontwerp van verschillende modulen welke kunnen worden toegepast in CIs zodat ruimte kan worden bespaard, het vermogensverbruik kan worden gereduceerd en dat er uiteindelijk kan worden gewerkt in de richting van een volledig implanteerbaar CI.

Om de waarneming van tonale talen (zoals Thais en Chinees) en muziek te verbeteren zal er een inspanning moeten worden geleverd om de spraakprocessor, welke verantwoordelijk is voor het imiteren van de binnenste haarcellen en het gedrag van de gehoorzenuw, preciezer te maken. Uit recente fysiologische experimenten blijkt dat de omhullende en fase van spraaksignalen nodig zijn om de spraakverstaanbaarheid van een CI geïmplanteerde patiënt te verbeteren. Het ontwerp van een analoog complexe gammatoon filter is voorgesteld om zowel de omhullende als de faseinformatie uit het binnenkomende spraaksignaal te extraheren en het gedrag van het basilaire membraan te imiteren. Een subthreshold $G_m - C$ circuittopologie is gekozen om de geschiktheid van een complex gammatoon filter welke functioneert op heel erg lage vermogens te onderzoeken.

Verschillende spraakcoderingsalgoritmes zoals “continuous time interleaved sampling (CIS)”, “race-to-spike asynchronous interleaved sampling (AIS)”, “phase-locking zero-crossing detection (PL-ZCD)” en “phase-locking peak-picking (PL-PP)” zijn bestudeerd en vergeleken om tot een compacte analoog spraakprocessor te komen die volledig kan worden geïmplanteerd en tegelijkertijd zowel de tijd- als frequentiecomponenten van het binnenkomende

signaal kan omzetten in een set elektrische stimulatie pulsen. Aan de hand van een vergelijking van de ingangs en de gereconstrueerde spraaksignalen, kijkend naar de correlatiefactor en hardware complexiteit, geeft een PL-PP strategie een compacte oplossing voor het CI elektrische hardwareontwerp omdat deze strategie geen hogeprecisie omhullendedetector nodig heeft. Een subthreshold CMOS peak-instant detector welke kan worden gebruikt in een PL-PP CI processor is ontworpen. Circuitsimulaties in AMIS 0,35 µm technologie laten zien dat voor de voorgestelde detector een 1,2 V voeding kan worden gebruikt en dat deze een statisch vermogensverbruik heeft van minder dan 1 µW voor het detecteren van een 5 kHz ingangssignaal. Het uitgangssignaal van de detector, samen met de amplitude van het ingangssignaal (de uitgang van het banddoorlaatfilter van elk kanaal) kunnen worden gebruikt als aanstuurparameters in een stimulator voor apicale cochleaire elektroden.

Stimulatoren die ontworpen zijn voor implantatie in het lichaam moeten aan hele strenge eisen voldoen op het gebied van afmetingen en vermogensverbruik. Daarom is het belangrijk om zo veel mogelijk lading in het weefsel te brengen terwijl er zo min mogelijk voedingsspanning wordt gebruikt zodat het vermogens verbruik zo laag mogelijk wordt gehouden. Een nieuw uitgevonden methode om de ladingsoverdracht van constantestroom stimulatoren te maximaliseren is gepresenteerd. Dit concept maakt gebruik van een aantal extra aftakkingen voor het vormen van twee stroomterugkoppelingen zodat de uitgangsweerstand van de MOS stroomspiegel wordt verhoogd en slechts een effectieve drain-source spanningsval heeft. Het grootste voordeel dat we hiermee bereiken is de grotere hoeveelheid lading die naar de stimulatieelektrode kan worden gebracht. In andere woorden, voor dezelfde hoeveelheid lading die nodig is kan een lagere voedingsspanning worden gebruikt. Aan de hand van bovenstaand concept is er een compacte programmeerbare bifasische stimulator voor cochleaire implantaten ontworpen. Deze is geïmplementeerd in AMS 0,18 µm hoogspannings CMOS IC technologie en gebruikt een actief chip oppervlak van slechts $0,042$ mm^2. Meetresultaten laten een juiste ladingsbalancering van de anodische en kathodische stimulatiefasen zien waardoor een DC blokkeercapaciteit kan worden weggelaten. De resulterende reductie in de benodigde oppervlakte maakt het mogelijk om vele kanalen op een enkele chip te plaatsen.

Omdat het werk in dit proefschrift alleen uit losse modules bestaat, zou

toekomstig onderzoek moeten worden gericht op het combineren van al deze modules om een CI processor te formeren die geschikt is om toe te passen in een compleet implanteerbaar cochleair implantaat.

Contents

Chapter 1

Introduction

1.1 Motivation

Cochlear implants (CIs) are commonly accepted as therapeutic devices for clinical use and have restored hearing to more than 320,000 profoundly deaf people all around the world by the middle of 2013 [1]. CI users can participate in normal conversation and other situations where the sound environment is relatively clean. However their hearing performance drops dramatically in complex sound environments, causing poor appreciation of music and inability to converse in crowded rooms [2]. One of the major remaining problems with CIs is an individual difference of outcomes. Many users achieve a good score in hearing ability, while other users obtain little benefit [3, 4]. There is much in the world of electrical hearing that is not yet well understood. New research directions in the field of CI implantation are increasingly diverse and interdisciplinary in order to solve the perceptional limitation which may be because of the design of the hardware, the interface, the electrode, the method to convey the sound information into the brain or the brain itself.

Conventional CIs rely on an external unit comprising a microphone and sound processor to pick up and encode sound. For programmability, cochlear implant processing is done mostly in the digital domain by digitizing the output of a microphone front-end and feeding it to a digital signal processor (DSP) as is shown in Fig. 1.1a. Although digital technology in the external sound processor has the advantage of being more flexible to modifications through software, the power consumed by the microphone front-end, analog

to digital converter (ADC), and DSP are high, approximately 5 mW. Additionally, the power consumption used for stimulation can range from 1 mW to 10 mW, depending on the electrode-tissue impedance and the stimulation strategy [5, 6]. This results in the need of a big battery. The power consumption is always a key issue as it is directly related to the size of the CI battery and thereby to the overall size of the CI itself. It would be very convenient for a CI user if the device could be made completely invisible. There are some interesting reasons motivating the need for the development of CIs towards a fully implantable device as the next generation CIs.

The first reason is that a conventional CI creates inconvenience during activities in the CI user's daily life. Users gave their opinion about the external part, worn behind the ear [7–10]. It is big and looks not nice thereby affecting their self-confidence. The external part needs to be turned off or removed while sleeping or engaging in rough sports, etc. In these situations, the CI user is not able to hear anything. Moreover, having every part of the device implanted in the body, it becomes significantly easier to use for children. Second, having the microphone implanted in the ear canal may help improving perception as the CI user can make use of the directional "amplification" provided by the external pinna, while also reducing noise from wind, an effect observed from "in-the-canal" hearing aids. In addition, the data rate limitation between the implanted part and the external processor can be solved. The higher temporal resolution can be used without compromising the number of active channels. The positive result on CI performance is not proven clinically, it is inferred from vocoder simulations and experiments with auditory chimerae [11–13].

A fully implantable CI is still in the research phase and it needs more investigation [14–20]. The development of an implantable microphone, rechargeable battery and low-power sound processor is still a challenge. The microphone must be space efficient, low noise and have sufficient sensitivity. It is either implanted underneath the skin in the ear canal so that the user can benefit from directional cues or attached to the middle ear so that sound signals can be captured from the vibration of the tympanic membrane or the ossicles (the three tiny bones in the middle ear). The rechargeable battery must be small, safe and have a long life. The sound processor and stimulator must be efficient to minimize power consumption and at least small enough for implantation with conventional surgery.

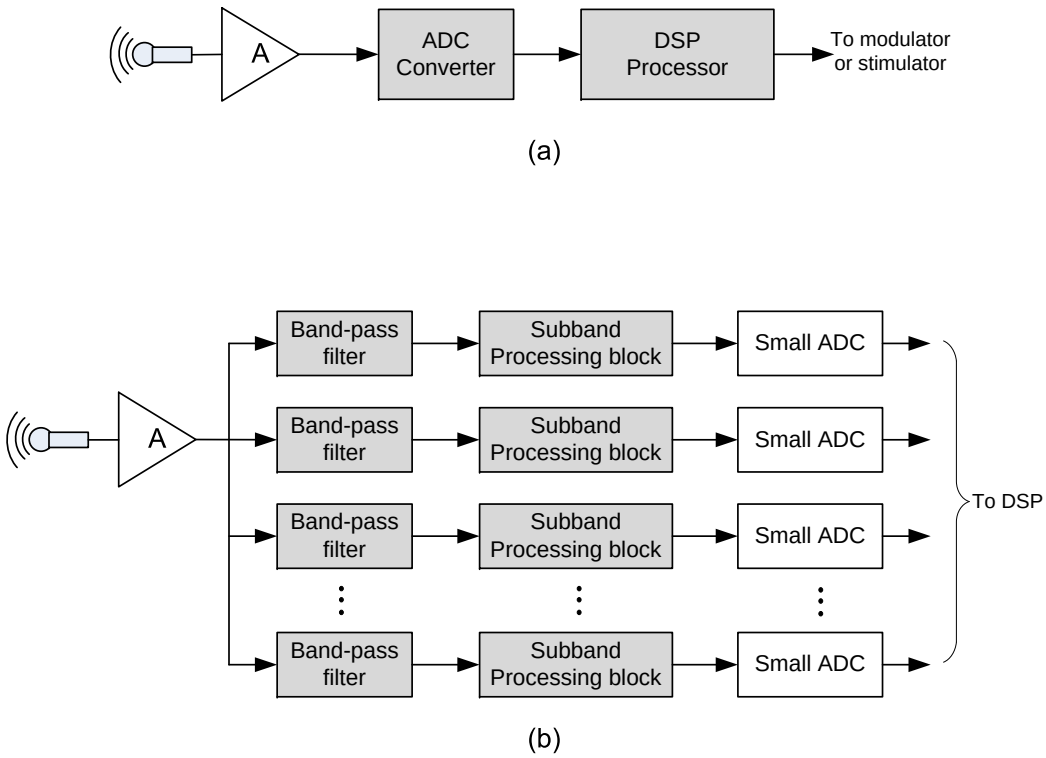

Figure 1.1: (a) Audio front-end architecture consisting of an ADC converter and DSP processor (b) Audio front-end architecture consisting of an array of bandpass filters, subband signal processing and small ADCs.

Technology allows more miniaturization than ever before; advancements in microelectronics/MEMS and battery technology allow for smaller device size and longer lifetime; computer architecture innovations allow for smarter system-level design. With the help of these advances it is feasible to improve the cochlear implant in terms of reliability, power consumption, sound perception, convenience and reduced visibility of external parts.

1.2 Challenges of cochlear implants from an electronic design perspective

For cochlear implants, power consumption is always a key issue as it is directly related to the size of the CI battery and thereby to the overall size of the CI itself. Apart from battery size, also the number of external (non-integrated) components is a major concern, as they contribute to the size of the CI and affect its reliability. For fully implantable CIs, even the size of the chip can become a limiting factor, something which is not often the case in the field of integrated circuit design. In this thesis, power consumption and size of the (integrated) electronic circuitry and speech processing performance are the major design aspects addressed.

For a fully implantable CI, placing an analog signal processing block immediately after the audio sensor gives an advantage in power saving. For instance, analog circuitry can be used for frequency decomposition. More signal processing, envelope, peak, and zero-crossing detection etc., could be performed with analog circuits on the subband signals before they are recombined or sent through individual, smaller ADCs, as is illustrated in Fig. 1.1b. Consequently, the overall system can have a smaller digital processing block than was previously required (Fig. 1.1a) [21].

1.3 Objective and scope of the thesis

This thesis aims to develop an improved cochlear implant to become fully implanted, area efficient and consuming the least amount of power. The low-power electronic circuit design of various CI modules and the selection of an appropriate speech coding strategy required for a fully implantable cochlear implant will be introduced. The two major contributions of this thesis will be described in the following subsections.

1.3.1 Ultra low-power analog speech processor design

- To convey both envelope and fine structure (phase) to the stimulator circuit, thereby enhancing the perception of tonal languages, i.e.,

Thai and Chinese, and music, we follow a design methodology that is both bio-mimetic and employs extremely compact low-power circuits for realizing the analog CI speech processor. A continuous-time filter structure that simultaneously imitates the basilar membrane behaviour (providing a gammatone impulse response) and extracts envelope and phase information from the incoming speech signals have been developed [22]. This filter structure is called complex gammatone filter, which can be realized by a network of subthreshold transistors and capacitors which requires a very low power consumption (a few micro-watts per channel).

- A comparison of speech processing strategies for the design of an ultra low-power analog CI has been presented [23]. A comparison of the input and reconstructed signals in terms of correlation factor and hardware complexity pointed out that a phase-locking peak-picking strategy (PL-PP) provides a compact solution for the CI electronic hardware design since this strategy does not require a high precision envelope detector.

- The design of a subthreshold CMOS peak-instant detector (PID) to be used in the analog CI speech processor has been introduced [24]. The detector is formed by a nano-power sample and hold amplifier (SHA) and a voltage comparator to perform the detection of occurrences of maximum and minimum values of the input. The proposed detector can be operated from a 1.2 V supply and consumes less than 1 μW static power for detecting a 5 kHz input signal (viz., the maximum frequency of the processor). This PID extracts amplitudes at the relevant moments that the peaks occur which is equivalent to the amplitude extracted by conducting a Hilbert transformation but in this case a power consumption of less than 1 micro-watt per channel is obtained. The output signals (amplitude and time) of the PID will be used as control parameters in the stimulator.

1.3.2 Stimulator design

- A novel circuit technique for the stimulator that requires less supply voltage and maintains precise stimulation current in a biphasic scheme by using a double-loop feedback topology has been proposed [25]. The circuit has a higher power efficiency than commonly used stimulator

circuits due to a lower voltage drop accross the current generation transistor.

- A compact biphasic programmable stimulator chip for cochlear implants has been presented [26]. The proposed circuit has been implemented in AMS 0.18 μm high-voltage CMOS technology. Its active chip area is very small, only 0.04 mm^2 [27]. The charge mismatch was found to be well below the safety limits.

1.4 Thesis outline

The remainder of this thesis is organized as follows:

Chapter 2 explains the auditory system, a brief history and a system overview of cochlear implants. Additionally, the signal processing in cochlear implants is also described. Four types of speech processing strategies are compared and evaluated in order to find an appropriate strategy for a fully implantable cochlear implant.

Chapter 3 presents the design and circuit simulation of an analog complex gammatone filter using CMOS transistors operating in their subthreshold region. It will be shown that a continuous-time complex filter can be implemented by employing a state space orthonormal ladder structure and a subthreshold $G_m - C$ circuit topology.

Chapter 4 presents an ultra low-power, robust, compact, discrete-time peak-instant detector (PID) for application in an analog cochlear implant speech processor. A design methodology based on a subthreshold sample and hold circuit and a comparator is used to obtain a peak-instant detector having a very low power consumption and compact hardware implementation.

Chapter 5 shows the design of a compact programmable biphasic stimulator for cochlear implants. By using a double-loop negative feedback topology, a single power supply and a switch array the circuit requires less supply voltage and maintains precise charge balance in a biphasic scheme. The output current is set by scaling a reference current using a two-stage binary-weighted transistor DAC configuration (3 bits high-voltage transistor DAC

and 4 bits low-voltage transistor DAC). By employing two stages the speed of the stimulation pulses is improved and the area of the circuit can be minimized. The measurement results are also reported.

Chapter 6 summarizes the thesis and discusses the possibilities for future work.

Chapter 2

Background information and signal processing strategies for cochlear implants

This chapter begins with describing the human peripheral auditory system in Section 2.1, followed by the explanation of hearing loss in Section 2.2. Section 2.3 gives a brief history of cochlear implants (CIs). A cochlear implant system overview will be described in Section 2.4. In order to find a compact analog sound processor that allows for full implantation and is able to convey both time and frequency components of the incoming sound to a set of electrical pulse stimuli, signal processing strategies will be considered and discussed in Section 2.5. Then, four types of speech encoding strategies are studied, compared and evaluated in Section 2.6 and 2.7, respectively. Finally, Section 2.8 summarizes this chapter.

2.1 The peripheral auditory system

In order to perceive sound, the auditory system must complete three tasks. First, it must deliver acoustic signals to the middle ear; second, it must convert the acoustic signals from pressure changes into electrical signals; and third, it must transmit these electrical signals to the auditory nerve and then to the brain where the electrical signals are converted into a meaningful perception.

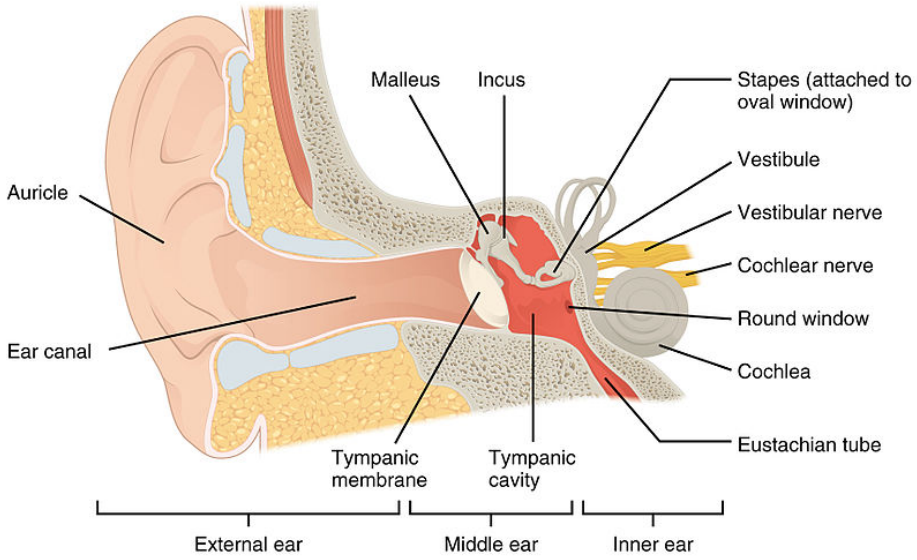

Figure 2.1: The structure of the ear (reproduced with permission from OpenStax College, Anatomy & Physiology, © Jan 5, 2015).

In normal hearing, the human ear can be divided into three components, the outer ear, the middle ear and the inner ear as shown in Fig. 2.1 [28]. The outer ear consists of the visible part of the ear or auricle, the ear canal (the external auditory canal) and the tympanic membrane or eardrum. It is responsible for gathering sound waves and guiding them to the eardrum. The middle ear is an air-filled chamber containing three interlocking small bones called ossicles (malleus, incus and stapes). The function of the middle ear is to transmit the vibrations caused by sound stimulation at the tympanic membrane to the inner ear. The ossicles act as amplitude control and impedance matching between the external ear and the inner ear. They also prevent damage to the inner ear caused by very loud sounds. The inner ear is fluid-filled and contains the cochlea where the auditory perception is located together with the vestibular organ, which is responsible for keeping the body balanced.

Sound waves are gathering into the ear canal by the auricle and consequently hitting the tympanic membrane causing it to vibrate. These vibrations are guided from the tympanic membrane to the cochlea by the malleus, incus and stapes. The stapes is attached to the oval window which is located at

the base of the cochlea.

The cochlea has a spiral shape similar to the shell of a snail. It is approximately 30 mm long from the base (where the oval window and the round window are located) to the apex (the top the spiral) and 2 mm diameter. In the cochlea, there are three chambers: the scala vestibuli which joints the oval window, the scala tympani which ends the round window and the scala media (cochlear duct) as shown in Fig. 2.2. Inside the cochlear duct, the organ of Corti is located. The organ of Corti contains hair cells, and is located on top of the basilar membrane and covered by the tectorial membrane.

The movement of the stapes in response to sound pushes the oval window in and out. This action causes the fluid in the scala vestibuli and the scala tympani to vibrate. The fluid vibration in the scala vestibuli and the scala tympani brings the basilar membrane into motion. The motion is described as a travelling wave. The maximum amplitude of the travelling wave that occurs at each position on the basilar membrane depends on the frequency of the sound. High-frequency sounds cause greatest amplitude of the travelling wave near the base of the membrane, and low frequencies cause greatest amplitude of the travelling wave near the apex. This means the basilar membrane acts like a series of band-pass filter. Each point on the membrane responds to the sound at a different centre frequency. Fig. 2.3 shows the tonotopic mapping of the basilar membrane.

The organ of Corti contains up to 5 rows of outer hair cells which run along the basilar membrane. The row closest to the center of the cochlea consists of the inner hair cells. They transform mechanical energy into electrical signals. When the basilar membrane vibrates, the inner hair cells located at the position where the travelling wave occurs respond. The hair bundle of the inner hair cells bends. This results in patterns of electrical impulses which are sent to the cochlear nerve [30]. The information coming from the cochlear nerve is integrated by the central auditory nervous system and relayed to the brain to translate it into the meaning of sound.

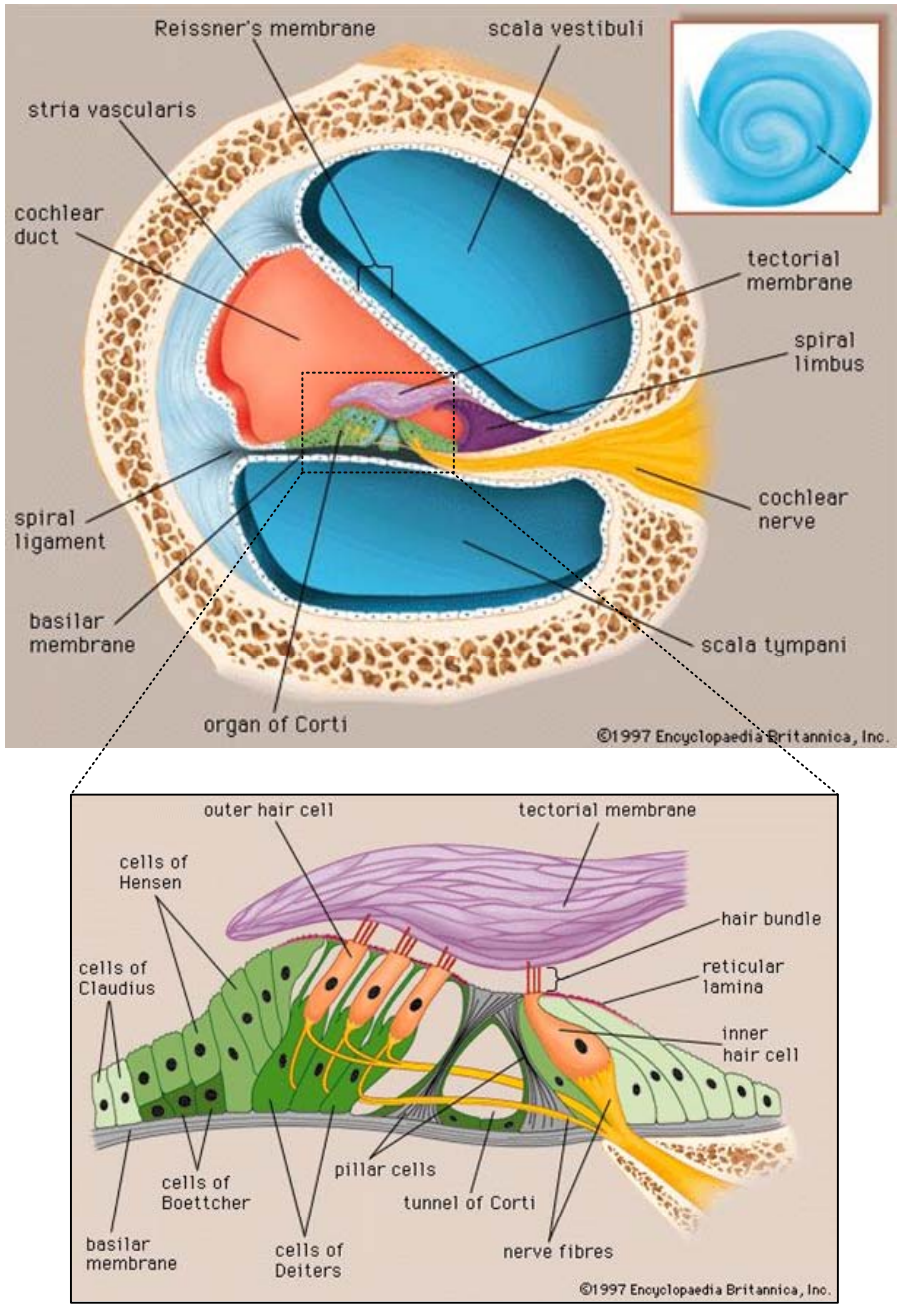

Figure 2.2: Crossection of the cochlea (By courtesy of Encyclopaedia Britannica, Inc., copyright 1997; used with permission).

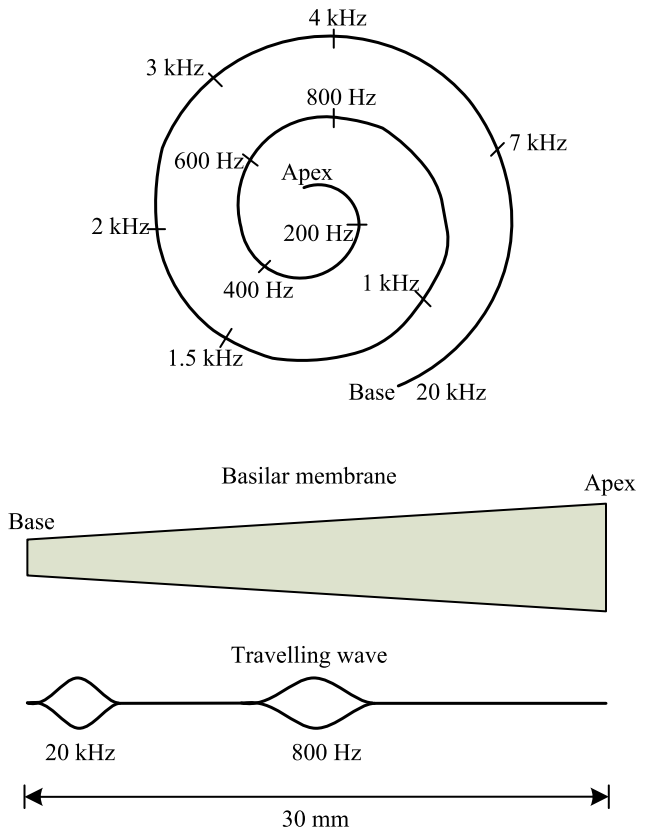

Figure 2.3: Tonotopic mapping of the basilar membrane [29].

2.2 Hearing loss

In normal hearing, humans can comfortably detect sounds in a wide range of sound pressure levels (from 0 to 100 decibel (dB SPL)). A person who cannot detect sounds up till 70 dB SPL is considered to have severe-to-profound hearing loss. The common cause of such a profound hearing loss is damage to or complete destruction of the hair cells. There is no pathway to generate and transmit electrical signals to the auditory nerve. The hair cells can be damaged by certain diseases (e.g., rubella, meningitis, Meniere's disease), aging, congenital disorders, prolonged exposure to loud sound or drugs like streptomycin [30–32]. The deafness due to damaged hair cells, as long as the auditory nerve is still present, can be treated by cochlear implants.

2.3 A brief history of cochlear implants

A cochlear implant is an electronic medical device that bypasses the damaged parts of the inner ear and directly stimulates the remaining auditory nerve in the cochlea with electrical signals. The journey of cochlear implants started when Alessandor Volta (1745-1872), an Italian physicist, inserted the metal rods of a 50 V battery into his own ear. He received a shock in his head and after some moments he heard a bubbling or crackling sound. He did not repeat this experiment because he believed it might be dangerous due to the shock in his brain [33]. This was the first report of using electrical signals to stimulate the auditory nerve. In 1880, Alexander Graham Bell founded the Volta laboratory. He used his profits from the laboratory for research that relates to deafness. Research laboratories of the Bell Telephone System conducted early research in hearing and speech that forms the theoretical foundation needed for the later success of the cochlear implant [34,35].

In 1957, Djourono and Eyries reported successful hearing using electric stimulation [36–38]. They used a wire to directly stimulate the auditory nerve of a deaf patient with an electrical current. The patient showed improved lip-reading capabilities. This observation gave an impulse to the search for a treatment of profound deafness. In 1961, House, Urban and Doyle implanted a gold electrode insulated with silicon rubber in the scala tympani of two deaf patients for nearly three weeks. Both patients reported useful hearing

with electric stimulation. They described that loudness changed with the level of stimulation and the pitch changed with variation in the rate of stimulation [39]. In 1964, Blair Simmons at Stanford Medical School placed a six stainless-steel electrode array through the vestibule and directly into the modiolus in a profoundly deaf patient. The patient showed an ability to discriminate a pitch at a different stimulation position and rate [40]. In 1978, Graeme Clark in Australia implanted a 20-electrode array in two deaf patients. Other similar experimental efforts included Chouard in France [41], Eddington in Utah [42], and Hochmair in Austria [43].

In 1972, the first single-channel electrode array was introduced by House and 3M. By 1975, 13 patients in the United States had functioning, single-channel CIs. The National Institutes of Health (NIH)-funded study on these patients reported that the patients were able to hear some environmental sounds and gained some improvements in lipreading scores, but were unable to understand speech [44].

In 1980, systems using multiple channels and multiple stimulation sites in the cochlea were developed and these systems supported significantly higher levels of speech reception than the single-channel device. Since that time, research has been dedicated to improve the design of the implant system [35, 39, 45].

In 1984, the Food and Drug Administration (FDA) in United States approved the cochlear implant for adults.

Currently there are three major cochlear implant manufacturers including Advanced Bionics Corporation, USA, Med-El Corporation, Austria and Cochlear Corporation, Australia [35].

2.4 Cochlear implant system overview

There are two types of cochlear implants, a modern commercial cochlear implant and a totally implantable cochear implant. A modern commercial cochlear implant system consists of two main components as shown in Fig. 2.4 [46]: the external component, which is worn on the outer ear, and the internal component, the implant, which delivers stimuli to the hearing nerve.

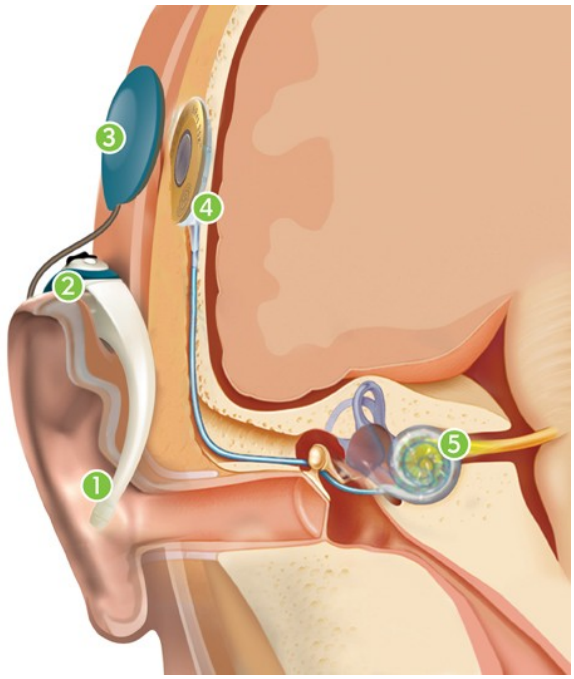

Figure 2.4: A modern comercial cochlear implant system (Picture courtesy of Advanced Bionics).

Cochlear implants bypass the damaged part of the ear; sound is captured by a microphone (1) and offered to the sound processor (2). The sound processor converts the captured sound into detailed digital information. The magnetic headpiece (3) transmits the digital signals to the internal implant under the skin. The implant (4) turns the received digital information into electrical information that travels down the electrode array (5) to the auditory nerve. The auditory nerve sends impulses to the brain, where they are interpreted as sound. A typically modern cochlear implant system has the functional blocks as shown in Fig. 2.5. An external unit, also known as the sound processor consists of a digital signal processing (DSP) unit, a power amplifier and an RF transmitter for the transmission of power and stimulus information through the skin. The internal unit consists of a RF receiver to demodulate and reconstruct the digital signal consisting of encoded sound data. Then, the microcontroller decodes the sound data and offers this to the stimulator. The stimulator applies stimuli to the electrode arrays. The readout system reads out the neural response.

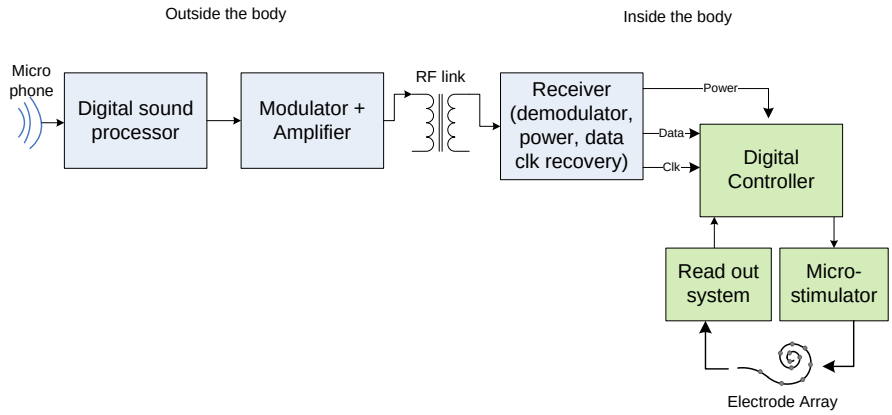

Figure 2.5: Functional block diagram of a modern commercial cochlear implant system

Another type of implant, which is still in the research phase, is a totally implantable cochlear implant, as shown in Fig. 2.6. In this type, everything is embeded inside the body and the RF coil is used only when an external control and battery charging system is needed. Fig. 2.7. shows the functional block diagram of a totally implantable cochlear implant. In order to pick up sound, a microphone is anchored within the auditory canal [19] or an accelerometer is attached to the middle ear bone structure to convert bone vibration into an electrical signal representing the original acoustic information, thus acting as a microphone [47]. A sound processor of this type can be implemented by using analog or digital methods which consume as little power as possible.

2.5 Signal processing in cochlear implants

A sound processor plays an important role in the development of different techniques for deriving electrical stimuli from the sound signal. In multichannel stimulation this goal has been achieved by the invention of a speech processing strategy called 'Continuous Interleaved Sampling, (CIS)' [48] which roughly emulates the behavior of the basilar membrane and inner and outer hair cells, and successfully prevents simultaneous interactions between electrodes using fixed-rate interleaved amplitude-modulated stimuli. CIS has been employed as a default processor in several commercially available CI

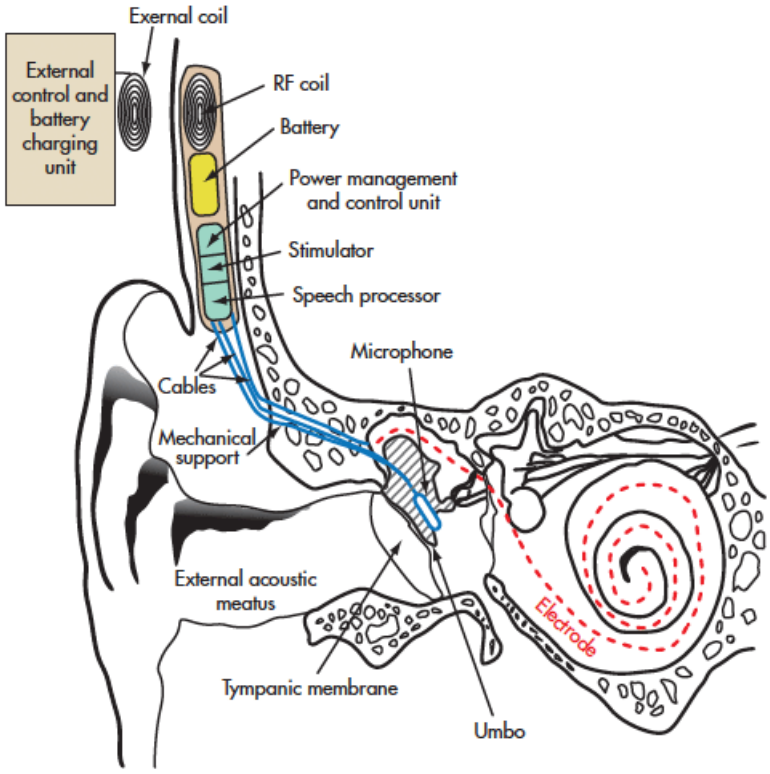

Figure 2.6: A totally implantable cochlear implant system (Reproduced with permission from University of Utah, Case Western Reserve University).

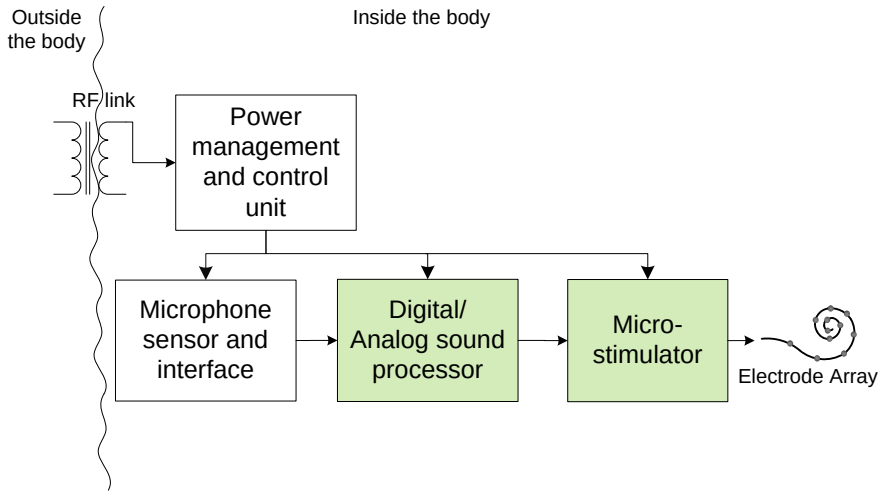

Figure 2.7: Functional block diagram of a totally implantable cochlear implant system.

devices produced by different manufacturers, i.e., MED-EL GmbH, Cochlear Ltd., Advanced Bionics Corp., and the results obtained from clinical experiments have shown to offer reliable understanding of sentences in quiet environments but poor results are obtained for simple melodies. In typical noisy environments, the patients (CI recipients) are still having difficulties to understand both sentences and melodies [49].

These indications imply that the temporal fine structure (TFS, fast varying components of the sound) is not being conveyed to the brain. To gain the perception of tonal languages and music, an effort of realizing a speech processing strategy that imitates the inner hair cells and the auditory nerve behavior more precisely should be considered. For this reason, the 'Hilbert Transform, (HT)' has been introduced in the CI processor, to extract the temporal envelope, instantaneous frequency and phase, and thereby several strategies that convey the TFS have been introduced [50].

Fig. 2.8 shows a general block diagram that can be used to describe all strategies that are considered in this chapter. The processor comprises three layers of operation. At Layer-1, indicated by the white background boxes, the incoming sound is pre-emphasized by either (linearly/non-linearly) am-

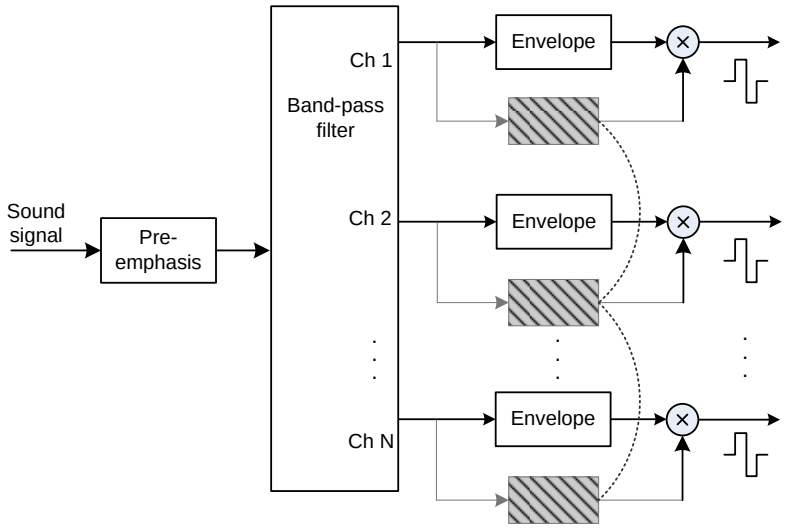

Figure 2.8: General block diagram for envelope-based speech processing.

plifying or filtering or both before entering the bank of band-pass filters (BPFs). This mechanism is adapted from the role of the outer hair cells that map the wide range of the incoming sound pressure onto the limited dynamic range of the ear. The BPF bank roughly mimics the basilar membrane behavior by decomposing the signal into a limited number (N) of frequency bands (channels). The signal strength of each channel will be extracted in the form of the temporal envelope (which roughly emulates the role of the inner hair cell) and then modulated with the generated pulse trains to further stimulate the nerve fibers. These are common for all envelope-based processors.

The study in [51] shows that spiking patterns depend somewhat on input frequency so that Layer-2 (indicated by the gray boxes) is introduced. Particular features (frequency, phase, TFS) of the output waveform of each channel will be detected and combined with the envelope to define the suitable stimulation pulse features. At this layer, the pulses generated from each channel are independent from each other and the stochastic spiking behavior of the auditory nerve is ignored. Layer-3 (represented by the dotted lines) is therefore added to include this phenomenon by somehow conditioning the features detected from different channels to create a stimulation pat-

tern that avoids electrode interaction and preserves the relevant extracted features. Note that the attempt to convey all the features of the incoming signal to the stimulation electrode is based on the assumption that the brain can interpret this information, but in practice there are factors that deviate from what really happens along the auditory pathway. So the number of layers (system complexity) does not guarantee the quality of perception in real patients [52] but serves only as a first order estimation.

This thesis aims to design a totally implantable CI by using an analog sound processor. We thus explore some processing strategies that do not require the computationally intensive and power exhausting HT. We try to optimally balance the quality of the sound that can be conveyed via a set of pulse trains to the stimulation electrodes and reduce the hardware complexity of the processors. The study covers widely recognized continuous time interleaved sampling (CIS) and strategies to convey the temporal fine structure (TFS), including race-to-spike asynchronous interleaved sampling (AIS), phase-locking (PL) using zero-crossing detection (ZCD), and PL using a peak-picking (PP) technique. To estimate the performances of the four systems, a spike-based reconstruction algorithm is employed to retrieve the original sounds after being processed by different strategies. The correlation factors between the reconstructed and original signals imply that strategies conveying TFS outperform CIS. Among them, the peak picking technique combines good performance with great compactness since envelope detectors are not required. The details will be described in the next section.

2.6 Review and comparison of the existing speech processing strategies

2.6.1 Continuous Interleaved Sampling (CIS)

From the default setting of several CI models [53], it can be said that CIS is the most successful strategy. Fig. 2.9 shows the block diagram of the CIS strategy. CIS uses only the 1^{st} layer of operation. The temporal envelope from each band is extracted by either half-wave or full-wave rectification followed by a low-pass filter. The envelope is then logarithmically compressed to match the widely varying acoustic amplitudes to the narrow electric dynamic range. The compressed envelope amplitude modulates a fixed rate biphasic carrier, whose rate can vary from several hundreds to several thou-

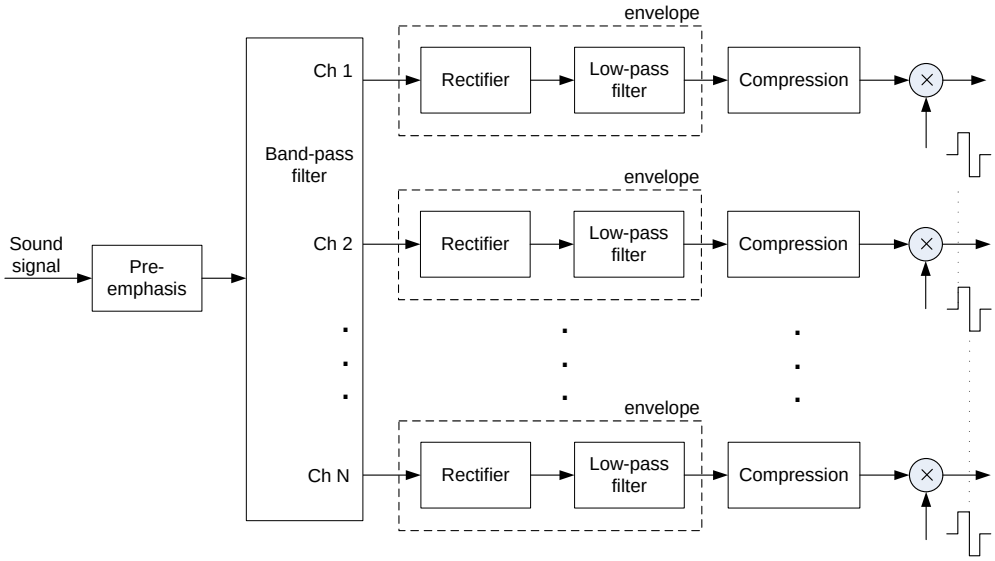

Figure 2.9: Block diagram of the continuous interleaved sampling (CIS) strategy.

sands per second. To avoid simultaneous electrical field interference the biphasic carriers are time interleaved between the bands so that no simultaneous stimulation occurs between the bands at any time [35].

There is some evidence that quality of speech perception obtained from a CIS processor strongly depends on the precision of the extracted envelopes [50, 54]. Accordingly, an attempt to replace the simple envelope detector (ED) comprising a rectifier and a low-pass filter (LPF) by a HT based ED is of interest. This issue needs to be carefully considered for an analog processor since in order to perform the HT, a high complexity of constituting electronic circuitry is unavoidable [22]. Fig. 2.10(a) shows a fraction of the speech signal from the word 'die' after 4^{th}-order Butterworth BP filtering with a center frequency of 150 Hz. The envelopes are extracted by a simple ED with 200 Hz LPF cutoff frequency (the dashed line of Figs. 2.10(b)-(c) and (e)) and by the HT-ED (the dotted line of Figs. 2.10(b)-(e)). The positive pulse train generated within the CIS processor is represented by the solid line in Fig. 2.10(b). In this case, we can clearly see that the accuracy of the amplitude of the pulses highly depends on the accuracy of the ED. Also, it is hardly possible that the brain can recognize frequency,

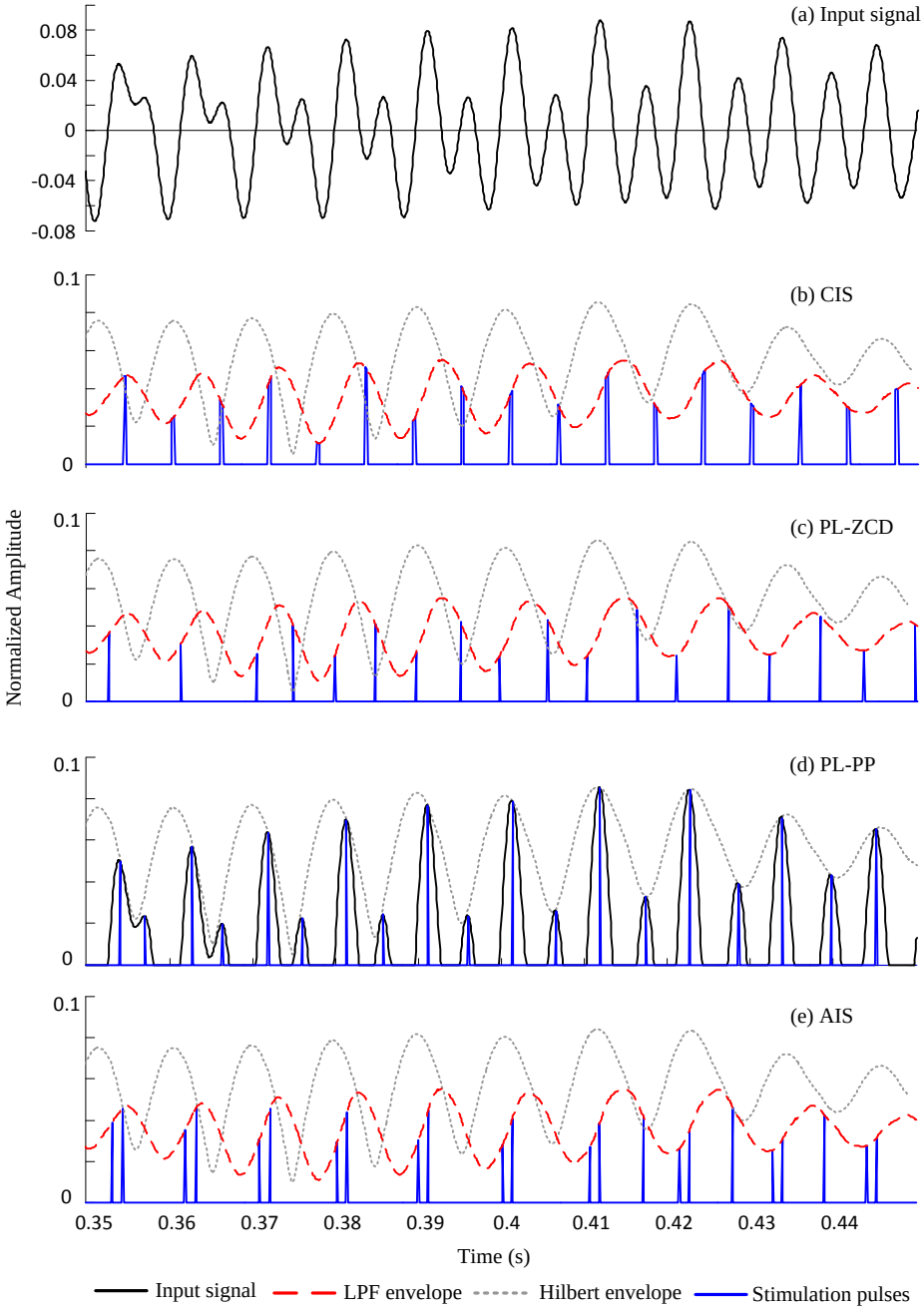

Figure 2.10: Waveforms obtained from different strategies.

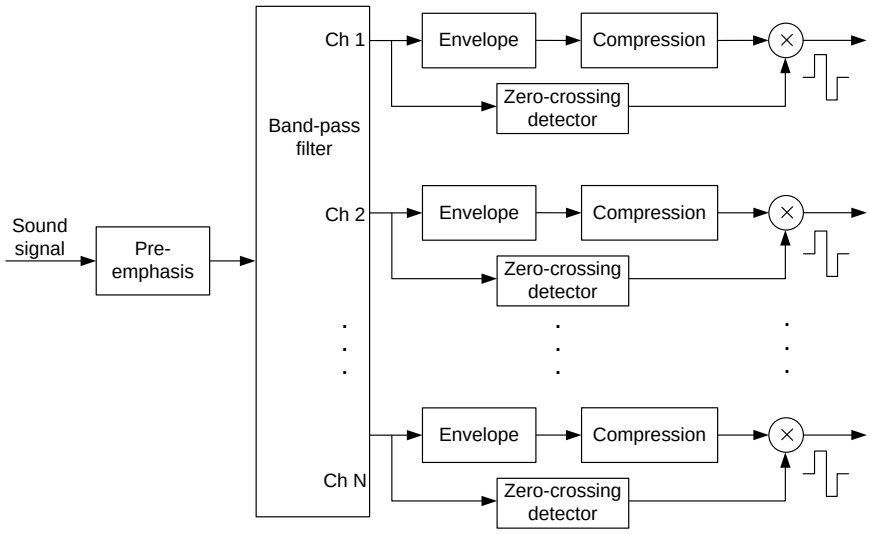

Figure 2.11: Block diagram of the phase-locking zero-crossing detection (PL-ZCD) strategy.

phase and TFS from the fixed timing interval of the pulse train.

2.6.2 Zero-Crossing Detection

In this strategy, the 2nd layer is put on top of the 1st layer to introduce a phase locking amplitude modulated pulse train. Fig. 2.11 shows the block diagram of a phase-locking zero-crossing detection strategy (PL-ZCD) or a simulated phase-locking stimulation (SPLS) strategy [55]. The signal after each band-pass filter goes through 2 signal pathways: the envelope extraction and the phase extraction. At the moment that the input signal crosses zero from negative to positive values, the pulse is generated and will be modulated with the momentary value of the envelope at that moment to create the stimulation pulse train. As we can see from the blue line of Fig. 2.10(c), the amplitudes of the pulse are also defined by the quality of the ED but the real-time period of the fundamental frequency (F0) can only be roughly encoded. This processor thus requires high precision zero crossing instant and high accuracy envelope detectors.

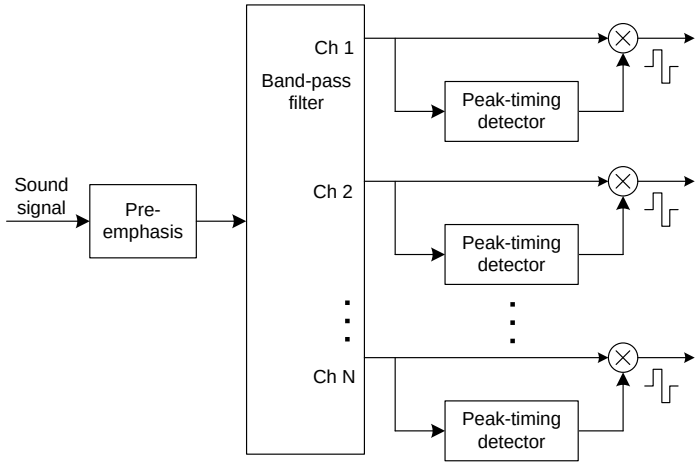

Figure 2.12: Block diagram of the phase-locking peak-picking (PL-PP) strategy.

2.6.3 Peak-Picking technique

This strategy also contains two layers of operations (1 and 2). But instead of detecting the zero-crossing moments to create the phase-locked pulse train, the occurrences of peaks in the input signal are detected [56]. The block diagram of this strategy is shown in Fig. 2.12. There are two main features different from the PL-ZCD. First, the number of peaks detected is higher than the number of zero crossing moments which can be seen from the blue lines in Figs. 2.10(c) and (d) during 0.35s $<$ t $<$ 0.37s. This implies that more instantaneous frequency information other than F0 can be conveyed to the stimulation electrodes. Second, as we can see from the peaks that always touch the Hilbert envelope, the BPF output signal and the detected peaking moments can be used to generate the stimulation pulses directly without the need for ED. For this reason, the precision of the stimulation pulse amplitudes is relayed to be dependent on the precision of a peak-instant detector.

2.6.4 Race-to-Spike Asynchronous Interleaved Sampling

In this case the 3$^{\text{rd}}$ layer is introduced. It has been proposed in [57] that to achieve the stochastic stimulation behavior, the gray boxes of Fig. 2.8

are replaced by half-wave rectifier circuits as shown in Fig. 2.13. Then, at particular repetitive time instants, the amplitudes from all channels will be sent to a winner takes all (WTA) network letting only the strongest amplitude pass to enable the pulse generator. To avoid successive stimulation within one channel that violates the bio-realism spiking behavior [58], additional circuit blocks are inserted to create an inhibition. At the moment that a stimulation pulse is being generated, there will be a signal created and applied to inhibit the signal from the half-wave rectifier (within the channel that is being stimulated), so that it will not be processed by the WTA network at the next time step. Even if the signal strength of that channel is highest, it will be ignored. Within this processor, the amplitude of each pulse is still specified by the ED of each channel but the location of the stimulated electrode is defined by the strength of the signal at that moment. The pulse waveform obtained from this processor is shown by the solid line in Fig. 2.10(e). To some extent, encoding sound using this strategy can emulate the random spiking behavior of the normal auditory nerve fiber and the perception of music is expected. It is unfortunate that the system is very complicated requiring two more additional circuits blocks.

2.7 System estimation and evaluation

MATLAB was used to simulate all encoding strategies. Three kinds of sounds were picked up for the simulation with a sampling frequency of 11,025 Hz including the word '*die*', the sentence '*the discrete Fourier transform of a real value signal is conjugate symmetric*' and the song phrase '*Hallelujah*' from Handel's Messiah. An 8 channel 4^{th}-order Butterworth BPF bank is used for all strategies with center frequencies ranging from 150 Hz to 4,000 Hz arranged according to the equivalent rectangular bandwidth (ERB) scheme [59]. Each envelope detector is formed by a full-wave rectifier followed by a 4^{th}-order Chebyshev LPF with 200 Hz cutoff frequency. The envelope detector is applied for all processors except PL-PP since this strategy does not need one.

The stimulation pulses obtained from Channels 1 to 8 of all strategies (the solid line as shown in Fig. 2.10 is only from the 1^{st} channel) are collected for reconstruction using the spike-based technique (in this context, spike refers to the pulse signal). This technique has its foundation in prior neurophysiology work showing that the original analog waveform can be accurately

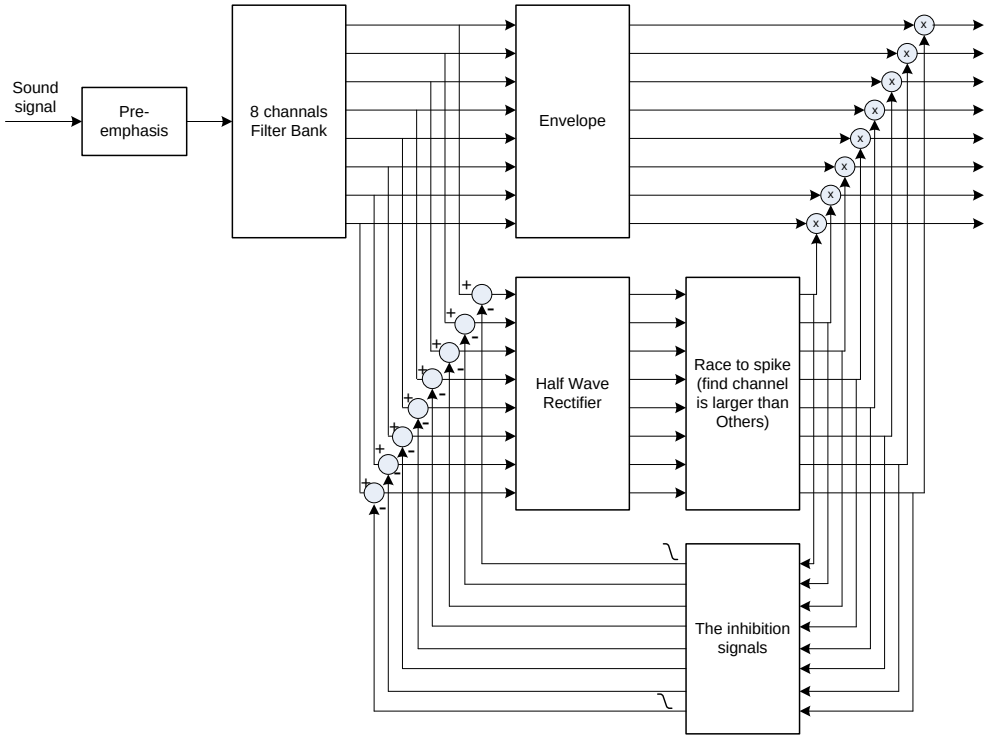

Figure 2.13: Block diagram of the asynchronous interleaved sampling (AIS) strategy.

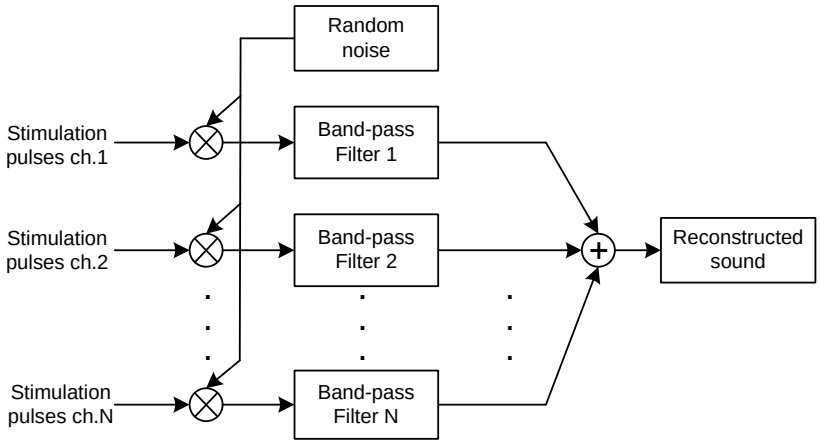

Figure 2.14: Spike-based reconstruction.

reconstructed from a spiking waveform [60]. We therefore use this technique for the signal reconstruction. Fig. 2.14 shows a block diagram of this reconstruction technique. The stimulation pulses of each channel are multiplied by uniformly distributed random noise before injecting into the BPF with the same center frequency as in the processor.

The resulting signals from all channels were added to produce the output sound. To exemplify the reconstructed waveforms, Figs. 2.15 and 2.16 show the reconstructed sounds of the word "*die*" from the CIS and PL-PP strategies, respectively. The original and reconstructed signals are represented by green and blue lines, respectively. Roughly, it is visible that the reconstructed signal from PL-PP is closer to its origin than that of CIS. The correlation coefficient (r) between the original signal and the reconstructed signal was used to estimate the quality of the signals encoded from different strategies. The correlation coefficient is computed from the following equation

$$r = \frac{\sum_{i=0}^{n} \left(X_i - \overline{X}\right)\left(Y_i - \overline{Y}\right)}{\sqrt{\sum_{i=0}^{n} \left(X_i - \overline{X}\right)^2} \sqrt{\sum_{i=0}^{n} \left(Y_i - \overline{Y}\right)^2}}, \tag{2.1}$$

where X_i,Y_i, $\overline{X}$ and $\overline{Y}$ are the original signal, the reconstructed signal and the mean values of X_i and Y_i, respectively. The correlation coefficient varies in the range of -1 to 1, where 1 indicates a perfect positive correlation, -1 the

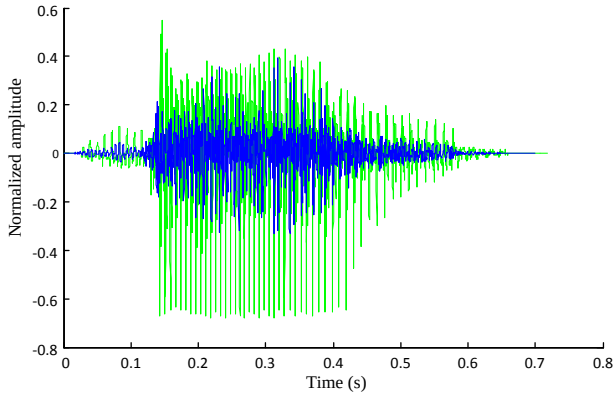

Figure 2.15: Reconstructed waveform of the word "*die*" from the CIS.

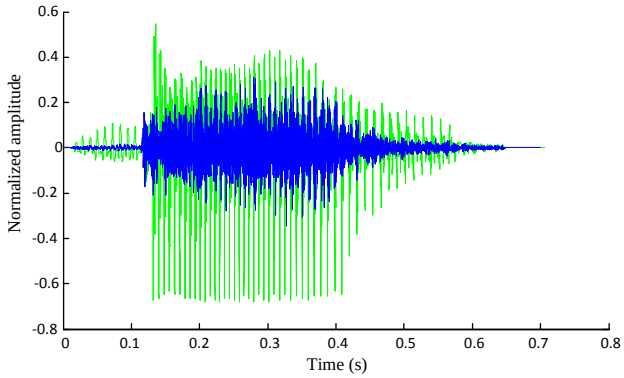

Figure 2.16: Reconstructed waveform of the word "*die*" from the PL-PP.

opposite and 0 indicates there is no correlation. The resulting correlation coefficients obtained from different strategies are shown in Table 2.1. It is clear that CIS performs worst of all. Besides, within the results from CIS, the values of r depend on the complexity of the original sounds. The highest value of $r = 0.11$ is from the simple word (single tone) and the lowest $r = 0.02$ is from the song which contains several tones that CIS could not capture.

Among the PL strategies, as expected from the coding mechanism that conveys more instantaneous information without loss from the non-ideality of

Table 2.1: Correlation for different strategies

Strategy	"*die*"	Sentence	'*hallelujah*'
CIS	0.11	0.05	0.02
PL-ZCD	0.36	0.14	0.50
PL-PP	0.47	0.25	0.59
AIS	0.49	0.38	0.52

the ED (see Fig. 2.10(d)) the PL-PP provides a better value of r than PL-ZCD for all cases. The race-to-spike AIS gives the best values of r for less complicated sounds (word and sentence) but for multitone sounds (song), the highest value of r is given by the PL-PP.

2.8 Conclusions

In order to understand how the ear functions, the anatomy of the ear has been described. Defects in the ear are mainly caused by the destruction or abscence of hair cells. These defects are causing hearing loss. In an attempt to solve this hearing loss, cochlear implants are developed. For understanding the working of cochlear implants, a brief history and overview of cochlear implants has been discussed. Despite the potential of the device, users are still not capable to hear melody or tonal languages. Reasearchers have developed several signal processing strategies in order to improve the cochlear implants performance. The system complexities and quality of the reconstructed signals from different signal processing strategies have been investigated and compared. Targeting the design of a fully implantable analog CI with an ability of tone recognition, the PL-PP provides the best solution, both in terms of compactness and correlation factors. Since the information of frequency, phase and TFS cannot be conveyed to the stimulation electrodes by CIS, it is really hard to believe that the brain can recognize any tone without proper input information. CIS is therefore removed from our consideration. It is true that the numbers of the correlation factor cannot 100% guarantee the quality of hearing perception in real CI recipients. Still, we are optimistic that the brain can interpret multi-tone sounds from the fast varying information conveyed to the stimulation electrodes by the rest of the strategies and that, after long term training, the patients would be able to recognize tonal languages and melodies. Combining the aforementioned

facts with the feasibility of building ultra low-power analog hardware, the PL-PP has proven itself as the most suitable analog sound processor.

Chapter 3

An analog complex gammatone filter

This chapter describes the design of an analog complex gammatone filter in order to extract both envelope and phase information of the incoming signals as well as to emulate the basilar membrane spectral selectivity. To synthesize the filter, the transfer functions are mapped onto an orthonormal ladder structure which provides good dynamic range, minimum sensitivity to component variations and high sparsity. A subthreshold $G_m - C$ filter is selected to realize the filter in order to verify the feasibility of the complex gammatone filter at very low power operation.

3.1 Introduction

To realize the spectral analysis in an analog speech processor, band-pass filter designs based on 2^{nd}-order filters in the form of log-domain [35,61] and $G_m - C$ filters [15] using CMOS circuits operating in weak inversion have been reported. These filter circuits are successful in terms of power consumption, but lack operation that is analogous to a real cochlea. Besides, in conventional speech processors [15, 35, 61], the envelopes are extracted by a full-wave rectifier and a low-pass filter that may provide compact hardware implementation, yet their high frequency information is corrupted [50, 54]. It was found in [62] that, observing a cochlear nucleus after electrical stimulation, a gammatone function could closely describe the resulting cochlear impulse responses. As a consequence, the gammatone filter has been pop-

ularly used in cochlear modeling [63] and speech recognition [64]. Also it has been suggested in [50, 54] that, in order to preserve the high frequency information of speech signals, the Hilbert transform should be employed instead of the simple rectifier combined with a low-pass filter. Recently, partially driven by the motivation mentioned above, a realization of a gammatone filter has been introduced [65]. The design is based on a class-AB log domain circuit using signal splitting and cascaded class-A biquad sections. The filter successfully emulates the pseudo-resonance behavior of the basilar membranes and provides a very high dynamic range of 120 dB. This paves the way for high performance bio-inspired analog filter design for new generations of cochlear implants.

In order to develop further, this chapter introduces a bio-realism of the cochlear channels by combining the gammatone impulse response with the 'Hilbert Transform (HT)' within a compact frequency selective circuit. The design methodology starts with Laplace transforming the gammatone function into two band-pass transfer functions which represent the real and imaginary signal of the complex gammatone filter.

3.2 Temperal envelope and fine structure

During the past several years, encoding of the temperal fine structure cue in cochlear implants has received much attention [66–71]. The temporal fine structure contributes mainly to auditory object information whereas the temporal envelope contributes to speech intelligibility [72]. In [13], it has also been recognized that the temporal fine structure is more important for music perception than the temporal envelope.

In 1912 David Hilbert showed that signals can be decomposed into slowly varying envelopes that modulate high frequency carriers [73]. Applying the Hilbert transform to an incoming speech signal, which is considered a real signal, $x_{re}(t)$, results in an imaginary signal $x_{im}(t)$ which can be combined to create the analytic signal

$$s(t) = x_{re}(t) + x_{im}(t). \tag{3.1}$$

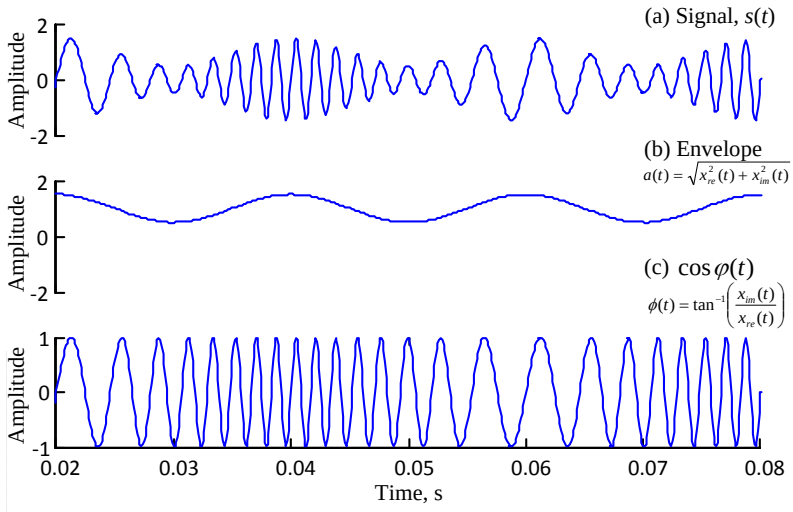

Figure 3.1: Decomposition of a signal using the Hilbert transformation. (a) original waveform, (b) the Hilbert envelope, and (c) the Hilbert fine structure.

Temporal envelope and fine structure (phase information) are respectively defined by

$$a\left(t\right) = \sqrt{x_{re}^2\left(t\right) + x_{im}^2\left(t\right)}, \tag{3.2}$$

and $cos\left(\phi\left(t\right)\right)$, where

$$\phi\left(t\right) = \tan^{-1}\left(\frac{x_{im}\left(t\right)}{x_{re}\left(t\right)}\right) \tag{3.3}$$

(3.3) is the phase of the analytic signal. An example of such a decomposition is presented in Fig. 3.1

3.3 The gammatone auditory filter bank

The name gammatone (or Γ-tone) was given by Aertsen and Johannesma after observing its impulse response which consists of a gamma-distribution envelope times a sinusoidal tone [65, 74]. Its popularity, within the auditory modeling community, results from its ability to provide an appropriately shaped 'pseudo-resonant' frequency transfer function that can be used to reasonably match physiologically measured responses [65]. The gammatone

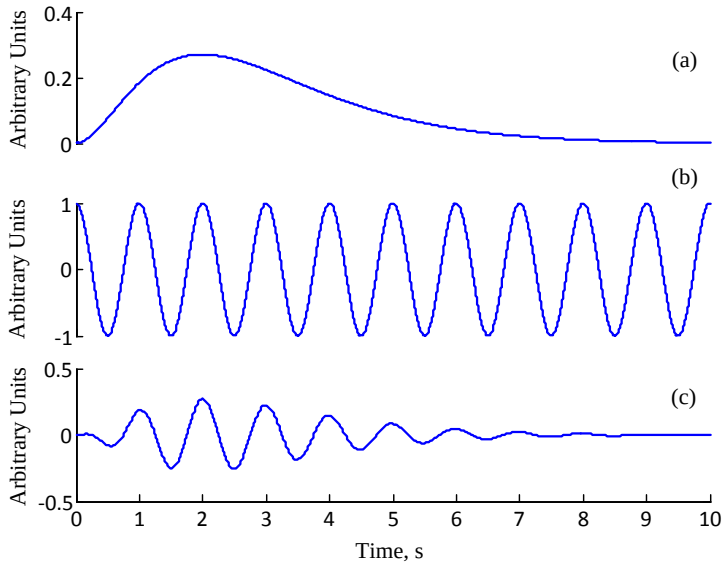

Figure 3.2: The components of a gammatone filter impulse response: (a) the gamma-distribution envelope, (b) the sinusoidal tone, and (c) the gammatone impulse response.

filter function describes the impulse responses of the mammalian cochlea and is defined by

$$g(t) = at^{(n-1)}e^{(2\pi bt)}\cos\left(2\pi f_c t + \phi\right);(t > 0)\,. \tag{3.4}$$

The parameter n is the order of the filter, b is the bandwidth of the filter, f_c is the centre frequency of the filter, a is used as an arbitrary factor in the filter response and it is typically chosen to make the peak gain equal unity and ϕ is the starting phase. The gammatone impulse response with its components is shown in Fig. 3.2.

The impulse response of the gammatone filter function provides an excellent fit to the impulse responses obtained from cats with the revcor technique [75, 76]. When n is 4 and b is 1.019 times the Equivalent Rectangular Bandwidth (ERB), (4) can represent the human auditory filter [77].

The ERB is a psychoacoustic measure of the bandwidth of the auditory filter at each point along the cochlea. In this work Glasberg and Moore's [78]

Table 3.1: $ERBs$ and center frequency of 16 cochlear channels

Channels	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
ERB (Hz)	40.89	50.55	62.48	77.23	95.46	118.00	145.86	180.30	222.87	275.49	340.53	420.93	520.31	643.16	795.01	982.71
f_c(Hz)	150.0	239.4	350.0	486.7	655.6	864.4	1122.5	1441.6	1835.9	2323.4	2926.0	3670.9	4591.6	5729.7	7136.5	8875.5

parameters have been adopted to calculate the ERB which is given as

$$ERB = 24.7\left(4.37\frac{f_c}{1000} + 1\right). \tag{3.5}$$

The f_c at each channel was determined using an expression derived in [79] for implementation of the Patterson-Holdsworth cochlear filter bank based on $ERBs$, shown as

$$\begin{aligned} f_c \;=\; & -(EarQ + minBW) + \cdots \\ & e^{\left((1{:}numChannels)^{\mathrm{T}} \times -log\left(\frac{f_s}{2} + (EarQ + minBW)\right) + log\frac{(lowfreq + (EarQ + minBW))}{numChannels}\right)} \\ & \times \left(\frac{f_s}{2} + (EarQ + minBW)\right) \end{aligned} \tag{3.6}$$

in which $EarQ$ is the asymptotic filter quality at large frequencies, $minBW$ is the minimum bandwidth for low frequency channels, $numChannels$ is the number of channels, $lowfreq$ is a low frequency and f_s is the sampling rate. An example of the centre frequencies of 16 cochlear channels and their ERB is shown in Table 3.1. The parameters in this example were set as follows: $EarQ$=9.26 and $minBW$=24.7 (Glasberg and Moore's parameters), $numChannels$=16, $lowfreq$=150 Hz and f_s=22050 Hz. Together, (3.4), (3.5) and (3.6) define the gammatone auditory filter bank.

3.4 Gammatone filter topology design

In order to implement the analog complex gammatone filter circuit, the gammatone functions in the time domain need to be transformed to the complex frequency domain (s-domain) using the Laplace transform and then these transfer functions need to be implemented by a state space orthonormal ladder structure. Using this structure, the subsequent circuit implementation can be performed easily. The flowchart of the gammatone filter disign is shown in Fig. 3.3. Details of the first two steps will be described in the next subsections.

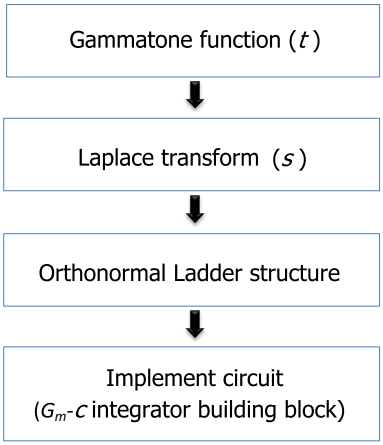

Figure 3.3: Gammatone filter design flowchart.

3.4.1 Laplace transform of the complex gammatone filter

A complex gammatone filter can be written as

$$g_c(t) = at^{(n-1)}e^{-2\pi bt}e^{j\omega t}. \tag{3.7}$$

By setting a=1, n=4 and ϕ=0, (3.7) can be modified for a complex tone as

$$\begin{aligned} g_c(t) &= g_{re}(t) + g_{im}(t) \\ &= t^3e^{-2\pi bt}\cos(\omega t) + jt^3e^{-2\pi bt}\sin(\omega t), \end{aligned} \tag{3.8}$$

where $g_{re}(t)$ and $g_{im}(t)$ are the real and imaginary gammatone filter function, respectively.
Converting (3.8) into the frequency domain using the Laplace transform, we obtain

$$G_{re}(s) = \frac{N_{re}(s)}{D_{re}(s)} = -\frac{d^3\left(\frac{s+B}{(s+B)^2+\omega^2}\right)}{ds}, \tag{3.9}$$

and

$$G_{im}(s) = \frac{N_{im}(s)}{D_{im}(s)} = -\frac{d^3\left(\frac{B}{(s+B)^2+\omega^2}\right)}{ds}, \tag{3.10}$$

where $B = 2\pi b = 2\pi(1.019ERB)$ and $\omega = 2\pi f_c$. $G_{re}(s)$ and $G_{im}(s)$ are

the transfer functions of the real and imaginary signals, respectively. Note that the denominators of both transfer functions are the same, facilitating a compact hardware implementation, which will be illustrated shortly.

To exemplify the case of a centre frequency of 1 kHz and an *ERB* of 132.64 Hz, we have normalized the transfer function as

$$\begin{aligned} N_{re}(s) &= -1.05\times10^{12}s^4 - 3.566\times10^{15}s^3 + 2.441\times10^{20}s^2 \\ &\quad +4.197\times10^{23}s - 1.457\times10^{27}, \\ N_{im}(s) &= -2.638\times10^{16}s^3 - 6.722\times10^{19}s^2 + 9.845\times10^{23}s \\ &\quad +8.684\times10^{26} \text{ and} \\ D(s) &= s^8 + 6.794\times10^3 s^7 + 1.781\times10^8 s^6 + 8.389\times10^{11}s^5 \\ &\quad +1.11\times10^{16}s^4 + 3.372\times10^{19}s^3 + 2.878\times10^{23}s^2 \\ &\quad +4.413\times10^{26}s + 2.611\times10^{30}. \end{aligned} \tag{3.11}$$

Fig. 3.4 shows the impulse responses including the envelope (simulated using MATLAB) of the real and imaginary transfer function in (3.11). Magnitude responses of 16 cochlear channel real transfer functions by using the parameters in Table 3.1 are shown in Fig. 3.5.

3.4.2 Orthonormal state space representation

In order to implement the complex gammatone filter, both real and imaginary transfer functions are mapped onto a state space orthonormal ladder structure. When designing high-order filters, it is very desirable to concentrate on circuits that are less sensitive to component variations. The Dynamic range-Sparsity-Sensitivity figure-of-merit (DRSS) in [80] shows that the orthonormal ladder structure presents the best performance (minimum DRSS) compared to the other state space description such as Optimal Dynamic Range, Biquad, Schur and Canonical. The common form of a state space description in the Laplace domain is given by

$$\begin{aligned} sX(s) &= \mathbf{A}X(s) + \mathbf{B}U(s) \\ Y(s) &= \mathbf{C}X(s) + \mathbf{D}U(s), \end{aligned}$$

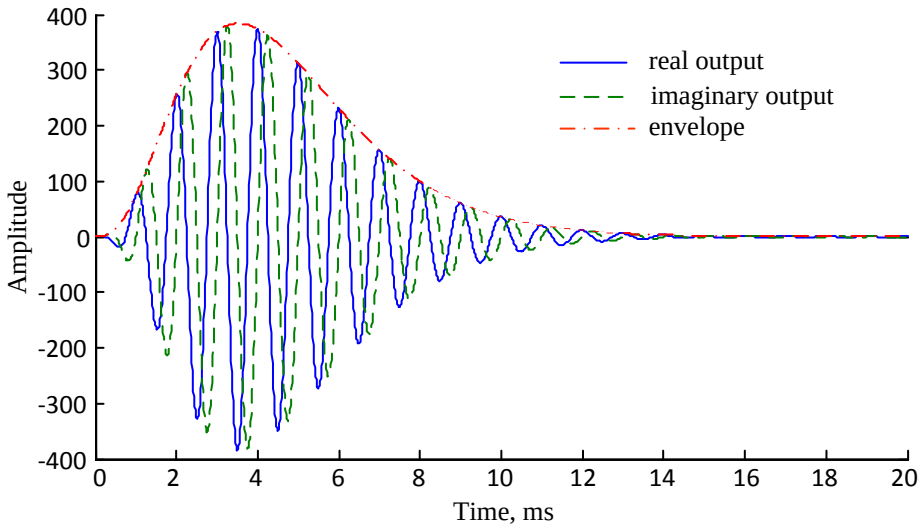

Figure 3.4: Impulse responses including the envelope (simulated using MATLAB) of the real and imaginary transfer function in (3.11).

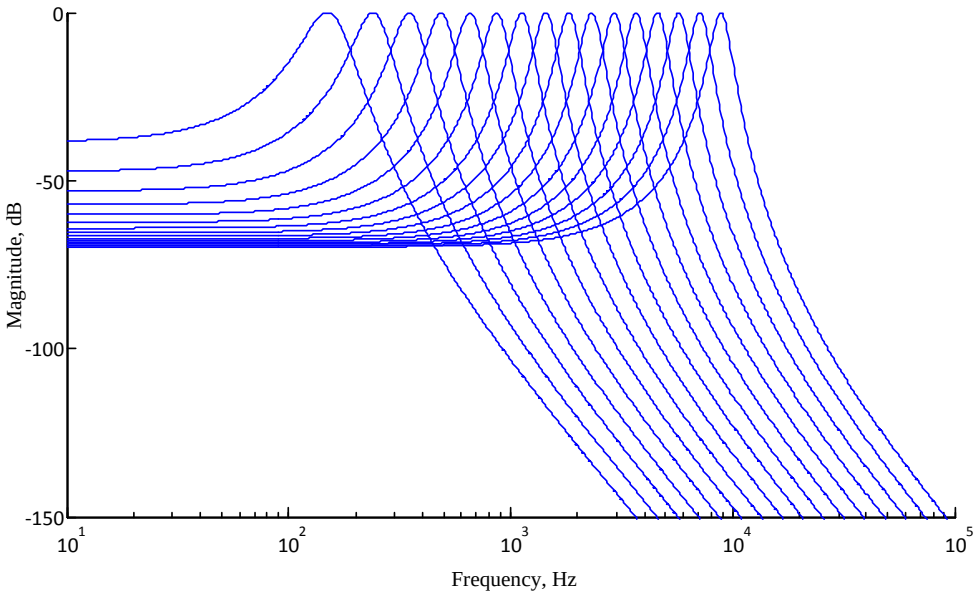

Figure 3.5: Magnitude responses of 16 cochlear channel real transfer functions.

where $U(s)$ and $Y(s)$ are the input and output signals of the system, respectively. The vector variable $X(s)$ represents the state of the system. **A**, **B**, and **C** are the coefficients that weigh the state variable, input and output, respectively. **D** is the coefficient that weigh the system inputs. For many physical systems the matrix D is the null matrix, which also holds for the orthonormal ladder structure. The state space description, viz., **A**, **B** and **C** matrices of this structure are given by [81]

$$\mathbf{A} = \begin{bmatrix} 0 & \alpha_1 & & \cdots & & 0 \\ -\alpha_1 & 0 & \alpha_2 & & & 0 \\ & -\alpha_2 & 0 & \alpha_3 & \cdots & \\ \vdots & & \ddots & \ddots & \ddots & \vdots \\ 0 & & \cdots & -\alpha_{n-2} & 0 & \alpha_{n-1} \\ 0 & & \cdots & & -\alpha_{n-1} & \alpha_n \end{bmatrix}, \mathbf{B} = \begin{bmatrix} 0 \\ 0 \\ 0 \\ \vdots \\ 0 \\ \sqrt{\frac{\alpha_n}{\pi}} \end{bmatrix} \text{ and}$$

$$\mathbf{C^T} = \begin{bmatrix} c_1 \\ c_2 \\ c_3 \\ \vdots \\ c_{n-1} \\ c_n \end{bmatrix}. \tag{3.12}$$

The coefficients, α are defined as

$$\begin{aligned} \alpha_i &= \sqrt{\frac{1}{x_i x_{i+1}}} \quad 1 \leq i < n, \\ \alpha_n &= \frac{1}{x_n} \quad i = n, \end{aligned} \tag{3.13}$$

where x_i is the reactive component of a singly terminated LC ladder structure. In order to calculate the values of the reactive elements x_i, one needs to apply a continued fraction expansion on the denominator of the transfer function. In order to implement the numerator $N(s)$ of the transfer function, the proper **C** vector must be obtained. Using the intermediate function F_i, the coefficients c_i can be written as

$$N(s) = c_1 \cdot F_1 + c_2 \cdot F_2 + \cdots + c_n \cdot F_n, \tag{3.14}$$

where

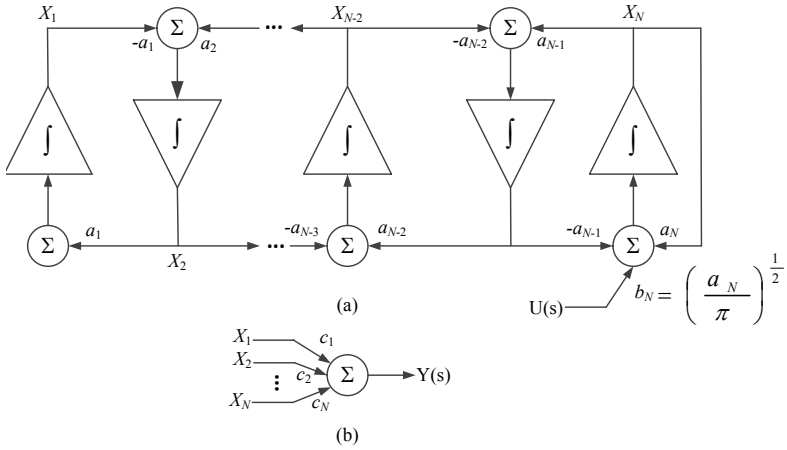

Figure 3.6: Block diagram of an orthonormal ladder filter [81], (a) Leapfrog structure and (b) Output summing stage.

$$\begin{aligned} F_1 &= \sqrt{\frac{x_1}{\pi}} \cdot N(0) \\ F_2 &= \frac{s}{\alpha_1} F_1 \\ F_i &= \frac{1}{\alpha_{i-1}} \left(s F_{i-1} + \alpha_{i-2} F_{i-2} \right) \quad 3 \leq i \leq n. \end{aligned} \tag{3.15}$$

The proper **C** vector is found as the multiplying coefficients required to create the desired numerator [82] .
Fig. 3.6 shows a block diagram of a general orthonormal ladder filter [81]. As shown in the block diagram, the filter output is obtained from a linear combination of the outputs of all integrators.

The state space description, viz., the **A**, **B**, and **C** matrices of the example transfer function (3.11) are given by

$$\mathbf{A_{re,im}} = \begin{bmatrix} 0 & 6201 & 0 & 0 & 0 & 0 & 0 & 0 \\ -6201 & 0 & 778.5 & 0 & 0 & 0 & 0 & 0 \\ 0 & -778.5 & 0 & 6093 & 0 & 0 & 0 & 0 \\ 0 & 0 & -6093 & 0 & 1608 & 0 & 0 & 0 \\ 0 & 0 & 0 & -1608 & 0 & 5788 & 0 & 0 \\ 0 & 0 & 0 & 0 & -5788 & 0 & 3350 & 0 \\ 0 & 0 & 0 & 0 & 0 & -3350 & 0 & 7391 \\ 0 & 0 & 0 & 0 & 0 & 0 & -7391 & -6794 \end{bmatrix},$$

$$\mathbf{C_{re}} = \begin{bmatrix} -39.4 & 10.99 & 4.96 & -0.324 & -0.158 & 0 & 0 & 0 \end{bmatrix},$$

$$\mathbf{C_{im}} = \begin{bmatrix} 10.95 & 39.63 & -1.03 & -2.46 & 0 & 0 & 0 & 0 \end{bmatrix},$$

and

$$\mathbf{B^T} = \begin{bmatrix} 0 & 0 & 0 & 0 & 0 & 0 & 0 & 46.5 \end{bmatrix}.$$

Fig. 3.7 shows the block diagram and the impulse responses of this example transfer function. The **A** matrix determines the denominator of both real and imaginary transfer functions. A scaling factor for the whole filter is defined by matrix **B**. To realize the real and imaginary outputs, different parameters in matrices $\mathbf{C_{re}}$ and $\mathbf{C_{im}}$ will be used. Therefore, in a practical implementation (a $G_m - C$ structure in this case, See Fig. 3.9 in Section 3.5), we can save area and power since all the time constants whose realizations consume most of the total chip area and power can be shared. Unlike other realizations that double hardware to realize real and imaginary transfer functions [83], in this work, only two different sets of transconductors are required.

3.5 Circuit design of the complex gammatone filter

The circuit design of the filter is based on the $G_m - C$ integrator approach using identical simple subthreshold differential transconductors as main building blocks shown in Fig. 3.8. The voltage to current relationship of the transconductor is given by

$$I_{out} = I_B \tanh \frac{V_d}{2nU_T}, \tag{3.16}$$

where n and U_T are the subthreshold slope factor and thermal voltage, respectively [84].
The small signal transconductance, $g_m = I_B/2nU_T$ can be found from the first term of the Taylor series expansion of (3.16). Fig. 3.9 shows the topology of the complex gammatone filter corresponding to the above state-space representation. The integrator time constants in the **A** matrix are defined

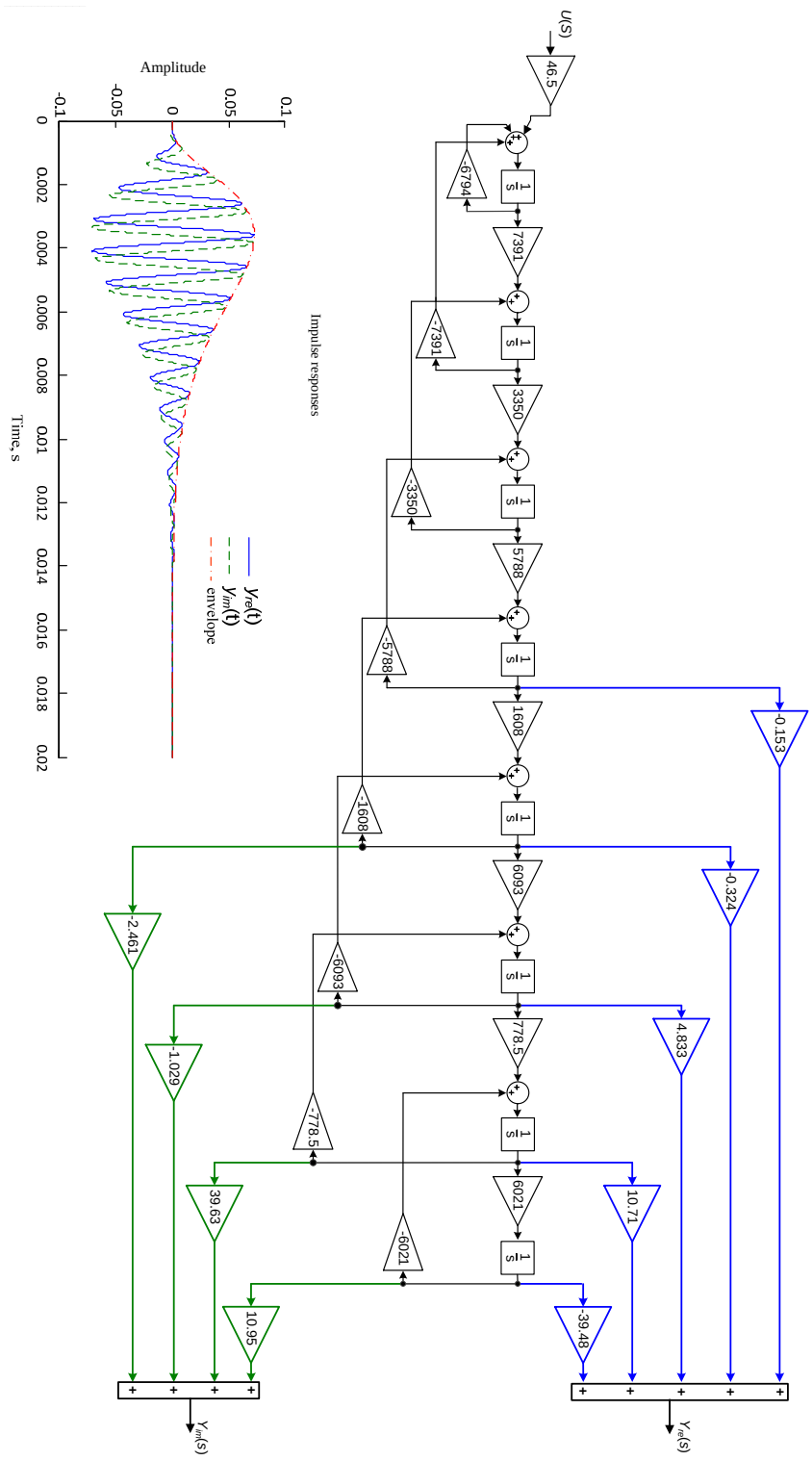

Figure 3.7: The blockdiagram and the impulse responses of the example transfer function (3.11).

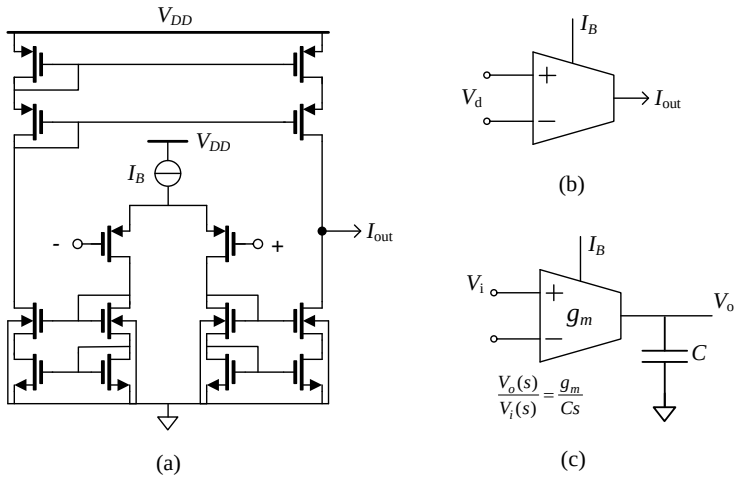

Figure 3.8: Subthreshold Tanh transconductor (a) circuit (b) symbol and (c) the $G_m - C$ integrator.

by ($\tau = C/g_m$) where $C = C_i$= 20pF. The bias current of each transconductor is set according to the coefficients in the matrices. The centre frequency and the gain of the filter can be varied by scaling the bias currents of the transconductors of matrices **A**, **B**, and **C**, respectively. The parameter $\mathbf{A_{ij}}$ is implemented by the corresponding $G_m - C$ integrator with bias current $I_{A_{ij}}$, defined by

$$I_{A_{ij}} = 2nU_T C_i \mathbf{A_{ij}}. \tag{3.17}$$

The state-space vector **B** is realized by the first row from the top of Fig. 3.9. The current $I_{B_{i1}}$ is related to the parameter $\mathbf{B_{i1}}$ by

$$I_{B_{i1}} = 2nU_T C_i \mathbf{B_{i1}}. \tag{3.18}$$

In the orthonormal case, only one non-zero parameter of the **B** vector is present ($\mathbf{B_{81}}$). Consequently, $I_{B_{i1}} = I_{B_{81}}$. The bias current vector $I_{C_{i1}}$, which is controlled by the vector **C**, is defined as

$$I_{C_{i1}} = 2nU_T \mathbf{C_{i1}}. \tag{3.19}$$

The imaginary output is obtained by adding only the **C** vector of the imaginary transfer function ($\mathbf{C_{im}}$), as shown in Fig. 3.9.

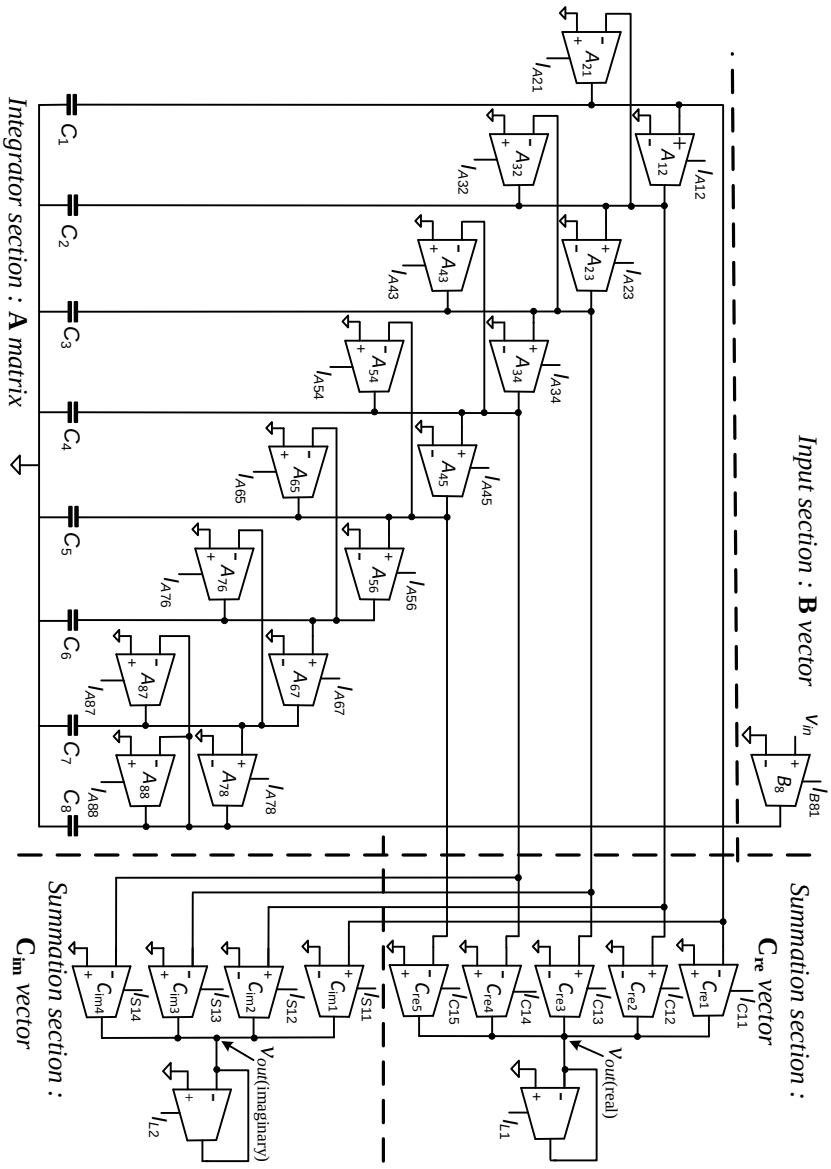

Figure 3.9: Circuit of the gammatone filter.

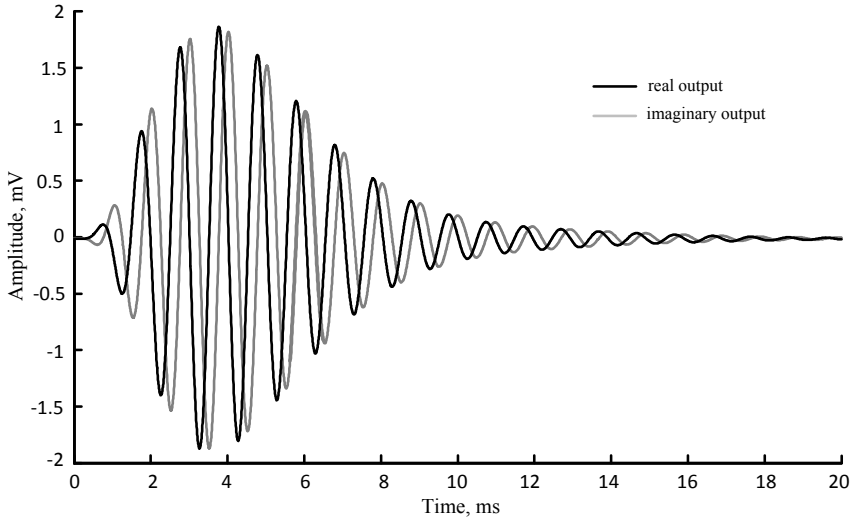

Figure 3.10: Simulated impulse response of the example transfer function, (3.11).

3.6 Circuit Simulations

The concept of the complex gammatone filter was verified in Cadence using RF spectre and AMIS 0.35 µm CMOS technology. The dimensions equal W/L=6µm/6µm and 6µm/2µm for the PMOS differential pair and all transistors in the cascoded current mirrors, respectively. Supply voltage V_{DD}= 2V and the common mode voltage reference was set at 1 V. The quiescent power consumption equals 4.71 µW. Fig. 3.10 shows the impulse response of the filter at 1 kHz centre frequency by applying a positive pulse signal, with an amplitude of 10 mV and a pulse width equal to 100 µs. The common mode signal has been removed for clarity. The frequency responses of the filter are shown in Fig. 3.11 and 3.12 for the real and imaginary outputs, respectively. It is clear that, in the pass-band, the results are close to the ideal case. Fortunately, errors induced from non-idealities of the transconductor occurred mainly in the stop-bands and do not harm the filter's functionality. The integrated output noise power over the range from 15 Hz to 15 kHz is $2\mu V^2$ and the noise power spectral density (PSD) is shown in Fig. 3.13. Fig. 3.14 shows the total harmonic distortion (THD) of the real and imaginary output, when sinusoidal inputs signals, ranging from 2 mV to 34 mV, are applied at the centre frequency of 1 kHz.

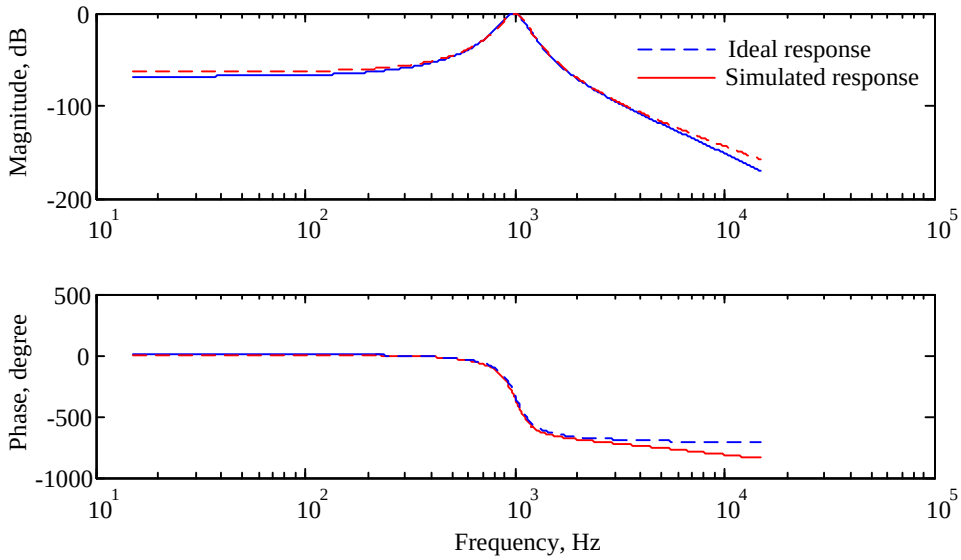

Figure 3.11: Frequency responses of the filter's real output.

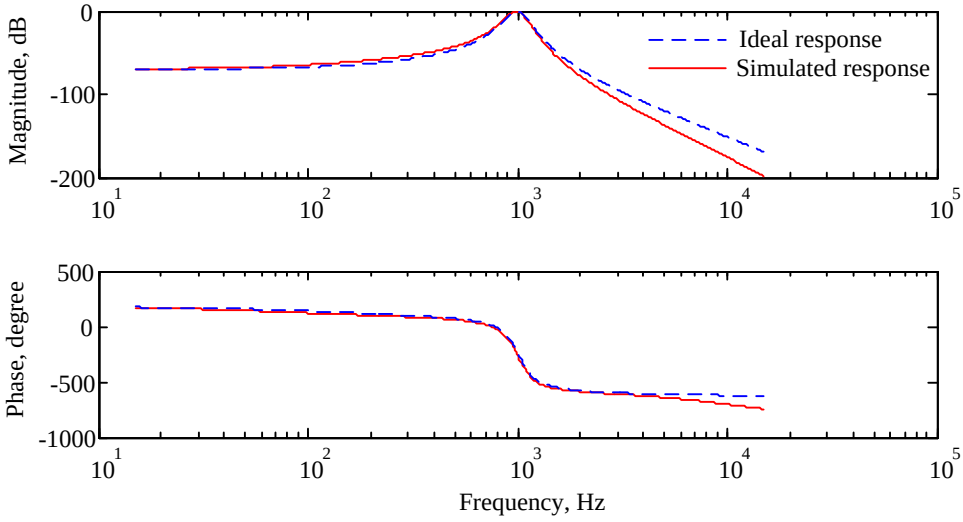

Figure 3.12: Frequency responses of the filter's imaginary output.

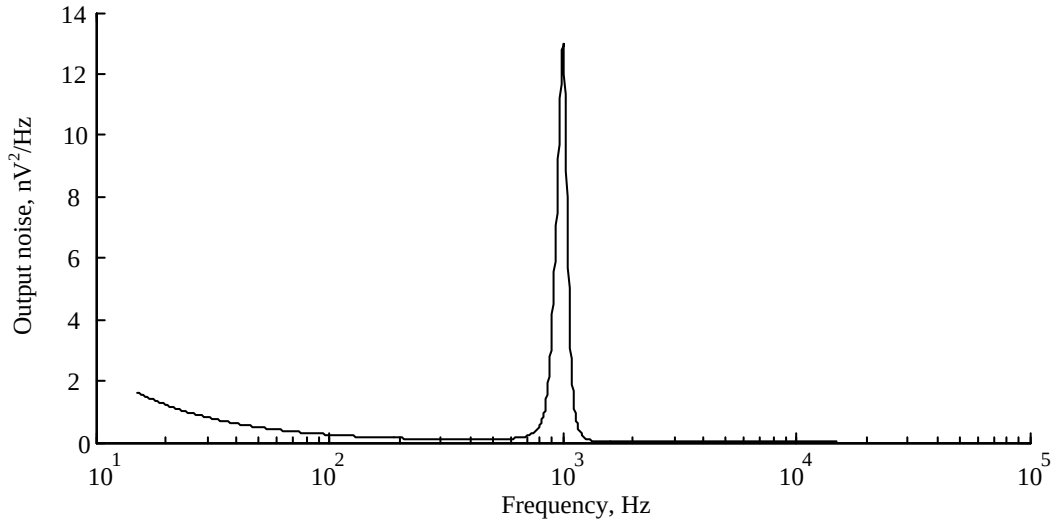

Figure 3.13: Output noise (PSD).

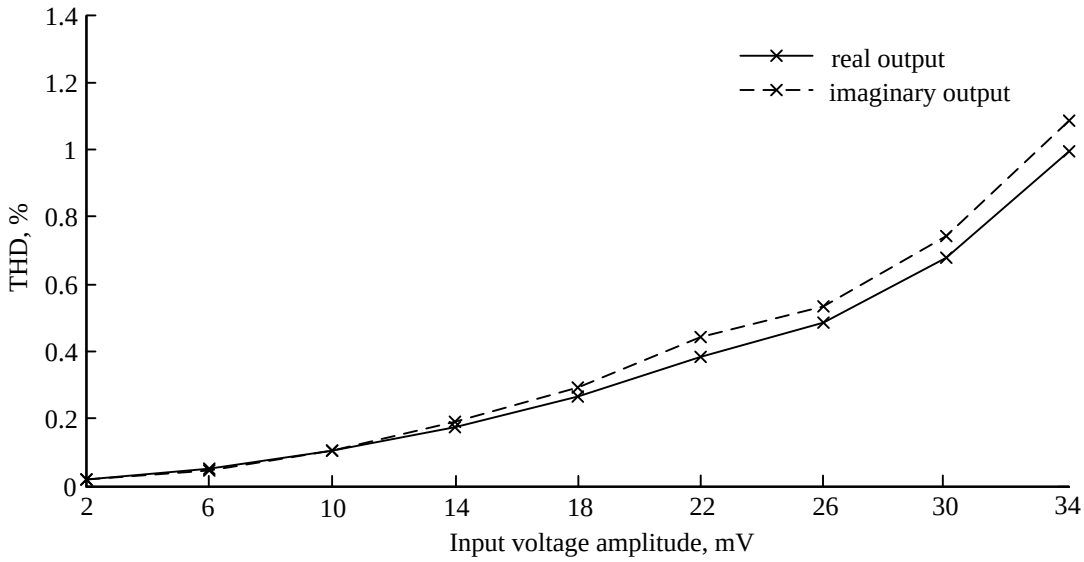

Figure 3.14: Total harmonic distortion.

3.7 Conclusions

The theory and design of a complex gammatone filter for cochlear implants has been introduced in this chapter. The key features for speech intelligibility including temporal envelope and phase information can be extracted from a compact $G_m - C$ poly-phase band-pass filter circuit. The gammatone impulse response is first transformed into the complex frequency (s-) domain and the resulting 8^{th}-order transfer function is subsequently mapped onto a state-space description of an orthonormal ladder filter. Using this approach, the real and imaginary transfer functions that share the same denominator can be extracted using two different $\mathbf{C}$ matrices. This results in a compact filter structure.

Chapter 4

An ultra low-power peak instant detector for a peak picking cochlear implant processor

Targeting the design of a fully implantable analog cochlear implant with an ability of tone recognition, a comparison of the input and reconstructed signals in terms of correlation factor and hardware complexity in Chapter 2 pointed out that a phase-locking peak-picking strategy (PL-PP) provides a compact solution for the fully implantable cochlear implant electronic hardware design. This chapter presents the design of a subthreshold CMOS peak-instant detector (PID) to be used in a PL-PP cochlear implant processor.

4.1 Introduction

Trying to allow a cochlear implant (CI) processor to convey phase and temporal fine structure (TFS) in addition to the envelope of the speech signal to the auditory nerve fibers, several speech processing strategies have been proposed to be used in the CI processor including phase-locking zero-crossing detection (PL-ZCD) [55], asynchronous interleaved sampling (AIS) [57], and PL-PP [56] strategies. They are based on the idea of imitating either phase locking [51] or random firing [85] of the spike train in the auditory nerve fiber.

In the normal mammalian auditory nerve fibers, the spike trains synchronize with the stimulus waveform periodicity up to 5 kHz [51]. Beyond that frequency range, the spike trains are generated randomly [85]. These mechanisms are missing in the conventional CIS strategy since the pulse stimulation rate is fixed [48]. To gain the perception of tonal languages and music, an effort of realizing the cochlear implant processor that imitates the inner hair cells and the auditory nerve behavior more precisely is necessary. One way to achieve this is introducing the Hilbert Transform (HT) to the CI processor to extract temporal envelope, instantaneous frequency and phase, and thereby the TFS [50] and try to convey them to the stimulation electrodes. Although extraction is possible, conveying all of the information to the brain via electrical pulse trains is still a challenge that remains. Besides, performing the HT imposes a large computational cost for both digital [86] and analog [22] processors.

The comparative study in Chapter 2 [23] suggests that the PL-PP strategy provides a compact solution to partially convey the TFS suitable for an ultra low-power analog cochlear implant processor. This chapter designs a low-power peak-instant detector for supporting the PL-PP strategy to be incorporated together with the continuous interleaved sampling (CIS) strategy within an ultra low-power analog cochlear implant processor. To operate the entire CMOS circuit in weak inversion region for the purpose of very low power consumption, the switched current (SI) technique is applied to let us benefit from the mismatch insensitive feature of the SI memory cell.

4.2 Peak-Picking strategy

Fig. 4.1 shows a block diagram of the PL-PP speech processing strategy. It comprises four main elements; a preemphasis block, a band pass filter (BPF) bank, a number of peak-instant detectors (PIDs), and modulators. The incoming sound is pre-emphasized by non-linearly amplifying it before entering the bank of BPFs. This mechanism is adapted from the role of the outer hair cells that map the wide range of the incoming sound pressure onto the limited dynamic range of the ear. The BPF bank roughly mimics the basilar membrane behavior by decomposing the signal into a limited number (N) of frequency bands (channels). The peaks of the signal coming from the

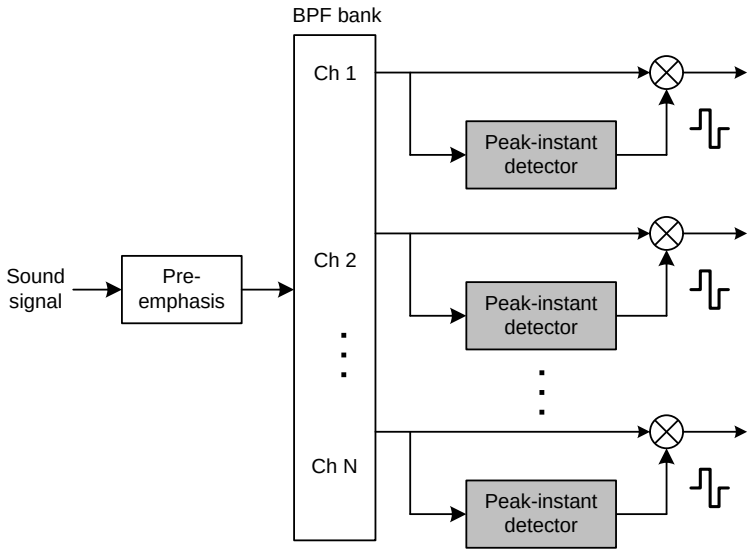

Figure 4.1: PL-PP speech processing block diagram.

BPF of each channel will be extracted by the PID enabling the modulator to perform multiplication of a rectangular pulse signal and the peak amplitude. This results in a set of rectangular stimulation pulses of which the amplitude is defined by the peak of the signal of each channel and the pulse frequency changes according to the speech signal of each channel.

Fig. 4.2 shows a fraction of the speech signal from the word 'die' after 4^{th}-order Butterworth BP filtering with a center frequency of 150 Hz (Ch. 1 of the block diagram in Fig. 4.1). The signal obtained from Ch. 1 is represented by the dashed line. The HT (which is not part of the PL-PP strategy) is applied to the dashed line signal and the envelope is extracted and shown by the dotted line. The resulting pulses taken from the output of the modulator are represented by the solid line. As we can see from the peaks that always touch the Hilbert envelope, the BPF output signal and the detected peaking moments can be used to generate the stimulation pulses directly without the need for a very precise envelope detector. The precision requirement of the stimulation pulse amplitudes is relayed onto the precision of a PID instead.

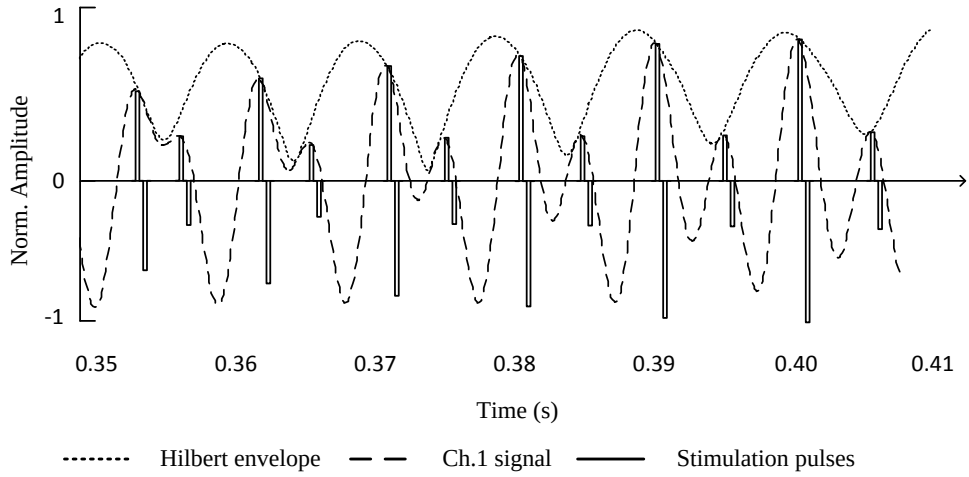

Figure 4.2: Waveforms obtained from PL-PP strategy.

4.3 The circuit of the current mode peak-instant detector

4.3.1 Concept

The basic idea of the proposed PID is shown by the block diagram in Fig. 4.3a [87, 88]. Input signal x_t is split into two signal paths. First, it goes to the sample and hold amplifier, SHA, (with a unity gain) generating a half delayed signal, x_{td}. Second, it goes to the summing node. The sample and hold time period are controlled by a clock signal (Clk) with 50% duty cycle indicated as the middle trace of Figures. 4.3b and 4.3c. The subtracted result of x_t and x_{td} at the holding period will change its polarity when x_t reaches its maximum and minimum values. For this reason, the comparator can decide on its logical output y_t according to its input sign reversing moment.

Since the incoming signal is random, this concept gives us two extreme cases of delay time (assuming the comparator is ideal). Firstly, the minimum delay time (t_d) occurs when the falling edge of the clock signal is located exactly at the peak of x_t (See Fig. 4.3b). In this case, the detected y_t will not be delayed. Secondly, the maximum delay time occurs when the rising edge

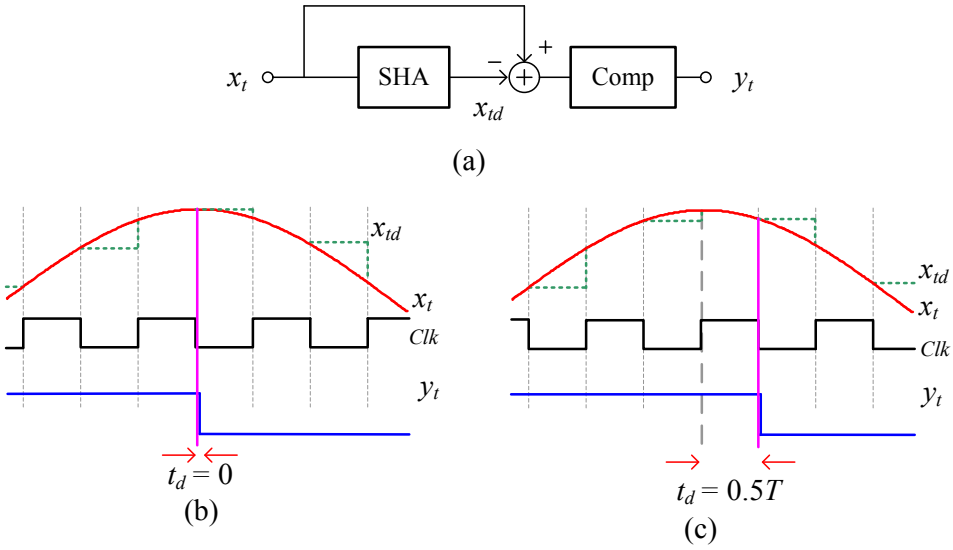

Figure 4.3: Peak-instant detection concept (a) operational block diagram (b) best case detection and (c) worst case detection.

of the clock is located exactly at the peak. In this case, t_d becomes a half period of the clock signal. In practice, the charge injection error and output noise of the SHA and minimum detectable input signal and delay time of the comparator introduce additional errors. In circuit level design, the architecture of the SHA needs to be insensitive to the switch charge injection error and the resolution and speed of the comparator need to be sufficiently good to decide on its logical output within a half clock period.

4.3.2 Circuit design

Fig. 4.4 shows a macro-model of the proposed PID. It comprises a fully differential SI-SHA and a voltage comparator. The PID is controlled by two non-overlapping clock phases S_1 (sampling) and S_2 (holding). When the set of switches S_1 turns on, the differential input current will be converted into voltages across C_H. In the next phase, S_1 turns off and the set of switches S_2 turns on. Both identical C_H's will memorize the voltages across them producing a constant differential current via transconductor G_m. The memorized current will be compared with the input current and converted into a

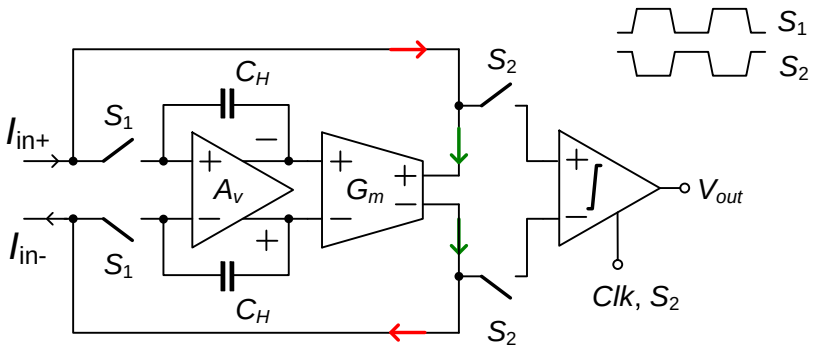

Figure 4.4: Macromodel of the SI peak-instant detector.

differential voltage at the input nodes of the comparator. The comparator will make a decision within this phase and generate an output logical voltage V_{out}. The clock control signal is applied to allow the comparator to operate only at the holding period otherwise the logical output remains. Due to the large loop gain providing by voltage amplifier A_v, voltages across switches S_1 are forced to be fixed at the input common mode level. This leads to signal independent charge injection errors after the (practical MOS) switches are turned off and thus will be cancelled out by the differential operation at the input of the comparator [89].

The sub-circuits used to realize all active elements in Fig. 4.4 are shown in Fig. 4.5. A_v is formed by the circuit of Fig. 4.5a and its output common-mode level V_{C2} is controlled by the common-mode feedback (CMFB) circuit depicted in Fig. 4.5b. G_m is realized by the circuit in Fig. 4.5c and its output common-mode level V_{C1} is controlled by the CMFB circuit in Fig. 4.5d. Stability of the feedback loop can be maintained by setting a fixed ratio of bias currents I_{B2} and I_{B1} and a value of C_H that needs to be bigger than the parasitic capacitances present at the input nodes of the A_v and those of G_m when the loop is closed [89]. We satisfied this condition by setting I_{B2}= 2.2I_{B1}= 220 nA and realizing C_H by NMOS capacitors biased in their strong inversion region. We thus set supply voltage V_{DD} = 1.2 V, common-mode voltages V_{C1}= 1 V and V_{C2}= 0.2 V. All the transistors in the entire circuit are working in weak inversion and the parasitic capacitances are smaller compared to those of MOS transistors in the strong inversion region for the same device size.

Table 4.1: Transistor dimensions

MOSFET	W [μm]	L [μm]
M_1, M_4, M_6, M_9	24	6
M_2, M_3, M_5, M_7,M_8, M_{10}	3	3
NMOS M_H (C_H)	11	11
M_{11}	6	3
M_{12}	3	3
M_{13}, M_{14}, M_{15},M_{16}	0.5	0.35

The comparator is realized by the circuit shown in Fig. 4.6. It is composed of a differential input stage cascaded by a chain of CMOS inverters to enhance the overall gain. Input parasitic capacitors C_{in+} and C_{in-} are employed to memorize the input voltage for keeping the output voltage at the same value for the whole sampling period (switches S_2 are turned off). Note that the comparator employed in this work is a simple high gain open-loop amplifier which does not provide high speed and high sensitivity. Better results can be expected from using more sophisticated comparator circuitry, if needed.

4.4 Simulation results

The PID circuit has been designed to be implemented in AMIS 0.35 μm CMOS process technology. The bias current of the comparator is set to I_{B2}= 50 nA. The total bias current becomes 720 nA (excluding that of the bias generator circuit). This results in a static power consumption of 864 nW. Dimensions of the MOS transistors used are listed in Table 4.1. The transistors are largely sized to alleviate the mismatch problem of MOS transistors in weak inversion.

Fig. 4.7 demonstrates the transient response of the proposed PID circuit in the worst case detection (see Fig. 4.3c) for a sinusoidal differential input current with an amplitude of 80 nA, a 5 kHz frequency and a 100 kS/s sampling frequency. The input current and the holding current are shown on the top by the dotted and solid lines, respectively. There are large transient glitches appearing at the beginning of the holding phases but they do not affect the corrected circuit operation. In the middle graph, we can see that

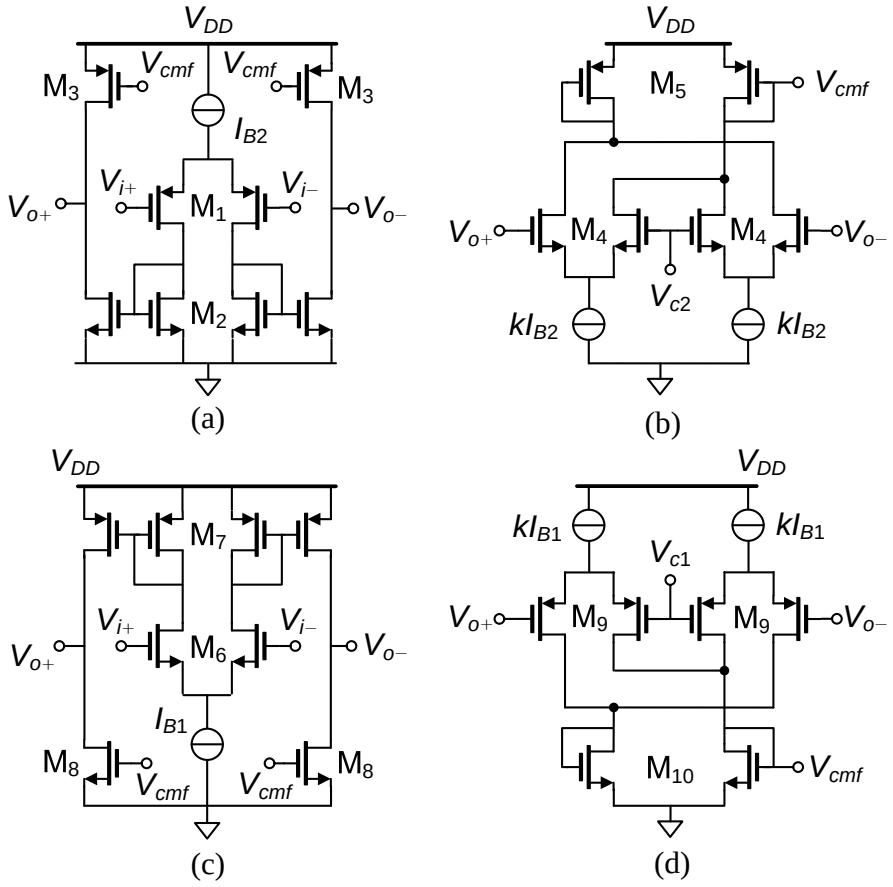

Figure 4.5: Sub-circuits of the SHA (a) transconductor G_m, (b) CMFB circuit for the G_m, (c) voltage amplifier A_v and (d) CMFB circuit for the A_v.

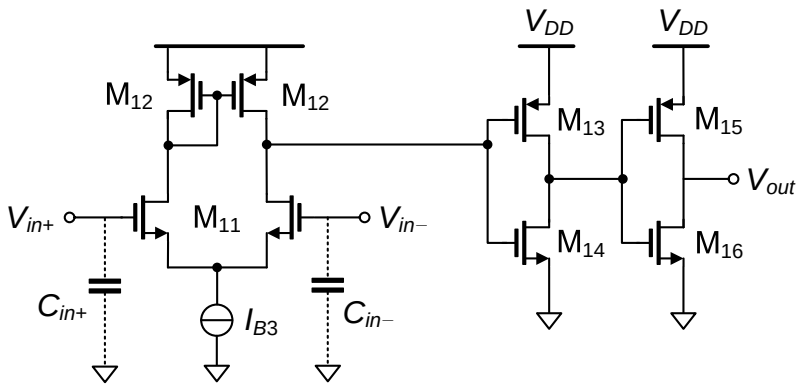

Figure 4.6: Comparator circuit

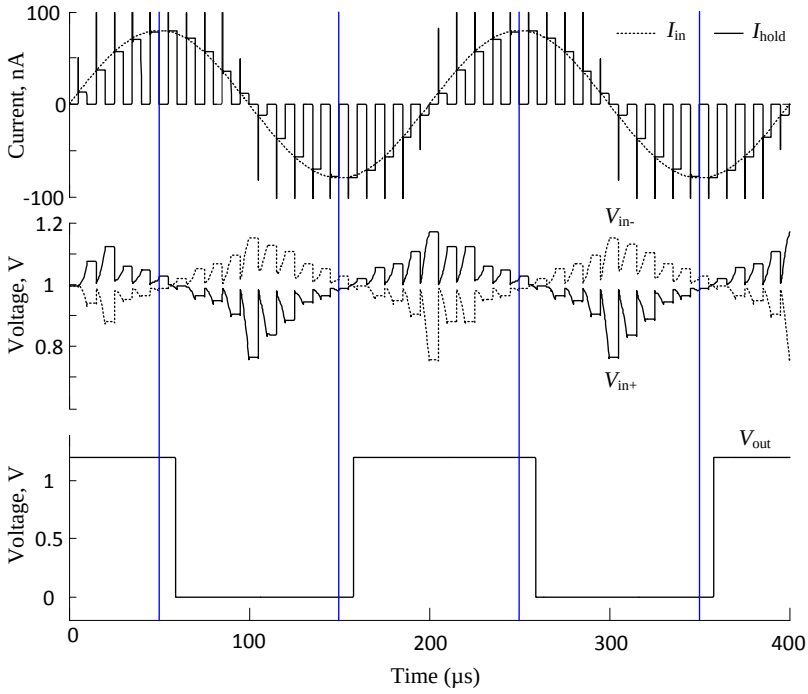

Figure 4.7: The transient response of the proposed PID circuit.

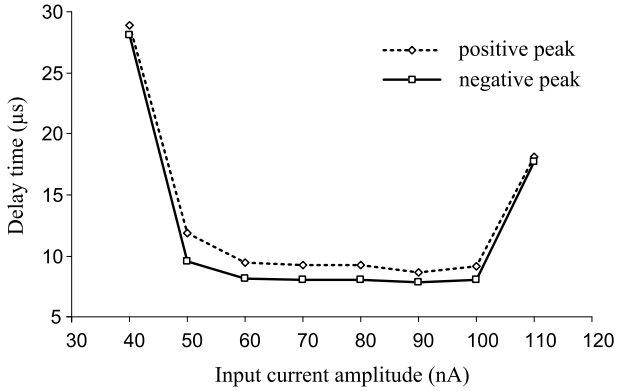

Figure 4.8: Delay time versus input current amplitude.

the voltages at the input nodes of the comparator are swinging up and down crossing each other within the first holding period after the peak occurred. This operation is consistent with the theory explained in Section 4.3.1 but, as we can see from the output waveform V_{out} shown in the bottom graph, the comparator produces an additional time delay. Also it can be seen that the delay time for the negative peak is slightly shorter.

In Fig. 4.8, it is indicated that the delay times of the PID circuit for both positive and negative peaks depend on the input amplitude. For very small input amplitudes less than 50 nA the proposed circuit gives a delay time bigger than 10μs which is 5% of the period of the input signal. This is due to limited resolution of the comparator. For the range of input amplitude of 50 nA to 100 nA, the delay time remains less than 5% of the input signal period. The delay time goes up again for the input amplitude higher than 100 nA. This is not because of a limitation of the comparator but of the SHA. As the internal voltage swings at the input of G_m go too high, the charge injection error cannot be completely cancelled out leading to a wrong decision of the comparator.

Since the mismatch in weak inversion is worse than in strong inversion, a Monte Carlo simulation has been performed to verify the circuit operation. For the same condition of the transient response shown in Fig. 4.7, with 300 runs, it gives the mean values (x) and standard deviation (σ) of 8.8 µs and 2.16 µs for the positive peak and x = 8.2 µs and σ = 2.4 µs for the negative

one. These numbers indicate that the delays spread around 5% of the input signal's period.

4.5 Conclusions

An ultra low-power PID designed for a PL-PP BE processor has been presented. The instants detected are delayed within less than one clock period even if the transistors' mismatch is taken into account. Either the rising or the falling edges of the output signal together with the input signal amplitude are expected to be used as control parameters in a stimulator for cochlear apical electrodes which operates in the frequency range of 300 Hz - 5 kHz.

Chapter 5

A charge balanced biphasic stimulator for cochlear implants

The output signal of the filter at each channel (Chapter 3) serves as the input of the peak-picking instant detector (Chapter 4). Either the rising or the falling edges of the output signal of the detector together with the input signal amplitude (the output of the filter) are expected to be used as control parameters in a stimulator for cochlear apical electrodes. To design stimulators that are implanted inside the body, there are very strict requirements on the size and power consumption of the device. Therefore it is important to be able to convey as much charge as possible into the tissue while using an as low as possible voltage supply to minimize power consumption.

This chapter presents a compact programmable biphasic stimulator for cochlear implants. By employing double-loop negative feedback, the output impedance of the current generator is increased, while maximizing the voltage compliance of the output transistor. To make the stimulator circuit compact, the stimulation current is set by scaling a reference current using a two stage binary-weighted transistor DAC (comprising a 3 bit high-voltage transistor DAC and a 4 bit low-voltage transistor DAC). With this structure the power consumption and the area of the circuit can be minimized.

5.1 Introduction

Since the stimulator is implanted inside the body, a small size and a low power consumption are critical requirements, especially if a large number of channels is preferred. Moreover, the circuit must be able to provide charge-balanced stimulation in order to prevent tissue damage [90]. A current mode stimulator seems to be an attractive method because the amount of charge injected into the tissue can easily be defined by the current amplitude and the duration of the pulses.

Several current mode stimulators have been reported thus far. Stimulators based on a current mirror circuit have been widely used [57, 91–99]. To maintain constant current stimulation, wide-swing and regulated cascode current mirror topologies are used but these limit the voltage compliance. Moreover, when using a dual supply with two current sources to create the stimulator, additional circuitry to match the two current sources is needed to ensure charge cancellation [92–94].

A voltage-controlled resistor based implementation has been presented in [95] to achieve a high voltage compliance but it needs additional circuitry to reduce non-linearity. A blocking capacitor free stimulator using dynamic current matching is a useful idea to reduce the size of the implant and preserve a charge error less than 6 pC [57]. However, a dual supply is used and additional circuitry is needed in this method.

Another issue is related to making the output current programmable. In many cases a digital-to-analog converter (DAC) is used to generate a programmable reference current [91–93], [96], [97]. Then, a current mirror replicating or scaling the reference current is used to provide the stimulation current. All these system blocks consume power and area. It has therefore been suggested to combine the DAC function into the output current stage in order to reduce the complexity and minimize the silicon area and power consumption [98]. This work has adopted this suggestion and tackles several other drawbacks mentioned in the previous paragraph.

In this chapter, a current mode, biphasic neural stimulator for application in cochlear implants is presented. It uses a compact stimulator circuit, avoids the use of external blocking capacitors by achieving a good charge balance

and thereby allows for an increase in the number of stimulator channels. By using a double-loop negative feedback topology, the output impedance of the current source can be maximized while only one effective drain-source voltage drop (V_{eff}) is required. This means that more voltage headroom at the tissue is achieved and more charge can be conveyed into the tissue.

5.2 Constant current stimulation

The principle of electrical stimulation is to activate neural cells by injecting a particular amount of charge into the tissue, either by using a constant voltage or a constant current. Since stimulation comes down to lifting the potential of the tissue either above or below a particular threshold and the tissue can be modeled as being merely capacitive in nature, stimulation entails inserting a particular amount of charge into the tissue. This makes charge the most fundamental quantity for neural stimulation. When charge is built up at the electrodes, electrolysis will start to occur at the interface, generating toxic by-products [90]. These toxic by-products will damage the tissue and therefore it is important to remove any charge built up at the electrodes after neuronal recruitment. Charge cancellation can be conveniently achieved by the stimulation scheme called constant current biphasic stimulation. The pulse of current is typically made up of equal-sized negative and positive phases, with the goal of delivering no net charge through the electrode at the end of the pulse [100].

In Fig. 5.1(a) the circuit principle for constant current stimulation is depicted. The stimulator uses a single supply and a single current source stimulation scheme. The switches allow the current to reverse its direction in between the two stimulation phases S_1 and S_2. The advantage of using switches over a topology using positive and negative current sources is that only a positive supply voltage is needed. To ensure charge cancellation, it is important that the current through the tissue remains constant during both stimulation phases. To maintain a constant current through the tissue, it is important to have a current source with an output impedance as high as possible.

The principle of constant current biphasic stimulation can be described using Fig. 5.1(b). The stimulation pattern is controlled by the switch array

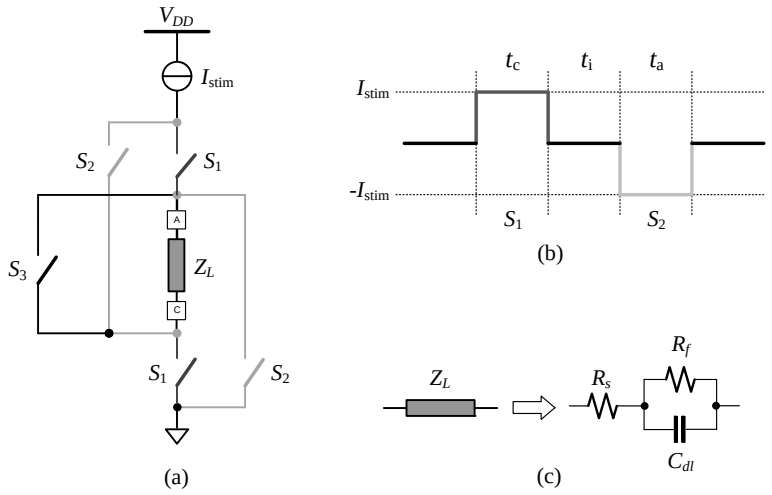

Figure 5.1: (a) Single supply stimulation scheme, (b) Biphasic stimulation waveform and (c) Electrode-tissue interface model.

comprising switches S_1, S_2, and S_3. When switches S_1 are closed (during t_c) the current flows from A to C. When switches S_2 are closed and S_1 are opened (during t_a) the current reverses its direction. An inter-phase delay (t_i) is added between the stimulation phases when switches S_1 and S_2 are opened. Switch S_3 is used to short circuit and thus passively discharge the tissue. The advantage of using a switch array for performing both anodic and cathodic current injection is that only a single voltage supply is needed. Also, since only one source is used, the currents are easily matched during both phases.

5.3 Electrode-tissue interface model

The load (Z_L) of the stimulator comprises the tissue and the electrode-tissue interface which can be modeled in the electrical domain. In this work a simple model is used as shown in Fig. 5.1(c) [101]. R_s corresponds to the resistance of the electrode leads and the tissue. In practice the resistance of the electrolyte (the tissue) will be much higher and is therefore the dominant component. C_{dl} and R_f correspond to the interface between the electrode

and the tissue. C_{dl} is the double-layer capacitance and R_f is the Faradaic resistance. For simplify, we assume that R_f remains large (>1 MΩ) during the stimulation pulse (< 100 μs), and can therefore be neglected. In cochlear implants, a typical RC series impedance presented by an electrode can be as high as 10 kΩ and 1 nF.

5.4 Design concepts

5.4.1 High output resistance current source

A straightforward implementation of a current driver uses a current mirror, which is often cascoded in order to have a sufficiently high output resistance [102]. Fig. 5.2(a) shows the simplest version of a PMOS cascode current mirror. A small reference current, I_{DAC}, generated from a digital to analog converter, is applied through diode connected transistors M_1 and M_4. Subsequently, the current is scaled up by a factor n to become the stimulation current, I_{stim}, flowing through transistors M_2, M_3, and load Z_L. In this case, the output resistance equals $g_{m3}r_{o3}r_{o2}$, where r_{o2} and r_{o3} are the output resistance of M_2 and M_3, respectively, $g_{m3}= \sqrt{2I_{D3}K_pW/L}$ is the transconductance of M_3, where I_{D3} is the drain current through M_3, K_p is the intrinsic transconductance, and W and L are the width and length of M_3, respectively. However, the minimum required voltage across the current source (voltage drop, V_d) becomes one source-gate voltage (V_{SG}) plus one effective source-drain voltage (V_{eff}). This limits the voltage headroom (V_L) and the amount of charge that can be conveyed to the tissue (load).

To increase V_L, a current mirror employing active feedback to boost the output impedance can be used. In Fig. 5.2(b), a high-gain amplifier, A_v, is applied to make the drain voltage of M_2 equal to the drain voltage of M_1. The same biasing condition makes I_{stim} n times I_{DAC}. The output resistance of the active feedback current generator is given by $A_v g_{m3}r_{o3}r_{o2}$. This causes V_d to become $V_{eff3} + V_{eff2}$. Due to the fact that the output resistance of this mirror is higher than in the previous cases but requires less V_d, this cascoded structure is popularly used in neural stimulation [92], [103].

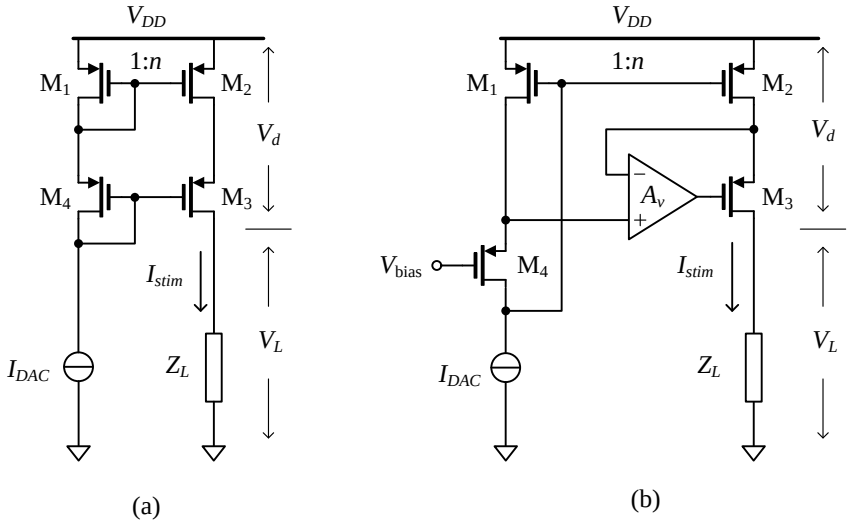

Figure 5.2: Cascode current sources (a) simple cascode (b) regulated cascade.

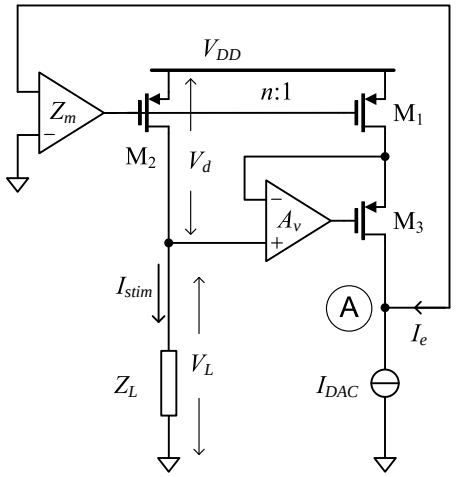

Figure 5.3: Proposed current source.

5.4.2 Proposed current source

In order to allow for an even higher V_L, we proposed a high output impedance current source that requires V_d to be only a single V_{eff} [25], [26]. The concept of the proposed current source is shown in Fig. 5.3. It contains two feedback loops. The first local one is used for high precision down scaling of I_{stim} (to I_{stim}/n). Transistor M_2 generates I_{stim} flowing through Z_L. The gate terminal of transistor M_1 is connected to the gate terminal of M_2 to accurately scale down the current flowing through M_3 to summing node A. Based on the same principle as used for the current mirror of Fig. 5.2(b), A_v is used to force the drain terminals of M_1 and M_2 to be equal, resulting in a very precisely copied current I_{stim}/n flowing into node A. This current will be compared with I_{DAC} and an error current, I_e, equal to

$$I_e = \frac{I_{stim}}{n} - I_{DAC}, \tag{5.1}$$

flows into transimpedance amplifier Z_m converting the very small I_e into the voltage needed at the gate of M_2 to produce I_{stim}. I_e will be forced to be zero by the large loop gain of the second global feedback loop creating a relationship of

$$I_{stim} = nI_{DAC}. \tag{5.2}$$

We can simplify the feedback block diagram of the proposed circuit as shown in Fig. 5.4. The loop gain of the system can be found to be

$$LG = \frac{G_{m2}Z_m}{n}, \tag{5.3}$$

where G_{m2} is the transconductance gain of transistor M_2.

To maintain the desired current given by (5.2), LG needs to be as large as possible. Since G_{m2} is limited by the values of I_{stim} and the dimension of M_2 and n is preferred to be high (10-100) to keep the total power consumption low, a large Z_m becomes the main factor that defines the accuracy of the proposed circuit.

The simulated output current versus the voltage headroom of the three current source designs V_L , the simple cascode (Fig. 5.2(a)), the regulated cascode (Fig. 5.2(b)), and the proposed circuit (Fig. 5.3) is shown in Fig. 5.5.

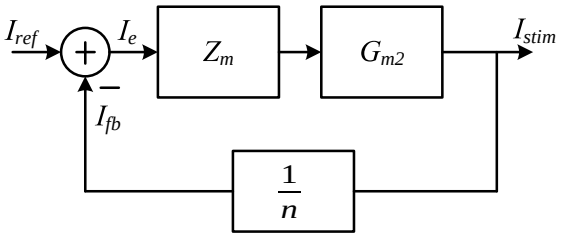

Figure 5.4: Feedback block diagram of the proposed current source.

AMS 0.18µm high-voltage technology parameters were used for circuit simulations. The simulation is performed using the same transistor dimensions for all three designs. A high voltage supply (>10 V) is needed to accommodate the maximum current required (1 mA) through the maximum load expected (< 20 kΩ). V_{DD} is set at 18 V and I_{DAC} is 50 µA, yielding I_{stim}=1 mA with a scaling factor of $n = 20$. Ideal op-amps with a gain $A_v = 200$ are used for the circuits in Figs. 5.2(b) and Fig. 5.3. V_L was varied from 0 to 18 V with a 0.5 V step size by using an ideal voltage source, as we can see the proposed current source achieves a larger voltage headroom than those of the others (see Fig.5.5). This verifies that the proposed current source can inject more charge into the tissue for the same supply voltage.

5.5 Circuit implementation

From the concept as described in the previous section, we have derived a programmable biphasic stimulator circuit for cochlear implants. The design aims to support the flexible electrode array as developed in the SMAC-It (Smart cochlear implants) project [104]. In order to reduce the size and parasitic capacitances of the stimulator output transistor (M_2), the proposed current source was modified as shown in Fig. 5.6. I_{stim} is created by scaling a reference current (I_{ref}) by scaling factors n and m of M_7 and M_2, respectively. Thereby I_{stim} becomes

$$I_{stim} = n \cdot m \cdot I_{ref}. \tag{5.4}$$

To make n and m programmable M_7 and M_2 are implemented using a binary weighted DAC scheme. The circuit diagram of the implemented stimulator circuit is shown in Fig. 5.7(a). This requires the use of high-voltage (HV)

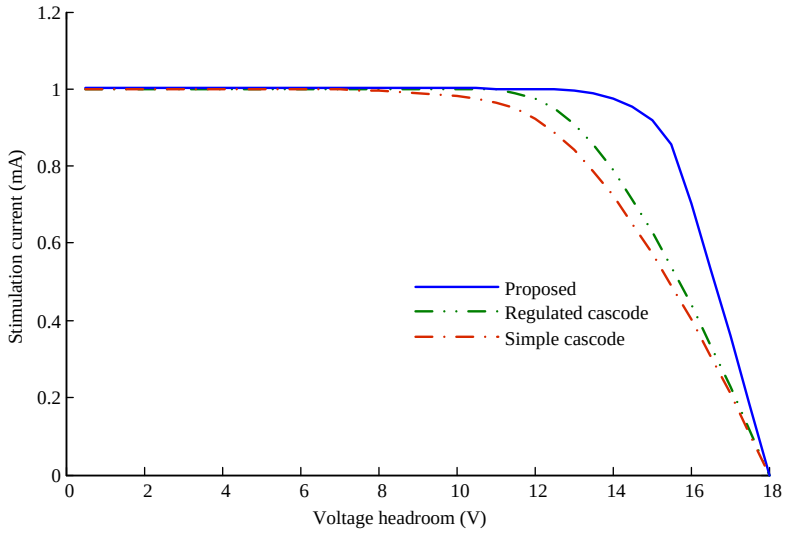

Figure 5.5: A comparison between the output characteristics of the current sources.

transistors (indicated by the thick drain terminal) combined with low-voltage (LV) transistors. To minimize the area occupied by the circuit, the number and size of HV transistors used should be as small as possible. The design of the individual sub-circuits will be described in the next subsections.

5.5.1 High-voltage and low-voltage DAC configuration

In order to create a 10 μA resolution for a 1 mA full-scale stimulation current, a 7-bit resolution is required. The silicon area of the circuit can be minimized when using two stages in cascade, a HV DAC and a LV DAC. The number of bits in the HV DAC should be as small as possible. This will reduce the number of (large) HV transistors resulting in a smaller area as well as a lower parasitic capacitance. However, a certain minimum equivalent transistor size is needed to be able to supply the maximum stimulation current. In our design 3 bits for the HV DAC was found to be optimal.

The remaining 4 bits can be implemented using LV transistors. These transistors are much smaller, making the area contribution negligible compared to the area occupied by the HV DAC. The reference current was chosen to

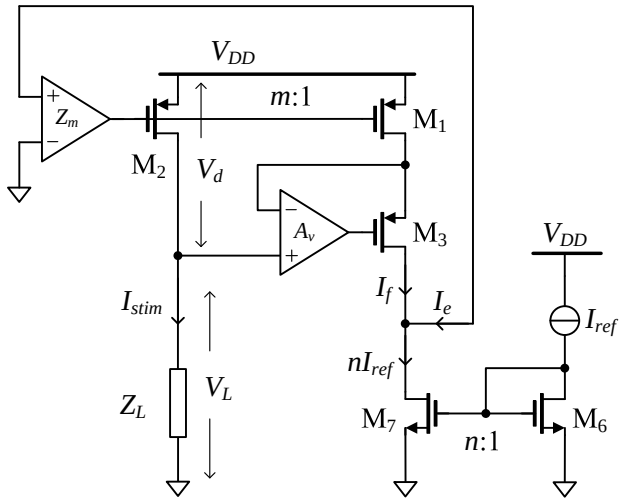

Figure 5.6: Modification of the proposed current source.

be $I_{ref} = 10$ µA. By enabling one or more transistors in the binary weighted DACs (using transistor switches), I_{stim} can be made programmable using the following relation :

$$I_{stim} = \left(\sum_{u=0}^{2} a_u 2^u\right)\left(\sum_{l=0}^{3} a_l 2^l\right) I_{ref}, \tag{5.5}$$

in which u and l are the bit-numbers of the enabled HV transistors M_2 and LV transistors M_7, respectively. In this way the LV DAC can generate a current in steps of 10 µA from 10 µA to 150 µA. The HV DAC can scale this current with a factor 1 up to 7, resulting in a maximum stimulation current of 1.05 mA.

5.5.2 Differential amplifier A_v

Amplifier A_v is used in the feedback loop to control the drain voltage of M_1. It is implemented using a standard differential amplifier (using HV transistors) with an active load as depicted in Fig. 5.7(b). An offset voltage source, V_{off}, is needed at the output of the amplifier to bias the gate of M_3 properly. It has been implemented using a diode connected LV transistor chain and current sources $I_s = 10$ µA. The minimum common mode input voltage that the amplifier can handle is about 3 V because of the biasing of

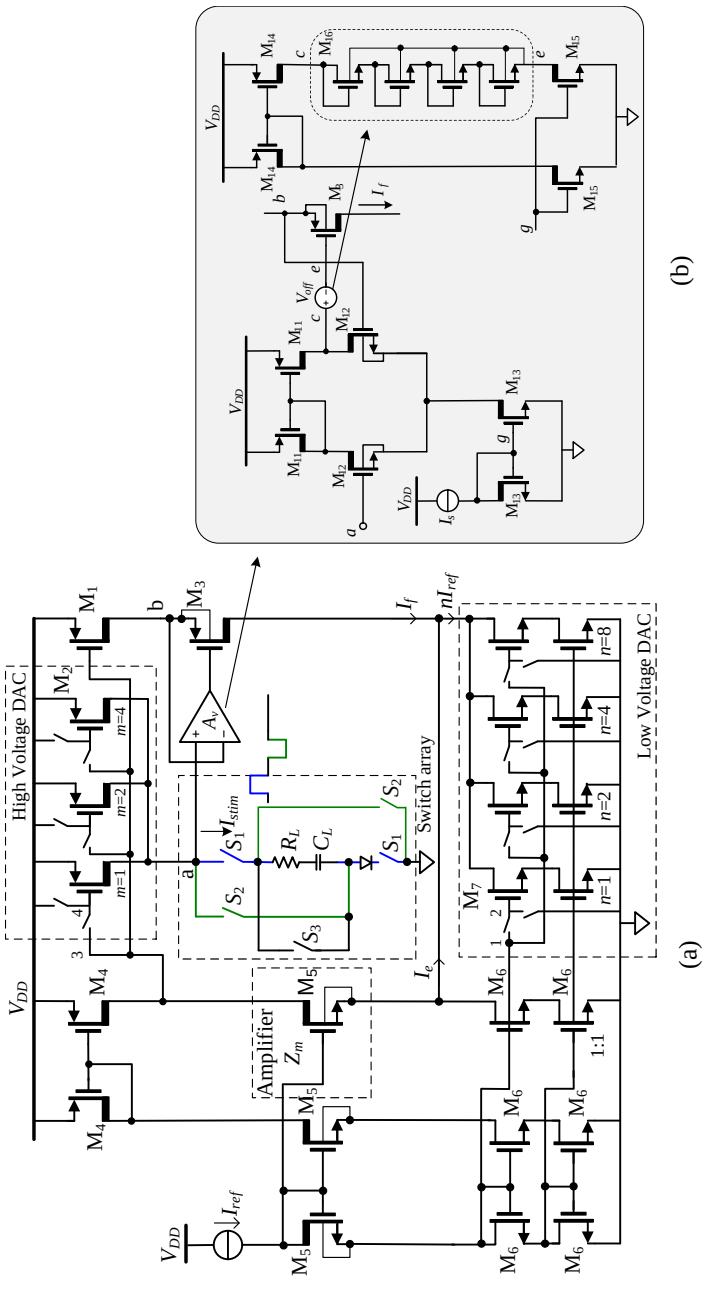

Figure 5.7: Principle circuit diagram of the implemented programmable biphasic stimulator circuit.

Table 5.1: Transistor dimensions

MOSFET	W [μm]	L [μm]
M_1, M_2(m=1), M_4, M_5, M_{11}, and M_{12}	5	5
M_6, M_7, and M_{16}(n=1)	0.5	0.18
M_{13}	5	0.4
M_3, M_{14}, and M_{15}	5	0.6

the LV DAC. When $V_a < 3$ V an error is introduced in the output current because $V_{DS,\mathrm{M}_2} \neq V_{DS,\mathrm{M}_1}$. However this error is small because $|V_{DS,\mathrm{M}_2}| \gg |V_{DS,\mathrm{M1}} - V_{DS,\mathrm{M2}}|$.

5.5.3 Switch array

The implemented switch array is shown in Fig. 5.8. The upper switches can be implemented using PMOS HV transistors. The minimum gate length (1.5 μm) permitted by the process was chosen to provide low on-resistance. A gate width of 50 μm was chosen. The lower switches are implemented using NMOS HV transistors. The gate lengths and widths were chosen 1.5 μm and 15 μm, respectively. It should be noted that at node n the voltage with respect to ground can become negative because of the charging of C_L and the subsequent reversed current direction during the charge cancellation phase. Therefore a substrate isolated Schottky diode is placed in series to prevent leakage between the substrate and the drain of the transistor. Switch S_3 is implemented using back-to-back PMOS transistors with their source terminals biased at V_{DD}. The back-to-back configuration is necessary in order to allow for current flow in both directions. Finally, a standard cross-coupled level shifter is used to convert a LV control signal into a HV control signal,$V_{control}$ [105]. The dimensions of the transistors are indicated in Table 5.1 and were selected to suit their application in fully implantable cochlear implants.

5.6 Measurement results

The stimulator circuit has been implemented in AMS 0.18 μm HV CMOS technology. The active area is approximately 200 μm × 210 μm. The layout

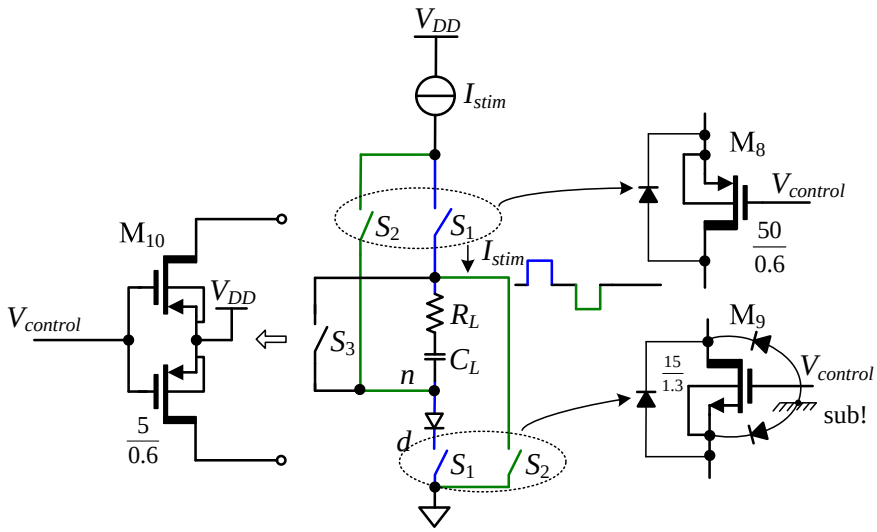

Figure 5.8: Switch array.

capture and the micrograph of the chip are depicted in Fig. 5.9(a) and Fig. 5.9(b), respectively. From the layout it can be seen that the HV transistors dominate the area. The area was minimized by implementing multiple HV transistors in the same deep n-well whenever possible, e.g. in the HV DAC.

The measurement setup is presented in Fig. 5.10. An external 18 V supply is used for the main circuit. A 5 V supply is used for powering the pad ring of the chip. The control of the HV and LV DACs were set by DIP switches. I_{ref} and I_s were set at 10 µA by a Keithley 6430 Sub-Femtoamp source meter. Finally, 5 digital outputs from an Arduino UNO microcontroller board were used in order to control the timing and current direction of the switch array.

5.6.1 Output DC characteristics

First the accuracy of the stimulation current was measured. For this, the load was chosen to be a single resistor R_L=10 kΩ without a capacitor. The output current was measured using a Keithley 6430 Sub-Femtoamp source meter. Fig. 5.11 shows the measured output current versus full-scale digital input code for the positive and negative stimulation direction, respectively.

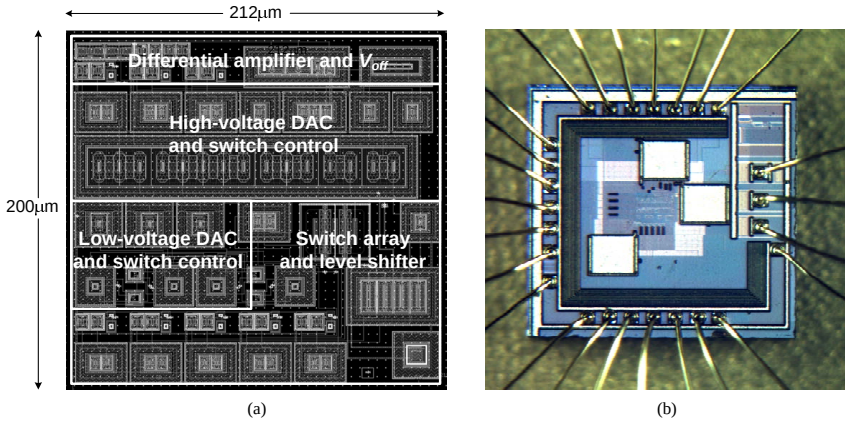

Figure 5.9: (a) Layout capture and (b) micrograph.

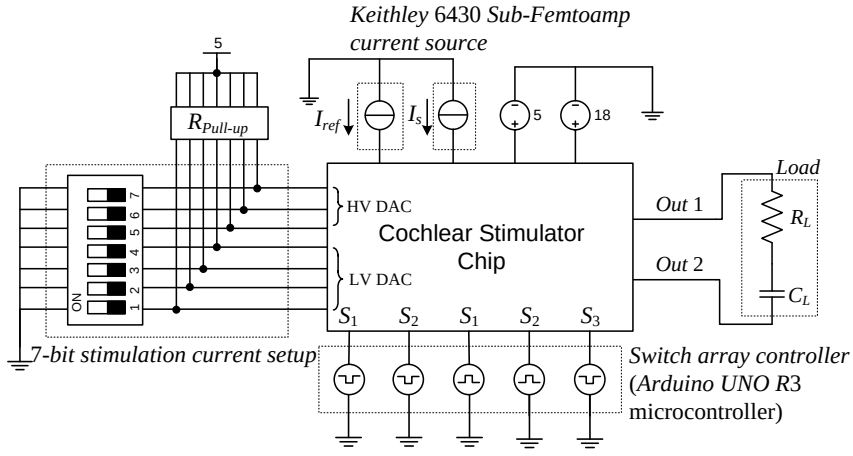

Figure 5.10: Measurement setup.

The current values in both positive and negative directions are almost identical, which is required for proper charge balancing. The percentage of current mismatch is 0.02% and 0.3% at the minimum and maximum output current, respectively. The current mismatch mostly occurred at large output currents. This is because of the effect from the threshold voltage of the Schottky diode at the positive direction.

The measured output current versus output voltage at several stimulation current levels is shown in Fig. 5.12. The output voltage was varied from 0 to 18 V with a 0.5 V step size by using a Keithley 6430 Sub-Femtoamp source meter as a voltage source. The voltage headroom is about 12.5 V and 16.5 V at maximum and minimum stimulation current, respectively. This value is mainly limited due to the relatively small dimensions of the HV DAC transistors. The voltage headroom can be increased by increasing the width of the HV DAC transistors. Moreover, the voltage headroom also depends on the voltage across the switch array. This voltage is related to the dimensions of the HV switch transistors in order to allow the maximum stimulation current to pass through. In this design it also depends on the voltage across the Schottky diode. This diode has a small (0.4 V) voltage drop.

The output resistance calculated from the measurement results plotted in Fig. 5.12 is about 33 MΩ and 500 kΩ at I_{stim}=10 μA and 1.05 mA, respectively.

5.6.2 Biphasic stimulation

Next, the chip was measured while providing a programmable biphasic stimulation current in the range of I_{stim}=10 μA (minimum) to 1.05mA (maximum). The digital outputs from the microcontroller board are used to control the timing of the biphasic waveform. The pulse widths of t_a, t_i and t_c were set to 50 μs, and the total cycle time to 600 μs. The measured output voltages for I_{stim}= 50 μA and 1.05 mA across a 10 kΩ resistive load are shown in Fig. 5.13.

Fig. 5.14, Fig. 5.15, and Fig. 5.16 show the measured biphasic output voltages for three amplitudes of I_{stim} across a 1kΩ+10nF (minimum), 10kΩ+1nF

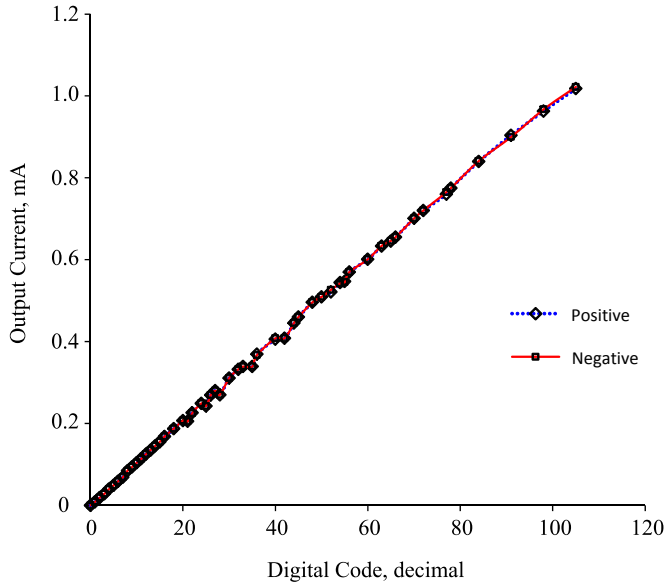

Figure 5.11: Output current in the positive and negative stimulation direction.

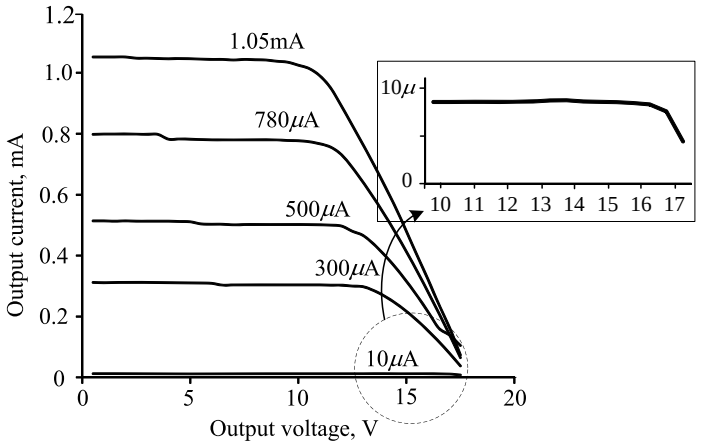

Figure 5.12: Measured output characteristic of the stimulator.

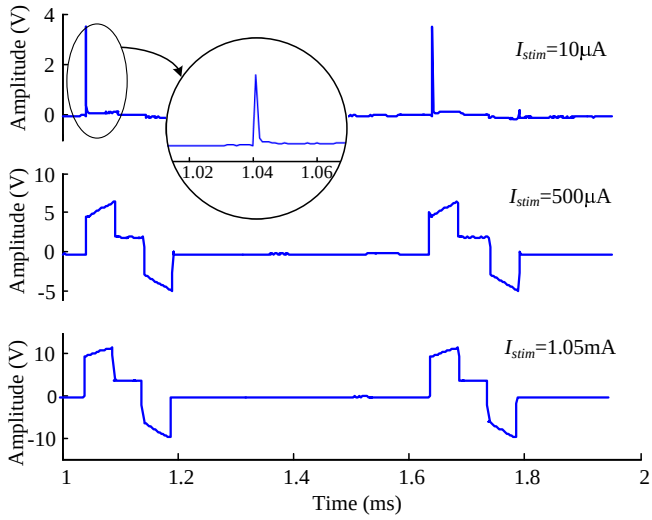

Figure 5.13: Biphasic output voltage.

(maximum), and 10kΩ+10nF (typical) load, respectively. These measurement results show that the stimulator can be used with a wide range of electrode-tissue impedances. Note that for the minimum load (Fig. 5.14) the output voltage at I_{stim}=10 µA is not shown because it is very small. In Fig. 5.15, the stimulation time has changed to 10 µs in order to prevent voltage clipping. The spikes due to switching, and consequently settling of the stimulator current sources, (see the magnified output voltage in Fig. 5.15 and Fig. 5.16) do not contribute to significant charge mismatch, as will be discussed in the next section.

In order to test the stimulator in a realistic situation, the load was changed to a CI electrode array in 0.9% saline solution. Clarion HiFocus Cochlear electrodes were used. These are platinum iridium electrodes, produced by Advanced Bionics, used for studies in animal cochleae and each electrode has an area of approximately 0.2 mm^2. Fig. 5.17 shows the measured output voltage across the two electrode sites at I_{stim}= 500 µA, and 1.05 mA. As can be seen from Fig. 5.17, the circuit works as expected. The output voltage at the end of each stimulation cycle remains constant and goes to zero without creating any voltage accumulation.

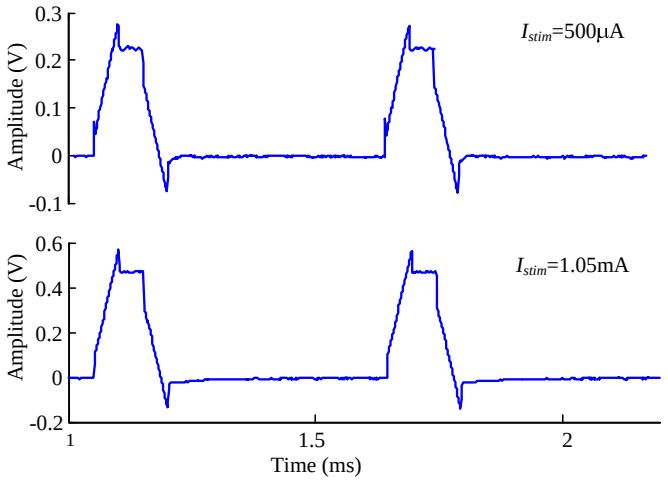

Figure 5.14: Output voltages for a 1kΩ+10nF load.

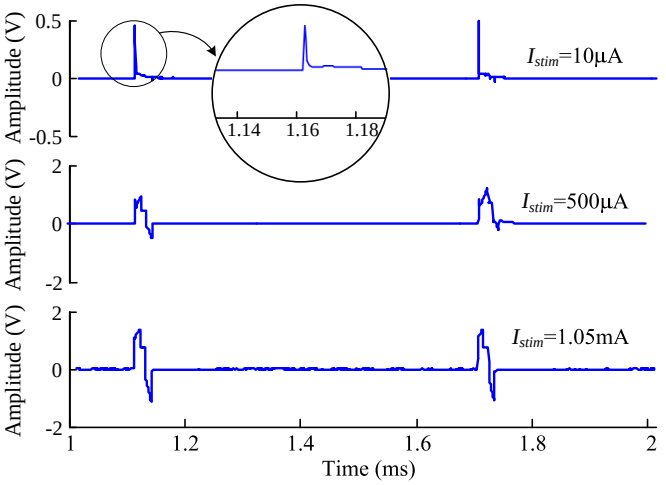

Figure 5.15: Output voltages for a 10kΩ+1nF load.

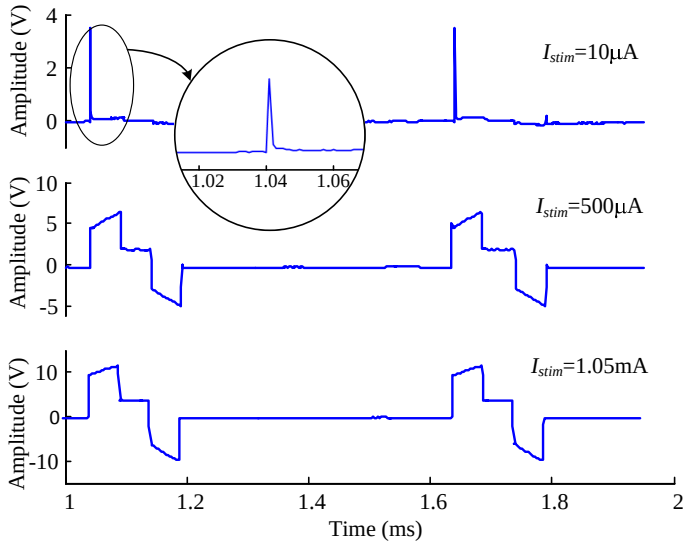

Figure 5.16: Output voltages for a 10kΩ+10nF load.

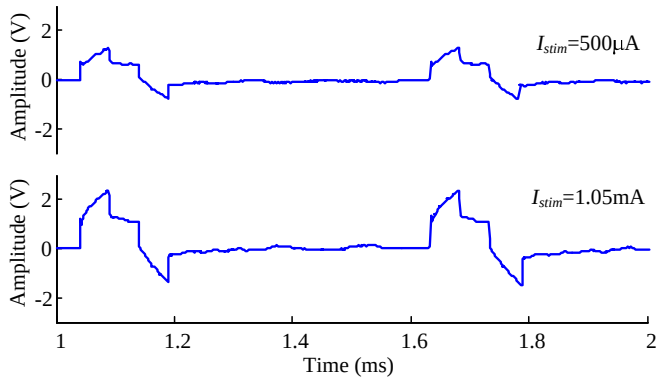

Figure 5.17: Output voltages for CI electrode load in 0.9% saline solution.

Table 5.2: Charge error and dc current error for R_L=10 kΩ, C_L=10 nF.

Stimulation current	Charge error	DC current error
10μA (50μs)	0.50pC	0.83nA
500μA(50μs)	0.45pC	0.75nA
1.05mA (10μs)	1pC	1.60nA

5.6.3 Charge error

The residual voltage ($V_{residual}$) at the end of the stimulation cycle has been measured to determine the remaining charge imbalance. It was measured by connecting an instrumentation amplifier (AD826) in parallel with C_L. The output of the amplifier was connected to a 20-bit analog to digital converter (ADC) card (APPLICOS model ATX7006). A shielding enclosure (ground connected Faraday cage) was used to reduce the amount of noise picked up from the environment. A computer running APPLICOS ATXView software was used to acquire, store and analyze the data. The average DC offset voltage and noise in the data acquisition hardware was measured before each residual voltage measurement and subsequently subtracted from the acquired data. The charge error can be calculated by multiplying the measured residual voltage at the end of stimulation cycle with the capacitive load value ($Q_{error} = C_L V_{residual}$). The dc current error is subsequently determined by dividing the charge error by the stimulation cycle time ($I_{dc} = Q_{error}/t_{stim}$). Table 5.2 shows the computed charge errors and dc current errors for several values of I_{stim} at 10kΩ+10nF load. The pulse width was set to 50 μs and the stimulation cycle to 600μs. For I_{stim}=1.05 mA the pulse widths t_c and t_a were chosen to be 10 μs to prevent clipping of I_{stim}. The results show that the charge error and DC current error stay well below the safety limits. The specified industry limit on current mismatch in cochlear implants is 25 nA [106].

5.6.4 Current and power efficiency

For the maximum output current (I_{stim}=1.05 mA) through the maximum load (R_L = 10 kΩ) the current efficiency (defined by the ratio of the load current and the supply current) is 87% as shown in Fig. 5.18. The maximum power efficiency is found to be 61%. The power consumption is dominated by the bias sources in the differential amplifier (30 μA) and the current through

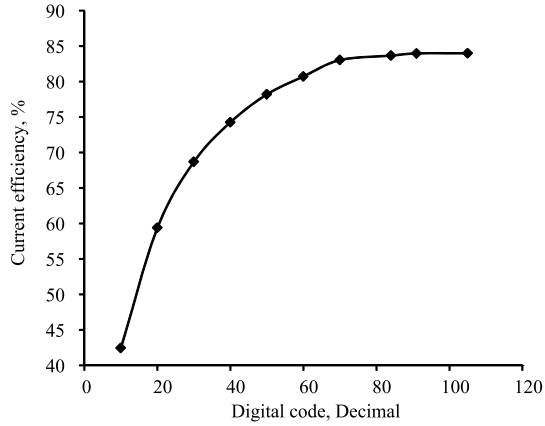

Figure 5.18: Current efficiency.

the DACs, depending on the number of bits enabled in the LV DAC (ranging from 40∼158 μA). The measured quiescent current is 210 μA which is limited by the biasing of M_3. Note that all these bias sources can be switched off when stimulation is not active, yielding very low static power consumption.

5.6.5 Multichannel operation

The proposed stimulator can be used for multichannel stimulation as shown in Fig. 5.19. The reference circuit provides biasing quantities for the LV DAC, HV DAC and amplifier Z_m, which can be shared among stimulation channels. The control logic for setting the 7 bit current amplitude and 3 bit current direction/pulse width are received from a programmable controller.

5.7 Conclusions

A compact programmable biphasic stimulator chip for cochlear implants has been presented in this chapter. A double loop negative feedback topology was employed to increase the output impedance. The circuit can deliver stimulation amplitudes in the range of 10 μA∼1.05 mA for a wide range of electrode-tissue impedances: R_L=1kΩ∼10kΩ, C_L=1nF∼10nF. The current error (< 1.6 nA) was found to be well below the safety limits. It consumes

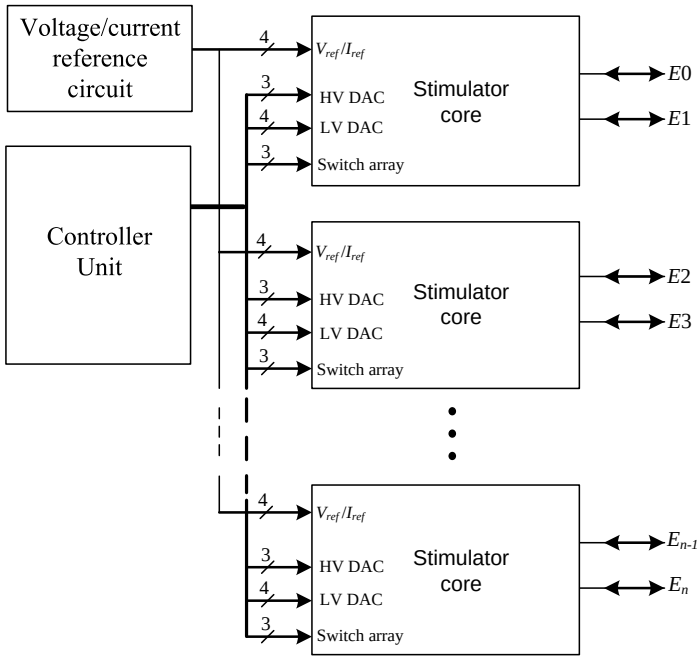

Figure 5.19: Multichannel stimulator.

a very small chip area ($0.042\,\mathrm{mm}^2$) allowing for many stimulation channels on a single die.

Chapter 6

Conclusions and future work

This thesis describes the electronic circuit design of various modules for application in CIs in order to save area, consume less power and ultimately moving towards a totally implantable CI. Besides that, the design process also considers how to convey correct information to the cochlea by means of a speech processing strategy which is suitable for a small and low-power CI.

6.1 General conclusions

Miniaturizing area and reducing power consumption of cochlear prosthetic devices is strongly required for full implantation. In **Chapter 2**, several speech encoding strategies were studied and compared in order to develop a compact speech processor that allows for full implantation and is able to convey both time and frequency components of the incoming speech to a set of electrical pulse stimuli. The study covers the widely recognized continuous time interleaved sampling (CIS) algorithm and strategies that convey the temporal fine structure (TFS) including race-to-spike asynchronous interleaved sampling (AIS), phaselocking (PL) using zero-crossing detection (ZCD), and PL using a peak-picking (PP) technique. To estimate the performance of the four systems, a spike-based reconstruction algorithm has been employed to retrieve the original sounds after being processed by these strategies. The correlation factors between the reconstructed and original signals imply that strategies conveying TFS outperform CIS. Among them, the peak picking technique combines good performance with great compactness since envelope detectors are not required.

According to physiological experiments, the envelope and phase of speech signals are required to enhance the perceptive capability of a cochlear implant processor. In **Chapter 3**, the design of an analog complex gammatone filter is introduced in order to extract both envelope and phase information of the incoming speech signals as well as to emulate the basilar membrane spectral selectivity. The gammatone impulse response is first transformed into the frequency domain and the resulting 8^{th}-order transfer function is subsequently mapped onto a state-space description of an orthonormal ladder filter. Using this approach, the real and imaginary transfer functions that share the same denominator can be extracted using two different **C** matrices. This results in a compact filter structure. The proposed filter is designed using $G_m - C$ integrators and subthreshold CMOS devices in AMIS 0.35 μm technology. Simulation results using Cadence RF Spectre confirm the design principle and ultra low power operation.

Chapter 4 demonstrates the design of a subthreshold CMOS peak-instant detector (PID) to be used in an analog CI speech processor based on the result from Chapter 2. The detector is formed by a nano-power sample and hold amplifier (SHA) and a voltage comparator to perform the detection of occurrences of maximum and minimum values of the input signal. The proposed detector can be operated from a 1.2 V supply and consumes less than 1 μW static power for detecting a 5 kHz input signal. This PID extracts amplitudes at the relevant moments that the peaks occur which is equivalent to the amplitude extracted by Hilbert transformation but in this case a power consumption of less than 1 micro-watt per channel is obtained. The output signals (amplitude and time) of the PID can be used as control parameters in a stimulator.

Chapter 5 discusses a novel method to maximize the charge transfer for constant current neural stimulators. By employing double-loop negative feedback, the output resistance of a MOS current mirror circuit is increased and the circuit requires only one effective drain-source voltage drop. The proposed circuit requires a few additional current branches to form two feedback loops. With its compact structure, the main benefit we achieve for neural stimulation is the larger amount of charge that can be conveyed to the stimulation electrode. In other words, for the same amount of charge required, the supply voltage can be reduced. From this concept, we have also designed a compact programmable biphasic stimulator for cochlear implants.

To make the stimulator circuit compact, the stimulation current is set by scaling a reference current using a two stage binary-weighted transistor DAC (comprising a 3 bit high-voltage transistor DAC and a 4 bit low-voltage transistor DAC). With this structure the power consumption and the area of the circuit can be minimized. The current error was found to be well below the safety limits. It consumes a very small chip area ($0.042\,\mathrm{mm}^2$) allowing for many stimulation channels on a single die.

6.2 List of scientific contributions

The outcomes of the research work in this thesis can be summarized as follows:

- A subthreshold $G_m - C$ complex gammatone filter has been designed and verified by circuit simulations in AMIS 0.35 μm technology. The filter provides both real and imaginary outputs that can be used to extract both envelope and phase information of the incoming speech signals.

- An ultra low-power, robust, compact, discrete-time peak instant detector (PID) has been designed to be implemented in AMIS 0.35 μm technology to support the PL-PP CI processor. This design employs a weak-inversion sample and hold circuit and a comparator in order to extract amplitudes at the relevant moments that the peaks occur which is equivalent to the envelope extracted by Hilbert transformation. Moreover, in this case the proposed detector can be operated from a 1.2 V supply and consumes less than 1 μW static power for detecting a 5 kHz input signal.

- A least-voltage drop high output resistance current source for neural stimulation has been introduced and verified by circuit simulation in AMIS 0.35 μm technology. This concept requires a few additional current branches to form two feedback loops to increase the output resistance of a MOS current mirror circuit that requires only one effective drain-source voltage drop. With its compact structure, the proposed circuit is suitable as a current generator for neural stimulation.

- A compact programmable biphasic stimulator for cochlear implants has been designed. The proposed circuit has been implemented in AMS

0.18 µm high-voltage CMOS IC technology, using an active chip area of about 0.042 mm^2. Measurement results show that proper charge balance of the anodic and cathodic stimulation phases is achieved and a dc blocking capacitor can be omitted. The resulting reduction in the required area makes the proposed system suitable for a large number of channels on a single die.

6.3 Future research directions

The following items can be studied and/or developed further:

- Starting from the complex waveforms obtained from the complex gammatone filter in Chapter 3, we can realize the envelope information by taking the square root of the sum of the real output squared and the imaginary output squared. We can obtain the phase information by computing the arctangent of the ratio of the imaginary and the real outputs. Both envelope and phase information are useful for realizing a speech processing strategy that contains TFS. However, additional circuitry to implement these nonlinear functions will cause a higher power consumption to the system.

- The PID in Chapter 4 requires the output from the BPF at each channel for processing. So, if we do not require a specific BPF characteristic like that of a gammatone filter for realizing a speech processing strategy, this detector can be implemented with another type of BPF, for example the nanopower 4^{th}-order BPF presented in [107]. A very compact and low-power system can be expected.

- As several electronic CI modules in this thesis have only been used in a stand-alone fasion, future work should combine all modules together and implement them in the same technology, including the design of the logic controller for the system. Then, an evaluation of the area and power consumption using a multichannel topology can be performed.

- The analog CI processor presented in this thesis can be combined with a readout system that is able to read out the neural response already during stimulus and artifact [108]. This makes the system complete

with a neural recording system that can perform superior data analysis and adjust the stimulation strategy in a closed-loop fashion.

- A single component failure analysis of the stimulator circuit should be considered. A monitoring circuit can be added in order to make sure that the stimulator is switched off when a component failure takes place causing unbalanced stimuli and/or dc currents being applied to the tissue.

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List of Publications

1. **W. Ngamkham**, M. N. van Dongen, W. A. Serdijn C. J. Bes, J. J. Briaire, and J. H. M. Frijns, "A 0.042 mm^2 Programmable Biphasic Stimulator for Cochlear Implants Suitable for a Large Number of Channels," in *arXiv.org*, arXiv:1502.00549, Jan. 2015.
2. C. Sawigun, **W. Ngamkham** and W. A. Serdijn, "A 0.5 V, 2 nW, 55 dB-DR, Fourth-Order BPF Using Single Branch Biquads: An Efficient Design for FoM Enhancement" *Microelectronics Journal*, vol. 45, pp.367-374, April 2014.
3. N. S. Lawand, **W. Ngamkham**, G. Nazarian, P. J. French, W. A. Serdijn, G. N. Gaydadjiev, "An improved system approach towards future cochlear implants, in *Proc. IEEE Engineering in Medicine and Biology Society (EMBC)*, Osaka, Japan, July 2013.
4. **W. Ngamkham**, M. N. van Dongen and W. A. Serdijn,"A Charge Balanced Biphasic Stimulator for Cochlear Implants," invited presentation, *BME 2013*, Egmond aan Zee, the Netherlands, Jan. 24-25, 2013.
5. C. Sawigun, **W. Ngamkham**, and W. A. Serdijn, "A 2.6 nW, 0.5 V, 52 dB-DR, 4th-order Gm-C BPF: Moving Closer to the FoM's Fundamental Limit," *in Proc. IEEE International Symposium on Circuits and Systems (ISCAS)*, Seoul, South Korea, May 20-23, 2012, pp. 656-659.
6. **W. Ngamkham**, M. N. van Dongen, and W. A. Serdijn, "Biphasic Stimulator Circuit for a Wide Range of Electrode-Tissue Impedance Dedicated to Cochlear Implants," *in Proc. IEEE International Symposium on Circuits and Systems (ISCAS),* Seoul, South Korea, May 20 - 23, 2012, pp. 1083-1086.
7. **W. Ngamkham**, Marijn van Dongen, Wouter A. Serdijn: An Implementation of Least-Voltage Drop Stimulator Circuit for Cochlear Implants, Book of Abstracts, ICT.Open, Rotterdam, the Netherlands, October 22-23, 2012.
8. **W. Ngamkham**, C. Sawigun and W. A. Serdijn, "The design of an ultra low-power analog bionic ear," invited presentation, *BME 2011*, Egmond aan Zee, the Netherlands, Jan. 20, 2011.
9. C. Sawigun, **W. Ngamkham**, and W. A. Serdijn, "A least-voltage drop high output resistance current source for neural stimulation," in *Proc. IEEE Biomedical Circuits and Systems Conference (BioCAS)*, Paphos, Cyprus, Nov. 2010, pp. 110-113.

10. C. Sawigun, **W. Ngamkham**, and W. A. Serdijn, "An ultra low-power peak-instant detector for a peak picking cochlear implant processor," in *Proc. IEEE Biomedical Circuits and Systems Conference (BioCAS)*, Paphos, Cyprus, Nov. 2010, pp. 222-225.

11. C. Sawigun, **W. Ngamkham**, and W. A. Serdijn, "Comparison of speech processing strategies for the design of and ultra low-power analog bionic ear," in *Proc. IEEE Engineering in Medicine and Biology Society (EMBC)*, Buenos Aires, Argentina, 2010, pp. 1374-1377.

12. **W.Ngamkham**, C.Sawigun, S.Hiseni, and W.A.Serdijn, "Analog complex gammatone filter for cochlear implant channels," in *Proc. IEEE International Symposium on Circuits and Systems (ISCAS)*, Paris, France, May 2010, pp. 969-972.

13. S. Hiseni, C. Sawigun, **W. Ngamkham**, and W. A. Serdijn, "A Compact, Nano-Power CMOS Action Potential Detector", In *Proc. IEEE Biomedical Circuits and Systems Conference (BioCAS)*, Beijing, China, Nov. 26-28 2009.

About the Author

Wannaya Ngamkham was born in Nong Prue, Thailand on August 23rd, 1972. She received the B. Eng and M. Eng. both in electrical engineering from Mahanakorn University of Technology (MUT), Bangkok, Thailand, in 1995 and 2001, respectively. From 1995-2008 she was a lecturer at the Department of Control Systems and Instrumentation, MUT. In November 2008, she joined the Section Bioelectronics of the Department of Microelectronics, Faculty of Electrical Engineering, Mathematics, and Computer Science, Delft University of Technology (TUDelft), the Netherlands, where she started her research towards her Ph.D. degree. Her research is part of the STW funded SMAC-It project (Smart Cochlear Implants). Her research interests include low power analog integrated circuits and system designs for totally implantable cochlear implants.