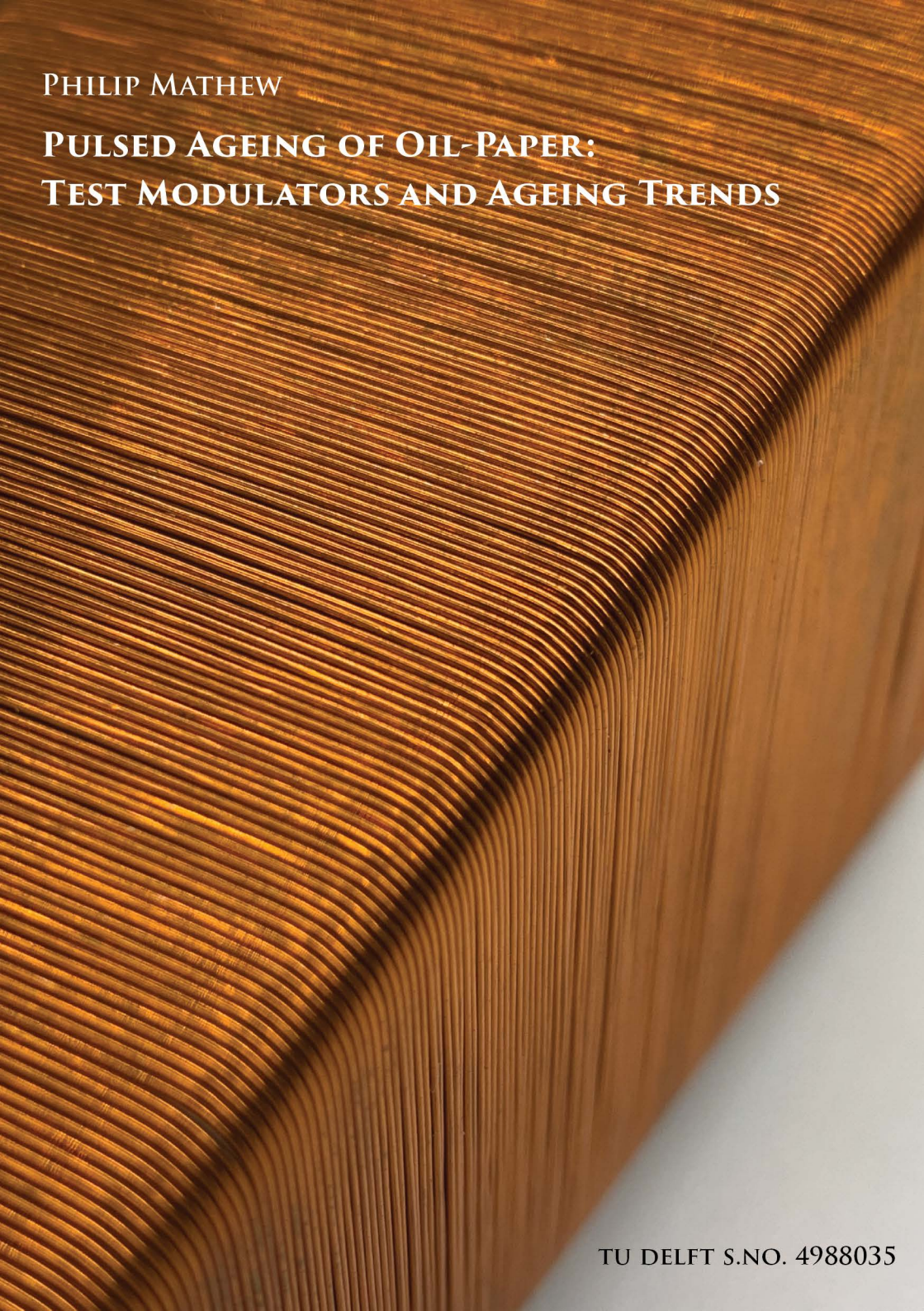
Philip Mathew

Pulsed Ageing of Oil-Paper: Test Modulators and Ageing Trends



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THESIS REPORT

PULSED AGEING OF OIL-PAPER: TEST MODULATORS AND AGEING TRENDS

by

Philip Mathew

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Pulsed Ageing of Oil-Paper: Test Modulators and Ageing Trends

For Mama, Dada, and Nonie.

ABSTRACT

The ambitious transition towards a renewable future is being made possible by power electronic systems that facilitate effective control and efficient conversion of energy. One such system is the solid-state transformer (SST) which aims to replace conventional transformers by offering larger energy densities and flexible power flow. However these benefits come at the cost of severe mixed-frequency stresses experienced by the medium frequency transformer (MFT) of the SST. These stresses are characterised by fast-rising pulsed waveforms of several tens of kilovolts repeating at frequencies of up to hundred kilohertz. In contrast to pure sinusoids, the behaviour of dielectrics under mixed-frequency stresses is to a large extent unknown. This research gap forms the core motivation behind this thesis project.

To analyse these exciting yet extreme phenomenon, the first objective was to build a pulse modulator for testing cellulosic dielectrics under voltages up to 10 kV with rise-times $\approx$ 2 µs at frequencies between 10 to 50 kHz. The topology consists of a rectified DC supply feeding a SiC H-bridge pulse generator connected to a 4:200 pulse transformer and other variable test elements. The work began with selecting the switch and gate driver, simulations in LTspice and TINA-TI, and the fabrication of the PCB pulse generator prototype using Altium Designer. Next, a novel third-order PQR equation was derived for a PT with capacitive load involving the parasitic leakage flux L_σ and distributed capacitance C_d. The influence of bobbin geometry on parasitics was studied with 20 different 3D printed iterations designed in Fusion 360. A failure mode analysis was conducted to identify weak points in a transformer, and the solutions detailed in this report.

The final objective was to apply the produced waveforms of $T_r \approx 1.8\mu s$ across single-layer OIP samples at 10 kHz and 50 kHz. The sample strength was determined through ramp tests with 1 kV/s slope. The lifetime curves were obtained by performing ageing tests at 10 field strengths each for 21-41 samples, and fitting the median failure time into a inverse power law model. The results show a clear reduction in lifetime at higher frequencies proving the unsuitability of OIP in its current form as an insulation for MFTs. A transition point was observed indicating a shift in ageing mechanism at lower fields. The report ends with a discussion on future scopes of research.

ACKNOWLEDGEMENTS

In a countless number of ways, the past two years have changed me more than I could have ever prepared for. Studying at the TU Delft has been wholesome in every sense, academic and otherwise, and I am grateful for the opportunity to have carried out my masters in this beautiful country.

I owe the culmination of this thesis to several individuals and elements.

Firstly, to *the scientific truth*, for humbling me to the core (pun intended) with its brutal honesty. I have felt it crush my hopes with every fried MOSFET, failed experiment, and seemingly unsolvable problem. But every dead-end has brought another chance to build in me the patience to repair, the will to rethink, the wisdom to reason, and the warmth of rationale. Research has proven to be like incomplete alliteration, a perfect imperfection.

To *Mohamad Niasar*, for educating me on the importance of failures and the lessons to be learnt from them. Your passion for the subject has been the greatest inspiration for me to turn every stone and push every limit. The late evenings we spent working at the lab were genuinely fun, two nerds delving into physics and mathematics to understand our observations. I am grateful to have had you as a mentor, teacher, and friend. I aspire to become for students what you were for me, supporting them just enough to promote original and independent ideas. I look forward to joining forces on more scientific adventures, or at least start a repair shop for PCBs.

To *Peter Vaessen*, for introducing to me the field of high-voltage engineering, and enthusiastically teaching it to me as a beautiful amalgamation of physics, chemistry, mechanics, and a good amount of common-sense.

To *Wim*, for his energy to strive for perfection in the tiniest of details. And to *Luis, Geert Jan, and Radek*, for helping me make the most out of our HV lab.

To *Dhanashree, Tianming, Weichuan, and Christian*, for being approachable to have intellectual discussions about our projects, which have played a significant role in exciting me about pursuing a PhD in the future.

To *Mama and Dada*, for teaching my sister and I the value of education, culture, and genuine hardwork. I am so proud to be your son, that every sleepless night spent has partly been to make you proud to be my parent.

To *Nonie*, for being my sister. Although you spent your first four (tragic) years without me, I pray that I never have to spend a single day without you.

To *Keeka*, for being my raccoon through chonk and thin, for the paws of app-woval that supported me the past two years, and for being merciful towards apple peels. To *CoeurdeLion and Zangetsu*, for being my fellow guardians, siegers, and racers. To *Sai*, for being a constant friend in need, and the best SSD board-mate indeed. To *Meenu*, for the food truck lunches and positive encouragement. To my *classmates*, for providing me the fondest of memories.

To *my teachers*, from high-school to bachelors to masters and more, for their sincerity in fostering the courage to follow my curiosities and ambitions.

To *strawberry yoghurt and muesli*, for keeping me healthy and happy, two aspects of life I tend to ignore. To my *iPhone*, for providing photos worth oggling at and to my *laptop*, for not giving up on me. Lastly to *cellophane tape* and *copper tape*, for fixing too many problems that I have lost count of.

The stochasticity of this universe has instilled in me time after time a fire to answer its endless questions, to teach others the answers to these questions, and to eagerly work together on searching for new puzzles to solve.

With joy in my soul, and a cat on my lap.

Philip Mathew
Delft, 2021

CONTENTS

NOTATION

PHYSICAL CONSTANTS

SYMBOL	VALUE	UNIT	DESCRIPTION
c	$2.997\,924\,58 \times 10^{8}$	m/s	Speed of light in Vacuum
ϵ_0	8.854×10^{-12}	F/m	Permittivity of Free Space
μ_0	$4ß10 \times 10^{-7}$	H/m	Permeability of Free Space
q_e	1.602×10^{19}	C	Elementary electrical charge

FREQUENTLY USED SYMBOLS

V_{peak}	Pulse peak amplitude in kilovolts
V_{pk-pk}	Pulse peak-to-peak amplitude in kilovolts
ΔV_o	Pulse overshoot in % V_p
T_r	Pulse rise time in nanoseconds
T_f	Pulse fall time in nanoseconds
T_p	Pulse top width in nanoseconds
L_σ	Leakage inductance in milli/micro-henries
C_d	Distributed capacitance

FREQUENTLY USED ABBREVIATIONS

SST	Solid-state transformer
MFT	Medium frequency transformer
PDs	Partial discharges
PDIV	Partial discharge inception voltage
OIP	Oil-impregnated paper
PT	Pulse transformer
SiCFET	Silicon-carbide Field-effect transistor

1

INTRODUCTION

The consequences of a failure in an electric power system are tremendous and high reliability and a long voltage life of its components are absolute musts.

F. H. Kreuger
Industrial High DC Voltage (1995)

The first chapter of this thesis begins by setting the context of the project, describing its research objectives and scientific challenges, illustrating the topology of the designed pulse modulator system, and providing the project timeline.

1.1 THESIS CONTEXT

While it is only human to take our own inventions for granted, there is perhaps no technology as underappreciated than the blessing of a stable electric power supply. From lighting up homes and schools across the globe to providing life in the busiest of hospitals, we have all come to expect our access to energy as a fundamental human right. Although it is hard to imagine life without electricity, its conception occurred not so long ago. Compared to the discovery of fire around two million years ago and the wheel sometime between 2800-4000 BC, the invention of the battery in 1800 can be considered relatively recent. Since then electricity rapidly reached every corner of the world within the span of a hundred years, making it one of the greatest engineering achievements of the 20th century [1]. During this period the techniques for generation, transmission, and distribution of electric power have remained fairly constant. In recent decades, however, two transformative research directions have emerged *viz.* towards distributed generation [2] and towards renewable integration [3]. This massive energy transition has been made possible through wide-spread application of power electronics at numerous points in the grid, albeit limited in operational voltage due to inherently low bandgaps of silicon-based power switches. With the introduction of silicon carbide, these limitations are gradually being pushed towards the medium-voltage level with technologies such as the solid-state transformer. SSTs are expected to be a vital part of fu-

ture power systems, wherein renewable energies are integrated seamlessly without any significant disturbance [4]. The medium-voltage transformers used in these SSTs will experience a diverse variety of quasi-rectangular stresses across their insulations, characterised by fast rise and fall times repeating at frequencies of up to a hundred kilohertz. This "mix" of stresses are known to catalyze gradual deterioration on account of enhanced partial discharge activity [5], which are further exacerbated by thermal runaways caused by capacitive currents flowing through the dielectric. All of this leads to increased probabilities of breakdown thereby lowering the expected life-times of the insulation. Hence, it is of crucial importance to quantify this accelerated ageing in meaningful ways, understand what causes it, and draft guidelines for designing insulations in solid-state transformers for the future. Considering this, it is therefore the responsibility of us Electrical Power engineers to explore these questions to ensure resilient infrastructure that can last generations. This forms the core motivation behind this thesis.

1.2 RESEARCH QUESTIONS

The aim of this work is to investigate the performance of oil-paper insulations under pulsed waveforms, by linking the dielectric breakdown to specific pulse parameters such as repetition rate and peak voltage magnitude. To do this, the research objectives (RO) were set as follows,

- RO1: To develop a solid-state pulse modulator for testing dielectrics
- RO2: To study the ageing trend of oil-paper under pulsed stresses

In the process of achieving these objectives, the answers to three research questions (RQs) were found. These are summarised as follows,

- RQ1: Are SiC MOSFETs a practical substitute to Si IGBTs in solid-state medium-voltage pulse-modulator applications?
- RQ2: What are the critical pulse transformer design considerations when generating quasi-rectangular pulses across capacitive samples?
- RQ3: How does the frequency of pulsed voltages accelerate the ageing processes in oil-impregnated paper?

Apart from these academic objectives, the personal goals of the thesis were to build hardware from the ground-up, use this hardware to produce suitable results, and finally analyse these results to gain important insights.

1.3 MODULATOR TOPOLOGY

The designed pulse modulator is shown in Fig. 1.1. The full-bridge converter rectifies power from the AC mains to charge the DC link capacitor C_{dc} the voltage across which is then converted to sharp pulses through the H-bridge pulse generator. The switches are controlled with a microcontroller to produce unipolar/bipolar pulses of variable frequency. The output is then stepped up via the pulse transformer with turns ratio n and finally applied onto the oil-paper sample through elements R_t and C_t.

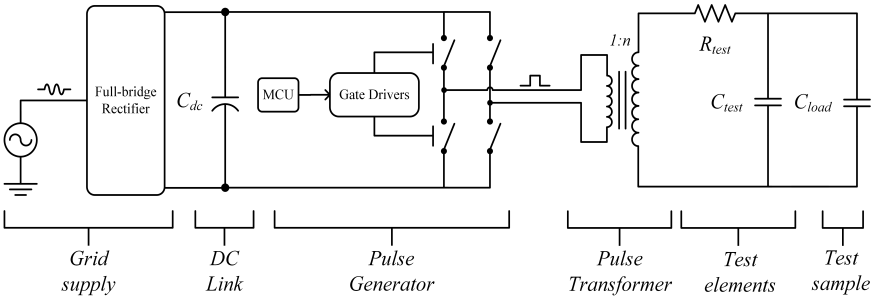


FIGURE 1.1: Circuit of the pulse modulator system

1.4 PROJECT OVERVIEW

An overview of the project timeline is given in Fig 1.2. **Chapter 2** discusses the history of oil-paper insulation, the origin of pulses in the grid, their deteriorating effects on insulations, and techniques to replicate these pulses for experiments. **Chapter 3** develops the variable frequency SiC-based H-bridge pulse generator through component selection, simulation studies, PCB prototypes, and evaluation tests. **Chapter 4** derives a novel PQR equation to characterise the modulator, designs the pulse transformer through analysing the tradeoffs, comparing the bobbin iterations, the magnetic core characteristics, the failure modes with their solutions, and the required modulator sub-circuits. **Chapter 5** describes the theory of the ageing experiments, the followed test protocols, and demonstrates the influence of pulse parameters on oil-paper samples through statistical analysis. **Chapter 6** draws the main conclusions through a reflection of the obtained results, the learning experiences, the possible scopes of improvement, and new research questions that emerged during the course of the thesis.

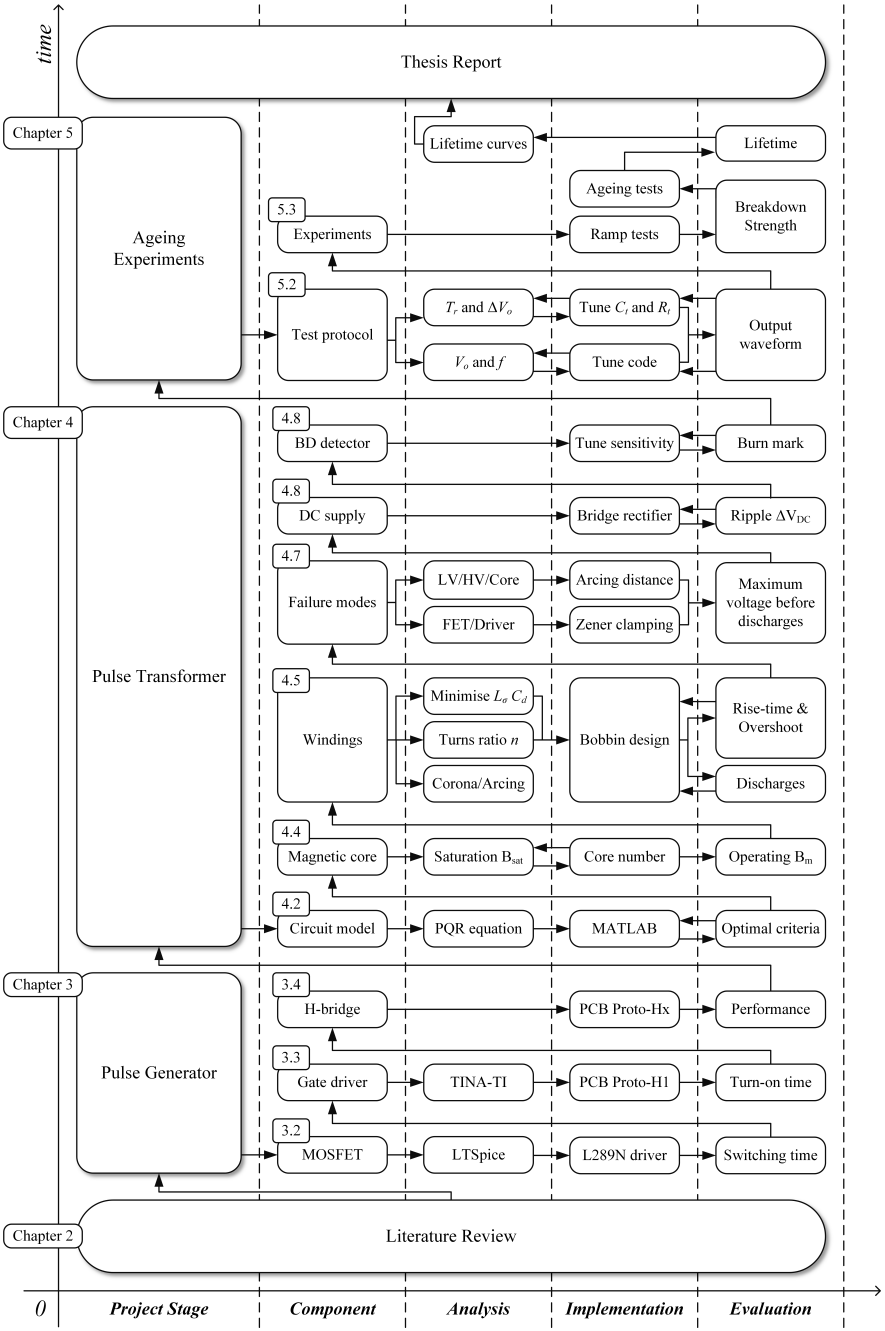


FIGURE 1.2: Project timeline

2

LITERATURE SURVEY

My goal is simple. It is a complete understanding of the universe, why it is as it is and why it exists at all.

Stephen Hawking
The Theory of Everything (2002)

Since the thesis project spans several different subtopics of high-voltage engineering and power electronics, the purpose of this chapter is to impart to the reader a thorough theoretical background related to the concepts utilised in subsequent chapters. This is done by walking through relevant works in the form of journal articles, books, standards, and so on. Considering the vast expanse of available literature, special care has been taken to condense it into a sizeable chapter by citing what the author believes to be the most influential works in the respective subtopics.

2.1 PROPERTIES AND APPLICATIONS OF OIL-IMPREGNATED PAPER

Cellulose-based materials such as paper have been used as electrical winding insulation ever since the invention of the first transformer. This can be attributed to two reasons *viz.* the natural abundance of its primary source i.e. wood, and the excellent dielectric properties of pure cellulose [6]. The primary ingredient for making paper is pulp, a fibrous material prepared by extracting cellulose fibres from tree wood through mechanical, chemical, or chemi-thermomechanical techniques. Paper pulp consists of around 80% cellulose (crystalline and hydrophilic), 10-15% hemicellulose (amorphous and semi-soluble), and 2-5% lignin (rigid and hydrophobic). The ratio of these three "incompatible" polymers determine the strength of the pulp and depends on the pulping process [7]. One such process is the Kraft process used to produce Kraft paper, the dominant insulation material in power transformers. Unlike other techniques, the kraft method uses sodium hydroxide ($NaOH$) and sodium sulphide (Na_2S) to break the bonds between cellulose, hemicellulose, and lignin. In doing so, the resulting Kraft paper is made free from almost all lignin content, which is responsible for weakening the bonds between cellulose and hemicellulose due to its hy-

drophobic nature. The pulp is finally converted into paper through pressing and drying. The fibrous intricacy of paper can be better appreciated from the micrograph of common tissue paper shown in Fig 2.1. The picture was constructed by manually stitching 9 separate images into a single panorama. Each individual fibre is approximately 10 micrometres wide.

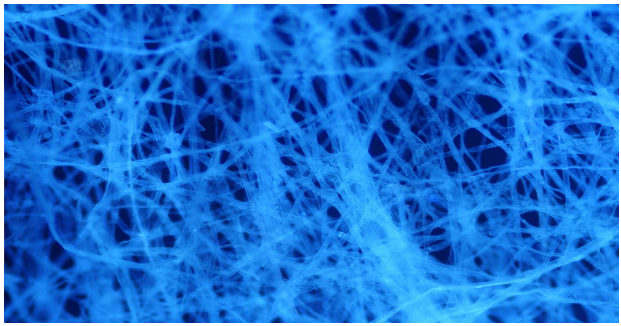


FIGURE 2.1: Micrograph of tissue paper fibres under ultraviolet light by R. Wheeler

Historically speaking, cellulose has been a major tool in shaping human culture and development, from the Egyptian papyri we studied ancient writings from to the cotton clothes we wear to the wooden furniture we use. This has made it the most common polymer on Earth and is also considered to be almost inexhaustible [8]. Cellulose ($[C_6H_{10}O_5]_n$) is an organic polysaccharide made up of hundreds (poly) of glucose chains (saccharide) linked to each other via glycosidic bonds. The molecular structure of a cellulose fibre (Fig 2.2) contains a large number of anhydroglucose units, each made of 3 hydroxy groups, with every second ring rotated 180° in the plane. The number of these units define the polymer's Degree of Polymerisation (DP), a useful measure of its chemical and mechanical properties. The DP values for newly installed transformer insulation can range from 1000-1400, slowly degrading over time to values of 200-300 at the end of its lifetime.

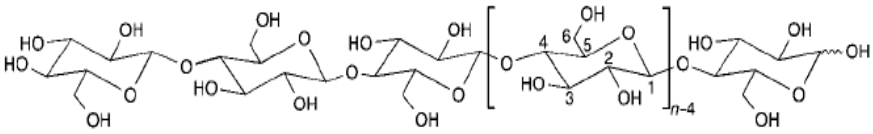
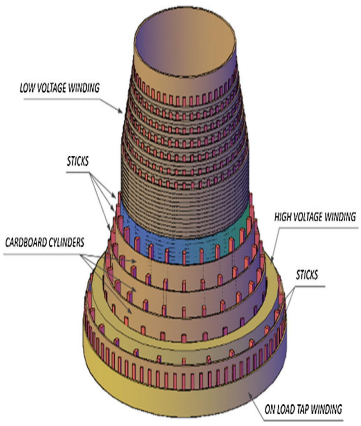


FIGURE 2.2: Molecular structure of cellulose; n = Degree of Polymerisation [8]

Being hydrophilic, cellulose is highly susceptible to absorb moisture even in the presence of the slightest amount of humidity. For this reason, paper is always dried before it is used in combination with either oil or a resin, oil-paper being the most common form. Additionally, the oil is filtered to remove unwanted impurities and degassed to remove any gases dissolved in it. While paper provides mechanical support to the windings, oil provides cooling from the heat generated within the equipment. Hence the quality of the oil used is also another factor for healthy transformer operation. Mineral oil is obtained as a by-product during the distillation of crude petroleum. The refining processes are selected in such a way so as to produce oil which satisfies the operating limits of the transformer. These processes are similar to those used to produce common lubricating oils, making transformer oil a monetarily feasible choice as an electrical insulating liquid [9]. However their dependence on crude petroleum makes mineral oils a non-renewable resource with limited biodegradability. They also have low ignition temperatures which can lead to disastrous consequences in the event of an arc or lightning strike. As an alternative, synthetic silicone oils (polydimethylsiloxane or PDMS) have excellent thermal stability, self-extinguishing capabilities, and do not require major transformer design alterations [10]. Despite this, mineral oil still remains as the most widely used insulating liquid in transformers. A comparison of typical properties between mineral and silicone oils is given in Fig 2.4.

(a) Items made from Kraft paper [6]



(b) Insulation layers [11]

FIGURE 2.3: Illustrations of Kraft paper implemented as insulation

The developments in high-voltage equipment such as power transformers and cables have been hand in hand with the developments in oil-paper insulations. Some early examples of transformer insulations include cotton or jute cloth boiled in oil. It was in 1922 that the *American Institute of Electrical Engineering* (AIEE) began their experiments on oil-paper materials to better analyse their breakdown strengths and mechanisms [12]. At the time, however, chemistry was not considered a significant contributor to the field of high-voltage, making it difficult for the then physicists to gain significant insights. Regardless of this knowledge gap, the major findings were the need to reduce air bubbles and moisture content, both of which are direct causative factors for dielectric loss and breakdown.

Through the next decade, scientists slowly recognised the importance of material science expertise in studying insulation materials. It was this realisation that led to several key improvements in high-voltage equipment constructions and designs during the 1930s, such as the introduction of plastic-based insulations for power cables [12]. By the 1950s, Kraft paper had gained massive traction as the prime dielectric used in power transformers and a prime topic of research for material scientists across the world. To meet the increase in insulation requirements due to increase in voltage levels, power transformers began to use Kraft paper with insulating oil. These international efforts led to a number of enhancements in paper strength, for example by adding synthetic fibres. Now again in the 21st century, oil-paper studies have regained interest due to the effect of pulsed waveforms on accelerate ageing of these insulation materials. But before studying the effects of sharply changing stresses on oil-paper insulations, it is first important to identify the source of these waveforms and parametrise them. This is discussed in the next section.

Table II: Mineral Transformer Oil—Typical Molecular Characteristics

Transformer Oil Type	Naphthenic	Paraffinic
Distillate Boiling Range (ASTM D2887)		
Initial Boiling Point, °C	238	239
5% Recovery Temperature, °C	271	306
50% Recovery Temperature, °C	330	372
95% Recovery Temperature, °C	384	419
Final Boiling Point, °C	429	531
Average Molecular Weight - g/mole	384	419
Number of Carbon in Average Molecule	18	21

(a) Mineral oil [9]

TABLE I
TYPICAL PROPERTIES OF SILICONE TRANSFORMER LIQUID

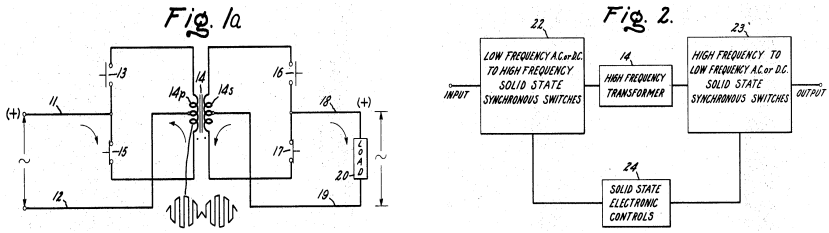
Thermal	
Flash point °C	>300
Fire point °C	>350
Pour point °C	−55
Relative thermal conductivity (cal/cm/s/°C)10^{-4}	3.6
Specific heat (cal/gm/°C) 25°C	0.360
Coefficient of expansion (cm^3/cm^3/°C) 25°C	0.00109
Rate of heat release (kW/m^2) (48-in pan)	100–125
U.L. fire hazard rating	4–5

(b) Silicone oil [10]

FIGURE 2.4: Property tables for typical transformer oils

2.2 ORIGIN AND CHARACTERIZATION OF PULSE WAVEFORMS

As mentioned in Chapter 1, the energy sector is currently undergoing a transition to a greener future wherein our dependence on fossil fuels is reduced through renewable integration. The use of power electronics have facilitated the interfacing of these renewables to function in tandem with the existing AC-dominated infrastructure. Advancements in semiconductor technologies in the second-half of the twentieth century made possible the accurate control and efficient conversion of power, such as in variable speed drives (VSDs) [13] and solid-state transformers (SSTs) [14]. The idea of an SST was first patented in 1970 by W. McMurray, stemming from the concept that a high frequency link in power circuits could significantly reduce the effective volume of the device while also being able to push through larger power densities. This can be implemented by using solid-state switches to produce medium-frequency voltages which would then be passed through a transformer (hence the term SST). This is illustrated in Fig. 2.5.



(a) Circuit diagram (b) System diagram

FIGURE 2.5: Figures from Patent US3517300 filed by W. McMurray [15]

Due to the limited capabilities of semiconductor devices, SST technology could not be fully realised in that era. However with massive breakthroughs in the field of power electronics during the last decade, SSTs are now a central topic of research in several leading groups across the world. Some examples of such transformative work are those carried out by J. W. Kolar of ETH Zürich, Switzerland [4] and W. van der Merwe of University of Stellenbosch, South Africa [16]. The simple yet powerful concept of an SST can provide several flexibility features such as bi-directional power flow between AC or DC grids, real-time active/reactive power control, as well as conversion or conditioning of energy within the grid. A comprehensive overview of SST applications is given in [17]. For high-voltage applications, multi-level converters (MMCs) are implemented to reduce the harmonic

distortion, reduce the size of the output filter, increase the power efficiency, and to allow better fault tolerance [18]. In addition to these benefits, increasing the number of levels n in an MMC reduces the withstand potential of each switch in the converter. As an example, an 11 kV SST requires at least seven voltage levels which brings the per-switch rating to around 2.7 kV [14]. On the other hand, a higher n results in higher costs and complex switching control. There is hence a tradeoff between choosing higher values of n and using switches with greater voltage ratings. This tradeoff is what made the introduction of wide band gap silicon-carbide (SiC) monumental for the future of high-power electronics [19]. While Si MOSFETs have superior switching speeds of a few nanoseconds, their inherently low band gap makes them unsuitable for high-voltage switching applications. Conversely, Si IGBTs can withstand larger voltages up to 6.5 kV, but have significantly slower switching characteristics. The SiC MOSFET, introduced by CREE Wolfspeed in 2011, overcomes both these drawbacks by combining the strength of IGBTs and the speed of MOSFETs (Fig. 2.6). Consequently, they are expected to play an integral role in SST applications for the power systems of the future. Due to their unique properties, the implementation of SiC-devices requires extra considerations that will be explained in Chapter 3. It is another one of the research objectives (RQ1) of this thesis to explore the design of SiC-devices in high-voltage high-speed switching applications.

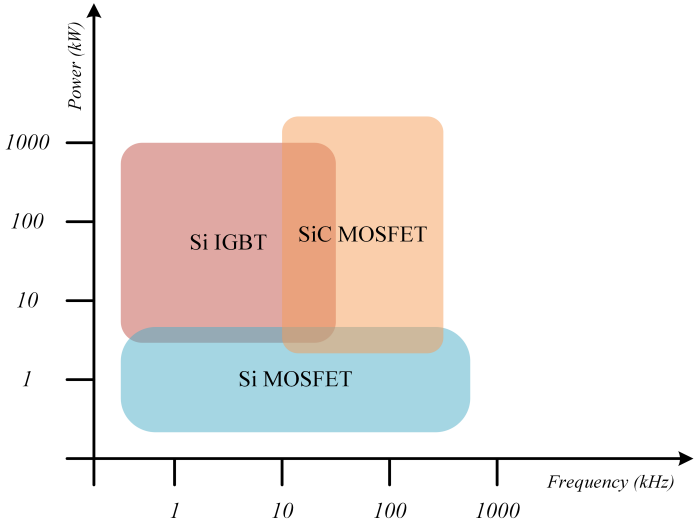


FIGURE 2.6: Comparison of Power and Switching capabilities of Si and SiC devices

The most critical component of the SST is the medium frequency transformer. In the modern power system, SSTs consist of pulse-width-modulation (PWM) controlled inverters that operate at frequencies of up to several tens of kilohertz. As a result, the waveforms observed in these SSTs contain fast-rising frequency components as shown in Fig. 2.7, and can be characterised using certain parameters. The peak amplitude V_{pk} is measured as the maximum numerical voltage value for a unipolar pulse, while the peak-to-peak swing V_{pk-pk} depends on the polarity of the pulses i.e. unipolar ($V_{pk} = V_{pk-pk}$) or bipolar ($V_{pk} = 2V_{pk-pk}$). The fundamental fourier component of the waveform is a sine wave corresponding to the operating frequency of the SST. The terms switching frequency f_s and repetition rate RR are used interchangeably, since they are both related to the time between two successive pulses. Apart from the parameters that define the waveform as a whole, specific parameters define each individual pulse. The rise time t_r is the time taken for the pulse to rise from 10% to 90% of its final value, converse to the fall time t_f. The V_{pk} and t_r determine the slew rate of the pulse, an important characteristic that measures the rate of change of voltage (and thereby field stress) across the insulation in kV/μs. When designing pulse transformers, the t_r and overshoot V_{os} possess an inverse relationship as will be shown later in Chapter 4. The pulse width t_p and droop V_d have a direct proportionality, which is intuitive since a larger pulse width would provide more time for the pulse top to decay. The t_p is related to the duty cycle D which varies per pulse due to pulse width modulation [20]. After the pulse completes its fall transition, it usually settles at a non-zero value known as quiescent voltage V_q. Finally, it is important to note that since only 2-level inverters are considered here, parameters such as number of levels n are not discussed. The standard IEC 60034 Part 18-41 provides some common characteristic ranges of the terminal voltages of converter-fed rotating machines [21]. Similar, if not faster and larger, values can be expected in present day SSTs. Table 2.1 summarises the values given in the IEC standard as well as those used by R. Färber in his PhD thesis [22]. In this thesis he explored the effect of mixed-frequency medium-voltage stresses on polymeric insulations to determined the best potting material for MFTs. To that end, he designed and developed an online dielectric spectrometer for evaluating the dielectric health. Now that we have learnt the origin of pulsed waveforms in the power system, characterised them with familiar parameters, and observed their usual values we can now study the impact of these sharp voltages on insulation materials, specifically oil-paper.

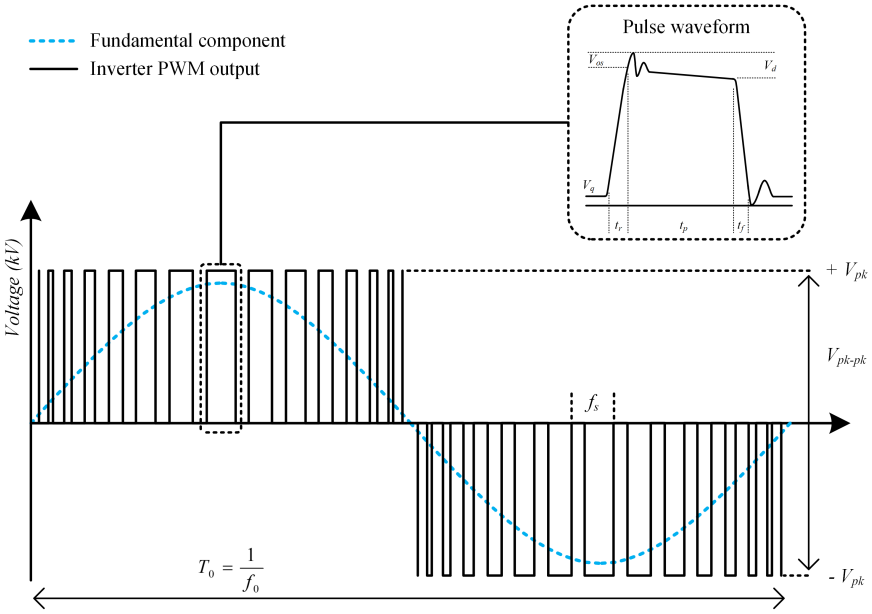


FIGURE 2.7: Typical pulse-width modulated voltage output of an inverter

PARAMETER	SYMBOL	RANGE
Peak voltage amplitude	V_{pk}	0.5 to 10 kV
Peak-to-peak voltage swing	V_{pk-pk}	0.5 to 20 kV
Switching frequency	f_s	5 Hz to 20 kHz
Fundamental frequency	f_0	5 Hz to 1 kHz
Pulse Rise time	t_r	0.05 to 2 μs
Pulse Fall time	t_f	0.05 to 4 μs
Slew rate	-	0.5 to 50 kV/μs
Pulse Polarity	-	Unipolar or Bipolar
Pulse width	t_p	2 μs to 100 μs
Peak overshoot	ΔV	2 % to 5%
Voltage droop	V_d	variable
Quiescent voltage	V_q	variable

TABLE 2.1: Common parameter ranges of 2-level SST inverter waveforms

2.3 EFFECTS OF PULSED STRESSES ON INSULATION MATERIALS

The influence of quasi-rectangular voltages on insulation ageing was first observed in the stator windings of inverter-fed motors which were "magnet" wires embedded in epoxy. The 1980s saw an increased application of variable speed drives for the control of motors used in industrial sectors. The engineers at the time also observed proportionately higher occurrences of failures in the insulations of these motor stator windings. It was then hypothesised that there must be some link between medium frequency components and insulation ageing, thereby leading to several studies in the 1990s in this topic [23] [24] [25]. In 1992, G.C. Stone *et al.* examined the effect of unipolar repetitive voltage surges on the ageing of pure epoxy [26]. His results showed that accelerated ageing could occur even in the absence of partial discharges (PDs), which was then believed to be the phenomenon that causes ageing. He studied how the repetition rate, polarity and magnitude of voltage surges could instead better explain ageing in the non-PD regime. In 1995, J.A. Oliver *et al.* elucidated in detail the effect of steep-fronted surges on motor windings [27]. The brief moment at which such a wave strikes the stator, the frequency content causes a capacitive division of surge voltage across the windings which is concentrated in the first few turns. Sharper waves contain faster frequencies causing larger voltages across these turns leading to sooner failures in the insulation. The magnitude of this voltage is expected to increase with developments in semiconductor switches, shown in Fig. 2.8 by A.H. Bonnett.

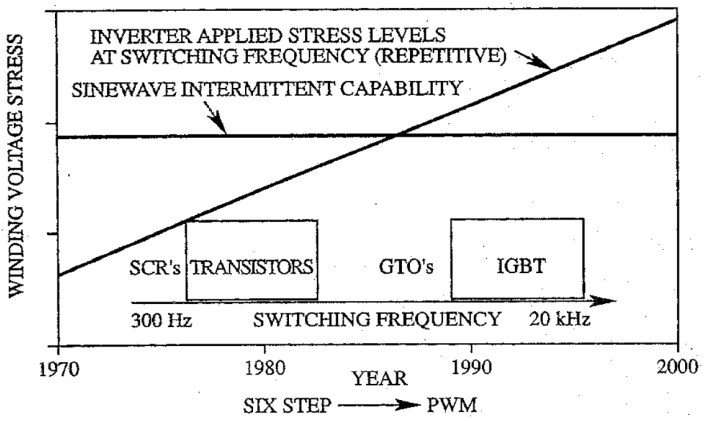


FIGURE 2.8: Winding stresses versus transistor developments [28]

An important insight from these studies was that the mechanism of failure in the PD and non-PD regimes diffed greatly. This was illustrated by M. Kaufhold in 1995 [29] when investigating the failure mechanism of interturn winding insulations with 0.1/5 μs 5 kHz 0.7 to 4 kV pulses. He introduced the idea that dielectric failure in the PD regime is determined by a p_{PD} probability of partial discharge occurrence and a n_b number of PD pulses required to induce breakdown. The values of p_{PD} were computed as the ratio of measured pulses which caused PD to the number of pulses applied. These two parameters were then plotted against the amplitude of the pulse in three distinct ranges, as shown in Fig. 2.9. In voltage range 1 almost all applied pulses cause a PD ($p_{PD} = 1$), indicating that failure would occur exactly after n_b pulses. In voltage range 2 the probability reduces but to some non-zero value ($0 < p_{PD} < 1$), indicating that $n > n_b$ pulses would cause breakdown. Voltage range 3 refers to the non-PD regime ($p_{PD} = 0$) where partial discharges are hardly observed. He also noted that it was the peak-to-peak voltage V_{pk-pk} that caused breakdown, indicating that alternating (bipolar) pulses can cause quicker failures than unipolar ones. With these results, he concluded that failures were a consequence of partial discharges alone. It would then be expected that failures under partial discharge inception voltage (PDIV) should be non-existent, but this is not the case and hence requires more research (which was later explored for epoxy by R. Färber from ETH Zürich in 2019 [22]).

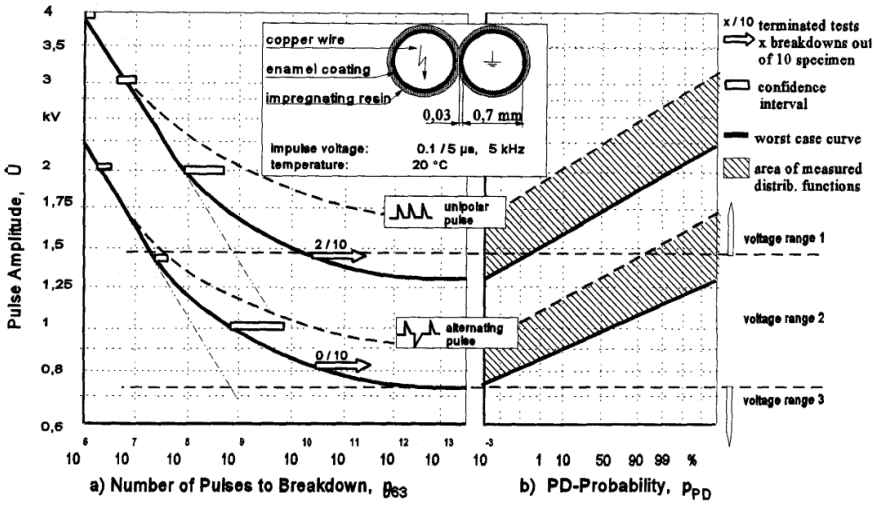
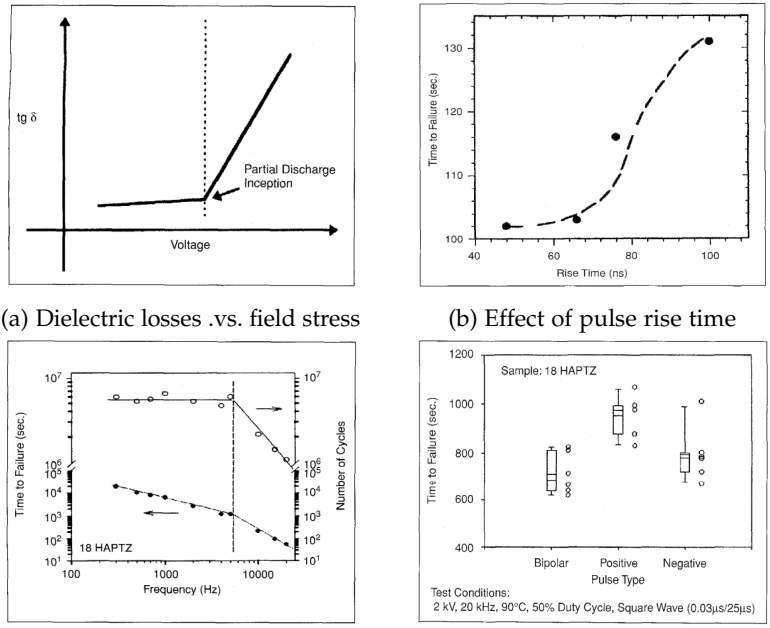


FIGURE 2.9: Plot of p_{PD} and n_b in three pulse voltage regions [29]

The most influential work that answered these pending questions was by W. Yin in 1997. She explained that the failure of these insulation materials cannot be attributed to a single factor, but rather a combination of multiple factors such as partial discharge, dielectric heating, and space charge formation [30]. She first showed that under the PDIV, the flow of high-frequency component currents through the insulation caused dielectric heating which result in failures. This is further increased in the PD regime as illustrated in Fig. 2.10a. Next, she showed that fast pulse rise-times lead to rapid changes in temperature and an inability to dissipate this heat quickly enough is what causes failures, as illustrated in Fig. 4.8. She then showed the effect of frequency, illustrated in Fig. 2.10c, which indicated a transition point at around 5 kHz above which failure times decreased significantly. Finally, she showed that insulations under bipolar fail the quickest due to the local space-charge field, similar to that in modern HVDC cables. For this reason, bipolar pulses at 10 kHz and above were selected for this thesis to reduce experimental time. W. Yin's comprehensive analysis ended the debate at the time, paving the way for standardised rules for motor windings [31].



(a) Dielectric losses .vs. field stress

(b) Effect of pulse rise time

(c) Effect of pulse frequency

(d) Effect of pulse polarity

FIGURE 2.10: Important dependencies found by W. Yin [30]

Following W. Yin's work and subsequent standards, the need for dielectric ageing studies under mixed frequencies died down in the 2000s. This decade saw an increased research in SST technologies and by the 2010s the SST was seen as a vital part of future smart grids. This renewed the interest in studying insulation materials used in medium-frequency transformers, since they would experience stresses quite similar to those in motor windings. Above PDIV, the factors affecting the lifetime include,

- **Pulse magnitude**: The most influential parameter causing dielectric failure is the peak-to-peak voltage magnitude, regardless of the waveform shape. This follows the inverse power model of the form,

$$L = L_0 V^{-n} \tag{2.1}$$

  Cavallini *et al.* elucidates this with the fact that the lifetimes for different waveforms of the same frequency when plotted on a double logarithmic plot fall on the same line [32].

- **Pulse frequency**: There is a common consensus that the lifetime decreases with an increase in frequency. This is expressed as an inverse exponential,

$$T_{failure} \propto f_s^{-k} \tag{2.2}$$

  There is still debate on the value of $k > 0$ itself. M. Moonesan *et al.* proposed an inverse relationship ($k = 1$) wherein the damage due to PDs is independent of f_s [33]. But P. Wang *et al.* obtained $k \approx 0.6 - 0.8$ with the per-PD degradation being proportional to f_s [34].

- **Pulse rise time**: As shown by W. Yin [30] and M. Kaufhold [29], faster rise times can reduce the lifetime. This is consistent with the observation that these shorter rise times lead to larger PD magnitudes [34] [35].

- **Pulse polarity**: It was also shown by W. Yin [30] and M. Kaufhold [29] that the peak to peak voltage magnitude is what reduces insulation lifetime, as opposed to just peak magnitude. M. Kaufhold explains that PD occurrences lead to an accumulation of heteropolar space charges on the enamel surface. The electric field due to this charge negates the applied electric field for unipolar excitations, but instead increases the field intensity for bipolar excitation. Hence the time to failure under bipolar pulses is almost half as much as it is under unipolar pulses.

- **Pulse duty cycle**: Cavallini *et al.* illustrated that the shorter impulse widths require larger voltages to incept repetitive PDs, but the PDIV itself does not depend on the impulse width [36]. However the authors showed that longer pulse widths can result in lower repetitive partial discharge inception voltage (RPDIV) since there is more time for a starting electron to become available and begin the discharge. This was further validated by P. Wang *et al.* by observing that reducing the duty cycle from 50% to 5% can bring about almost 30% increase in failure time [37].

When compared to the ageing above PDIV, the trend of insulation failures under PDIV is significantly less severe. An excellent example of this is provided in [38] wherein the drops in lifetime of twisted enamelled wires were compared between 50 Hz and 10 kHz. It was observed that in the PD regime the drop was around 4 orders of magnitude while in the non-PD regime the drop was only 2 orders of magnitude. This then leads to the question: *"What causes insulation failure under PDIV?"* The closest answer was provided by D. König *et al.* in 1998 when comparing lifetimes of "healthy" well-impregnated samples and "unhealthy" partially-impregnated samples under 50 Hz and 50 kHz [39]. Although the PDIV of healthy samples was measured to be 20 kV, they began to fail at only 10 kV under 50 kHz. The authors attribute this to higher dielectric losses (by 1000 times) at 50 kHz. The temperature increases when the rate of cooling is insufficiently fast to compensate for the rate of heating. Further, the losses increase at higher temperatures leading to a thermal runaway [40]. The losses themselves are due to conduction and polarisation currents, both of which are temperature-dependent [41]. B. Sonerud *et al.* importantly described the dielectric heating involving harmonics as a function of RMS voltage U_n, harmonic phase n, fundamental frequency ω_0, real part of capacitance C', and the loss factor $\tan\delta$ [42]. This is then summed for each harmonic and written as,

$$P = \sum_{n=1}^{\infty} |U_n|^2 \, n\omega_0 C'(n\omega_0) \tan\delta(n\omega_0) \tag{2.3}$$

This equation will be revisited in Chapter 5. Considering that PDs in oil-impregnated paper is relatively less probable than in polymeric insulations such as epoxy, the failure mechanism due to dielectric heating is important to consider when designing insulations for medium frequency applications. Despite its need, substantive work for oil-paper in this area has been limited in frequency (up to 10 kHz). **This thesis project aims to fill this research gap** by comparing lifetimes at 10 kHz and 50 kHz. Next, we study techniques for replicating pulsed waveforms for experiments.

2.4 TECHNIQUES FOR REPLICATING QUASI-RECTANGULAR VOLTAGES

The generation of high voltage (and usually high power) pulses has been widely explored in literature, owing to their diverse set of applications such as in linear accelerators, klystrons, and high-power RF tubes. The system which generate these pulses are termed pulse modulators and can be realised using different approaches, which are described below.

- **Line-type modulators**

  These modulators employ a pulse-forming network (PFN) feeding a pulse transformer which is then connected to the load, as shown in Fig. 2.11 (a). PFNs comprise of energy storage components such as capacitors and inductors charged by a high-voltage source. This energy is then released in the form of fast pulses (up to a few kHz) into the load, the impedance of which is matched with that of the PFN [43]. Such modulators have been used for several decades, and are relatively compact. However they suffer from limited pulse precision, since the pulse shape is mainly determined by the PFN discharge characteristics. Additionally, load impedance matching is imperative for its functioning.

- **High-voltage switch**

  The simplest topology is to directly discharge a capacitor charged to high-voltage through a semiconductor switch as shown in Fig. 2.11 (b). To allow for higher ratings, multiple switches (IGBTs or MOSFETs) can be used in series. Several such modulators are commercially available with ratings up to 200 kV and 5 kA. The main advantages of this topology include precise control of pulse parameters, the ability to attain very fast rise-times, and no limitation on voltage-time product since there is no transformer present. However the switches and capacitors required for this topology are expensive resulting in high development costs and procurement times. Higher voltage ratings require multiple switches which calls for accurate synchronisation in their gate pulses without which the output pulse is deformed and can lead to failure. Further, more switches results in a decrease in overall reliability [44].

- **Marx generators**

  As an alternative to the HV-switch modulator, Marx generators produce a high-voltage pulse from a low-voltage supply by discharging a series of identical capacitances with spark gaps as in Fig. 2.11 (c). These are limited in repetition rate, since the required charging time $\approx 2N^2RC$

and is further increased due to the resistors [45]. The resistors can be replaced with inductors to achieve better repetition rates, but the pulses are restricted by the operation of spark gaps. Replacing these with semiconductor switches such as IGBTs result in the more modern solid-state Marx generators which have been built to generate several kilovolts at repetition rates up to tens of kilohertz [46]. However reaching higher voltages requires higher number of stages in the Marx generator, which also reduces flexibility in varying the voltage magnitude (and hence field stress) across the test sample during ramp tests.

- **Solid-state fed pulse transformer**

  With the advent of silicon-carbide, the fast switching speeds of Si-MOSFETs and voltage/current ruggedness of Si-IGBTs have found an attractive overlap, resulting in power converters with high $\frac{dV}{dt}$ capabilities. These converters can be connected to pulse transformers to produce sharp pulses with nanosecond rise-times as in [47]. The advantages are flexible control over pulse parameters with a simple microcontroller and galvanic isolation [48]. Also, very high voltages of hundreds of kilovolts can be achieved with high turns ratios. However this also requires careful design minimisation of leakage flux and parasitic capacitance which reduce the bandwidth and slow the waveform.

An overview of the four discussed pulse modulator topologies is given in Table 2.2. Since pulse shape control is a priority in dielectric testing the line-type is not considered. Breakdown tests can cause failures in system parts which would need replacement, hence an expensive option like HV-switch is not suitable. The Marx generator requires too many stages to produce higher voltages which is unreliable for dielectric testing. Therefore, a solid-state fed pulse transformer configuration was chosen, with an H-bridge pulse generator (for uni/bipolar pulses) feeding a 1:50 pulse transformer.

TOPOLOGY	MAIN-PRO	MAIN-CON
Line-type	Relatively compact	Limited shape control
HV-switch	Simple design	$\uparrow$ Cost (source, switches)
Marx generator	Sourced at LV	$\uparrow N_{stages} = \downarrow$ Reliability
Solid-state fed PT	Voltage, shape control	Sensitive transformer design

TABLE 2.2: Main advantages and disadvantages of modulator topologies

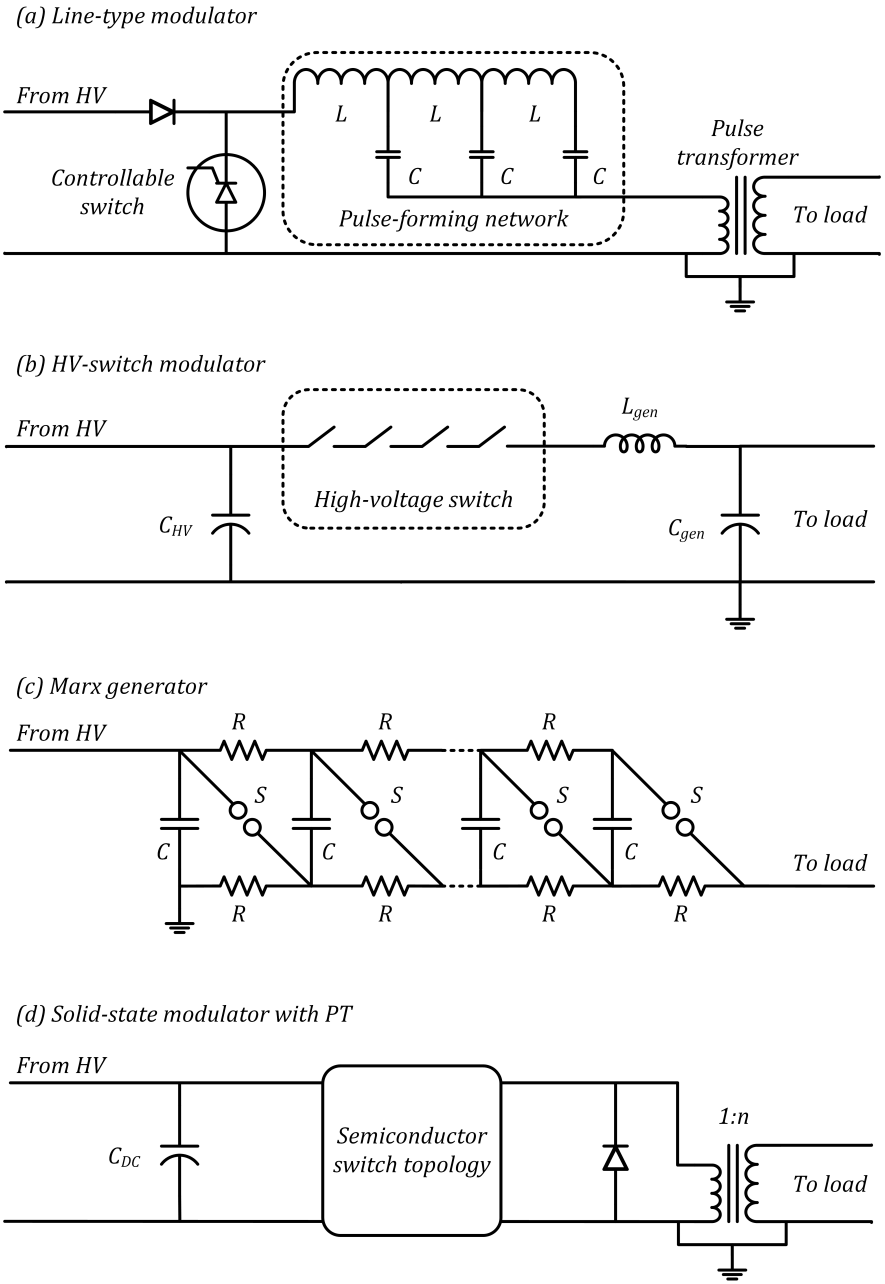


FIGURE 2.11: Schematics of pulse modulator topologies from literature

3

PULSE GENERATOR

In broad terms, the task of power electronics is to process and control the flow of electric energy by supplying voltages and currents in a form that is optimally suited for user loads.
NED MOHAN
Power Electronics (1989)

The pulse generator can be seen as the most reliable component of the pulse modulator, thanks to the control that power electronics provides. Since the pulse transformer suffers from its parasitics which affects its output waveform shape, the goal while building the pulse generator is to produce the fastest possible pulses so as to give more design flexibility in later stages. The subsequent sections of this chapter describe the theory and selection of semiconductor switches with their drivers, the PCB hardware prototypes and their learning outcomes, the power and parameter calculations, and finally the performed evaluation tests and an analysis of results.

3.1 SIC MOSFET

3.1.1 *Theory and mechanisms*

The typical structure of an *n*-channel MOSFET, as shown in Fig 3.1, consists of a *p*-type doped silicon substrate connected to two heavily *n*-type doped regions called the source (*S*) and the drain (*D*). Under biased conditions *i.e.* when a potential V_{DS} is applied across the structure, the device does not allow charge to be conducted through it. However when a positive potential V_{GS} is applied to the gate terminal (*G*), an inversion layer begins to develop that allows charges to "leak" in the *D* to *S* direction. This is the underlying principle of field-effect transistors (FETs). As an improvement over silicon-based FETs, materials such as SiC and GaN have wider energy bandgaps (lower leakage currents), higher critical electric field (lower on-resistances), higher electron saturation velocity (higher switching frequencies), and higher thermal conductivity (higher operating power densities) [49]. Several studies have been carried out to compare the characteristics of SiC MOSFETs with Si IGBTs [50] and Si MOSFETs [51].

A capacitive model of the MOSFET, shown in Fig 3.2, is used to better understand the mechanism of turning on the MOSFET. The three junctions within the transistor can be represented with three equivalent capacitors C_{GD}-C_{GS}-C_{DS}. The first step in switching on is to linearly charge the capacitance C_{GS} to a potential V_{th} at which the switch begins to conduct *i.e.* in the D to S direction. Due to this new flow of current the capacitance C_{GS} injects charge into the D terminal of the transistor while at the same time C_{GD} is being charged from the G terminal. This period where further increase in charge causes no increase in potential is called the Miller region and is quantified with an equivalent Miller capacitance. This phenomenon ends when the charge reaches a certain value Q_B, after which C_{GD} and C_{GS} resuming charging linearly until the transistor is completed turned on at a potential V_{on}. Since the gate is inherently an insulator its resistance is modelled with an internal gate resistance R_G, an important factor to consider during switch selection as will be discussed later.

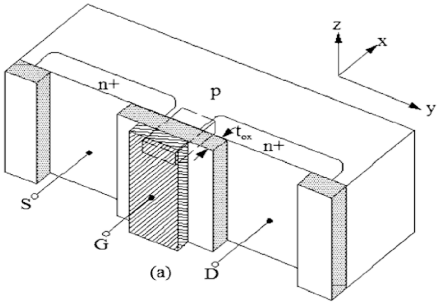


FIGURE 3.1: Idealised MOSFET structure [52]

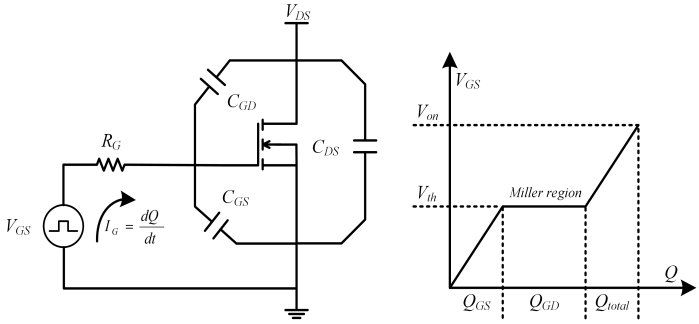


FIGURE 3.2: Capacitive MOSFET model and Turn-on mechanism

3.1.2 *Switch selection: IMW120R140*

The right selection of power switch can make a monumental difference in the simplicity of the converter circuitry and must hence be carried out with care. Although a SiC MOSFET can accommodate the high-voltage and high-frequency requirements of the pulse modulator, they are made by only a handful of manufacturers such as CREE Wolfspeed, Infineon Technologies, Rohm Semiconductor, and ON Semiconductor. The required criteria for the MOSFET include,

- A withstand voltage $V_{DS} \geq 1200$ V
- A sufficient pulse current rating $I_{D(pulse)}$ in the order of 10 A
- A low on resistance $R_{DS(on)}$ in the order of 100 mΩ
- A low switching delay $t_{d(on)}$ and $t_{d(off)}$ in the order of 10 ns
- A fast switching characteristic t_r and t_f in the order of a few ns
- A low internal gate resistance $R_{G(int)}$ in the order of 10 Ω
- A suitable through-hole package to allow a heat sink to be used
- A cost price below 10 euros, since multiple switches are required

There is of course no switch that excels in all these criteria, and hence a trade-off analysis must be performed to make an educated decision. Such an analysis was conducted for 20 SiC MOSFETs from 4 manufacturers to produce a switch selection chart as shown in Fig 3.3.

MOSFET																												
SWITCH PARAMETERS						STATIC						SWITCHING					DYNAMIC				LOSSES							
Supplier	Price (€)		Datasheet	Name	Package	V_{DS}	$I_{D(cont)}$	$I_{D(pulse)}$	$R_{DS(on)}$	$V_{GS(max)}$	$V_{GS(op)}$	V_{SD}	$t_{d(on)}$	t_r	$t_{d(off)}$	t_f	$R_{G(int)}$	Q_g	C_{iss}	C_{oss}	C_{rss}	T_j	P_D							
	RS	Farnell				V	A	A	mΩ	V	V	V	ns	ns	ns	ns	Ω	nC	pF	pF	pF	°C	W						
Wolfspeed	99,18	78,49	link	C2M0045170D	TO-247-3	1700	72	160	45	-10/+25	-5/+20	4.1	65	20	48	18	1.3	188	3672	171	6.7	-40/+150	520						
	-	69,37	link	C2M0045170P	TO-247-4	1700	72	160	45	-10/+25	-5/+20	4.1	35	13	46	10	1.3	188	3672	171	6.7	-40/+150	520						
	6,79	-	link	C2M1000170D	TO-247-3	1700	5	6	1000	-10/+25	-5/+20	3.8	6	10.5	11	60	24.8	13	200	12	1.3	-55/+150	69						
	13,42	11,80	link	C3M0075120D	TO-247-3	1200	30	80	75	-8/+19	-4/+15	4.1	56	17	32	13	10.5	54	1350	58	3	-55/+150	113.6						
	11,5	12,12	link	C3M0075120K	TO-247-3	1200	30	80	75	-8/+19	-4/+15	4.5	30	14	38	10	9	53	1390	58	2	-55/+150	113.6						
Infineon	-	3,95	link	IMBF170R1K0M1	TO-263-7 (D2PAK)	1700	5.2	13.3	1000	-10/+20	-0/+15	-	19	14	20	22	35	5	275	7.2	0.7	-55/+175	68						
	-	8,37	link	IMBF170R450M1	TO-263-7 (D2PAK)	1700	9.8	24.8	450	-10/+20	-0/+15	-	27	20	32	24	20	11	610	16	1.7	-55/+175	107						
	-	6,20	link	IMBF170R650M1	TO-263-7 (D2PAK)	1700	7.4	18.7	650	-10/+20	-0/+15	-	22	16	24	22	25.4	8	422	12	1.1	-55/+175	88						
	-	7,79	link	IMW120R220M1HXKSA1	TO-247-3	1200	13	21	220	-7/+23	-0/+15	-	5	1.4	10	14	22	8.5	289	16	2	-55/+175	75						
	-	9,13	link	IM2120R220M1HXKSA1	TO-247-4	1200	13	21	220	-7/+23	-0/+15	-	4.8	1	9.8	12.7	22	8.5	289	16	2	-55/+175	75						
	-	9,52	link	IMW120R140M1HXKSA1	TO-247-3	1200	19	32	140	-7/+23	-0/+15	4.1	5	2.4	10.4	13	14	13	454	25	3	-55/+175	94						
	-	9,33	link	IM2120R140M1HXKSA1	TO-247-4	1200	19	32	140	-7/+23	-0/+15	4.1	5	2	10.3	11.6	14	13	454	25	3	-55/+175	94						
	-	7,22	link	IMW120R350M1HXKSA1	TO-247-3	1200	4.7	13	350	-7/+23	-0/+15	4.1	7	0.7	11.4	21.5	35	5.3	182	10	1	-55/+175	60						
	-	7,22	link	IM2120R350M1HXKSA1	TO-247-4	1200	4.7	13	350	-7/+23	-0/+15	4.1	4.8	0.7	10.8	19.3	35	5.3	182	10	1	-55/+175	60						
ON-SEMI	8,24	9,78	link	NVHL160N120SC1	TO-247-3	1200	17	69	162	-15/+25	-5/+20	4	11	19	15	8	1.4	34	665	50	5	-55/+175	119						
	8,24	9,78	link	NVH4L160N120SC1	TO-247-4	1200	17.3	69	160	-15/+25	-5/+20	4	11	10	14	7	1.4	34	665	49.5	4.3	-55/+175	111						
	-	9,92	link	NVHL080N120SC1A	TO-247-3	1200	31	132	110	-15/+25	-5/+20	4	13	20	22	10	1.7	56	1112	80	6.5	-55/+175	178						
	11,17	6,83	link	NTHL080N120SC1A	TO-247-3	1200	31	132	110	-15/+25	-5/+20	4	13	20	22	10	1.7	56	1112	80	6.5	-55/+175	178						
ROHM	6,18	8,31	link	SCT2280KEC	TO-247-3	1200	14	35	280	-10/+26	-6/+22	4	19	19	47	29	17	36	667	27	5	-55/+175	108						
	4,90	7,72	link	SCT2450KEC	TO-247-3	1200	10	25	450	-10/+26	-6/+22	4.3	19	17	38	34	25	27	463	21	4	-55/+175	85						

FIGURE 3.3: Switch selection chart used to compare available SiC MOSFETS

The 1700V CREE Wolfspeed MOSFETs have the most attractive V_{DS}, $I_{D(pulse)}$ and $R_{DS(on)}$ but are also the most expensive. The 1700V Infineon MOSFETs are only available in surface-mount-device (SMD) packages and are not suitable for this application. The switches from ON Semiconductor and Rohm Semiconductor are affordable but do not have impressive functional capabilities. The best overall switches are the 1200V CREE Wolfspeed C2M1000170D (lower $R_{G(int)}$ lower $I_{D(pulse)}$) and the 1200V Infineon IMW120R140M1H (higher $R_{G(int)}$ higher $I_{D(pulse)}$). What distinguishes the latter is its unique 0V turn-off potential V_{GS} making it possible to drive the MOSFET with a unipolar positive supply instead of a +20/-5 supply. Also, its higher $R_{G(int)}$ is nullified by its much lower gate charge Q_g meaning that the gate capacitance can be charged quickly. Hence, it was selected for the H-bridge.

3.1.3 *Operational characteristics in LTspice*

The switching characteristics of the Infineon SiCFET [53] were simulated in LTspice and the results shown in Fig. 3.4. The on/off time and the propagation delays of V_{GS} were set to 1 ns. It can be seen that the turn-on is significantly quicker than the turn-off. This can be tackled by either applying a negative V_{GS} or selecting a gate driver with higher sink current.

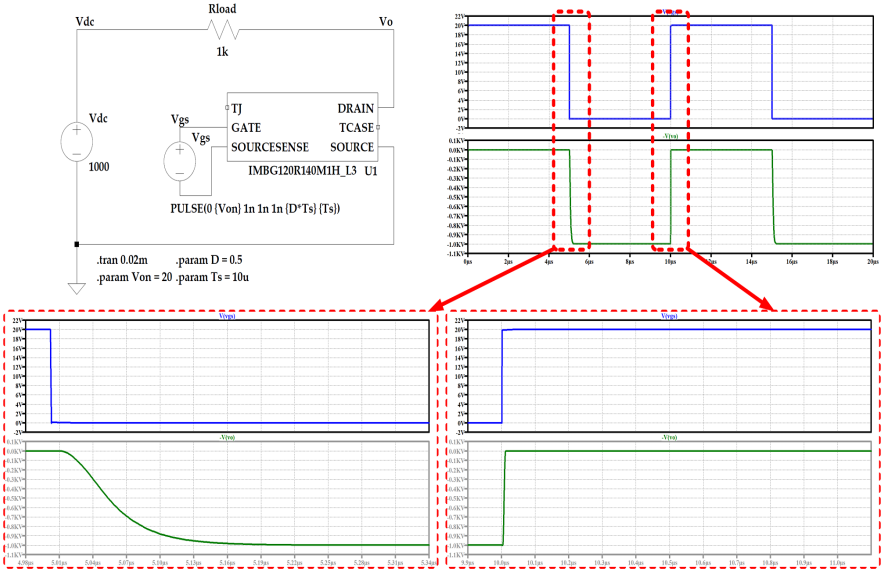


FIGURE 3.4: Simulation of IMW120R140M1H in LTspice

3.2 GATE DRIVER

3.2.1 *Theory and mechanisms*

Behind every well-functioning MOSFET is a driver selected specifically for operating that semiconductor switch. The primary purposes of gate drivers are to galvanically isolate power signals from control signals and to condition the gate signals as per the input requirements of the switch. Reinforced isolation (between power-side and signal-side) comes in three forms *viz.* optical (high current and low noise immunity), magnetic (high current and medium noise immunity), and capacitive (low current and high noise immunity) [54]. Additional features such as functional isolation (between high-side and low-side outputs) and basic isolation (to prevent electrical shocks) are available for high-voltage applications [55]. The most critical criteria of the gate driver is its drive strength, parameter that determines how fast it can switch the MOSFET and how much current it requires to do so. The switching operation of the MOSFET is carried out by charging and discharging the input capacitance $C_{ISS} = C_{GD} + C_{GS}$ with a gate charge Q_G through a gate current I_G. This is calculated as,

$$Q_G = \int I_G \, dt \;\Rightarrow\; I_G = \frac{Q_G}{T_r \; or \; T_f} = \frac{13 \; nC}{7.4 \; ns} = 1.8 \; A \tag{3.1}$$

The current I_G differs for switching on and switching off operations as source I_{o+} and sink I_{o-} currents, respectively. For SiC applications, drivers with +4/-6 A outputs are used to ensure effective charge transmission to the MOSFET gate terminal. The internal $R_{G(int)}$ and external $R_{G(ext)}$ gate resistances of the MOSFET limit the gate current depending on the drive voltage V_{DD} *i.e* the amplitude of the gating pulses sent to the MOSFET.

$$I_G = \frac{V_{DD}}{R_{G(int)} \; + \; R_{G(ext)}} \tag{3.2}$$

The $R_{G(ext)}$ is kept smaller for the sink path than the source path to allow higher sink currents. The switching frequency f_s determines the power requirement of the driver as,

$$P_C = V_{DD} \times Q_G \times f_s = 20 \; V \times 13 \; nC \times 20kHz = 5.2 \; mW \tag{3.3}$$

Hence, Higher gate currents equate to faster switching times. Faster switching causes higher switching losses, requiring higher power rated drivers.

3.2.2 *Driver selection: UCC21521*

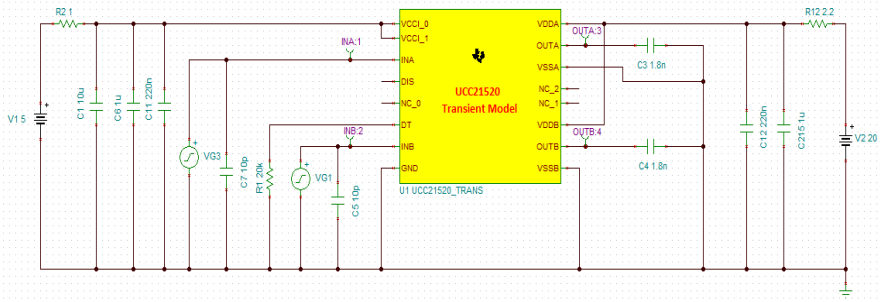
The selection of gate driver limits the operation of the switch and must hence be done in tandem with the datasheet of the switch. Most high-quality driver ICs are manufactured by Texas Instruments making them a leader in the semiconductor control industry. The considerations for the SiC driver include,

- A reinforced isolation voltage rating $\geq$ 1200 V
- A high source/sink current rating preferably +4/-6 A
- A low propagation delay in the order of tens of ns
- A low rise and fall time in the order of ns
- A sufficient power rating $\geq$ 5.2 mW
- A high-side low-side driving functionality
- A suitable SMD package for easy PCB designing
- A interfacing range of $V_{CC} = 5V$ and $V_{DD} = 20V$
- A common-mode transient immunity (CMTI) greater than 100 V/s

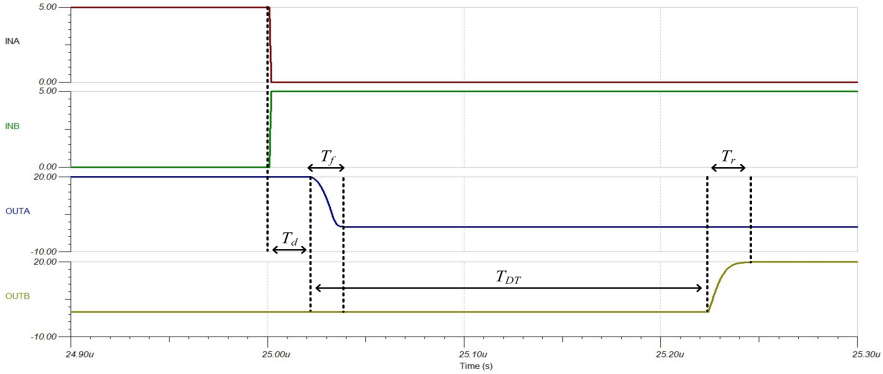
In half-bridge applications, a minimum dead-time is required to prevent a current shoot-through between the high and low side switches. A gate driver with a programmable dead-time is therefore a must. Since the pulse modulator is being used for test applications, which ends in an insulation failure, it is useful to have a separate Enable/Disable pin on the gate driver IC to implement short-circuit protection. The dual-channel +4/-6 A isolated driver UCC21521 from Texas Instruments was finally selected since it satisfies all necessary criteria requirements. It features a 5.7 kV_{RMS} reinforced isolation barrier between power and signal sides, as well as a 1500 kV_{DC} function isolation between high and low outputs. With a 19 ns propagation delay, 6 ns rise-time, and 7 ns fall-time, its switching characteristics match the selected SiC MOSFET. It also has programmable dead-time and Enable pin capabilities, both discussed in better detail in later subsections. The UCC21521 comes in two under-voltage lock-out (UVLO) variants, the UCC21521ADW with 5 V UVLO and the UCC21521DW with 8 V UVLO. Both variants are identical and were used interchangeably depending on their availability.

3.2.3 *Operational characteristics in TINA-TI*

To observe the driver characteristics in simulation the TINA-TI software was used, the Texas Instruments equivalent of LTspice. The simulated circuit is shown in Fig. 3.5a. It should be noted that the UCC21520 model is used for this purpose which has a DISABLE pin instead of an ENABLE pin in the UCC21521. The source $V1 = 5V$ represents V_{CC} which powers the driver and is supported by $C1$-$C6$-$C11$ through $R2$. The source $V2 = 20V$ represents V_{DD} which biases the output pulses, and is supported by the $C12$-$C215$ through $R12$. The pulse inputs $VG3$ and $VG1$ are filtered by $10pF$ capacitors $C7$-$C5$. The DT pin is connected to a $20k\Omega$ resistor resulting in a dead-time of $DT = 10 \times 20 = 200ns$ (explained again in 3.3.1). The dead-time is the period from before the fall (T_f) of the first output (OUTA) to before the rise (T_r) of the second output (OUTB), shown in Fig. 3.5b.



(a) Simulated circuit diagram



(b) Switching characteristic showing the T_r-T_f-T_d-T_{DT} time periods

FIGURE 3.5: Simulation of UCC21520-UCC21521 in TINA-TI

3.3 HARDWARE PROTOTYPES

After simulating the characteristics of both switch and driver, two PCB prototypes were built. ProtoH1 is a unoptimised test PCB of the gate circuitry of a single UCC-driver. The traces are made longer and test-points were added to each part of the trace for evaluation. This allowed an in-depth analysis of the effect of each component on the signals flowing through the traces. Using the results from this analysis modifications were implemented when designing ProtoHx, the final PCB of the complete H-bridge converter including the DC link, the switches, and their gate drivers. Additional considerations had to be taken when designing the high-voltage power-stage of the PCB as per the IPCC2221 standard. The following sub-sections discuss the procedure and calculations used for producing ProtoH1 and ProtoHx. An overview of the employed PCB workflow is shown in Fig. 3.6.

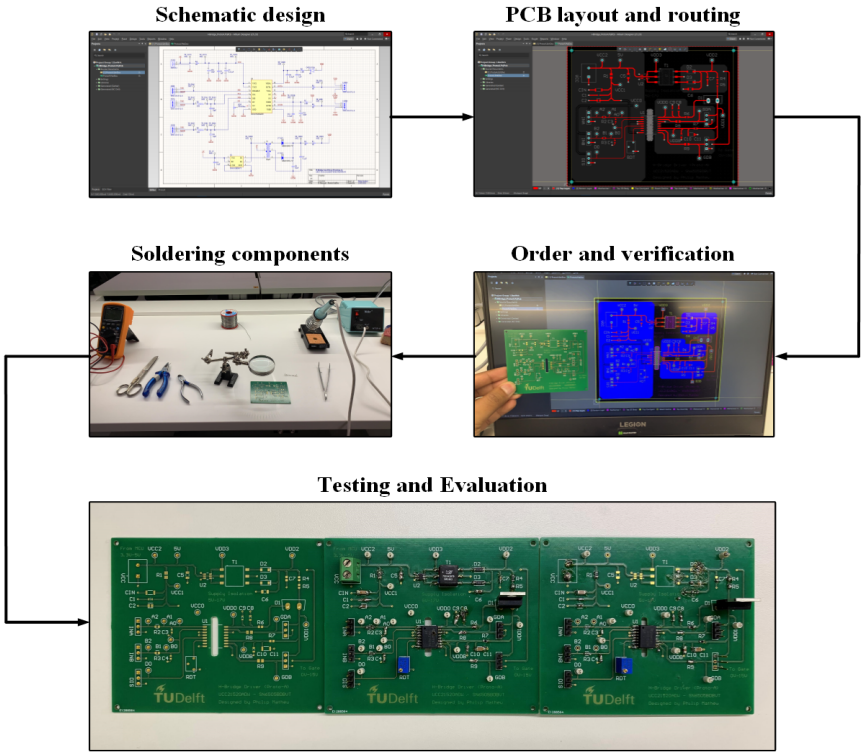


FIGURE 3.6: PCB design workflow using Altium Designer

3.3.1 *Proto-H1: UCC-Driver PCB*

The objectives when designing ProtoH1 were first to get acquainted with the Altium Designer software, and second to produce a single gate-driver so as to individually test the IMW-switch and UCC-driver. The datasheet of the UCC21521 provides a typical application schematic as shown in Fig. 3.7. A brief description of each component is given below.

- Signal-side components:
  - R_{IN} and C_{IN} filters the input pulse signals from the MCU
  - C_{VCC} supports the supply voltage V_{CC} for long PCB traces
  - R_{EN} provides limits the current to the EN pin
  - R_{DT} programs the dead-time selection of output pulses
  - C_{DT} supports the 1.8 V source held at the DT pin
- Gate-side components:
  - R_{BOOT} and C_{BOOT} forms the bootstrap circuitry with V_{DD}
  - C_{VDD} supports the supply voltage V_{DD} for long PCB traces
  - R_{ON} and R_{OFF} limit the source/sink currents during switching
  - R_{GS} provides a path for discharge of switch gate capacitance

The resistances R_{OFF} and R_{ON} are switch-dependent and were hence not added to the ProtoH1 circuit. The component R_{GS} is not required.

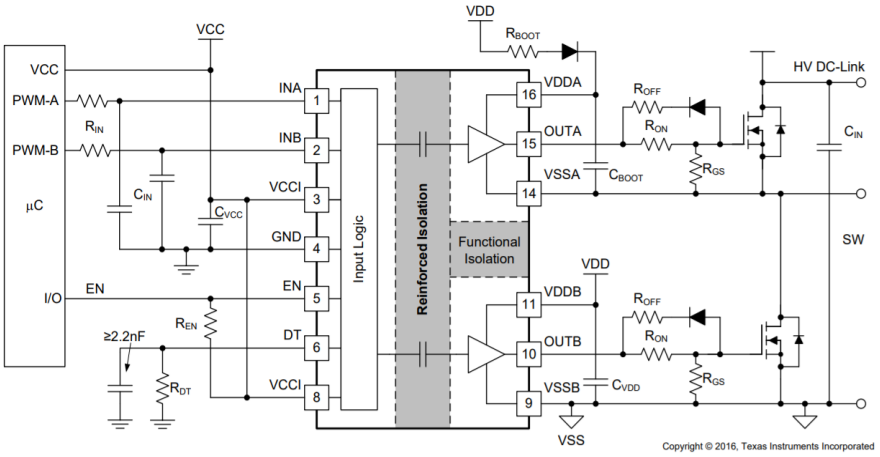


FIGURE 3.7: Typical application schematic of the UCC21521 SiC driver

The implemented schematic is shown in Fig. 3.8. The input V_{CC} was fed from the Arduino and isolated using a push-pull transformer configuration (U2 and T1) to produce V_{DD}. To allow trace testing, 18 test points (TPs) were connected at various parts of the schematic. The C4D05120 SiC Schottky diode was selected for the bootstrap circuit. The designed layout of the PCB is shown in Fig. 3.9. Polygon pours (blue regions) were used in the PCB for the signal ground SGND, the reference for high-side gating signal GNDA, and the reference for the low-side gating signal GNDB. A board cut-out (purple-lined region) was used for better isolation between the signal and power ground planes. Three copies of the board were procured to analyse possible improvements to be implemented in the final prototype. These boards were labelled as ProtoH1.A, ProtoH1.B, and ProtoH1.C as shown in Fig. 3.10. The major learning outcomes are discussed below.

- **Isolation technique**: Replace the complex SN6505 configuration with a simpler Murata MGJ2D052005SC isolated DC-DC converter.
- **Component package**: Choose package sizes no smaller than the standard 0805 for easier soldering. The standard 1206 can be used as well.
- **Other modifications**: Minimise pulse trace lengths to reduce stray inductances. Add LED indication for checking power supply functioning.

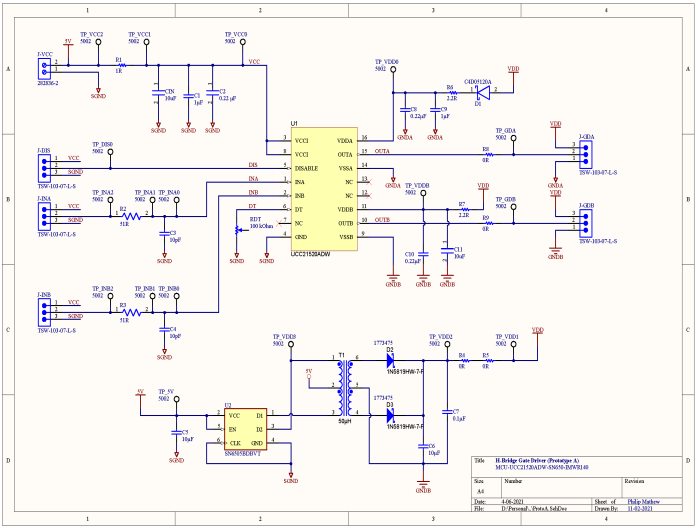


FIGURE 3.8: Schematic diagram of ProtoH1

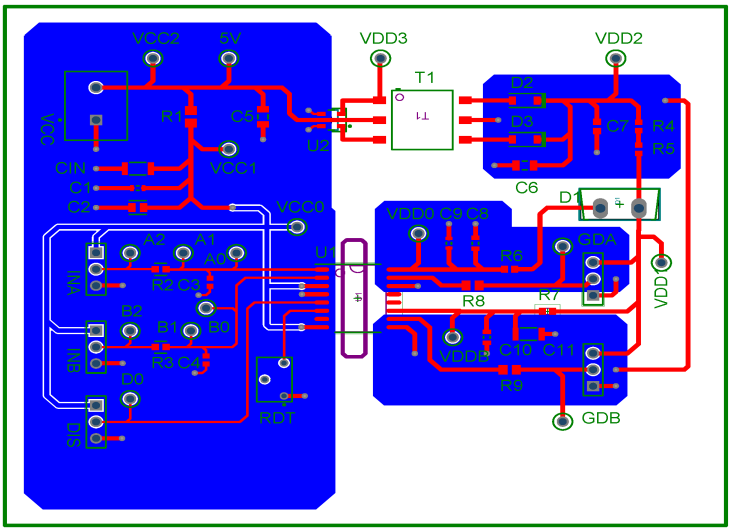


FIGURE 3.9: PCB layout diagram of ProtoH1

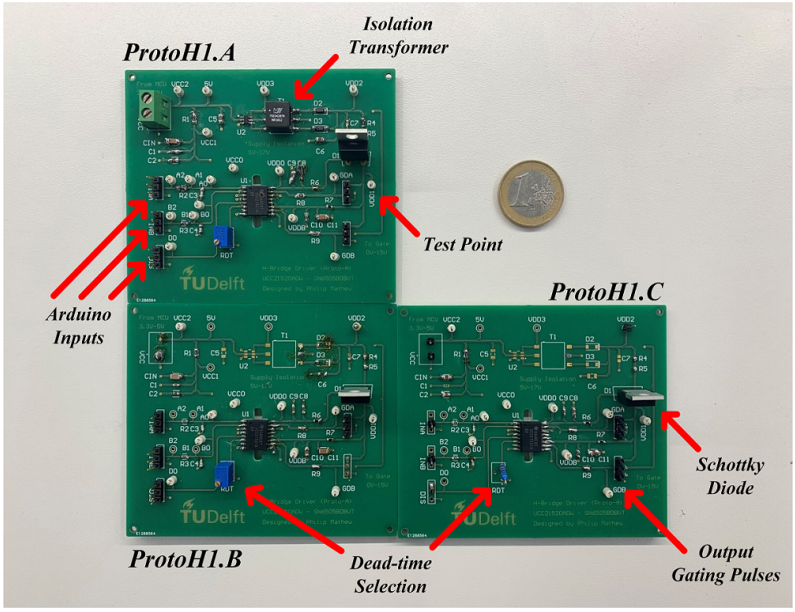


FIGURE 3.10: ProtoH1 prototypes after soldering and evaluation

3.3.2 *Power and parameter calculations*

In this subsection, the reasoning behind the selection of each component is discussed in further detail, and finally an estimation of power dissipation is calculated. The H-bridge circuit consists of 4 SiC switches, 2 dual-side gate drivers, and the DC link. The gate-circuitry components are as follows.

- **Input Filter**: An R_{IN} of 51 Ω and C_{IN} of 10 pF are selected for a corner frequency of approximately 100 MHz. This value is calculated as,

$$F_{corner} = \frac{1}{2\pi \times R_{IN} \times C_{IN}} = \frac{1}{2\pi \times 51\Omega \times 10pF} \approx 100MHz \tag{3.4}$$

- **Bootstrap capacitor**: The C_{BOOT} stores the charge required to switch on the high-side transistor, and the magnitude of this charge is,

$$Q_{total} = Q_G + \frac{I_{VDD}\ @\ 100kHz}{F_{sw}} = 13\text{nC} + \frac{80\text{mA}}{20\text{kHz}} \approx 13\text{nC} \tag{3.5}$$

  where Q_G is the gate charge of the SiCFET, I_{VDD} is the current consumption of the channel, and F_{sw} is the operating switching frequency. The required minimum value of C_{BOOT} is hence,

$$C_{BOOT} = \frac{Q_{total}}{\Delta V_{DD}} = \frac{13\text{nC}}{0.5\text{V}} = 26\text{nF} \tag{3.6}$$

  In practice, a larger C_{BOOT} is used to account for possible transients in the bootstrap circuit. Hence, a 50 V **1 µF** capacitor is selected. An additional 100 nF bypass capacitor is placed in parallel to further lower the AC impedance for a wide frequency range.

- **Bootstrap diode**: The D_{BOOT} turns ON every cycle when the low-side transistor is switched ON to charge the C_{BOOT}. High currents flow through this diode and can result in significant transient conduction losses, which can be minimised with smaller forward voltage drops. Reverse recovery losses in the diode can be reduced with lower junction capacitances. A high-voltage fast-recovery SiC Schottky diode C4D05120E is selected for this purpose due to its low forward voltage of 1.4 V and high peak current capacity of 10 A. It has a DC blocking voltage of 1200 V which is suitable for 1000 V operation with a safety margin of 20%.

- **Bootstrap resistor**: The R_{BOOT} limits the current drawn from V_{DD} and prevents any over-current damage to D_{BOOT}. However larger resistance values would slow the charging time of C_{BOOT}. With an R_{BOOT} of 2.2 Ω the current $I_{BOOT_{pk}}$ would be,

$$I_{BOOT_{pk}} = \frac{V_{DD} - V_{BDF}}{R_{BOOT}} = \frac{20\text{V} - 2.5\text{V}}{2.2\Omega} \approx \mathbf{8}\ \text{A} \tag{3.7}$$

  where V_{DD} is the output biasing supply of the driver, and V_{BDF} is the estimated forward voltage of D_{BOOT} at 8 A.

- **Gate output resistors**: The resistances R_{ON} and R_{OFF} trim the source and sink currents so as to ensure efficient switching of the power transistor. During turn ON, only R_{ON} limits the source current which charges the gate capacitance of the transistor. During turn OFF, the parallel combination of both R_{ON} and R_{OFF} allow for larger sink currents to discharge the gate capacitance. The datasheet of UCC21521 shows the internal pull-up structure of the output stage which consists of a P-channel MOSFET and parallel N-channel MOSFET. The expected source currents of high-side and low-side channels with an R_{ON} of 2.2 Ω are,

$$I_{H+} = \frac{V_{DD} - V_{BDF}}{R_{NMOS} \parallel R_{OH} + R_{GFET}} = \frac{20\text{V} - 0.8\text{V}}{1.47\Omega \parallel 5\Omega + 2.2\Omega + 14\Omega} \approx \mathbf{1.2}\ \text{A}$$

$$I_{L+} = \frac{V_{DD}}{R_{NMOS} \parallel R_{OH} + R_{GFET}} = \frac{20\text{V}}{1.47\Omega \parallel 5\Omega + 2.2\Omega + 14\Omega} \approx \mathbf{1.3}\ \text{A}$$

  where R_{NMOS} is the resistance of the internal transistor specified as 1.47 Ω, R_{OH} is the internal resistance of the high-channel specified as 5 Ω, and R_{GFET} is the internal gate resistance of the SiCFET specified as 14 Ω. With MSS1P4 selected as D_{OFF} the sink currents can be calculated as,

$$I_{H-} = \frac{V_{DD} - V_{BDF} - V_{GDF}}{R_{OL} + R_{OFF} \parallel R_{ON} + R_{GFET}} = \frac{20\text{V} - 0.8\text{V} - 0.75\text{V}}{0.55\Omega + 0\Omega + 14\Omega} \approx \mathbf{1.3}\ \text{A}$$

$$I_{L-} = \frac{V_{DD} - V_{GDF}}{R_{OL} + R_{OFF} \parallel R_{ON} + R_{GFET}} = \frac{20\text{V} - 0.75\text{V}}{0.55\Omega + 0\Omega + 14\Omega} \approx \mathbf{1.3}\ \text{A}$$

  where V_{GDF} is the forward voltage drop of the anti-parallel diode MSS1P4 specified as 0.75 V, and R_{OL} is the internal resistance of the low-channel specified as 0.55 Ω. Higher currents can be achieved with a higher supply voltage V_{DD} or with a lower R_{GFET} SiCFET.

- **Dead-time resistor**: The required dead-time is calculated as,

$$T_{DT} = [(T_{DOFF}^{max} - T_{DON}^{min}) + (T_{PD}^{max} - T_{PD}^{min})] \times 1.2 \tag{3.8}$$

Where T_{DOFF}^{max} is the maximal turn-off delay time, T_{DON}^{min} is the minimal turn-on delay time, T_{PD}^{max} is the maximal propagation delay, and T_{PD}^{min} is the minimal propagation delay. Substituting values from the datasheet,

$$T_{DT} = [(7\text{ns} + 10.4\text{ns} - 6\text{ns} + 5.4\text{ns}) + (30\text{ns} - 19\text{ns})] \times 1.2 \approx \mathbf{20}\text{ns}$$

A larger dead-time of 200ns is selected to ensure zero shoot-through current during switching. The value of R_{DT} for this setting $DT_{setting}$ is,

$$R_{DT}\ in\ \text{k}\Omega = \frac{DT_{setting}}{10} = \frac{200\text{ns}}{10} = \mathbf{20}\text{k}\Omega \tag{3.9}$$

The DT pin of UCC21521 is held at an internal voltage of 0.8 V and the current drawn from R_{DT} is measured for setting the dead-time. A 2.2 nF ceramic capacitor is placed in parallel with R_{DT} to support this voltage.

- **Power losses**: The power loss in the gate driver P_G determines safe operation of the UCC21521 within thermal limits. It consists of static power loss P_{GDQ} and switching power loss P_{GDO} calculated as,

$$P_{GDQ} = V_{CCI} \times I_{CCI} + V_{DDA} \times I_{DDA} + V_{DDB} \times I_{DDB}$$

$$P_{GDQ} = 5\text{V} \times 3\text{mA} + 20\text{mA} \times 2\text{mA} + 20\text{V} \times 2\text{mA} \approx \mathbf{95}\text{ mW}$$

Where the currents I_{CCI}-I_{DDA}-I_{DDB} are the currents drawn from the sources V_{CC} and V_{DD} respectively. Their worst-case values are estimated to be 3 mA and 2 mA. Next, the total dynamic loss P_{GSW} is given by,

$$P_{GSW} = 2 \times V_{DD} \times Q_G \times F_{sw} = 2 \times 20\text{V} \times 13\text{nC} \times 20\text{kHz} \approx \mathbf{10}\text{mW}$$

This is used to determine the values of R_{eq} (a factor) and P_{GSW} as,

$$R_{eq} = \left[\frac{R_{OH} \parallel R_{NMOS}}{R_{OH} \parallel R_{NMOS} + R_{ON} + R_{GFET}} + \frac{R_{OL}}{R_{OL} + R_{OFF} \parallel R_{ON} + R_{GFET}} \right]$$

$$\Rightarrow R_{eq} \approx 0.18 \Rightarrow P_{GDO} = P_{GSW} \times R_{eq} = 10\text{mW} \times 0.18 \approx \mathbf{1.8}\text{ mW}$$

Finally, the total gate driver loss P_G is calculated as,

$$P_G = P_{GDQ} + P_{GDO} = 95\text{mW} + 1.8\text{mW} \approx \mathbf{100}\text{mW} \tag{3.10}$$

3.3.3 *Proto-Hx: Complete H-bridge PCB*

With the learning outcomes of Proto-H1 and the results from T1 and T2, the next step is to build a prototype with the entire H-bridge. By bringing all the components onto a single board, the stray inductances are effectively minimised for better performance. The PCB consists of two parts, the power stage operating at high-voltage (above 1000 V) and the signal stage operating at low-voltage (3.3 to 25 V). The power stage shown in Fig. 3.11 consists of the input terminals DC+ and DC-, the DC link capacitors CDC1-CDC2 connected in parallel, the four SiCFETs S1-S2-S3-S4 connected in an H-bridge topology, the commutation capacitors CC1-CC2 connected across the switches, and the output terminals PUL+ and PUL-. Since the operational voltage levels of the power stage can exceed 1000 volts, strict guidelines must be carefully followed when deciding the component placements and connections. Some of these rules are provided in the IPC-22221 standard [56] while others are based on general rules of thumb. Due to high current ratings in the range of several amperes, brass M3 terminals are used for the inputs and outputs. The high-voltage X7R MLCC commutation capacitors reduce the effective inductance of the commutation loop thereby improving the switching performance of the SiCFETs [57]. The switches are controlled through gate pulses sent from the signal stage, referenced to DC- for low-side and PUL+ or PUL- for high-side.

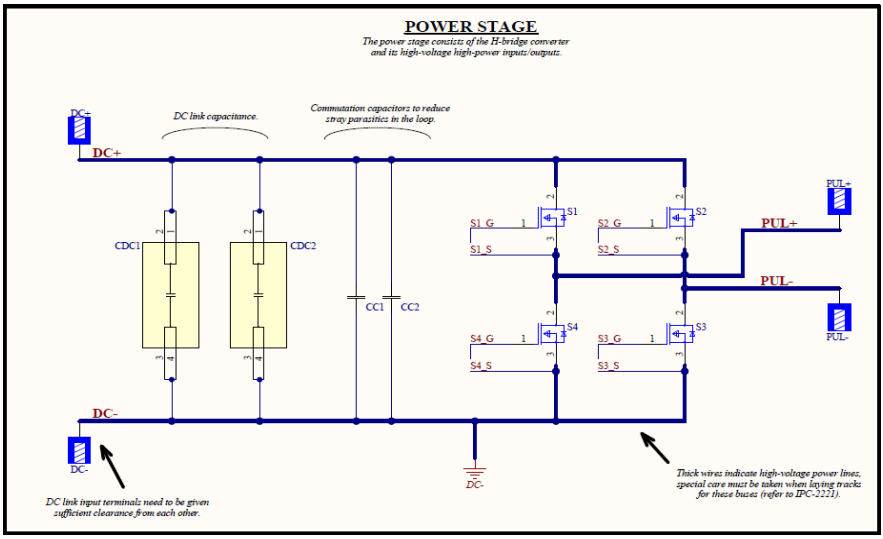


FIGURE 3.11: Schematic of the power stage of Proto-Hx

The signal stage shown in Fig. 3.12 consists of the gate drivers UD14-UD23 for the switch arms S1-S4 and S2-S3 respectively, the isolated DC-DC converters US14-US23 for the drivers UD14-UD23 respectively, and the jumpers JE14-JE23-JP14-JP23 to acquire signal inputs from the Arduino. The modifications in gate driver circuitry from Proto-H1 are the addition of a current-limiting 51 Ω resistor at the ENABLE pin and the addition of R_{OFF}-D_{OFF} to improve switch OFF times of the SiCFET. The diode used for this purpose is the Vishay MSS1P4. The MGJ2D052005SCs isolate the $V_{CC} = 5V$ to a $V_{DD} = 20V$ for biasing the gate driver outputs. The capacitors C10-C11-C16-C17 support these voltages and the LEDs provide a visual indication check during operation. The pulse signals PWM1-PWM4 and PWM2-PWM3 are fed through jumpers JP14 and JP23 respectively. The signals EN14-EN23 are fed through JE14-JE23 and can disable each driver separately if needed such as in short-circuit conditions. Unlike the Proto-H1 which was powered from the Arduino, the Proto-Hx needs to be powered from a voltage source through the VCC+ and VCC- banana plugs. The ground of the Arduino must hence be connected to the ground of this source, which can be done via the third pins of JE14 and JE23. The lengths of high-frequency signal carrying traces must be kept as short as possible so as to minimise loop inductances that cause attenuation. The voltage ratings of all capacitors in the signal stage are 50V and the power ratings of all resistors are 125mW. All components are selected in the standard 0805 package, apart from the 10µF capacitors which are in the 1812 package.

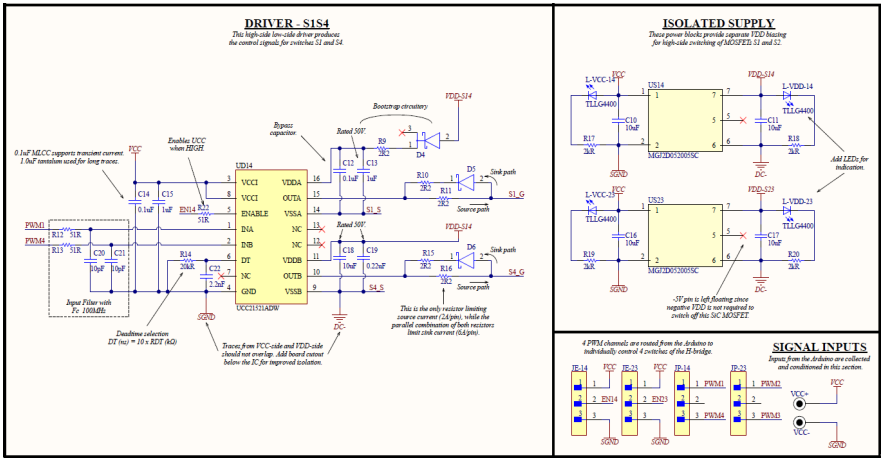
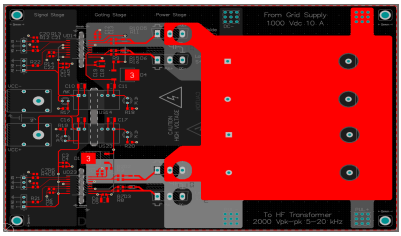
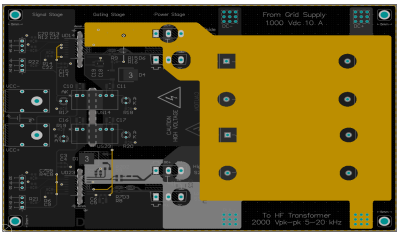


FIGURE 3.12: Schematic of the signal stage of Proto-Hx (Driver-S2S3 not shown)

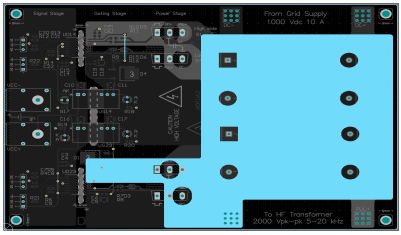
The 4-layer 17cm x 12cm PCB layout of the Proto-Hx is shown in Fig. 3.13. The top layer (red) has signal traces with the DC+ polygon pour while the bottom layer (dark blue) has the signal ground and DC- polygon pours. The sections and components of the printed PCB are shown in Fig. 3.14.



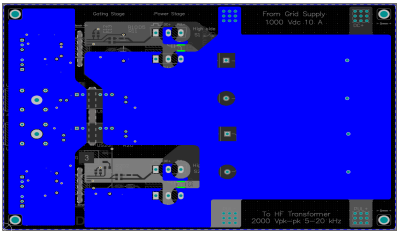
(a) Top layer with DC+



(b) Middle-top layer with PUL+



(c) Middle-bot layer with PUL-



(d) Bottom layer with DC-

FIGURE 3.13: PCB layout of Proto-Hx in Altium Designer

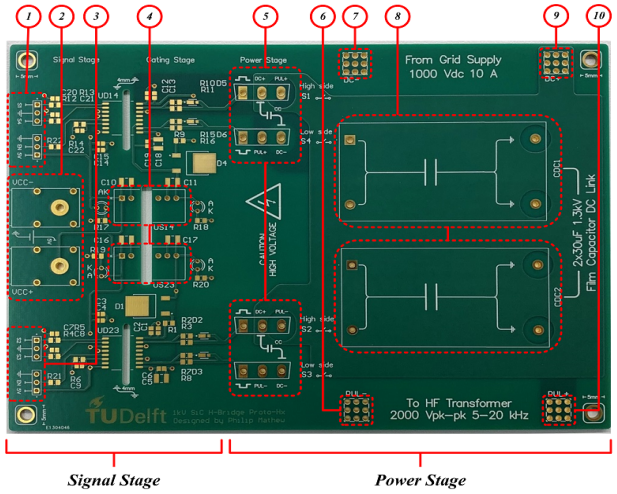


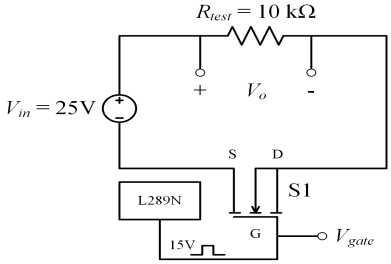
FIGURE 3.14: Printed PCB of Proto-Hx

3.4 EVALUATION TESTS

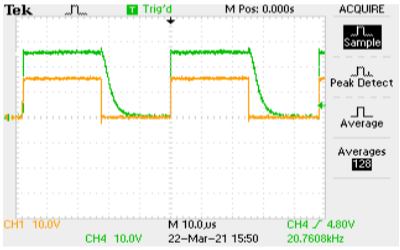
Two evaluation tests were conducted to study the individual characteristics of the IMW120R140 SiC MOSFET and the UCC21521ADW ProtoH1. The power supply was provided from a Keysight E36313A 25V/2A Programmable DC Supply. A Tektronix 100MHz 1GS/s TDS-2014B oscilloscope was used for recording the waveforms via the OpenChoice Desktop application in Windows. The results from these tests are presented and analysed in this subsection.

3.4.1 *T1: SiCFET with L289N driver*

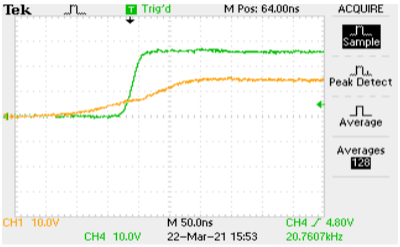
In this test, the switching characteristics of the IMW120R140 SiCFET was studied by driving it with the L289N Dual Full-bridge driver (datasheet) as shown in Fig 3.15a. The recorded waveforms are shown in Fig. 3.15.



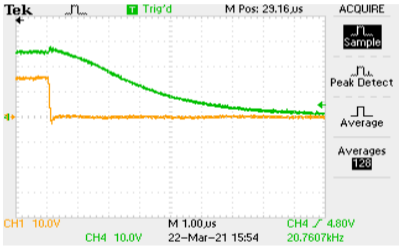
(a) Evaluation test circuit and outputs
V_o = *Green channel*
V_g = *Yellow channel*



(b) Voltage switching waveform
$V_o: \ Y = 10V/div \ X = 10\mu s/div$
$V_g: \ Y = 10V/div \ X = 10\mu s/div$



(c) Rising characteristic waveform
$V_o: \ Y = 10V/div \ X = 50ns/div$
$V_g: \ Y = 10V/div \ X = 50ns/div$



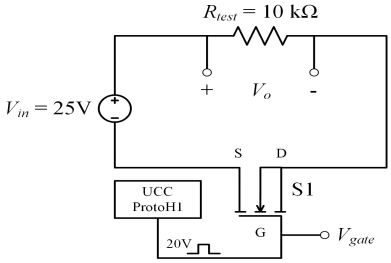
(d) Falling characteristic waveform
$V_o: \ Y = 10V/div \ X = 1\mu s/div$
$V_g: \ Y = 10V/div \ X = 1\mu s/div$

FIGURE 3.15: IMW120R140 switching characteristics with L289N driver

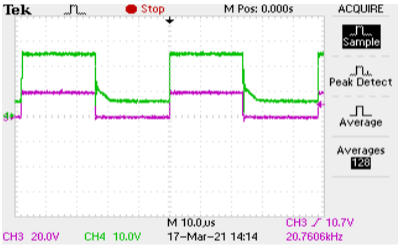
An interesting observation in Fig. 3.15c is that although it is the L289N that drives the SiCFET, it is the SiCFET that completes its rise (~25ns) before the L289N (~150ns). This demonstrates the superior switching capabilities of SiC MOSFETs. From Fig. 3.15d it can be seen that the switch takes much longer to switch-off (~9µs) even though the pulse from the L289N has turned low. This is due to the poor sink current capabilities which is required to discharge the gate-source capacitance C_{GS} quickly.

3.4.2 *T2: SiCFET with Proto-H1*

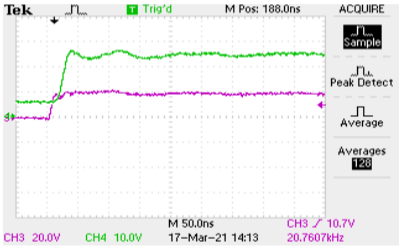
In this test, the output characteristics of the UCC21521ADW and its synergy with the IMW120R140 SiCFET was studied with the test circuit shown in Fig 3.16a. The high-side output of the ProtoH1 was used to test the functionality of the bootstrap circuit (hence the observed DC offset of the waveform). The recorded waveforms are shown in Fig. 3.16.



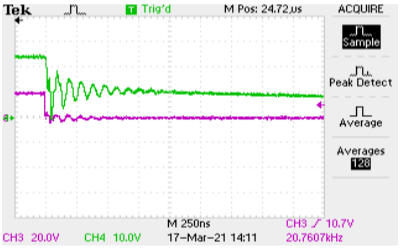
(a) Evaluation test circuit and outputs
V_o = *Green channel*
V_g = *Purple channel*



(b) Voltage switching waveform
$V_o: \ Y = 10V/div \ X = 10\mu s/div$
$V_g: \ Y = 20V/div \ X = 10\mu s/div$



(c) Rising characteristic waveform
$V_o: \ Y = 10V/div \ X = 50ns/div$
$V_g: \ Y = 20V/div \ X = 50ns/div$

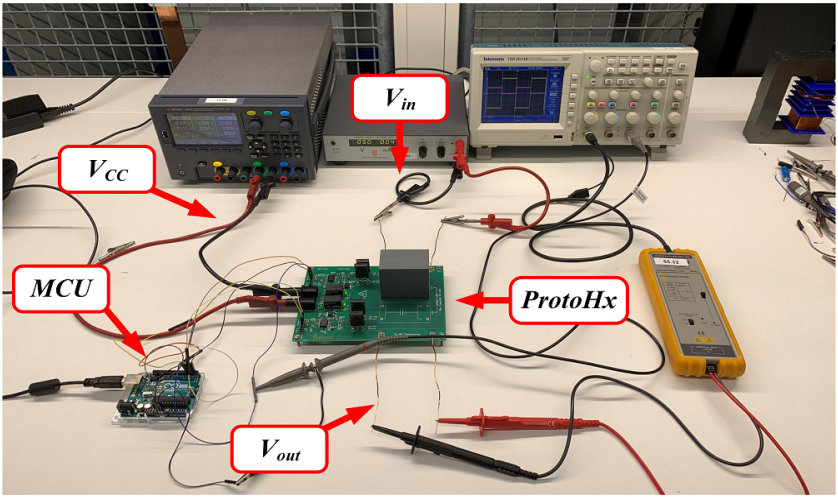


(d) Falling characteristic waveform
$V_o: \ Y = 10V/div \ X = 250ns/div$
$V_g: \ Y = 20V/div \ X = 250ns/div$

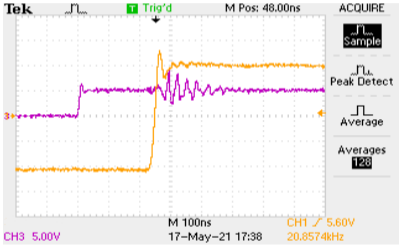
FIGURE 3.16: IMW120R140 switching characteristics with UCC21521ADW driver

3.4.3 *T3: Low-voltage response of Proto-Hx*

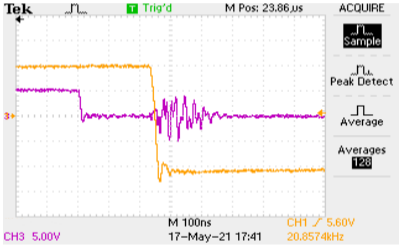
In this test, the output characteristics and capabilities of the ProtoHx were tested at the 300V voltage level. The test setup is shown in Fig. 3.17a. A separate Delta Elektronika ES 0300 (300 V, 450 mA) was used to supply a $V_{in} = 200V$ to Proto-Hx. The output V_{out} (yellow waveform) was observed using a differential probe with a 200x attenuation. The results show that the Proto-Hx is capable of producing pulses with rise-fall times of 100ns. This would provide much-needed flexibility when optimising the parasitics of the transformer, the design of which will be described in the next chapter.



(a) Test setup with the Proto-Hx



(b) Rising characteristic waveform
$V_o : Y = 100V/div\ X = 100ns/div$
$V_g : Y = 5V/div\ X = 100ns/div$



(c) Falling characteristic waveform
$V_o : Y = 100V/div\ X = 100ns/div$
$V_g : Y = 5V/div\ X = 100ns/div$

FIGURE 3.17: Low-voltage Proto-Hx response (probe has 200x attenuation)

4

PULSE TRANSFORMER

An ideal transformer has zero distortion, but there are zero ideal transformers.

Rob Elliot
Elliot Sound Products

The pulse modulator is the system that ultimately replicates the voltage waveforms to be used in the ageing experiments. It consists of the pulse driver designed in Chapter 3 and a medium-frequency pulse transformer which, in the context of this thesis project, steps up the 230 V bipolar pulses to the 10 kV voltage level. Special care has to be taken to control and minimise the parasitics of this transformer so as to ensure that the final output of the modulator satisfies required criteria. The subsequent sections of this chapter describe the related theory, the derivation of a modulator circuit model, the design tradeoffs to be considered, the evaluation of parasitics, selection of bobbin geometry, and analysis of failure modes.

4.1 THEORETICAL BACKGROUND

4.1.1 *Brief history of pulsed power applications*

It is quite uncommon to not have heard of a transformer in today's world. From blaming a distribution transformer failure for power-cuts to thanking power transformers for enabling long-distance transmission, this simple but yet powerful device has played a pivotal role in the field of electrical power engineering. This importance stems from the essential need for us power engineers to be able to "transform" voltages or currents in the grid as and when necessary. Because of this, a diverse array of transformers of several shapes and sizes have been employed in various parts of the power system. The underlying principle common to all these transformer types and topologies was discovered more than two centuries ago by a British scientist, M. Faraday [58]. In 1831, Faraday discovered that current could be transferred between two independent coils by simply passing a varying current through one coil and "linking" this changing magnetic flux to the second coil. This phenomenon, termed as electromagnetic induction, would go on to be the cornerstone of future electromagnetic technology

such as motors and transformers. The first modern transformer (one of constant-potential) was invented in 1885 by three Hungarian electrical engineers, O. Bláthy, M. Déri and K. Zipernowsky, at the Ganz Factory in Budapest [59]. Although, its intricate toroidal winding geometry made it difficult to manufacture with the machines available at the time. It was later that year when three American engineers of the Westinghouse factory at Pittsburgh W. Stanley, A. Schmid, and O. B. Shallenberger perfected the design to build the classic E-I cored transformer that we know of today. Since then, transformers have become the bare essential component of any AC-dominated power system [60]. The biggest characteristic feature of these 50Hz or 60Hz transformers was, of course, their bulk. But this fact was not a significant issue in grid-related applications since there always was ample space available in, say, sub-stations. However as electrical systems gradually began to miniaturize towards electronic systems, such as in the field of communications, the dimensional constraints became a growing concern. The true game-changer was the development of radar technology in 1935 soon before the second World War began. The US radar systems used during the war, the SCR-268 and SCR-270 shown in Fig. 4.1, operated at peak powers of 50 kW and 100 kW respectively [61]. In order to make these radar systems airborne, power was supplied to the microwave magnetrons in the form of high speed quasi-rectangular voltage pulses, which were just a few microseconds wide with a repetition rate of around 1000 pulses per second [62]. At the heart of those systems were the pulse generators, quite similar to the one developed for the purpose of this thesis.

FIGURE 4.1: An SCR-268 at Henderson Field, Guadalcanal [61]

With the developments in semiconductor devices in the 20th century, pulsed power applications grew rapidly in number ranging in their peak volt-per-second and peak power capabilities, as shown in 4.2. It was S. Levy *et al.* in 1992 that gathered and described 66, later 100, of these applications in their highly cited symposium paper [63]. An important application is in the field of bioelectrics, wherein pulsed electric fields of several kVs per cm over microsecond durations are used to instill reversible electroporation of cellular membranes (which are dielectric in nature). With this, scientists are capable of controlling the internal functions and membrane transport processes in cells [64]. This phenomenon has also been extended into the treatment of cancer cells by delivering pulses above a certain lethal threshold to clear tumors [65]. The conventional water treatment technologies have mostly involved the addition of chemicals or antimicrobial agents. Owing to their precise control over physical and chemical reactions, pulsed power systems have gained significant traction over the years in the replacement of these archaic methods. Pulses of 50kV-150kV in the nanosecond timescale result in degradation and later inactivation of E. coli. bacteria [66]. Additionally, the authors of [67] showed that 1.5kW pulsed corona streamer discharges are highly effective in removing harmful toxins from exhaust gases such as in electrostatic precipitators. A review of various industrial applications of pulse generators has been presented in [68].

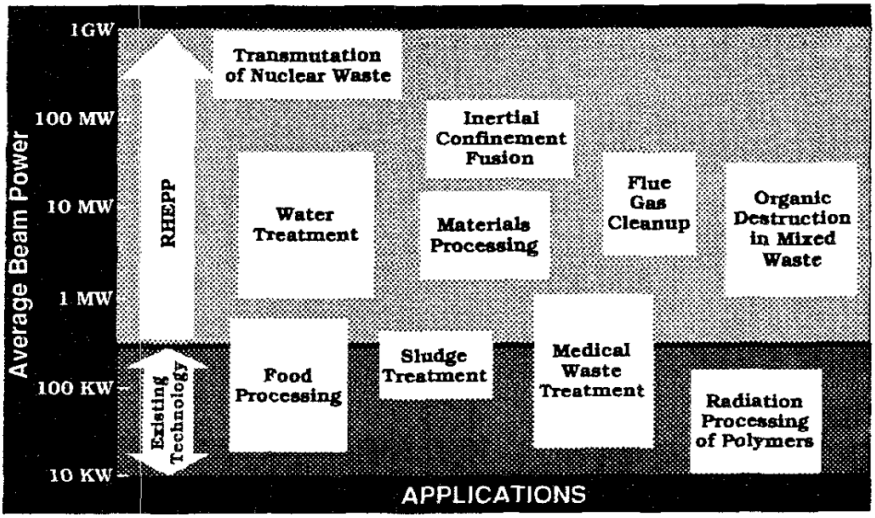


FIGURE 4.2: Typical pulsed power applications summarised by SNL [69]

4.1.2 *Literature on pulse transformer design*

The IEEE took a first step in 1987 towards standardising pulse transformers by publishing the "ANSI/IEEE Standard 390", with its latest revision in 2007 [70]. This standard forms the basis of many equations and considerations used for this thesis. The books written by P. W. Smith [71], G. A. Mesyats [72], and H. Bluhm [73] have provided a solid foundation to learn the fundamental principles related to pulse transformers. Building further on these concepts, several authors have carried out significant research, discussed in the following paragraphs.

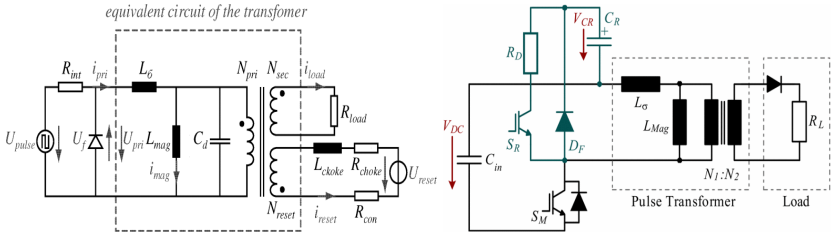
D. Bortis (ETH Zürich, Switzerland) carried out extensive work in achieving faster and sharper output pulses from pulse transformers. In [74], the authors determined an optimal design of a DC reset circuit, as shown in 4.3a. Since the pulses in HF-transformer systems are usually unipolar in nature, the magnetic core of the transformer is not optimally utilised due to a positive remnant flux. A reset circuit supplies opposing flux into the core resulting in a negative remnant flux and thereby almost twice the operable region on the hysteris curve. Although the DC reset circuit is the most simple and common method of resetting the core, it results in significant losses due to high stresses over the freewheeling diode. In [75], the authors designed an alternative active reset circuit as shown in 4.3b. Through controlling the switch S_R the energy stored in capacitor C_R can be transferred into the magnetizing inductance L_{Mag} of the pulse transformer to pre-magnetize its core. After the transfer of the pulse to the secondary, the energy in L_{Mag} is restored back into C_R for the next cycle. For his doctoral thesis [47], D. Bortis designed an IGBT-based 20MW power modulator to generate 170kV pulses with rise times less than 500ns. Pulse widths of 120ns with a maximum repetition rate of 600Hz were achieved through a powerful plug-in gate driver.

Perhaps his most significant work relevant to this thesis was in describing a detailed design procedure for pulse transformers with fast-rise times [76]. The authors demonstrated the influence of inductive and capacitive parasitic elements on waveform parameters such as overshoot and rise-time. Next, the article discusses appropriate construction techniques such as different winding arrangements to reduce these parasitics. Finally, the distributed capacitance is determined from regional energy calculations of the transformer tank, and the leakage inductance is determined through Finite Element Analysis (FEA). The methods provided in this article will be discussed later in Section 4 of this thesis.

S. Candolfi. (Université Laval, Canada) explored the application of FEA in optimizing pulse transformer design. The authors of [77] evaluated the effect of age on the breakdown strengths of two silicon oil variants, MIDEL 7131 and RHODORSIL, and used these results to identify weak points in the pulse transformer insulation. As an alternative to the methods proposed in [76], a CAD environment was presented in [78] which can carry out direct non-linear optimization of transformer design parameters based on two-dimensional (2D) and three-dimensional (3D) FEA. The model was tested on a prototype pulse transformer, and the outputs were verified using the experimental procedures presented in [79]. Another FEA-based optimization algorithm was presented in [80], but this time using a correction factor to align the less-accurate but faster 2D model with the more-accurate but slower 3D model. Through appropriate calibration of these correction factors, the time taken for the 3D model to achieve convergence was effectively reduced. Finally in [81], 3D FEA was applied to a prototype pulse transformer to identify a high-order generalized equivalent circuit (HOGEC), and compare this HOGEC with the low-order IEEE Standard equivalent model in [70]. This was done by decomposing the transformer into n elementary windings each associated with a certain node number. While the inductive HOGEC network (4.4a) was constructed by associating the inductances and magnetic coupling factors of these elements , the capacitive HOGEC network (4.4b) was constructed by associating the capacitances and capacitive influence coefficients. Then these two networks were combined by adding resistances in series with the inductances and in parallel with the capacitances, to produce a final HOGEC which can be described with a simple netlist. The identified HOGEC was shown to be more efficient than the IEEE circuit, hence providing a method to study the influence of mechanical parameters and winding spatial configuration on the internal dynamics.

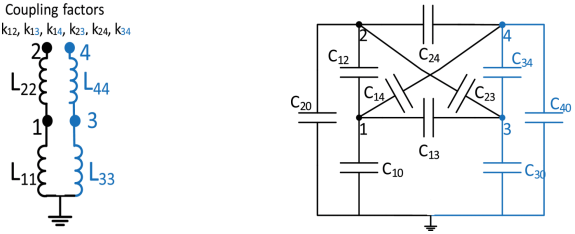
J. Biela (ETH Zürich, Switzerland) worked on perfecting the analytical model of pulse transformers to accurately capture the effect of the underlying parasitics. In [82], the authors model the capacitive parasitics using six equivalent capacitors, each correlating to a specific region in or around the conical transformer windings as shown in 4.5a. The capacitance values are calculated from the distributed energies stored in these regions which are determined analytically. With this model, designers can alter specific parameters such as winding height so as to accurately predict the distortion in output pulses. The energies from this cut-section represent per-unit-length energies, and was hence multiplied with the dimensions shown in

4.5b to obtain the total energy. This work is further expanded in [83] with validation of results using 2D FEA. These equations are applicable to both non-parallel and parallel plate winding arrangements.



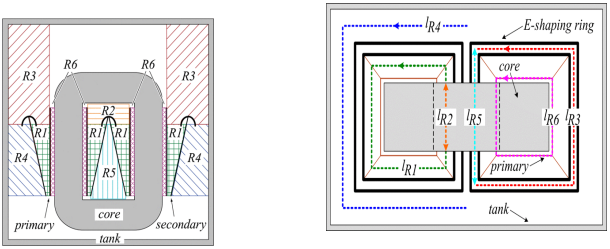
(a) The DC reset circuit [74] (b) The active reset circuit [75]

FIGURE 4.3: Pulse transformer reset circuits designed by Bortis *et al.*



(a) The inductive HOGEC (b) The capacitive HOGEC

FIGURE 4.4: HOGEC networks identified by Candolfi *et al.* [81]



(a) Division of pulse transformer tank into relevant regions (b) Transformer length definitions for obtaining total energy

FIGURE 4.5: Parasitic capacitance modelling by Biela *et al.* [82]

4.2 DERIVING AN EQUIVALENT MODULATOR MODEL

Owing to their diverse application set, pulse modulators have been widely studied resulting in several equivalent models that can accurately predict the output waveform at a certain operating point. The most commonly used model is that provided in the IEEE 390 standard [70] as shown in Fig 4.6 (a). It should be noted that the output load is modified to Z_{load} instead of R_{load} for the purposes of this thesis. The elements in the circuit include,

- An ideal transformer with turns ratio n
- An ideal pulse generator of peak magnitude U_g
- The primary and secondary winding resistances R_{11}-R_{21}
- The primary and secondary leakage inductances L_{11}-L_{21}
- The primary and secondary distributed capacitances C_1-C_2
- The interwinding capacitance C_{12} between primary-secondary windings
- The core-loss resistance R_c and magnetising inductance L_m

In the time-domain, a single pulse can be divided into three unique portions *viz.* the leading edge T_1, the pulse top T_2, and the trailing edge T_3. The circuit dynamics during each of these time durations can be independently studied through separate circuits as shown in Fig 4.6 (b). In these circuits, all parasitic elements have been referred to the secondary and lumped into the elements L_σ and C_d while assuming that $n >> 1$. The duration T_1 contains high-frequency components which allow the removal of R_c-L_m since there is no influence of the core material in such a short time. The duration T_2 contains only low-frequency components allowing the series L_σ and shunt C_d to be removed. The "droop" of output voltage depends on the pulse width t_p and the time constant L_m/R_g and should satisfy,

$$\frac{t_p}{\tau} = \frac{t_p}{L_m/R_g} < 0.2 \tag{4.1}$$

Finally in T_3 all inductive and capacitive elements need to be returned to the circuit since they possess stored energy. The flow of this energy through the circuit causes the fall of output voltage, followed by "ringing" and eventual decay to zero. Since we are interested in the rise-time and overshoot, an equation for duration T_1 will be derived in the next sub-sections.

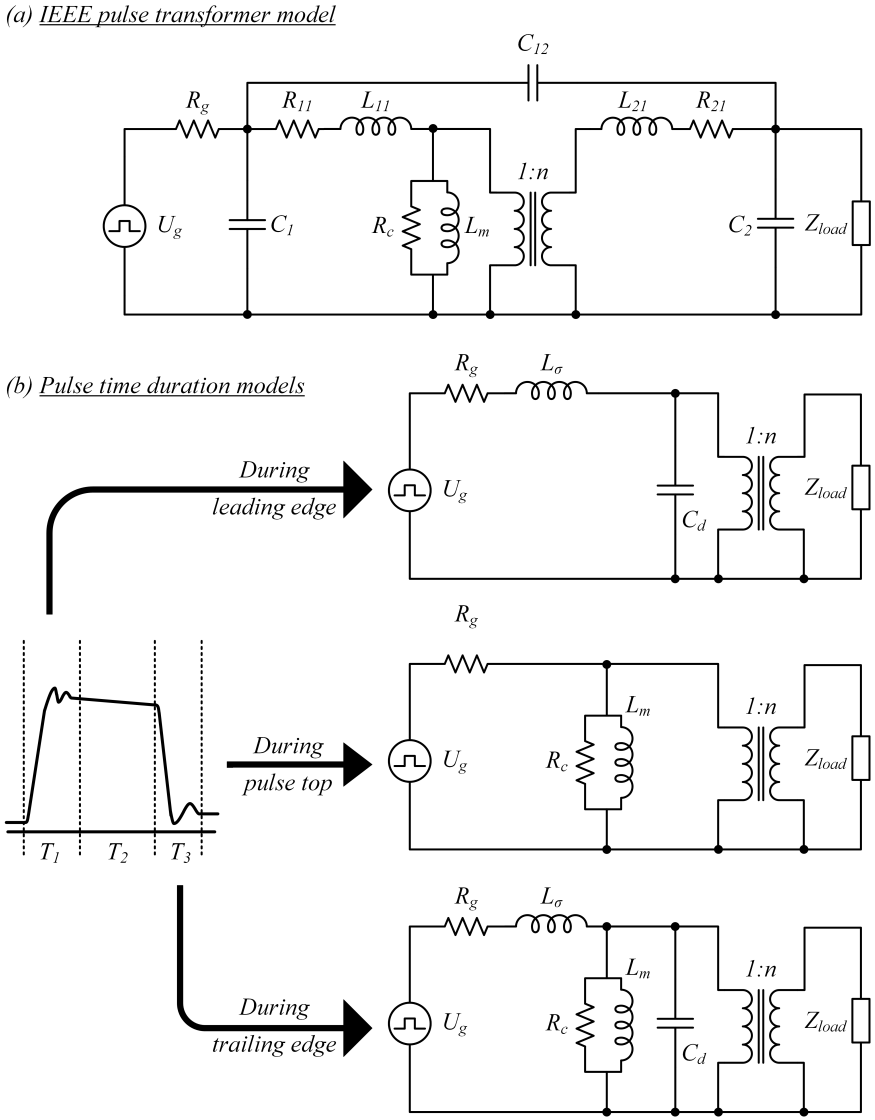


FIGURE 4.6: (a) The complete IEEE equivalent circuit for a pulse transformer and (b) splitting into three circuits for modelling characteristics during different time durations of the output pulse

4.2.1 *For resistive (klystron) loads*

One of the earliest influential literature related to pulse generators was the fifth volume of the MIT Radiation Laboratory Series published in 1948 [84]. These volumes were written after the end of World War II due to efforts by the US governments efforts to promote key researchers to write about their work. The writings of W. H. Bostick in Chapter 14 Volume 5 of this series were on deriving an equation for the leading edge of the output voltage. These combined with the works of D. Bortis in his PhD thesis [47] are described here in the form of a derivation. We first begin with the leading-edge circuit as in Fig. 4.7 (a) with a resistive load and its Norton-equivalent in Fig. 4.7 (b). The output voltage $U_o(s)$ can then be expressed as,

$$U_o(s) = \frac{U_g}{s} \cdot \frac{1}{R_g + sL_\sigma} \times \frac{1}{\frac{1}{R_{load}} + sC_d + \frac{1}{R_g + sL_\sigma}}$$

$$U_o(s) = \frac{U_g}{s} \times \frac{R_{load}}{s^2 C_d L_\sigma R_{load} + s(C_d R_g R_{load} + L_\sigma) + (R_g + R_{load})}$$

$$U_o(s) = \frac{U_g}{s \times C_d L_\sigma} \times \frac{1}{s^2 + s\frac{C_d R_g R_{load} + L_\sigma}{C_d L_\sigma R_{load}} + \frac{R_g + R_{load}}{C_d L_\sigma R_{load}}}$$

$$U_o(s) = \frac{U_g}{s \times C_d L_\sigma} \times \frac{1}{s^2 + s\left(\frac{R_g}{L_\sigma} + \frac{1}{C_d R_{load}}\right) + \frac{1}{L_\sigma C_d}\left(1 + \frac{R_g}{R_{load}}\right)}$$

The quadratic equation in the denominator can be simplified with the variables a and b assigned as per the form $s^2 + 2as + b$.

$$2a = \frac{R_g}{L_\sigma} + \frac{1}{C_d R_{load}} \quad , \quad b = \frac{1}{L_\sigma C_d}\left(1 + \frac{R_g}{R_{load}}\right) \tag{4.2}$$

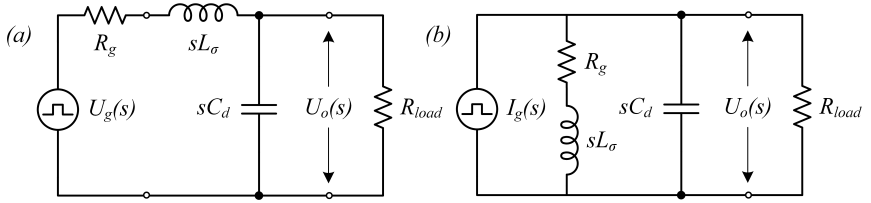


FIGURE 4.7: Equivalent circuit of pulse modulator with resistive load

The next step is to split the polynomial into a partial fraction of the form,

$$\frac{1}{s(s^2+2as+b)} = \frac{A}{s} + \frac{B(s+a)+c}{(s+a)^2+\omega^2}$$

where $\omega^2 = b - a^2$ and the solution in time-domain is found to be,

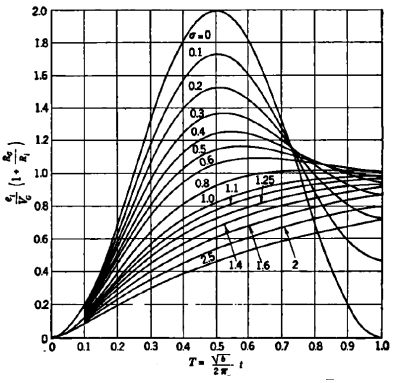
$$u_o(t) = \frac{U_g R_{load}}{R_g + R_{load}} \left[1 - e^{-at} \left(\frac{a}{\omega} sin\omega t + cos\omega t \right) \right] \tag{4.3}$$

The damping coefficient σ is then defined as,

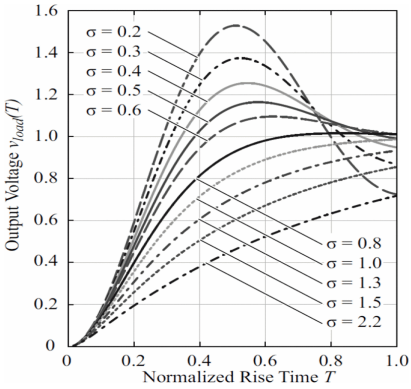
$$\sigma = \frac{a}{\sqrt{b}} = \frac{C_d R_g R_{load}}{2\sqrt{R_{load} L_\sigma C_d (R_g + R_{load})}} \xrightarrow[R_g \approx 0]{assuming} \sigma = \frac{1}{2R_{load}} \sqrt{\frac{L_\sigma}{C_d}} \tag{4.4}$$

The transient output waveform is plotted against the normalised time axis $T = \frac{\sqrt{b}}{2\pi} t$ in Fig. 4.8. It can be seen that a higher damping σ produces lesser overshoot but also slower rise-times T_r. Hence an optimum balance (usually at $\sigma = 0.75$) must be found between minimising T_r while constraining the overshoot. This tradeoff is expressed analytically in terms of transformer parasitics L_σ and C_d through the following equations derived in [47].

$$2R_{load} \cdot \sigma = \sqrt{\frac{L_\sigma}{C_d}} \quad , \quad T_r = 2\pi \cdot T_{10\%-90\%} \sqrt{L_\sigma C_d} \tag{4.5}$$



(a) Considering effect of R_g [84]



(b) Neglecting effect of R_g [47]

FIGURE 4.8: Effect of circuit elements on the rise-characteristics of the pulse

It is clear that reducing the rise-time involves minimising the parasitic product $L_\sigma C_d$ while ensuring lesser overshoots depends on the parasitic ratio $\frac{L_\sigma}{C_d}$ of the transformer. There exists several methods to achieve this described in [76]. The parasitic ratio can be improved through mechanical design choices, but the parasitic product is defined solely by the topology of the transformer connections. The leakage inductance L_σ stems from the energy stored in the magnetic field $|\overrightarrow{H}|$ in the volume between the primary and secondary windings. It was shown in [47] that this depends on the primary turns N_p, winding length l_w, winding distance d_w, and core height h_k as follows,

$$L_\sigma \propto K_{L_\sigma} \cdot \mu \cdot \frac{N_p^2 \cdot l_w \cdot d_w}{h_k} \tag{4.6}$$

The parasitic capacitance C_d on the other hand depends on the energy stored in the electric field $|\overrightarrow{E}|$ directed horizontally from the primary winding to the secondary winding. This therefore depends on the turns ratio $n = \frac{N_s}{N_p}$ and the geometrical distances as follows,

$$C_d \propto K_{C_d} \cdot \epsilon \cdot n^2 \cdot \frac{l_w \dot{h}_w}{d_w} \tag{4.7}$$

The factors K_{L_σ} and K_{C_d} for different winding configurations are shown in Table 4.1, from which it can be seen that the conical winding improves both L_σ and C_d. Apart from this, the parasitic product can be altered through interconnection of pulse transformers or by utilising multiple cores. It can hence be concluded that the procedure for building a fast-rise pulse modulator for resistive loads is relatively simple and straightforward, as long as the underlying tradeoffs are carefully considered. With a capacitive load, however, there are additional dynamics (of the third-order) that must be studied to predict the output waveform. This has not been explored previously, and will be dealt with for the first time in the next sub-section.

WINDING GEOMETRY	K_{L_σ}	K_{C_d}	EFFECTIVE $L_\sigma C_d$ PRODUCT
Parallel	1	$\frac{1}{3}$	$\frac{1}{3}$
Conical	$\frac{1}{2}$	$\frac{1}{2}$	$\frac{1}{4}$
Foil	$\frac{1}{2}$	$(k+1)$	$\frac{k+1}{2}$

TABLE 4.1: Effective parasitic products for three winding configurations [76]

4.2.2 *For capacitive (dielectric) loads*

For the purpose of dielectric testing, the modulator should be capable of delivering high-speed voltage pulses across an insulation sample. A test resistance R_t and capacitance C_t is added between the pulse transformer and the test sample as in Fig 4.9 (a). This is done for two reasons,

- Without R_t the C_l of the test sample would be added to the parasitic C_d of the transformer resulting in lower damping and higher rise-times. The modified overshoot and rise-time equations are as follows,

$$2R_{load} \cdot \sigma = \sqrt{\frac{L_\sigma}{C_d + C_l}} \quad , \quad T_r = 2\pi \cdot T_{10\%-90\%} \sqrt{L_\sigma (C_d + C_l)}$$

  The addition of R_t decouples the dynamics of the transformer and test sample. This allows fine-tuning of the output waveform for different sample capacitances since C_l varies on electrode arrangement. The combination of R_t-C_t acts as a filter with cutoff frequency,

$$F_c = \frac{1}{2\pi \cdot R_t \cdot C_t}$$

  Hence the waveform can be modified (overshoot can be reduced to zero) by tuning appropriate values of R_t-C_t for a given C_l.

- After dielectric breakdown occurs, the R_t plays an important role in limiting the steady-state short-circuit current flowing through the modulator. The current-rise is also slowed by the transformer inductance providing a time window for the protection circuit to act.

The challenge of this method, however, lies in solving the resultant third order circuit shown in Fig. 4.9 (a). The first step is to solve for the output voltage $U_o(s)$ in the Norton-equivalent as shown in Fig. 4.9 (b).

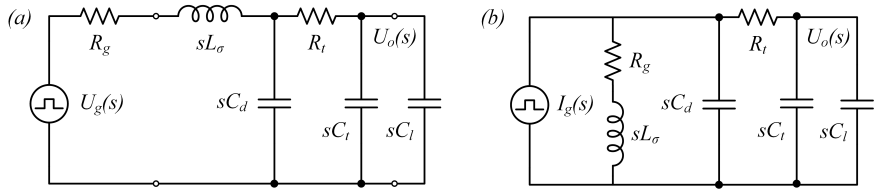


FIGURE 4.9: Equivalent circuit of pulse modulator with capacitive load

After simplifications (described in appendix δ), assuming $C_{eq} = C_t + C_l$ and $R_g \approx 0$ the output voltage $U_o(s)$ can then be expressed as,

$$U_o(s) = \frac{U_g}{sL_\sigma C_d R_t C_{eq}} \times \frac{1 + sR_t C_{eq}}{s^3 + s^2\left(\frac{1}{R_t C_{eq}} + \frac{1}{R_t C_d}\right) + s\left(\frac{1}{L_\sigma C_d}\right) + \left(\frac{1}{L_\sigma C_d R_t C_{eq}}\right)}$$

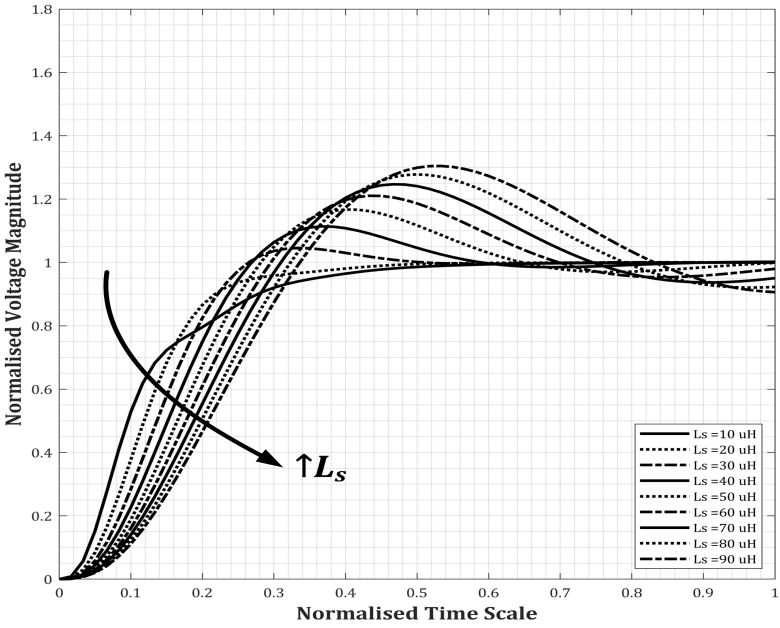
This can be written in the form $s^3 + s^2 R + sP + PQ$ by assigning,

$$P = \frac{1}{L_\sigma C_d} \quad , \quad Q = \frac{1}{R_t C_{eq}} \quad , \quad R = \frac{1}{R_t}\left(\frac{1}{C_{eq}} + \frac{1}{C_d}\right) = Q + \frac{1}{R_t C_d} \tag{4.8}$$

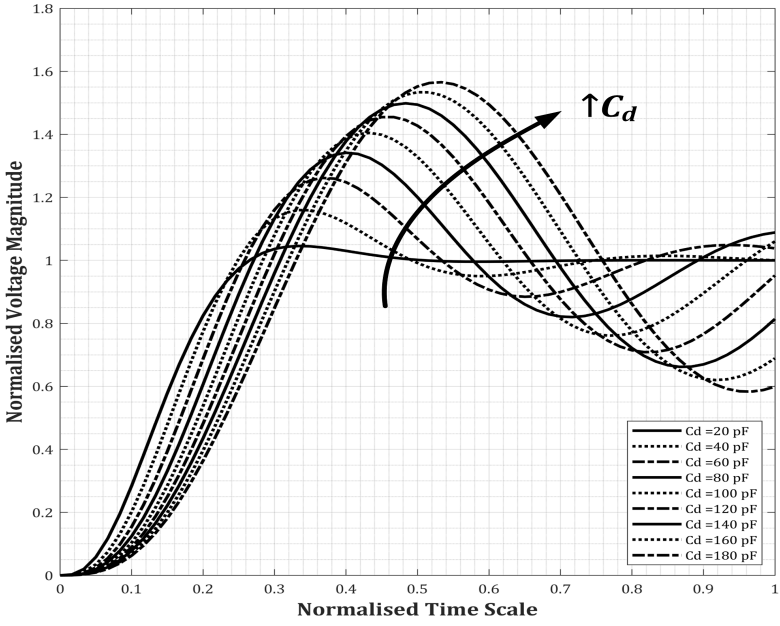
Where P is the parasitics parameter representing the dynamics of the transformer, Q is the quality or bandwidth parameter representing the dynamics of the $R_t C_{eq}$ filter, and R is the relational parameter symbolising the coupling between them. These parameters, henceforth referred to as the PQR parameters, are an intuitive and powerful method to characterise the pulse modulator. The equation is rewritten as the PQR equation as,

$$U_o(s) = \frac{U_g}{s} \times P \cdot (s + Q) \times \frac{1}{s^3 + s^2 R + sP + P \cdot Q} \tag{4.9}$$

Instead of solving for a general time-domain expression, the output voltage $u_o(t)$ can now be solved in MATLAB for varying values of L_σ, C_d, R_t, and C_l (explained in appendix ϵ). The effect of individual elements on the rising characteristics of the pulse waveform are shown in Fig. 4.10 and 4.11. It should be noted that the default values were taken to be $L_\sigma = 20\ \mu H$, $C_d = 20\ pF$, $R_t = 10\ k\Omega$ and $C_l = 50\ pF$ for generating these graphs. Achieving optimal rise-times and acceptable overshoots clearly requires the minimisation of transformer parasitics. Even unrealistically low values of L_σ and C_d produce atmost a critically damped response. On the other hand, an increase in R_t or C_l decreases the cutoff frequency F_c hence reducing the overshoot. This means that if either of the two were to be increased, the other must be proportionately reduced to maintain the same output. This is important when tuning the modulator for different electrode arrangements, since the value of C_l varies depending on electrode shape and number of insulation layers. However these graphs only show an incomplete design picture. In the next sub-section, the tradeoff between rise-times and overshoots is qualitatively analysed with respect to the previously defined PQR parameters to arrive at an optimal set of design criteria for the pulse modulator. These will set the grounds for the prototype.

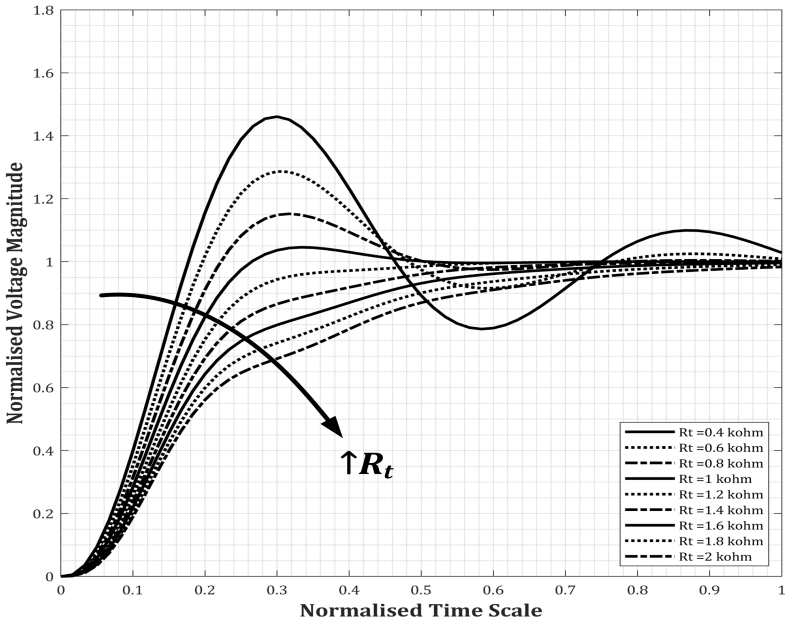


(a) Influence of transformer parasitic inductance L_σ

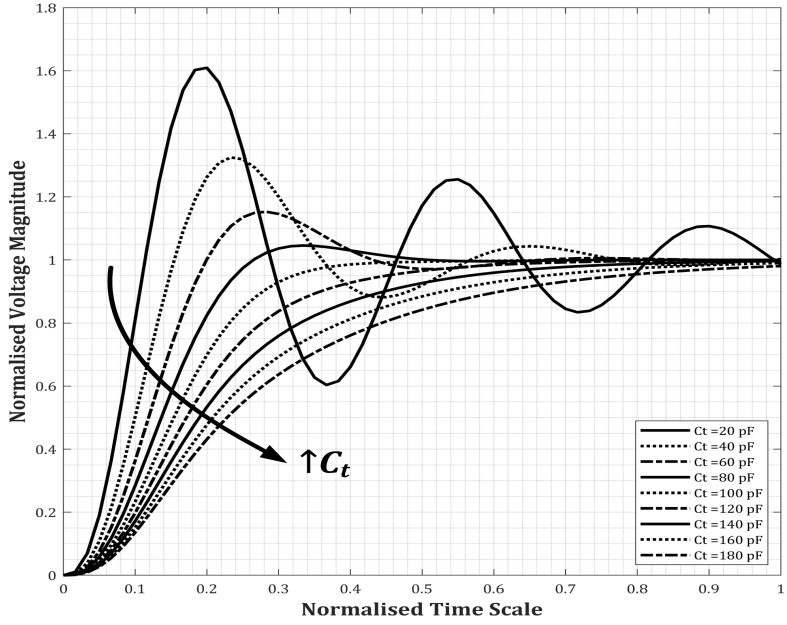


(b) Influence of transformer parasitic capacitance C_d

FIGURE 4.10: Influence of P-parameter elements on pulse rising characteristics



(a) Influence of filtering test resistance R_t



(b) Influence of capacitive test load C_l

FIGURE 4.11: Influence of Q-parameter elements on pulse rising characteristics

4.2.3 *Understanding the PQR equation*

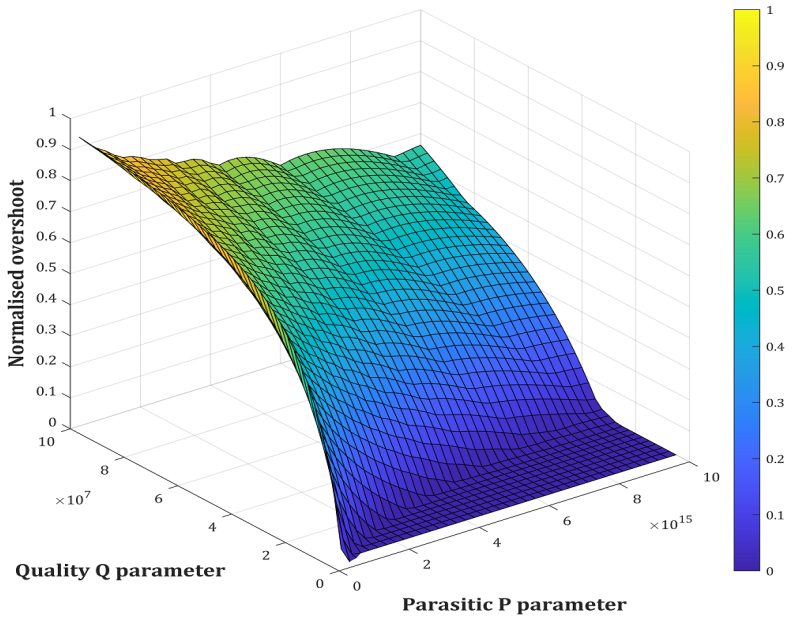
It should be noted that the content of this sub-section is **purely qualitative** in nature, and should only be considered a tool for visualising the inherent tradeoffs when designing a pulse modulator. D. Bortis *et al.* in [76] proposed that limiting the parasitic product $L_\sigma C_d$ (reciprocal of the P parameter) below 4.75×10^{-14} for a damping coefficient $\sigma = 0.75$ can ensure a rise-time below $T_r = 500\ ns$. However this is only applicable for purely resistive loads wherein any load capacitances are added to the parasitic capacitance C_d as stated previously. In the case of dielectric testing, a variation in C_l would require somehow altering the transformer parasitics which is, for obvious reasons, not practical. The addition of test elements R_t-C_t overcomes this challenge by providing flexibility to maintain the delivery of sharp output pulses. As explained in appendix ϵ, the normalised rise-time and overshoot were computed for 1600 combinations of P-Q-R in MATLAB. The observations are summarised as follows,

- As seen in Fig. 4.12 (a), the overshoot $\Delta\hat{V}_o$ increases for larger values of Q parameter and smaller values of P parameter. This means that minimum parasitics combined with larger output loads yield smaller overshoots.
- As seen in Fig. 4.12 (b), the rise-time $\Delta\hat{T}_r$ increases for smaller values of Q parameter and smaller values of P parameter. This means that minimum parasitics combined with smaller output loads yield faster rise-times.
- There is hence a clear trade-off between obtaining smaller overshoots and faster rise-times. However it is also clear that minimising transformer parasitics always improves the modulator performance, as expected.

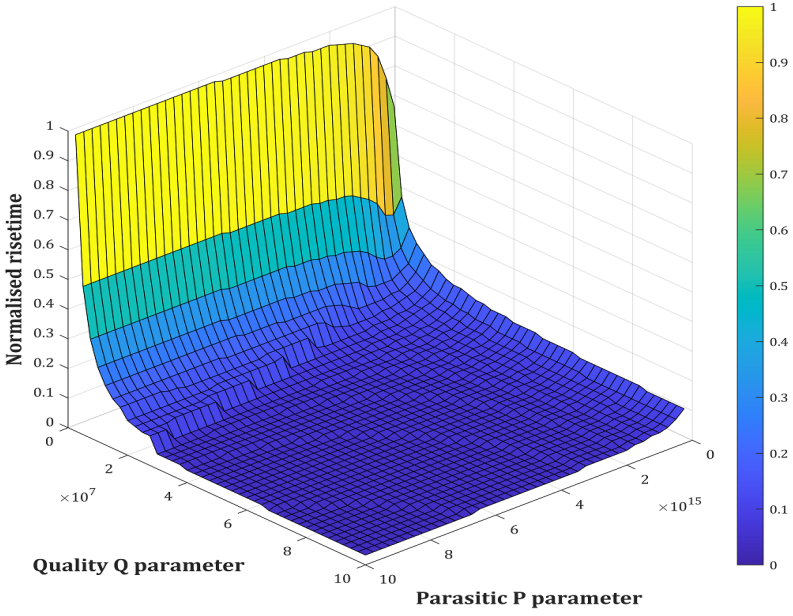
An optimal value of P and Q can be found for minimising both $\Delta\hat{V}_o$ and $\Delta\hat{T}_r$ by defining a **Pulse Modulator Performance Coefficient** Ψ_{pmc} as,

$$\Psi_{pmc} = 1 - [K_v \times \Delta\hat{V}_o + K_t \times \hat{T}_r] \tag{4.10}$$

When plotting Ψ_{pmc} with $K_v = K_t = 1$ as in Fig. 4.13a an optimal region is observed which, when viewed in 2D, is seen as a line traversing across the PQ design space where the Ψ_{pmc} is maximum. This "Ψ-line" as shown in Fig. 4.13b represents the optimal design region for the modulator for a given Ψ_{pmc}. If the requirement is $\Delta\hat{V}_o \approx 0$ such as for testing, the weights K_v and K_t can be redefined accordingly to obtain a new Ψ-line. The application of the PQR model is only proposed here, but requires more research which was not possible within the time-frame of this project.

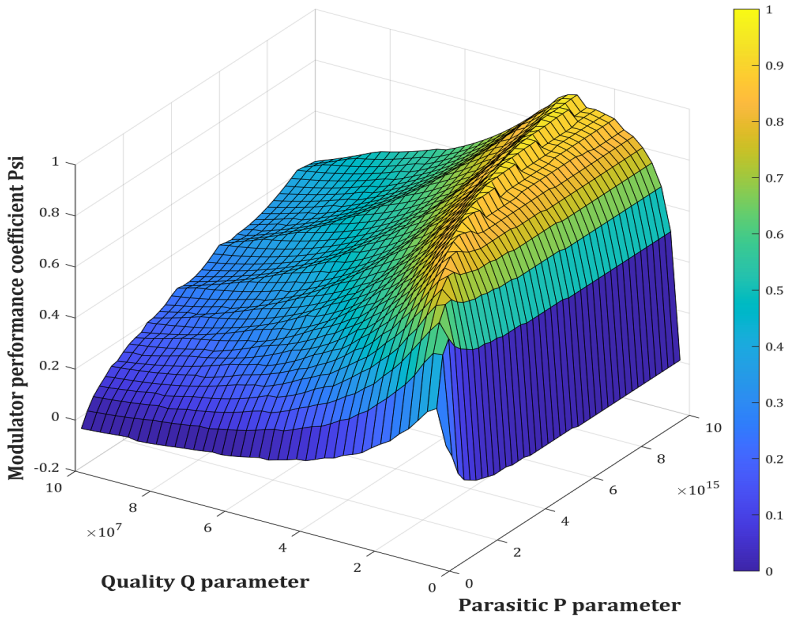


(a) Plot of output overshoot $\Delta\hat{V}_o$

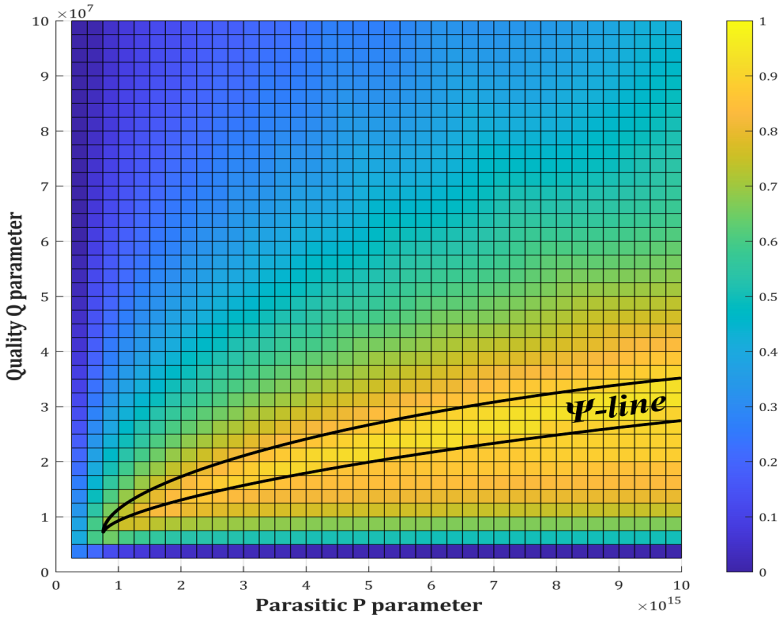


(b) Plot of output rise-time $\hat{T}_r$

FIGURE 4.12: Illustrating overshoots and rise-times across the PQ design space



(a) Plot of Ψ_{pmc} across the PQ design space

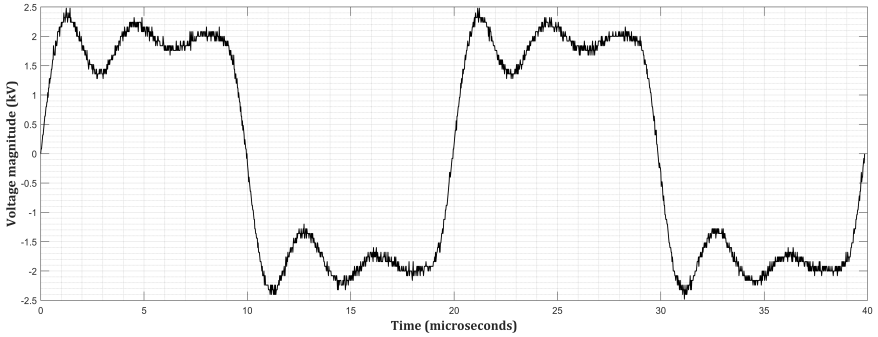


(b) 2D view showing the optimal Ψ-line

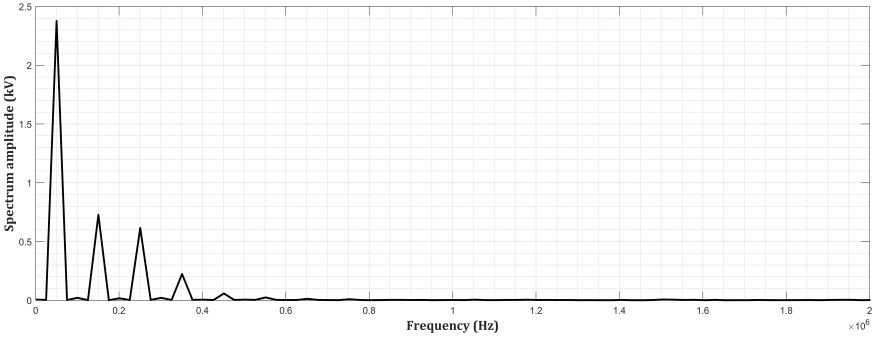
FIGURE 4.13: Determining optimal modulator design criteria using the Ψ-line

4.3 TRANSFORMER DESIGN

Unlike conventional high-frequency sine-wave transformers, pulse transformers transmit a wide frequency bandwidth (f_{lower} f_{upper}) varying from tens of kilohertz corresponding to the fundamental component to several megahertz corresponding to fast rise-times. A sample 2 kV 50 kHz pulse waveform with a $T_r \approx 2.5\mu s$ was produced from the modulator and analysed in the frequency domain as shown in Fig. 4.14. The results show that although the fundamental component dominates as expected, there still exists a significant magnitude of higher frequency content. The lower bandwidth limit f_{lower} is due to the non-infinite permeability of the magnetic core and its saturation flux density B_{sat}. The upper limit f_{upper} is defined by the parasitics L_σ-C_d of the transformer. This section elucidates the tradeoffs to be considered when designing the pulse transformer.



(a) Sample pulse waveform produced from modulator



(b) Frequency spectrum of sample pulse waveform

FIGURE 4.14: Fourier analysis of a typical pulse waveform

4.3.1 *Desired output specifications*

Before considering the design tradeoffs, it is important to set the desired specifications expected from the final modulator. The maximum input voltage from the AC mains is 230 V. An output voltage of 10 kV provides flexibility to test samples at different field strengths. This results in a required turns ratio of at least $n = 50$. The frequency or pulse rate can be varied from 10 to 50 kHz and the rise-time must be at most 20% of the pulse width. The lowest frequency should not result in saturation of the transformer core. The modulator should also be capable of having a minimal overshoot since sample breakdown is sensitive to peak voltage magnitude. Table 4.2 summarises the output specifications. Apart from these, there are other requirements that must be met. The modulator must be capable of producing sustained pulses for long periods of time without significant changes in the waveform. This is especially important during lifetime tests. For determining dielectric breakdown strength, a ramp of ≈ 1 kV/s should be applied across the sample. There should be a reliable method of controlling the voltage to perform this ramp increase. Further, the rise time and overshoot should be set by external parameters *viz.* R_t and C_t. This means that the same waveform should be applied across the dielectric regardless of the frequency, voltage magnitude, and sample capacitance thereby allowing accurate comparison of statistics. There should be no discharges or disturbances within the modulator that affect the quality of the output waveform. Finally, the modulator should disconnect within a short time frame after dielectric breakdown occurs. A faster response ensures lower electrode deformation and less frequent need for polishing.

SPECIFICATION	SYMBOL	MAGNITUDE
DC link voltage	V_{in}	230 V
Output voltage	V_o	10 kV
Turns ratio	n	1:50
Pulse rate	f_s	10-50 kHz
Pulse width	T_p	100-10 μs
Rise time	T_r	< 20% of T_p
Overshoot	ΔV	0-5%

TABLE 4.2: Desired pulse modulator specifications

4.3.2 *Parameters and tradeoffs*

The goal of transformer design is to broaden the bandwidth (f_{lower} f_{upper}) which limits its performance. Since almost every design improvement comes at the cost of something else, it is beneficial to define a set of parameters to characterise any given transformer design. These are illustrated in Fig 4.15 and listed in Table 4.3. The most influential tradeoffs include,

- Increasing d_{pc} comes at the cost of reducing d_{sp} which causes HV-LV failures. The core was grounded so that d_{pc} could be small (section 4.6.1).
- Increasing d_{sp} comes at the cost of reducing d'_{sc} which causes HV-core failures (section 4.6.2). This tradeoff was critical due to limited l_w.
- Increasing h_p reduces leakage flux but comes at the cost of reducing d''_{sp} which causes HV-LV failures (section 4.6.3). This could be solved by increasing d_{sp} but this is limited as mentioned above.
- Increasing N_s results in a longer h_s thereby reducing d''_{sc}. This tradeoff was critical due to limited h_w which is why d'_{sp} is set to 0 mm.
- Immersing in oil would eliminate flashovers but its $\epsilon_r \approx 2.4$ would increase C_d. A gas medium such as SF_6 is possible but tricky to extract.

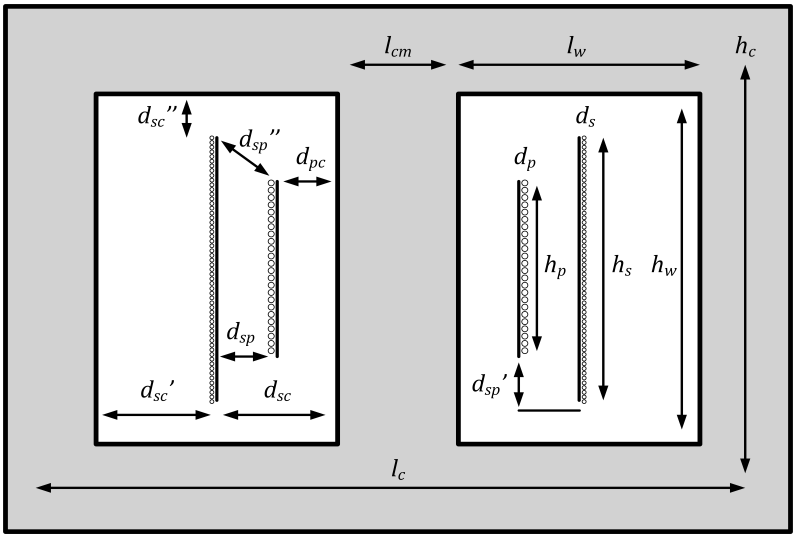


FIGURE 4.15: Geometrical parameters of the pulse transformer

	CORE PARAMETERS
h_c	Height of core (mm)
l_c	Length of core (mm)
l_{cm}	Length of core middle arm (mm)
h_w	Height of core window (mm)
l_w	Length of core window (mm)
A_e	Cross-sectional area (mm²)
	WINDING PARAMETERS
d_p	Diameter of primary winding (mm)
d_s	Diameter of secondary winding (mm)
h_p	Height of primary winding (mm)
h_s	Height of secondary winding (mm)
d_{pc}	Distance between primary winding and core (mm)
d_{sp}	Horizontal distance between secondary and primary (mm)
d'_{sp}	Vertical distance between lowest of primary and secondary (mm)
d''_{sp}	Shortest distance between primary and HV of secondary (mm)
d_{sc}	Horizontal distance between secondary and inner core (mm)
d'_{sc}	Horizontal distance between secondary and outer core (mm)
d''_{sc}	Vertical distance between secondary and upper core (mm)
	PERFORMANCE PARAMETERS
N_p	Number of primary turns
N_s	Number of secondary turns
n	Turns ratio
V_p	Voltage on primary winding (V)
V_p	Voltage on secondary winding (V)
N_c	Total number of cores
B_{sat}	Saturation flux density of magnetic core (mT)
L_σ	Leakage inductance referred to secondary (mH)
C_d	Distributed capacitance referred to secondary (pF)

TABLE 4.3: List of parameters in a typical pulse transformer

4.4 PARASITIC EVALUATION

The measurement of transformer parasitics is key in predicting its performance. The *PQR* equation shows that the minimisation of parasitics improves the output waveform. But as shown in the tradeoff analysis, there are limits to this minimisation. This section will discuss the measurement of leakage inductance and distributed capacitance, a comparison of various bobbin geometries, and a summary of the final bobbin arrangement.

4.4.1 *Measuring leakage inductance*

The concept of leakage stems from the imperfect magnetic coupling between the transformer windings. Although leakage is induced on purpose for some applications as an energy storage medium, it is an unwanted parasitic in pulse transformers. To measure the leakage inductance L_σ referred to the secondary, the RLC meter is connected across the secondary winding with the primary winding shorted. A Keysight U1733C is used for this purpose.

4.4.2 *Measuring distributed capacitance*

Determining C_d was done by first measuring time constant τ_{RC} as in Fig. 4.16. The C_d is then calculated with the resonance equation written as,

$$\omega_{RC} = \frac{2\pi}{\tau_{RC}} = \frac{1}{\sqrt{L_\sigma C_d}} \tag{4.11}$$

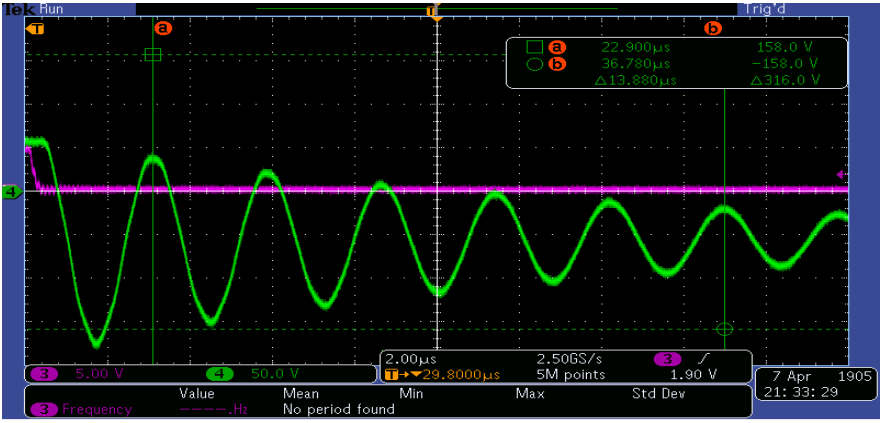


FIGURE 4.16: Measuring the resonant time constant τ_{RC} between L_σ-C_d

4.4.3 *Bobbin iterations and comparisons*

While the core is the carrier of magnetic flux, it is the primary winding that generates this flux within the core and the secondary winding that receives it to produce an output voltage. The windings consist of several turns of a conductive material (usually copper) wound on a bobbin of a certain shape and size. The geometry of the bobbin plays a decisive role in the resulting transformer parasitics. The bobbins for this project were designed in Autodesk Fusion 360 and exported as a .STL file. This is converted into G-code in Cura which is transferred to the Creality CR-10s Pro printer. The printed bobbins are wound in a Micafil machine and tested.

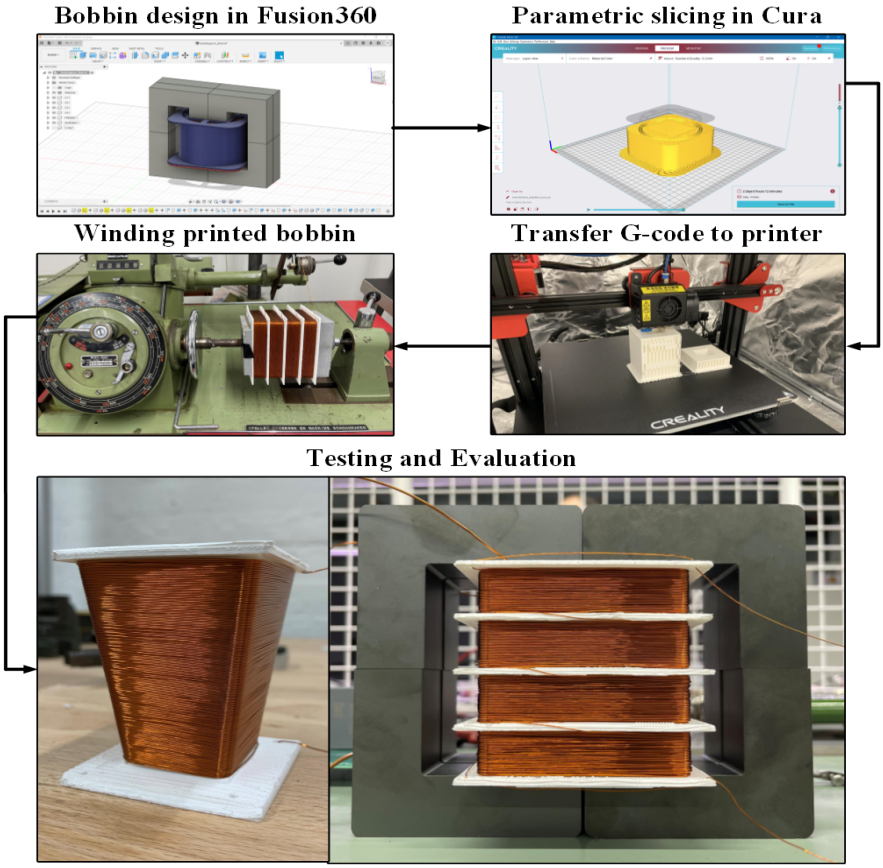


FIGURE 4.17: Bobbin construction workflow from design to winding

A total of 20 bobbins were designed and are shown in Fig. 4.18, each with their own unique learning outcome. The initial iterations were for a 2-core geometry and later for the 8-core geometry (explained in section 4.5). The effect of winding parameters on the leakage flux of the transformer is illustrated in Fig. 4.22. The observations are summarised as follows,

- It was observed that placing the primary and secondary bobbins as close to each other improves linking between them, as expected. A concentric winding design reduces the leakage by more than twice in all cases.
- Windings with 1:1 turns ratio have the least leakage in the order of microhenries. Higher turns ratio results in larger leakages in the range of millihenries because the secondary leakage dominates.
- A conical winding worsens the leakage unless the height of primary winding is close to that of the secondary *i.e.* $h_p \approx h_s$. From a high-voltage standpoint, bringing the LV closer to the top potential of HV increases chances of discharges.

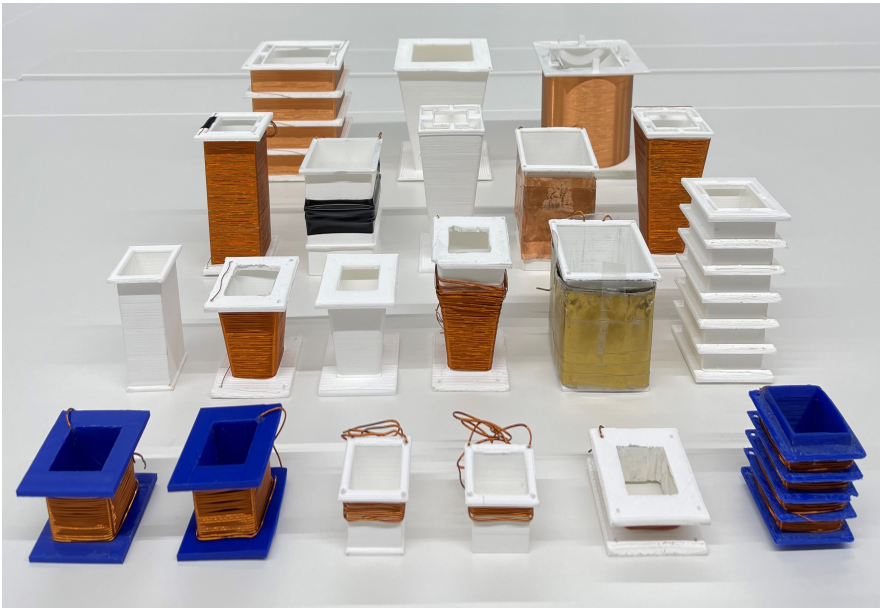
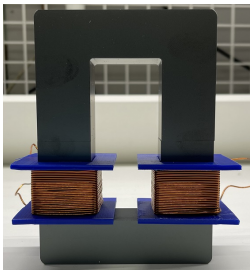
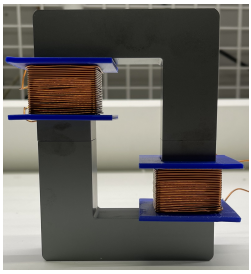


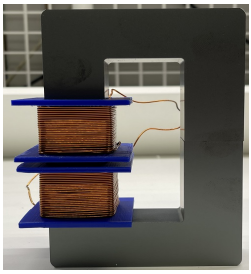
FIGURE 4.18: Design iterations printed in the lab for primary and secondary windings



(a) 25:25, $L_\sigma = 277\ \mu H$

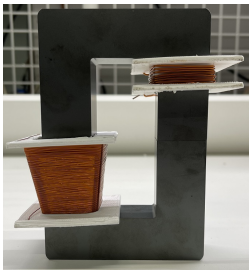


(b) 25:25, $L_\sigma = 330\ \mu H$



(c) 25:25, $L_\sigma = 137\ \mu H$

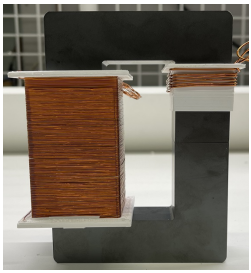
(a) 85:8, $L_\sigma = 3.9\ mH$



(b) 85:8, $L_\sigma = 4.6\ mH$

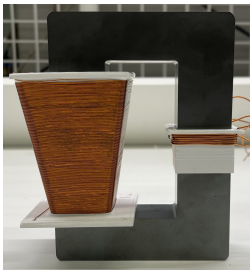
(c) 85:8, $L_\sigma = 1.9\ mH$

(a) 135:6, $L_\sigma = 11.5\ mH$



(b) 135:6, $L_\sigma = 12\ mH$

(c) 135:6, $L_\sigma = 5.1\ mH$



(a) 135:6, $L_\sigma = 13.5\ mH$

(b) 135:6, $L_\sigma = 14\ mH$

(c) 135:6, $L_\sigma = 6.9\ mH$

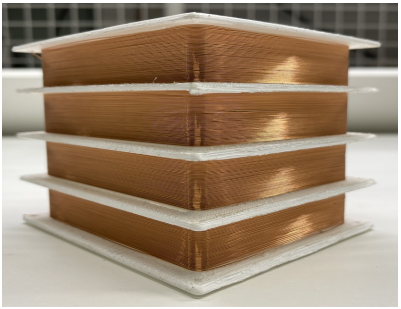
FIGURE 4.22: Effect of bobbin turns and geometry on leakage flux L_σ

The 8-core bobbin designs are shown in Fig. 4.23. The observations were,

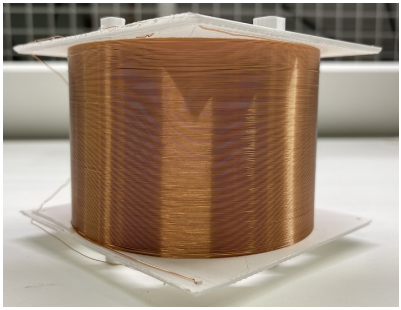
- The conical design in Fig. 4.23 (a) was avoided since it did not improve the performance, and made winding procedure difficult due to slipping.
- The foil winding in Fig. 4.23 (b) improves leakage when compared to wire winding from $L_\sigma = 24.8\ mH$ to $L_\sigma = 13.5\ mH$ for 1-turn and from $L_\sigma = 11.8\ mH$ to $L_\sigma = 5.36\ mH$ for 4-turns. A similar improvement can be achieved by spacing out the primary turns along the bobbin making $h_p \approx h_s$. However both methods reduce d''_{sp} increasing risk of flashover.
- The "fins" on the secondary bobbin in Fig. 4.23 (c) were made to accommodate multi-layer windings. However this design produced near-sinuous output due to significant increase in parasitic C_d between the turns.
- The cylindrical secondary bobbin in Fig. 4.23 (d) reduced the winding time from a few hours to a couple of minutes due to lack of any edges.

(a) 25:25, $L_\sigma = 277\ \mu H$

(b) 25:25, $L_\sigma = 330\ \mu H$



(c) 25:25, $L_\sigma = 137\ \mu H$



(d) 25:25, $L_\sigma = 137\ \mu H$

FIGURE 4.23: Effect of bobbin turns and geometry on leakage flux L_σ

4.4.4 *Winding design summary*

The final bobbin design iteration is illustrated in Fig. 4.24 and its design parameters listed in Table 4.4. The features are summarised here,

- The LV bobbin (blue) was made to enter the HV bobbin (red) from the bottom instead of the top to increase the distance d''_{sp}.
- The LV bobbin rests on the core *i.e.* $d'_{sp} = 0\ mm$. This is only possible since the core is grounded to reduce Core-LV failures (section 4.6).
- The height of the LV bobbin was made equal to the HV bobbin. However the LV winding height is only half of this *i.e.* $h_p = 0.5 \cdot h_s$ to prevent LV-HV failures. A silicone-insulated wire is used to avoid discharges.
- Slots were made on the faces of the bobbins to provide an exit point for LV winding, decrease print time, promote fluid flow of insulating medium (in case of SF_6 or CO_2). The gaps also allowed a visual check of any discharges occurring inside the windings.
- Ample distance was considered between HV-core and HV-LV. This was done to reduce failures such as flashovers and discharges.
- The design has a measured $L_\sigma = 7.3\ mH$ and $C_d = 25\ pF$.

It is clear than in addition to parasitic minimisation, a major part of bobbin design was to avoid failures. This will explained in detail in section 4.6.

PRIMARY	SECONDARY	CORE
N_p = 4	N_s = 200	h_c = 152 mm
d_p = 1 mm stranded	d_s = 0.35 mm solid	l_c = 186 mm
h_p = 35 mm	h_s = 70 mm	l_{cm} = 20 mm
d_{pc} = 2 mm	d_{sc} = 22.5 mm	h_w = 96 mm
d_{sp} = 10 mm	d'_{sc} = 9.5 mm	l_w = 33 mm
d'_{sp} = 0 mm	d''_{sc} = 20 mm	A_e = 3360 mm²
d''_{sp} = 45 mm		

TABLE 4.4: Overview of design parameters of final winding

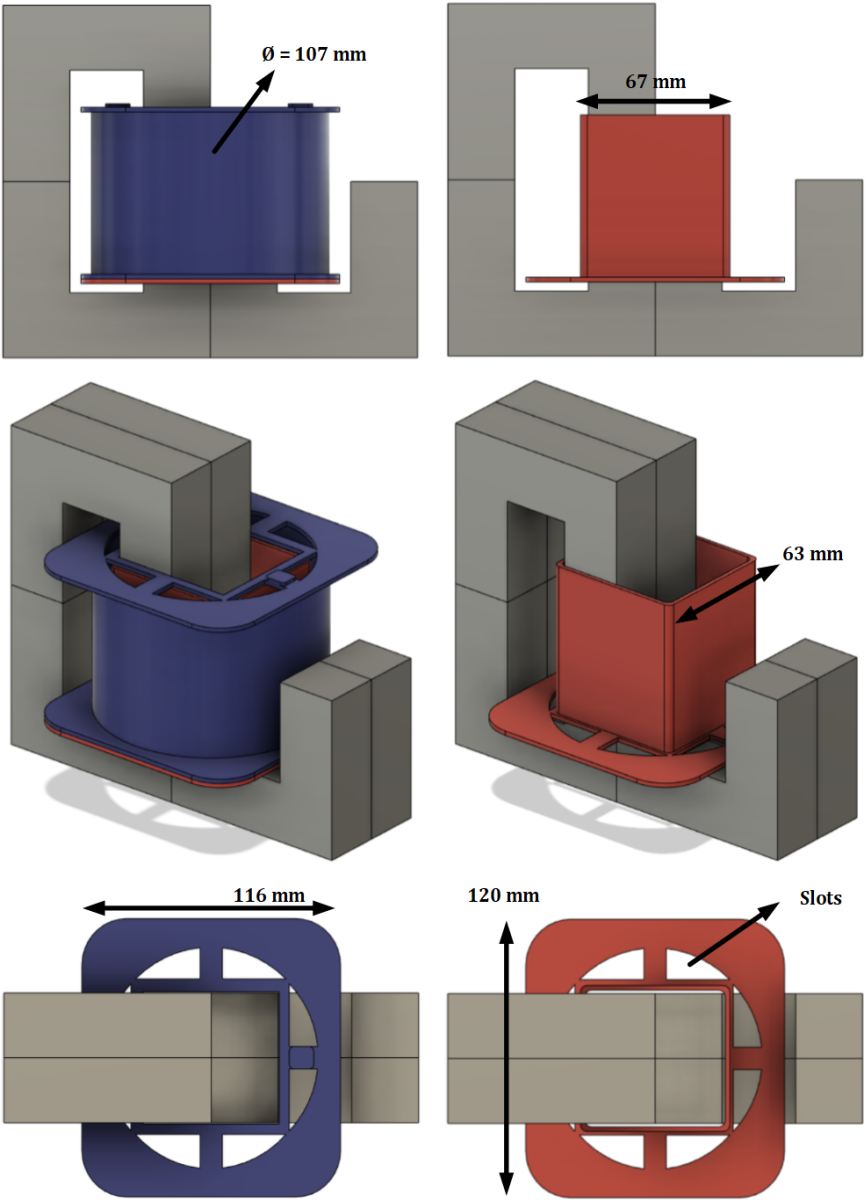


FIGURE 4.24: Final bobbin design overview (screenshots taken in Fusion 360)

4.5 MAGNETIC CORE

A transformer consists of two or more windings linked through a path of reluctance which, in most cases, is provided by the magnetic core. It tightly bundles the flux lines within itself and increases magnetic field density, thereby improving the linking between windings. Commonly used magnetic materials include soft ferrites such as manganese-zinc (MnZn) or nickel-zinc (NiZn) and iron-based alloys such as silicon steel (Si-steel). While the latter have higher saturation densities B_{sat} but also high core losses, soft ferrites have lower conductivities (resulting in lower losses) but also lower saturation limits. For the unipolar pulse transformer designed in [47] the author used an amorphous iron-based magnetic alloy manufactured by Metglas, USA with a $B_{sat} = 1.6\ T$. However such materials are expensive to procure and lossy at high frequencies. Due to availability and lower costs, an N87 (MnZn ferrite) U-core from TDK Electronics is used in this thesis. The next sub-sections discuss the material characteristics of the selected magnetic core and their effect on modulator operation.

4.5.1 *Material hysteresis characteristics*

Under bipolar excitation of the primary, the core experiences a bipolar magnetisation curve as shown in Fig. 4.25. The maximum flux density obtained after a duration t_{on} is denoted by B_{max}. The flux swing for equal duty cycles is then $\Delta B = +B_{max} - (-B_{max}) = 2B_{max}$.

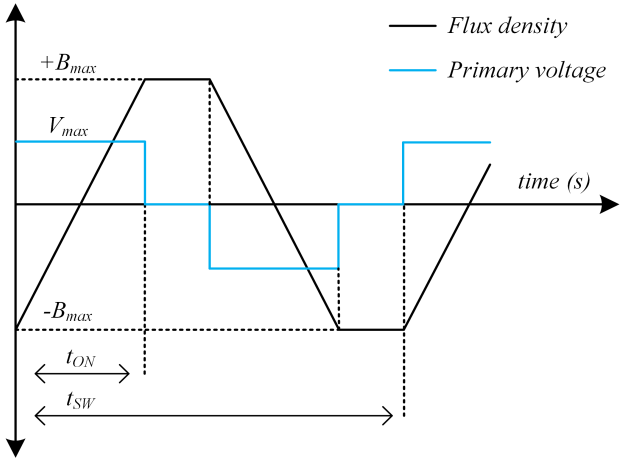


FIGURE 4.25: Magnetisation of magnetic core under bipolar excitation

In electrical circuits, a current I begins to flow when a voltage V is applied which in turn sets up an electric field. This current flow is directly proportional to the applied voltage as predicated by the Ohm's Law. Similarly in magnetic circuits, a flux density B begins to flow through the material when a magnetic field H is applied. However the B is non-linear in nature and is said to lag behind H. This means that when H is decreased back to zero, the B within the core does not follow the same return path. This phenomenon of the material characteristics depending on its "history" is termed hysteresis, and is visualised through the B-H curve shown in Fig. 4.26. Soft-ferrites are called so due the ease of starting or ending a B-flow within them. Hard-ferrites on the other hand require larger H and the B remains even after applying opposite H polarity (this fact is used in "memory" circuits such as computer hard-drives). Hence, soft-ferrites are used in power applications wherein only a small variation in H can greatly affect the flux flow thereby allowing for faster frequency operations [85].

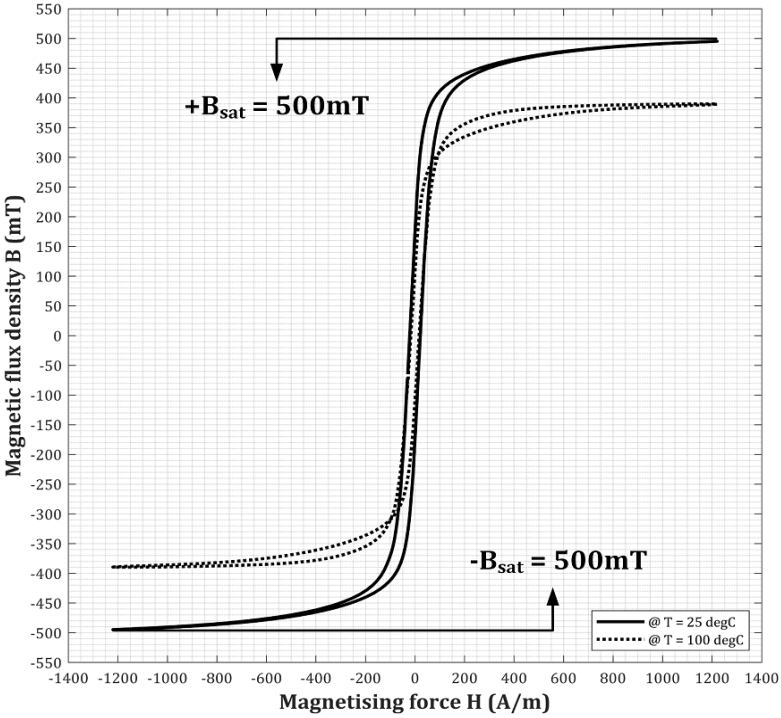


FIGURE 4.26: B-H characteristics of N87 material of TDK Electronics

4.5.2 *Saturation prevention criteria*

When an external magnetic field is applied across a soft-ferrite, some of the dipole moments within the material align themselves along the direction of the field. Strengthening the field aligns more of these moments but after a certain value of H, all available moments have been aligned and no further increase of B can be achieved. This is called saturation and corresponds to the flat region of the B-H curve, where the slope $\mu = \Delta B/\Delta H$ tends to near-zero. This μ (or permeability) indicates the extent to which a material can be magnetised. Operating near saturation leads to a dramatic drop in inductance resulting in high primary currents (which are limited only by the leakage inductance L_σ and winding resistance R_p). To prevent this, the flux density travelling in the core should not be allowed to approach near B_{sat} which for N87 is 500 mT. The flux swing ΔB is expressed in terms of the primary volt-per-turn V_{max}/n_1, the ON-duration t_{on}, and the core cross-sectional area A_e as,

$$\Delta B = 2B_{max} = \frac{V_{max} \cdot t_{on}}{n_1 \cdot A_e}$$

Saturation can thus be caused by a large volt-per-turn, a slow frequency, or a small cross-section. This leads to the following saturation criteria,

$$B_{sat} >> B_{max} = \frac{V_{max} \cdot t_{on}}{2 \cdot n_1 \cdot A_e} \tag{4.12}$$

From Fig. 4.26 it can be seen that N87 has a $B_{sat} \approx 500mT$ at room temperature. To prevent saturation, an operating flux density of $B_{max} = 400\ mT$ is selected. With $V_{max} = 230\ V$ (from AC mains) and $A_e = 840\ mm^2$ (from Fig. 4.27a) for a $t_{on} = 50\ \mu s$ (corresponding to $f = 10\ kHz$), the minimum primary turns to satisfy the saturation criteria can be calculated as,

$$n_1^{min} = \frac{230\ V \cdot 50 \times 10^{-}6\ s}{2 \cdot 400\ mT \cdot 840\ mm^2} = 17.2 \approx 18\ turns \tag{4.13}$$

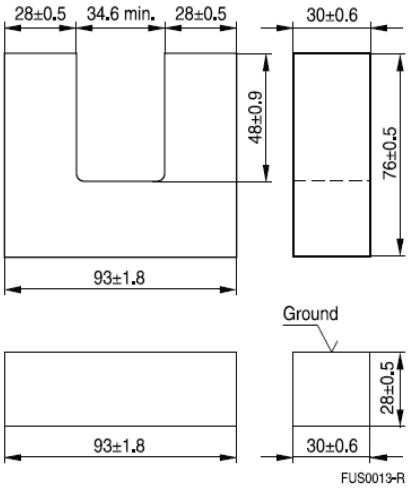
This indicates the first challenge of building a pulse modulator for dielectric testing. The B_{sat} poses a limit on the minimum number of turns on the primary, and higher turns increases leakage flux thereby deforming the output waveform. To reduce L_σ klystron modulators commonly have a single turn primary, but this is feasible since they only transmit pulses of short duration $\approx 5\mu s$ that too at 400-500 Hz such as in in [47]. In the case of dielectric testing however a continuous train of pulses is required which makes preventing saturation a more nuanced procedure.

U 93/76/30 cores
UI 93/104/30 cores **B67345**

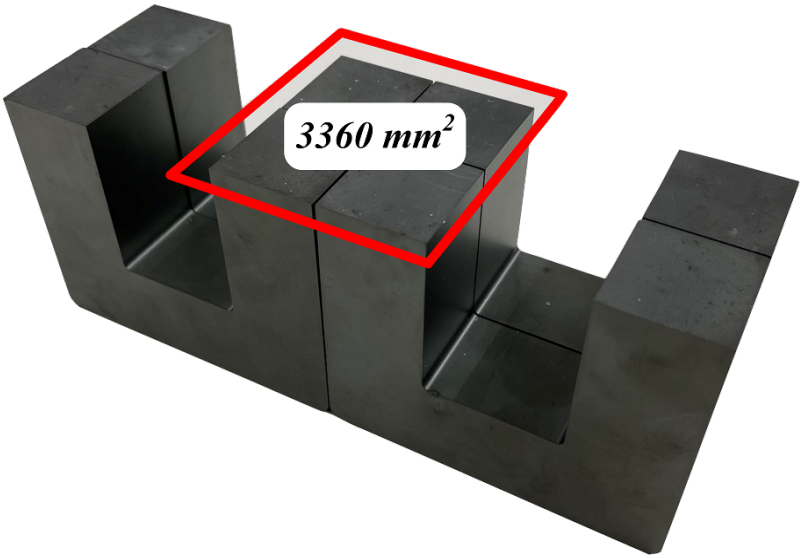
■ For power transformers >1 kW (20 kHz)

Magnetic characteristics (per set)

	UU 93/152/30	UI 93/104/30	
$\Sigma l/A$	0.42	0.31	mm^{-1}
l_e	354	258	mm
A_e	840	840	mm^2
A_{min}	840	840	mm^2
V_e	297000	217000	mm^3
m	1500	1100	g/set



(a) Magnetic core (U-93/104/30) geometrical parameters



(b) Lower half of the 8-core arrangement with $A_e = 4 \times 840 mm^2$

FIGURE 4.27: Magnetic core and geometry chosen for pulse transformer

To solve this, an 8-core geometry was selected as in Fig. 4.27b. By increasing the effective cross-sectional area of the core by a factor of four, the minimum required primary turns now decreases by a factor of 4 to become,

$$n_1^{min} = \frac{230\ V \cdot 50 \times 10^{-}6\ s}{2 \cdot 400\ mT \cdot 4 \times 840\ mm^2} = 4.3 \approx 5\ turns \tag{4.14}$$

The 8-core geometry also reduces the effective reluctance of the magnetic flux path, since there are now two parallel paths with higher core area seen by the flux. The magnetic linking is also improved since the bobbin is now contained within the core from both sides, as shown in Fig. 4.28.

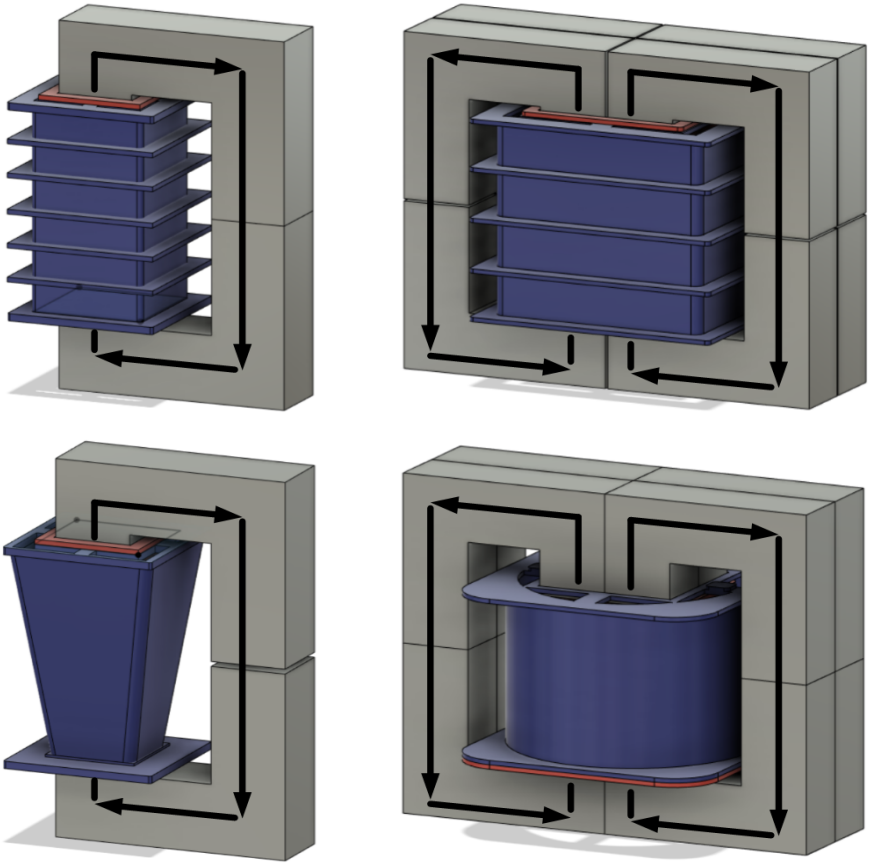


FIGURE 4.28: Comparison of 2-core (left) and 8-core (right) geometries.

4.5.3 *Complex permeability curves*

When compared to air, magnetic materials such as iron have a larger capacity to store magnetic energy. The permeability μ is a complex quantity which measures this storage capacity of a certain core material, and is expressed in terms of the permeability of free space μ_0 expressed as,

$$\mu = \mu_0(\mu' - j\mu'') = \mu_0\mu_r \tag{4.15}$$

The slope of the B-H curve is μ and varies non-linearly over H, but also over the operating frequency range as shown in Fig. 4.29. The frequency after which the real component μ' falls rapidly and the imaginary component μ'' reaches its peak is known as the cutoff frequency. When operated beyond this cutoff, the core material ceases to be magnetic (low μ') and dissipates most of the flux as loss (high μ''). Since the pulses contain frequency content up to a few megahertz, the $f_{cutoff} \approx 2\ MHz$ for N87 is hence suitable.

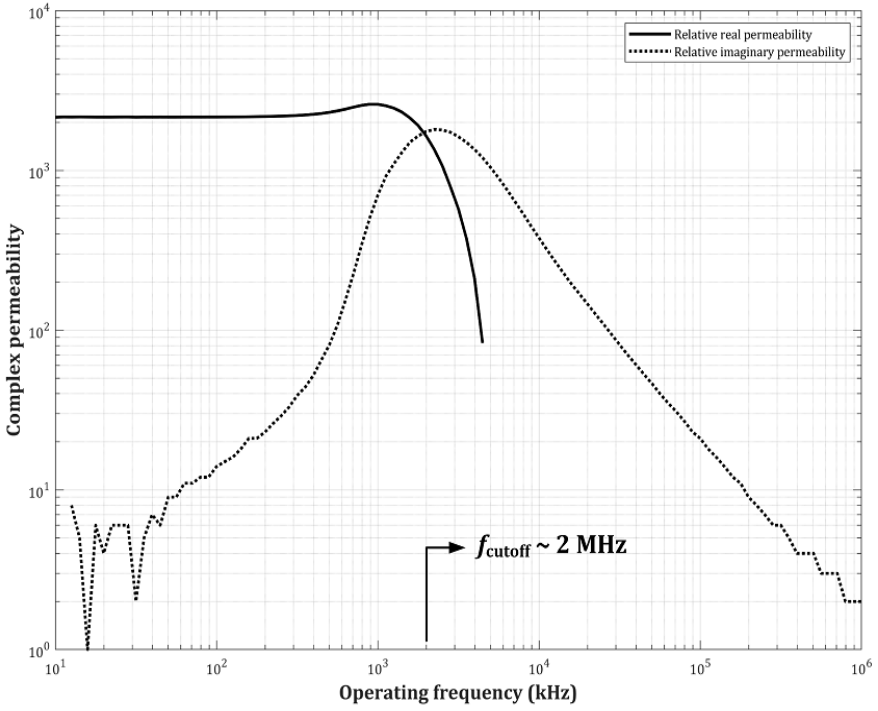


FIGURE 4.29: Plot of permeability μ against frequency for N87 material

4.5.4 *Evaluation of core losses*

Losses in a magnetic core are of two types *viz.* eddy current losses and hysteresis losses. When exposed to an alternating magnetic field, the core develops voltages within its volume due to Faraday's law which in turn sets up circulating eddy currents. These currents flow through the non-zero resistance of the core thereby generating loss. Since the selected core is a ferrite, it is possible to neglect the eddy current losses. Hysteresis losses stem from the fact that the B always lags behind the H (except during the initial magnetisation), and is equivalent to the area contained within the B-H loop [86]. The total core losses is thus written as the following sum,

$$P_{Fe} = P_e + P_h = K_e B_m^2 f^2 t^2 V_e + \eta B_{max}^{\eta} f V_e \tag{4.16}$$

The volumetric core loss graph was acquired from TDK as shown in Fig. 4.30. The losses at 50kHz with $B = 75\ mT$ is around $P_v \approx 40 kW/m^3$. Considering a core volume $V_e = 4 \times 297000\ mm^3$ the total core loss is,

$$P_{Fe} = P_v \times V_e = 40\ kW/m^3 \times 4 \times 297000 \cdot 10^{-9}\ m^3 \approx 50\ W \tag{4.17}$$

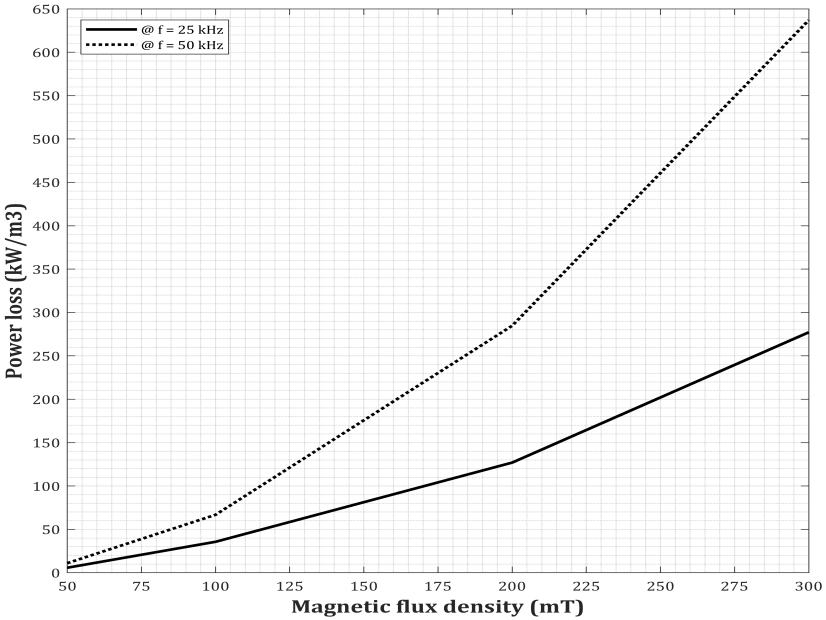


FIGURE 4.30: Volumetric loss graph for N87 material of TDK Electronics

4.6 FAILURE MODES AND SOLUTIONS

The generation of high voltages with high-power electronics in a compact frame is a certain recipe for a wide variety of failures. These failures lead to time delays due to repair as well as monetary losses in replacing components. It is therefore important to diagnose these faults, analyse their consequences, and trace them back to their causes. This section will discuss just that, along with the employed mitigation measures.

4.6.1 *Mode I: Core to LV discharges*

During operation, the secondary winding is energised to voltage levels of up to tens of kilovolts which can induce a potential onto the magnetic core of the transformer. Once this voltage exceeds a certain value the electric field from the core to the LV winding will exceed the breakdown strength of air. These discharges damage the primary bobbin as in Fig. 4.31 (a), and can cause flashovers at weak points such as in Fig. 4.31 (b). To understand the cause of these failures, the floating potential on the core was first measured and then validated through finite element analysis in COMSOL.

(a) Damage to primary bobbin caused due to repeated core-LV discharges

(b) Weak point for flashover at the exit of LV from the primary bobbin

FIGURE 4.31: Overview of causes and consequences of Core to LV failures

Since the core is an electrically floating object, the potential on it must be measured with an electrostatic voltmeter so as to not discharge it. An electrometer made by Leybold in Amsterdam as shown in Fig. 4.32 (a) was used for this purpose. A potential $\approx$ 500 V was measured on the core with a secondary output of 2000 V. This was validated in COMSOL Multiphysics illustrated in Fig. 4.33. There are two possible solutions to prevent failure,

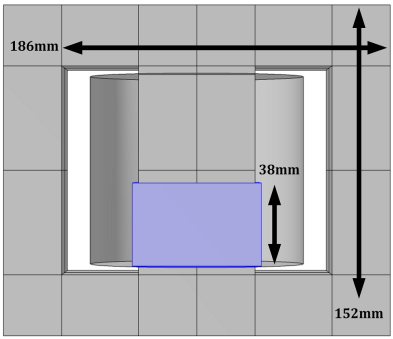
- Increase the isolation distance between LV winding and core. However this requires a larger HV diameter bringing it closer to the core on the other side. This solution would also increase leakage flux.
- Ground the core to earth. Doing so would require increasing the isolation distance between HV and core, but this is relatively easy to achieve.

Considering the limited window areas, the chosen solution was to ground the core by placing grounded metal clamps. This solved Mode I failures, but due to the considerable resistivity of the N87 material with $\rho_{core} = 10\Omega\ /m$ the grounding could not be made uniform which produced discharges between cores (Mode IV). This will be discussed in section 4.6.4.

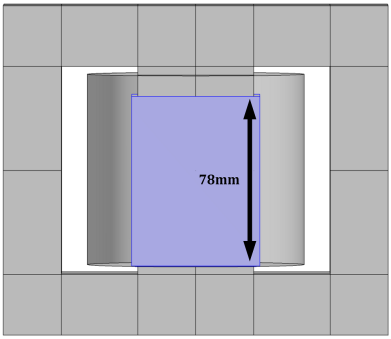
(a) Electrostatic voltmeter Leybold, Amsterdam

(b) Measured $V_{core} \approx 500V$ at $V_{HV} = 1000V$

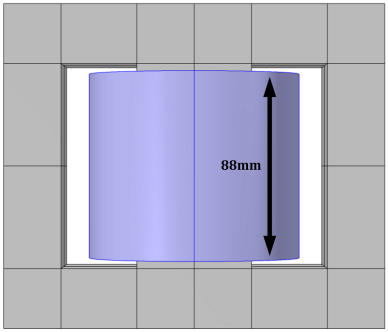
FIGURE 4.32: Measuring the floating potential of magnetic core.



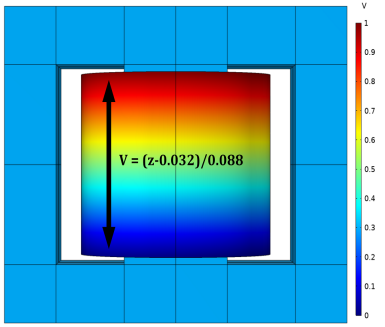
(a) Grounded LV of $h_p = 38mm$



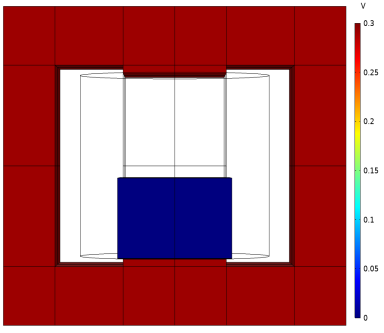
(b) Grounded LV of $h_p = 78mm$



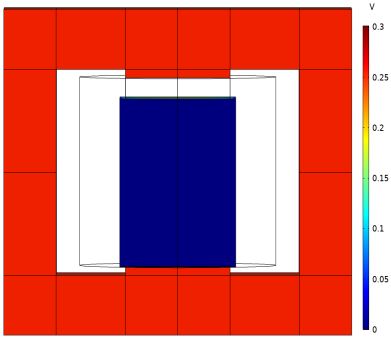
(c) HV winding of $h_s = 88mm$



(d) HV potential distribution



(e) $V_{core} = 0.24 \times V_{HV}$

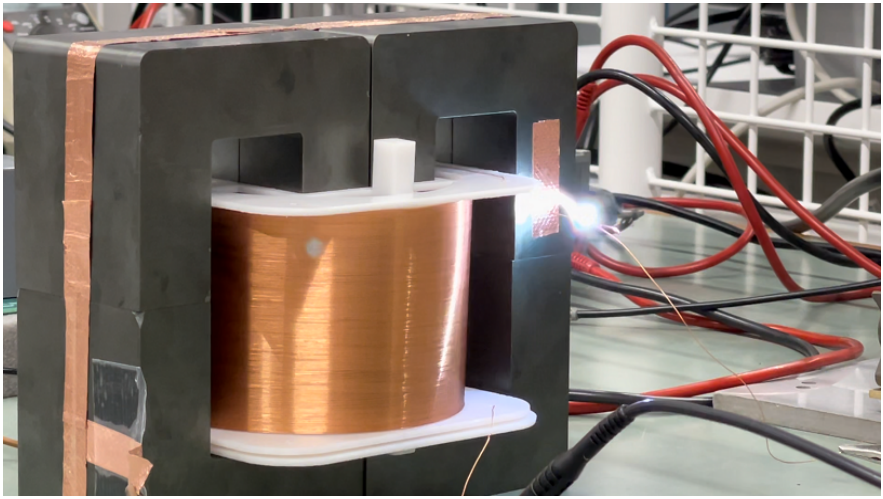


(f) $V_{core} = 0.29 \times V_{HV}$

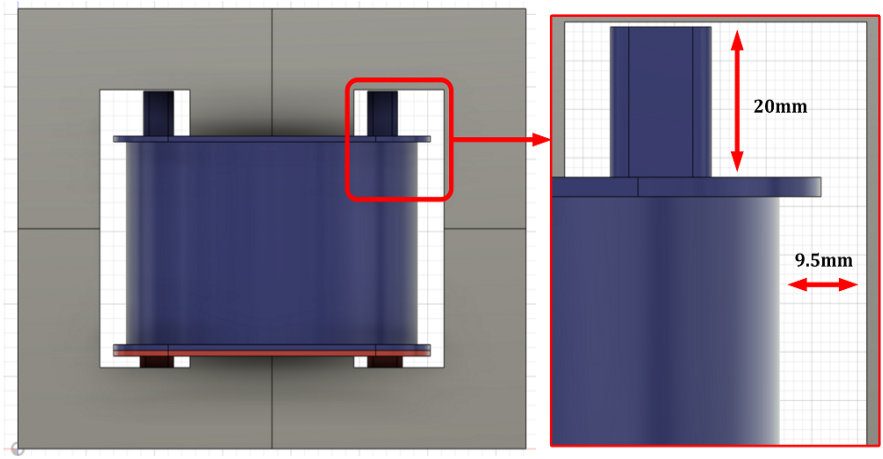
FIGURE 4.33: Determining floating potential of magnetic core with the electrostatics (*es*) physics in COMSOL Multiphysics. The transformer is placed inside air at 600 cm from the ground. The core can take a voltage of $\approx 0.3 \times V_{HV}$ which causes discharges from the core to LV winding. The V_{core} is observed to be lower when the LV is closer to the HV.

4.6.2 *Mode II: HV to core discharges*

With the transformer core now grounded, a significant field stress can be expected between the secondary winding and the core. This was estimated by forcing a HV-core flashover as seen in Fig. 4.34 (a). The solution was to ensure sufficient isolation distances in the bobbin as in Fig. 4.34 (b).



(a) Flashover by bringing secondary winding a few millimetres closer to core

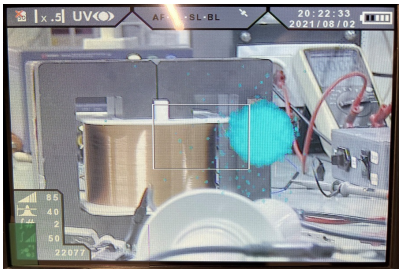


(b) Isolation distances at top (2cm considering corona ring) and sides (1cm)

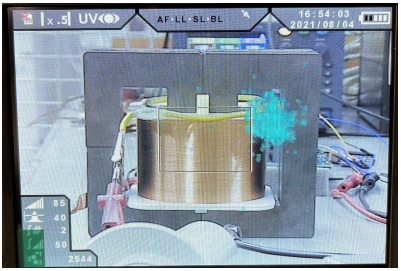
FIGURE 4.34: Forced HV to Core failure and subsequent bobbin redesign

Apart from flashovers, improper terminations of the HV or close proximity to another element can produce corona discharges. These were identified with the UViRCO CoroCAM in Fig. 4.35 (a). The discharges show up as blue blips on the screen of the CoroCAM as seen in Fig. 4.35 (b-d). A corona ring was made with a insulated wire, but this brought the HV potential closer to the inner side of the core window. An alternative termination with the HV wire inside a copper pipe was used as shown in Fig. 4.35 (f).

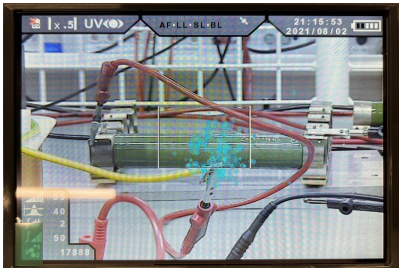
(a) UViRCO CoroCAM for detection



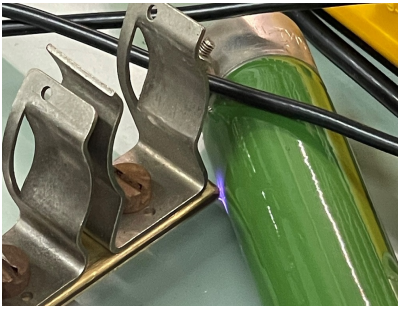
(b) Discharges between HV and core



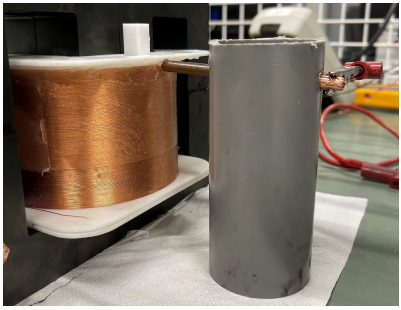
(c) Discharges between ring and core



(d) Corona at HV wire connection



(e) Corona between HV and object



(f) HV termination without ring

FIGURE 4.35: Overview of HV corona discharges and prevention strategies

4.6.3 *Mode III: HV to LV discharges*

Compared to other modes, the failures between HV and LV windings are the most severe, seen in Fig. 4.38. These failures occur in the form of,

- Corona discharges as shown in Fig. 4.37 (a). These are harmless to the bobbin, but produce distorted output waveforms seen on the oscilloscope. This is solved by using a silicone insulated wire as in Fig. 4.37 (b) and ensuring appropriate isolation distances as shown in Fig. 4.37 (c).
- Flashovers as shown in Fig. 4.38 (c). These are severe and cause damage to the bobbin and the winding insulation. Almost all such failures lead to Mode V failures *i.e.* breakdown of switches and gate drivers.

An alternative solution was explored which involved using a gas-insulated tank shown in Fig. 4.36. Testing this at 1 bar of Co_2 did not solve the issue, and higher pressures were avoided due to danger of glass explosion. Using 1 bar of SF_6 would be ideal but was not preferred because of extraction complications. Mineral oil is unsuitable since $\epsilon_r \neq 1 \Rightarrow \uparrow C_d$.

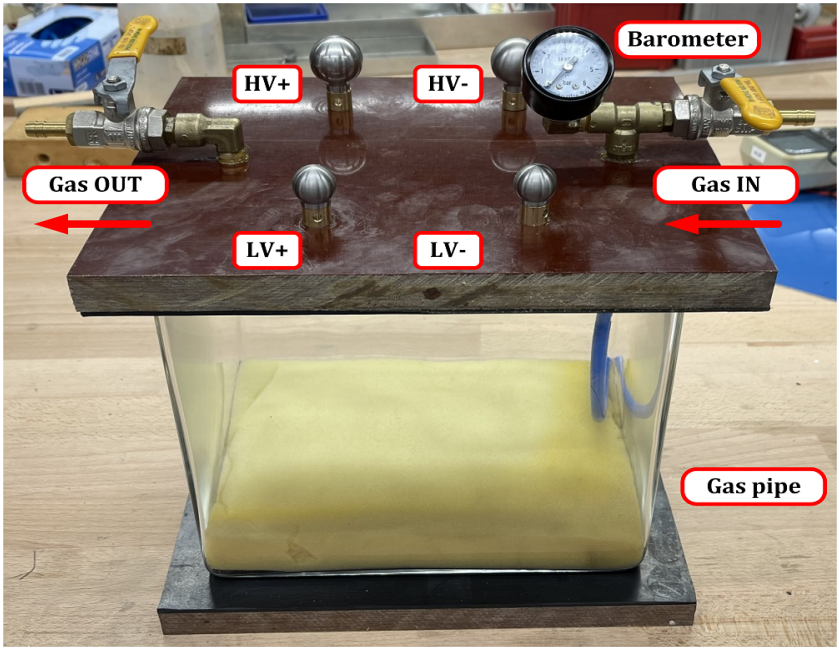
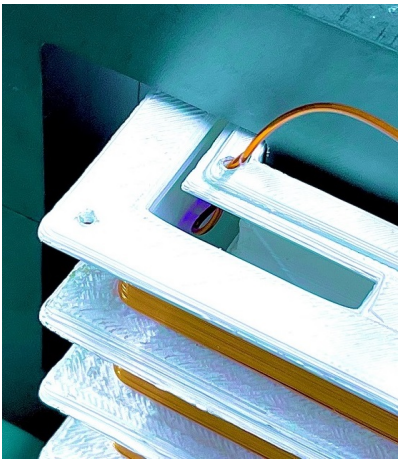
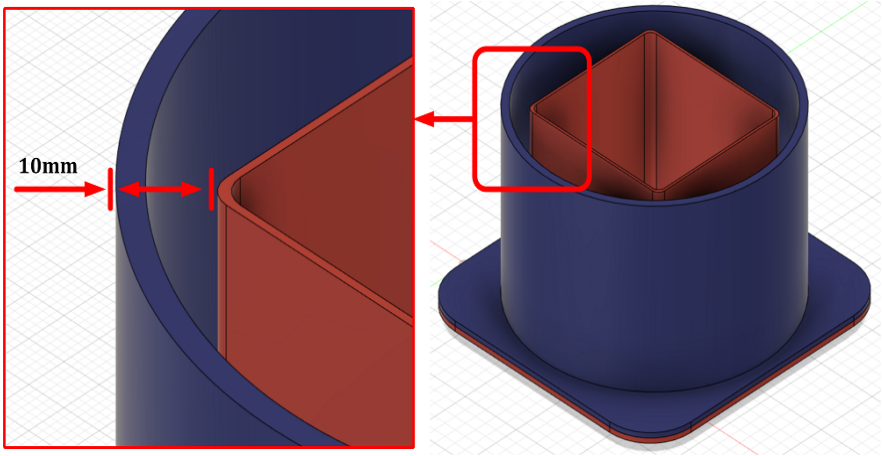


FIGURE 4.36: Transformer tank built for preventing Mode III failures



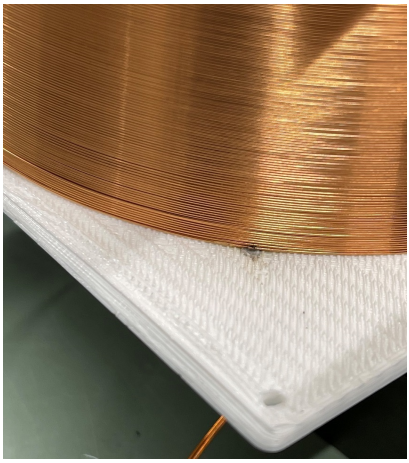
(a) Corona discharges observed between LV and HV. These were due to routing of the primary winding from the edge of the bobbin. The windings were then routed from the centre instead, which prevented occurence of corona.

(b) Primary winding made with 25 kV insulated wire. If the insulation is thicker the permittivity of the silicone would increase the C_d by a large factor. Spacing out the wire would improve leakage flux but also causes HV-LV flashovers.

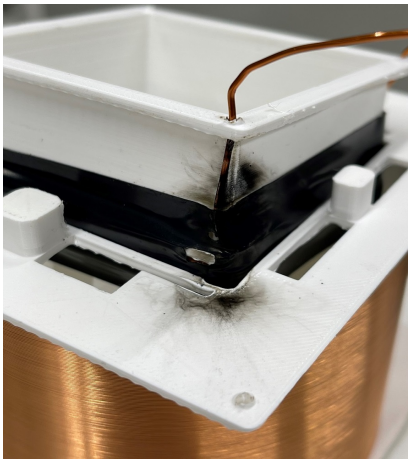


(c) Horizontal isolation distance between HV and LV bobbins. Increasing this distance would bring the secondary winding closer to the core and cause Mode II failures. Reducing it would bring the secondary closer to primary thereby causing Mode III failures. An optimal in-between had to be found of $\approx$ 1 cm.

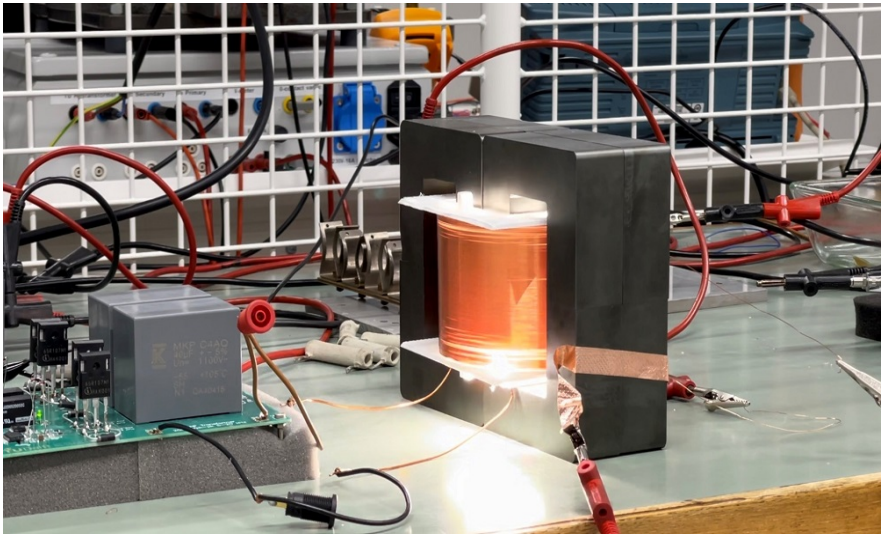
FIGURE 4.37: Solving the Mode III failures in the pulse transformer. The challenge was the small core window which complicates design optimisation.



(a) The origin point of the HV-LV flashover. The arc burnt a hole in HV bobbin and damaged the insulation of a winding section. A few turns had to be removed.



(b) The end point of the HV-LV flashover. The arc burnt the insulation tape as well as the insulation of the wire. The entire primary had to replaced with a new winding.

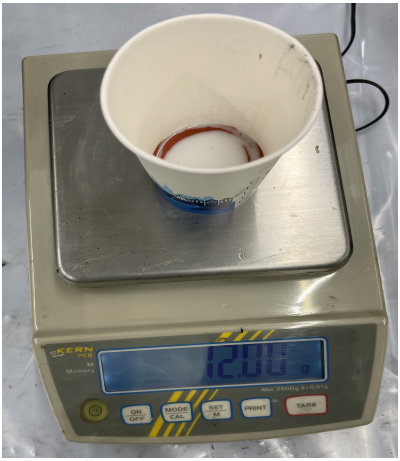


(c) Flashover from the the highest potential of the HV winding to the LV winding. To solve this, the primary was designed to be upside-down *i.e.* the LV potential would be placed at the level of the lowest potential of the HV winding.

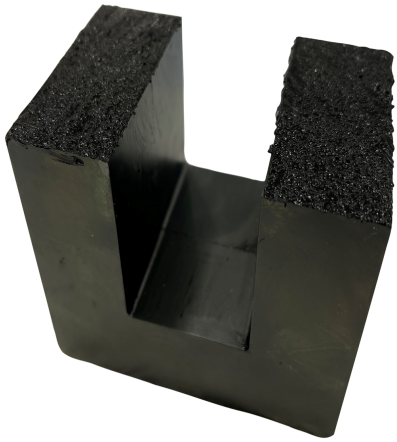
FIGURE 4.38: Severe flashover from HV to LV windings. The switches and gate drivers broke down with Mode V failure and had to be replaced.

4.6.4 *Mode IV: Core to core discharges*

Although grounding the magnetic core solved Mode I failures, improper grounding can lead to Mode IV failures. This occurs when some core sets are grounded and others are left floating, hence producing discharges in the gaps between them. This mode was the most difficult to diagnose since the discharges cannot be easily seen, and was only identified by removing each core piece one after the other. The discharges produce a distinct metal-striking sound and is very different from the "buzz" due to corona. These can happened between the top-bottom side faces, the former being louder than the latter. The solve this, the first step was to electrically connect the cores to each other with a carbon black with silicon rubber mixture. For this, a 1:1 (6g:6g) mixture of TFC Silicone Rubber Type 3 base and catalyst was made as seen in Fig. 4.39 (a). This was then combined with 0.6g (10%) of powdered carbon black to make the mixture conductive. The cores were then cleaned and grouped into sets of two. The prepared carbon paste was applied on the inside faces and the cores pressed to each other, after which the paste was applied to the top faces to produce the core set shown in Fig. 4.39 (b). The individual core sets were then assembled in the 8-core transformer arrangement. However applying excess paste decreased the primary inductance from $L_p = 193.4\ \mu H$ to $L_p = 62.78\ \mu H$. This decrease altered the time constant τ of the transformer resulting in a pulse droop.



(a) Mixing 6g base with 6g catalyst of TFC Silicon Rubber Type 3



(b) Electrically connected set of two magnetic U-cores

FIGURE 4.39: Conductively connecting the core pieces with carbon black mixture

After the excess carbon black was cleaned for a $L_p \approx 150.4\ \mu H$, the next step was to uniformly ground the now electrically connected core pieces. Two strips of copper foil were placed on the top and bottom of the transformer. A plexiglass frame consisting of two plates and M10 nylon threads was built to provide mechanical support and hold the foils in place with nylon bolts. A grounded metal clamp was attached across the thickness of the core piece to which the ground wire was connected. Copper tapes were used to connect the top and bottom foils with the clamp. Electrical connectivity of this surface was checked with a multimeter which showed good connection. The final setup is shown in Fig. 4.40. These modifications successfully prevented any core to core discharges. It should be noted that the two sets of 4-core on either side were not pasted together to allow easy disassembly in the future if needed. This produced very minor discharges which did not cause any fluctuations in the output waveform, and was hence ignored.

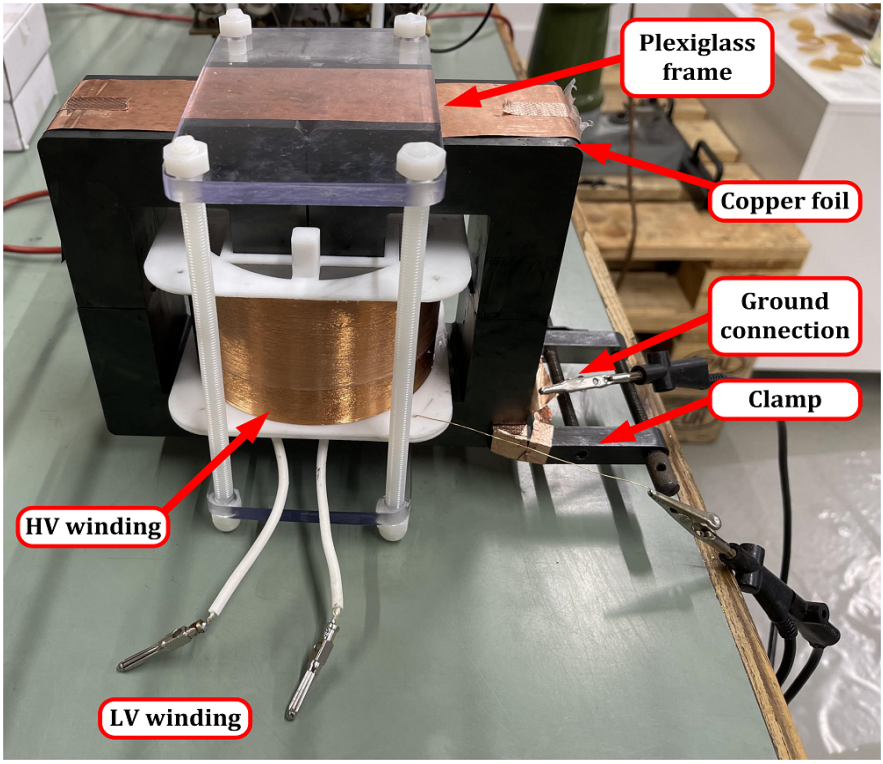


FIGURE 4.40: Setup for uniformly grounding the transformer core

4.6.5 *Mode V: Breakdown of FET/Driver*

Apart from the transformer, the semiconductor switches and gate drivers of the pulse generator are also prone to failures. These are mostly due to transient over-voltages that occur during Mode I-IV failures which then travel back to the PCB. The observed failures as shown in Fig. 4.41 include,

- A failure between the Gate and Source legs of the MOSFET. This can be diagnosed by checking if $R_{GS} = 0\ \Omega$ across these pins.
- A failure between the V_{GS} and V_{SS} pins of gate driver. This can be diagnosed by checking if $R_{GS} = 0\ \Omega$.
- A partial failure can also occur which shows as $R_{GS} = 0.8\ M\Omega$ instead of the healthy condition where $R_{GS} = 1.9\ M\Omega$.

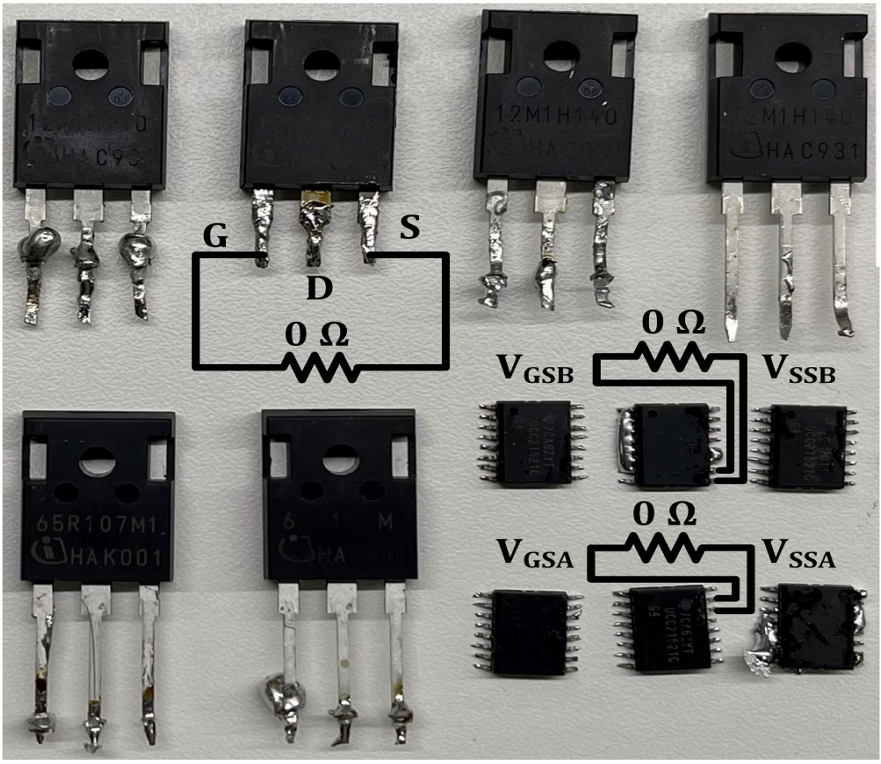
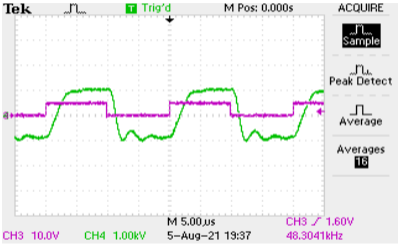


FIGURE 4.41: Observed failures in MOSFETs and gate drivers

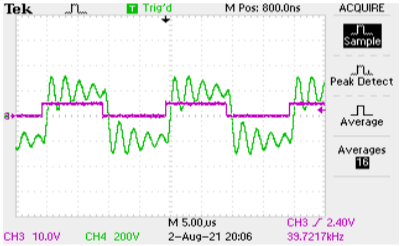
Replacing each PCB component after a failure has occurred is both cumbersome and time-consuming. A few patterns were noted through experience which simplify the diagnosis and repair process. Attempting to operate the modulator after a failure can have the following outcomes,

- If one of the gate drivers has completely failed, a "drooped" waveform will be produced as shown in Fig. 4.42 (a). The droop can either be on the rise or fall of the waveform. The drivers must then be removed and their resistances checked for possible short-circuits.
- If one of the gate drivers has partially failed, a "wavy" waveform will be produced as shown in Fig. 4.42 (b). The output voltage will not increase after a certain value (usually 300 V). This failure is less common.
- If a switch has failed, then no output waveform will be produced. Each G-S pin must be tested with a multimeter to identify the failed switch. This resistance value for a healthy MOSFET is around 1 MΩ.
- If a combination of both a switch and a driver has failed, a ringing sound is generated (could also be due to 10 kHz signals). Checking which driver heats up when the V_{CC} is connected will reveal which one is faulty. Then the G-S pins of must be checked to identify the failed switch.

It is clear that the above failures are caused due to breakdown of gate-to-source junctions at the MOSFET and gate driver. Since these junctions are usually rated for $\approx$ 30 V as given in their datasheets, it is highly probable for a transient overvoltage travelling from the transformer to cause their breakdown. It is hence important to employ mechanisms to prevent them.



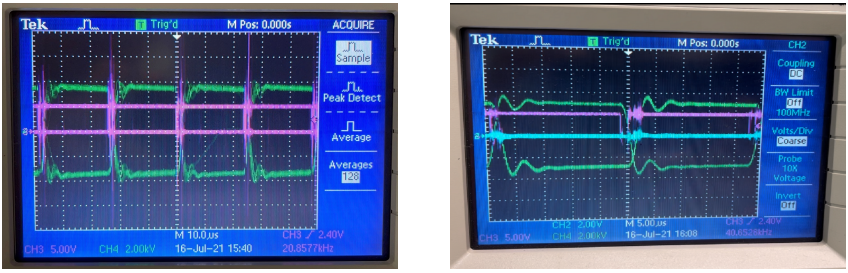
(a) "Drooped" waveform with a complete driver failure
V_{GS} : $Y = 10V/div$ $X = 5\mu s/div$
V_{out} : $Y = 1kV/div$ $X = 5\mu s/div$



(b) "Wavy" waveform with a partial driver failure
V_{GS} : $Y = 10V/div$ $X = 5\mu s/div$
V_{out} : $Y = 1kV/div$ $X = 5\mu s/div$

FIGURE 4.42: Effects of various failures on V_{GS} (magenta) and V_{out} (green)

A forced discharge was induced to produce the waveforms shown in Fig. 4.43. It should be noted that flashovers cause far more severe consequences. These transients can travel to the pulse generator in two possible ways *viz.* through the wires and through electromagnetic interference as seen in Fig. 4.43. Zener diodes were connected across the MOSFETs and at the output pins of the gate driver directly as shown in Fig. 4.44. Also, the pulse generator was placed in a metallic box to prevent interferences.



(a) Fluctuations observed on the signals from the Arduino (magenta)

(b) Fluctuations observed on a magnetic antenna near the modulator

FIGURE 4.43: Transient fluctuations during induced discharges

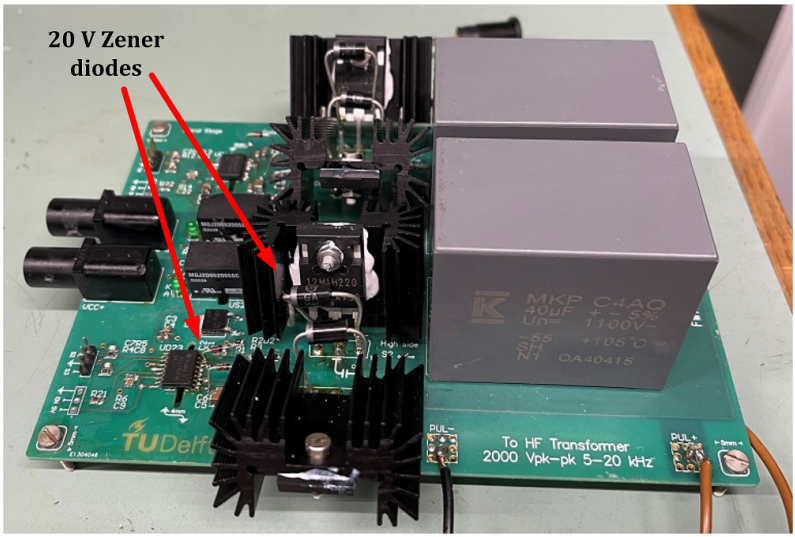
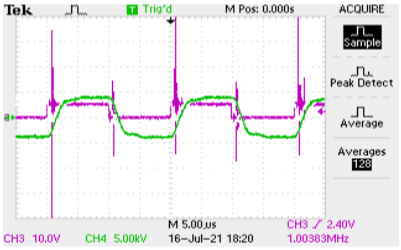
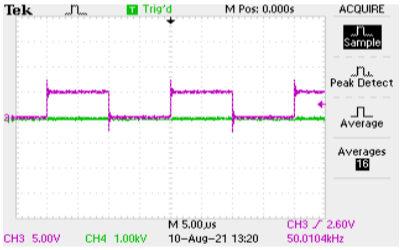


FIGURE 4.44: Zener diodes connected across MOSFETs and gate drivers

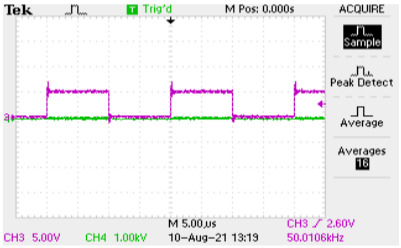
Although the addition of zener diodes improved the failure frequency and number of failures, they could not be completely prevented. A set of snap-on ferrites were used on the wires connecting the primary winding with the pulse generator, however these slow down the pulse waveform. A possible improvement is to use TVS diodes instead of zeners since they offer faster clamping in the range of hundred nanoseconds. But due to lack of their availability this option could not be explored fully. To demonstrate the superior capabilities of TVS over zener diodes, the transient over the Arduino pulses shown in Fig. 4.45 (b) were clamped with zener diodes in Fig. 4.45 (c) and TVS diodes in Fig. 4.45 (d). The overshoots are caused when connecting the pulses to the oscilloscope with a long coaxial cable. The zener clamps only the negative overshoot due to diode characteristics, but is unable to clamp the positive overshoot. The TVS diode can effectively remove overshoots without slowing down the signal. Hence, it is expected that TVS diodes across the switch/drivers will eliminate possible failures.



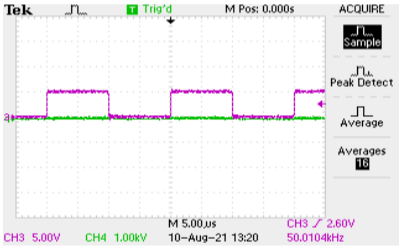
(a) Typical operational overshoots
V_{GS} : $Y = 10V/div$ $X = 5\mu s/div$
V_{out} : $Y = 5kV/div$ $X = 5\mu s/div$



(b) Overshoots due to long coaxial cable connected to Arduino
V_{GS} : $Y = 5V/div$ $X = 5\mu s/div$



(c) Negative overshoots are clamped with only zener connected
V_{GS} : $Y = 5V/div$ $X = 5\mu s/div$



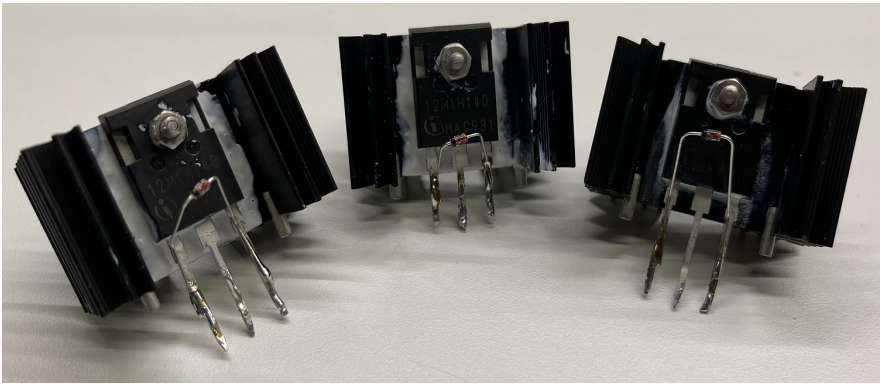
(d) Negative and positive overshoots are clamped with TVS diode
V_{GS} : $Y = 5V/div$ $X = 5\mu s/div$

FIGURE 4.45: Improvement in clamping capability with TVS over Zener diode

The failure risk is increased at high switch temperatures which is common during operation. For this reason, the switches are passively cooled with heat sinks of $R_{th} = 2.7\ °C/W$ with thermal paste of $K_{th} = 0.65\ W/mK$ and actively cooled with a 138 CFM fan, as shown in Fig. 4.46.

(a) Without any cooling techniques
Observed $T_{FET}^{max} = 133\ °C$

(b) With heatsink and 138 CFM fan
Observed $T_{FET}^{max} = 26\ °C$



(c) Heat sink and paste to MOSFET with a G-S zener clamp

FIGURE 4.46: Temperatures of the SiCFETs under continuous operation

4.7 MODULATOR SUBCIRCUITS

4.7.1 *Rectified DC power supply*

The power supply holds the DC link voltage, provides current to magnetise the primary winding, to satisfy the magnetic and copper losses in the transformer, and finally to the load on the secondary. This requirement is,

$$I_{in} = I_{mag} + I_{Fe} + I_{Cu} + I'_{load} \tag{4.18}$$

To compute I_{mag} the voltage across the primary $v_p(t)$ is taken as the sum of voltages across the primary inductance $L_p = L_\sigma + L_m$ and the winding resistance R_p with a current flow of $i(t)$. This in the form,

$$v_p(t) = L_p \cdot \frac{d}{dt} i(t) + R_p \cdot i(t)$$

Taking $R_p \approx 0$ the magnetising current is written in terms of the primary voltage V_p and the fundamental frequency f_1 as,

$$I_{mag} = \frac{V_p}{2\pi \cdot f_1 \cdot L_p} \tag{4.19}$$

The inductance L_p is proportional to the square of primary turns N_p. As observed before, this causes higher current draw when reducing winding turns. To compute the load current I'_{load} the secondary output is first considered to be a trapezoidal waveform of as shown in Fig. 4.47.

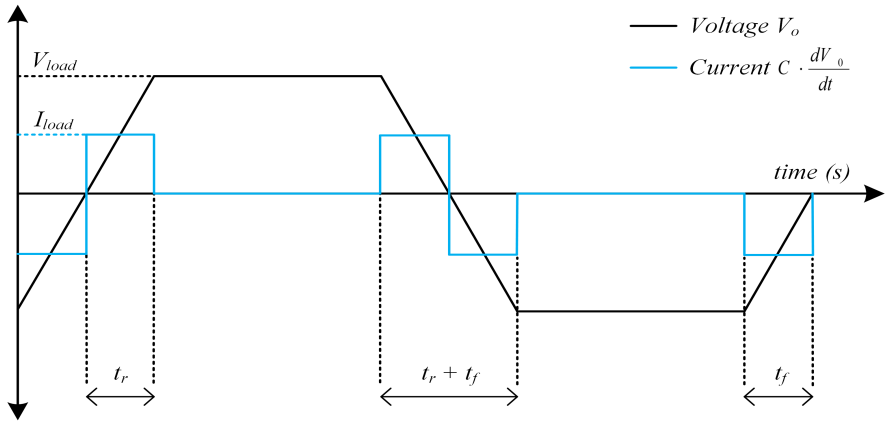


FIGURE 4.47: Trapezoidal voltage and step current waveforms of pulse modulator

The capacitive load draws current only during the voltage transitions, to charge the C_l to a new steady-state value. The peak value of this current is the load capacitance times the differential of the voltage and is written as,

$$I_{load}^{peak} = C_l \cdot \frac{dV_o}{dt}$$

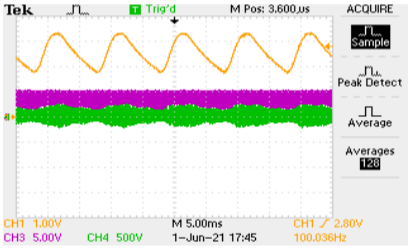
This is then averaged over the entire pulse duration T as,

$$I_{load}^{avg} = \frac{4 \cdot t_r}{T} \times I_{load}$$

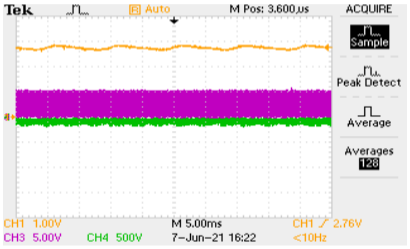
And finally referred to the primary across a turns ratio n as,

$$I'_{load} = \frac{I_{load}^{avg}}{n} \tag{4.20}$$

The magnetic core loss current depends on the chosen core material and cross-sectional area, while the copper loss current depends on the winding wire diameter and length. Through modulator testing, the required primary current is found to be in the range of **10 A**. Although there exists commercially available DC sources such as the Delta Elektronika SM 1500-CP-30 (link) capable of supplying 1500 V and 30 A, these are quite expensive to procure. Hence a variable autotransformer is connected to a KBPC5010 1 kV 50 A bridge rectifier for powering the modulator. Since the rectifier is line commutated unlike in commercial sources that utilise high-frequency converters, the smoothing capacitor must be carefully selected to prevent output ripple as shown in Fig. 4.48 (a). Two parallel 400 V 680uF electrolytic capacitors were used for this purpose and the result shown in Fig. 4.48 (b).



(a) Analysis with a $68\mu F$ capacitor
$V_{GS}: \ Y = 5V/div \ X = 5ms/div$
$V_{in}: \ Y = 1V/div \ X = 5ms/div$
$V_o: \ Y = 500V/div \ X = 5ms/div$



(b) Analysis with a $1360\mu F$ capacitor
$V_{GS}: \ Y = 5V/div \ X = 5ms/div$
$V_{in}: \ Y = 1V/div \ X = 5ms/div$
$V_o: \ Y = 500V/div \ X = 5ms/div$

FIGURE 4.48: Rectified DC (yellow) and load voltage (green) after smoothing

After choosing an appropriate smoothing capacitance, the discharge (DCH) circuit is then designed accordingly. The resistance must satisfy two criteria. The first is that the the time constant τ_{dch} of the circuit should be fast enough to discharge the capacitance within a time T_{set}. The second is that the power dissipation within each resistor R_{set} should not exceed its power rating P_{set} at maximum DC voltage $V_{dc,max}$. These criteria are written as,

$$R_{set} > \frac{V_{dc,max}^2}{P_{set}} \quad , \quad 5\tau_{dch} = 5 \cdot R_{eff} \cdot C_{smooth} < T_{set}$$

By setting $P_{set} = 10W$ and $T_{set} = 60s$ the calculations become,

$$R_{set} > \frac{(400V)^2}{10W} = 16\ k\Omega \quad , \quad R_{eff} < \frac{60s}{5 \times 1.3mF} \approx 9\ k\Omega$$

Hence two parallel resistors of $R_{set} = 15k\Omega$ are used for an $R_{eff} = 7.5k\Omega$. The rectifier is constructed into a metallic box as shown in Fig. 4.49. The rectifier is stuck to the bottom with a thermal paste to improve cooling. The DCH switch closes the discharge circuit, and the DC switch closes the bridge output. An M10 screw is drilled into the side for ground connection.

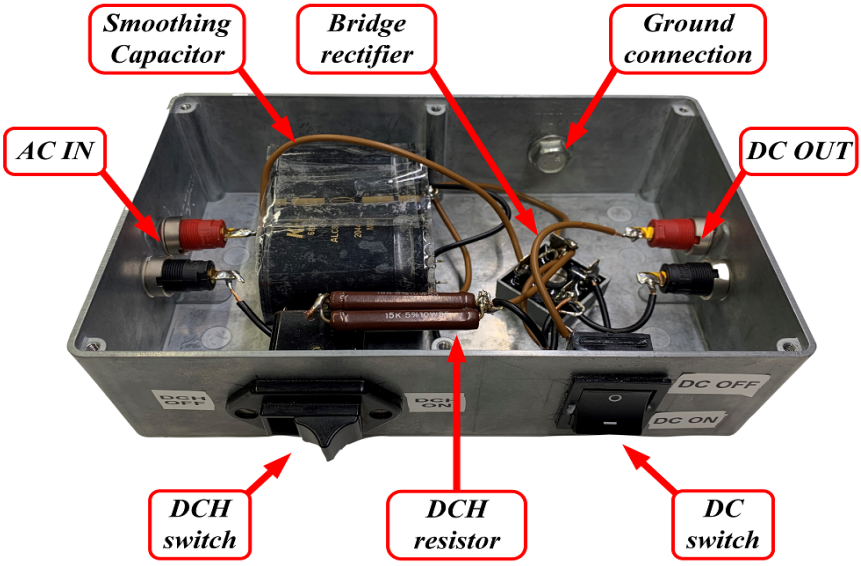


FIGURE 4.49: Rectifier box with discharge circuit and smoothing capacitor

4.7.2 *Dielectric breakdown protection*

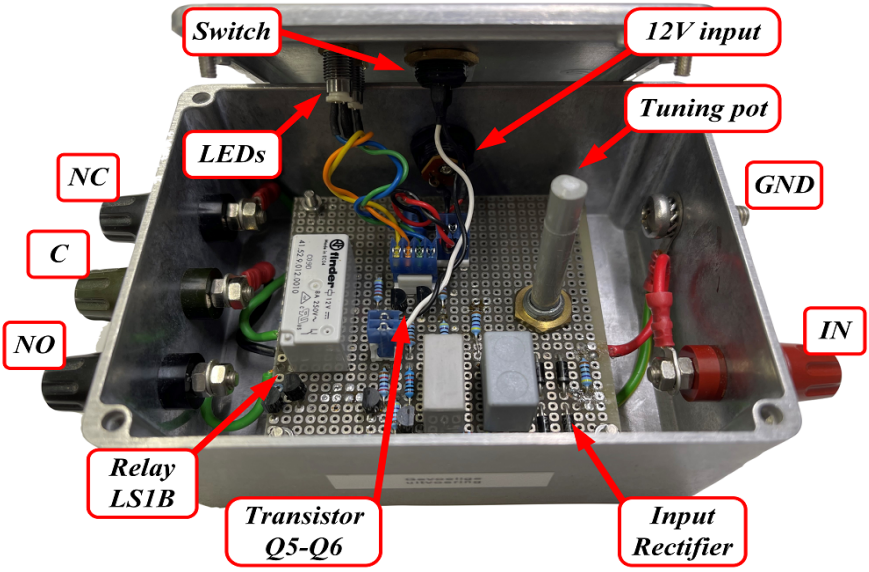
In the event of insulation breakdown, the pulse modulator must be capable of self-opening itself within a few milliseconds. If this is not done correctly, the cellulosic sample will begin to burn due to the conducting arc which can also deform the electrode. To prevent this, a doorslag (breakdown) detector was fabricated by the staff of the HV laboratory at TU Delft. The schematic of this circuit is shown in Fig. 4.50 and has the following elements,

- *J*1-*J*3: To be connected in series with the dielectric under test
- *J*4-*J*5: To be connected in series with the circuit to be broken
- *J*2: To be connected to a 12 V DC power supply
- *LS*1*C*: Relay with two sets of contacts *LS*1*A* and *LS*1*B*
- *R*7: Potentiometer for calibrating detector sensitivity
- *C*3: Calibration capacitor for supporting voltage across *Q*3
- *D*1-*D*3: Indicative LEDs triggered by transistors *Q*5-*Q*6
- *D*3-*D*4-*D*7-*D*8: Bridge to rectify dielectric current
- *D*5: Thyristor surge protection for clamping input current to the circuit

When a 12 V DC is supplied through the header *J*2 a positive voltage is dropped across *R*11 which turns on the transistor *Q*6 and in-turn the red LED *D*2. Next, pushing the switch *SW*1 energises the coil *LS*1*C* moving *LS*1*A* to position 5 and *LS*1*B* to position 7. This produces a positive voltage across transistor *Q*5 thereby turning green LED *D*1 on and red LED *D*2 off. The transistor *Q*4 is also conducting, and the circuit is now ready to detect for breakdown. A breakdown causes a current to pass through *J*1-*J*3 which is rectified through *D*3-*D*4-*D*7-*D*8 and produces a voltage drop across *R*8 and makes *Q*3 to conduct. This pulls down the energising voltage of the coil to zero and opens the contacts between *J*4-*J*5. The de-energising of the coil switches off transistor *Q*5 and green LED *D*1, while the 12 V powers the red LED *D*2 and the detector attains its original state. The detector is soldered onto a board and machined into a metallic box as shown in Fig. 4.51. Microscopic photos were taken to compare the effect of the doorslag detector on sample breakdown, shown in Fig. 4.51 (a-b). The detector significantly sharpens the breakdown with minimal deformation to the electrode, thereby significantly improving the quality of the results.

(a) Breakdown mark without detector

(b) Breakdown mark with detector



(c) Implemented doorslag detector in metallic box

FIGURE 4.51: Effect of doorslag (breakdown) detector on sample

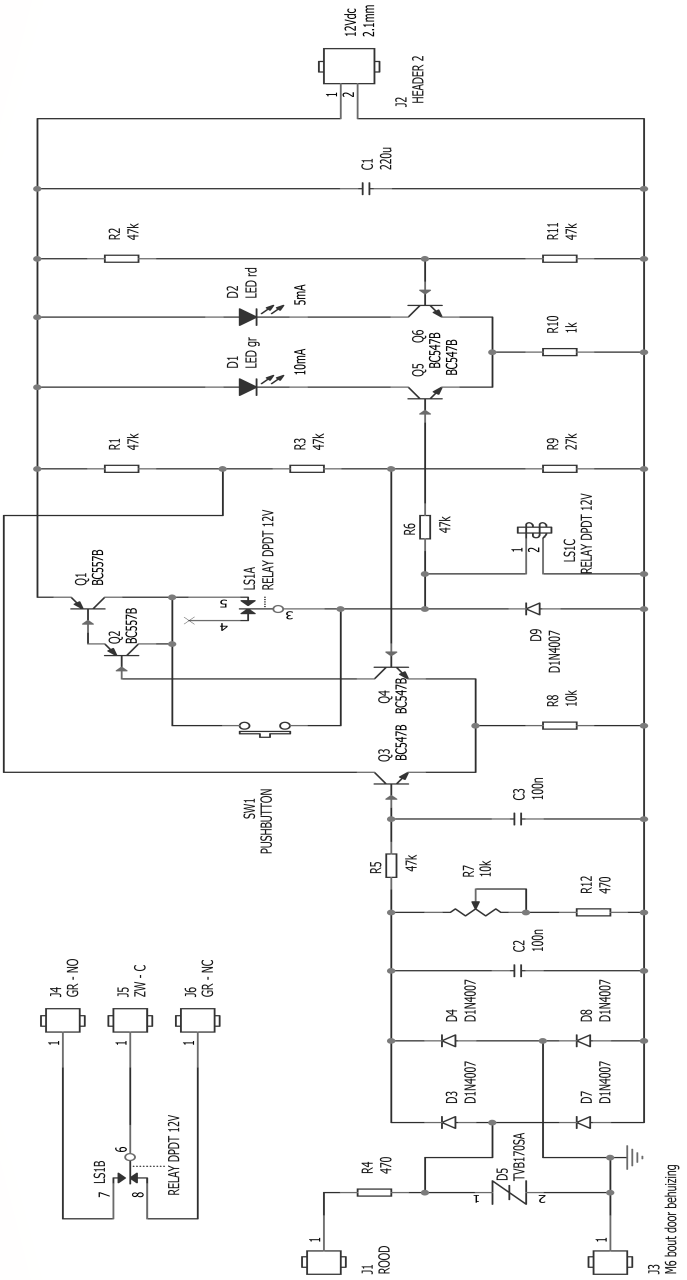


FIGURE 4.50: Circuit schematic of the doorslag detector

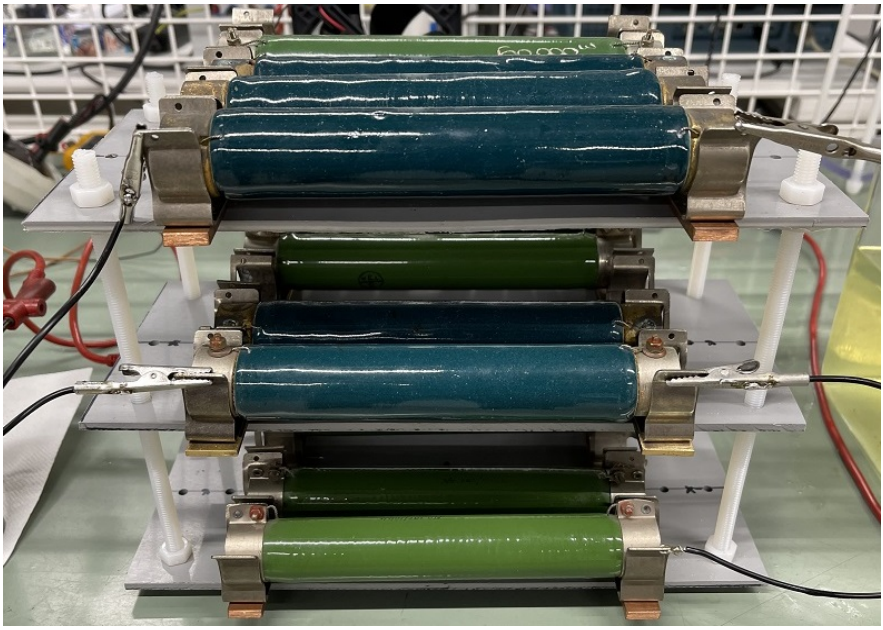
4.7.3 *Variable test elements*

The output pulse waveform can be tuned by varying the values of test resistance R_t and test capacitance C_t in the circuit. This provides the possibility of testing the dielectric under different rise-times and overshoots. However these elements must be capable of withstanding high voltages across and high currents through them. Their construction is described as follows,

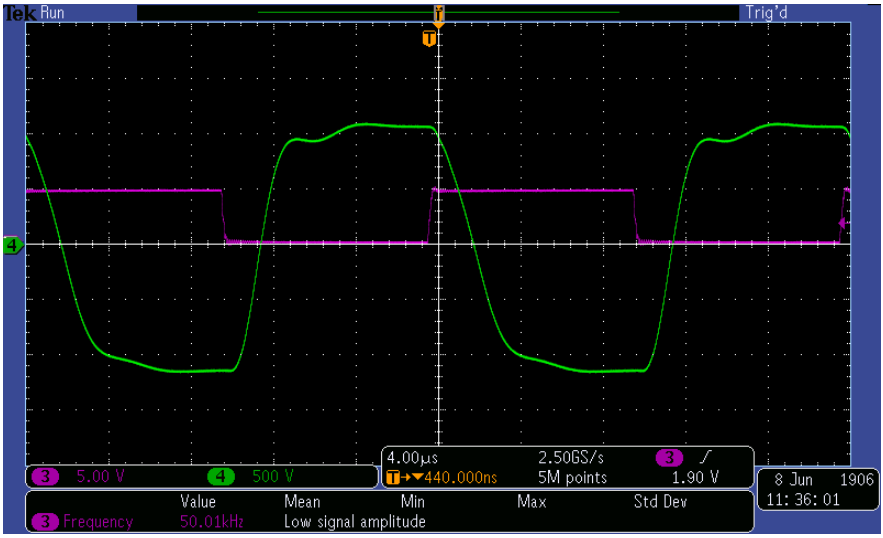
- **Variable Test Resistance** R_t: A resistance bank was constructed with three series sets of five parallel brackets as shown in Fig. 4.52 (a). Increasing the resistance improves the damping and reduces overshoot. However it was observed that beyond a critical value R_t^{max} the rise of the pulse waveform is deformed as seen in Fig. 4.52 (b). This maximal value was found to be around $R_t = 20\ k\Omega$ with single and double layers of oil-paper sample. Hence for the tests an $R_t = 17.75\ k\Omega$ was set which produced the waveform given in Fig. 4.53 (a). Parallel combinations of 20 kΩ and 50 kΩ were used to divide the power. During long-term tests, it is important that the value of resistance remains almost the same. The measured resistances at $T_{R_t} = 25\ ^\circ C$ and $T_{R_t} = 85\ ^\circ C$ (usual operating temperature) were $R_t = 17.75\ k\Omega$ and $R_t = 18.25\ k\Omega$ respectively, indicating that the variation is negligible. Additionally, a 138 CFM fan was placed nearby to keep the temperatures below $T_{R_t} = 50\ ^\circ C$.

- **Variable Test Capacitance** C_t: A high voltage variable capacitor shown in Fig. 4.53 (a) available in the lab was used in the modulator system. The diameter of each metal disk is 20 cm and the distance can be controlling through a rotational handle. The distance between the plates is measured on a linear pitch. The capacitor is connected in parallel to the test sample and the high voltage probe. Decreasing the distance increases the $C_t = \epsilon \frac{A}{d}$ and can be tuned to produce no overshoot in the output waveform as in Fig. 4.54 (a). This flexibility is very important since achieving such a shape with just R_t is impossible due to the R_t^{max} limit. On the other hand, increasing the distance which decreases the C_t can produce an overshoot as seen in Fig. 4.54 (b). This allows the testing of samples under different overshoots. The calibration of C_t must be repeated when the C_l is changed by a large magnitude such as when changing from 1-layer to 2-layer. It should be kept in mind that bringing the plates too close can cause arcing but such a large capacitance is not required.

The thermal and electrical stability of the test elements was observed under different operating conditions (such as long test durations) and it was concluded to be fit for the purpose of ageing experiments.

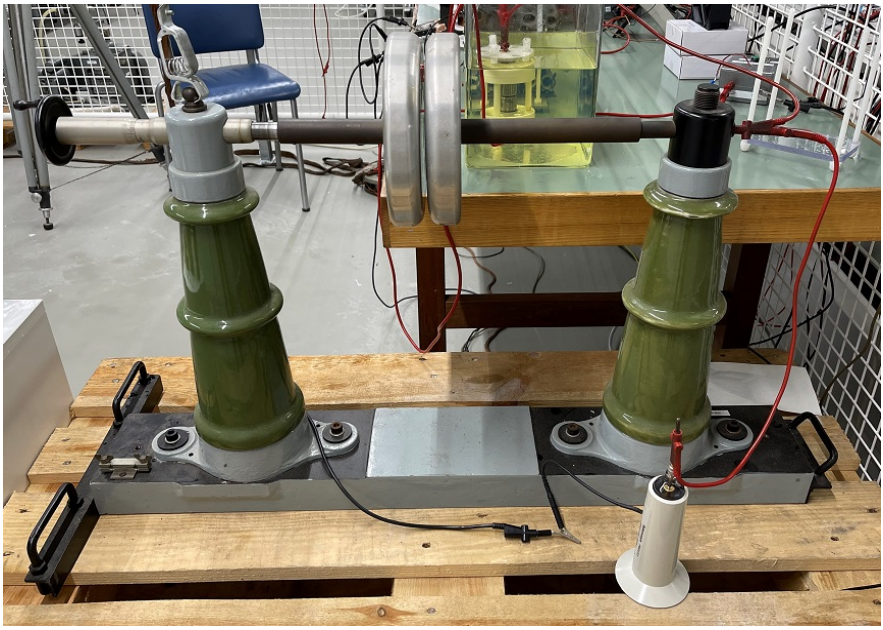


(a) Variable resistance bank constructed in the lab

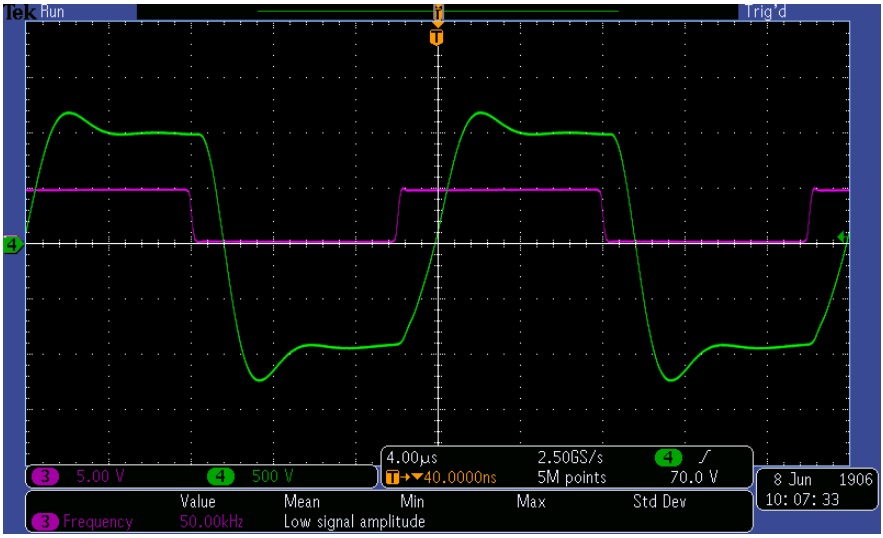


(b) Output waveform when exceeding the R_t^{max} criteria

FIGURE 4.52: Overview of test resistance R_t and the consequence of exceeding R_t^{max} which results in a deformed output pulse shape

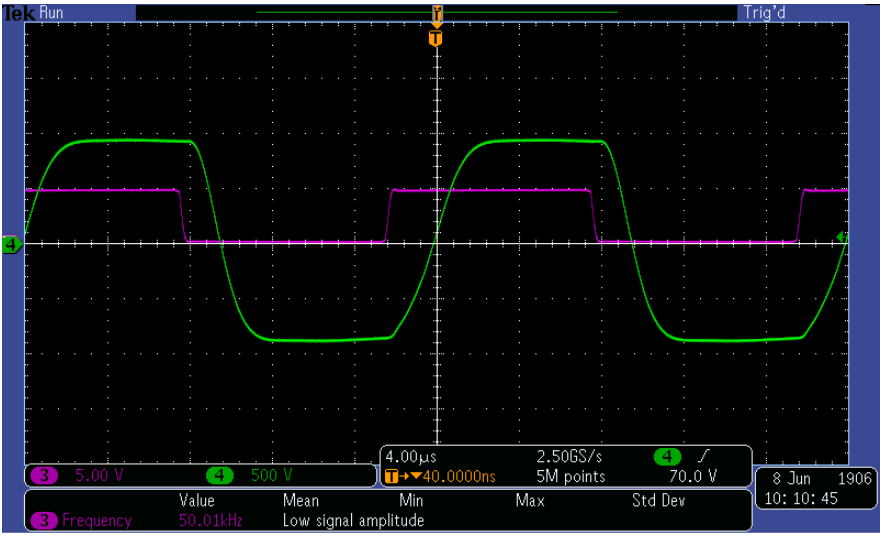


(a) High voltage variable capacitor used as C_t in the modulator

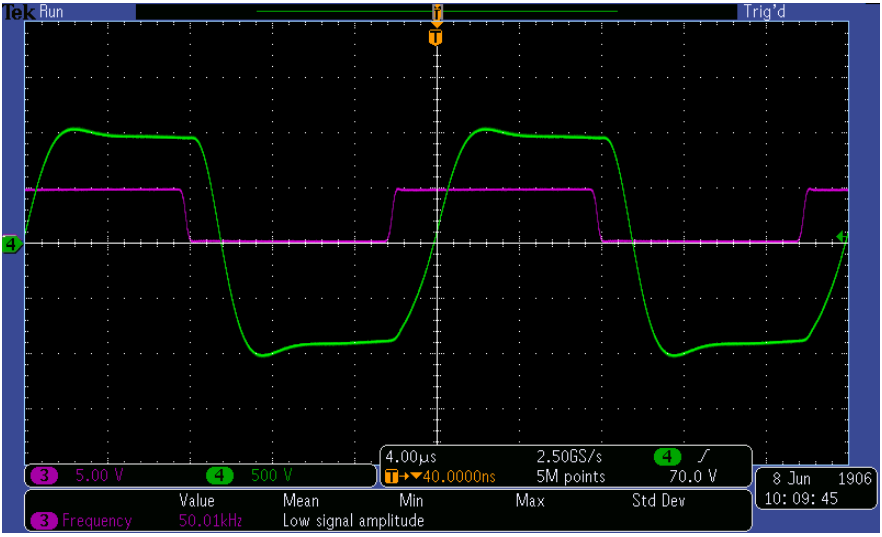


(b) Output pulse waveform without C_t in the circuit. Notice that the overshoot still exists, but increasing R_t further beyond R_t^{max} would cause a deformation.

FIGURE 4.53: Overview of test capacitance C_t and the implemented lab setup



(a) Output pulse with C_t tuned for zero overshoot



(b) Output pulse with C_t tuned for slight overshoot

FIGURE 4.54: Effect of calibrating test capacitor C_t for a 2-layer oil-paper sample. The C_t provides much needed flexibility in tuning the output waveform without solely relying on resistance R_t. Waveforms with overshoot, without overshoot, and over-damped waveforms can now be obtained by easily re-tuning the capacitance.

4.8 MODULATOR SUMMARY

The various components of the pulse modulator system are consolidated into a block diagram shown in Fig. 4.55. The lab setup of the modulator is shown in Fig. 4.56. The modulator operation is summarised as follows,

- **Power supply**: The primary source is the 230 V_{AC} mains linked to a control box capable of breaking large currents during a non-breakdown short circuit event. Switching on the control box powers the modulator and can be switched off manually. The output of the box is connected to one of the primary phases of a three-phase autotransformer (or variac). The secondary phase is passed through an isolation transformer placed inside the cage generating an independent reference for the rest of the modulator. The body of this transformer is earthed. The isolated voltage is rectified and to provide a smooth DC source for the pulse generator.
- **Pulse generator**: The rectified voltage charges the DC link of the H-bridge (Proto-Hx) and is switched into 460 $V_{peak\text{-}peak}$ variable frequency pulses at its output. The switching of the SiCFETs are controlled by an Arduino Nano which sends gating signals the gate drivers. The signal stage of the board is powered by the 5 V programmable DC supply. One of these signals is sent to the DPO 3034 oscilloscope as a trigger. The output of the pulse generator is fed to the pulse transformer.
- **Pulse transformer**: The low voltage pulses are stepped up to the medium-voltage level through the 1:50 PT. The core and secondary windings are grounded. The MV pulses are then transferred to the test elements.
- **Test elements**: The variable R_t and C_t condition the pulses to the desired waveform shape before applying them across the OIP test sample. The sample is placed between an electrode arrangement immerse in oil to prevent surface discharges. The breakdown detector is connected in series with the sample and disconnects the rectifier from the outside of the cage in case of dielectric breakdown. This disconnection is occurs in the live power line between the isolation transformer and the bridge rectifier.
- **Voltage measurements**: The voltage across the OIP sample is measured with a Tektronix P6015A high voltage probe connected to a 300 MHz 2.5 GS/s Tektronix DPO 3034 Digital Phosphor Oscilloscope. Waveform capture and data logs are transferred to a laptop via USB. A Tenma 72-7780 was used to measure current after the isolation transformer, and a Voltcraft VC270 was used to measure DC link voltage.

The modulator can produce voltages up to $V_{out} \approx 7\ kV_{peak}$ or $V_{out} \approx 14\ kV_{peak-peak}$ without any discharges, and even more with few discharges. The operational frequency can be varied from 10 kHz to 50 kHz. Below 10 kHz, higher voltages would be required to break the OIP sample which leads to saturation. Above 50 kHz, the rise-time of the pulse becomes comparable to the pulse width. Although this chapter ends here, the actual design procedure was highly iterative involving several back-and-forths to ensure that the modulator is capable of successfully breaking down the test samples. The major limitations faced when building the modulator were the small core window size and unavailability of a industry-made high power DC source. However it is due to these shortcomings that the failures and weak points could be experienced and thoroughly analysed.

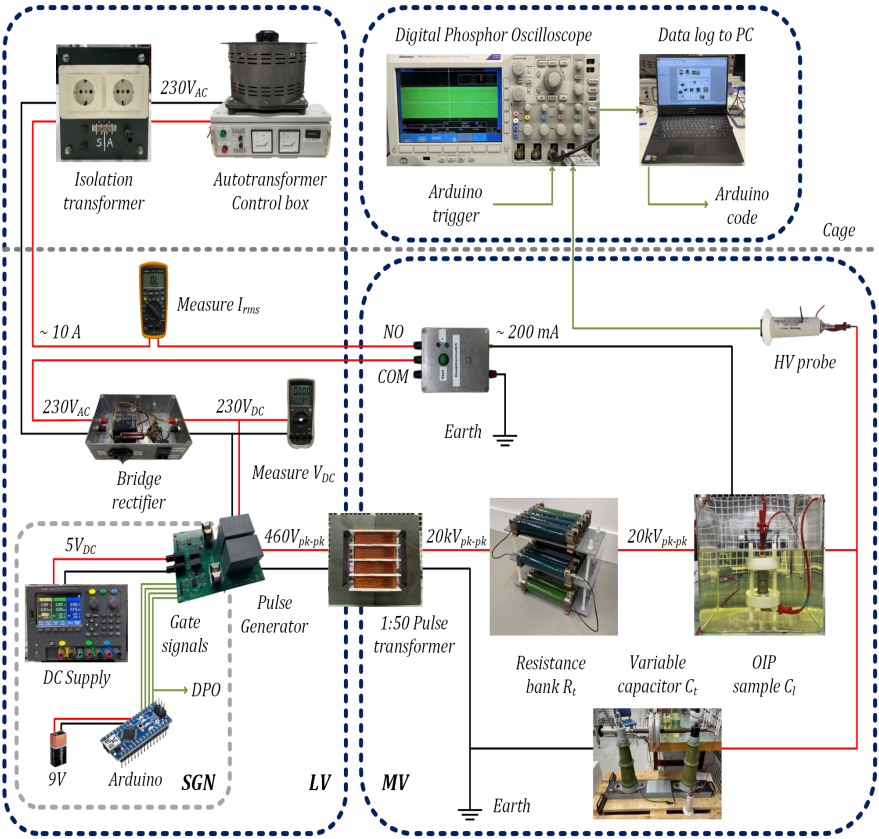


FIGURE 4.55: Block diagram of solid-state fed pulse transformer modulator

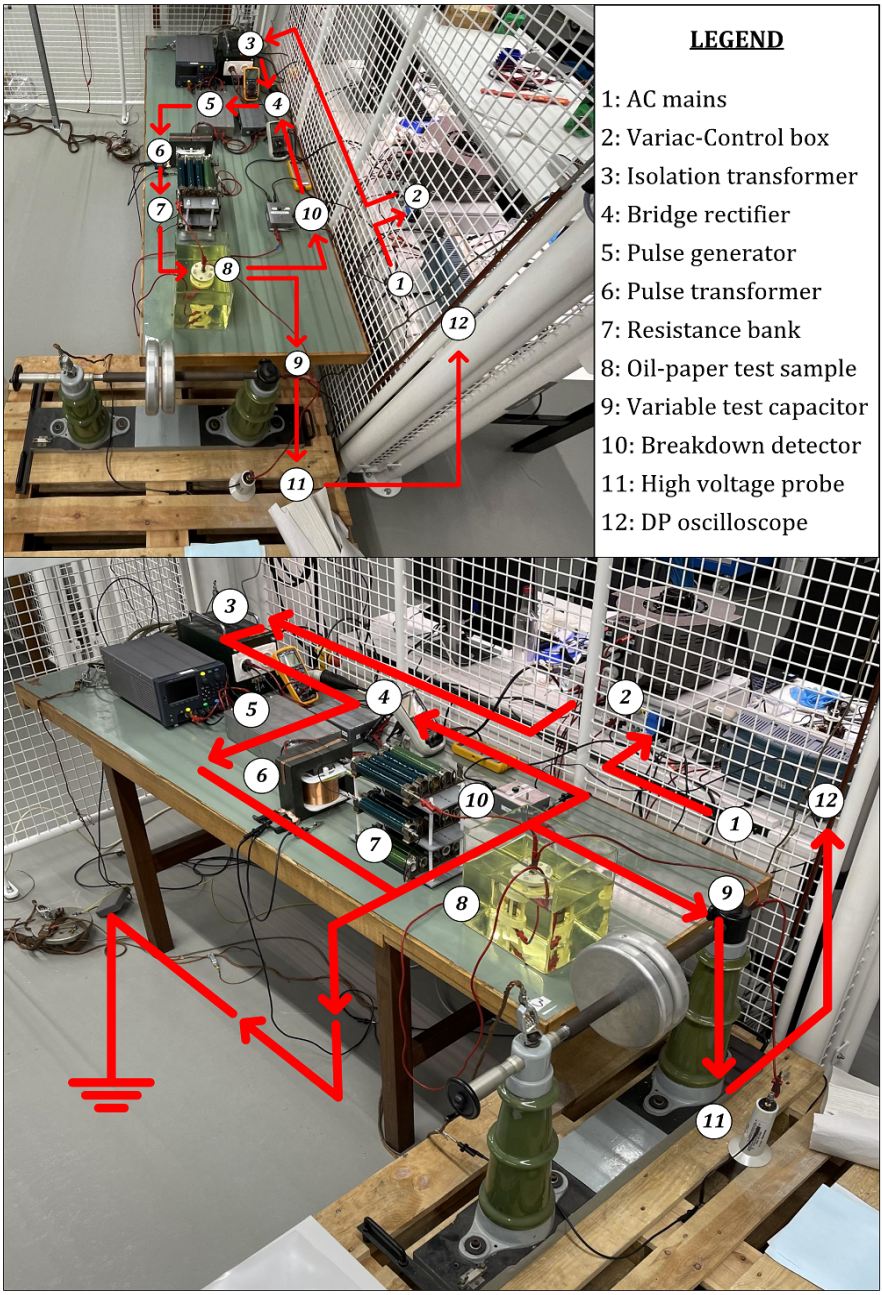


FIGURE 4.56: Lab setup of the pulse modulator for testing cellulosic insulations

5

AGEING EXPERIMENTS

No matter how many times the results of experiments agree with some theory, you can never be sure that the next time the result will not contradict the theory.

STEPHEN HAWKING
A Brief History of Time (1988)

With the pulse modulator designed in Chapter 4, the final task is to study the performance of oil-impregnated paper when subjected to the produced pulsed waveforms. The subsequent sections of this chapter describe the theory related to dielectric losses and inverse power law distributions, the followed test protocol including sample preparation procedure, electrode arrangement, and fine-tuning and calibration of equipment. Finally, the results from the breakdown and ageing experiments are discussed.

5.1 THEORETICAL BACKGROUND

5.1.1 *Dielectric loss under sinusoidal stresses*

When a voltage is applied across an ideal dielectric, the current flowing through it is purely capacitive. However non-ideal dielectrics such as electrical insulation possess a non-infinite resistance due to the existence of conductive impurities. In this case, the current flow is a combination of resistive (in phase with voltage) and capacitive (leads the voltage by 90°) components, the ratio of which yields $\tan\delta$. Higher $\tan\delta$ indicates higher resistive current flows leading to dielectric heating as per Joule's law. As shown by F. H. Kreuger in [40] the dielectric loss in a capacitance C depends on the applied voltage U and the excitation frequency ω as,

$$W = U^2 \omega C \tan\delta \tag{5.1}$$

Under sinusoidal excitation the above equation becomes frequency dependent. The modified relationship can then be written as,

$$W = U_{rms}^2 \omega C'(\omega) \tan\delta(\omega) \tag{5.2}$$

Thus, dielectric losses increases with an increase in excitation frequency.

When the sinusoid is polluted with harmonics, the dielectric heating due to the additional harmonics must also be considered. B. Sonerud *et al.* [42] described this as the sum of each component,

$$P = \sum_{n=1}^{\infty} |U_n|^2 \, n\omega_0 C'(n\omega_0) \tan\delta(n\omega_0) \tag{5.3}$$

Where n is the harmonic number and ω_0 the fundamental frequency.

5.1.2 *Dielectric loss under pulsed stresses*

Compared to the sinusoidal waveform, the pulsed waveform contains the fundamental sine component as well as higher frequency content corresponding to the rise-time. To derive the losses under quasi-rectangular waveforms, the pulse is first assumed to be almost square but with exponential rise-times. The time and frequency-domain expressions are,

$$U(t) = U_p(1 - e^{-t/\tau}) \tag{5.4}$$

$$U(j\omega) = \frac{U_p}{j\omega(1 + j\omega\tau)} \tag{5.5}$$

The cutoff frequency is then defined as $\omega_c = \frac{1}{\tau}$. The behaviour of losses differs above and below this cut-off frequency and is written in [42] as,

$$P \propto U^2\omega_n \propto \omega_n^{-1} \qquad \omega_n \ll \omega_c \tag{5.6}$$

$$P \propto U^2\omega_{\mathrm{n}} \propto \omega_n^{-3} \qquad \omega_n \gg \omega_c \tag{5.7}$$

This shows that above the cutoff frequency ω_c the rise-time begins to play a role by reducing the harmonic amplitudes as shown in Fig. 5.1.

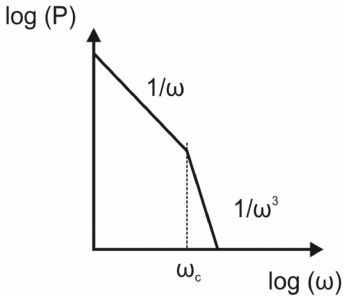


FIGURE 5.1: Behaviour of dielectric loss power over frequency [42]

5.1.3 *Weibull distribution for breakdown strengths*

To estimate the breakdown strength of an insulation, ramp field tests are conducted at a specified ramp rate and the breakdown fields are recorded. The data is then plotted on a special Weibull probability graph. This graph linearises the cumulative probability of failure $F(E)$ on the y-axis across the breakdown strengths E_{break} on the x-axis. This is expressed in the form,

$$F(E) = 1 - e^{\left(\frac{E_{break}}{\alpha}\right)^{\beta}} \tag{5.8}$$

The constant β is called the shape parameter and represents the slope of the line. The constant α is called the scale parameter and is determined as the E_{break} corresponding to a $F(E) = 63.2\%$ on the graph. It was shown in [87] that the value of α for single-layer OIP reduces from 77.0 to 59.9 at 50 Hz and 1500 Hz respectively. This means that the breakdown strength of OIP at 50 Hz is significantly larger than that at 1500 Hz. It was also shown that the value of β for single-layer OIP reduces from 16.85 to 7.29 at 50 Hz and 1500 Hz respectively. This means that higher frequencies produce "spread" in the breakdown data making it harder to design the insulation. This study will be extended through the results from this thesis.

5.1.4 *Inverse power law model for lifetime estimation*

To estimate the remaining lifetime of an insulation, accelerated ageing tests are conducted at field levels that are much higher than the nominal operational level. Several tests are carried out at a few selected field levels and the median at each level is used to extrapolate a lifeline on a log-log scale. If this method procedure results in a straight-line then the life of the insulation is said to fit an inverse power law model. Such a model predicts that the remaining lifetime T_{life} of a sample is inversely proportional to the n^{th} power of the applied field E (kV/mm). This is expressed in the form,

$$T_{life} = k \cdot \left(\frac{E}{E_0}\right)^{-n} \tag{5.9}$$

The constant k has a unit of time and varies with test conditions like number of layers while E_0 has a unit of electric field ($1\ \frac{V}{mm}$). The constant n is the slope of the lifeline indicating the sensitivity of a given insulation to a change in field. It was shown in [87] that the value of n for single-layer OIP reduces from 25.64 to 7.15 at 50 Hz and 1500 Hz respectively. This means that operating at higher frequencies causes the insulation to be less sensitive to field and depend more on the applied frequency.

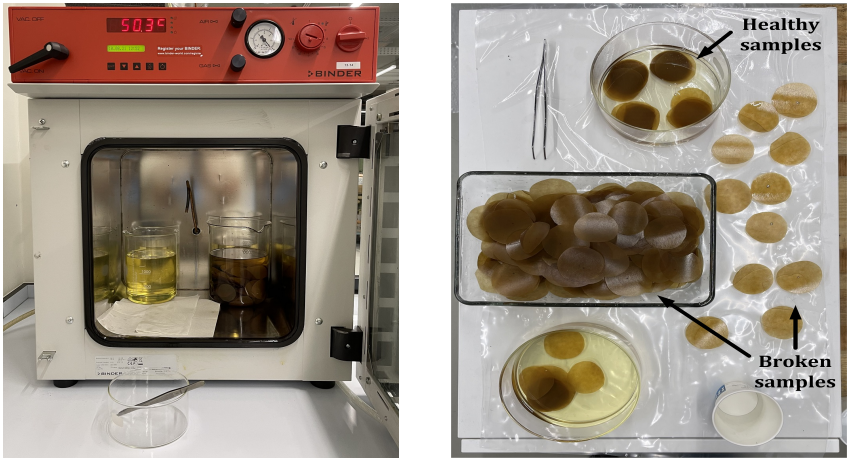
5.2 TEST PROTOCOL

5.2.1 *Preparing oil-paper samples*

The samples and their preparation is the same as that described in [87]. The paper used for the ageing tests is Tervakovski cable paper and has an average thickness of 150 μm. Circular samples were cut out manually from a larger sheet and impregnated inside a BINDER VD 53 vacuum oven shown in Fig. 5.2 (a). The impregnation procedure is summarised as follows,

- First, the samples were vacuum dried at 120°C for 24 hours.
- The oven temperature was reduced gradually to 60°C after which the chamber was filled with dry nitrogen. The oil container was placed inside and the pressure reduced to 5 mbar. The oil and paper were vacuum dried at 60°C for another 24 hours.
- The samples were placed inside the oil container and left to impregnate under vacuum at 60°C for 24 hours.
- Finally, the heater was turned off and the samples cooled in vacuum.

The samples are kept under oil, transferred to the electrodes when testing, and then transferred into a glass dish to observe breakdown patterns.

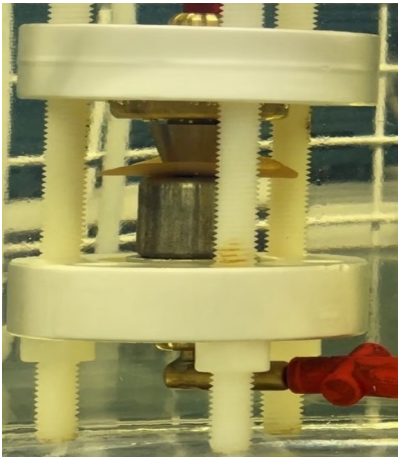


(a) BINDER VD vacuum oven (b) Sample table during experiments

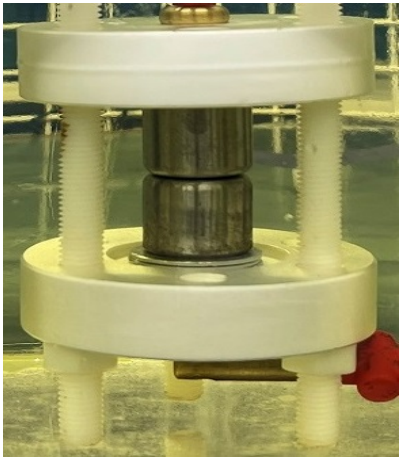
FIGURE 5.2: OIP sample workflow from impregnation to sample table

5.2.2 *Arranging test electrodes*

A teflon frame was built to connect the electrodes via BNC. Two arrangements were tested *viz.* the conical-cylindrical in Fig. 5.3 (a) and the complete cylindrical in Fig. 5.3 (b). The latter was selected with $d = 2.54\ mm$ for the tests for applying uniform field across the OIP sample. The electrodes were immersed in oil to prevent surface discharges as shown in Fig. 5.3 (c).



(a) Conical-cylindrical electrode



(b) Complete cylindrical electrode

(c) Surface discharges in OIP sample due to drying up of oil

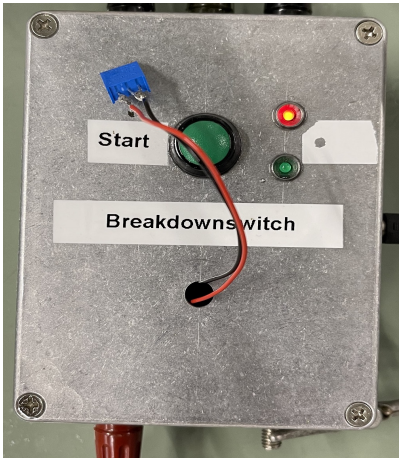
FIGURE 5.3: Oil-immersed electrode arrangement for the ageing tests

5.2.3 *Tuning breaker sensitivity*

The breaking method at high frequencies is a challenge due to high $\frac{dV}{dt}$ of the output waveform. The designed breakdown detector measures the current flowing through the OIP sample and disconnects the modulator from the supply if the current exceeds a certain threshold. The value of this threshold determines the sensitivity of the detector and can be controlled with a tuning pot as shown in Fig. 5.4 (a). The recorded observations were,

- If the detector is made over-sensitive, the supply would disconnect before sample breakdown. Thus the sensitivity had to be tuned for lifetime tests at different voltage levels. The tuning should be made less-sensitive during ramp breakdowns to avoid neglecting healthy samples.
- If the detector is made less-sensitive, the breakdown of the sample leads to an unextinguished arc thereby carbonising the paper and deforms the electrode. The sensitivity was hence also checked by analysing the breakdown mark on the sample under an Olympus SZH-ILLD microscope shown in Fig. 5.4 (b). The effect of sensitivity on the mark is illustrated in Fig. 5.5. The mark was observed to be less severe at 10 kHz than 50 kHz.

The optimal resistance value was found to be between 30 Ω and 60 Ω.



(a) Tuning pot (blue) of detector

(b) Olympus SZH-ILLD microscope

FIGURE 5.4: Overview of breakdown detector and analysis of its sensitivity

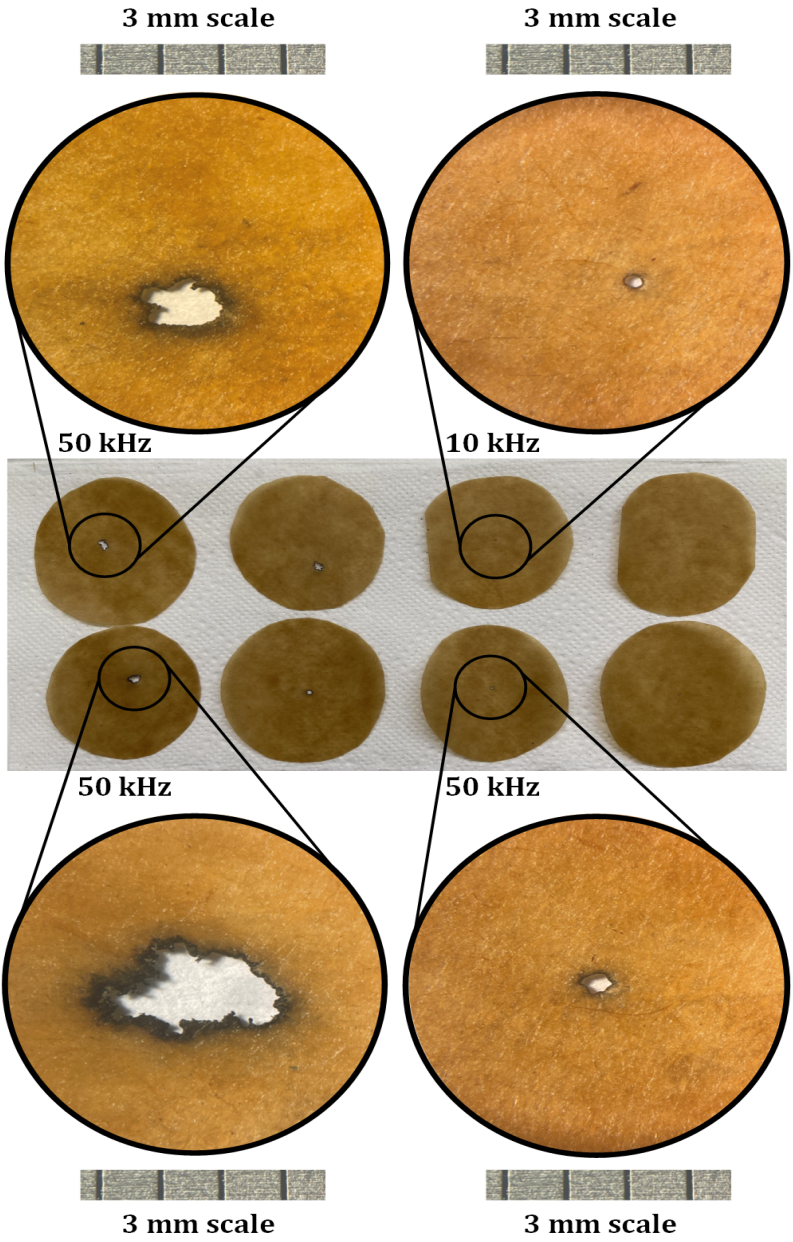
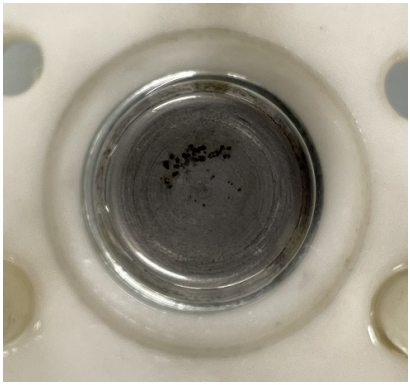


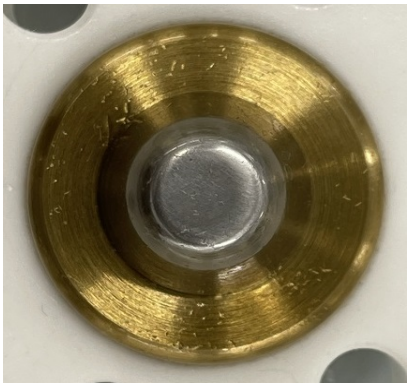
FIGURE 5.5: Effect of increasing sensitivity (left to right) on breakdown mark.

Although the detector sensitivity is important, it is quite difficult to always tune it perfectly. It is therefore expected that breakdowns would inevitably cause deformation to the electrode as shown in Fig. 5.6 (a-b). In some cases such as ramp breakdown tests it is statistically favourable to tune the detector for less sensitivity, polish the uniformly electrode after every test, and carry out a larger number of tests to reduce any bias. The electrodes were polished very finely in a slow circular motion using a P2000 sand paper. The results are shown in Fig. 5.6 (c-d). The position of the spots also gives an indication if there are sharp points which cause the breakdown to occur faster than usual, and the electrode must hence be polished again uniformly. As such, the spots at 10 kHz were observed to be less prominent than at 50 kHz. Hence polishing was carried out more frequently at 50 kHz.

(a) Cone before polishing



(b) Cylinder before polishing



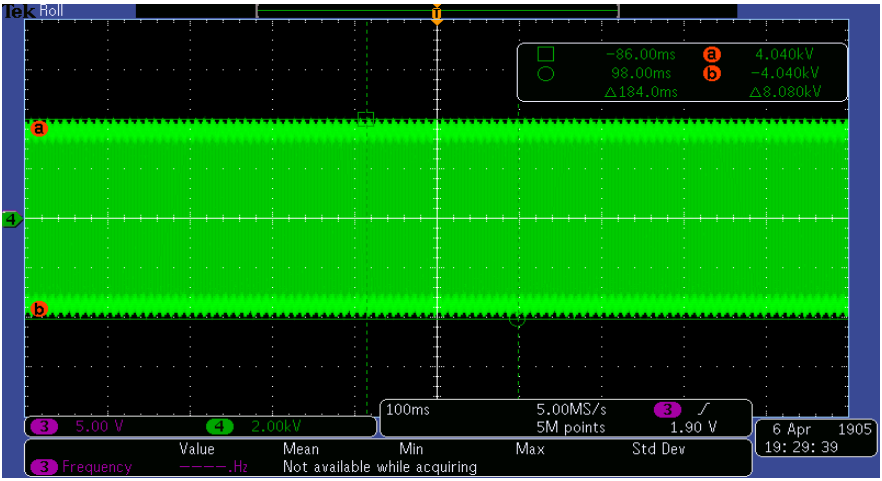
(c) Cone after polishing

(d) Cylinder after polishing

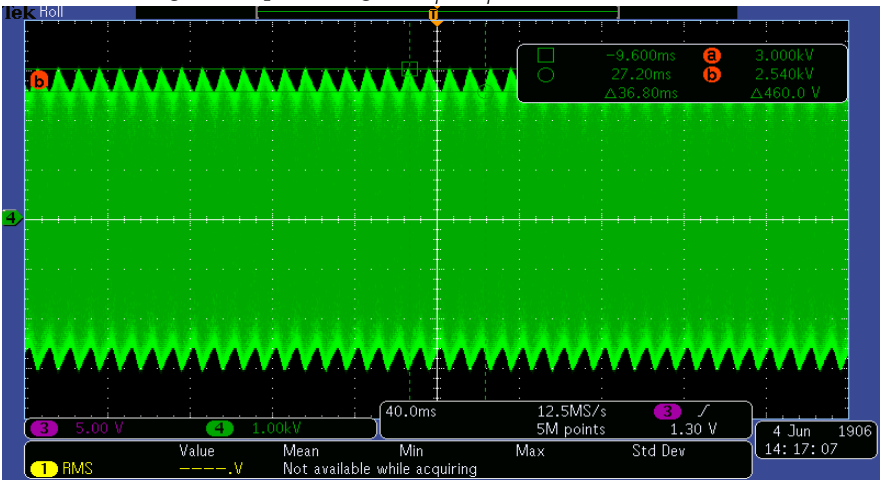
FIGURE 5.6: Breakdown spots on electrodes before and after sandpaper polishing

5.2.4 *Calibrating applied voltage*

The lifetime and breakdown of insulations are highly sensitive to slight changes in field and hence even more so with voltage. Due to a small 50 Hz ripple, the $V_{peak-peak}$ was considered for the tests as shown in Fig. 5.7. This ripple was observed to be more at 50 kHz due to higher current draw.



(a) Calibrating the output voltage to $V_{peak-peak} = 8.08\ kV$ and $E = 27\ kV/mm$



(b) Measuring the ripple in the output waveform using vertical cursor lines

FIGURE 5.7: Overview of calibrating $V_{peak-peak}$ and applied field

5.2.5 *Setting frequency in Arduino*

To carry out testing at different frequencies, the widths of the pulses being generated from the Arduino must be accurately controlled. The interrupt feature of the Arduino was disabled to prevent jittering. Then the inline assembler statements were used which are assembly code encased in parenthesis preceded by the compiler keyword *asm*. The assembly instruction *nop* stands for no operation, and placing this in the code as shown in Fig. 5.8 introduces an operation skip. This produces exact frequencies of $f = 50.0\ kHz$ instead of, for example, $f = 50.1\ kHz$ or $f = 49.9\ kHz$.

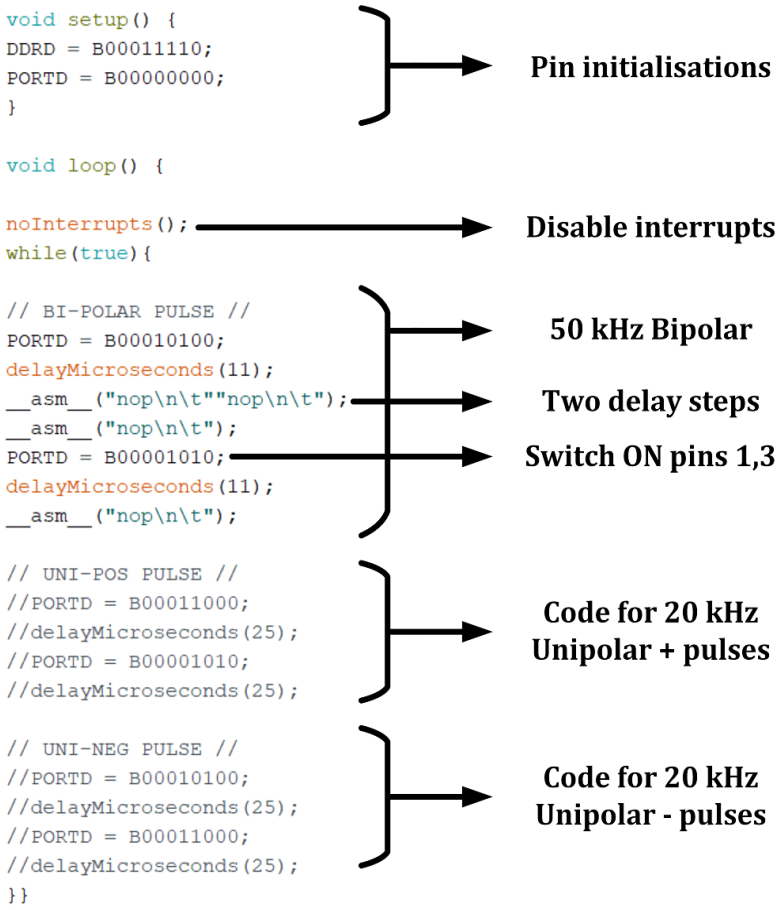


FIGURE 5.8: Implemented arduino code for fast, jitter-less, and accurate pulses

5.3 DIELECTRIC EXPERIMENTS

5.3.1 *Determining breakdown strength*

Ramp tests with slope 1 kV_p/s were carried out at 50 kHz for cylindrical and conical electrodes. The results were linearised with a Weibull distribution plot as shown in Fig. 5.9. The cylindrical electrode applies the electric field across more area of the sample thereby lowering its breakdown strength. The obtained Weibull parameters are summarised in Table 5.1.

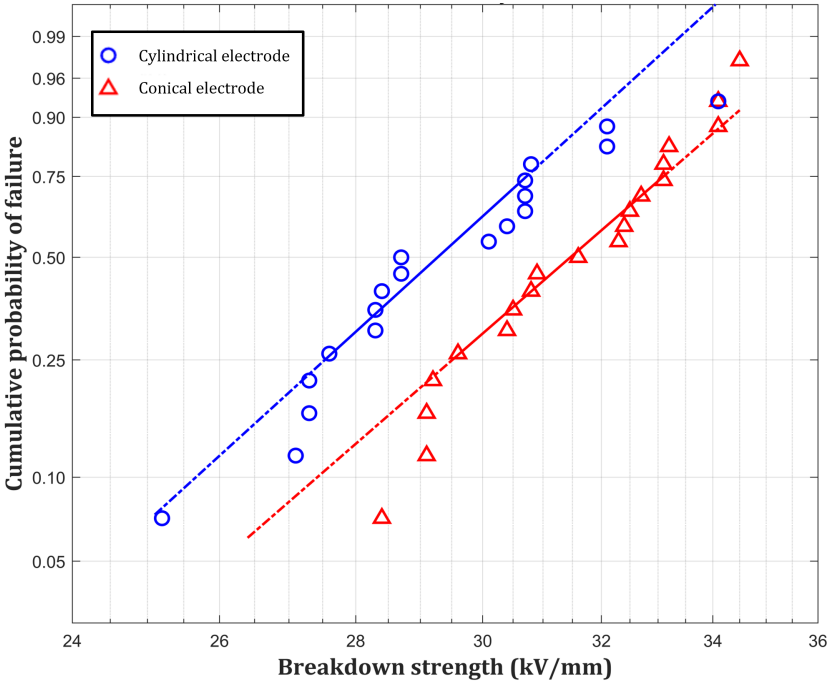


FIGURE 5.9: Comparison of Weibull plots with cylindrical and conical electrodes

STUDY CASE	β	$\alpha\,(kV_p/mm)$	ρ
Conical electrode	32.285	18.053	0.901
Cylindrical electrode	31.256	17.839	0.988

TABLE 5.1: Obtained Weibull distribution parameters

5.3.2 *Estimating remaining lifetime*

From the 50 kHz breakdown test results, a set of 6 electric field values were selected for the accelerated ageing tests. The highest of these values must be smaller than the lowest recorded value *i.e.* $E \approx 25\ kV/mm$. This is to ensure that the samples take some time to breakdown. The selected values were $E = 24,\ 23,\ 22,\ 21,\ 20,\ 19\ kV/mm$ which are $V_{peak-peak} = 7.2,\ 6.9,\ 6.6,\ 6.3,\ 6.0,\ 5.7\ kV$ considering a $d_{sample} = 150\mu m$. The frequency was set and the rise-time recorded to be $T_r = \frac{3.68}{2}\ \mu s$ for both 50 kHz and 10 kHz as shown in Fig. 5.10 and Fig. 5.11, respectively. The voltage droop is more noticeable at 10 kHz due to longer pulse width t_p however the change in magnitude is negligible compared to the 50 Hz ripple of the waveform. The voltage was then calibrated to the desired value by placing a single-layer OIP between the test electrodes. It is important to note that calibrating for single-layer tests must be done with single-layer samples only. The test begins with switching the control box and recording the starting time on the oscilloscope. After the sample breaks down, the time taken for failure is calculated with the end time and recorded. If a sample takes far longer than usual then the test is halted and recorded as such.

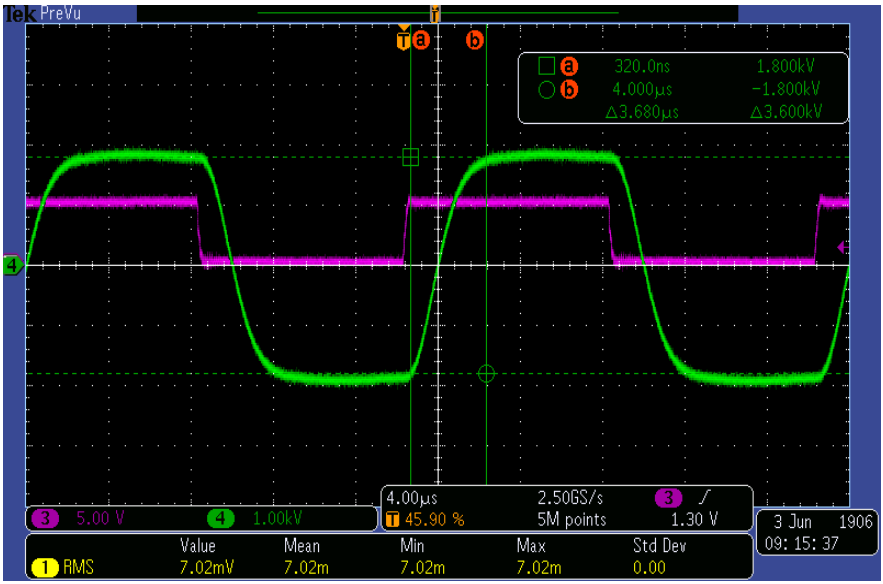
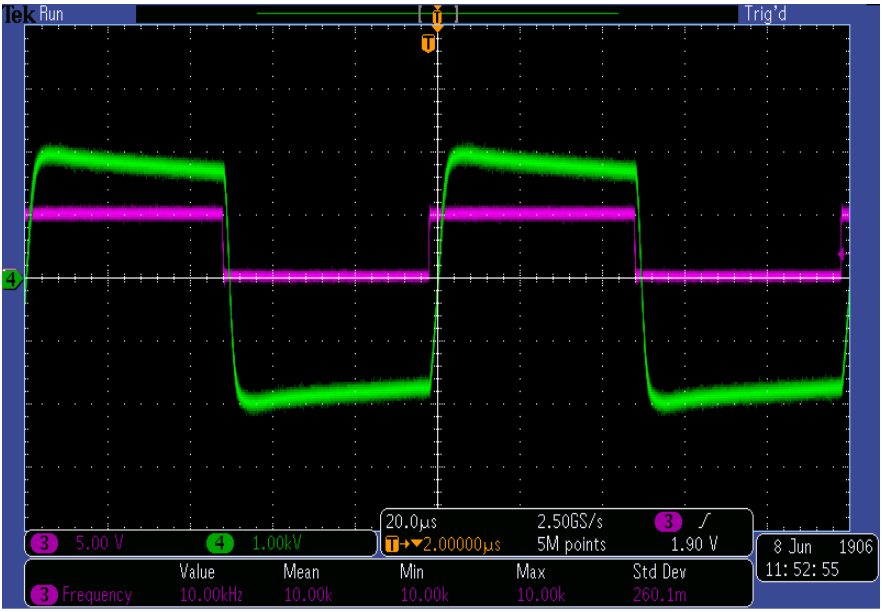
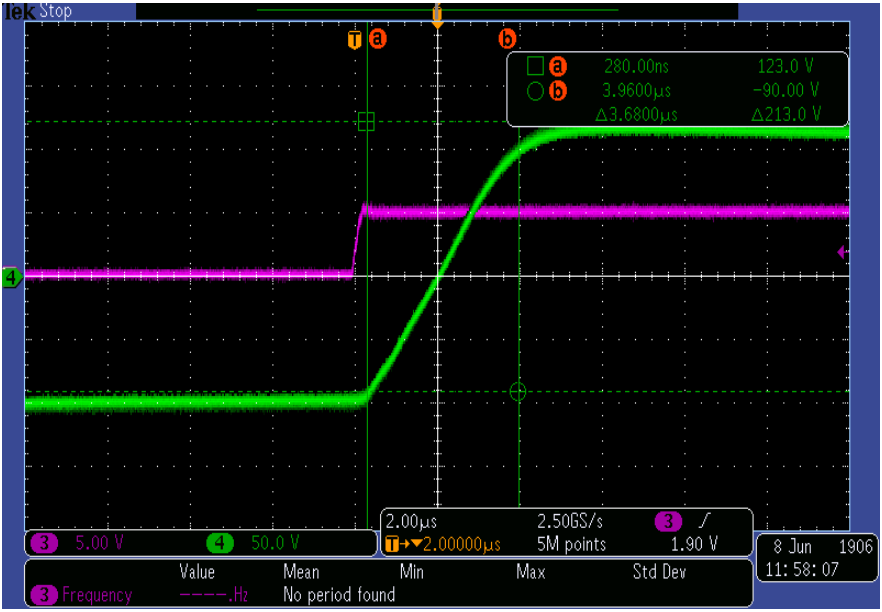


FIGURE 5.10: Measuring bipolar rise-time as 3.68 μs. Hence, $T_r = \frac{3.68}{2} = 1.84\ \mu s$



(a) Pulse waveform shape at 10 kHz. The slight droop is due to time constant.



(b) Measuring rise-time of the pulse waveform at 10 kHz

FIGURE 5.11: Produced pulse waveform at 10 kHz

A total of 292 tests were carried out with 21 to 41 tests at each field value resulting in a total test time of 38,558 s $\approx$ 10.7 hours. Each data point was then plotted on a log-log scale in MATLAB as shown in Fig. 5.12. First, the 50 kHz lifetime tests were carried out. Then the field values for 10 kHz were selected as $E = 30,\ 29,\ 28,\ 27\ kV/mm$. The medians (blue points) at each field were connected with a best-fit line to produce the lifetime line of the insulation. An interesting observation was that below $E = 21\ kV/mm$ the slope of the line drastically increased. This indicates that there is a transition in insulation ageing mechanism below this point. The obtained lifetime parameters for each curve are summarised in Table 5.2.

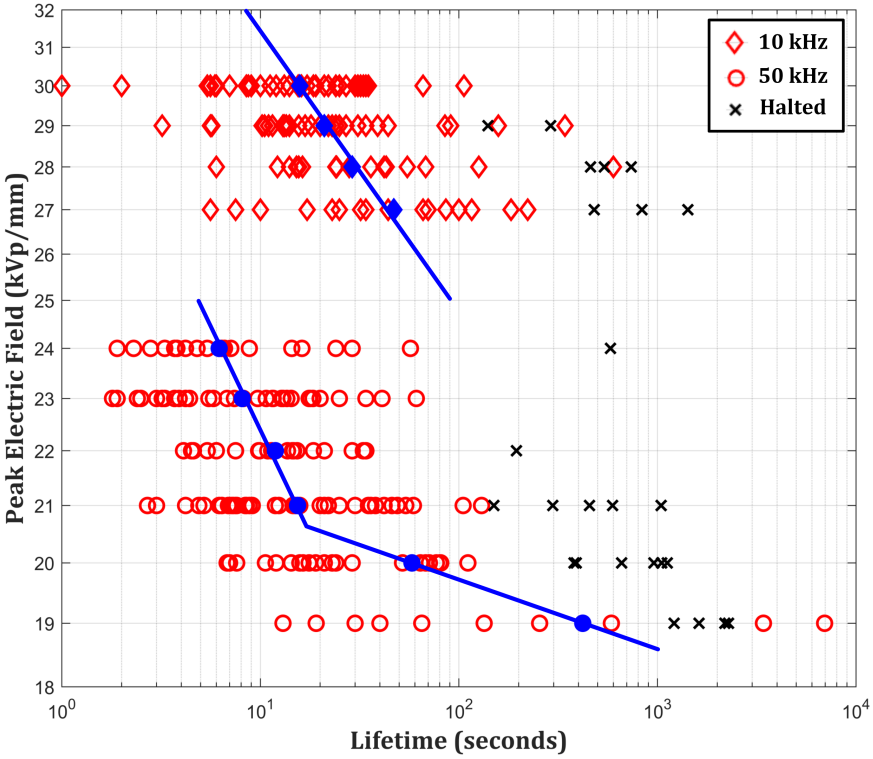


FIGURE 5.12: The lifetime curves obtained at 10 kHz (red diamonds) and 50 kHz (red circles). The blue points are the median values for each field set. The black crosses are halted experiments. The slope of the lifetime at 50 kHz "bends" further away below $E = 21\ kV/mm$ indicating a shift in ageing mechanism below this point.

A clearer plot is provided in Fig. 5.13 containing only the median points and the lifetime curves. The transition point seems to lie between $E = 21\ kV/mm$ and $E = 20\ kV/mm$. More tests could be conducted at a field value in between these, say $E = 20.5\ kV/mm$, however this was not done due to lack of time. This transition point has not been observed before for OIP since the applied field for the tests are usually in the range of $E = 70\ kV/mm$ [87].

STUDY CASE	n	k
10 kHz (above transition)	9.5	1.7×10^{15}
50 kHz (above transition)	6.9	2.1×10^{10}
50 kHz (below transition)	37.5	3.6×10^{50}

TABLE 5.2: Obtained lifetime curve parameters

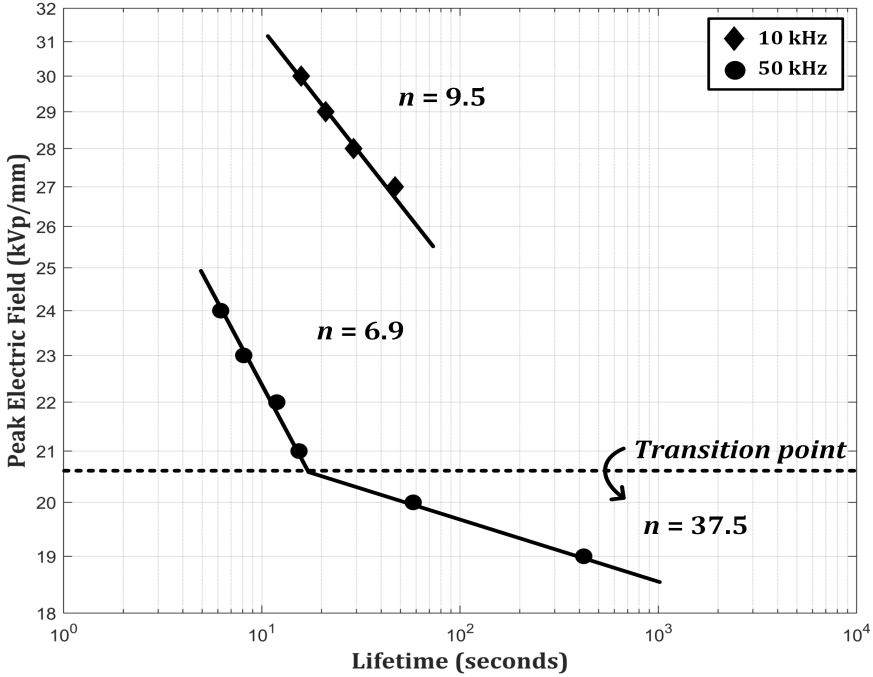


FIGURE 5.13: Clean lifetime curves illustrating the transition point

There are two possible hypotheses to explain the transition phenomenon,

- It is possible that a field enhancement occurs at the edge of the electrodes, which exceeds the PDIV of oil at that point. This could accelerate the breakdown of the paper itself. If true, the breakdown marks on the sample would tend to be on the extreme outer rim of the electrode. However by observing the breakdown marks of all broken samples, this is was concluded to not be the case.
- It is possible that there exists oil-filled voids within the paper between its individual fibres as shown in Fig. 5.14. Above a certain field, the field enhancement within these cavities could then exceed the local PDIV thereby causing partial discharges to occur. This would then accelerate the ageing of the insulation, very similar to [36].

Although the second hypothesis could explain the observed phenomenon, it still requires further verification and analysis. This is out of the scope of this thesis, but will be discussed in the summary.

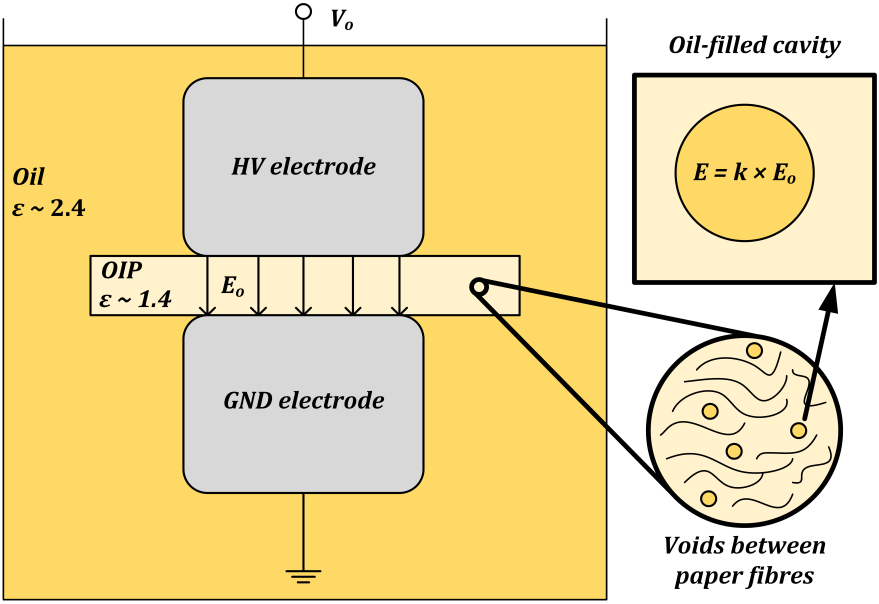
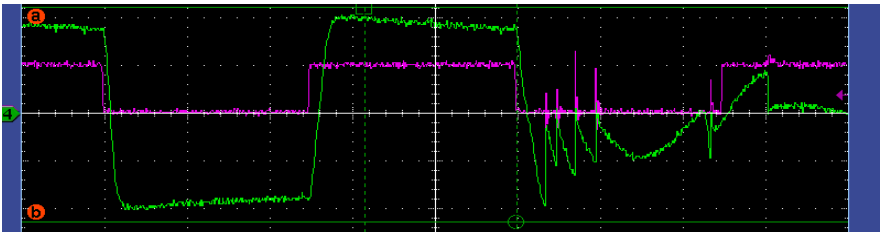


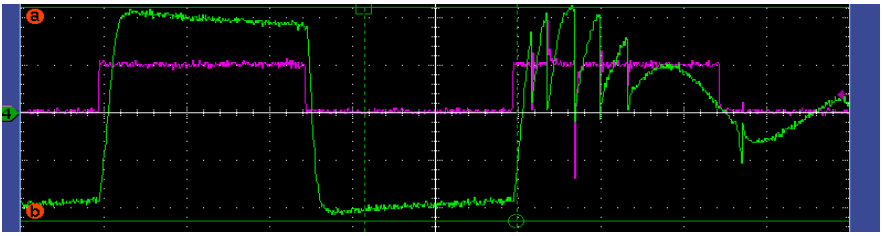
FIGURE 5.14: Hypothesised oil-filled cavities within the paper insulation

5.3.3 *Analysing breakdown instant*

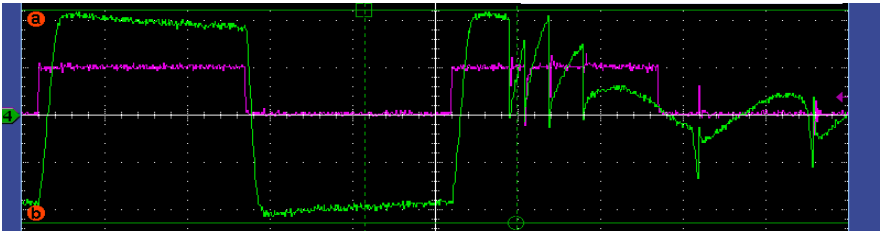
Additionally, the breakdown instants were analysed. Breakdowns during the fall time as in Fig. 5.15 (a) are the most common, but can also occur during the rise-time and at both pulse tops, albeit with less likelihood.



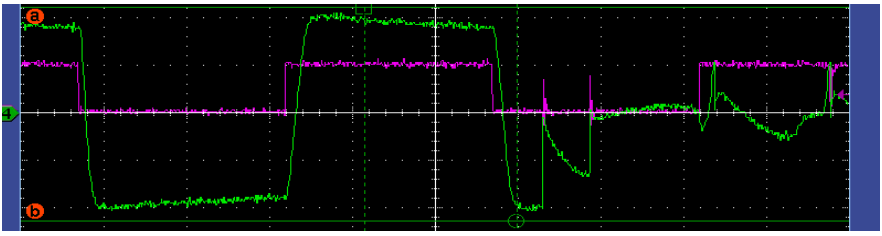
(a) Breakdown during the fall time of the pulse



(b) Breakdown during the rise time of the pulse



(c) Breakdown during the positive pulse top



(d) Breakdown during the negative pulse top

FIGURE 5.15: Various breakdown locations observed during the tests

5.4 RESULTS SUMMARY

The results from the ageing experiments certainly provided more insight into the ageing of oil-paper and in-turn its suitability for medium-frequency applications. These insights are summarised as follows,

- The suitability of oil-impregnated paper as an insulation in MFTs is highly unlikely, at least in its current form. The increase in frequency causes a severe reduction in lifetime of OIP which can only be countered by designing thicker insulation systems or developing new techniques of reinforcing the OIP. The former is not attractive since the main advantage of MFTs are their smaller form factors. The latter is expensive and requires more exploration to determine if it is monetary feasible.

- The slope of the lifetime curve becomes more sharp with an increase in frequency. The slope at 1500 Hz in [87] is smaller than that of 50 kHz obtained here due to larger electrode size. However the trend remains consistent in both works. From a qualitative stand-point, the decrease in n appears to slow down with increasing frequency meaning that it might not decrease any more beyond this point. Moreover, the operational frequencies in SSTs are not expected to exceed 50 kHz.

- A transition point was clearly observed indicating a shift in ageing mechanism at lower fields. This could not be observed before in ageing tests at higher field stresses with lower frequencies. Testing at higher frequencies, however, allows us to lower the field while also ensuring the test does not take several months to complete. One hypothesis to explain this transition is the existence of oil-filled cavities within the insulation. To confirm this, tests at another frequency, say 30 kHz, can be done to observe if it follows a similar trend. A detection mechanism can be used to PD occurrences below and above the transition point. These would lead towards a better understanding the underlying physics.

- The ageing trends under pulsed stresses does not seem to deviate significantly from sinuous stresses. This can be further explored by comparing sinuous and pulsed tests results at the same frequency, and then isolate only the effect of the harmonics on the ageing of the insulation. Also, effects of rise-times and overshoots can also be studied similarly.

Overall, the results from the experiments have opened the doors to new exciting pathways of research. These will be discussed further in Chapter 6.

6

CONCLUSIONS

There is always a vast field left to experimentation and I hope that we may have some beautiful progress in the following years.

MARIE CURIE
The Discovery of Radium (1921)

With the pulse generator, pulse transformer, and ageing experiments complete, the vast number of results need to be condensed in a meaningful manner to promote further exploration of this field. The subsequent sections of this chapter list the challenges faced in the project and the limitations they caused, provides the answers to the initial research questions and the accomplishments achieved in doing so, and finally plans the possible paths to take when directing future research.

6.1 SCIENTIFIC CHALLENGES AND LIMITATIONS

Attempting a project of this scale was bound to face challenges, and was also the reason for several of the various learning outcomes during the thesis. The main limitations can be grouped into the need for,

- **More resources**... for procuring a robust DC source and importantly, for building a resilient transformer. The available cores had a window size too small to allow producing larger voltages without causing flashovers or discharges. Each of these failures would then cause the switches/drivers to burn which would require time and effort to replace. This limited the possible voltage and frequency ranges that could be used in the experiments, and would have been solved with a larger core size.
- **More time**... for carrying out further ageing experiments. The existence of a transition point is an extremely interesting observation, one which could have been explored further at another frequency such as 30 kHz.

Despite these two limitations, the results provide an important proof-of-concept of the idea that building a modulator for dielectric testing can produce insightful outcomes. The limitations have also provided the author a chance to learn how to optimise and be resourceful with what is available.

6.2 RESEARCH ANSWERS AND ACCOMPLISHMENTS

The initial research questions are revisited here with their answers.

- *Are SiC MOSFETs a practical substitute to Si IGBTs in solid-state medium-voltage pulse-modulator applications?*

  The selection of SiCFETs in the project was due to an initial idea of having the primary voltage $V_p = 1000\ V$. Considering that the primary is now fed by the AC mains, the need for silicon carbide technology in the context of this modulator has diminished. Further, the cost of these switches is unsuitable for applications that are inherently used for breakdown testing. As an alternative, silicon IGBTs are far more rugged and possess similar switching performance. Si MOSFETs are capable of switching a few thousand volts (albeit with lower current ratings). An alternative selection of semiconductor switch in addition with TVS diodes for protection appears to be the best direction to work towards.

- *What are the critical pulse transformer design considerations when generating quasi-rectangular pulses across capacitive samples?*

  The PQR equation shows that the test elements R_t and C_t provide much needed breathing room when optimising the transformer parasitics. Slightly higher parasitics can be compensated by tuning the test elements to achieve desired results, although even higher parasitics reduce the fastest achievable rise-time. Apart from these, it is also important to carefully consider the tradeoffs and failure modes when designing the pulse transformer. Reducing the primary number of turns is crucial, but not at the cost of inducing core saturation. Spreading the primary to improve leakage is beneficial, but not at the cost of possible flashovers. Large current draws are to be expected when generating high frequency voltages. As such, developing pulse transformers has proven to require a shift in expertise from just high-voltage to also high-power.

- *How does the frequency of pulsed voltages accelerate the ageing processes in oil-impregnated paper?*

  The frequency of applied field stresses significantly decreases the lifetime of the insulation, although the underlying cause for this phenomenon is still unclear. Dielectric losses or partial discharges could be the most likely culprits, but this remains to be explored. What is clear, however, is that oil-impregnated paper in its current form is probably not suitable for MFT applications. Building MFTs for future SSTs would hence require some smart rethinking of methods to choose an apt insulation material.

6.3 FUTURE RESEARCH DIRECTIONS

The topic of pulsed ageing has two halves, similar to the structure of this thesis *viz.* the development of the pulse modulator, and the ageing trends obtained from pulsed experiments. For the modulator, the development of the pulse generator can be improved in terms of protection (such as with TVS diodes), switch selection (IGBTs or SiFETs), and minor improvements to the PCB (modular design, adding TVS diodes). It would be highly beneficial to design the pulse transformer with a larger core window allowing tests at even higher voltages and thereby lower frequencies. Further analysis of the PQR equation would certainly lead to better intuition of optimising the parasitics L_σ-C_d and test elements R_t-C_t. For the ageing trends, the results can be divided into pulse-related and frequency-related studies. The former involves comparing pulsed ageing with sinuous ageing to isolate the effect of harmonics, and understanding the effects of rise-time and pulse polarity. The latter involves identifying the ageing mechanism at higher frequencies and especially below the identified transition point. As a whole, this project has led to new research lines waiting to be explored which have been summarised in Fig. 6.1. This chapter, and hence this thesis, ends with the hope that its contents have inspired readers to carry on this work.

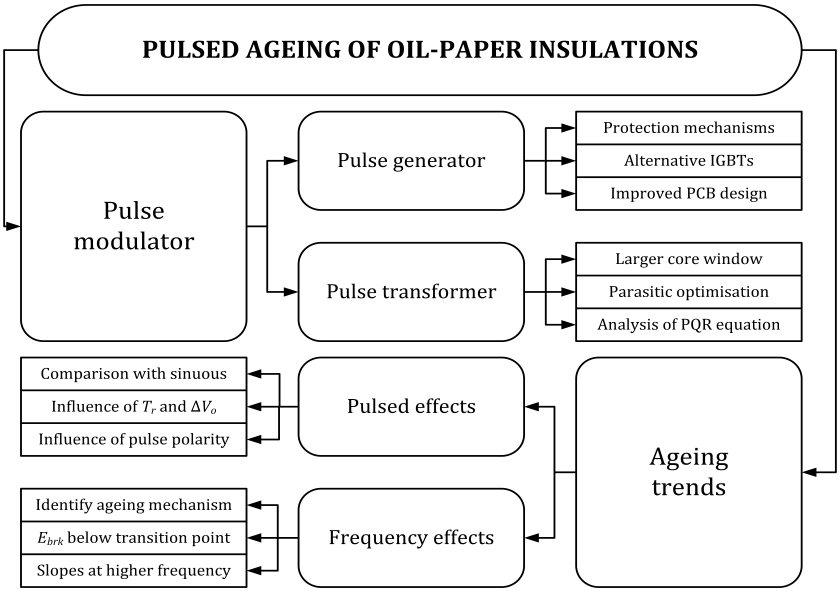


FIGURE 6.1: Overview of suggestions for future work

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A

APPENDIX

Here be dragons.

α: PLANNING AND PRACTICES FOR SUCCESSFUL PCB DESIGN

The most conventional method for connecting electrical circuits has been to use insulated wires. It is clear that such a technique would lead to untidy results for complex circuits of large sizes. The next alternative available is a general-purpose board (GPB), also called Veroboard or perfboard, which is a copper sheet drilled with holes with standard pitch. Components can be put in through the holes of the board and soldered from below in the required configuration. GPBs offer flexibility in circuit alteration and are a great way to test if a circuit functions as expected. Despite this, GPBs are prone to failures due to short-circuits and improper connections. Once the design is decided, the best option is to fabricate a printed circuit board (PCB). As the name suggests, these are boards with a circuit printed on them permanently with copper. The use of PCBs reduces the risk of errors and greatly enhances the reliability of the circuit. There exist several electronic design automation (EDA) software for designing PCBs such as EAGLE, Altium Designer, KiCad, and DipTrace. Although slightly different in their functionality and features, all of them have more or less a common workflow. This includes wiring the schematic, selecting the components, placing them optimally on the board, drawing copper traces, and exporting the design to a Gerber file which can then be sent to a PCB manufacturer. In this appendix, each of these steps are briefly discussed in the context of Altium Designer. It is highly recommended to learn the procedure with a simple circuit initially, and then move on to bigger projects. A six month educational licence can be acquired for Altium with a valid email ID.

Project file: Every project has four fundamental files *viz.* the schematic (.SchDoc), the schematic library (.SchLib), the PCB (.PcbDoc), and the PCB library (.PcbLib). It is good practice to make these new files after a new project is made. Apart from these, there are also the fabrication outputs which are sent to the PCB manufacturer. It is useful to ensure all project files are saved locally within the same folder (refrain from using the cloud).

Circuit schematic: The schematic can be thought of as a base blueprint for the PCB. It's design is hence considered to be the most important stage, since a well-planned schematic can save a significant amount of time in later stages. It is important to first decide on details such as the number of ground nets, voltage sources, and signals that are needed. In Altium Designer, new components can be added as a symbol to the Schematic Library. It is possible to use the same symbol multiple times in the same schematic, as long as each copy has a unique designator. For example, ten resistors can have the same symbol in the schematic sheet but will have to be designated *R*1-*R*2-... and so on. This can also be done automatically using the annotation tool. A useful tip is to keep the designators short in length to reduce the occupied space on the silk screen. Finally, ensure that a "Generic no ERC" parameter is connected to all floating ports in the circuit to prevent warning messages when carrying out an ERC.

Components and footprints: Every component symbol in the schematic library is linked to what is called a footprint. These contain information about the physical construction of the component, more importantly the location and direction of its pins. It is a common mistake to skip adding footprints, which in most cases wastes time due to error messages during PCB placement. Components can be either through-hole or surface-mounted devices (SMD). The latter can be chosen for signal resistors, tantalum/ceramic capacitors, and low-wattage diodes. It is good practice to keep all SMD packages in the standard 0805 size, or the 1206 if necessary. Through-hole packages such as TO-247 are popular for semiconductor switches, but the parasitic inductance of the leads must be considered. The manufacturer part search feature in Altium is useful for finding the footprints of selected components. If unavailable, they can also be found on the Digi-Key website. The footprints should be added to the PCB library. Additionally, 3D models can also be added in the form of .STEP files. These need to be placed onto the existing footprint with the "Place 3D body" feature.

PCB placement: After carefully completing the schematic sheet, the design can be switched over to the .PcbDoc file in Altium. All used footprints can be seen at the bottom right of the screen, and can be dragged/rotated around the board space. The best start is to plan a draft board size while in the Board Planning mode with the "Redefine Board Shape" feature. It should be checked that the units are set to "mm" when doing this. Curving the edges of the board promotes better handling, as does having a rectangular board shape. For components with considerable heights, it is helpful to check if there is enough surrounding area with the 3D view.

Layer management: Every PCB has at least two sides onto which traces can be printed *i.e.* the top and the bottom. On top of each of these copper layers is the solder mask and the silk screen. The solder mask is what gives PCBs their iconic green hue and is responsible for masking the non-solderable areas. The silk screen is where text such as designators and directions are printed. The copper layers are isolated by the substrate which is usually a fiberglass known as FR4. However it is also possible to have several sheets of copper in between (for a higher manufacturing cost) to get more printable area with the same board size. Copper traces on separate layers are better insulate from one another as compared to traces on the same layer. The name, thickness, material, and order of all PCB layers can be modified from the Layer Stack Manager in Altium Designer.

Traces, vias, pours: The physical connections on the PCB are made by making copper traces between elements. However two traces cannot intersect if they carry different signals (in some cases they must not come close to each other). In this case, one of the traces is routed to another layer of the PCB through a via such that it will not cross the other trace. To connect a large number of elements to the same potential, such as to a ground or power plane, polygon pours can be used.

β: TESTING RESILIENCE OF PLA AGAINST TRANSFORMER OIL

To check if mineral oil had any effects on the PLA plastic used for 3D printing, PLA samples were immersed in oil as shown in Fig. A.1. No damage was observed over a period of three months, concluding that no short-term corrosion can occur.

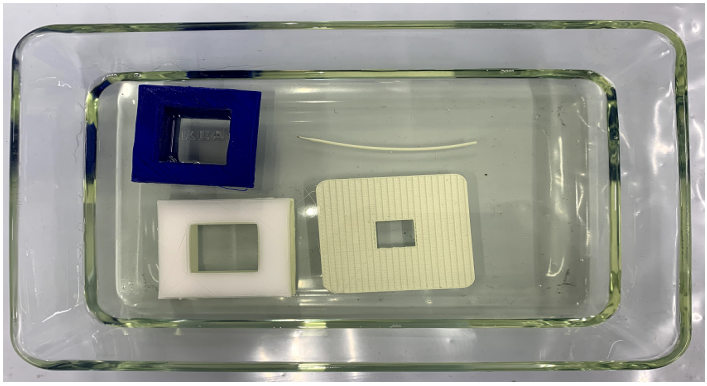
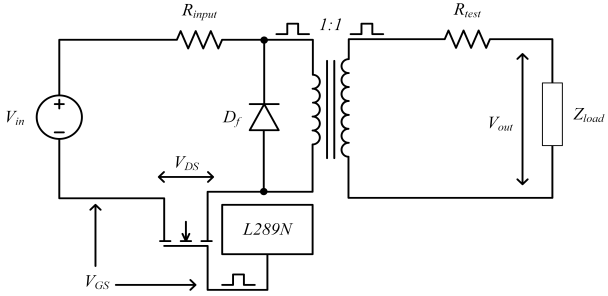


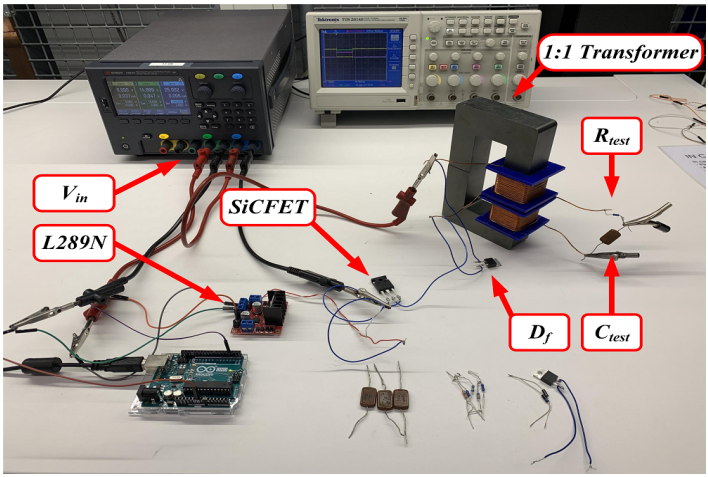
FIGURE A.1: Samples of PLA immersed in mineral oil

γ: PROTOTYPING AN INITIAL LOW-VOLTAGE PULSE MODULATOR

When designing the pulse modulator there exists two kinds of considerations *viz.* high-frequency considerations and high-voltage considerations. The latter are more geometrical in-nature (related to breakdown strengths, field enhancements, ...) and can be determined quite accurately with analytical formulas and general thumb rules. On the other hand, the high-frequency aspects are affected by a variety of factors such as stray resistances, leakage fluxes, and distributed capacitances. The purpose of the low-voltage prototype shown in Fig. A.2 is to decouple these aspects to analyse and optimise the frequency performance without any safety risks.



(a) Prototype circuit diagram of the prototype

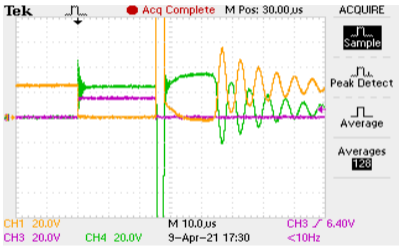


(b) Prototype experimental setup

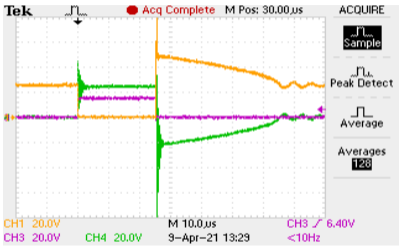
FIGURE A.2: Low-voltage pulse modulator prototype

Effect of free-wheel diode

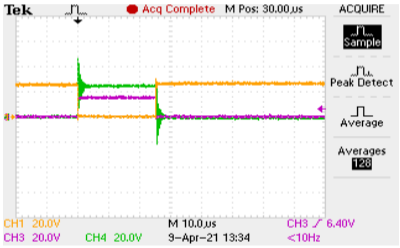
In this test, the elements R_{input}-R_{test}-Z_{load} are removed from the circuit, and the input V_{in} is set to 25 V. The diode D_f provides a de-energising path for the inductance of the transformer after every pulse cycle. In the absence of the free-wheeling diode the voltage across the secondary begins to oscillate out of control as shown in Fig. A.3a. Upon adding an Si-based diode, the oscillations are prevented and the output voltage takes some time to reach steady-state as shown in Fig. A.3b. If a SiC-based diode is used instead, this time is significantly improved producing an acceptable waveform as shown in Fig. A.3c. An interesting observation is that any diode in the secondary causes severe oscillations as shown in Fig. A.3d. This configuration is not practical either as the 10 kV secondary winding would require multiple SiC diodes to be placed in series which is expensive and inefficient.



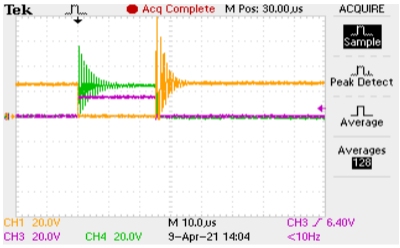
(a) Without free-wheel diode
V_{GS} : $Y = 20V/div$ $X = 10\mu s/div$
V_{DS} : $Y = 20V/div$ $X = 10\mu s/div$
V_{out} : $Y = 20V/div$ $X = 10\mu s/div$



(b) With Si-diode on primary
V_{GS} : $Y = 20V/div$ $X = 10\mu s/div$
V_{DS} : $Y = 20V/div$ $X = 10\mu s/div$
V_{out} : $Y = 20V/div$ $X = 10\mu s/div$



(c) With SiC-diode on primary
V_{GS} : $Y = 20V/div$ $X = 10\mu s/div$
V_{DS} : $Y = 20V/div$ $X = 10\mu s/div$
V_{out} : $Y = 20V/div$ $X = 10\mu s/div$

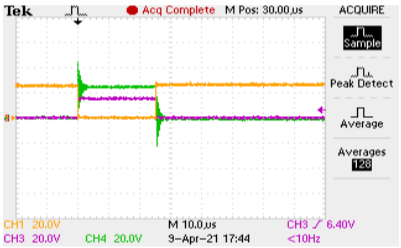


(d) With SiC-diode on secondary
V_{GS} : $Y = 20V/div$ $X = 10\mu s/div$
V_{DS} : $Y = 20V/div$ $X = 10\mu s/div$
V_{out} : $Y = 20V/div$ $X = 10\mu s/div$

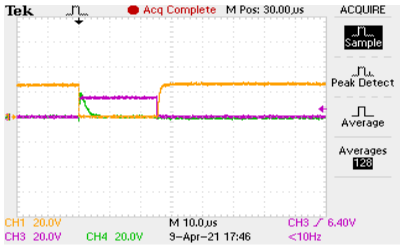
FIGURE A.3: Effect of D_f on V_{out} (green), V_{DS} (yellow), V_{GS} (magenta)

Effect of input resistance

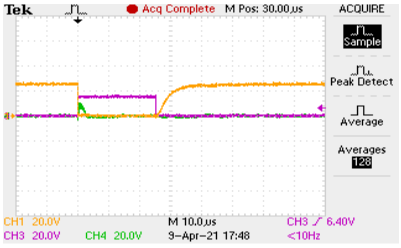
In this test, the elements R_{test}-Z_{load} are removed from the circuit, the D_f is a SiC-diode, and the input V_{in} is set to 25 V. The resistance R_{input} symbolises the inevitable copper resistance in copper wires connecting the transformer to the pulse driver. The increase in magnitude of R_{input} limits the magnetising current responsible for energising the transformer windings. A value of around 1 kΩ allows only for a small current as shown in Fig. A.4b, which is further reduced with values of 10 kΩ and 100 kΩ as shown in Fig. A.4c and Fig. A.4d, respectively. It can also be seen that this phenomenon affects the switching performance of the SiCFET. However these are extreme case scenarios since the connecting resistance can expected to be in the range of a few ohms to tens of ohms which produces an acceptable waveform as shown in Fig. A.4a. Nevertheless the R_{input} must be as small as possible.



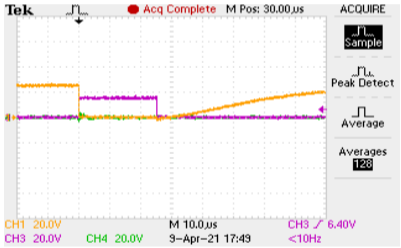
(a) With $R_{input} = 1\ \Omega$
$V_{GS}: Y = 20V/div\ X = 10\mu s/div$
$V_{DS}: Y = 20V/div\ X = 10\mu s/div$
$V_{out}: Y = 20V/div\ X = 10\mu s/div$



(b) With $R_{input} = 1\ k\Omega$
$V_{GS}: Y = 20V/div\ X = 10\mu s/div$
$V_{DS}: Y = 20V/div\ X = 10\mu s/div$
$V_{out}: Y = 20V/div\ X = 10\mu s/div$



(c) With $R_{input} = 10\ k\Omega$
$V_{GS}: Y = 20V/div\ X = 10\mu s/div$
$V_{DS}: Y = 20V/div\ X = 10\mu s/div$
$V_{out}: Y = 20V/div\ X = 10\mu s/div$

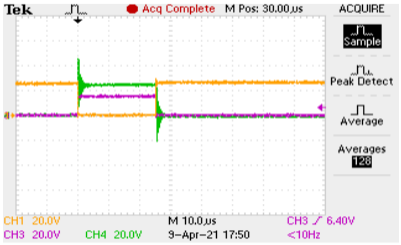


(d) With $R_{input} = 100\ k\Omega$
$V_{GS}: Y = 20V/div\ X = 10\mu s/div$
$V_{DS}: Y = 20V/div\ X = 10\mu s/div$
$V_{out}: Y = 20V/div\ X = 10\mu s/div$

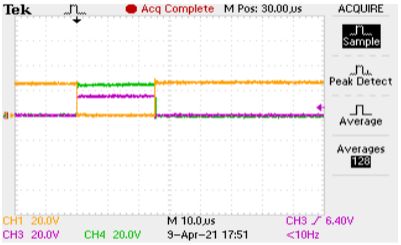
FIGURE A.4: Effect of R_{input} on V_{out} (green), V_{DS} (yellow), V_{GS} (magenta)

Effect of load under test

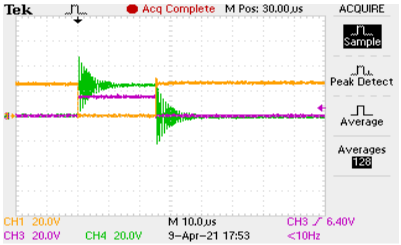
In this test, the elements R_{test}-R_{input} are removed from the circuit, the D_f is a SiC-diode, and the input V_{in} is set to 25 V. The load of transformer is a crucial factor that affects its output waveform. In open circuit, the transient oscillations are less as shown in Fig. A.5a. In klystron modulators, the load is purely resistive which helps in damping these oscillations as shown in Fig. A.5b. However capacitive loads such as cellulosic insulations amplify these oscillations causing severe ringing at the output as shown in Fig. A.5d. This test illustrates the challenge in building pulse modulators for non-resistive loads which essentially add to the parasitics of the high-frequency transformer. It is hence imperative to limit the capacitance of the test samples by controlling their thickness and radius. The C_{test} is expected to be maximally 100pF which would produce a waveform close to Fig. A.5c.



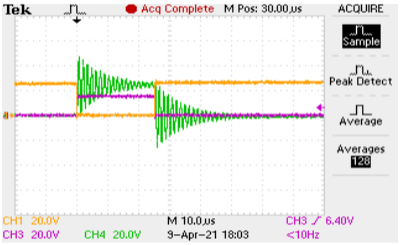
(a) With no connected load
V_{GS} : $Y = 20V/div$ $X = 10\mu s/div$
V_{DS} : $Y = 20V/div$ $X = 10\mu s/div$
V_{out} : $Y = 20V/div$ $X = 10\mu s/div$



(b) With load of 10 $k\Omega$
V_{GS} : $Y = 20V/div$ $X = 10\mu s/div$
V_{DS} : $Y = 20V/div$ $X = 10\mu s/div$
V_{out} : $Y = 20V/div$ $X = 10\mu s/div$



(c) With load of 82 pF
V_{GS} : $Y = 20V/div$ $X = 10\mu s/div$
V_{DS} : $Y = 20V/div$ $X = 10\mu s/div$
V_{out} : $Y = 20V/div$ $X = 10\mu s/div$

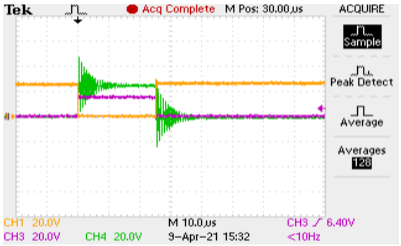


(d) With load of 330 pF
V_{GS} : $Y = 20V/div$ $X = 10\mu s/div$
V_{DS} : $Y = 20V/div$ $X = 10\mu s/div$
V_{out} : $Y = 20V/div$ $X = 10\mu s/div$

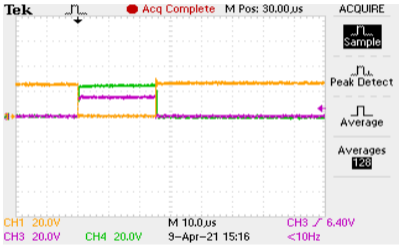
FIGURE A.5: Effect of Z_{load} on V_{out} (green), V_{DS} (yellow), V_{GS} (magenta)

Effect of output resistance

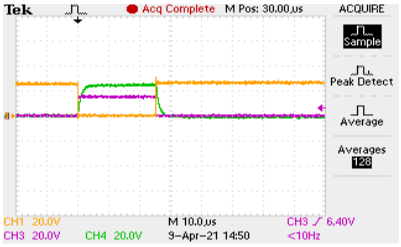
In this test, the element R_{input} is removed from the circuit, the D_f is a SiC-diode, the Z_{load} is an 82 pF capacitor, and the input V_{in} is set to 25 V. The output resistance R_{test} limits the current flow and reduces copper losses in the wires. A side-effect of this resistance is the damping of oscillations since the RC combination filters out the rapid transients present in the rise and fall of the pulse waveform. An R_{test} of 1 kΩ results in a cut-off frequency $F_c \approx 2$ MHz and produces the desirable waveform shown in Fig. A.6b. However an increase in R_{test} brings the F_c closer to the switching frequency causing slower rise and fall times, as shown in Fig. A.6c and Fig. A.6d. It is hence crucial to fine-tune the RC bandwidth to a value in the MHz range by varying the magnitudes of R_{test} and C_{test}. Additionally, a high power-rated R_{test} should be used in the high-voltage modulator.



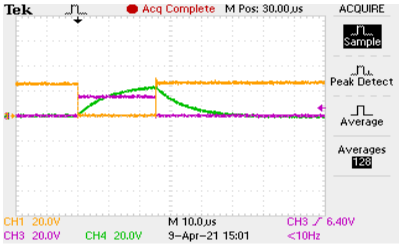
(a) With $R_{test} = 0\ \Omega$
$V_{GS}: Y = 20V/div\ X = 10\mu s/div$
$V_{DS}: Y = 20V/div\ X = 10\mu s/div$
$V_{out}: Y = 20V/div\ X = 10\mu s/div$



(b) With $R_{test} = 1\ k\Omega$ $F_c \approx 2$MHz
$V_{GS}: Y = 20V/div\ X = 10\mu s/div$
$V_{DS}: Y = 20V/div\ X = 10\mu s/div$
$V_{out}: Y = 20V/div\ X = 10\mu s/div$



(c) With $R_{test} = 10\ k\Omega$ $F_c \approx 0.2$MHz
$V_{GS}: Y = 20V/div\ X = 10\mu s/div$
$V_{DS}: Y = 20V/div\ X = 10\mu s/div$
$V_{out}: Y = 20V/div\ X = 10\mu s/div$

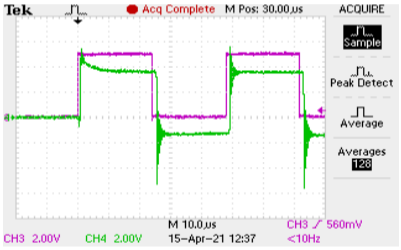


(d) With $R_{test} = 100\ k\Omega$ $F_c \approx 20$kHz
$V_{GS}: Y = 20V/div\ X = 10\mu s/div$
$V_{DS}: Y = 20V/div\ X = 10\mu s/div$
$V_{out}: Y = 20V/div\ X = 10\mu s/div$

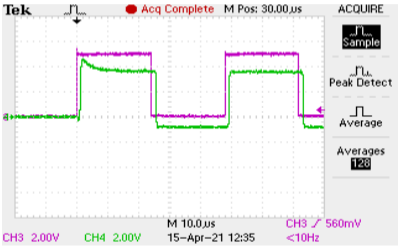
FIGURE A.6: Effect of R_{test} on V_{out} (green), V_{DS} (yellow), V_{GS} (magenta)

Effect of pulse polarity

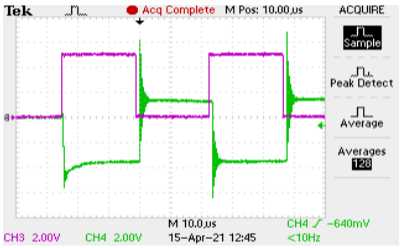
In this test, the transformer is fed directly from the L289N driver and the input V_{in} is set to 5 V. The left-column of Fig. A.7 is with D_f-R_{test}-Z_{load} removed, and the right-column are with these elements added.



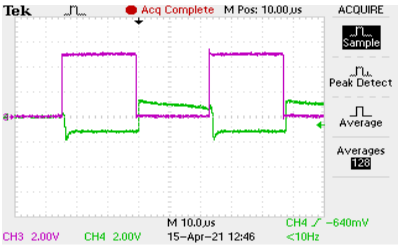
(a) Unipolar+ pulse output waveform
V_{GS} : $Y = 2V/div$ $X = 10\mu s/div$
V_{out} : $Y = 2V/div$ $X = 10\mu s/div$



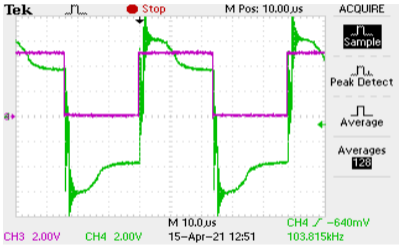
(b) Unipolar+ with D_f-R_{test}-Z_{load}
V_{GS} : $Y = 2V/div$ $X = 10\mu s/div$
V_{out} : $Y = 2V/div$ $X = 10\mu s/div$



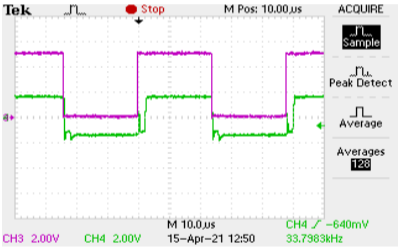
(c) Unipolar- pulse output waveform
V_{GS} : $Y = 2V/div$ $X = 10\mu s/div$
V_{out} : $Y = 2V/div$ $X = 10\mu s/div$



(d) Unipolar- with D_f-R_{test}-Z_{load}
V_{GS} : $Y = 2V/div$ $X = 10\mu s/div$
V_{out} : $Y = 2V/div$ $X = 10\mu s/div$



(e) Bipolar+- pulse output waveform
V_{GS} : $Y = 2V/div$ $X = 10\mu s/div$
V_{out} : $Y = 2V/div$ $X = 10\mu s/div$

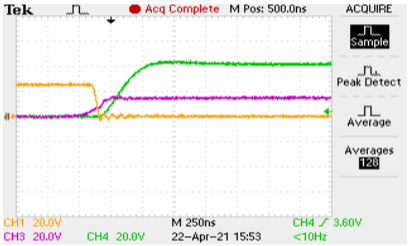


(f) Bipolar+- with D_f-R_{test}-Z_{load}
V_{GS} : $Y = 2V/div$ $X = 10\mu s/div$
V_{out} : $Y = 2V/div$ $X = 10\mu s/div$

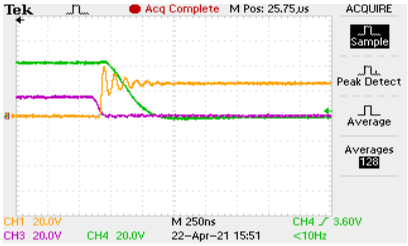
FIGURE A.7: Effect of pulse polarity on V_{out} (green) and V_{GS} (magenta)

Effect of turns ratio

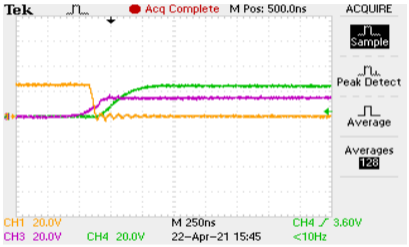
In this test, the element R_{input} is removed from the circuit, the D_f is a SiC-diode, the Z_{load} is an 82 pF capacitor, and the input V_{in} is set to 25 V. The turns ratio $N_p : N_s$ determines the output voltage magnitude and more importantly the slew rate experienced by the winding insulations on the secondary-side of the pulse transformer. A unity turns ratio results in a rising rate of 0.1 V/ns as shown in Fig. A.8c and a falling rate of 0.05 V/ns as shown in Fig. A.8d. A step-up turns ratio of 3:5 results in a rising rate of 0.16 V/ns as shown in Fig. A.8a and a falling rate of 0.08 V/ns as shown in Fig. A.8b. Since the rise times will remain fairly similar in the high-voltage modulator, it can hence be expected that a turns ratio of 1:30 would result in slew rates in the order of 30 V/ns to 60 V/ns. This is an important criteria to consider when designing the insulation of the secondary windings.



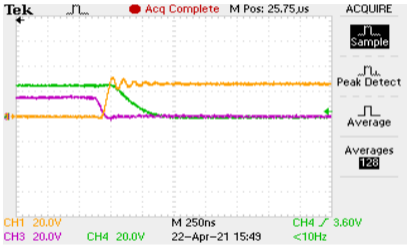
(a) With $N_p : N_s = 15 : 25 = 3 : 5$
V_{GS} : $Y = 20V/div$ $X = 250ns/div$
V_{DS} : $Y = 20V/div$ $X = 250ns/div$
V_{out} : $Y = 20V/div$ $X = 250ns/div$



(b) With $N_p : N_s = 15 : 25 = 3 : 5$
V_{GS} : $Y = 20V/div$ $X = 250ns/div$
V_{DS} : $Y = 20V/div$ $X = 250ns/div$
V_{out} : $Y = 20V/div$ $X = 250ns/div$



(c) With $N_p : N_s = 25 : 25 = 1 : 1$
V_{GS} : $Y = 20V/div$ $X = 250ns/div$
V_{DS} : $Y = 20V/div$ $X = 250ns/div$
V_{out} : $Y = 20V/div$ $X = 250ns/div$



(d) With $N_p : N_s = 25 : 25 = 1 : 1$
V_{GS} : $Y = 20V/div$ $X = 250ns/div$
V_{DS} : $Y = 20V/div$ $X = 250ns/div$
V_{out} : $Y = 20V/div$ $X = 250ns/div$

FIGURE A.8: Effect of turns ratio on V_{out} (green), V_{DS} (yellow), V_{GS} (magenta)

Effect of primary turns

In this test, the element R_{input} is removed from the circuit, the D_f is a SiC-diode, the Z_{load} is an 82 pF capacitor, and the input V_{in} is set to 10 V. The number of primary winding turns N_p and thereby its inductance L_p affects the primary magnetisation current I_p drawn from the source V_{in}.

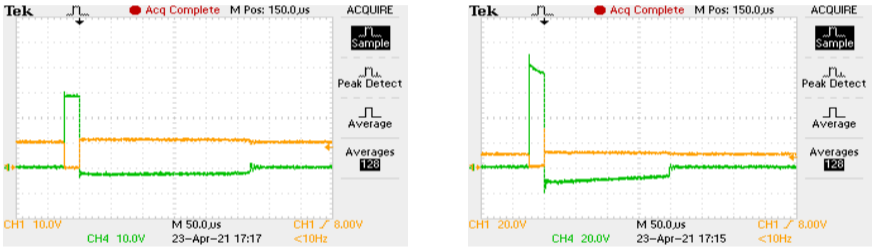
$$\downarrow L_p = \frac{\downarrow N^2 \times \mu_r \mu_o A}{l} \Rightarrow \downarrow X_L = \omega L_p \Rightarrow \uparrow I_p = \frac{V_{in}}{X_L} \tag{A.1}$$

While a reduced number of turns is favorable due to smaller parasitic capacitances, it also results in larger magnetising currents. During the OFF cycle, this current remains due to the inductance and causes a voltage drop across the equivalent series resistance (ESR) of the winding. This then produces a negative voltage on the secondary-side until the energy in the winding is removed, as seen in Fig. A.9a and A.9b. It is also interesting to observe the accordance of the results with the volt-second rule, which states that the net area under the graph of voltage applied across an inductor should be zero. As an example, these are calculated for $N_p = 8$ as,

$$A_{cycle+} = V_{cycle+} \times t_{cycle+} = 30 \text{ V} \times 25 \text{ µs} = 750 \text{ Vµs}$$

$$A_{cycle-} = V_{cycle-} \times t_{cycle-} = 2.5 \text{ V} \times 300 \text{ µs} = 750 \text{ Vµs}$$

A solution to this issue is to transmit bipolar pulses that "self-reset" the inductor and will decrease the current drawn by the winding. This is another reason for choosing bipolar pulses for the high-voltage modulator in this thesis, in addition to removing the need for an auxillary core-reset circuit. The next sub-section will further explore these results in simulation.



(a) With $N_p = 8$ and $N_s = 25$
V_{GS} : $Y = 10V/div$ $X = 50\mu s/div$
V_{out} : $Y = 10V/div$ $X = 50\mu s/div$

(b) With $N_p = 2$ and $N_s = 25$
V_{GS} : $Y = 20V/div$ $X = 50\mu s/div$
V_{out} : $Y = 20V/div$ $X = 50\mu s/div$

FIGURE A.9: Effect of primary turns on V_{out} (green) and V_{DS} (yellow)

Validation of results in LTspice

In this section, the results obtained in evaluation tests are validated in simulation with the LTspice model shown in Fig. A.10. A Keysight U1733C RLC meter was used to determine the open-circuit/short-circuit inductances of the primary/secondary at 1/10 kHz (Table A.1). The self-inductances L_p-L_s are set as the L_{oc} value in the LTspice model. Then the coupling coefficients K are computed with the expression,

$$K = \sqrt{1 - \frac{L_{sc}}{L_{oc}}} \tag{A.2}$$

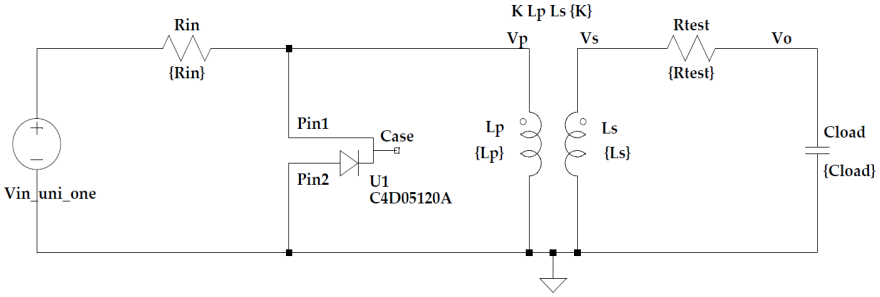
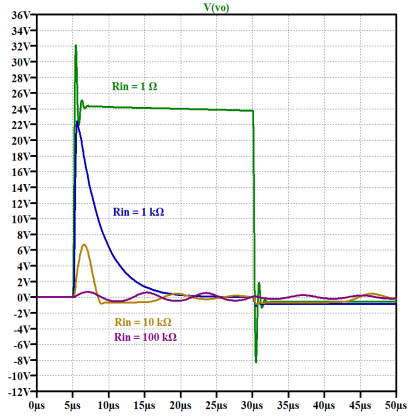


FIGURE A.10: Pulse modulator LTspice simulation model

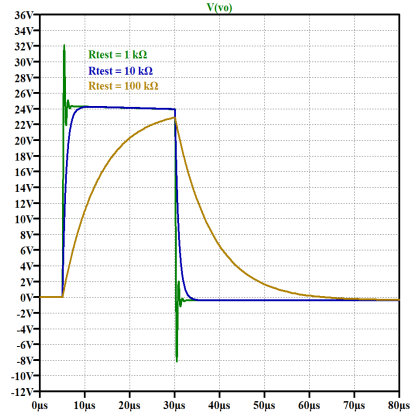
$N_p : N_s$	MEASURED FROM	$f_{setting}$	L_{oc}	L_{sc}	K
2:25	Primary	1kHz	47.46μH	4.06μH	0.95627
2:25	Primary	10kHz	46.91μH	4.03μH	0.95608
2:25	Secondary	1kHz	3.53mH	302.1μH	0.95625
2:25	Secondary	10kHz	3.51mH	288.9μH	0.95796
8:25	Primary	1kHz	423.9μH	35.73μH	0.95692
8:25	Primary	10kHz	420.9μH	35.58μH	0.95680
8:25	Secondary	1kHz	3.51mH	295.3μH	0.95701
8:25	Secondary	10kHz	3.49mH	293.6μH	0.95701
25:25	Primary/Secondary	1kHz	3.13mH	273.5μH	0.95531
25:25	Primary/Secondary	10kHz	3.12mH	272.5μH	0.95533

TABLE A.1: Obtained inductance values and calculated coupling coefficients

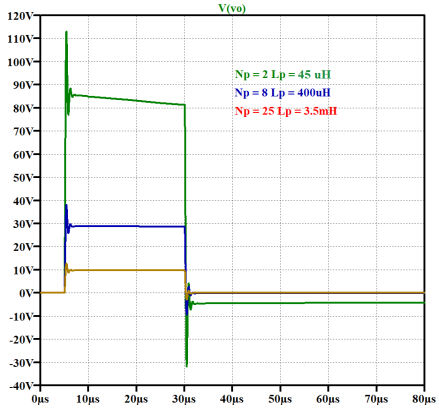
Three parametric sweeps for R_{in}-R_{test}-N_p were carried out in LTspice and the results shown in Fig. A.11. The sweep of R_{in} in Fig A.11a illustrates that higher input resistances limit the magnetising current and in-turn the output voltage. The sweep of R_{test} in Fig A.11b verifies the effect of fine-tuning the test resistance to filter high-frequency oscillations during rise-fall transitions. Finally the sweep of N_p in Fig A.11c confirms that lesser turns increases the reverse-current during the OFF cycle, which produces a voltage drop across the ESR of the winding that is observed at the secondary as a negative voltage. This was further validated by setting the R_p-R_s to zero, which does not cause any negative voltage on the secondary.

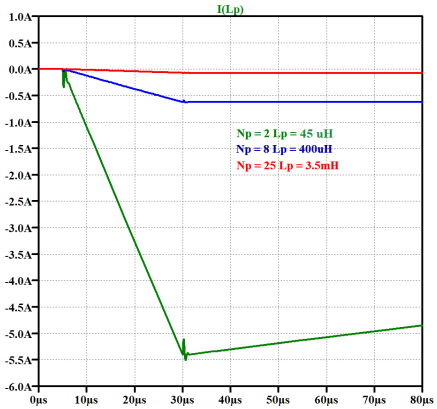


(a) Sweep of input resistance R_{in}



(b) Sweep of test resistance R_t





(c) Sweep of primary turns N_p

FIGURE A.11: Parametric sweeps in LTspice

Transmitting a bipolar waveform solves this issue since the polarity-reversal itself produces a de-energising current through the winding as shown in Fig A.12 (for $N_p = 2$). As mentioned earlier unipolar test voltages face several additional challenges such as the need for a reset circuit and higher magnetising currents, both of which are out of the scope of this thesis. Another key observation is that the overshoot seen in Ltspice is much larger than that observed in the hardware prototype. This is due to connection resistances that dampen the response, not accounted for in simulation.

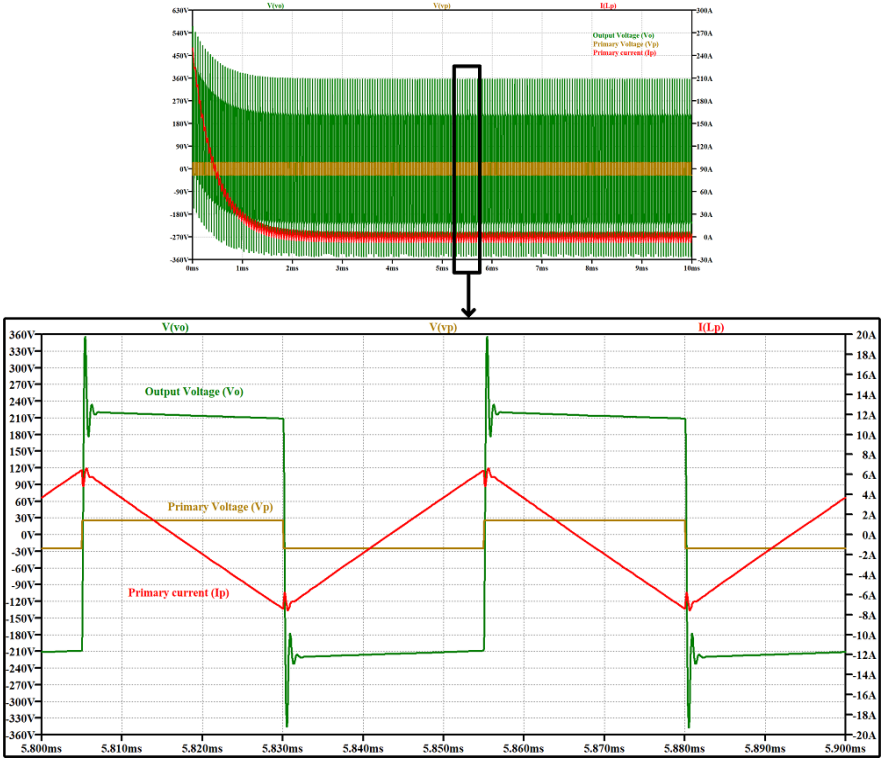


FIGURE A.12: Analysing the bipolar response in LTspice

Now that the high-frequency considerations of the pulse modulator have been studied, the next step is to construct the high-voltage modulator. This would require satisfying additional electric-field related constraints in the design to avoid any breakdowns in the winding insulation or bobbin, while also ensuring desirable output waveform characteristics. This is discussed in the sections of Chapter 4.

δ: DERIVING THE PQR MODULATOR EQUATION IN LAPLACE DOMAIN

The Laplace-domain expression of the PQR equation is derived below.

$$U_o = I_g(s) \times Z_{eq}(s) = \frac{U_g}{s} \times \frac{1}{(R_g + sL_\sigma)} \times Z_{eq}(s)$$

$$U_o = \frac{U_g}{s} \times \frac{1}{(R_g + sL_\sigma)} \times \frac{1}{\frac{1}{R_g + sL_\sigma} + sC_d + \frac{1}{R_t + sC_{eq}}}$$

$$U_o = \frac{U_g}{s} \times \frac{1}{(R_g + sL_\sigma)} \times \frac{(R_g + sL_\sigma)(1 + sR_tC_{eq})}{(1 + sR_tC_{eq}) + sC_d(R_g + sL_\sigma)(1 + sR_tC_{eq}) + sC_{eq}(R_g + sL_\sigma)}$$

$$U_o = \frac{U_g}{s} \times \frac{1}{\cancel{(R_g + sL_\sigma)}} \times \frac{\cancel{(R_g + sL_\sigma)}(1 + sR_tC_{eq})}{s^3(L_\sigma C_d R_t C_{eq}) + s^2(R_g R_t C_{eq} C_d + L_\sigma C_d + C_{eq} L_\sigma) + s\,(R_t C_{eq} + R_g C_d + R_g C_{eq}) + 1}$$

$$U_o = \frac{U_g}{s} \times \frac{(1 + sR_tC_{eq})}{L_\sigma C_d R_t C_{eq} \times \left[s^3 + s^2\left(\frac{R_g}{L_\sigma} + \frac{1}{R_tC_{eq}} + \frac{1}{R_tC_d}\right) + s\left(\frac{1}{L_\sigma C_d} + \frac{R_g}{L_\sigma R_t C_{eq}} + \frac{R_g}{L_\sigma R_t C_d}\right) + \frac{1}{L_\sigma C_d R_t C_{eq}} \right]}$$

$$U_o \xrightarrow[R_g = 0]{\text{assuming}} \frac{U_g}{s} \times \frac{1}{L_\sigma C_d R_t C_{eq}} \times \frac{(1 + sR_tC_{eq})}{\left[s^3 + s^2\left(\frac{\cancel{R_g}}{L_\sigma} + \frac{1}{R_tC_{eq}} + \frac{1}{R_tC_d}\right) + s\left(\frac{1}{L_\sigma C_d} + \frac{\cancel{R_g}}{L_\sigma R_t C_{eq}} + \frac{\cancel{R_g}}{L_\sigma R_t C_d}\right) + \frac{1}{L_\sigma C_d R_t C_{eq}} \right]}$$

$$\Rightarrow U_o = \frac{U_g}{s} \times \frac{(1 + sR_tC_{eq})}{L_\sigma C_d R_t C_{eq}} \times \frac{1}{\left[s^3 + s^2\left(\frac{1}{R_tC_{eq}} + \frac{1}{R_tC_d}\right) + s\left(\frac{1}{L_\sigma C_d}\right) + \frac{1}{L_\sigma C_d} \times \frac{1}{R_tC_{eq}} \right]}$$

$$U_o = \frac{U_g}{s} \times \left[\frac{1}{L_\sigma C_d R_t C_{eq}} + \frac{s\cancel{R_tC_{eq}}}{L_\sigma C_d \cancel{R_tC_{eq}}} \right] \times \frac{1}{\left[s^3 + s^2\left(\frac{1}{R_tC_{eq}} + \frac{1}{R_tC_d}\right) + s\left(\frac{1}{L_\sigma C_d}\right) + \frac{1}{L_\sigma C_d} \times \frac{1}{R_tC_{eq}} \right]}$$

$$U_o = \frac{U_g}{s} \times \frac{1}{L_\sigma C_d} \left[\frac{1}{R_tC_{eq}} + s \right] \times \frac{1}{\left[s^3 + s^2\left(\frac{1}{R_tC_{eq}} + \frac{1}{R_tC_d}\right) + s\left(\frac{1}{L_\sigma C_d}\right) + \frac{1}{L_\sigma C_d} \times \frac{1}{R_tC_{eq}} \right]}$$

$$\textit{Assigning: } P = \frac{1}{L_\sigma C_d},\ Q = \frac{1}{R_tC_{eq}},\ R = \frac{1}{R_tC_{eq}} + \frac{1}{R_tC_d} \qquad \textit{we arrive to...}$$

$$U_o = \frac{U_g}{s} \times P\,(Q + s) \times \frac{1}{s^3 + s^2R + sP + P \cdot Q}$$

ϵ: COMPUTING THIRD-ORDER TIME-DOMAIN SOLUTIONS IN MATLAB

MATLAB was used to solve the third-order *PQR* equation. The symbolic function was used to plot the output waveform for a given L_σ-C_d-R_t-C_t as shown in Fig. A.13 (a). Next, a script was written to determine the overshoot and rise-time from solutions as shown in Fig. A.13 (b).

```
% plot vector
tvec = 0:1e-8:2e-6;
% symbols
syms s t
% storage
final = zeros(length(Rt),length(tvec));

for i = 1:length(Rt)
    u = (Vg/s) * (P(i,1)*(1+Q(i,1))) * 1/(s^3 + R(i,1)*s^2 + P(i,1)*s + P(i,1)*Q(i,1));
    ut(t) = ilaplace(u);
    final(i,:) = vpa(ut(tvec));
    over(i,1) = max(final(i,:));
    plot(tvec,vpa(ut(tvec)),'LineWidth',2)
    hold on
end
```

(a) Symbolic function to plot output waveform for a given L_σ-C_d-R_t-C_t

```
for i = 1:length(P_range)
    tic
    for j = 1:length(Q_range)

        % define R param
        R = Q_range(i,1) + R_del;

        % define laplace
        u = 1/s * P_range(j,1)*(s+Q_range(i,1)) * 1/(s^3 + s^2*R + s*P_range(j,1) + P_range(j,1)*Q_range(i,1));

        % laplace -> time
        ut(t) = ilaplace(u);

        store solution
        utsols(i,j) = vpa(ut(tvec));

        % acquire overshoot
        overshoot(i,j) = abs(max(vpa(ut(tvec))));

        acquire rise-time
        buffer = find(utsol>0.95);
        risetime(i,j) = buffer(1);

        % computation progress
        ((i-1)*length(P_range)+j)/length(P_range)/length(Q_range)/100;
    end
    toc
end
```

(b) Script to compute time-domain solutions and determine overshoot and rise-time

FIGURE A.13: Computing and plotting solutions to the *PQR* equation in MATLAB