# Highly Efficient Dual-Side Wireless Power Transfer:

## Implementation of Synchronization and Wireless Communication

ET4300: Master Thesis

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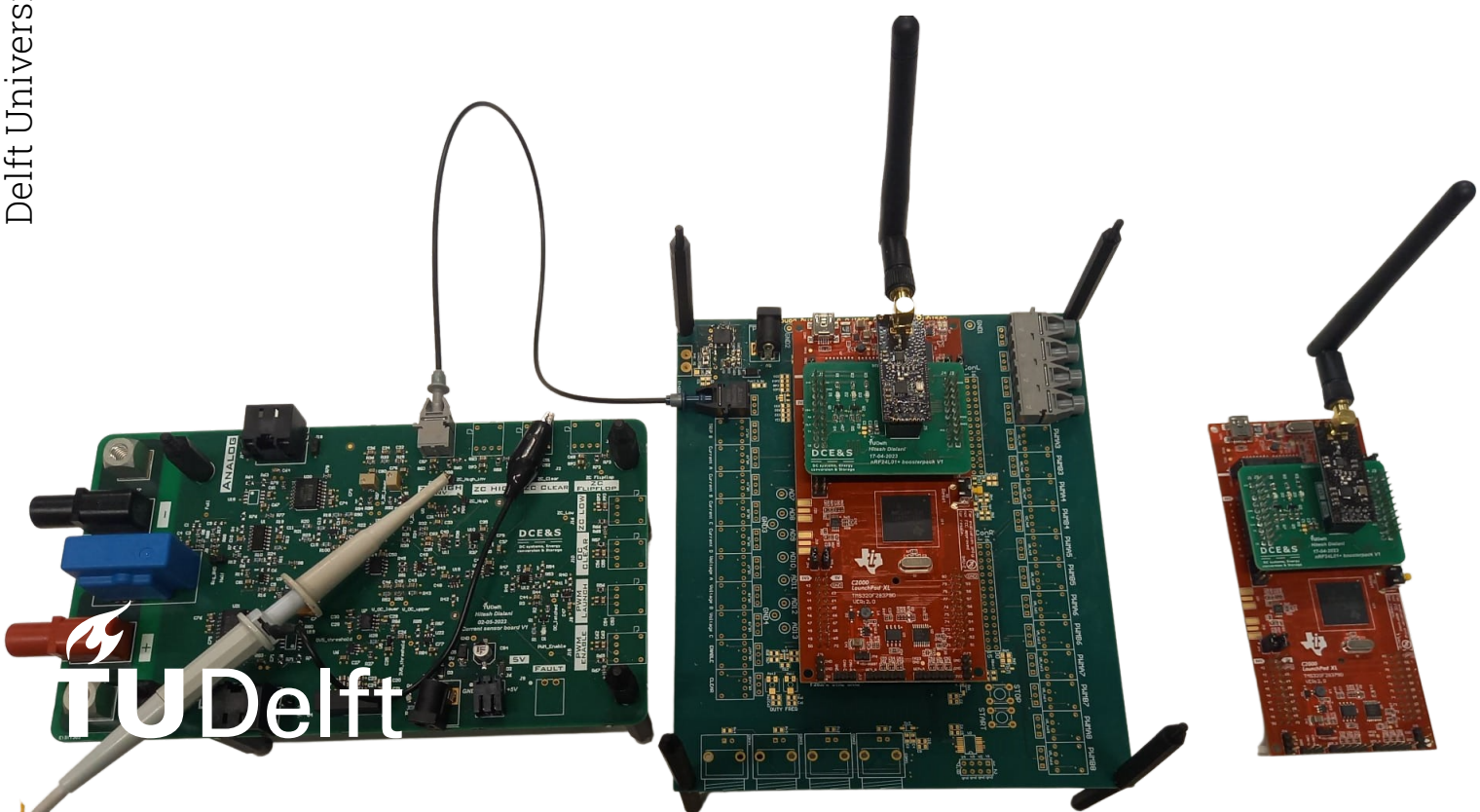
Delft University of Technology




TU Delft

# Highly Efficient Dual-Side Wireless Power Transfer:

## Implementation of Synchronization and Wireless Communication

by

H.Dialani

to obtain the degree of Master of Science
at the Delft University of Technology,
to be defended publicly on Wednesday July 26, 2023 at 9:00 AM.

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*Hitesh Dialani*
*Delft, July 2023*

# Abstract

*This thesis presents a practical topology for achieving highly efficient dual-side wireless power transfer (WPT). Traditional WPT systems with a diode rectifier on the secondary side lack flexibility in load matching, requiring the integration of an additional dc/dc converter at the back end. However, this approach leads to increased power losses and costs. In contrast, this thesis proposes the use of an active rectifier comprising MOSFETs, replacing the diode rectifier. By employing a dual active bridge topology with dual-side control, optimal load tracking is achieved by tuning one side and communicating the desired duty cycle or phase angle to the other side. To address practical challenges, two key aspects are considered. Firstly, synchronization is established between the generated current on the secondary side and the new active rectifier, enabling efficient load tracking and the potential for zero voltage switching (ZVS). This is accomplished using a printed circuit board (PCB) equipped with zero current crossing detection (ZCCD), validated with an $85kHz$ test signal. The PCB triggers the PWM output of the secondary side microcontroller with a latency of less than $< 50ns$, utilizing the trip-zone digital compare sub-block integrated into the TMS320F28379D. Secondly, seamless wireless communication between the primary and secondary sides is essential. While the secondary side can measure the current and voltage across the load to adjust its duty cycle for optimal conditions, the primary side lacks this information. Therefore, the secondary side transmits the new duty cycle to the primary side to ensure consistent power flow. The nRF24L01+ wifi module is utilized as a dual-purpose transmitter and receiver for achieving wireless communication. Validation of this wireless communication is performed by remotely controlling an external LED, connected to the receiver side, from a distance of approximately $5m$.accurately to the transmitted values. Additionally, a mathematical modeling approach is used to optimize power delivery and mitigate high-frequency noise by incorporating two parallel MLCC capacitors on a custom PCB near the nRF24L01+ module.*

# Contents

# 1 Introduction

This chapter states the problem definition and goals of this thesis.

## 1.1. Background

Significant progress has been made in wireless power transfer (WPT) over the past few decades, with a specific focus on inductive power transfer (IPT). While the terms WPT and IPT are presented, it is important to note that they refer to the same concept and are used interchangeably. IPT has brought about revolutionary advancements in various battery charging scenarios. Notable examples of IPT applications include medical implants [33], robotics [13], and smartphones [21]. By utilizing IPT technology, these devices benefit from the convenience and flexibility of wireless charging. Moreover, the versatility of this technology extends beyond power distribution in automation systems to the dynamic charging of electric vehicles (EVs).

The increasing energy demand, coupled with the depletion of fossil fuels and the resulting environmental pollution, presents one of the most significant challenges faced by modern society. Consequently, there is an urgent need to shift towards a renewable transport and energy system. Electric vehicles play a pivotal role in this transition, offering a sustainable solution.

In the realm of electric transportation, inductive power transfer (IPT) systems have emerged as a crucial solution, providing secure, hands-free, and efficient charging options for electric vehicles (EVs) as shown in Figure 1.1. With the soaring popularity of EVs and the prioritization of user convenience, wireless power transfer (WPT) has experienced remarkable growth as a viable charging solution.

Furthermore, the ability to charge vehicles dynamically while they are in motion has opened up new possibilities in transportation systems, enhancing their range and flexibility.

**Figure 1.1:** Inductive charging for EV [25].

The fundamental principle behind IPT involves two magnetically coupled coils: the transmitter coil, energized by an alternating current, generates an alternating magnetic field. This magnetic field links with the secondary coil, inducing a voltage according to Faraday's and Ampere's laws, which govern electromagnetic induction. The induced voltage can then power an electric load connected to the secondary coil [11]. In the context of EV wireless charging, the batteries play a significant role as loads in the IPT system.

## 1.2. Problem definition

Given the diverse battery profiles observed during the charging process as shown in Figure 1.2, achieving precise power flow control across a wide operating range becomes crucial for IPT systems [40]. Optimal load tracking has emerged as a critical performance indicator in IPT system design, aiming to maximize efficiency[15], [41].

Traditionally, the IPT system relies on diodes on the rectifier side. The use of diodes is preferred due to their simplicity, as they do not require a controller and are inherently passive. However, this simplicity comes at the cost of lower efficiency, as diodes alone are unable to implement optimal load matching.

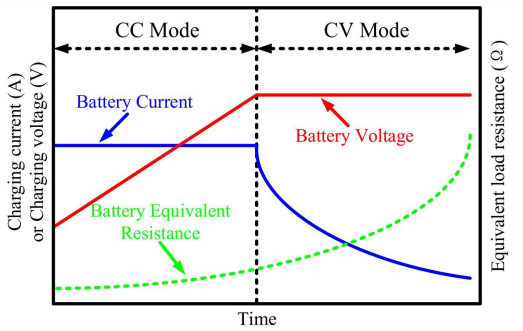



**Figure 1.2:** Typical charging profile of EV battery [9].

The implementation of a dual active bridge topology with dual-side control, as proposed in [44], enables optimal load tracking through independent duty cycle tuning using active rectifiers with MOSFETs. Dual-side control also allows for controlling the phase angle between current and voltage, facilitating zero voltage switching (ZVS) for increased system efficiency. However, the use of separate controllers for isolation between the primary and secondary sides presents two challenges that need to be addressed for practical applicability.

Effective synchronization between the generated current on the secondary side and the new active rectifier is crucial for optimal performance in the dual-active bridge topology with dual-side control.

In addition to synchronization, seamless communication between the primary and secondary sides plays a vital role in optimizing the overall performance of the system. This aspect primarily focuses on power flow control. While the secondary side has access to crucial parameters such as the load current and voltage, allowing it to adjust its duty cycle for optimal load conditions, the primary side lacks direct access to this information. Therefore, it becomes imperative for the secondary side to transmit the updated duty cycle to the primary side, ensuring consistent power flow between both sides. This seamless communication enables coordinated control and real-time adjustments, enabling efficient operation under varying load conditions. By enabling reliable and efficient power transfer, the communication between the primary and secondary sides plays a crucial role in maintaining overall system performance and stability

## 1.3. Research questions

- Why is it possible for an active rectifier to achieve optimal load matching with non-optimal loads, while a diode-based rectifier cannot?
- What are effective strategies for designing synchronization to minimize latency?
- What are the key factors to consider when designing wireless communication systems to improve reliability?

## 1.4. Thesis and scope

This thesis focuses on mathematically showing why an active rectifier can achieve load matching with non-optimal loads while diode rectifiers cannot. It also addresses hardware and software aspects to overcome synchronization and communication challenges, providing a comprehensive understanding of the design decisions made to achieve optimal load tracking and reliable wireless communication in the dual-side wireless power transfer system.

## 1.5. Layout of the thesis

This thesis is organized as followed:

- Chapter 2, provides a mathematical analysis of the principles underlying inductive power transfer (IPT). It begins by explaining the fundamentals of IPT and then proceeds to develop the traditional circuit configuration for IPT. Through mathematical analysis, it demonstrates why the traditional circuit configuration using a diode rectifier is unable to achieve optimal load matching.
- Chapter 3, is dedicated to the implementation of the dual-side topology in inductive power transfer (IPT). It highlights the capability of this topology to achieve optimal load matching, even in the presence of non-optimal loads, thus ensuring efficient power transfer. The chapter further investigates the integration of ZVS and power flow control techniques within the dual-side topology. Practical experiments and validations are carried out to provide empirical evidence of the effectiveness of ZVS and power flow control in a real-world IPT system.
- Chapter 4, focuses on the design and rationale behind synchronization.
- Chapter 5, explores the implementation of wireless communication and also how to improve stability during transmissions.
- Finally, Chapter 6, concludes the thesis and provides recommendations for future improvements.

# 2

# Fundamental of inductive power transfer (IPT) system

This chapter presents a mathematical analysis of the challenges associated with optimal load matching in fundamental inductive power transfer (IPT). It begins by examining the working principles of coils, followed by an expansion into the incorporation of power electronics.

## 2.1. The physics behind IPT

The physics underlying IPT relies on the fundamental principles of Maxwell's laws. Specifically, Ampere's Law governs the behavior on the primary side, while Faraday's Law governs the secondary side. These laws are essential in facilitating power transfer through the utilization of inductive coils, as depicted in Figure 2.1.

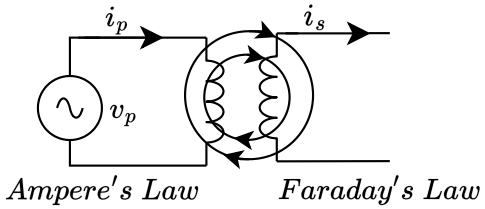



**Figure 2.1:** Illustration of Ampere's and Faraday's law being used in IPT.

### 2.1.1. Primary side utilizing Ampere's law

When an electric current passes through a conductor, it generates a magnetic field that surrounds the conductor, as depicted by the circles between the inductors in Figure 2.1. This relationship is mathematically described by Ampere's law, given by Equation (2.1). According to Ampere's law, the line integral of the magnetic field (B) along a closed loop (C) is equal to the surface integral of the current density (J) over an enclosed surface (S), divided by the permeability of free space (μ0).

$$\frac{1}{\mu_0} \oint_C \mathbf{B} \cdot \mathrm{d}\boldsymbol{l} = \iint_S \mathbf{J} \cdot \mathrm{d}\mathbf{S} \tag{2.1}$$

### 2.1.2. Secondary side utilizing Faraday's law

When a conductor is exposed to a time-varying magnetic field, it experiences the phenomenon of electromagnetic induction, resulting in the generation of an induced voltage. This is the reason why an alternating source (AC) is required at the primary side of the IPT system. The integral representation of Faraday's Law, depicted in Equation (2.2), illustrates this relationship. In Faraday's law, the electric field (E) is directly influenced by the rate of change of magnetic flux over time

$$\oint_C \mathbf{E} \cdot \mathrm{d}\boldsymbol{\ell} = -\frac{\mathrm{d}}{\mathrm{d}t} \iint_S \mathbf{B} \cdot \mathrm{d}\mathbf{S} \tag{2.2}$$

### 2.1.3. Magnetic coupling between primary and secondary side

Figure 2.1 provides a conceptual understanding of IPT, it is important to acknowledge that not all of the magnetic flux produced remains confined between the inductors in practice. A more realistic model is depicted in Figure 2.2(a). The author uses the phasor domain instead of the time domain in Figure 2.2(b), this transition will be highlighted later in the chapter. The magnetic flux that does not contribute to the coupling of the primary and secondary coils is referred to as leakage flux, represented by $\phi_{LKP}$ and $\phi_{LKS}$. To quantify the degree of coupling, the coupling coefficient $k$ is used, as shown in Equation (2.3). A coupling coefficient of $k = 1$ indicates that all the flux generated by the primary coil encircles the secondary coil, while a coupling coefficient of $k = 0$ indicates no coupling between the coils.

$$M = k\sqrt{L_p L_s} \tag{2.3}$$

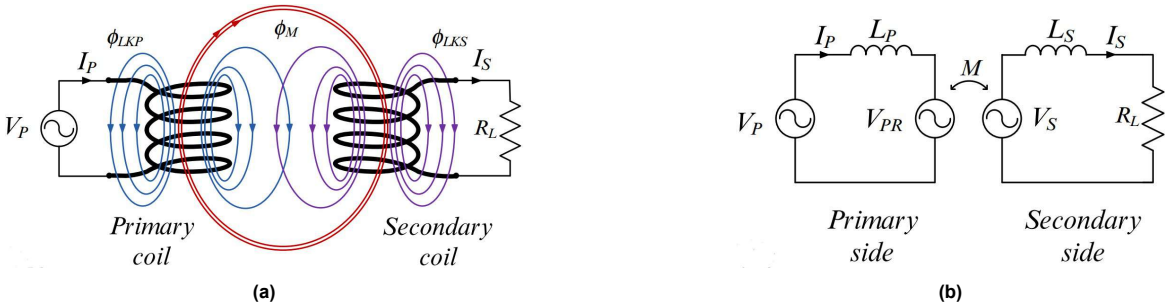



**Figure 2.2:** (a) Physical representation of IPT, and (b) circuit representation [3].

To grasp the level of mutual coupling between the primary and secondary sides, consider the direction of the current and the relative orientation of the coils. This dependency on orientation is visualized in Figure 2.2(a). If either of the inductors were rotated by 180 degrees, the mutual flux ($\phi_M$) would decrease, resulting in a reduced level of coupling between the two systems. In circuit representation, this relationship is denoted by a dot placed at one end of each magnetically coupled coil, indicating the direction of flux when current enters the dotted terminal. The commonly used circuit representation for IPT is depicted in Figure 2.3 [10], which will also be used for the remainder of this thesis.

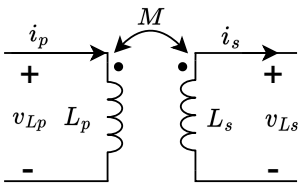



**Figure 2.3:** Time domain representation of general dot convention used for IPT.

The model shown in Figure 2.3 can be modeled using Equation (2.4)[4], here $v_{Lp}$ and $v_{Ls}$ represents the voltage over their respected coil.

$$\begin{bmatrix} v_{Lp} \\ v_{Ls} \end{bmatrix} = \begin{bmatrix} L_p & -M \\ M & -L_s \end{bmatrix} \cdot \frac{d}{dt} \begin{bmatrix} i_p \\ i_s \end{bmatrix} \tag{2.4}$$

## 2.2. Uncompensated IPT system

Now that an understanding of the physics behind IPT has been established, the relationship between the primary-side source and secondary-side load will be explored. This will be done by using an expanded model of Figure 2.3. To ensure a more realistic depiction, the model incorporates the parasitic

resistances of the inductors, denoted as $R_p$ and $R_s$. The resulting equivalent circuit is shown in Figure 2.4.

Certain assumptions will be made to simplify calculations and equations. These assumptions include considering the wires are ideal, assuming a purely resistive load, maintaining constant resistance and inductance in the circuit, and neglecting the skin effect. While these simplifications facilitate easier calculations, it is necessary to recognize that they will impact the accuracy of the results. These assumptions will be used for all models in this thesis.

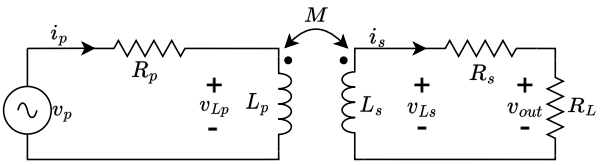



**Figure 2.4:** Time domain representation of the transformer equivalent model for an uncompensated IPT system.

It is important to gain an understanding of the flow of electromagnetic power within a system. This concept will be explained here. The flow of electromagnetic power can be effectively described by utilizing Poynting's Theorem. Poynting's Theorem, illustrated in Equation (2.5), establishes a fundamental principle: the power supplied by sources within a specified volume must be balanced by the power leaving the region, the power dissipated as heat, and the rate of change in stored electric and magnetic energy. For the IPT system, the specified volume encompasses the entire medium extending from the source to the load.

$$\underbrace{\iint_S (\boldsymbol{E}\times\boldsymbol{H})\cdot \mathrm{d}\boldsymbol{S}}_{\text{Instantaneous power leaving volume}} + \underbrace{\iiint_V \left(\boldsymbol{E}\cdot\frac{\partial \boldsymbol{D}}{\partial t}+\boldsymbol{H}\cdot\frac{\partial \boldsymbol{B}}{\partial t}\right)\mathrm{d}V}_{\text{Change of energy stored in the fields inside the volume}} + \underbrace{\iiint_V \boldsymbol{E}\cdot\boldsymbol{J}\mathrm{d}V}_{\text{Ohmic loss}} = \underbrace{-\iiint_V \boldsymbol{E}\cdot\boldsymbol{J}^{\text{ext}}\,\mathrm{d}V}_{\text{Electrical power from source}} \tag{2.5}$$

Understanding the ohmic loss in the system is relatively straightforward. The power leaving the system is used for charging batteries. However, in the case of an uncompensated IPT system, the energy stored in the fields becomes the most crucial aspect. Since power is transferred through an inductive medium, it is essential to determine whether the power provided by the source effectively reaches the load or if it gets stored in unwanted magnetic fields.

While Poynting's Theorem can be utilized for this purpose, it can be quite complex. Therefore, a simpler approach will be employed by examining the power factor (PF) of the system. The PF represents the ratio between real power and apparent power. The apparent power corresponds to the stored electric and magnetic power. A higher PF indicates that more power is being delivered to the load, whereas a lower power factor suggests that more power is being stored in the system instead.

The upcoming subsection will delve into the process of determining the power factor for an uncompensated IPT system.

### 2.2.1. Power Factor for uncompensated IPT system

The concept PF is captured by the general equation presented in Equation (2.6). The relationship between real power and apparent power is depicted in Figure 2.5(a). However, in the case of the complicated circuit shown in Figure 2.4, determining the real power (P) and apparent power (S) directly can give a complicated expression. To overcome this complexity, an alternative approach is employed.

By dividing all the quantities in Figure 2.5 by $I^2$, the impedance triangle is obtained, as shown in Figure 2.5(b). This allows for a simpler expression of power factor, as demonstrated in Equation (2.7). The advantage of this approach lies in its ability to provide a more straightforward calculation of PF.

$$\mathrm{PF} = \frac{\text{Real power}}{\text{Apparent power}} = \frac{P}{\sqrt{\mathrm{P}^2+\mathrm{Q}^2}} \tag{2.6}$$

$$\mathrm{PF} = \frac{\text{Resistance}}{\text{Impedance}} = \frac{\mathrm{R}}{\sqrt{\mathrm{R}^2+\mathrm{X}^2}} \tag{2.7}$$


**Figure 2.5:** AC circuit:(a) power triangle, and (b) impedance triangle.

A more simplified approach for PF can be achieved by expressing it solely in terms of the real and imaginary components of impedance ($Z$), rather than considering resistance ($R$) and reactance ($X$) separately. In this case, determining the suitable $Z$ value is straightforward, as it is determined by the voltage source $v_p$ and the secondary-side current $i_s$. More specifically, the input impedance ($Z_{in}$), representing the ratio between them, can be utilized for this purpose.

To calculate $Z_{in}$, a switch to the phasor domain representation of Figure 2.4 is necessary. The updated model is presented in Figure 2.6. Now $Z_{in}$ can be expressed as:

$$Z_{in} = \frac{V_p}{I_s} \tag{2.8}$$

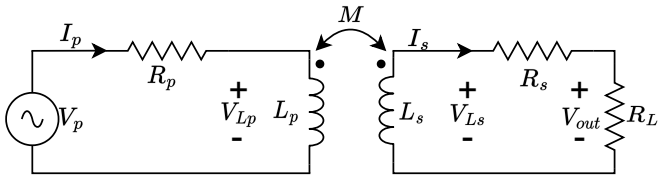



**Figure 2.6:** Phasor domain representation of the transformer equivalent model for an uncompensated IPT system.

Moving forward, the phasor domain representation will be consistently employed throughout this chapter, but will not be explicitly mentioned. Now that there is a way to express $Z_{in}$, the PF can be calculated using Equation (2.9).

$$\text{PF} = \frac{\mathfrak{Re}\left(Z_{in}\right)}{\sqrt{\mathfrak{Re}\left(Z_{in}\right)^2 + \mathfrak{Im}\left(Z_{in}\right)^2}} \tag{2.9}$$

Where $Z_{in}$ of the system is:

$$Z_{in} = R_p + j\omega L_p + \frac{(\omega M)^2}{j\omega L_s + R_s + R_L} \tag{2.10}$$

To determine $Z_{in}$, please refer to Appendix A.1 for detailed calculations. While parameters such as $L_p$, $L_s$, $R_p$, $R_s$, $R_L$, and $k$ can vary even during operation, the primary focus when examining PF lies in the variation of frequency ($f$). Therefore, considering $f$ as the sole independent variable is sufficient for studying PF. The plot illustrating the relationship between PF and frequency is presented in Figure 2.7, and the corresponding code can be found in Appendix B.1. The parameter values used in this analysis are listed in Table 2.1 [44].

Figure 2.7 demonstrates the expected relationship between PF and $f$, where decreasing $f$ results in a higher PF. This correlation can be attributed to the increased prominence of the parasitic resistance in the coils as $f$ decreases, leading to a reduced magnetic field. The relationship between $f$ and PF has also been observed in prior studies [10]. Although achieving a low $f$ is desirable for improved PF, it necessitates larger and costlier coils. Fortunately, there is a solution to enhance PF at higher frequencies: the incorporation of capacitors. By introducing capacitors, the imaginary component of $Z_{in}$ is reduced, resulting in an increased PF [10]. This modification transforms the system into a compensated IPT system topology, which will be explored further in the upcoming section.

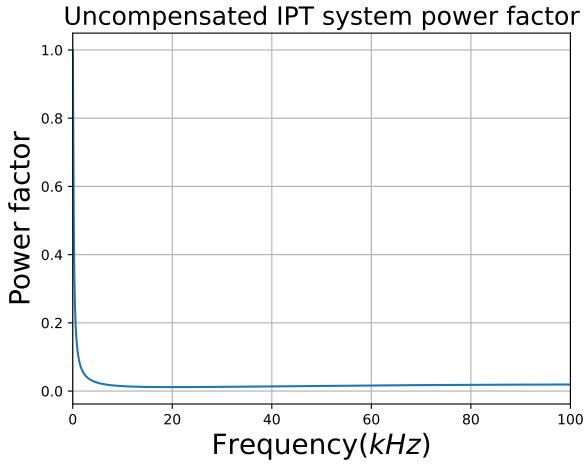



**Figure 2.7:** Power factor as a function of frequency for an uncompensated IPT system.

**Table 2.1:** System parameters used for simulations of Figure 2.7 [44].

| Symbol | Parameter | Values | Unit |
|---|---|---|---|
| $L_p$ | Primary coil inductance | 293.8 | $uH$ |
| $L_s$ | Secondary coil inductance | 198.8 | $uH$ |
| $M$ | Mutual inductance | 46 | $uH$ |
| $R_p$ | Primary coil parasitic resistance | 0.21 | $\Omega$ |
| $R_s$ | Secondary coil parasitic resistance | 0.14 | $\Omega$ |
| $R_L$ | Load resistance | 150 | $\Omega$ |

## 2.3. Compensated IPT system topologies

There are different compensation capacitors topology and they are all shown in Figure 2.8. These topologies are Series-Series (S-S), Parallel-Series (P-S), Series-Parallel (S-P), and Parallel-Parallel (P-P). To achieve the resonating effect between the capacitor and inductor for P-S and P-P configurations, a current source is required at the input.

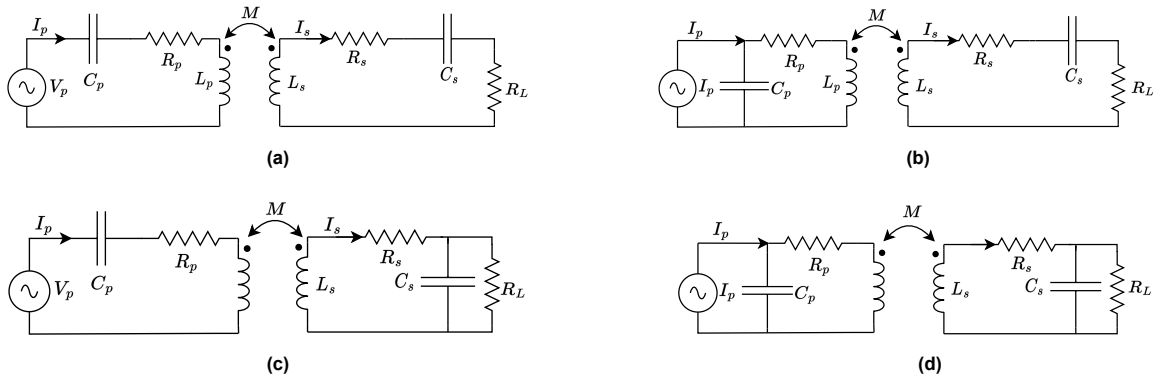



**Figure 2.8:** Four possible compensation capacitor configuration topologies for an IPT system. These configurations are: (a) Series-Series (S-S), (b) Parallel-Series (P-S), (c) Series-Parallel (S-P), and (d) Parallel-Parallel (P-P).

### 2.3.1. Power Factor for different compensation topologies

When selecting the most suitable topology for IPT, several criteria should be taken into account. One crucial consideration is to ensure a consistently high PF at high frequency. To achieve this, it is desirable to minimize the dependence of the compensation capacitors $C_p$ and $C_s$ on variables such as the coupling coefficient $k$ and the load resistance $R_L$, which may vary depending on the specific application. Fortunately, $C_s$ is independent of both $k$ and $R_L$, as indicated in Equation (2.11) [10]. In

Equation (2.11), $\omega_0$ represents the resonant frequency of the LC tank. It should be noted that the addition of compensation capacitors does not deliver a high PF for all frequencies, but rather at specific frequencies.

$$C_s = \frac{1}{\omega_0^2 L_s^2} = \frac{1}{4\pi^2 f^2 L_s^2} \tag{2.11}$$

Regarding $C_p$ its dependency on $k$ and $R_L$ can vary depending on the specific topology being utilized. The specific dependencies for each topology are outlined in Table 2.2 [10]. Notably, it can be observed that the S-S topology is independent of both variables, whereas the S-P topology solely depends on $k$. On the other hand, both the P-S and P-P topologies rely on both $k$ and $R_L$. These dependencies should be carefully considered when determining the suitable IPT topology.

**Table 2.2:** Primary side capacitance $C_p$ criteria for resonant for each compensation topology [10].

| | |
|---|---|
| S-S | $\frac{L_s C_s}{L_p}$ |
| S-P | $\frac{L_s^2 C_s}{L_p L_s - M^2}$ |
| P-S | $\frac{L_p L_s^2 C_s^2 R_L^2}{M^4 + L_s L_p R_L^2}$ |
| P-P | $\frac{L_s^2 \left(L_p L_s - M^2\right) C_s}{(L_p L_s - M^2)^2 + M^4 R_L^2 L_s C_s}$ |

### 2.3.2. Efficiency trade-off for different compensation topologies

The next criterion to consider is efficiency. In both P-P and P-S topologies, a current source is required, which introduces the need for an additional inductor at the input [8]. Unfortunately, the inclusion of this extra inductor leads to increased losses in the overall system [42]. Due to the lower efficiency and the dependency on both $k$ and $R_L$ when calculating $C_p$, both P-P and P-S topologies are deemed unsuitable as viable compensation topologies.

### 2.3.3. Chosen compensation topology for IPT System

By opting for S-S instead of S-P, the alignment-independent nature of $C_p$ is ensured, which is vital for maintaining consistent power transfer. While S-P allows for a smaller self-inductance of the receiver coil at the same load and operating frequency, as highlighted in [8], it's important to acknowledge that the magnetic coupling coefficient $k$ can vary, as observed in electric vehicles [22]. Taking these factors into consideration, the S-S configuration has been chosen for this thesis.

## 2.4. Series-Series (S-S) compensation IPT system

The PF can now be expressed as shown in Equation (2.12). For a detailed derivation, please refer to Appendix A.2.

$$Z_{in} = \frac{\left(R_p + j\omega L_p - j\frac{1}{\omega C_p}\right) \cdot \left(R_s + R_L + j\omega L_s - j\frac{1}{\omega C_s}\right) + (\omega M)^2}{R_s + R_L + j\omega L_s - j\frac{1}{\omega C_s}} \tag{2.12}$$

By manipulating the values of $C_p$ and $C_s$ in Equation (2.12), a near unity PF can be achieved, even at high frequencies. This is demonstrated in Figure 2.9, where specific capacitance values are carefully selected to attain a desired frequency with a near unity PF. The parameter values utilized for this analysis are listed in Table 2.3 [44].

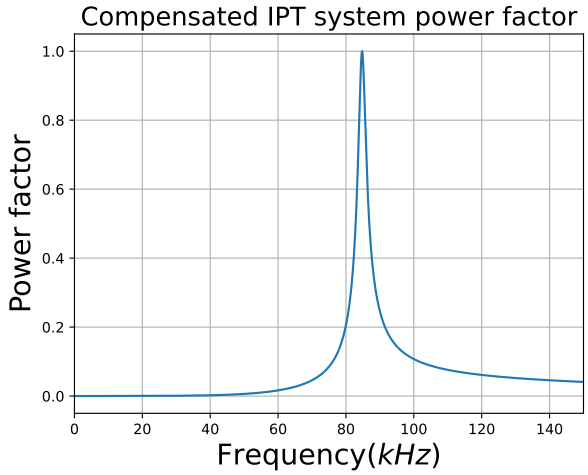



**Figure 2.9:** Power factor as a function of frequency for a compensated IPT system.

**Table 2.3:** System parameters used for simulations Figure 2.9 [44].

| Symbol | Parameter | Values | Unit |
|---|---|---|---|
| $L_p$ | Primary coil inductance | 293.8 | $uH$ |
| $L_s$ | Secondary coil inductance | 198.8 | $uH$ |
| $M$ | Mutual inductance | 46 | $uH$ |
| $R_p$ | Primary coil parasitic resistance | 0.21 | $\Omega$ |
| $R_s$ | Secondary coil parasitic resistance | 0.14 | $\Omega$ |
| $R_L$ | Load resistance | 150 | $\Omega$ |
| $C_p$ | Primary compensation capacitor | 12.0 | $nF$ |
| $C_s$ | Secondary compensation capacitor | 17.6 | $nF$ |
| $f_s$ | Switching frequency | 85 | $kHz$ |

## 2.5. Power electronic topologies for IPT

The previous section discussed the role of inductive coils in wireless power transfer and how adjusting compensation capacitors can optimize the system's power factor. This section delves into the power electronics required for driving the coils and converting the received power.

To achieve these objectives, different fundamental topologies can be utilized, including AC/DC, DC/DC, AC/AC, and DC/AC converters. In the case of IPT, the design goal is to provide DC voltage to a battery from a generated AC voltage from the secondary-side inductor. Therefore, an AC/DC topology is necessary. To drive the primary-side coil, AC voltage is required following Faraday's law. The power source can be either AC (grid) or DC (battery). However, this thesis focuses solely on the battery option, which necessitates the use of a DC/AC converter.

### 2.5.1. Overview of AC/DC converter topologies in power electronics

A potential topology for the AC/DC conversion is the single-phase diode rectifier, which operates as depicted in Figure 2.10. This topology employs a diode to eliminate the negative portion of the AC voltage, while a capacitor ensures a steady voltage supply to the load. The capacitor prevents the voltage from dropping to zero during the negative cycle by gradually discharging. As the AC source becomes positive again, the capacitor recharges, leading to an increase in voltage. The single-phase diode rectifier offers advantages such as a low component count and does not require a controller.

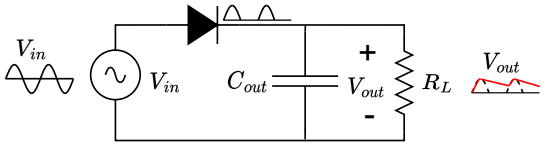



**Figure 2.10:** Circuit representation of single phase diode rectifier.

Although a single-phase diode rectifier functions adequately as an AC/DC converter, it only utilizes the positive cycle of the AC voltage. To take advantage of both cycles, a full bridge diode rectifier topology (illustrated in Figure 2.11) can be implemented. While this topology also requires no controller, it necessitates four diodes instead of one, introducing additional failure points and increasing the system's cost. Nevertheless, because it can utilize the entire received voltage range, it is generally preferred despite its drawbacks.

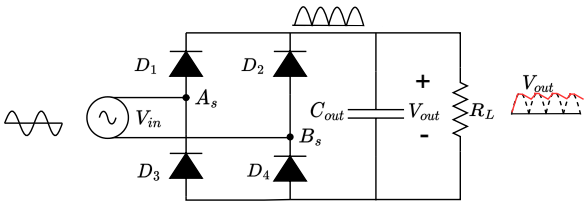



**Figure 2.11:** Circuit representation of full bridge diode rectifier.

## 2.5.2. Overview of DC/AC converter topologies in power electronics

A potential topology for the DC/AC conversion is the half-bridge inverter, illustrated in Figure 2.12. This topology utilizes two MOSFETs that can be switched between an ON (conducting) and OFF (non-conducting) state. To prevent both MOSFETs from conducting simultaneously and causing a low-resistance path with excessive current flow (known as "shoot-through"), a small dead time is introduced between the switching signals. This dead time ensures the proper operation of the inverter and prevents potential damage.

When MOSFET $S_1$ is closed, it provides a voltage of $V_{in}/2$, and when $S_2$ is closed, it provides a voltage of $-V_{in}/2$. As the use of a diode is not possible in the DC/AC converter, a controller will be required for this design.

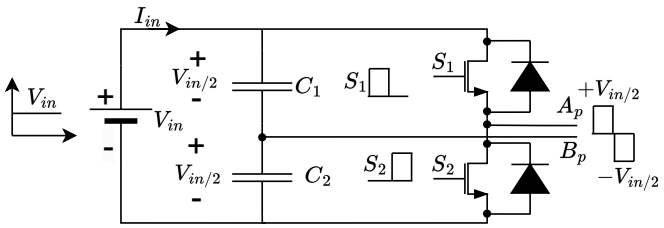



**Figure 2.12:** Circuit representation of half-bridge inverter.

Similar to the single-phase rectifier, the half-bridge inverter also operates at a reduced voltage compared to the full supplied voltage. However, by incorporating just two additional MOSFETs, the voltage can be increased to utilize the entire input voltage, as demonstrated in Figure 2.13. This enhancement, however, comes at the expense of added components and potential failure points. Nevertheless, the control algorithm can remain unchanged for both topologies, as illustrated in Figure 2.13. Similar to the AC/DC converter case, the topology that utilizes the entire voltage range is chosen.

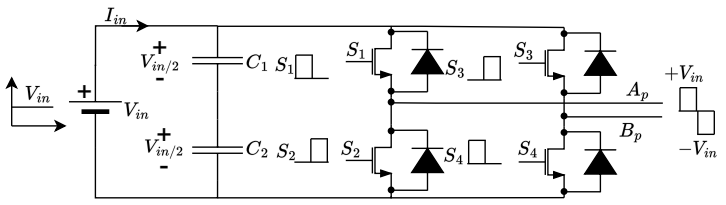



**Figure 2.13:** Circuit representation of full bridge inverter.

### 2.5.3. Compensated IPT system with power electronics

To showcase the combination of the chosen power electronics topologies and the compensated IPT system discussed earlier, please refer to Figure 2.14.

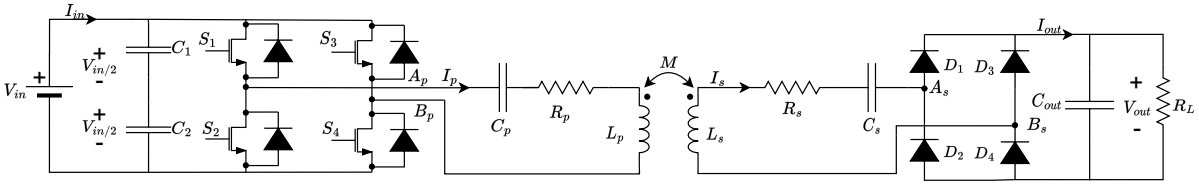



**Figure 2.14:** Circuit representation of traditional S-S configured IPT system. The primary side consists of a full bridge inverter, while the secondary side utilizes a full bridge diode rectifier.

In this setup, a full bridge diode is placed between the IPT and the load. However, to simplify the equation and avoid dealing with the non-linear characteristics of diodes, conveniently the load can be represented using an equivalent AC resistor ($R_{AC}$). The model depicting the load can be observed in Figure 2.15, and the corresponding value of $R_{AC}$ can be found in Equation (2.13). The derivation for this representation can be found in Appendix A.3. The validity of this approach is corroborated by both [37] and [16].

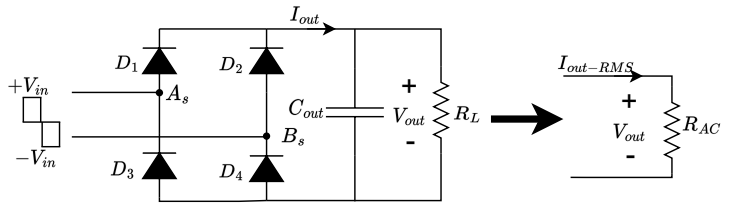



**Figure 2.15:** The $R_{AC}$ equivalent model for a full bridge diode rectifier with $R_L$.

$$R_{AC} = \frac{8}{\pi^2} R_L \tag{2.13}$$

## 2.6. Optimal load for diode-based S-S IPT topology

With the configuration of the system established, which includes a full bridge inverter driving the S-S compensated IPT system, connected to the load through a full bridge diode rectifier, the next step is to evaluate the system's efficiency. To simplify the analysis, Figure 2.16 will be employed as a representation of the overall system, as depicted in Figure 2.14.

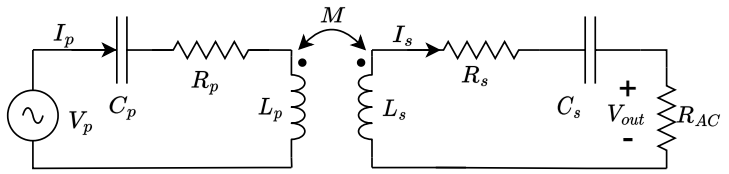



**Figure 2.16:** Equivalent circuit model to represent the system shown in Figure 2.14.

For this analysis, the first harmonic approximation (FHA) will be utilized, assuming that all currents are pure sinusoidal. This assumption is reasonable since, in an S-S configured system, power is primarily transferred in the first harmonic [18]. Considering that this is an S-S configured system, the secondary side functions as a current source. The output voltage is $I_s R_{AC}$, and the output voltage gain is calculated as follows:

$$G_v = \frac{I_s R_{AC}}{V_p} \tag{2.14}$$

The equation above can be expressed as Equation (2.15). For the derivation, please refer to Appendix A.4. At the resonant frequency, it can be reformulated as Equation (2.16). Notably, increasing $R_L$ will lead to a higher output voltage.

$$G_v = \frac{j\omega M R_{AC}}{(R_p + j\omega L_p + \frac{1}{j\omega C_p})(R_s + R_{AC} + j\omega L_s + \frac{1}{j\omega C_s}) + \omega^2 M^2} \tag{2.15}$$

$$G_v = \frac{j\omega_0 M R_{AC}}{R_p(R_s + R_{AC}) + \omega_0^2 M^2} \tag{2.16}$$

Depending on the application, increasing the output voltage may be desirable. Since power is the product of voltage and current, for the same amount of provided power, increasing the output voltage results in a decrease in the output current, which in turn reduces thermal losses and the required wire size. However, as will be shown shortly, increasing $R_L$ beyond its optimal point will result in a less power-efficient system. The following equation can be used to calculate efficiency:

$$\eta_p = G_i G_v \tag{2.17}$$

where:

$$G_i = \frac{I_s}{I_p} \tag{2.18}$$

This expression can be written as shown in Appendix A.4 as:

$$G_i = \frac{j\omega M}{R_{AC} + R_s + j\omega L_s + \frac{1}{j\omega C_s}} \tag{2.19}$$

Which can finally be written as:

$$\eta_p = \frac{j\omega M}{(R_{AC} + R_s + j\omega L_s + \frac{1}{j\omega C_s})} \cdot \frac{j\omega M R_{AC}}{(R_p + j\omega L_p + \frac{1}{j\omega C_p})(R_s + R_{AC} + j\omega L_s + \frac{1}{j\omega C_s}) + \omega^2 M^2} \tag{2.20}$$

At the resonant frequency $\omega_0$, the equation can be reformulated as shown in Equation (2.21). While this may not be immediately evident, it is important to note that at the resonant point, increasing $R_{\text{load}}$ leads to an increase in $G_V$ by a certain factor, but $G_i$ decreases by a larger factor. Consequently, the system's efficiency can decrease beyond a certain point.

$$\eta_p = \frac{j\omega_0 M}{(R_{AC} + R_s)} \cdot \frac{j\omega_0 M R_{AC}}{R_p(R_s + R_{AC}) + \omega_0^2 M^2} \tag{2.21}$$

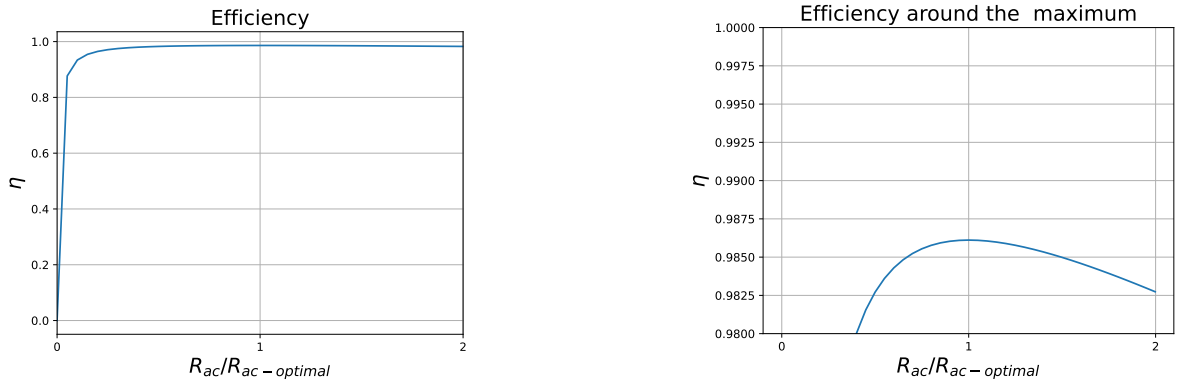
The optimal $R_{AC}$ can be calculated using Equation (2.22), thus will result in Equation (2.23). The derivation can be found in Appendix A.4. Using the parameters given in Table 2.3 will result in $R_{ac,optimal} = 20\Omega$.

$$R_{AC,optimal} => \frac{d\eta_p}{dR_{AC}} = 0 \tag{2.22}$$

$$R_{AC,optimal} \approx \omega_0 M \sqrt{\frac{R_s}{R_p}} \tag{2.23}$$

After examining the equation above, it can be determined that the derivative becomes zero at $R_{AC,optimal}$, indicating the presence of a maximum or minimum. Two methods can be employed to determine which

type it is: an analytical approach involving computing the second derivative $\eta''(R_{AC})$, or a graphical approach that involves plotting $\eta(R_{AC})$. If the second derivative around $R_{AC,optimal}$ is positive, then $R_{AC,optimal}$ corresponds to a minimum, whereas a negative second derivative indicates a maximum. In this case, the graphical approach was utilized, and the resulting plot is presented in Figure 2.17. The code for this plot can be found in Appendix B.2.




(a) (b)

**Figure 2.17:** Efficiency of traditional IPT systems at the resonant frequency, plotted as a function of load scaled by $R_{AC}$,: (a) full range, and (b) zoomed-in around the maximum.

Upon examining the plot above, it can be concluded that $R_{AC,optimal}$ is indeed a maximum It is worth noting that the x-axis is scaled by $R_{AC}/R_{ac,optimal}$.

# 3

# Dual side IPT control topology

The proposed traditional topology previously introduced encounters a practical challenge known as load-dependent optimal efficiency. This challenge becomes particularly significant in the context of electric vehicle (EV) charging, as the internal resistance of EV batteries varies throughout the charging cycle, as depicted in Figure 3.1. As a result, maintaining optimal efficiency throughout the entire charging process becomes challenging with the traditional design. This limitation highlights the need to explore more innovative solutions that can effectively mitigate the impact of load impedance variations and deliver consistent performance. Moreover, it is crucial to avoid designs that heavily rely on load impedance for achieving optimal efficiency.

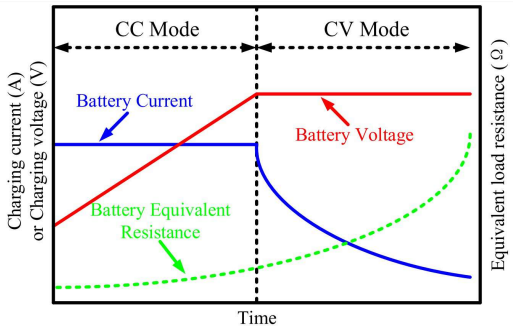



**Figure 3.1:** Typical charging profile of EV battery [9].

The upcoming subsection demonstrates a modification to the traditional design that eliminates the reliance on load impedance for achieving optimal efficiency.

## 3.1. Dual active topology

To address the issue of load-dependent efficiency in IPT systems, cascaded DC/DC converters are commonly employed, as evidenced by studies such as [12] and [19]. These converters are implemented either in the front-end or back-end of the system, with the primary-side converter ensuring a stable load voltage and the secondary-side converter responsible for maximum efficiency tracking. While the use of DC/DC converters enables achieving control objectives, it also introduces additional losses, increased costs, and reduced power density.

In [43], phase shift control was implemented in the primary-side inverter to match the load, eliminating the need for a front-end DC/DC converter by introducing active control of the inverter. However, a load-side DC/DC converter was still required to attain the desired output control metrics. To further eliminate the need for the load-side DC/DC converter, an active rectifier can be employed to regulate the equivalent load impedance, as proposed in [14] and [27]. In [24], a dual-phase-shift (DPS) control method based on the active rectifier was introduced, wherein the phase shift angles of the inverter and rectifier stages were cooperatively adjusted to achieve power regulation and load matching simultaneously.

Therefore, the proposed topology to overcome load-dependent maximum efficiency is showcased in Figure 3.2, also known as the dual active bridge (DAB) topology.

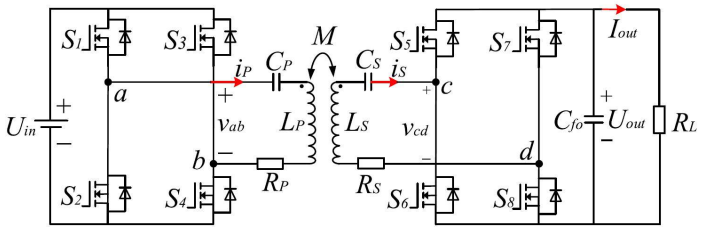



**Figure 3.2:** Circuit diagram of the S-S compensated IPT system with an active rectifier stage [44].

## 3.2. Dual side control

By adopting the DAB topology, the implementation of dual-side control becomes possible. This approach offers several advantages. Firstly, utilizing power MOSFETs instead of power diodes reduces losses and enhances system efficiency [44]. Secondly, the output can be precisely controlled to match specific load profiles, such as the two-stage charging process of EV batteries, involving constant current (CC) and constant voltage (CV) modes [44]. Thirdly, incorporating an active rectifier on the secondary side enables zero voltage switching (ZVS), effectively reducing electromagnetic interference (EMI) [44]. Lastly, by adjusting the duty cycle on the secondary sides, the maximum efficiency can be maintained independently of the load [44]. These features highlight the advantages of dual-side control in achieving improved efficiency, precise output regulation reduced EMI, and load-independent maximum efficiency.

### 3.2.1. Optimizing efficiency with active load tracking

In the previous chapter, Equation (2.13) was used to determine the equivalent resistance for a diode bridge configuration. However, since the diodes will now be replaced with an active rectifier, a new expression is required to represent $R_{AC}$. Although $R_{AC}$ was previously utilized to represent the load, it does not fully represent the complete expression for the load. The overall model is illustrated in Figure 3.3. For the diode rectifier $X_{\text{AC}}$ was neglected. The reason for this will be explained shortly.

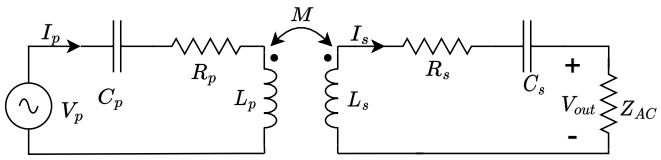



**Figure 3.3:** Circuit representation of simplified IPT S-S topology with reflected load impedance.

A general representation for $Z_{ac}$ is shown in Equation (3.1)[36].

$$Z_{AC} = R_{AC} + jX_{AC} \tag{3.1}$$

where

$$\begin{cases} R_{\text{AC}} = \frac{4}{\pi^2} R_L \cos^2(\varphi_s)(1 - \cos(D_s\pi)) \\ X_{\text{AC}} = \frac{4}{\pi^2} R_L \sin(\varphi_s)\cos(\varphi_s)(1 - \cos(D_s\pi)) \end{cases} \tag{3.2}$$

Before understanding why $X_{\text{AC}}$ can be neglected with a diode rectifier the parameters $\varphi_s$ and $D_s$ need to be understood. To help Figure 3.4 can be used. As can be seen, $\varphi_s$ represents the phase difference between the secondary side voltage and current, and $D_s$ is the duty cycle on the secondary side. In a diode rectifier, there is no phase shift between the secondary side voltage and current since diodes cannot introduce any phase shift ($\varphi_s = 0$). Consequently, when revisiting Equation (3.2), it leads to $X_{\text{AC}} = 0$. This explains why it was disregarded in the previous chapter. Furthermore, in a diode rectifier, $D_s = 1$ as it remains in continuous conduction. As a result, Equation (3.3) was obtained, which is the same expression used in the previous chapter for the diode rectifier configuration.

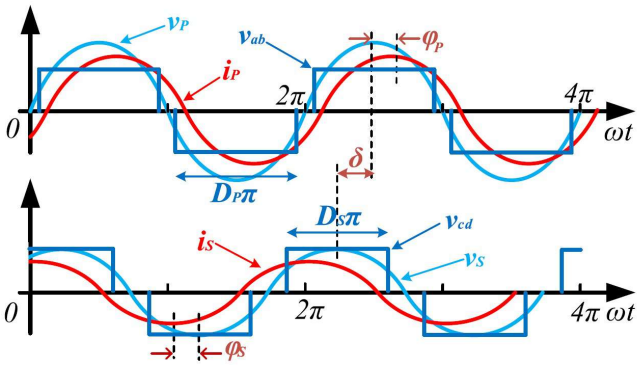



**Figure 3.4:** Typical waveforms of an IPT system using phase shift control. [44].

$$\begin{cases} R_{\text{AC}} = \frac{8}{\pi^2} R_L \\ X_{\text{AC}} = 0 \end{cases} \tag{3.3}$$

The optimal load is still

$$R_{AC,optimal} \approx \omega_0 M \sqrt{\frac{R_s}{R_p}} \tag{3.4}$$

While the notable advantage of utilizing an active rectifier lies in the flexibility to fine-tune $R_{AC}$ to its optimal value ($R_{AC,optimal}$), even when $R_L$ is suboptimal or deviates from the desired value by adjusting $D_s$, it is important to acknowledge that a purely resistive load ($X_{AC} = 0$) may not always be preferable due to its lack of ZVS functionality, potentially leading to reduced efficiency. Conversely, achieving ZVS implementation calls for the desirable characteristic of an inductive load[44]. Unlike diode bridges, an active rectifier can accommodate an inductive load by adjusting $\varphi_s$. This concept will be useful for ZVS which will be explained in the following subsection.

### 3.2.2. Increasing efficiency with zero-voltage switching (ZVS)

Before delving into the implementation of ZVS, it is important to understand why ZVS is necessary. In an ideal scenario, MOSFETs can only be fully conducting (ON) or completely blocking (OFF). However, in practical MOSFETs, there exist transition states between these two states. Due to parasitic inductance, the current through the MOSFET drain ($I_D$) gradually increases as the MOSFET transitions from OFF to ON, while due to parasitic capacitance, the voltage across the drain and source ($V_{DS}$) slowly decreases during the transition from OFF to ON. The same holds in the transition from ON to OFF but in reverse. This phenomenon is known as hard switching, and these transitions are illustrated in Figure 3.5. As shown, these transitions result in losses, known as the switching losses of a MOSFET. These losses become problematic when operating at higher frequencies because the more frequently the switch turns OFF and ON, the greater the number of switching losses. It is important to note that Figure 3.5 provides a simplified representation of these transitions.

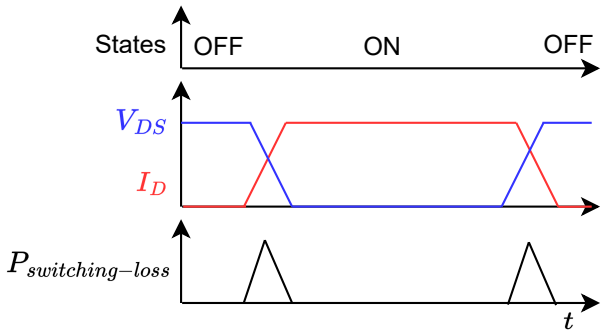



**Figure 3.5:** Simplified representation of switching losses with hard switching.

To reduce switching losses, the overlap between $V_{DS}$ and $I_D$ needs to be decrease. While this can be achieved through hardware means, such as incorporating snubber circuits, this approach introduces additional components and may require component replacements to fine-tune values. A more favorable and flexible alternative involves utilizing software techniques. Specifically, introducing phase shifts $\varphi_s$ and $\varphi_p$ between current and voltage, known as soft switching, proves highly beneficial.

Implementing ZVS is highly desirable as it helps minimize losses by ensuring that the voltage $V_{DS}$ remains at $0V$ during the transition stages of the current $I_D$. However, achieving ZVS with a resistive load is challenging due to the presence of the parasitic output capacitor $C_{DS}$. If the current is $0A$ and was previously greater than $0A$ before the transition, the voltage across $C_{DS}$ will not be discharged completely, preventing the voltage during transitions from reaching $0V$ and hindering true ZVS. As a result, the waveform depicted in Figure 3.6(a) does not represent true ZVS.

Achieving true ZVS can be accomplished by incorporating a negative current before the transition, resulting in the discharge of $C_{DS}$. Dual-side control plays a crucial role in modifying $\varphi_s$, wherein the preference for not always having a purely resistive load ($X_{AC} = 0$) becomes relevant. By adjusting the current to either lead or lag the voltage, the effective discharge of the voltage over $C_{DS}$ is achieved, enabling ZVS. This approach highlights the significance of dual-side control in achieving efficient ZVS operation.

The research conducted by [23] highlights the importance of utilizing Silicon Carbide (SiC) MOSFETs in ZVS applications, particularly for reducing turn-on losses rather than turn-off losses. Further analysis of the datasheet for the SiC MOSFET used in the DAB circuit explains this preference - the SiC MOSFET exhibits larger turn-on losses compared to turn-off losses [34]. Therefore, to improve the overall efficiency of the system, the current must lag, requiring the inclusion of an inductive load for effective ZVS implementation. This concept, as depicted in Figure 3.6(b), represents true ZVS.


**Figure 3.6:** (a) Waveforms without true ZVS, and (b) waveforms with true ZVS.

### 3.2.3. Enhancing battery charging profile tracking through power flow control

This subsection delves into another significant benefit of dual-side control, enabling it to follow the battery charging profile depicted in Figure 3.1. The system's output power, denoted as $P_{out}$, is governed by Equation (3.5) [44]. By employing dual-side control, not only $D_p$ but also $D_s$ can be precisely regulated, allowing the power delivered to EV batteries to be controlled in alignment with the charging profile.

$$P_{out} = \frac{U_{in}U_{out}\frac{8}{\pi^2}sin[(D_p\pi)/2]sin[(D_s\pi)/2]cos(\varphi_s)}{\omega_0 M} \tag{3.5}$$

## 3.3. Validation of higher efficiency through dual side control implementation

This section aims to validate the impact of ZVS implementation on overall system efficiency and demonstrates how adjusting parameters on both sides allows for precise control of the output power. While

active optimal load tracking will not be conducted due to the setup being utilized by another researcher, modifications are limited to only the PWM output from the microcontroller. The setup details are illustrated in Figure 3.7.

For the test, a bidirectional power supply efficiently feeds power back into the grid, minimizing wastage as heat. A single microcontroller effectively controls both primary and secondary sides remotely, using fiber optics for safe communication. System efficiency is assessed with a power analyzer, while differential probes provide voltage measurements. Full setup details are provided in Table 3.1.

**Table 3.1:** Important parameters for test setup shown in Figure 3.7.

| Material | Value | MPN | Manufacturer |
|---|---|---|---|
| Primary side inductor | $59.8907\mu H$ | - | DCE&S |
| Primary side compensation capacitance | $63.8636nF$ | - | DCE&S |
| Secondary side inductor | $59.8480\mu H$ | - | DCE&S |
| Secondary side compensation capacitance | $63.9625nF$ | - | DCE&S |
| Mutual inductance between primary and secondary | $17.5365\mu H$ | - | DCE&S |
| Microcontroller | - | LAUNCHXL-F28379D | Texas Instruments |
| High-Voltage Differential Probe, 25 MHz | - | N2791A | Keysight |
| Current probes 20MHz | - | 110 | PEARSON |
| Load/Source | - | SM500-CP-90 | Delta |
| Power analyzer | - | WT500 | Yokogawa |
| Oscilloscope | - | DLM2054 | Yokogawa |

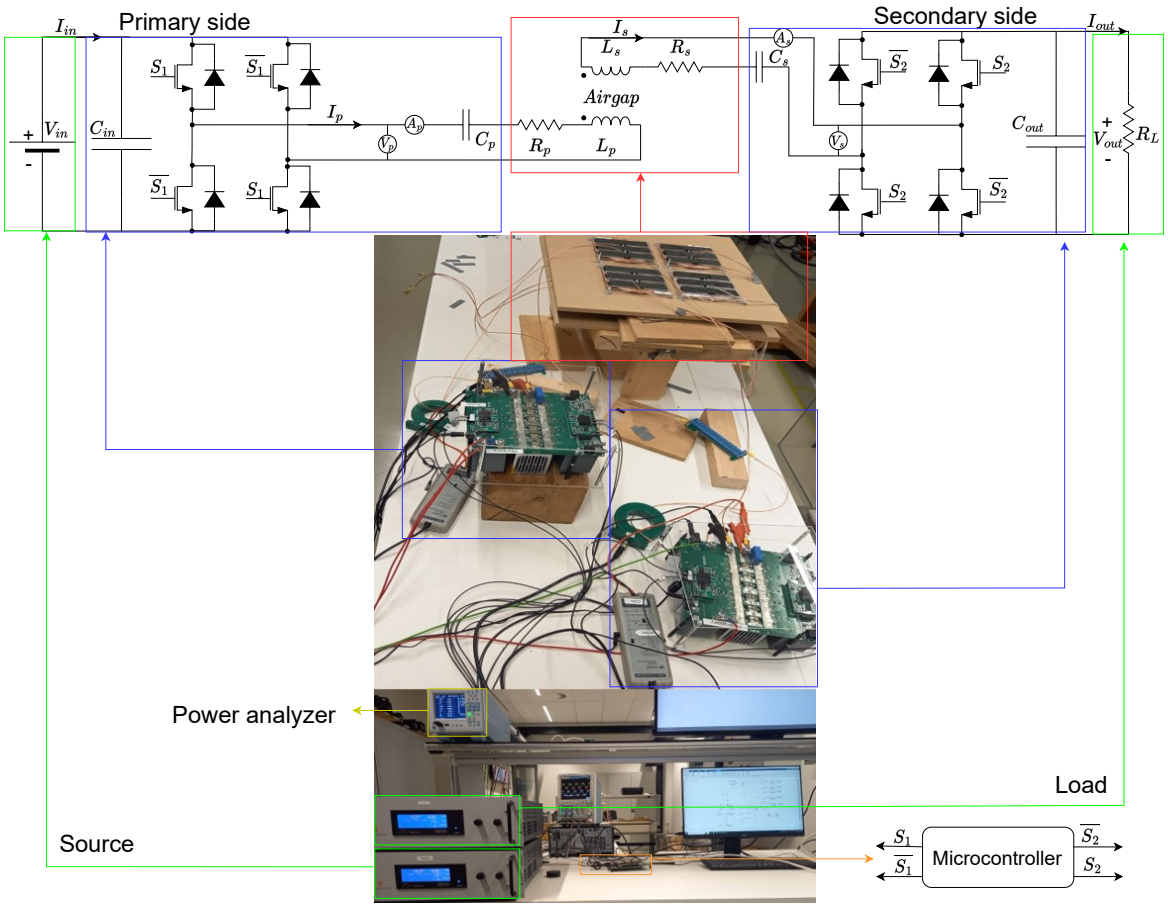



**Figure 3.7:** Test setup for dual side control.

While Figure 3.4 visually illustrates the time domain behavior in a typical IPT system, an alternative approach is to consider the phase vector representation. In this representation, the parameter $\varphi$ de-

notes the phase difference between the current and voltage of the respective side. However, it may not be immediately apparent how the secondary side current relates to the primary side voltage, and vice versa. To address this, Equation (2.4) offers valuable insights. By isolating the relevant term from the opposite side, the relationship between the two can be expressed as follows, the resistive terms are neglected since they do not affect phase shift thus:

$$\begin{cases} v_p \approx -M\frac{d}{dt}i_s \\ v_s \approx M\frac{d}{dt}i_p \end{cases} \tag{3.6}$$

Applying the Laplace transform to the aforementioned equation and considering an initial condition of $0$ yields the following expression in the phasor representation:

$$\begin{cases} V_p \approx -Mj\omega I_s \\ V_s \approx Mj\omega I_p \end{cases} \tag{3.7}$$

Thus the vector diagram can be given as:

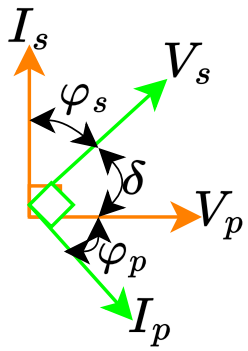



**Figure 3.8:** Equivalent vector representation of Figure 3.4

When the system operates without ZVS, the results are depicted in Figure 3.9. The line-to-line voltage and the coil currents are shown. For detailed parameters of both sides, please refer to Table 3.2. The operating frequency of $85kHz$ falls within the range of $81.38 - 90kHz$, which is determined by ISO/PAS19363[20].

**Table 3.2:** Parameters implemented in the microcontroller for Figure 3.9.

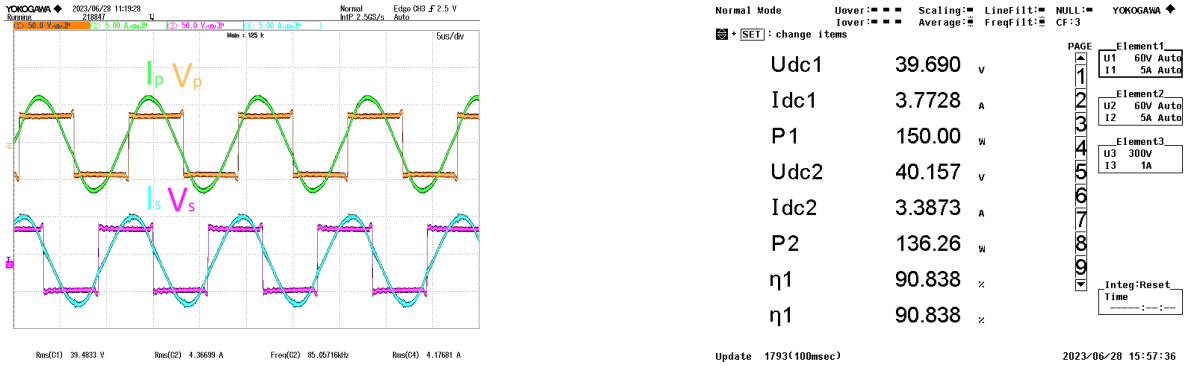
| Symbol | Parameter | Values | Unit |
|---|---|---|---|
| $D_p$ | Duty cycle primary side | 50 | % |
| $D_s$ | Duty cycle secondary side | 50 | % |
| $\delta$ | Phase difference | 10 | $^0$ |
| $f_s$ | Switching frequency | 85 | $kHz$ |

Now, the system undergoes a phase shift until ZVS is implemented, with detailed parameters presented in Table 3.3. The corresponding results are depicted in Figure 3.10, where only the phase angle is modified in comparison with Figure 3.9. While the correspondence $V_p$ and $I_p$ shown in Figure 3.10(a) may not be immediately apparent, it aligns with the waveform characteristics illustrated in Figure 3.6(b).

**Table 3.3:** Parameters implemented in the microcontroller for Figure 3.10

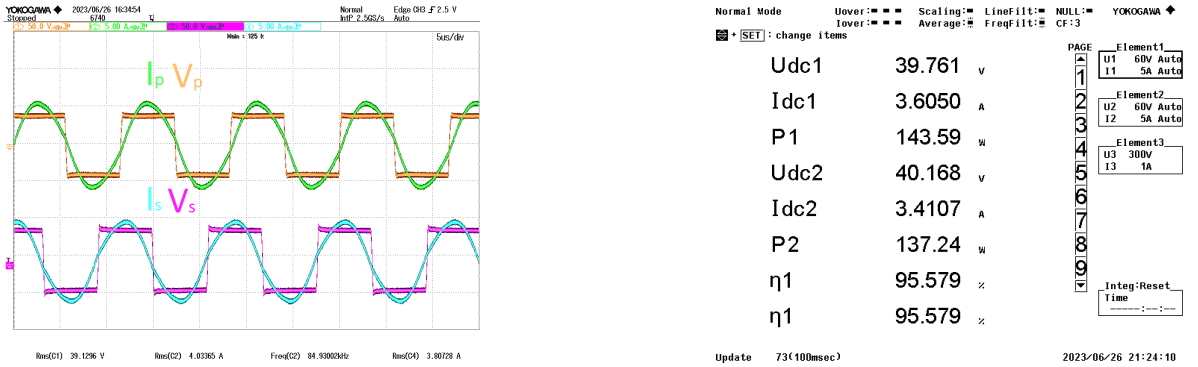
| Symbol | Parameter | Values | Unit |
|---|---|---|---|
| $D_p$ | Duty cycle primary side | 50 | % |
| $D_s$ | Duty cycle secondary side | 50 | % |
| $\delta$ | Phase difference | 45 | $^0$ |
| $f_s$ | Switching frequency | 85 | $kHz$ |

Now $D_p$ and $D_s$ will be modified to show power flow control.with detailed parameters presented in Table 3.4. The corresponding waveforms are depicted in Figure 3.11,




(a) (b)

**Figure 3.9:** Dual-side system without zero voltage switching (ZVS): (a) measured voltage and current waveforms of primary and secondary, and (b) efficiency of power transferred.

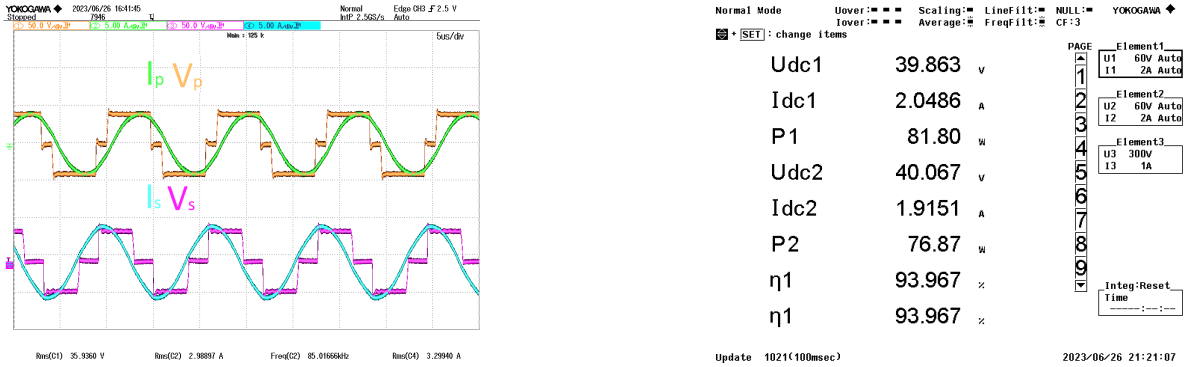



(a) (b)

**Figure 3.10:** Dual-side system with zero voltage switching (ZVS): (a) (a) measured voltage and current waveforms of primary and secondary, and (b) efficiency of power transferred.

**Table 3.4:** Parameters implemented in the microcontroller for Figure 3.11

| Symbol | Parameter | Values | Unit |
|---|---|---|---|
| $D_p$ | Duty cycle primary side | 40 | % |
| $D_s$ | Duty cycle secondary side | 30 | % |
| $\delta$ | Phase difference | 45 | $^0$ |
| $f_s$ | Switching frequency | 85 | $kHz$ |




(a) (b)

**Figure 3.11:** Dual-side system with modified duty cycle for power flow control: (a) measured voltage and current waveforms of primary and secondary, and (b)efficiency of power transferred.

## 3.4. New challenges with dual side control topology

In a previous study [44], the optimal duty cycle value was successfully transmitted. However, in real-world wireless power transfer scenarios, using a single microcontroller for both the primary and secondary sides becomes impractical. In practical applications, the primary side coils are typically implanted into the ground, while the secondary side is implanted inside an electric vehicle (EV). Therefore, employing two microcontrollers, one for the primary side and the other for the secondary side, is a more feasible solution. This allows for wireless transmission of the optimal duty cycle between the microcontrollers, similar to the wireless power transfer between the primary and secondary sides.

The proposed new design shows great potential, but it faces two significant challenges that require immediate attention. The first challenge is achieving synchronization between the MOSFET voltage on the secondary side and the induced secondary side current from the coils. If these two elements are significantly out of phase, it can lead to a loss of power transfer. Additionally, it is crucial to determine the appropriate value of $\varphi_s$ for optimal load management and the implementation of ZVS.

The second challenge arises when the desired value of $R_L$ is not achieved, necessitating adjustments to $D_s$ and/or $\varphi_s$ on the secondary side to attain the optimal $R_{AC,optimal}$. However, changing $D_s$ to meet the optimal $R_{AC,optimal}$ also affects the power required on the secondary side. The primary side remains unaware of this change, resulting in an excessive or insufficient power supply, leading to less smooth power delivery. Hence, while optimal load matching is essential on the secondary side, both the primary and secondary sides play a crucial role in representing the system's output power. The expression for the system's output power, denoted as $P_{out}$, can be seen in Equation (3.5) [44], with the parameters derived from Figure 3.2. Consequently, the primary side's duty cycle also needs to be adjusted accordingly.

However, this approach introduces a new challenge. In the previous section, the secondary side PWM could be phase-shifted with respect to the primary side PWM. But with two separate microcontrollers, this method becomes impractical. Nevertheless, the secondary side does have access to $I_s$, which opens up the possibility of synchronizing the secondary side microcontroller with $I_s$ instead. While this synchronization hardware could be integrated inside the secondary side converter, it would be limiting if a newer converter is developed for this application. A more favorable approach is designing the synchronization system as a separate PCB that can be easily added to any converter, resulting in a more modular and versatile solution. The suggested design is shown below:

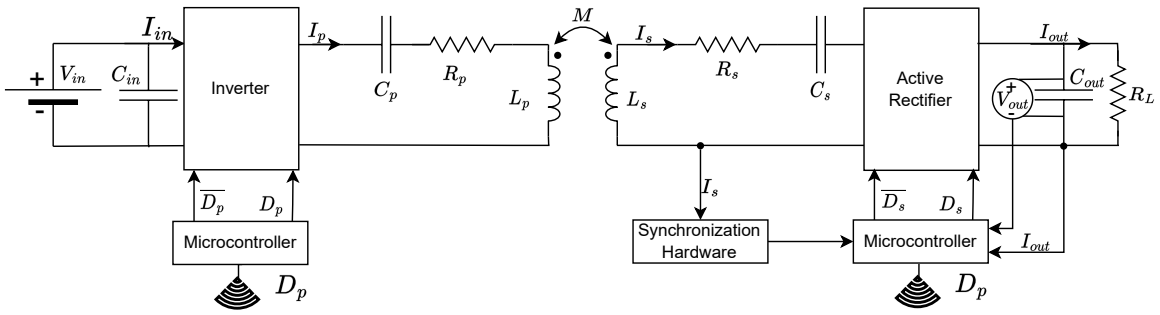



**Figure 3.12:** Proposed top-level design topology for dual side control of an IPT system.

In the proposed model, the synchronization hardware is situated on the secondary side. By measuring the output voltage and current, the secondary side microcontroller can accurately determine the optimal $D_s$ value and subsequently calculate the optimal $D_p$ to ensure steady power flow. The microcontroller then transmits this optimal value to the primary side using Wi-Fi, facilitating efficient power transfer.

This thesis focuses on addressing these challenges and presents a custom PCB design with a comprehensive schematic and layout, providing a clear rationale for its architecture. Furthermore, it demonstrates the PCB's exceptional ability to effectively synchronize the MOSFET voltage with the current in the secondary side coil. Additionally, wireless communication is used to transmit the duty cycle between the primary side microcontroller and the secondary side microcontroller.

# 4

# Synchronization design

This chapter aims to design a synchronization method between the voltage generated by the MOSFETs on the secondary side and the current produced by the secondary side coil.

In PCB design, trade-offs are inevitable. However, for this thesis, which centers around wireless charging for the DCES department, cost, and size are not the primary considerations. Instead, the emphasis lies on accuracy and low latency, vital factors supporting research in wireless charging. Regarding the synchronization software, its ultimate aim is to minimize the delay between the external trigger from the custom PCB and the generation of the microcontroller's PWM signals.

To ensure the proper switching of MOSFETs ON or OFF, a current sensor is indispensable. When selecting a controller, two options emerge: implementing it in either hardware or software. While a hardware controller occupies less space on the PCB, modifying it becomes more challenging as it involves replacing physical components. Additionally, integrating a new controller may necessitate design revisions. Hence, for this thesis, a digital controller utilizing the Texas Instruments LAUNCHXL-F28379D microcontroller was chosen. This widely-used microcontroller excels in power electronics applications, a realm that encompasses the endeavors within the DCES department. Throughout this chapter, unless explicitly specified otherwise, references to the microcontroller will specifically refer to the Texas Instruments LAUNCHXL-F28379D. This PCB needs to be able to know when the secondary side current crosses the zero point. Thus a zero current crossing detection (ZCCD) circuit is needed.

## 4.1. Schematic design for zero current crossing detection (ZCCD).

Before discussing the chosen design topology, the top-level design will be presented. The initial step involves capturing the input sine wave current centered around $0A$ using a current sensor. Subsequently, signal processing converts the sine wave current into a voltage source, eliminates negative values, and prepares it for measurement by a microcontroller that can only handle positive voltages. The top-level design is depicted in Figure 4.1.

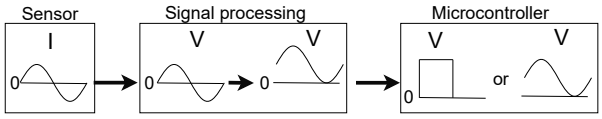



**Figure 4.1:** Top-level design for current signal processing.

After establishing the top-level design, the next step is to delve deeper into the system requirements. The zero current crossing system demands a sensor capable of measuring the AC source at a minimum of $85kHz$ and detecting both transitions through $0A$. Although the choice of the current sensor is not fixed, it must meet these requirements. The microcontroller can continuously measure voltage using the analog-to-digital converter (ADC), which has a range of $0$ to $3.3V$ [39], or it can use discrete values via general purpose input-output (GPIO), which are either $0$ or $3.3V$ [39].

### 4.1.1. Microcontroller measurement options

The first design decision to consider is the choice between utilizing the ADC or the GPIO for measurements. Each option has its own set of advantages and drawbacks.

The microcontroller employs Sigma Delta for ADC application[39]. While this thesis will not delve into the theory of Sigma Delta ADCs, it is worth noting their working principle. Sigma Delta ADCs employ oversampling by taking multiple samples and averaging them, resulting in a higher resolution value than what is sampled. As a result, Sigma Delta ADC provides more accurate measurements, but it tends to be slower due to the need for sampling, averaging, and signal processing to convert analog signals into digital form. This process introduces additional latency, as the microcontroller must perform further software computations to determine the zero point and enable the PWM signal.

On the other hand, GPIO offers a more straightforward approach without the need for complex signal processing. In the case of ZCCD, only the transition holds significance, rather than the magnitude itself. Considering this, utilizing the ADC option would require additional software implementation on the microcontroller to determine the zero point, which could introduce further delays.

After careful evaluation, the decision was made to use GPIOs on the microcontroller for this application. This choice aligns to minimize latency and ensures a more direct and efficient approach to detecting the zero-crossing points of the current waveform.

### 4.1.2. Current sensor selection

The next critical consideration is the choice of the current sensor. This thesis explores the four most widely utilized methods for measuring current in power electronics, as identified by Ziegler [45]: shunt resistor, current transformer, Rogowski coil, and Hall-effect sensor. Figure 4.2 depicts the current sensing capabilities of each method.

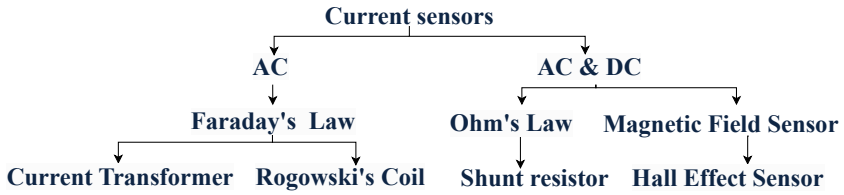



**Figure 4.2:** Various current sensor topologies for power electronics applications.

As the Rogowski coil and current transformer can solely measure AC, they are not adequate for overcurrent protection circuits, which were incorporated in this PCB for safety purposes, the overcurrent protection circuit is not the central focus of this thesis and thus will not be explained in this thesis. Thus, the shunt resistor and hall-effect sensor emerge as the only feasible alternatives for measuring both AC and DC.

Despite the availability of a more budget-friendly option like the shunt resistor, its insertion into the current path and tendency to generate heat can potentially undermine measurement accuracy, leading to errors and diminished precision over time. Therefore, for this thesis, the LAH-50P, a closed-loop hall-effect sensor, was selected as the preferred choice. This sensor offers precise measurements without these aforementioned drawbacks, albeit at a higher cost.

### 4.1.3. Designing the hardware signal processing

The signal processing aspect requires careful consideration. Directly linking the current passing through the coils to the microcontroller is not feasible without implementing signal processing techniques. The first step involves converting the high current into a manageable voltage level that can be handled by the microcontroller. To achieve this, the LAH-50P current sensor is employed, which reduces the target current $I_{target}$ by a factor of $2000$, resulting in a current of only a few milliamperes $(mA)$. This measurable current $I_{measured}$ then needs to be converted into a voltage suitable for the microcontroller. The most straightforward approach is to utilize resistors. The circuit configuration up to this point is illustrated in Figure 4.3.

Although the direct connection of the obtained $V_{measured}$ to the system rest of the system might seem appealing, it is, in fact, a suboptimal choice due to its dependency not only on the sensor resistance

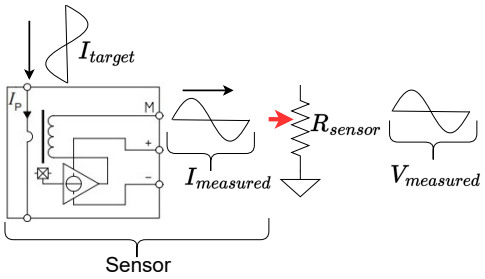



**Figure 4.3:** Signal processing: conversion from the target current to the measured voltage.

$R_{sensor}$ but also on the resistance beyond the sensor. This additional resistance can have a significant impact on $V_{measured}$, leading to what is known as the loading effect

To ensure highly accurate voltage measurement, the implementation of a voltage buffer becomes important. In this design, operational amplifiers (opamps) are utilized as voltage buffers to effectively address these concerns. Opamps, acting as voltage-dependent voltage sources, play a crucial role in compensating for the loading effect, thereby ensuring reliable and precise voltage measurements for the system.

For a quick refresher on opamps, consider the open-loop configuration depicted in Figure 4.4, where opamps serve as voltage-dependent voltage sources. This operation is given using Equation (4.1), with $A$ representing an extremely high gain factor. By amplifying the difference between its input terminals, the open-loop opamp achieves precise voltage amplification.

The $\pm V_{cc}$ represents the supply voltage range of the opamp. While they may not always be explicitly shown in the schematic representation for simplicity, the $\pm V_{cc}$ voltages are always present in the circuit, providing the necessary power for the opamp to operate.

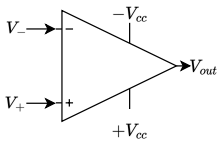



**Figure 4.4:** Open-loop configuration of an operational amplifier (opamp)

$$V_{out} = A(V_+ - V_-) \tag{4.1}$$

Before delving into the mathematics behind how a buffer can help mitigate the loading effect, it should be noted that there are two possible configurations for the buffer. Theoretically, these configurations are illustrated in Figure 4.5.


**Figure 4.5:** Opamps buffer topologies utilizing :(a) positive feedback, and (b) negative feedback.

In real-world applications, when it comes to buffering, Figure 4.5(b) is generally the preferred choice over Figure 4.5(a) due to the limited bandwidth of actual opamps. While both closed-loop configurations work well with ideal opamps, the use of negative feedback in Figure 4.5(b) makes it more suitable. On the other hand, Figure 4.5(a), which employs positive feedback, is better suited for applications involving oscillators or PWM signals.

To grasp the functioning of this buffer circuit, a fundamental understanding of closed-loop systems is essential. The system is represented as shown in Figure 4.6, with the controller's open-loop gain denoted by $A$, the feedback factor by $\beta$, and the system's closed-loop gain by $A_{CL}$. Employing negative

feedback, this buffer configuration proves advantageous, particularly due to the limited bandwidth of real-world opamps. The closed-loop transfer function is expressed in Equation (4.2), and its derivation is further elaborated in Appendix A.5.

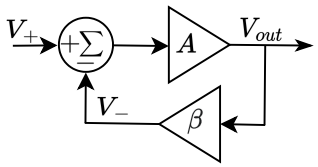



**Figure 4.6:** Representation of a closed-loop system for an opamp with negative feedback.

$$A_{CL} = \frac{V_{out}}{V_{in}} = \frac{A}{1 + A\beta} \tag{4.2}$$

The transfer function given by Equation (4.2) represents the gain of the system, but it may not explicitly indicate the overall gain of the system. To easily determine the system's gain, the transfer function can be expressed in the form of Equation (4.3), which introduces the error factor. This error factor accounts for the impact of the opamp's high gain, typically exceeding $100dB$. When the gain $A$ is exceptionally large, the error terms reduce to $1$, effectively simplifying the system's gain to the ideal value expressed in the transfer function of Equation (4.4). This allows for a clearer understanding of the overall gain of the system when considering the influence of the opamp's high gain.

$$A_{CL} = \underbrace{\frac{1}{\beta}}_{\text{Ideal gain}} \cdot \underbrace{\frac{A\beta}{1 + A\beta}}_{\text{Error}} \tag{4.3}$$

$$A_{CL} \approx \frac{1}{\beta}, \text{for } A\beta >> 1 \tag{4.4}$$

Upon examining the circuit depicted in Figure 4.5b, it becomes evident that the feedback factor $\beta$ has a value of 1, resulting in $A_{CL} = 1$. This is why the circuit is commonly referred to as a "voltage buffer." However, in practice, opamps cannot always provide the same gains for high frequencies due to the parasitic capacitance inherent in their design. As frequencies increase, the opamp begins to act as a low-pass filter, which necessitates a more accurate closed-loop system representation, as shown in Figure 4.7, where $\omega_c$ is the cut-off frequency.

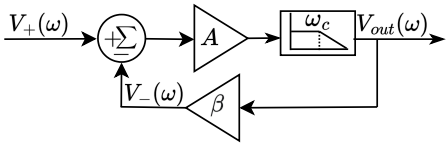



**Figure 4.7:** Representation of a closed-loop system for an opamp with negative feedback, considering limited bandwidth.

Consequently, the open-loop gain can be expressed as follows:

$$V_{out}(\omega) = A(V_+(\omega) - V_-(\omega))\frac{\omega_c}{j\omega + \omega_c} \tag{4.5}$$

Here, $\omega_c/(j\omega + \omega_c)$ represents a low-pass filter. The closed-loop gain with the frequency-dependent term is shown in Equation (4.6), and the derivation is provided in Appendix A.6.

$$A_{CL}(\omega) = \underbrace{\frac{A}{1 + A\beta}}_{\text{DC gain}} \cdot \underbrace{\frac{\omega_c \cdot (1 + A\beta)}{j\omega + \omega_c \cdot (1 + A\beta)}}_{\text{frequency dependent term}} \tag{4.6}$$

By implementing feedback in a circuit, the system's gain can be reduced by a factor of $1 + A\beta$, while simultaneously increasing the bandwidth by the same factor. This phenomenon is commonly known

as the gain-bandwidth relation, as illustrated in Figure 4.8. It represents a trade-off where the system's bandwidth is enhanced at the expense of decreased maximum amplification. This could be used if needed to increase the bandwidth of the system.

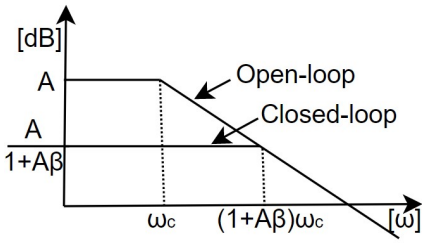



**Figure 4.8:** Relationship between opamp gain and bandwidth for open-loop and closed-loop feedback configurations.

In the context of this thesis, the target signal frequency falls within the $85kHz$ range. Among the opamps utilized, the TSV991IYLT opamp with a gain-bandwidth product of $20MHz$ [31] has the lowest bandwidth. Since a gain of only $1$ is required for the buffer, and as will be demonstrated later, all opamps in the final design will also operate with a gain of $1$. Therefore, the frequency-dependent aspect can be disregarded for the subsequent PCB design in this thesis.

It is important to note that manufacturing tolerances will introduce variations in $\Delta A$, impacting the open-loop gain $A$ and resulting in imprecise definitions as shown in Equation (4.7). Nevertheless, for feedback, the magnitude of $A$ is more critical than its precision. For instance, even a $10$% deviation of $\Delta A/A$ would only cause a small variation of $0.1/(1+A\beta)$ in the closed-loop gain. Therefore, the impact of tolerances can be considered negligible and does not pose significant concerns.

$$\frac{\Delta(A_{CL})}{A_{CL}} \approx \frac{\Delta A}{A}\frac{1}{1+A\beta} \tag{4.7}$$

Having established the foundational background information, the focus now shifts towards effectively implementing a voltage buffer to alleviate loading concerns arising from components beyond $R_{sensor}$. The decision to employ a buffer with feedback arises from the advantageous characteristics of opamps, particularly their high internal input resistance $r_i$ and low internal output resistance $r_o$. By utilizing negative feedback, the system's output resistance $R_o$ is reduced, while the input resistance $R_i$ is increased, further enhancing the system's performance. These enhancements prove particularly advantageous for $V_{measured}$, as it becomes dependent solely on $R_{sensor}$ and $R_i$. For a more detailed circuit depiction, please refer to figure 4.9.

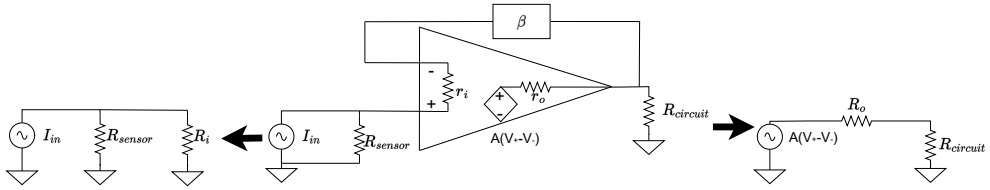



**Figure 4.9:** Buffer Opamp with an internal equivalent model, illustrating the internal resistance $R_i$ when viewed from the sensor $I_{in}$ and the output resistance $R_o$ when observed from the remaining circuit $R_{circuit}$.

By allowing $I_{measured}$ to choose between $R_{sensor}$ and $R_i$, increasing $R_i$ minimizes the loading effect and improves measurement accuracy. Similarly, a large $R_o$ in the opamp output can cause a significant voltage drop. Therefore, maintaining a low $R_o$ ensures sufficient voltage supply to subsequent components. Negative feedback in the opamp configuration greatly affects $R_i$ and $R_o$, as shown in Equation (4.8) and Equation (4.9). These equations demonstrate how negative feedback reduces $R_o$ and increases $R_i$. Please refer to Appendix A.7 for a detailed derivation of Equation (4.8) and Equation (4.9).

$$R_o \approx \frac{r_o}{1+A\beta} \tag{4.8}$$

$$R_i \approx r_i(1+A\beta) \tag{4.9}$$

The diagram presented in Figure 4.10 showcases the current circuit configuration, complete with the accompanying buffer circuitry. The voltage at the output of the buffer circuit is denoted as $V_{measured-buffered}$ in the diagram.

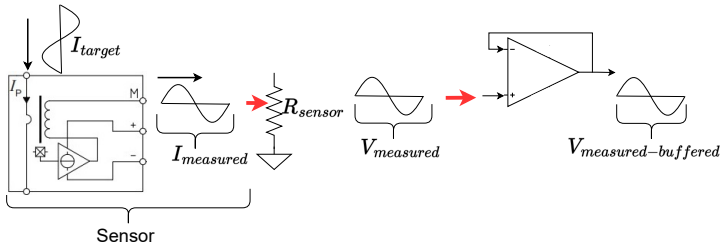



**Figure 4.10:** Signal processing: from the target current to measured buffered voltage.

The design of the ZCCD circuit can vary depending on specific requirements and constraints. The approach chosen for this thesis serves as an example of its implementation. The complete design is illustrated in Figure 4.11. This design involves the initial shifting of the voltage $V_{measured-buffered}$ through a differential amplifier by a DC offset, followed by the conversion of the resulting sine wave into a PWM signal using a comparator with hysteresis resulting in $V_{measured-compared}$ and finally inverting the PWM signal using an inverter resulting in $V_{ZCCD-output}$.

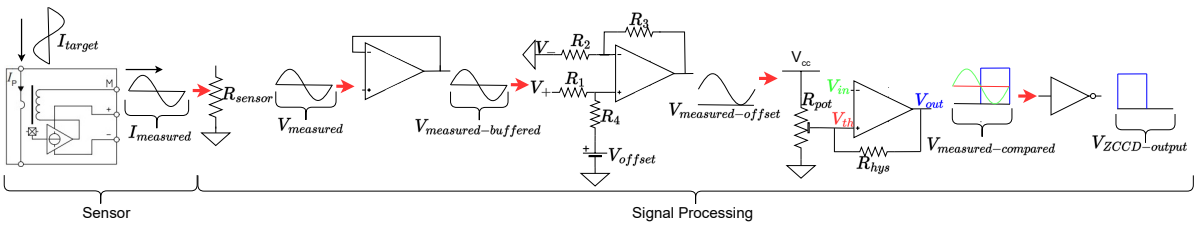



**Figure 4.11:** Chosen circuit topology for zero current crossing detection (ZCCD).

After selecting the ZCCD topology, this section will explain how it satisfies the required specifications. To begin, the voltage $V_{measured-buffered}$ is adjusted by adding a DC offset $V_{offset}$ to obtain the voltage $V_{measured-offset}$. The calculation for $V_{measured-offset}$ can be performed using Equation (4.10). For a comprehensive derivation of Equation (4.10), please refer to Appendix A.8.

$$V_{measured-offset} \approx V_+ \frac{R_3 + R_2}{R_2} \frac{R_4}{R_4 + R_1} + V_{offset} \frac{R_3 + R_2}{R_2} \frac{R_1}{R_4 + R_1} - \frac{R_3}{R_2} V_- \tag{4.10}$$

It is worth noting that by choosing $R_2 = R_1$ and $R_3 = R_4$, and considering that $V_-$ is grounded, the equation can be simplified as:

$$V_{measured-offset} \approx V_{offset} + \frac{R_3}{R_2} V_{measured-buffered} \tag{4.11}$$

The next step involving the conversion of $V_{measured-offset}$ into a discrete signal. To achieve this, a comparator with hysteresis was chosen, and the threshold voltage $V_{th}$ was set around the level of $V_{offset}$. This configuration ensures that a LOW signal is sent if $V_{measured}$ is positive, and a HIGH signal is sent if it is negative, providing the desired indication to the microcontroller. To precisely adjust the threshold, a variable resistor ($R_{pot}$) is used, and hysteresis is introduced to enhance noise resilience.

In this case, positive feedback is incorporated to ensure the output of the comparator saturates to either supply rail. To prevent the output from the opamp from loading the variable resistor, resistor $R_{hys}$ is included. The impact of $R_{hys}$ can be better understood by referring to Figure 4.12, where issues arise when $R_{hys} = 1$. To ensure that $R_{hys}$ does not affect $V_{th}$, the condition $R_{hys} >> R_{pot}$ must be satisfied.


**Figure 4.12:** Comparator opamp with hysteresis: (a) HIGH representation, and (b) LOW representation.

In the final step of the process shown in Figure 4.11, the PWM output from the comparator is inverted. This decision is based on the requirement for the voltage to be in phase with the current, rather than being out of phase by $\pi$ radians.

To determine the suitable voltage values for the ZCCD circuit, $V_{offset}$ is set to $V_{cc}/2$ for achieving a broad measuring range.

Moving on to $V_{cc}$, considering the voltage level for the HIGH state, digital ICs and microcontrollers commonly operate at either $3.3V$ or $5V$. However, it is important to note that the TMS320F28379D chip has a tolerance of only $3.3V$ [39]. Therefore, to ensure compatibility and proper functioning of the TMS320F28379D chip, $V_{cc}$ is set to $3.3V$.

Additionally, for safety reasons, the microcontroller is remotely integrated with the PCB, potentially over distances exceeding $1m$. To address concerns related to electromagnetic interference (EMI) and latency, optical fibers are used for communication between the microcontroller and the ZCCD circuit. By utilizing optical fibers, EMI issues, and latency are effectively mitigated.

Moreover, as optical fibers transmit light instead of voltage, the PCB has the flexibility to choose either $3.3V$ or $5V$ as the voltage level for the HIGH state. In this design, $5V$ is selected to provide larger quantization levels, enhancing the comparator's ability to distinguish signals from noise interference.

To validate the functionality of the ZCCD circuit, an LTSpice model was constructed. The circuit, along with the corresponding results depicting the current through the secondary coil and the output of the inverter, is illustrated in Figure 4.13.

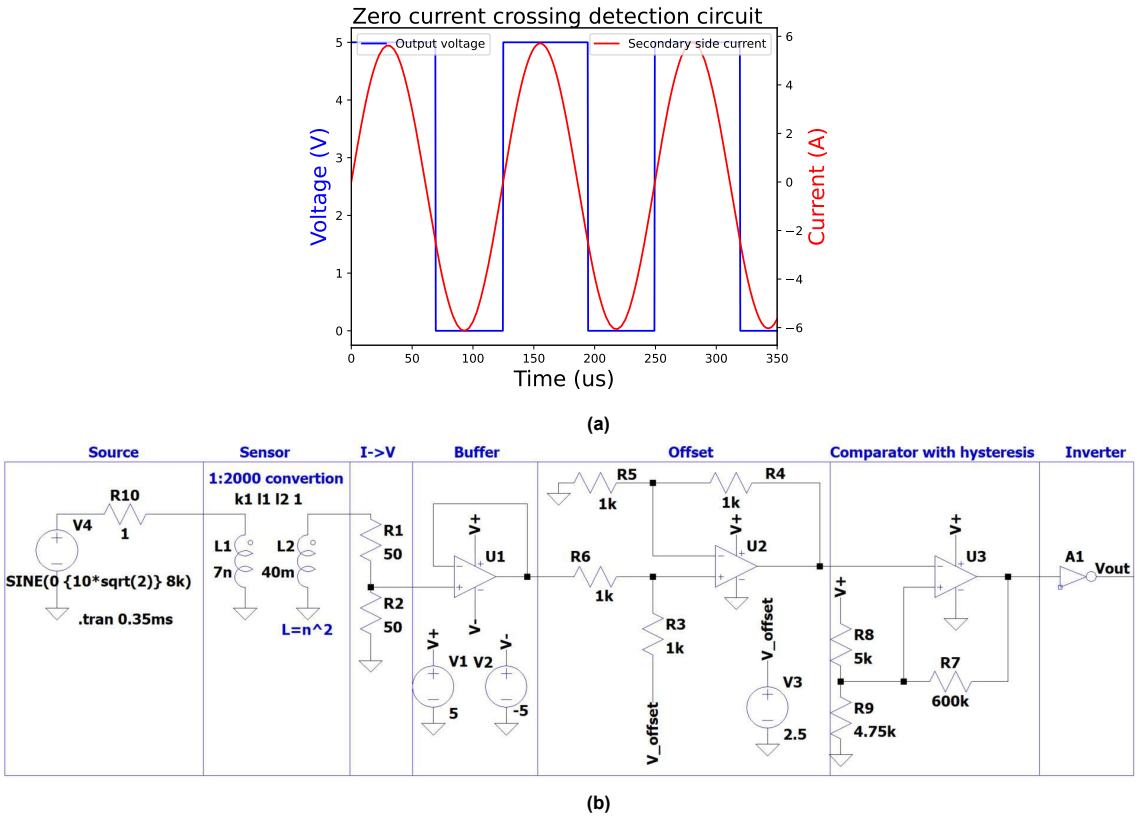



**Figure 4.13:** LTspice model of the ZCCD depicting the: (a) simulation result, and (b) simulation setup.

Upon examination, it is evident that during the transition from a negative to a positive current value, the rising edge occurs precisely at $0$. However, in the case of the transition from positive to negative, a falling edge is generated, though not precisely at the exact moment when the current reaches zero. This behavior is influenced by the presence of $R_{hys}$, even though the condition $R_{hys} >> R_{pot}$ has been satisfied. The hysteresis resistor is necessary to eliminate multiple small transitions before the final transition. A Texas Instruments reference article [38] demonstrates how the inclusion of a hysteresis resistor eliminates the additional small pulses, resulting in a single pulse without any extraneous fluctuations. Therefore, this effect will be present in the actual PCB.

Fortunately, this is not a cause for concern as the rising edge is chosen as the trigger to enable the PWM signals from the microcontroller, ensuring synchronization with the secondary side current. Since the MOSFET PWM duty cycle is determined by the internal counter in the microcontroller, it will consistently remain in phase with the current.

In conclusion, the schematic design for the ZCCD circuit is now complete. The routing method is a crucial aspect to consider when designing the PCB, and this will be discussed in the forthcoming section.

## 4.2. Understanding high-frequency energy transfer in PCB routing

This section draws from a seminar conducted by Rick Hartley on proper grounding techniques [26]. It begins by addressing common misconceptions related to energy transfer in high-frequency circuits. Firstly, it is crucial to understand that energy is predominantly carried by the electric and magnetic fields, rather than the copper trace itself [26]. Secondly, energy propagates through the dielectric space between traces and planes [26]. The subsequent sub-sections delve deeper into these statements, providing explanations for a better understanding.

### 4.2.1. Energy storage in electric and magnetic fields

In circuits operating at higher frequencies, the majority of energy associated with a current flow is stored in the electric and magnetic fields rather than within the copper trace itself. The time-varying current generates a magnetic field, as governed by Ampere's law, which in turn induces an electric field according to Faraday's law of electromagnetic induction. These interconnected electric and magnetic fields collectively store most of the energy.

It's worth noting that at these frequencies, the energy storage contribution of copper traces is limited due to the skin effect [26]. This effect causes the current to predominantly flow closer to the surface of the conductor rather than throughout its entire cross-section. As a result, the primary energy storage occurs in the electric and magnetic fields surrounding the traces themselves. Nevertheless, copper traces still function as effective waveguides, guiding the energy along their designated paths [26].

Each trace in the circuit produces its electromagnetic field, encompassing both the signal and its return path. When other signals are nearby, unintended coupling between adjacent traces can occur, leading to energy transfer between them. Please refer to Figure 4.14(a) for a visual representation of this phenomenon. To mitigate this issue, it is crucial to increase the spacing between the traces, as demonstrated in Figure 4.14(b).

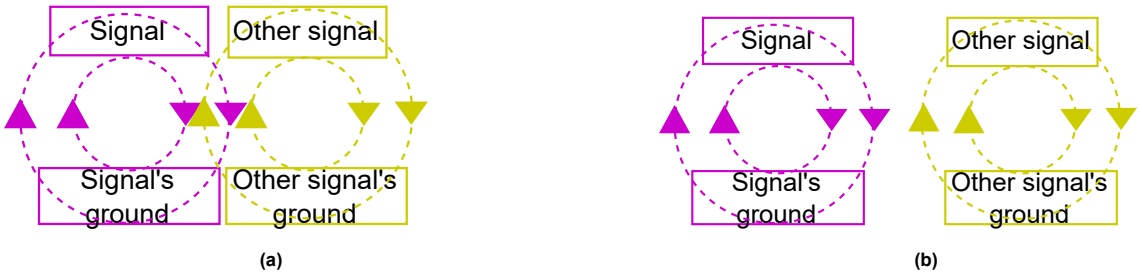



**Figure 4.14:** Simplified illustration of magnetic field coupling between traces: (a) interference due to proximity, and (b) no interference due to increased trace separation.

This phenomenon, known as cross-talk, occurs when energy is inadvertently exchanged between traces. Therefore, it is crucial to maintain a sufficient distance between traces to minimize cross-talk.

### 4.2.2. Energy travels through the dielectric space in high frequencies.

In high-frequency circuits, energy travels through the dielectric space surrounding transmission lines. This statement relates to the characteristic impedance of a transmission line. Figure 4.15 depicts a lumped model of a transmission line, and its characteristic impedance is given by Equation (4.12) [30]. It is important to acknowledge that this equation is not entirely accurate as it neglects dispersion and skin effect losses. However, for this thesis, this simplified general model will be utilized.

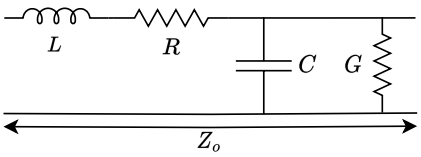



**Figure 4.15:** Simplified lumped characteristic model of a transmission line

$$Z_o = \sqrt{\frac{R + j\omega L}{G + j\omega C}} \tag{4.12}$$

From Equation 4.12

- $L$ is the series inductance, representing the total self and mutual inductance of both conductors[30].
- $C$ is the shunt capacitance, due to the proximity of the two conductors [30]
- $R$ is the resistance, due to the finite conductivity of both conductors [30].
- $G$ is the shunt conductance, due to dielectric loss in the material between the conductors [30].

At high frequencies, the parameters $R$ and $G$ can be disregarded, as the current prefers to flow through the path with the lowest impedance. This typically occurs where the capacitance is highest or the inductance is lowest, as shown in Equation (4.12). Understanding the significance of capacitance is crucial for comprehending how energy travels through the dielectric. To illustrate this, Professor Todd Hubing experimented, and a high-level model of the setup is depicted in Figure 4.16(a), while the current distribution through the strap is shown in Figure 4.16(b). At DC, all the current flows through the ground strap due to its shorter distance and dominant resistance. However, in the MHz frequency range, almost no return current flows through the ground strap. Instead, it chooses the shielding inside the coaxial cable. This behavior arises from the fact that the dielectric ($\epsilon_r$) of the coaxial cable is greater than the $\epsilon_r$ of the air between the signal and ground strap. The larger $\epsilon_r$ leads to a larger capacitance ($C$) and a lower characteristic impedance ($Z_0$) [6].

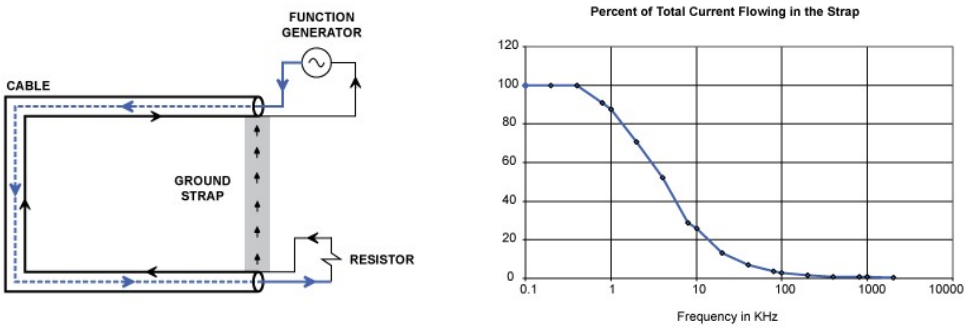



**Figure 4.16:** The return current distribution in a short connection between the ends of a coaxial cable with a ground strap:(a) an illustration of the setup, and (b) a graph depicting the distribution of current flowing through the ground strap[6].

The validity of this experiment was confirmed through electromagnetic simulation (Figure 4.17 [2]). Please note that the table displaying the magnitude in Figure 4.17 is unreadable, but this is how it was presented in the original article

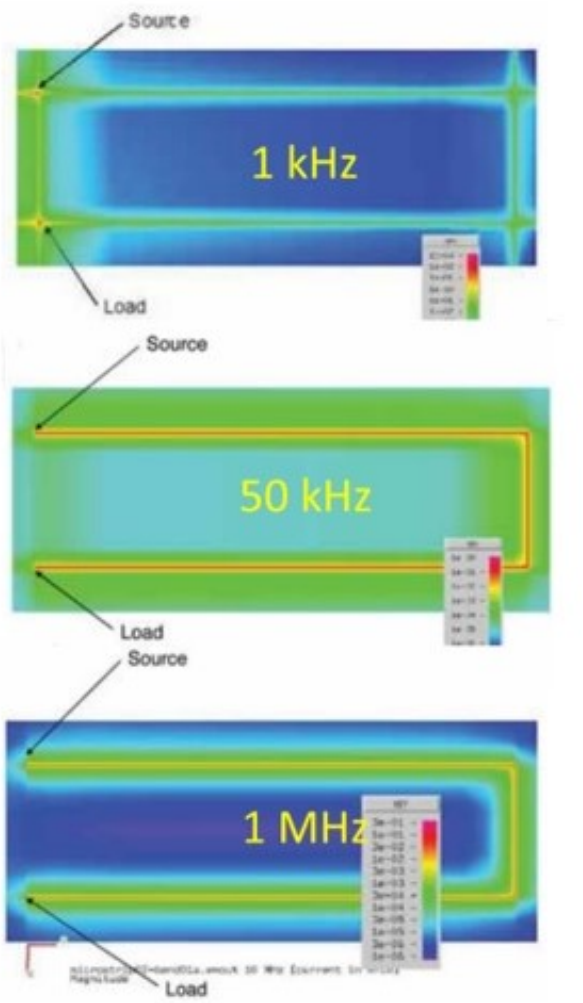



**Figure 4.17:** Conducted a simulation of the signal and return current in a microstrip using a proprietary IBM field solver [2].

Strategically placing a ground plane beneath the signal trace is an effective technique for keeping the return signal below the main signal, particularly at higher frequencies. This observation is corroborated by the findings presented in Figure 4.17, where the return current consistently remains beneath the signal trace. The inclusion of a solid ground plane beneath the signal trace effectively suppresses the propagation of electromagnetic waves around the PCB, minimizing the risk of unwanted electromagnetic interference. Consequently, in the PCB design, the dedicated inner layer 2 was reserved exclusively for accommodating the ground plane.

## 4.3. Key considerations in PCB routing design

The significance of having a solid ground plane beneath the high-frequency signal trace to minimize electromagnetic interference (EMI) has been highlighted in the previous subsection. However, PCB routing involves several critical factors that contribute to the overall design. While these factors are extensive enough to be the focus of an entire thesis, this section will provide a brief overview of three key design considerations: minimizing parasitic inductance, ensuring sufficient copper for effective heat dissipation, and maintaining signal integrity of analog signals against digital signals.

### 4.3.1. Minimizing trace parasitic inductance

Parasitic inductance in PCB designs can introduce various issues, such as PWM signal distortion and power delivery instability. It will be shown mathematically what can be done to minimize this parasitic

inductance. To simplify calculations, the scenario considered in this analysis involves a single signal trace positioned above a solid ground plane without adjacent traces. The resulting modeled signal and ground return path is depicted in Figure 4.18, and the inductance can be calculated using Equation (4.13) [17].

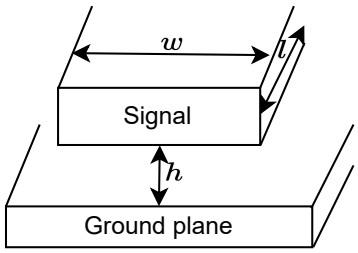



**Figure 4.18:** Signal and ground plane representing return path.

$$\begin{aligned} L &= \frac{60l}{v_0} \ln\left[\frac{8h}{w} + \frac{w}{4h}\right] && \text{for } \frac{w}{h} \leq 1 \\ L &= \frac{1200l}{v_0}\left[\frac{w}{\frac{w}{h}+1.393+0.667\ln\left(\frac{w}{h}+1.444\right)}\right] && \text{for } \frac{w}{h} > 1 \end{aligned} \tag{4.13}$$

The relationship between inductance and the parameters of the microstrip, such as propagation speed ($v_0$), trace length ($l$), trace width ($w$), and distance from the ground plane ($h$), is defined by Equation (4.13). While the impact of $l$ on inductance is straightforward, the influence of $w$ and $h$ is less obvious. To gain a deeper understanding of these relationships, plots were generated to visually demonstrate the variation of inductance with different values of $h$ and $w$, as depicted in Figure 4.19.

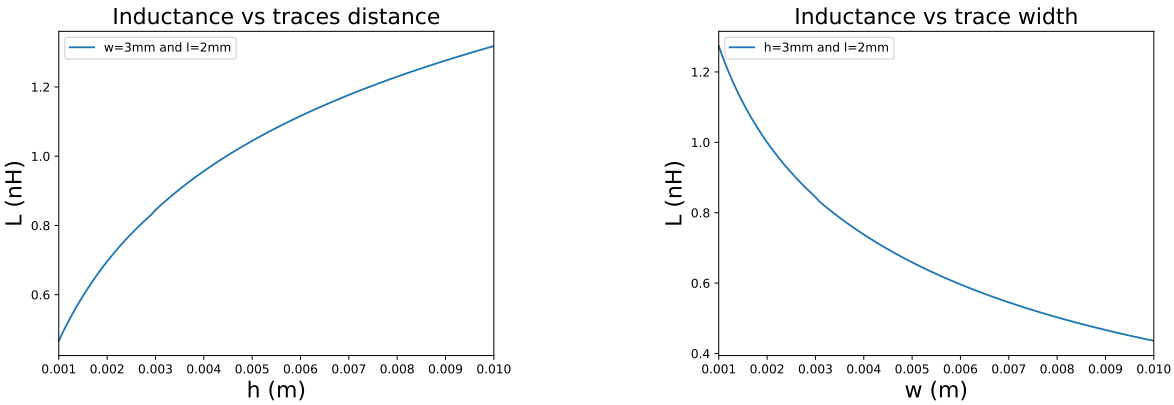



**Figure 4.19:** The inductance of a signal trace above a ground plane was examined in two scenarios: (a) the inductance of the trace was calculated against varying distances between the signal trace and return path, and (b) the inductance of the trace was calculated against different trace widths.

To understand the relationship between flux and inductance, it is important to consider the following equation, as it will be relevant for understanding the topic at hand.

$$\begin{aligned} \phi &= \iint_S \vec{B} \cdot \, \mathrm{d}\vec{S} \\ L &= \frac{\phi(i)}{i} \end{aligned} \tag{4.14}$$

Increasing $l$ generates a stronger magnetic field, leading to a larger magnetic flux ($\phi$) and, consequently, a higher inductance ($L$). Moreover, understanding the relationship between self and mutual inductance is crucial when dealing with two inductors with $h$ and $w$, as demonstrated in Equation (4.15).

This equation provides a simplified representation without considering frequency elements. Here, $L_{aid}$ represents the combination of magnetic fields produced by the two inductors to create a stronger field, while $L_{oppose}$ indicates that the fields oppose each other, resulting in a weaker field. In this equation, $L_1$ and $L_2$ refer to the self-inductance of each inductor, and $L$ is the sum of both self and mutual inductance.

$$\begin{aligned} L_{aid} &= L_1 + L_2 + 2M \\ L_{oppose} &= L_1 + L_2 - 2M \end{aligned} \tag{4.15}$$

When current flows in opposite directions through $h$, their magnetic fields cancel each other out, leading to the sum inductance $L_{oppose}$. As the traces move closer to each other, $M$ will increase, causing a decrease in $L_{oppose}$, as shown in Figure 4.19(a). Meanwhile, for $w$, it's important to keep in mind that the current in a wire is a sum of electrons, each generating its magnetic field. Because all these electrons move in the same direction, their magnetic fields combine, represented by $L_{aid}$. As the distance between current elements in the conductor increases with a larger $w$, mutual inductance decreases, leading to a smaller inductance, as illustrated in Figure 4.19(b).

### 4.3.2. Thermal considerations

The thermal aspects of PCB design are important in ensuring safety. When current flows through the copper traces, conduction losses occur, leading to a temperature rise. If this temperature increase becomes significant, it can result in excessive thermal stress and thermal runaway, potentially causing combustion. To prevent such scenarios, strategies for managing thermal stress are essential. The minimum required copper area for a given current can be determined using the IPC-2221 standard, and the corresponding equation is provided in Equation (4.16) [29], where $A$ represents the minimum required copper area cross-section in $mils^2$.

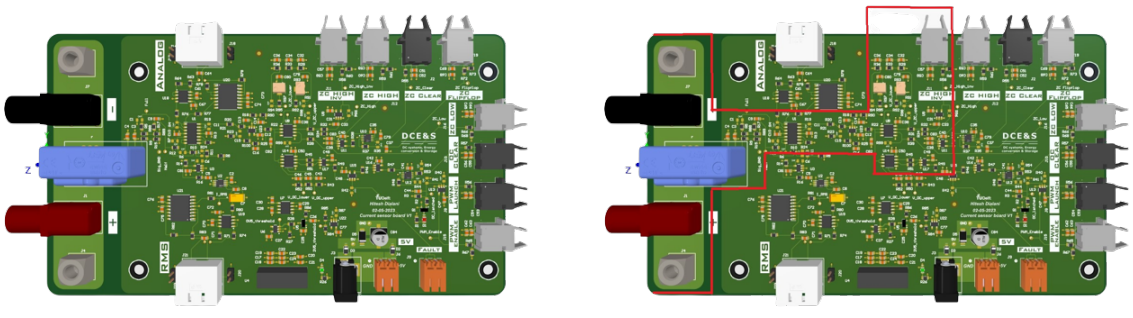
$$\begin{aligned} A &= \left( \frac{I}{k(\Delta T)^{0.44}} \right)^{1/0.725} \\ k &= \begin{cases} 0.048 \text{ (external layers)} \\ 0.024 \text{ (internal layers)} \end{cases} \end{aligned} \tag{4.16}$$

A smaller value of $k$ for the internal layer indicates a greater need for a larger copper area to effectively dissipate the same amount of current. This is because the outer layer of the PCB has the advantage of radiating heat into the surrounding air for cooling, whereas the inner traces lack this benefit. According to [32], it is expected that this PCB will handle a maximum current of $25Arms$. To determine the minimum required area, a temperature rise of $20°C$ was initially assumed, leading to an estimated area of $1463mils^2$ for the top external layer.

There are two options available to meet the minimum required area: adjusting the trace width or the copper thickness. However, it is generally preferable to use the lowest possible copper thickness to avoid significantly increasing the overall cost of the PCB since the copper width does not affect the price. For instance, Euro-circuits' standard copper thickness is $18\mu m$, which corresponds to a width of $36mm$. To prevent unnecessary enlargement of the PCB, both the top and bottom layers will have a copper width of $18mm$ instead of having only one layer with a width of $36mm$. This approach effectively increases the copper thickness without incurring additional costs. Additionally, a safety factor of 2 was taken into consideration to ensure reliable operation.

### 4.3.3. Ensuring analog signal integrity in the presence of digital interference

Ensuring the integrity of the analog signal requires careful consideration of potential EMI originating from digital signals. The rapid transitions between $0V$ and $Vcc$ states in digital signals can introduce distortion to the analog signal by generating significant $dv/dt$. Therefore, it is crucial to isolate all digital signals starting from the comparator to prevent interference with any signals preceding the comparator. Taking into account all the aforementioned design considerations, the PCB shown in Figure 4.20 illustrates the process outlined in Figure 4.11 (see Figure 4.20(b)). It is important to note that this thesis does not delve into topics such as overcurrent, RMS, real-time analog measurement, and alternative methods for zero-crossing detection. However, these aspects are present in the final PCB design.

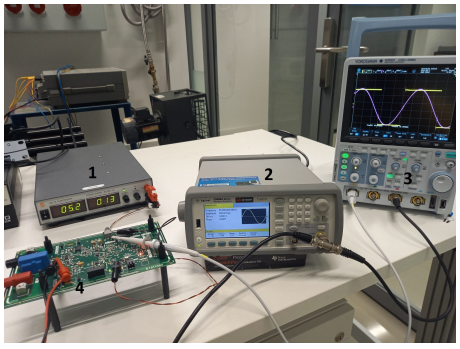


(a) (b)

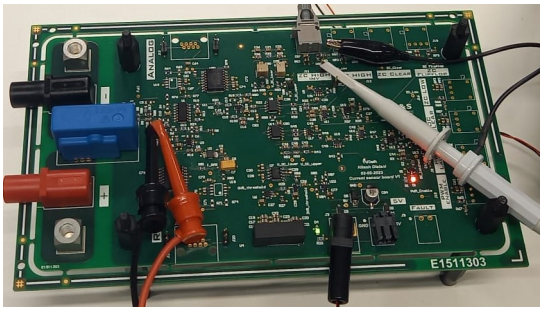
**Figure 4.20:** The Altium model of the designed PCB for zero current crossing detection (ZCCD) is presented in two views: (a) the full PCB, and (b) a close-up view highlighting the relevant section dedicated to ZCCD, indicated by a red box.

## 4.4. Validation of ZCCD hardware

After designing and producing the ZCCD PCB, it requires testing to verify its functionality. The testing procedure is outlined in this section, with the test setup depicted in Figure 4.21(a). To simplify the initial testing and confirm the functionality of the ZCCD, a waveform generator will be used. The waveform generator supplies the measured voltage signal ($V_{measured}$) as shown in Figure 4.11. The remaining steps in the testing process remain consistent, enabling effective validation of the ZCCD feature. The components used in the testing setup are listed below, corresponding to the numbering in Figure 4.21(a). It's worth noting that not all components shown in Figure 4.21(b) were populated, as they were unnecessary for ZCCD validation, avoiding unnecessary assembly for potential revisions.




(a)

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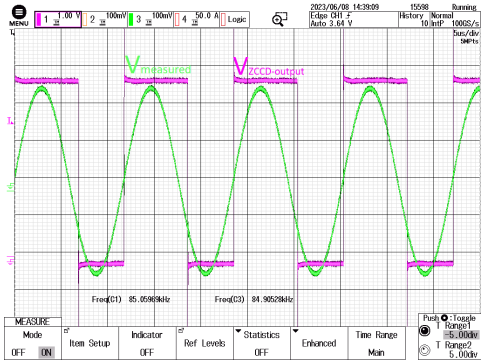



(c)

**Figure 4.21:** Test setup for validating zero current crossing detection (ZCCD). (a) entire test setup, (b) PCB under test, and (c) waveforms captured from the oscilloscope with corresponding labels.

1. The Delta Elektronika ES-030-10 power supply provides $5V$ voltage to the ZCCD PCB.

2. The Keysight 33600A waveform generator generates an $85kHz$ sinusoidal test waveform to validate the ZCCD.
3. The Yokogawa DLM3034 oscilloscope measures both the input test waveform and the square-wave output of the ZCCD PCB.
4. The ZCCD PCB is equipped with measurement probes at the output.

After successfully operating the ZCCD circuit, the next step is to integrate it with the microcontroller for synchronization. This synchronization involves aligning the microcontroller with the rising edge of the ZCCD hardware. To achieve this, a software implementation will be employed, as the microcontroller generates the PWM signals. The details of this software implementation will be discussed in the following section.

## 4.5. Synchronization software between microcontroller PWM and ZCCD rising edge

The software implementation can be done using either Simulink or C/C++. Although C/C++ offers greater versatility and flexibility for handling complex systems and making modifications, the DCES department predominantly utilizes Simulink for programming their microcontrollers. Hence, in this case, Simulink will be the chosen software for implementation.

There are two main types of PWM signals: asymmetrical and symmetrical PWM. Symmetrical PWM is preferred due to its ability to generate fewer harmonics in the output current and voltage [28]. While a complete proof demonstrating this preference is beyond the scope of this thesis, readers interested in more detailed information and practical experimentation on both asymmetrical and symmetrical PWM can refer to [28]. For this thesis, synchronized PWM will be utilized, and the synchronization software follows the state diagram depicted in Figure 4.22.

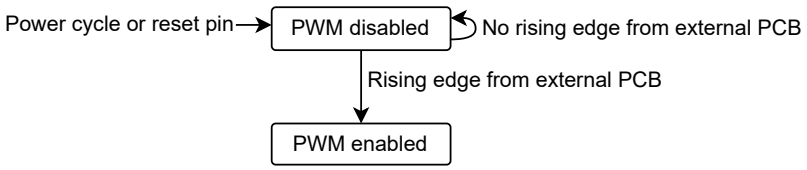
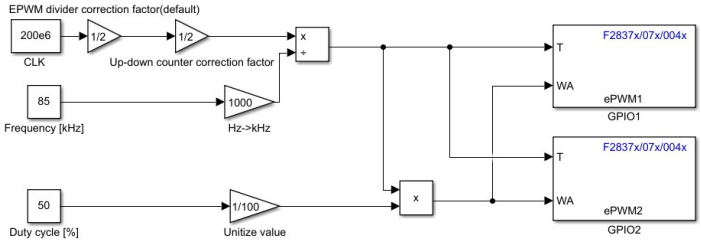
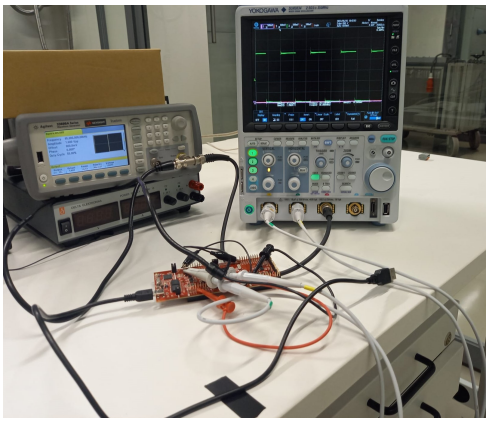



**Figure 4.22:** State diagram illustrating the functionality of the synchronization software.

The microcontroller offers the advantage of utilizing the digital compare block, which enables swift disabling and enabling of PWM signals [39]. To validate the functionality of the synchronization software, a test setup is devised, incorporating a function generator as an external source. The setup and the programmed software are illustrated in Figure 4.23. In Figure 4.23(b), the microcontroller is not powered on, while the external signal generator sends a PWM signal to the microcontroller. In Figure 4.23(c), the microcontroller is powered on and instantly synchronized, as evident from Figure 4.23(d). The output is not only the synchronized PWM signal but also the inverted PWM signal.




(a)



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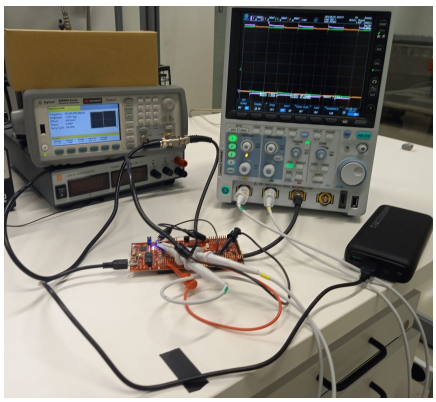
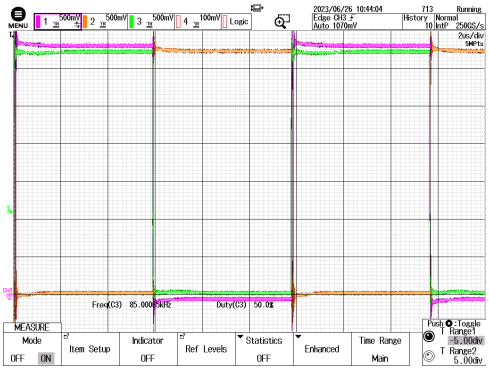
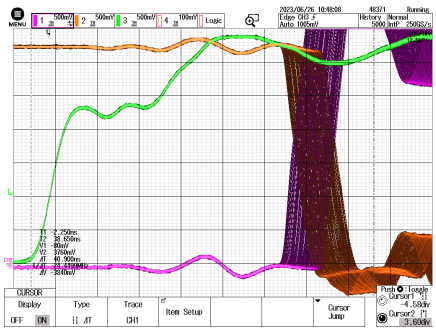


(c)



(d)



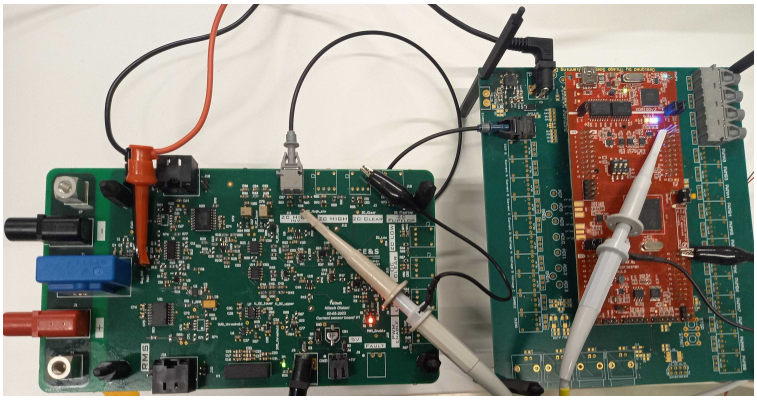
(e)

**Figure 4.23:** Test setup for validating the synchronization software: (a) implementation of Simulink software in the microcontroller, (b) test setup for synchronization software with microcontroller deactivated, (c) test setup for synchronization software with microcontroller activated, (d) waveforms of the synchronization setup showcasing the reference signal and complementary PWM output, and (e) zoomed-in view of the waveforms from the d.

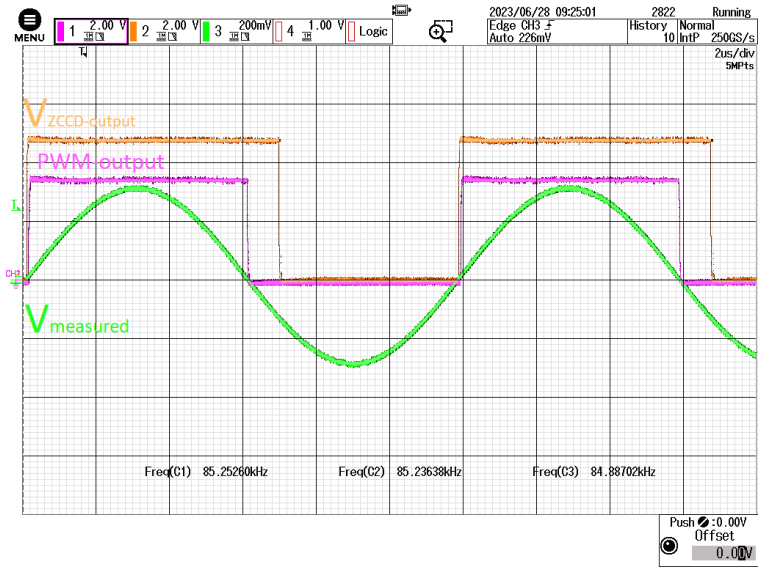
Based on the observed results, it is evident that the microcontroller's PWM is effectively synchronized with the external PWM. Another crucial aspect to consider is latency looking at Figure 4.23(e) indicates a latency of less than $< 50ns$. The next section will conclude this chapter by integrating both the ZCCD hardware and the synchronization software.

## 4.6. Validation of the entire synchronization system

The validation of the entire synchronization system was conducted using the setup depicted in Figure 4.24(a).



(a)




(b)

**Figure 4.24:** Validation of the complete synchronization system: (a) setup includes the ZCCD PCB receiving a sinusoidal input signal representing an AC source. The output of the ZCCD PCB is connected to a voltage probe and linked to the signal processing board at DCES via an optic fiber. The PWM output of the microcontroller is also connected to a voltage probe, and (b) measurement waveforms are captured on the oscilloscope, featuring the input reference signal and output signals with corresponding labels.

Upon analyzing the measurement waveforms depicted in Figure 4.24(b), it becomes apparent that the synchronization mechanism operates effectively. This validation affirms that the synchronization system successfully meets the specified requirements, ensuring its reliable functionality.

# 5

# Wireless communication

This chapter focuses on the validation of wireless communication. It covers the necessary software design for operating the nRF24L01+ module as both a transmitter and receiver. Additionally, hardware implementation measures are demonstrated to enhance communication reliability.

## 5.1. Theory of wireless communication

To comprehend wireless communication, a basic understanding of the underlying physics is necessary. Electromagnetic waves propagate through space, generated by the motion of electric charges. This motion produces changing electric and magnetic fields that give rise to the propagation of electromagnetic waves. As discussed earlier in the section on routing, traces on a PCB can guide these waves along transmission lines, while antennas, in conjunction with traces, can radiate them through free space. Unlike traces, which operate based on circuit theory and require a return path, antennas operate with electromagnetic radiation and do not necessitate a return path. The concept of a return path does not apply to electromagnetic waves, as they exist solely as radiated energy, as demonstrated by the sun's emissions. For a visual representation of the general structure of transmitting and receiving antennas, please refer to Figure 5.1.

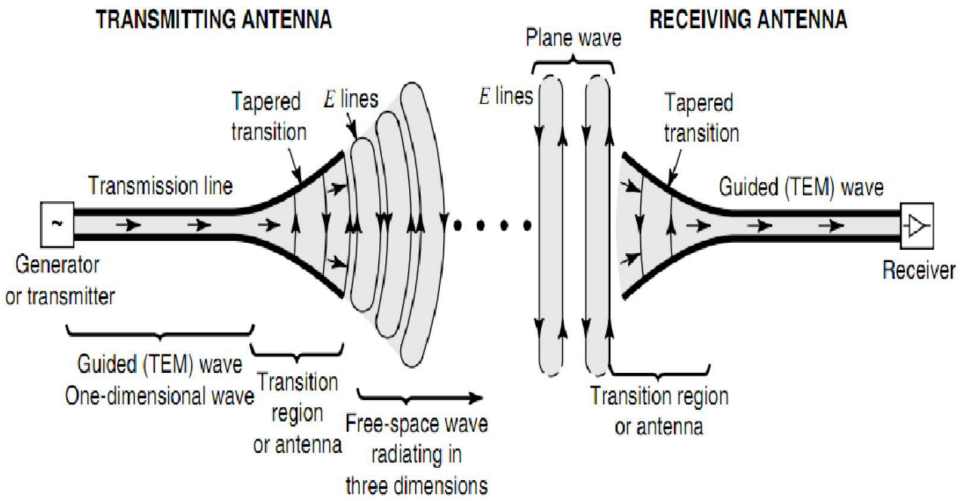



**Figure 5.1:** Structure of transmitting and receiving antennas [1].

## 5.2. Background information for nRF24L01+ module

This section provides the essential information required for operating the nRF24L01+ module, specifically focusing on the relevant parameters from its datasheet that are necessary for ensuring proper wireless communication. These details apply to any microcontroller and serve as general guidelines.

### 5.2.1. Reasoning for picking the nRF24L01+ module

To establish wireless communication between the microcontroller, the nRF24L01+ module from Nordic Semiconductor was selected (see Figure 5.2). This decision was based on several factors, including its affordability, dual functionality as a transmitter (TX) and receiver (RX), high reliability, and widespread adoption in hobbyist projects, particularly in the field of drones. The extensive user community associated with the nRF24L01+ module played a crucial role in its selection, as it provides a wealth of documentation and numerous working examples to address any potential communication challenges.

One of the main challenges encountered during this thesis was the development of C software specifically tailored for the Texas Instrument TMS320F28379D microcontroller for wireless communication. Initially, Simulink was considered for software development, but progress was hindered due to the scarcity of online resources and examples with SPI and wifi modules. In contrast, a wealth of C/C++ code examples for various microcontrollers such as Arduino, STM32, and Raspberry Pi facilitated the software development process, making it easier to overcome the hurdles.

(a) (b)

**Figure 5.2:** nRF24L01+ module with duck antenna: (a) assembled, and (b) disassembled.

### 5.2.2. nRF24L01+ module functionality

The nRF24L01+ module operates within the 2.4 GHz worldwide ISM frequency band, which is open for personal use. While this frequency range offers versatility, it also introduces challenges in real-world applications. Other devices operating at the same frequency can potentially cause interference by transmitting erroneous data to the receiver. Additionally, malicious actors may intercept the transmitted data and intentionally send incorrect values to the receiver. To address these risks, the nRF24L01+ module incorporates several security features.

Users can select the specific operating frequency within the range of $2.400GHz$ to $2.525GHz$ [35]. Furthermore, data transmission is encrypted using Gaussian frequency-shift keying (GFSK) [35], and a user-defined password of 3-5 bytes can be implemented [35]. The number of transmitted bytes can also be adjusted, ranging from 1 to 32 bytes. It is crucial for successful two-way communication that these settings remain identical between the transmitter and receiver.

The hardware design aspect of the nRF24L01+ module will not be discussed in this thesis. However, it is important to note that the module utilizes the Serial Peripheral Interface (SPI) protocol [35].

By incorporating these security measures and offering customizable settings, the nRF24L01+ module enhances data integrity and confidentiality in wireless communication applications.

### 5.2.3. Different types of communication protocols

To understand the context of this thesis, a basic understanding of the SPI protocol is needed. Figure 5.3 provides an overview of the general communication protocols diagram, and where SPI belongs within it. To establish communication between two microcontrollers or between a microcontroller and external devices such as an SD card, sensor, or the nRF24L01+ module, a bidirectional exchange of information is necessary.

Serial protocols, including SPI, are preferred over parallel protocols because they utilize fewer wires, which remain the same regardless of the data size. The serial protocols can be further divided into synchronous and asynchronous types. Synchronous protocols, such as SPI, incorporate a clock signal along with the data transmission. On the other hand, asynchronous protocols do not have a clock signal and are commonly used for long-distance communication to prevent clock rate discrepancies caused

by the wire. Asynchronous protocols overcome this by including starting and stopping bits within the transmitted data.

While the nRF24L01+ module transmits data within the $2.4GHz$ frequency band, the SPI data is transmitted at a much slower rate, with a maximum of $5MHz$ [35]. Due to the synchronization requirements between the clock signal and data, it is important to keep the cable length connecting the microcontroller and the nRF24L01+ module relatively short. This helps to ensure proper timing and reliable communication between the devices.

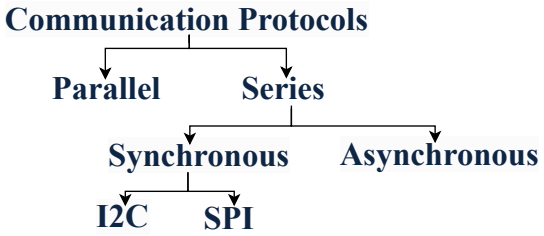



**Figure 5.3:** Positioning of SPI protocol within the general communication protocols diagram.

### 5.2.4. Relevant SPI information for nRF24L01+ module

To ensure successful SPI communication between the microcontroller and the nRF24L01+ module, several important considerations must be taken into account. This subsection covers key aspects, starting with the maximum data rate of $10MHz$ [35]. The SPI communication type involves different modes based on clock polarity (POL) and clock phase (PHA), each having two options. To determine the relevant modes, refer to Figure 5.4, focusing on the non-blacked-out lines. During SPI communication, the chip selects (CSN) should be set to LOW, and the clock signal (SCK) should be LOW in the idle state before and after communication, indicating a POL0 (clock low in idle) configuration. Additionally, observe the phase difference between the SCK and MOSI/MISO signals. In this case, there is a phase difference, resulting in a PHA1 (data captured on the trailing edge of the clock) configuration. Therefore, the nRF24L01+ module operates in the POL0PHA1 mode for SPI communication.

For a detailed explanation of each letter shown in Figure 5.4, refer to Table 5.1. While additional information is required for comprehensive communication with the nRF24L01+ module, such as configuring registers and specific SPI command bits, this thesis focuses on the top-level implementation. Readers seeking further information can refer to [35].

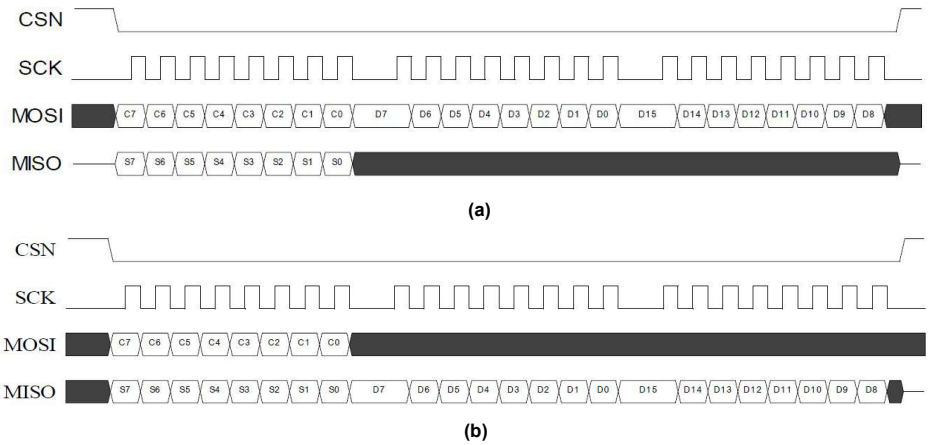



**Figure 5.4:** nRF24L01+ module SPI data transfer: (a) writing data, and (b) reading data [35].

## 5.3. Application and validation of wireless communication

In this thesis, the Texas Instruments TMS320F28379D microcontroller will be utilized for the final implementation. However, during the code development process, the Arduino Nano Atmel 8-bit AVR

**Table 5.1:** Abbreviation definition for nRF24L01+ module SPI commands [35].

| Abbreviation | Description |
|---|---|
| Cn | SPI command bit |
| Sn | STATUS register bit |
| Dn | Data Bit (Note: LSByte to MSByte, MSBit in each byte first) |

microcontroller was initially employed due to its easy-to-use programming interface and the availability of existing libraries for the nRF24L01+ module. Additionally, utilizing the Arduino allowed for the validation of self-written C code intended for the TMS320F28379D, demonstrating its effectiveness across different microcontroller architectures. The control state diagram for the nRF24L01+ module is displayed in Figure 5.5[35].

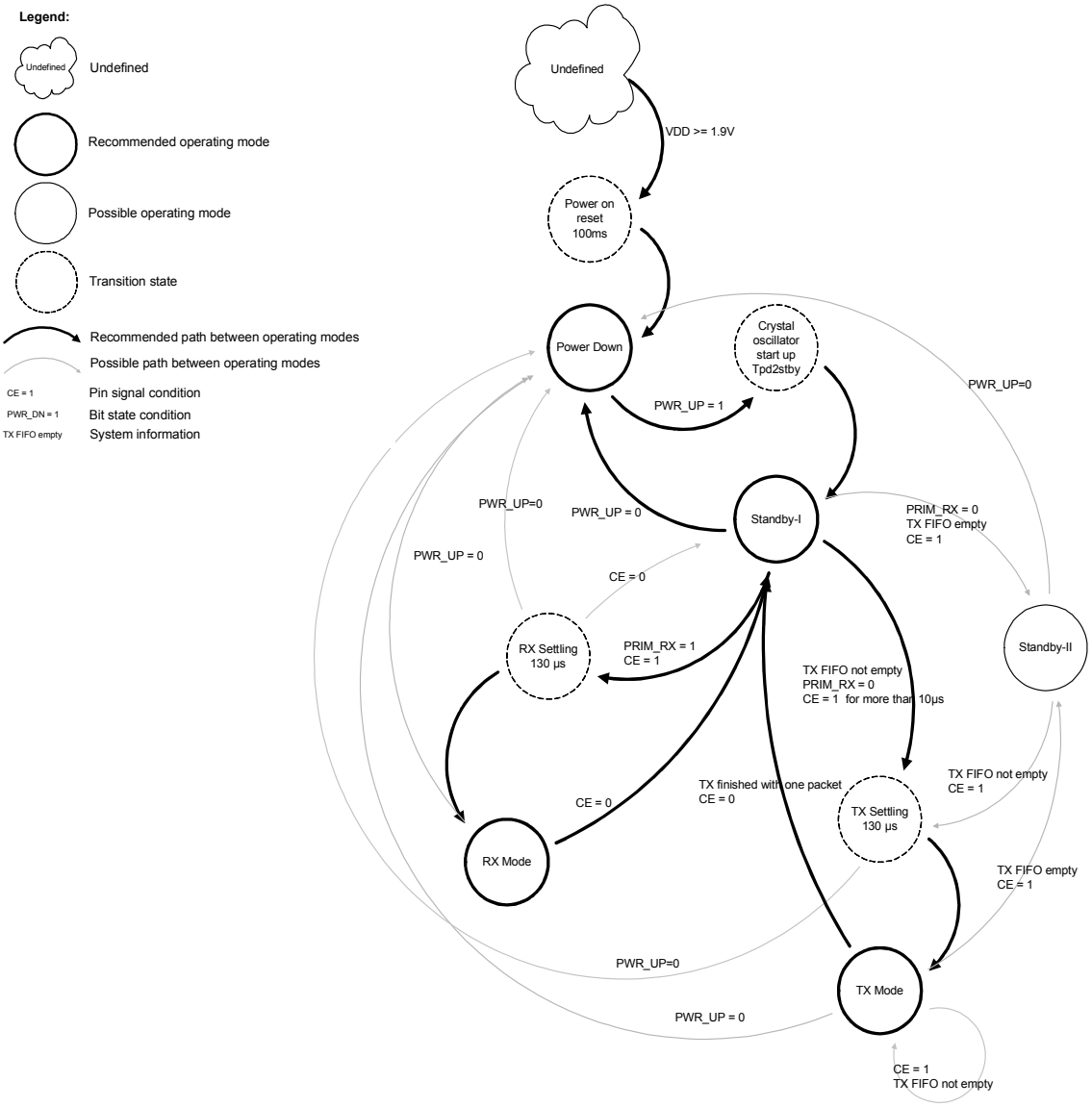



**Figure 5.5:** Full control state diagram of the nRF24L01+ module [35].

### 5.3.1. Validation of TX mode

In this subsection, the TMS320F28379D microcontroller serves as the transmitter, while the Arduino Nano microcontroller functions as the receiver. The nRF24L01+ module control state diagram presents

a complex system with various states and options, as depicted in Figure 5.5 [35]. Fortunately, not the entire system is required for TX validation. The relevant C code for transmitting data (TX code) closely follows the path outlined in Figure 5.6. Additionally, experimental results in Figure 5.7 demonstrate the successful execution of the transition phase.

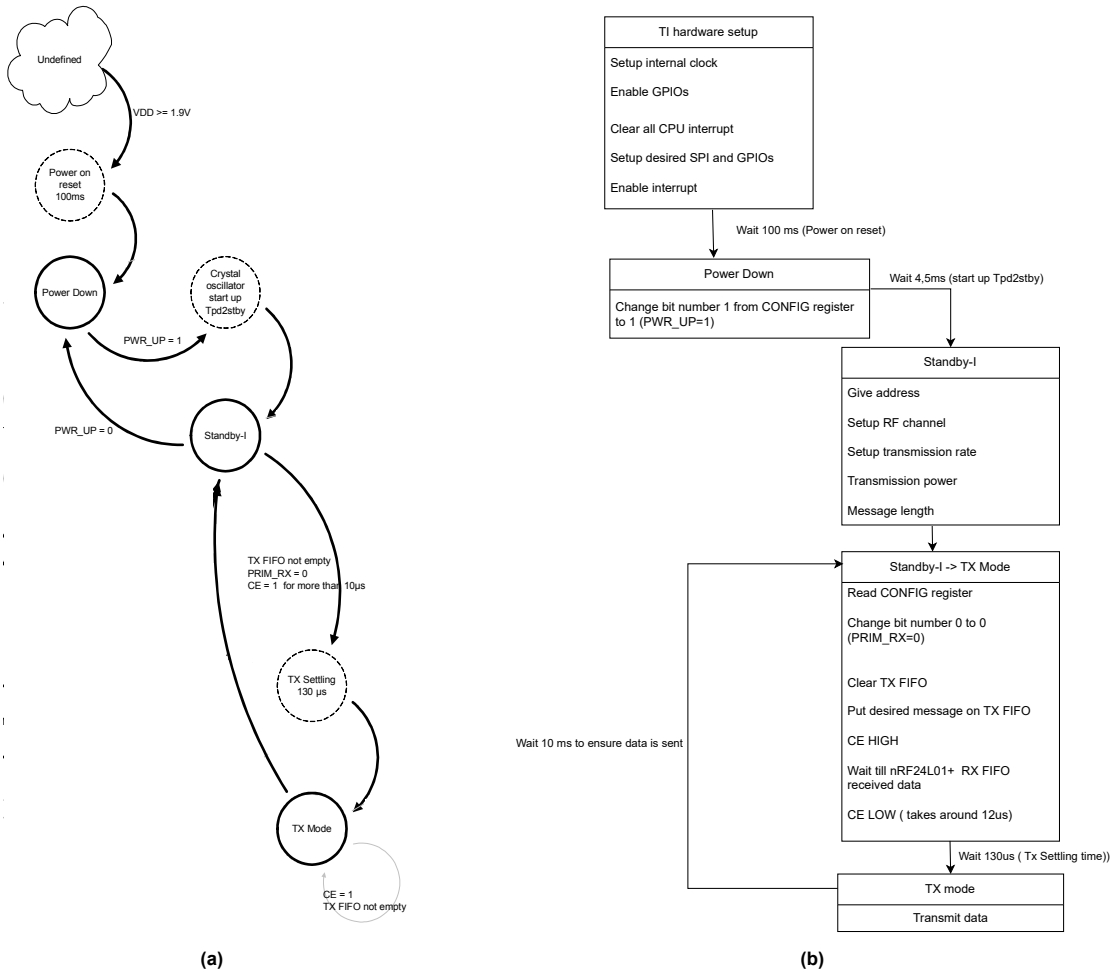



**Figure 5.6:** (a) Modified control state diagram relevant for TX portion [35], and (b) top-level C code implementation representing TX code.

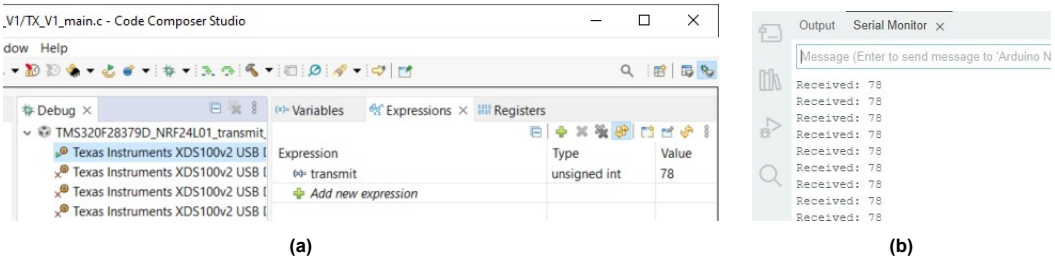



**Figure 5.7:** Validation of the nRF24L01+ module TX functionality: (a) TMS320F28379D microcontroller transmitting the value 78 using Code Composer, and (b) Arduino Nano microcontroller receiving the value 78 using Arduino IDE.

### 5.3.2. Validation of RX mode

In this subsection, the TMS320F28379D microcontroller serves as the receiver, while the Arduino nano functions as the transmitter. The relevant code for RX code implemented in C closely follows the path outlined in Figure 5.8. Furthermore, Figure 5.9 provides experimental results demonstrating the successful execution of the transition portion in the receiver code.

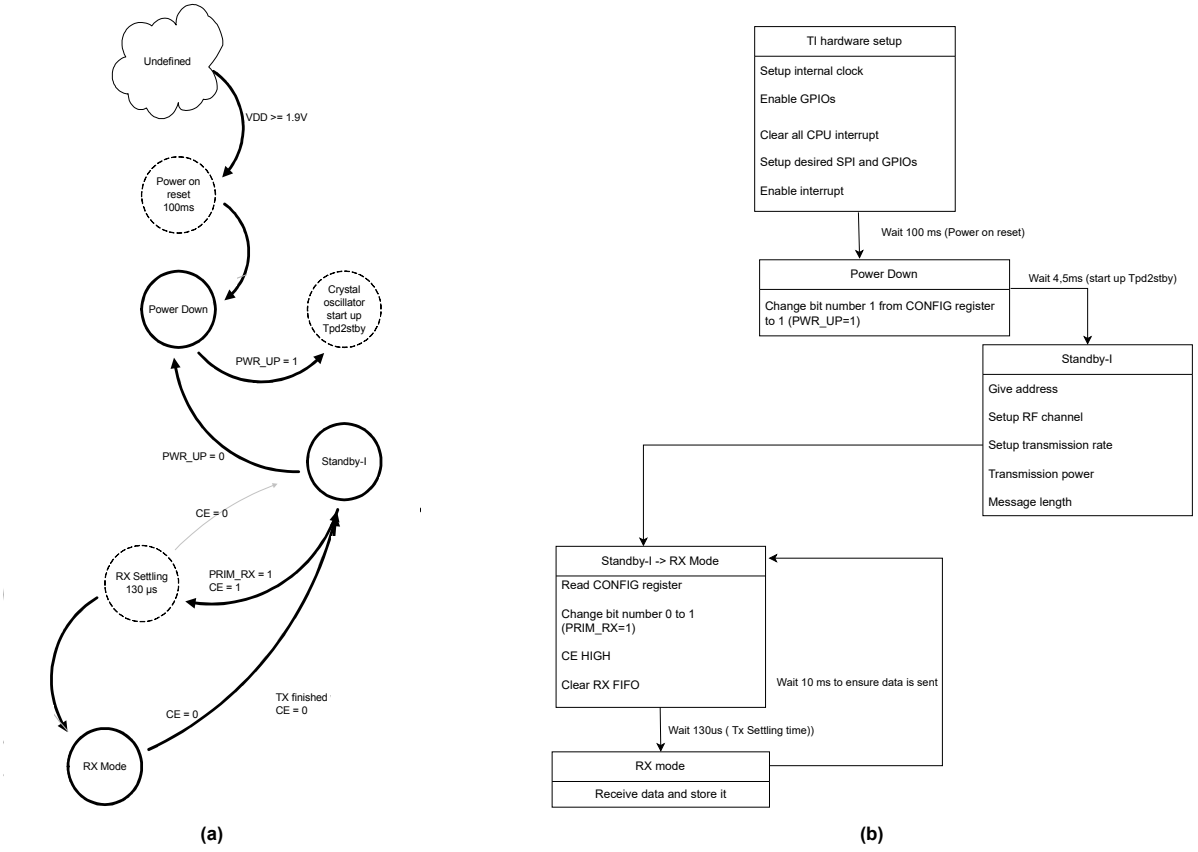



**Figure 5.8:** (a) Modified control state diagram relevant for RX portion [35] , and (b) top-level C code implementation representing RX code.

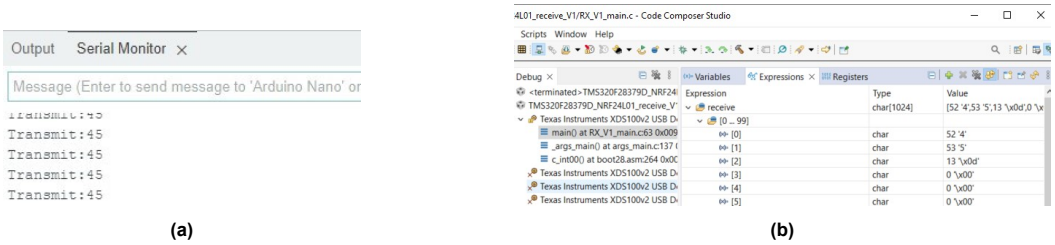



**Figure 5.9:** Validation of the nRF24L01+ module's RX functionality: (a) Arduino Nano microcontroller transmitting the value 45 using Arduino IDE, and (b) TMS320F28379D microcontroller receiving the value 45 using Code Composer.

### 5.3.3. Validation of TX and RX communication

In this subsection, the TMS320F28379D microcontroller was utilized as both the transmitter and receiver to conduct an experiment aimed at testing wireless communication capabilities. The objective of the experiment was to wirelessly transmit a value of ”3” across the room.

To simplify the setup process and save time, an alternative approach was adopted instead of setting up a second desktop with Codecomposer installed and configuring all the relevant settings. In this approach, the receiver was programmed via Flash, and the launchpad was configured to automatically execute the Flash code upon startup. This eliminated the need for the USB user code. The receiver launchpad only needs a power supply without requiring a PC. To validate the transmitted value without using a second PC, an LED was used instead. If the value ”3” was sent, the LED would turn on; any other value would not illuminate.

During the experiment, the transmitter state diagram depicted in Figure 5.6 and the receiver state diagram illustrated in Figure 5.8 were closely followed. The successful transmission and reception of the value ”3” wirelessly were verified by observing the activation of the LED.

## 5.4. Enhancing hardware stability

Ensuring reliable data transmission is vital for practical applications. To optimize the performance of the system, it is essential to address three key challenges that can significantly impact stability. These challenges encompass voltage drops caused by sudden changes in current demands, noise on the power line, and the influence of long wires connecting the RF24L01+ module to the microcontroller. For a more comprehensive understanding of the third challenge, please refer to Figure 5.10.

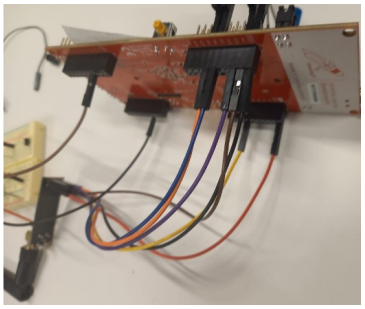


**Figure 5.10:** Illustration of a LaunchXL TMS320F28379D connected to the nRF24L01+ module for SPI communication.

### 5.4.1. Minimize possibility of accidental nRF24L01+ reset

The microcontroller GPIO should supply a steady $3.3V$ to power the nRF24L01+ module, ensuring its reliable operation. However, the actual voltage received by the nRF24L01+ module may vary due to the characteristics of the wire connection between the microcontroller and the module. This wire introduces parasitic effects, and a more realistic representation of this relationship is illustrated in Figure 5.11.

When the current consumption is constant, the voltage drop across the wire ($R_{wire}$) is minimal, and the inductance of the wire ($L_{wire}$) can be neglected, as stated in Equation (5.1). However, during state transitions, the current consumption fluctuates depending on the operational state, as outlined in Table 5.2 [35]. As a result, there is a voltage drop across the wire due to the presence of $L_{wire}$.

Of particular concern is if the voltage across the nRF24L01+ module falls below $1.9V$, as illustrated in Figure 5.5, the module may unintentionally enter power-down mode. This possibility underscores the importance of maintaining a steady $3.3V$ supply from the microcontroller GPIO to the nRF24L01+ module, ensuring its reliable and uninterrupted operation.

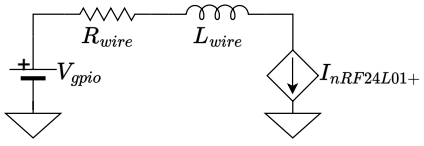



**Figure 5.11:** Circuit representation of a microcontroller GPIO connected to the nRF24L01+ module with wire parasitics present.

$$V = L\frac{di}{dt} \tag{5.1}$$

**Table 5.2:** Current consumption for each state of the nRF24L01+ module[35].

| nRF24L01+ module state | Current consumed |
|---|---|
| Power down | $900nA$ |
| Standby | $26uA$ |
| Transmitting | $13.5mA$ at 2Mbps |
| Receiving | $11.3mA$ at 2Mbps |

To ensure a stable voltage supply during state transitions and mitigate voltage drops caused by $L_{wire}$, the integration of capacitors is essential. This integration enhances stability, prevents unintentional power-down mode, and guarantees reliable operation of the system. Placing the capacitor near the nRF24L01+ module significantly reduces the voltage drop experienced during these transitions, thereby ensuring consistent and reliable operation.

During steady-state operation, the capacitor charges to the supply voltage, maintaining a stable voltage level. However, during transition states, the wire inductance absorbs a portion of the voltage, leading to the discharge of the capacitor. This discharge ensures a continuous voltage supply to the nRF24L01+ module, minimizing the voltage drop. When returning to steady-state operation, the GPIO pin voltage replenishes the capacitor, charging it back to the supply voltage.

The minimum capacitance required for effective voltage stabilization can be calculated using Equation (5.2), where $dt$ represents the rise time specific to the context of SPI protocol, not the PWM frequency [5]. The maximum allowable voltage drop during the transition is denoted as $dV$. Calculations indicate that the minimum required capacitance ($C_{min}$) is determined to be $4nF$. However, it is important to note that this value may not necessarily be the optimal choice for achieving the best performance.

$$I = C_{min}\frac{dV}{dt} \Rightarrow C_{min} = \frac{Idt}{dV} = \frac{13.5mA \cdot 30ns}{0.1V} = 4nF \tag{5.2}$$

The addition of a capacitor effectively mitigates the voltage drop issue; however, it introduces a new concern by forming a series RLC circuit, leading to ringing in the supply voltage waveform as depicted in Figure 5.12. This simulation captures the ringing behavior and is based on LTSpice, which will be presented shortly. It is crucial to take this ringing effect into account, particularly due to the nRF24L01+ module's maximum allowed supply voltage of $3.6V$ [35].

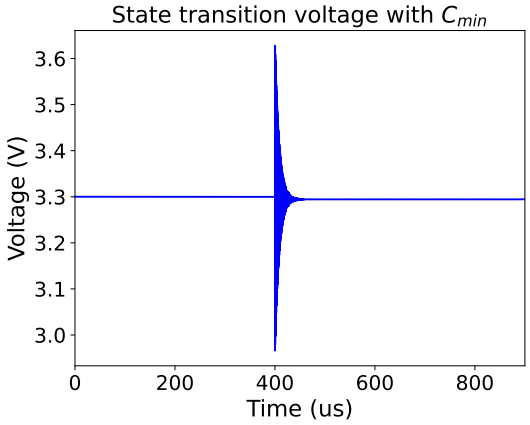



**Figure 5.12:** Voltage variation over the nRF24L01+ module during state transitions at $400\mu s$, with the addition of a $C_{min}$ decoupling capacitor on the power line.

To minimize the ringing effect, it is necessary to increase the damping factor of the series RLC circuit, which can be calculated using the formula presented in Equation (5.3), where $R$ and $L$ are constant and only $C$ can be adjusted. Therefore, to mitigate this effect, it is recommended to increase the value of $C$. The derivation of Equation (5.3) is given in Appendix A.9.

$$\zeta = \frac{R}{2}\sqrt{\frac{C}{L}} \tag{5.3}$$

The impact of the chosen decoupling capacitor on state transitions can be observed in the LTSpice simulation results shown in Figure 5.13. It is worth noting that the values assigned to parasitic effects and current consumption by the nRF24L01+ module are approximations. In the event of power-off occurrences during operation, it is recommended to adjust the capacitance value by increasing it to ensure proper functionality.

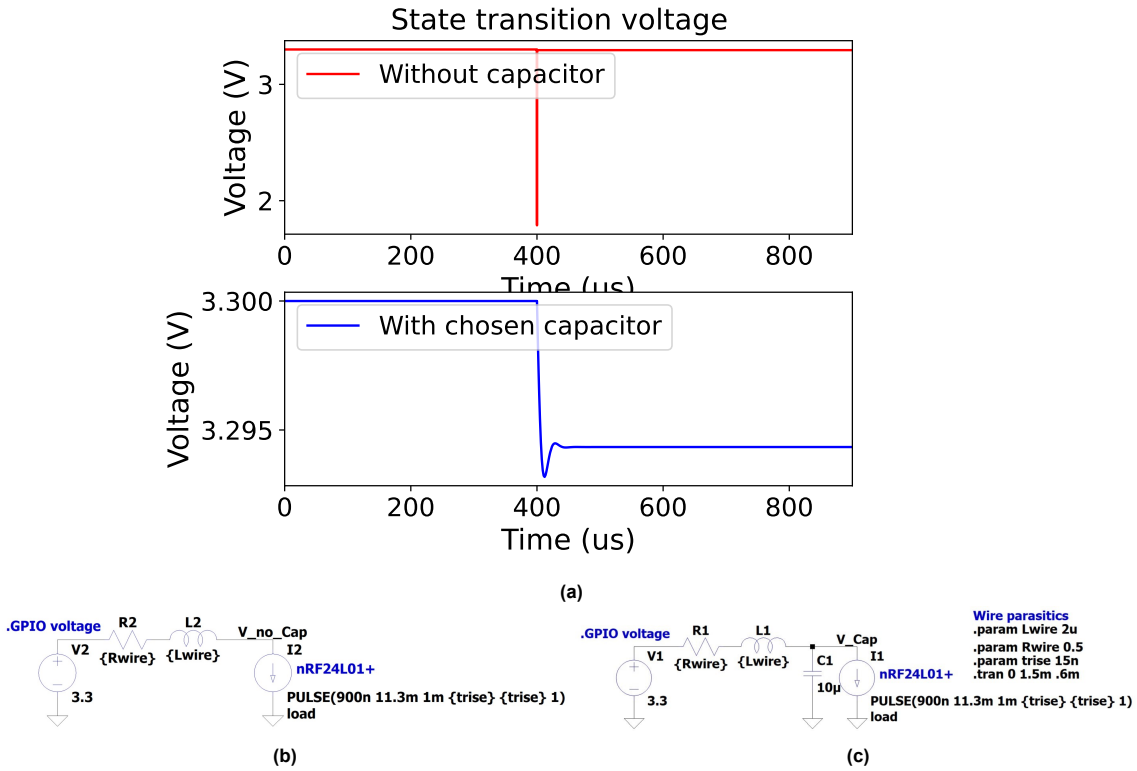



**Figure 5.13:** LTspice model for the nRF24L01+ demonstrating the effect of decoupling capacitors on voltage drop during state transitions at $400\mu s$: (a) simulation results, (b) circuit without the chosen capacitor, and (c) circuit with the chosen capacitor.

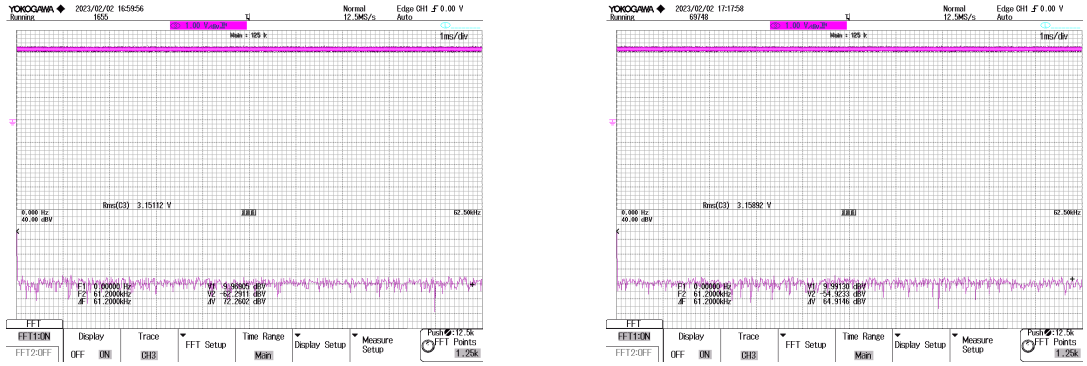
### 5.4.2. Minimizing power supply noise for the nRF24L01+ module.

Ideally, the power line should provide a clean and stable DC voltage of $3.3V$ to the nRF24L01+ module. However, as depicted in Figure 5.14, noise is observed on the $3.3V$ line even in the absence of nearby EMI sources. This noise, if left unaddressed, can potentially lead to communication errors for the nRF24L01+ module.

To mitigate this issue, a capacitor can be employed to divert high-frequency noise away from the power line. Compared to the alternative of using a common mode choke, capacitors are smaller and more cost-effective, making them a preferable choice. At high frequencies, the capacitor presents a low impedance, allowing high-frequency noise to be directed to the ground while the DC component of the $3.3V$ voltage remains unaffected as the capacitor acts as an open circuit. This behavior is illustrated in Figure 5.15b.

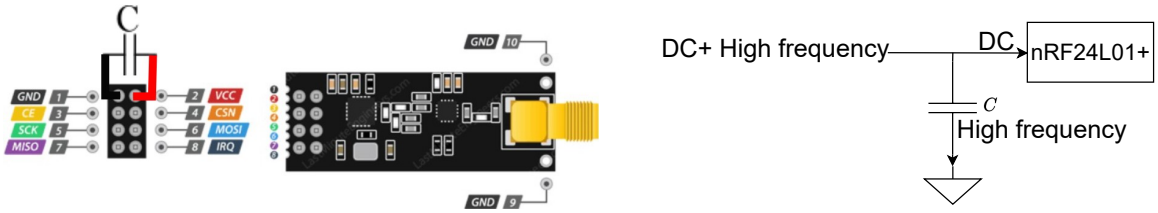
After determining the minimum required capacitance, as discussed in the previous subsection, the next step is to choose the suitable capacitor material and capacitance value to mitigate noise on the power line. In this thesis, electrolytic and ceramic capacitors are being considered due to their affordability and compactness. The relationship between impedance and capacitance will be explored, beginning with the ideal capacitor scenario and then transitioning to a more realistic capacitor model.

The transfer function for the impedance of an ideal capacitor is described by Equation (5.4), and its corresponding Bode plot can be seen in Figure 5.16.



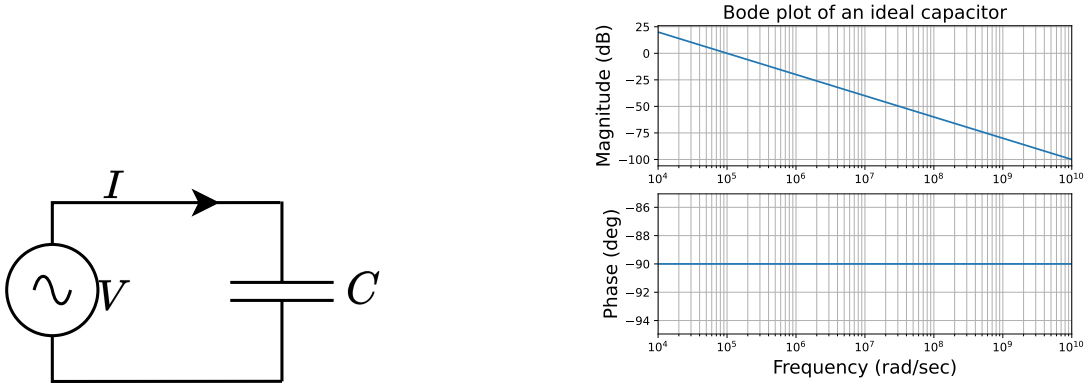
(a) (b)

**Figure 5.14:** FFT analysis of the provided $3.3V$ from launchpad signal under different conditions: (a) idle, and (b) during transmission.




(a) (b)

**Figure 5.15:** (a) illustration of decoupling capacitor connection to nRF24L01+ module,(b) of capacitor on high frequency components.




(a) (b)

**Figure 5.16:** Ideal capacitor impedance: (a) circuit model, and (b) Bode plot.

$$V = \frac{1}{C}\int i\,dt \xrightarrow[\text{Transform}]{\text{Laplace}} \frac{V}{I}(s) = \frac{1}{Cs} \tag{5.4}$$

When choosing a practical capacitor, it is important to consider various factors. One crucial consideration is the presence of parasitic equivalent series resistance ($R_{esr}$) and parasitic equivalent series inductance ($L_{esl}$), as practical capacitors are not purely capacitive. The impedance transfer function for a practical capacitor is given by Equation (5.5), and its corresponding Bode plot can be seen in Figure 5.17.

While the Bode plot exhibits similar characteristics to Figure 5.16 at low frequencies, the impedance starts to increase at higher frequencies due to the influence of $Lesl$. This behavior highlights the importance of considering the impact of parasitic elements on capacitor performance.

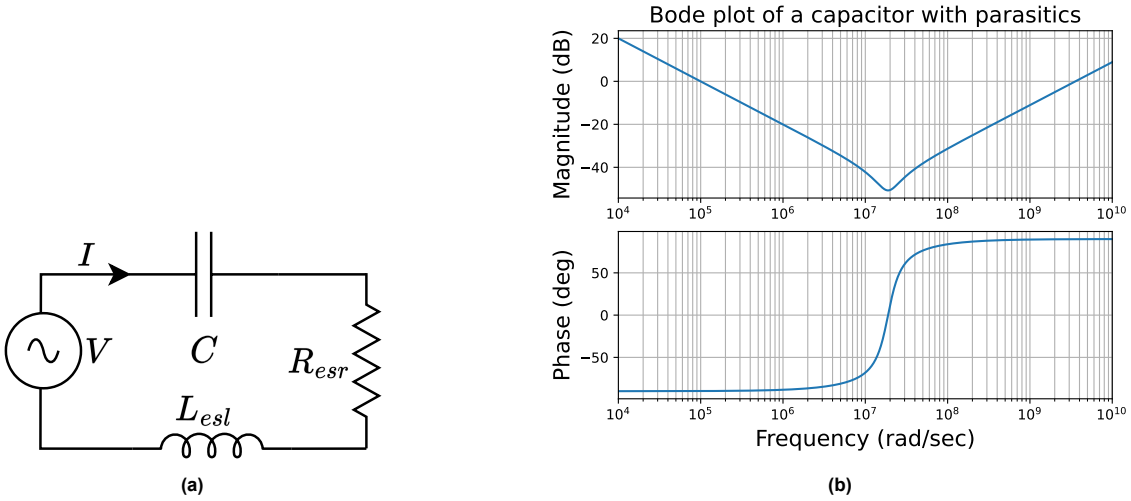



**Figure 5.17:** Impedance of a practical capacitor with parasitic ESR and ESL: (a) circuit model, and (b) Bode plot.

$$V = \frac{1}{C}\int i\,dt + iR_{esr} + L_{esl}\frac{di}{dt} \xrightarrow[\text{Transform}]{\text{Laplace}} \frac{V}{I}(s) = \frac{1}{Cs} + R_{esr} + sL_{esl} \Rightarrow \frac{L_{esl}Cs^2 + R_{esr}Cs + 1}{Cs} \quad (5.5)$$

To begin, Multilayer Ceramic Chip Capacitors (MLCC) will be examined. For simulating real-world effects, the C2012JB1V106K085AC ($10\mu F$) and the C2012JB1H105K085AB ($1\mu F$) capacitors were selected, with their respective impedances displayed in Figure 5.18.

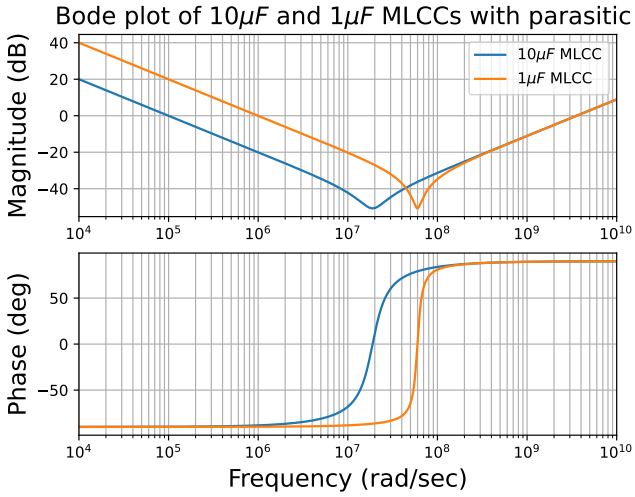



**Figure 5.18:** Bode plot of impedance for MLCC capacitors with parasitic ESR and ESL: $10\mu F$ and $1\mu F$.

Upon careful analysis of the impedance response plot shown in Figure 5.18, it is evident that combining a $10\mu F$ capacitor with a $1\mu F$ capacitor can lead to a desirable response. At low frequencies, the $10\mu F$ capacitor exhibits lower impedance, while at high frequencies, when the impedance of the $10\mu F$ capacitor begins to rise, the $1\mu F$ capacitor demonstrates lower impedance. A combination would provide effective impedance control across a wide frequency range, making it suitable for addressing various frequency components in the system.

To further explore the topic, two configurations were simulated: series configuration and parallel configuration. The simulation results for both configurations are presented in Figure 5.19, and the corresponding transfer functions for the series and parallel configurations are provided in Equation (5.6) and Equation (5.7), respectively.

It is important to note that in Equation (5.7), the parameters for the parallel configuration ($R_{esr1}$, $R_{esr2}$, $L_{esl1}$, and $L_{esl2}$) were substituted with $R_1$, $R_2$, $L_1$, and $L_2$, respectively, to ensure a better fit of the equation.

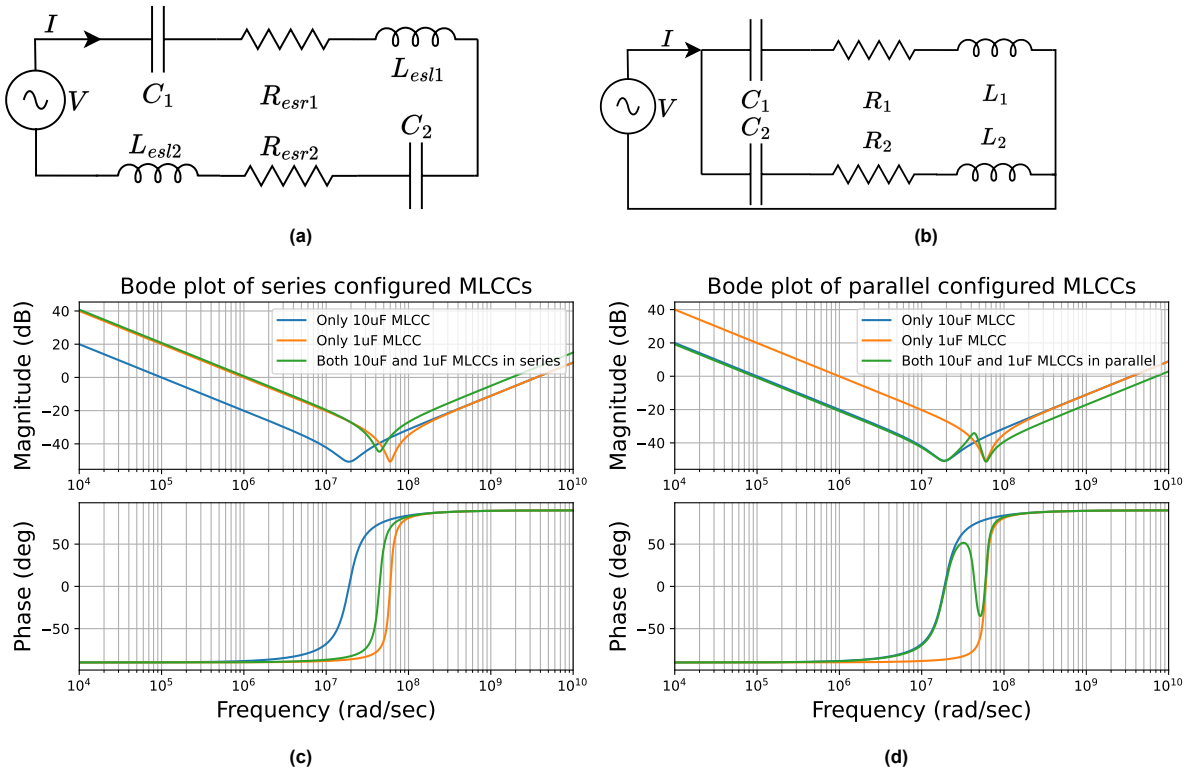



**Figure 5.19:** Impedance model with parasitic: (a) circuit model of series configuration of two capacitors with ESR and ESL, (b) circuit model of parallel configuration of two capacitors with ESR and ESL, (c) Bode plot of $10\mu F$, $1\mu F$ alone, and both in series, and (d) Bode plot of $10\mu F$, $1\mu F$ alone, and both in parallel.

$$\frac{V}{I}(s) = \frac{(L_{esl1} + L_{esl2})C_1C_2s^2 + (R_{esr1} + R_{esl2})C_1C_2s + (C_1 + C_2)}{C_1C_2s} \tag{5.6}$$

$$\frac{V}{I}(s) = \frac{C_1C_2L_2L_1s^4 + (L_1R_2 + L_2R_1)C_1C_2s^3 + (C_1L_1 + C_1C_2R_1R_2 + C_2L_2)s^2 + (C_1R_1 + C_2R_2)s + 1}{(L_2 + L_1)C_1C_2s^3 + (R_2 + R_1)C_1C_2s^2 + (C_1 + C_2)s} \tag{5.7}$$

The Bode plots reveal that the series configuration is less effective than either of the individual MLCC capacitors. In contrast, the parallel configuration shows potential in achieving the desired response but exhibits a rise in impedance between $10^7$ rad/s and $10^8$ rad/s, likely due to the $10\mu F$ capacitor becoming more inductive and forming a parallel RLC tank with the $1\mu F$ capacitor. To compare the Bode plot of the RLC tank with the parallel configuration, refer to Figure 5.20. The transfer function of the RLC tank, which requires a damping resistor to decrease the resonant peak, is provided in Equation (5.8), and the RLC tank values were selected through experimentation.

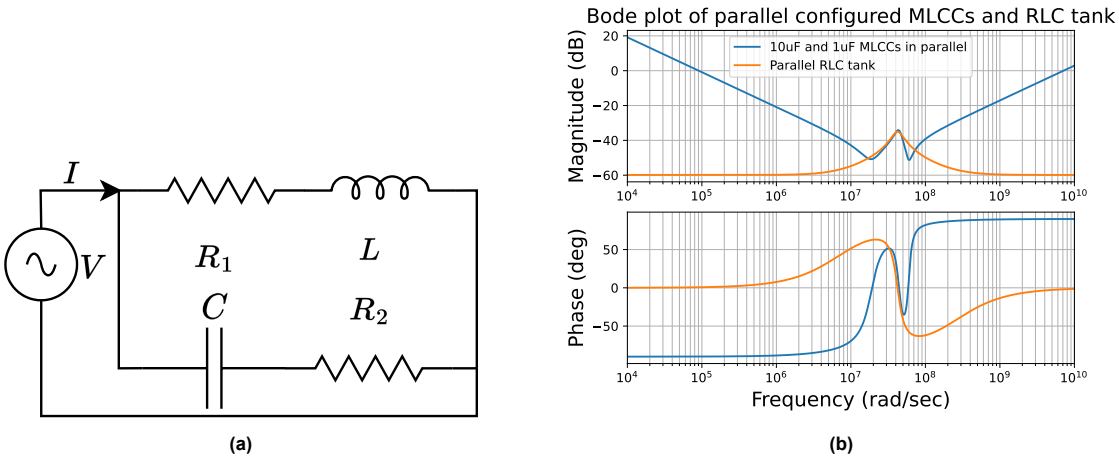



**Figure 5.20:** Impedance model: (a) circuit model of parallel RC and RL tank, and (b) Bode plot of impedance for parallel RLC tank overlapping $10\mu F$ and $1\mu F$ parallel configuration.

$$\frac{V}{I}(s) = \frac{CLR_2s^2 + (L + CsR_1R_2)s + R_1}{CLs^2 + (CR_2 + CR_1)s + 1} \tag{5.8}$$

Looking at Figure 5.19(d) the impedance increase between $10^7$ rad/s and $10^8$ $rad/s$ raises concerns about the performance of the nRF24L01+ module, which operates at a frequency of $2.4 \cdot 10^9 Hz$ and utilizes SPI at $5 \cdot 10^6 Hz$. When two capacitors of different values are used, resonances can occur. However, using two capacitors with identical capacitance may alleviate this issue. This can be observed by analyzing the transfer function in Equation (5.7) under the conditions of $C_1 = C_2$, $R_1 = R_2$, and $L_1 = L_2$, as illustrated in Figure 5.21.

$$\frac{V}{I}(s) = \frac{CLs^2 + RCs + 1}{2Cs} \tag{5.9}$$

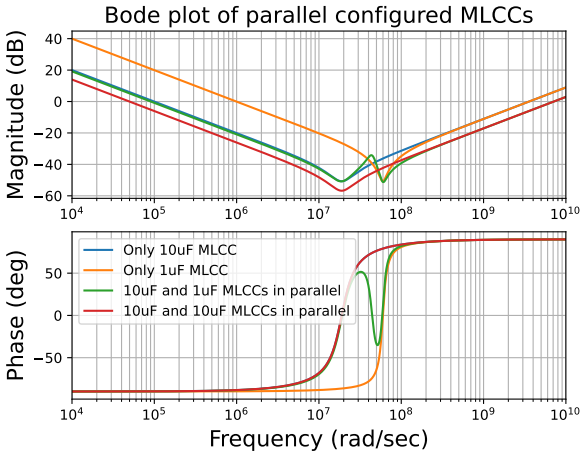



**Figure 5.21:** Bode plot showing the impedance of a $10\mu F$ and $1\mu F$ MLCC capacitors in different parallel configurations.

The analysis of the graph demonstrates that employing identical MLCC in parallel yields the most favorable impedance outcome. To validate these mathematical models, a comparison will be conducted with LTSpice. While constructing and testing physical models would provide a more comprehensive understanding, it would necessitate an impedance analyzer, a test setup, and a substantial amount of time. Thus, confirmation through LTspice will suffice. As depicted in Figure 5.22, the results align with the theoretical model shown in Figure 5.21, affirming that the optimal impedance is achieved by utilizing the same MLCC in parallel.

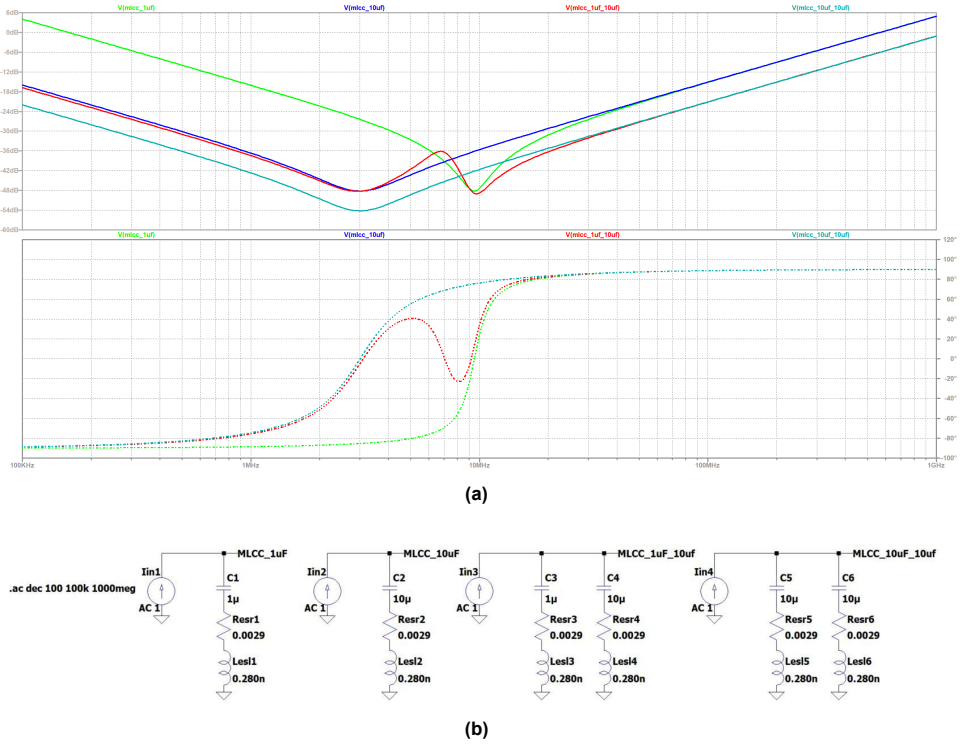



**Figure 5.22:** LTSpice simulation for comparing with Figure 5.21: (a) simulation result, and (b) simulation setup

To investigate the performance of electrolytic capacitors (ECaps) and compare them to the results obtained with MLCCs, a resimulation focusing on Figure 5.21 will be conducted. ECaps will be used in this resimulation, specifically the EEE-HB1C100AR model for the $10\mu F$ capacitor and the EEE-1HA010SR model for the $1\mu F$ capacitor. The obtained results will be compared visually to the MLCC results shown in Figure 5.23 to identify any observed differences.

As evident from Figure 5.23, the ECaps lack the resonating effect observed when different magnitudes of capacitors are connected in parallel, but exhibit higher impedance at the same frequency. This behavior can be attributed to the larger ESL values associated with ECaps [7].

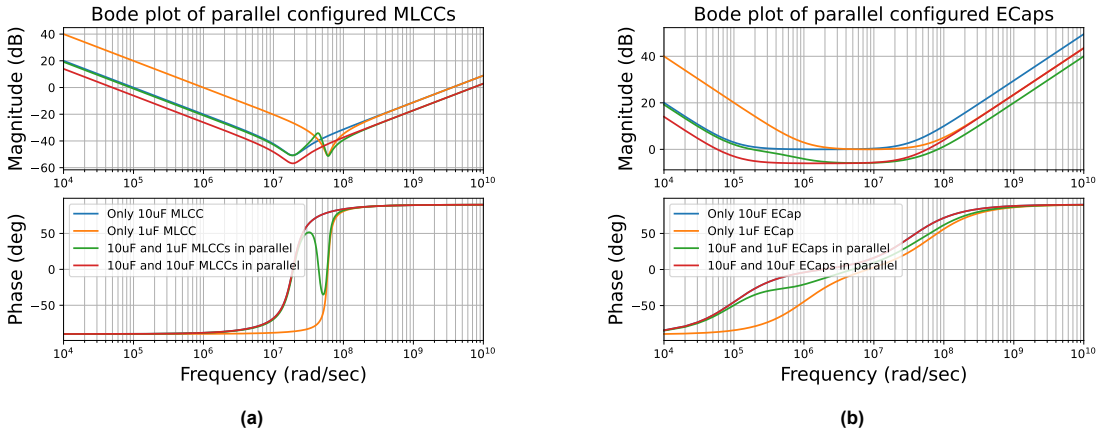



**Figure 5.23:** Bode plots of impedance for different parallel configurations of $10\mu F$ and $1\mu F$ capacitors using: (a) only MLCC, and (b) only ECap.

In conclusion, the optimal approach is to parallel multiple MLCCs of the same value, as it results in the lowest impedance. Alternatively, ECaps with different values can be used to achieve a smooth and flat impedance response. Combinations of MLCCs and ECaps are also viable, but their results fell between

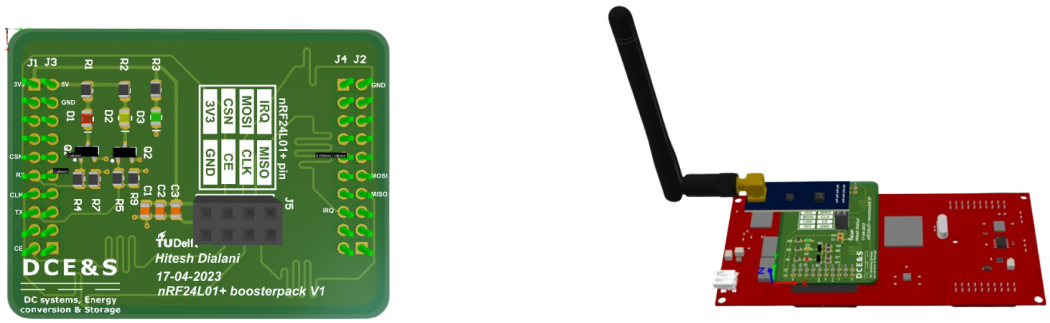
those shown in Figure 5.23. Although the plots for the combination of MLCCs and ECaps are not included in this thesis, readers interested in exploring them can modify Appendix B.3 or Appendix C.1 for further analysis.

MLCCs are preferred due to their compact size, and as shown in Figure 5.23, they exhibit lower impedance compared to ECaps. Of course, various factors such as applied voltage, and operating temperature, to name a few, but exploring their impact is beyond the scope of this thesis. For this design, two MLCCs with a capacitance of $10\mu F$ were chosen, with an additional empty pad available for another $10\mu F$ capacitor if needed. While $1\mu F$ capacitors will result in lower impedance at a higher frequency and thus have less high-frequency noise, it may present challenges in delivering sufficient charge during state transitions due to the lower capacitance. Given that digital signals are transmitted via SPI rather than analog, ensuring consistent power delivery to the nRF24L01+ module takes precedence over less high-frequency noise in the power line.

### 5.4.3. Addressing long wire connections between nRF24L01+ and microcontroller

An important consideration is the reliability of the connectors utilized. If the wires become disconnected, reconnecting them may result in incorrect socket connections. Additionally, the use of long wires can introduce issues such as susceptibility to EMI and signal degradation.

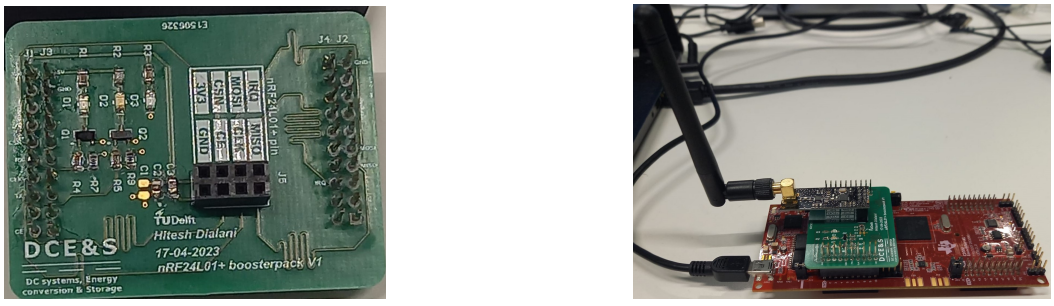
To address the issue of signal integrity when connecting the microcontroller to the nRF24L01+, minimizing wire distance is crucial, in addition to adding capacitors. Traces were employed instead of wires to enhance resilience against external EMI sources. Special attention was given to ensuring that all SPI traces had similar lengths, varying by only $\pm 1mm$. This meticulous design approach is demonstrated in the custom PCB shown in figure 5.24(a), while the complete PCB stack is depicted in figure 5.24(b). The zig-zag pattern implemented guarantees that all SPI traces have nearly identical lengths, with a tolerance of $\pm 1mm$.




(a) (b) .

**Figure 5.24:** Altium PCB design showcasing: (a) the custom nRF24L01+ boosterpack, and (b) nRF24L01+ boosterpack with nRF24L01+ and LaunchXL TMS320F28379D stacked.

Next, the PCB was produced which is shown below.




(a) (b)

**Figure 5.25:** Assembled PCB: (a) nRF24L01+ boosterpack, and (b) nRF24L01+ boosterpack with nRF24L01+ and LaunchXL TMS320F28379D microcontroller stacked.

## 5.5. Validation of wireless communication

Finally to conclude this chapter the newly designed custom PCB was tested. The setup is shown in Figure 5.26 It uses a LED for validation.

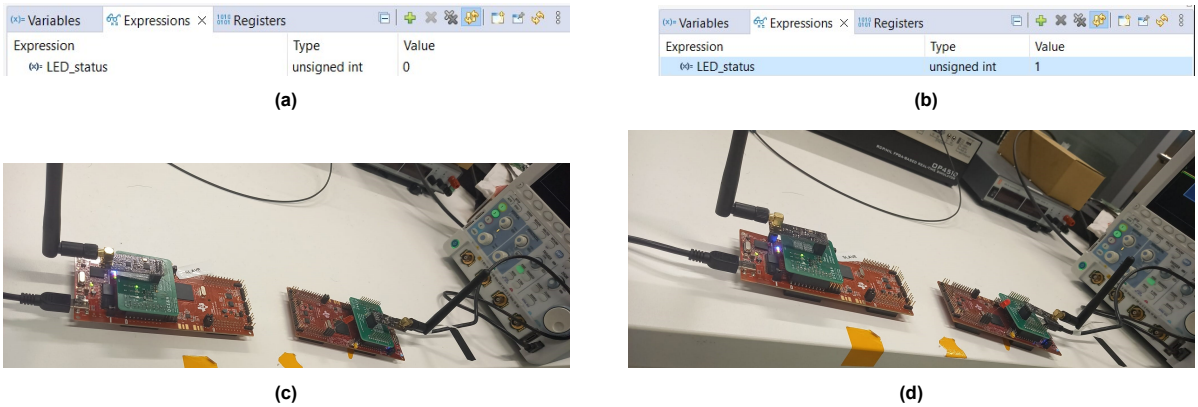



**Figure 5.26:** Validation of wireless communication: (a) transmitter sends LED status=0, denoting the LED is OFF from the left side. (b) the transmitter sends LED status=1, signifying the LED is ON from the left side. (c) the receiver microcontroller LED is OFF as a result of LED status=0, and (d) receiver microcontroller LED is illuminated as a result of LED status=1.

To perform the validation, the left-side microcontroller was programmed with a variable called LED status, which is then transmitted wirelessly to the right-side microcontroller. The right-side microcontroller, responsible for the LED, operates on flash memory and only requires a power supply to function. During the test, the USB port of the oscilloscope served as a power supply for the right-side microcontroller. The left-side microcontroller was programmed with SCI boot communications, enabling modification of the LED status.

# 6

# Conclusion and Future Work

In this chapter, a comprehensive summary of the obtained results is presented, along with valuable recommendations for future work.

## 6.1. Conclusion

The primary objective of this thesis, as discussed in Chapter 1, was to develop and implement an active rectifier tailored for practical EV charging. The active rectifier enables optimal load tracking. Effective communication between the primary and secondary sides is crucial for duty cycle coordination and power flow control. Two main challenges arise: synchronizing the secondary side MOSFETs with the secondary side current and ensuring efficient communication of the optimal primary side duty cycle when using separate microcontrollers.

the research question will be revisited shortly and seen how it has been answered throughout this thesis.

### 6.1.1. Why is it possible for an active rectifier to achieve optimal load matching with non-optimal loads, while a diode-based rectifier cannot?

In Chapter 2, a mathematical analysis demonstrates that the ideal load for maximum efficiency is solely dependent on the resonant frequency, mutual inductance, and parasitic resistance of both the primary and secondary side coils. A diode bridge with load can be approximated with an equivalent AC resistor as the load. However, due to the inherent nature of diodes, this AC resistance remains fixed, thus if it deviates from the optimal load there is nothing that can be done. On the other hand, Chapter 3 shows that by adjusting the secondary side duty cycle and phase shift between the secondary voltage and current, the AC resistance seen as the load can be modified. This allows the converter to tune the load seen from the converter to the optimal value.

In Chapter 3, in addition to the mathematical demonstration of an active rectifier's capability to achieve optimal load, the chapter also presents a practical setup showcasing the successful implementation of ZVS. This technique can be utilized to further increase system efficiency. Power flow control was also demonstrated by adjusting the duty cycle on both the primary and secondary sides.

### 6.1.2. What are effective strategies for designing synchronization to minimize latency?

In Chapter 4, the synchronization challenge is effectively addressed through the development of a custom printed circuit board (PCB) and custom software. The PCB underwent testing using a test signal that would represent the secondary side current. The test signal was then subjected to hardware signal processing, generating a rising edge signal whenever the current experienced a positive transition across the zero point. The hardware signal processing component with the lowest bandwidth used is the TSV991IYLT opamp, which has a bandwidth of $20MHz$ [31].

The PWM output of the LAUNCHXL-F28379D is programmed using Simulink to initiate the transmission of PWM signals upon receiving an external rising edge, which is generated by the aforementioned

PCB. This synchronization mechanism utilizes the digital compare sub-block, resulting in an impressively low latency of less than $50ns$ between the rising edge and the PWM output.

The PCB also incorporates a potentiometer for manual threshold tuning and utilizes hysteresis to prevent multiple rapid transitions from being interpreted as a single transition.

### 6.1.3. What are the key factors to consider when designing wireless communication systems to improve reliability?

In Chapter 5, the issue of transmitting the optimal duty cycle to the primary side is effectively tackled using the nRF24L01+ wireless transceiver. This wireless solution successfully enables communication between microcontrollers. To demonstrate this capability, a value of 3 was wirelessly transmitted from the transmitter side, while an attached LED on the receiver side illuminated only upon receiving the value 3. Both sides were programmed in C code to accommodate the complexity of the state diagram.

To enhance reliability and reduce issues like disconnected wires and susceptibility to electromagnetic interference (EMI), a custom PCB was used instead of physical wiring. This approach ensures dependable connections, minimizes the risk of disconnections, and mitigates EMI impact by utilizing traces on the PCB for the nRF24L01+ module to microcontroller connection. Additionally, decoupling capacitors were added to prevent accidental resets of the nRF24L01+ module during state transitions. Through LTspice simulations, it was demonstrated that the inclusion of a minimum $1\mu F$ capacitor effectively aids in this regard.

Moreover, through mathematical modeling, it was demonstrated that the parallel configuration of two MLCC (Multi-Layer Ceramic Capacitors) effectively diverts high-frequency noise from the power line, ensuring the reliability of the nRF24L01+ module. Specifically, it was found that utilizing two $10\mu F$ capacitors in parallel would deliver the best results. This configuration significantly enhances the system's overall reliability.

## 6.2. Recommendations for future work

Now that most of the project is finished, it is unavoidable to set some plans for future work and recommendations. These plans are:

- Implement the wireless communication software in Simulink instead of Code Composer to enhance user-friendliness.
- Implement auto-acknowledgment feature for more reliable wireless communication.
- Integrate communication and synchronization functionalities for a unified system.
- Design a controller specifically tailored for the dual-side topology.
- Combine the new controller with communication and synchronization capabilities.
- Evaluate the system's performance by implementing it with a non-optimal load and observe how it adapts itself toward achieving optimal load utilization.

# A

# Derivations

## A.1. Derivation of $Z_{in}$ uncompensated

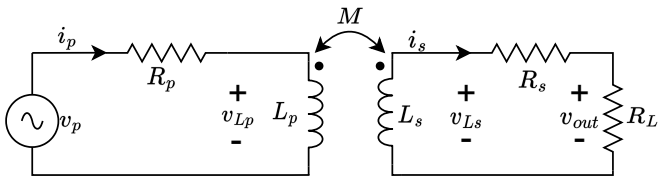



**Figure A.1:** Transformer equivalent model

The following relationship is known[4].

$$\begin{bmatrix} v_{Lp} \\ v_{Ls} \end{bmatrix} = \begin{bmatrix} L_p & -M \\ M & -L_s \end{bmatrix} \cdot \frac{d}{dt} \begin{bmatrix} i_p \\ i_s \end{bmatrix} \tag{A.1}$$

Using Kirchoff's voltage law

$$v_{Lp} = v_p - R_p i_p = Lp\frac{di_p}{dt} - M\frac{di_s}{dt} \tag{A.2}$$

$$v_{Ls} = M\frac{di_p}{dt} - L_s\frac{di_s}{dt} = R_s i_s + R_L i_s \tag{A.3}$$

Next convert it to phasor domain

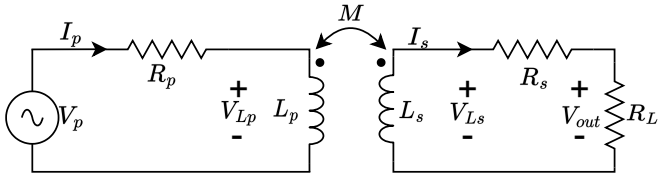



**Figure A.2:** Transformer equivalent model

Using Kirchoff's voltage law in phasor domain gives:

$$V_p - R_p I_p = j\omega L_p I_p - j\omega M I_s \Rightarrow V_p = (R_p + j\omega L_p)I_p - j\omega M I_s \tag{A.4}$$

$$j\omega M I_p - j\omega L_s I_s = R_s I_s + R_L I_s \Rightarrow j\omega M I_p = (j\omega L_s + R_s + R_L)I_s \tag{A.5}$$

from the above equation (A.6) can be derived.

$$I_s = \frac{j\omega M}{j\omega L_s + R_s + R_L} I_p \tag{A.6}$$

Now $I_p$ and $I_s$ can be written as

$$I_p = \frac{(R_L + R_s + j\omega L_s)}{(R_p + j\omega L_p)(R_L + R_s + j\omega L_s) - (j\omega M)^2} V_p \tag{A.7}$$

$$I_s = \frac{j\omega M}{(R_p + j\omega L_p)(R_L + R_s + j\omega L_s) - (j\omega M)^2} V_p \tag{A.8}$$

The equivalent impedance seen from the source is expressed as

$$Z_{in} = V_p / I_p \tag{A.9}$$

By substituting equation (A.6) into equation (A.4) the following can be found

$$Z_{in} = \frac{(R_p + j\omega L_p)(j\omega L_s + R_s + R_L) - (j\omega M)^2}{j\omega L_s + R_s + R_L} \Rightarrow R_p + j\omega L_p + \frac{(\omega M)^2}{j\omega L_s + R_s + R_L} \tag{A.10}$$

## A.2. Derivation of $Z_{in}$ with S-S compensation

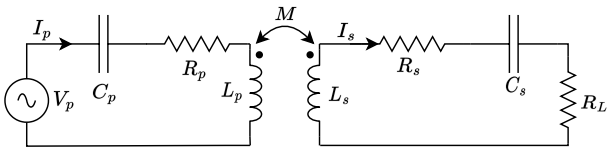



**Figure A.3:** Transformer equivalent model

Again in phasor domain. Using KVL on primary side

$$V_p - (R_P + \frac{1}{j\omega C_p}) I_p = j\omega L_p I_p - j\omega M I_s \Rightarrow V_p = (R_P + j\omega L_p - j\frac{1}{\omega C_p}) I_p - j\omega M I_s \tag{A.11}$$

Using KVL on secondary side

$$j\omega M I_p - j\omega L_s I_s = (R_s + R_L - j\frac{1}{\omega C_s}) I_s \Rightarrow j\omega M I_p = (R_s + R_L + j\omega L_s - j\frac{1}{\omega C_s}) I_s \tag{A.12}$$

From the above equation the following relationship can be made

$$I_s = \frac{j\omega M}{R_s + R_L + j\omega L_s - j\frac{1}{\omega C_s}} I_p \tag{A.13}$$

Now $I_p$ and $I_s$ can be written as

$$I_p = \frac{R_s + R_L + j\omega L_s - j\frac{1}{\omega C_s}}{\left(R_p + j\omega L_p - j\frac{1}{\omega C_p}\right)\left(R_s + R_L + j\omega L_s - j\frac{1}{\omega C_s}\right) - (j\omega M)^2} V_p \tag{A.14}$$

$$I_s = \frac{j\omega M}{\left(R_p + j\omega L_p - j\frac{1}{\omega C_p}\right)\left(R_s + R_L + j\omega L_s - j\frac{1}{\omega C_s}\right) - (j\omega M)^2} V_p \tag{A.15}$$

From this the $Z_{in} = V_p / I_p$

$$Z_{in} = \frac{\left(R_p + j\omega L_p - j\frac{1}{\omega C_p}\right)\left(R_s + R_L + j\omega L_s - j\frac{1}{\omega C_s}\right) + (\omega M)^2}{R_s + R_L + j\omega L_s - j\frac{1}{\omega C_s}} \tag{A.16}$$

## A.3. Equivalent ac resistor for full bridge diode rectifier

The full bridge inverter on the primary side generates a square wave voltage, which results in a square wave voltage on the secondary side as well. However, the resonant tank network on the secondary side filters out the higher harmonic voltages, resulting in a sine wave of current at the input to the resonant circuit. The series-resonant converter uses a capacitive output filter and therefore drives the rectifier with a current source [37]. For the proof equation (A.19) and equation (A.18) will be needed and appendix A.3.

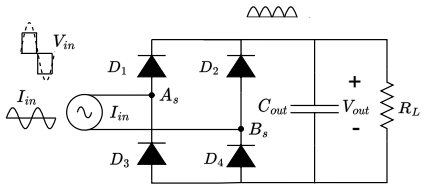



**Figure A.4:** Equivalent ac resistor as present for full bridge diode load for series converter

$$\text{average-rectified-sine} = \frac{2}{\pi}\text{sine-peak} \tag{A.17a}$$

$$\text{sine-RMS} = \frac{1}{\sqrt{2}}\text{sine-peak} \tag{A.17b}$$

The Fourier series of a square wave is given as:

$$f(x) = \frac{4}{\pi}\sum_{n=1,3,5,\ldots}^{\infty}\frac{1}{n}\sin\left(\frac{n\pi x}{L}\right) \tag{A.18}$$

For this analysis first harmonic approximation (FHA) will be used, this means all current are assumed to be pure sinusoidal. This is a reasonable assumption to be made since for a S-S configured system power is only transferred in the first harmonic [18], thus only the first harmonic is seen at the resistor.

$$\text{square-peak} = \frac{4}{\pi}\text{sine-peak-first-harmonic} \tag{A.19}$$

Combining equation (A.17) and equation (A.19) will result in

$$V_{out-ac-RMS} = \frac{2\sqrt{2}}{\pi}V_{out} \tag{A.20a}$$

$$I_{out-ac-RMS} = \frac{\pi}{2\sqrt{2}}I_{out} \tag{A.20b}$$

$$I_{out} = \frac{V_{out}}{R_{load}} \tag{A.20c}$$

with

$$R_{AC} = V_{out-ac-RMS}/I_{out-ac-RMS} \tag{A.21}$$

combining the above 2 equations results in

$$R_{AC} = \frac{\frac{2\sqrt{2}V_{out}}{\pi}}{\frac{\pi V_{out}}{2\sqrt{2}R_{load}}} \tag{A.22}$$

which can be simplified to

$$R_{AC} = \frac{(2\sqrt{2})^2}{\pi^2}R_{load} \tag{A.23}$$

which can be further simplified to

$$R_{AC} = \frac{8}{\pi^2}R_{load} \tag{A.24}$$

## A.4. Derivation of $P_{out}, V_{out}, \eta_{out}, R_{ac.opt}$ to load for S-S system with diode bridge

This time, a different approach will be taken. The coupled system is depicted in figure A.5. However, this system can be redrawn as two decoupled systems as shown in figure A.6. The mutual coupling between the two systems was replaced with current-dependent voltage sources. The polarity of the voltage sources depends on whether the current is entering or leaving the dot of the other system. Specifically, for the secondary side, $I_p$ enters the dot, so its dot is the positive terminal, while for the primary side, $I_s$ leaves the dot, so its dot is the negative terminal.

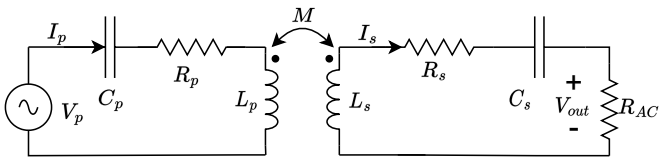



**Figure A.5:** Equivalent model coupled ciruit

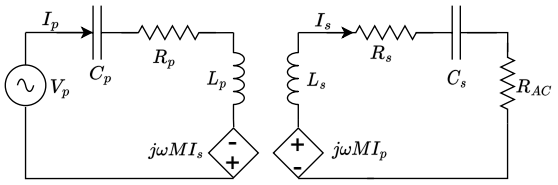



**Figure A.6:** Equivalent model decoupled circuit

Using KVL

$$I_s = \frac{j\omega M I_p}{R_{AC} + R_s + j\omega L_s + \frac{1}{j\omega C_s}} \tag{A.25a}$$

$$V_p = I_p * (R_p + j\omega L_p + \frac{1}{j\omega C_p}) - j\omega M I_s \tag{A.25b}$$

The voltage gain is

$$G_v = \frac{I_s R_{AC}}{V_p} \tag{A.26}$$

substituting everything gives

$$G_v = \frac{\frac{j\omega M I_p}{R_{AC}+R_s+j\omega L_s+\frac{1}{j\omega C_s}} R_{AC}}{I_p * (R_p + j\omega L_p + \frac{1}{j\omega C_p}) - j\omega M \frac{j\omega M I_p}{R_{AC}+R_s+j\omega L_s+\frac{1}{j\omega C_s}}} \tag{A.27}$$

which can be simplified to

$$G_v = \frac{j\omega M R_{AC}}{(R_p + j\omega L_p + \frac{1}{j\omega C_p})(R_s + R_{AC} + j\omega L_s + \frac{1}{j\omega C_s}) + \omega^2 M^2} \tag{A.28}$$

The efficiency can be written as

$$\eta_p = G_v G_i \tag{A.29}$$

Here

$$G_i = \frac{I_s}{I_p} \tag{A.30}$$

By using equation (A.13) it be written as

$$G_i = \frac{j\omega M}{R_{AC} + R_s + j\omega L_s + \frac{1}{j\omega C_s}} \tag{A.31}$$

resulting in

$$\eta_p = \frac{j\omega M}{(R_{AC} + R_s + j\omega L_s + \frac{1}{j\omega C_s})} \cdot \frac{j\omega M R_{AC}}{(R_p + j\omega L_p + \frac{1}{j\omega C_p})(R_s + R_{AC} + j\omega L_s + \frac{1}{j\omega C_s}) + \omega^2 M^2} \tag{A.32}$$

To simplify the equations and maximizing active power, the resonant frequency $\omega_0$ will be utilized. This approach will also be implemented in practice.

$$\eta_p = \frac{j\omega_0 M}{(R_{AC} + R_s)} \cdot \frac{j\omega_0 M R_{AC}}{R_p(R_s + R_{AC}) + \omega_0^2 M^2} \tag{A.33}$$

Now to find the optimal load $R_{AC,opt}$ the following can be used.

$$R_{AC,opt} => \frac{d\eta}{dR_{AC}} = 0 \tag{A.34}$$

This results in

$$\frac{d\eta}{dR_{AC}} = \frac{-(\omega_0 M)^2[R_p(R_s + R_{AC})^2 + \omega_0^2 M^2(R_{AC} + R_s)] + \omega_0^2 M^2 R_{AC}(2R_p R_s + 2R_p R_{AC} + \omega_0^2 M^2)}{[(R_p)(R_s + R_{AC})^2 + \omega_0^2 M^2(R_{AC} + R_s)]^2} \tag{A.35}$$

Then using Python the following result was found for the above equation $= 0$

$$R_{AC,opt} = \frac{1}{R_p}\sqrt{R_p R_s \omega_0^2 M^2 + R_p^2 R_s^2} = \sqrt{\omega_0^2 M^2 \frac{R_s}{R_p} + R_s^2} \tag{A.36}$$

Since $\omega_0^2 M^2 \frac{R_s}{R_p} >> R_s^2$ the $R_s^2$ term can be ignored for simplicity. Therefor

$$R_{AC,opt} = \sqrt{\omega_0^2 M^2 \frac{R_s}{R_p}} = \omega_0 M \sqrt{\frac{R_s}{R_p}} \tag{A.37}$$

## A.5. Derivation of opamp transfer function of closed loop transfer function

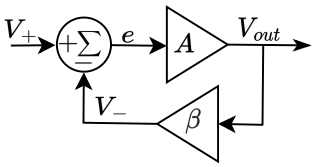



**Figure A.7:** Typical closed-loop system representation

Here $e$ has been added explicitly to help derive the transfer function. $e$ represents the error. The output can be written as:

$$V_{out} = eA \tag{A.38}$$

The error can be written as:

$$e = V_{in} - V_{out}\beta \tag{A.39}$$

Substituting the above equations into each other gives:

$$V_{out} = (V_{in} - V_{out}\beta) \cdot A \tag{A.40}$$

Placing all expressions of $Y(s)$ to the left results in

$$V_{out} + V_{out}\beta A = V_{in}A \tag{A.41}$$

This results in the following transfer function

$$\frac{V_{out}}{V_{in}} = \frac{A}{1 + \beta A} \tag{A.42}$$

## A.6. Derivation of opamp closed-loop with frequency dependency

From the previous derivation it is known that:

$$A_{CL} = \frac{V_{out}}{V_{in}} = \frac{A}{1 + \beta A} \tag{A.43}$$

The difference is now that A is frequency dependent

$$A = \underbrace{A_0}_{\text{DC gain}} \cdot \underbrace{\frac{\omega_c}{j\omega + \omega_c}}_{\text{frequency dependent term}} \tag{A.44}$$

This results in

$$A_{CL}(\omega) = \frac{A_0 \frac{\omega_c}{j\omega + \omega_c}}{1 + \beta A_0 \frac{\omega_c}{j\omega + \omega_c}} \tag{A.45}$$

Multiplying this with $j\omega + \omega_c$ results in

$$A_{CL}(\omega) = \frac{A_0 \frac{\omega_c}{j\omega + \omega_c}}{1 + \beta A_0 \frac{\omega_c}{j\omega + \omega_c}} \cdot \frac{j\omega + \omega_c}{j\omega + \omega_c} \Rightarrow \frac{A_0\omega_c}{j\omega + \omega_c + A_0\beta\omega_c} \tag{A.46}$$

Which can be rewritten as

$$A_{CL}(\omega) = \frac{A_0\omega_c}{j\omega + (1 + A\beta) \cdot \omega_c} \tag{A.47}$$

Multiply this with $1 + A_0\beta$ results in:

$$A_{CL}(\omega) = \frac{A_0\omega_c}{j\omega + (1 + A\beta) \cdot \omega_c} \cdot \frac{1 + A_0\beta}{1 + A\beta} \Rightarrow \frac{A_0\omega_c \cdot (1 + A_0\beta)}{(1 + A_0\beta) \cdot (j\omega + (1 + A\beta) \cdot \omega_c)} \tag{A.48}$$

This can be rewritten as:

$$A_{CL}(\omega) = \underbrace{\frac{A_0}{1 + A_0\beta}}_{\text{DC gain}} \cdot \underbrace{\frac{\omega_c \cdot (1 + A_0\beta)}{j\omega + \omega_c \cdot (1 + A_0\beta)}}_{\text{frequency dependent term}} \tag{A.49}$$

## A.7. Derivation of input and output resistance of opamp with negative feedback

First the output resistance will be found. To find the output resistace all input sources need to be shorted and an output 'test' source will be added. figure A.8 shows the circuit needed to find the output resistance.

First the minus terminal voltage of the opamp will be found. This is given with as:

$$V_{-} = \beta V_{test} \tag{A.50}$$

Next the ouput voltage of the opamp will be found the general equation is given as:

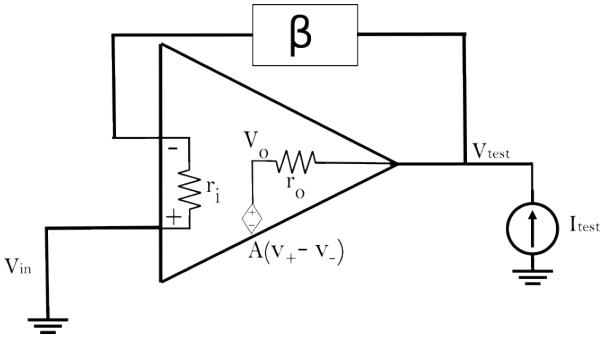



**Figure A.8:** Test circuit to find output resistance of opamp with negative feedback

$$V_o = A(V_+ - V_-) \tag{A.51}$$

Opamp amplifies the voltage difference between it's plus and minus terminal. Since the plus terminal is shorted $V_+ = 0$. Thus the equation can be rewritten as

$$V_o = A(V_+ - V_-) = -AV_- \tag{A.52}$$

Substituting above equations result in

$$V_o = -A\beta V_{test} \tag{A.53}$$

To determine the path of the test current, it can either flow through the opamp or the feedback circuit. However, due to the significantly higher input resistance ($r_i$) of the opamp compared to its output resistance ($r_o$), the contribution of the feedback system can be neglected. Despite this, as $r_o$ is not infinite, there will still be some degree of error, leading to an approximation that can be expressed as follows:

$$I_{test} \approx \frac{V_{test} - V_o}{r_o} \tag{A.54}$$

Which can be rewritten as

$$I_{test} \approx \frac{V_{test} + A\beta V_{test}}{r_o} \tag{A.55}$$

The output resistance of the circuit is shown below

$$R_o = \frac{V_{test}}{I_{test}} \approx \frac{r_o}{1 + A\beta} \tag{A.56}$$

Now the input resistance will be derived. For this the below circuit will be used. Now a test voltage will be added to the input and the output is an open circuit.

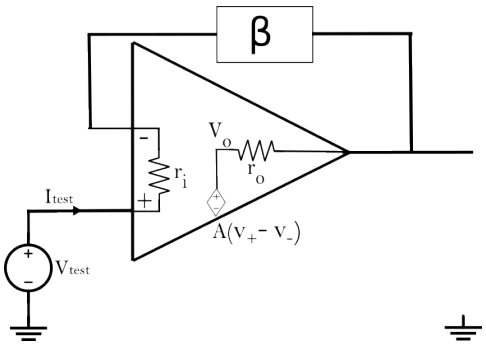



**Figure A.9:** Test circuit to find input resistance of opamp with negative feedback

Now the voltage difference between both terminals of the opamp can be written as

$$V_+ - V_- = r_i i_{test} \tag{A.57}$$

Therefor

$$V_o = A(V_+ - V_-) = -AV_- = Ar_i i_{test} \tag{A.58}$$

The input resistance is expressed as

$$R_i = \frac{V_{test}}{I_{test}} \tag{A.59}$$

The above 2 equations can be rewritten as

$$R_i = \frac{V_{test}}{I_{test}} = \frac{Ar_i V_{test}}{V_o} \tag{A.60}$$

Here the inverse of equation (A.42) can be used as substitution for $V_{test}/V_o$. This is not entirely true since $r_i \neq 0$. but it is so low that it can be approximately correct therefor:

$$R_i \approx \frac{1 + A\beta}{A} Ar_i \approx (1 + A\beta)r_i \tag{A.61}$$

## A.8. Derivation of differential amplifier

This sections show the derivation of how the differential amplifier works. The one chosen for this thesis is shown in figure A.10.

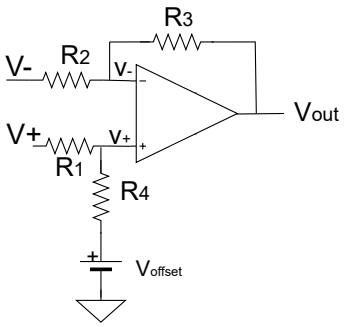



**Figure A.10:** Differential opamp with offset chosen for zero current crossing circuit

At first glance, the circuit may seem overwhelming due to the presence of three input voltage sources and a single output voltage, along with the additional complexity of four resistors. To simplify the process of deriving the transfer function, an assumption is necessary, which in this case is that the opamp is linear. This assumption holds true for ideal opamps, although it may not be applicable to practical opamps. By utilizing the superposition principle, the circuit can be simplified, allowing it to be seen in a new light as demonstrated in figure A.11.

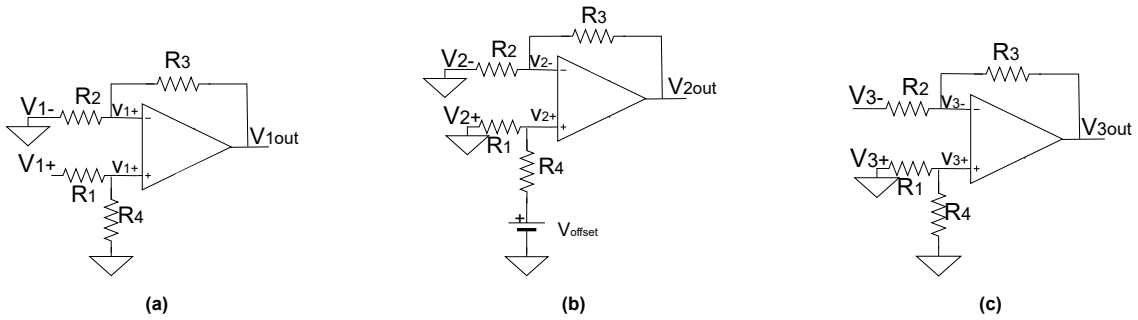



**Figure A.11:** Super position representation of previous circuit

In figure A.11a, the positive terminal of the opamp can be represented as a simple voltage divider using the following equation

$$v_{1+} = V_{1+}\frac{R_4}{R_4 + R_1} \tag{A.62}$$

Now to find $V_{1out}$ as a function of $v_{1+}$. The following sub equations show how this can be done.

$$V_{1out} = A(v_{1+} - v_{1-}) \tag{A.63a}$$

$$V_{1out} = A(v_{1+} - V_{1out}\frac{R_2}{R_3 + R_2}) \tag{A.63b}$$

$$V_{1out}(1 + A\frac{R_2}{R_3 + R_2}) = Av_{1+} \tag{A.63c}$$

$$\frac{V_{1out}}{v_{1+}} = \frac{A}{1 + A\frac{R_2}{R_3+R_2}} \tag{A.63d}$$

Since $A >> 1$ the above equation can be rewritten as:

$$\frac{V_{1out}}{v_{1+}} = \frac{R_3 + R_2}{R_2} \tag{A.64}$$

Therefor for figure A.11a:

$$V_{1out} = \frac{R_3 + R_2}{R_2}V_{1+}\frac{R_4}{R_4 + R_1} \tag{A.65}$$

For figure A.11b the same steps can be done, the only difference is that $v_{2+} = \frac{R_1}{R_4+R_1}V_{offset}$. This results in:

$$V_{2out} = \frac{R_3 + R_2}{R_2}V_{offset}\frac{R_1}{R_4 + R_1} \tag{A.66}$$

Now to figure A.11c it can be seen that $v_{3+} = 0$. Thus:

$$V_{3out} = A(v_{3+} - v_{3-}) \tag{A.67a}$$

$$V_{3out} = A(0 - v_{3-}) \tag{A.67b}$$

No current theoretically enters the opamp therefore:

$$\frac{V_{3-}}{R_2} = -\frac{V_{3out}}{R_3} \tag{A.68}$$

This can now be expressed as

$$V_{3out} = -\frac{R_3}{R_2}V_{3-} \tag{A.69}$$

Now the output of figure A.10 can be expressed as:

$$V_{out} = V_{1out} + V_{2out} + V_{3out} \tag{A.70}$$

Substituting everything results in

$$V_{out} = V_+\frac{R_3 + R_2}{R_2}\frac{R_4}{R_4 + R_1} + V_{offset}\frac{R_3 + R_2}{R_2}\frac{R_1}{R_4 + R_1} - \frac{R_3}{R_2}V_- \tag{A.71}$$

By taking the following condition:

$$R_3 = R_4, R_1 = R_2 \tag{A.72}$$

The following representation can be given:

$$V_{out} = V_{offset}\frac{R_1}{R_1}\frac{R_3 + R_1}{R_3 + R_1} + \frac{R_3}{R_1}(\frac{R_3 + R_1}{R_3 + R_1}V_+ - V_-) \tag{A.73}$$

Which can be simplified to

$$V_{out} = V_{offset} + \frac{R_3}{R_1}(V_+ - V_-) \tag{A.74}$$

In practice $A$ is large, but not $\infty$ thus

$$V_{out} \approx V_{offset} + \frac{R_3}{R_1}(V_+ - V_-) \tag{A.75}$$

## A.9. Derivation of series RLC dampening factor

The voltage over a series RLC circuit is

$$v(t) = L\frac{di(t)}{dt} + i(t)R + \frac{1}{C}\int i(t)dt \tag{A.76}$$

Converting the term into Laplace domain gives

$$V = LsI + IR + \frac{I}{Cs} \tag{A.77}$$

Which has the characteristic equation of

$$s^2 + \frac{R}{L}s + \frac{I}{CL} \tag{A.78}$$

The general equation for a second order transfer function is

$$s^2 + 2\zeta\omega_n + \omega_n^2 \tag{A.79}$$

Here $\omega_n$ is the resonance frequency and $\zeta$ is the dampening factor. This result in

$$\omega_n = \frac{1}{\sqrt{CL}} \tag{A.80a}$$

$$\zeta = \frac{R}{2}\sqrt{\frac{C}{L}} \tag{A.80b}$$

# B

# Code

## B.1. Uncompensated Power Factor vs frequency

```
"""
@Author: Hitesh Dialani
@Date:   25-01-2023
@Detail: Plots the power factor over a range of different frequency for uncompensated circuit
"""
import matplotlib.pyplot as plt
import numpy as np

# Primary
Lp = 55.6e-6          # in H
Rp = 13e-3            # in Ohm
Ls = 48.6e-6          # in H

# Secondary
Rs = 24e-3            # in Ohm
Rl = 10               # in Ohm

k  = 0.25
M = k*np.sqrt(Lp*Ls) # in H
f_max  = 5e3            # in Hz

# Values
Increments = 20  # Sampling resolution
X = np.arange(0, f_max+Increments, Increments)
omega_X=X *2*np.pi

b = np.empty(len(X))
for i, omega in enumerate(omega_X):
    RpjXLp = Rp + 1j*omega*Lp
    RsRljXLs = Rs + Rl + 1j*omega*Ls
    num=RpjXLp*RsRljXLs+(omega*M)**2
    denum=RsRljXLs
    c = num / denum
    b[i] = c.real /(np.sqrt(c.real**2+c.imag**2))

plt.plot(X/1000,b)
plt.xlabel(r'$frequency~(kHz)$', fontsize=18)
plt.ylabel(r'$PF$', fontsize=18)
plt.title(f'Power Factor as a function of frequency for uncompensated system', fontsize=18)
plt.xlim([0, np.max(f_max/1000)])
plt.grid()

# Export the plot as PDF format without the white border
plt.savefig('power_factor_uncompensated.pdf', format='pdf', bbox_inches='tight')
plt.show()
```

## B.2. Efficiency vs Rac

```
"""
@Author: Hitesh Dialani
@Date:   14-05-2023
@Detail: Plot efficiency of full system for SS traditional diode system
"""
import matplotlib.pyplot as plt
import numpy as np

# Primary
Lp = 293.8e-6       # in H
Rp = 0.21           # in Ohm
Cp = 12e-9         # in F

# Secondary
Ls = 198.8e-6         # in H
Rs = 0.14           # in Ohm
Cs = 17.6e-9         # in F

k  = 0.19
f_0=85e3

M= k*np.sqrt(Lp*Ls)
print(M)
w_0=2*np.pi*f_0

Rac_optimal=w_0*M*np.sqrt(Rs/Rp)

print(Rac_optimal)
# Calculate NUM for different values of Rac
Rac_values = np.arange(0, 2*Rac_optimal, 1)
Efficiency_values = []
for Rac in Rac_values:
    Num = w_0*M*w_0*M*Rac
    Denum = (Rac+Rs)*(Rp*(Rs+Rac)+(w_0*M)**2)
    Efficiency=Num/Denum
    Efficiency_values.append(Efficiency)

# Define factors of Rac to use as x-tick labels
Rac_factors = [0, 1, 2]

# Calculate the corresponding positions for each factor of Rac
Rac_positions = [Rac_optimal * factor for factor in Rac_factors]

# Plot the results
fig, ax = plt.subplots()
ax.plot(Rac_values, Efficiency_values)
ax.set_xlabel(r'$R_{ac}/R_{ac-optimal}$', fontsize=18)
ax.set_ylabel(r'$\eta$', fontsize=18)
ax.set_title(f'Efficiency as a function of different R_AC', fontsize=18)
ax.set_xlim([0, 2*Rac_optimal])
# ax.set_ylim([0.98, 1])
ax.grid()

# Set the x-tick positions and labels
ax.set_xticks(Rac_positions)
ax.set_xticklabels([f'{factor}' for factor in Rac_factors])

# Add a second vertical line at 1 RAC
ax.axvline(x=Rac_optimal, color='red', linestyle='--')

# # Export the plot as PDF format without the white border
# plt.savefig('RAC_plot.pdf', format='pdf', bbox_inches='tight')
# plt.savefig('RAC_plot_zoomed_in.pdf', format='pdf', bbox_inches='tight')
plt.show()
```

## B.3. Impedance bode plot of capacitor

```
"""
@Author: Hitesh Dialani
@Date:   31-01-2023
```

```
@Detail: Mathematical model of Capacitor impedance to compare with LTspice
"""

import numpy as np
import scipy.signal as signal
import matplotlib.pyplot as plt

### Capacitor options
# MLLC Capacitors
C_MLLC_10u = 10e-6   # Capacitance in Farads
R_MLLC_esr_10u=0.0029 # Parasitic resistor
L_MLLC_esl_10u=0.280e-9 # Parasitic resistor

C_MLLC_1u = 1e-6   # Capacitance in Farads
R_MLLC_esr_1u=0.0029 # Parasitic resistor
L_MLLC_esl_1u=0.280e-9 # Parasitic resistor

# Electrolytic Capacitors
C_elec_10u = 10e-6   # Capacitance in Farads
R_elec_esr_10u=1 # Parasitic resistor
L_elec_esl_10u=30e-9 # Parasitic resistor

C_elec_1u = 1e-6   # Capacitance in Farads
R_elec_esr_1u=0.1 # Parasitic resistor
L_elec_esl_1u=15e-9 # Parasitic resistor


### Chosen parameters for simulation
C_10u = C_MLLC_10u   # Capacitance in Farads
R_esr_10u=R_MLLC_esr_10u # Parasitic resistor
L_esl_10u=L_MLLC_esl_10u # Parasitic resistor

C_1u  = C_MLLC_1u   # Capacitance in Farads
R_esr_1u=R_MLLC_esr_1u # Parasitic resistor
L_esl_1u=L_MLLC_esl_1u # Parasitic resistor

# C_10u = C_elec_10u   # Capacitance in Farads
# R_esr_10u=R_elec_esr_10u # Parasitic resistor
# L_esl_10u=L_elec_esl_10u # Parasitic resistor
#
# C_1u  = C_elec_1u   # Capacitance in Farads
# R_esr_1u=R_elec_esr_1u # Parasitic resistor
# L_esl_1u=L_elec_esl_1u # Parasitic resistor

R1_tank=0.35*R_esr_10u
R2_tank=0.35*R_esr_10u
C_tank=.4*C_MLLC_10u   # Capacitance in Farads
L_tank=.5*L_MLLC_esl_1u # Parasitic resistor

#### Frequencies range
w_start = 10e2
w_stop = 10e9
step = 10000
N = int ((w_stop-w_start )/step) + 1
w = np.linspace (w_start , w_stop , N)

### Transfer functions
# Single ideal capacitor with transfer function 1/sC
num_ideal_10u = np.array([1])
den_ideal_10u = np.array([C_10u ,  0])
H_ideal_10u = signal.TransferFunction(num_ideal_10u, den_ideal_10u)

# Single realistic capacitor with transfer function (LCs^2+RCs+1)/sC
num_parasitic_10u = np.array([L_esl_10u*C_10u,  R_esr_10u*C_10u,1])
den_parasitic_10u = np.array([C_10u ,  0])
H_parasitic_10u = signal.TransferFunction(num_parasitic_10u, den_parasitic_10u)

num_parasitic_1u = np.array([L_esl_1u*C_1u,  R_esr_1u*C_1u,1])
den_parasitic_1u = np.array([C_1u ,  0])
H_parasitic_1u = signal.TransferFunction(num_parasitic_1u, den_parasitic_1u)

```

```
# Two realistic capacitor below each other with transfer function (L_1+L_2)C_1C_2s^2+(R_1+R_2)C_1C_2s+(C_1+C_2)/C_1C_2s
num_parasitic_10u_1u_s = np.array([ (L_esl_1u+L_esl_10u)*C_10u*C_1u,(R_esr_1u+R_esr_10u)*C_10u*C_1u, C_10u+C_1u])
den_parasitic_10u_1u_s = np.array([C_10u*C_1u,0])
H_parasitic_10u_1u_s = signal.TransferFunction(num_parasitic_10u_1u_s, den_parasitic_10u_1u_s)


# Two different realistic capacitor in parallel with transfer function      12214+(12+21)         123+(11+1212+22)   2+(11+22)+1  /  (2+1)   123+(2+1)   122+(1+2)
num_parasitic_10u_1u_p = np.array([C_10u*C_1u*L_esl_10u*L_esl_1u, (L_esl_10u*R_esr_1u+L_esl_1u*R_esr_10u )*C_10u*C_1u,(C_10u*L_esl_10u+C_10u*C_1u*R_esr_10u*R_esr_1u+C_1u*L_esl_1u),(C_10u*R_esr_10u+C_1u*R_esr_1u), 1])
den_parasitic_10u_1u_p = np.array([(L_esl_1u+L_esl_10u)*C_10u*C_1u,(R_esr_1u+R_esr_10u)*C_10u*C_1u,(C_10u+C_1u),0])
H_parasitic_10u_1u_p = signal.TransferFunction(num_parasitic_10u_1u_p, den_parasitic_10u_1u_p)

# Two same realistic capacitor in parallel with transfer function (CLs2 + RCs + 1) / 2Cs
num_parasitic_10u_10u_p = np.array([ C_10u*L_esl_10u ,R_esr_10u*C_10u, 1])
den_parasitic_10u_10u_p = np.array([2*C_10u,0])
H_parasitic_10u_10u_p = signal.TransferFunction(num_parasitic_10u_10u_p, den_parasitic_10u_10u_p)

# Parallel RLC      (22+(+12) +1)/    (2+(2+1) +1)
num_RLC_tank = np.array([L_tank*C_tank*R2_tank,(L_tank+C_tank*R2_tank*R1_tank),R1_tank])
den_RLC_tank = np.array([C_tank*L_tank, (R1_tank+R2_tank)*C_tank,  1])
H_RLC_tank = signal.TransferFunction(num_RLC_tank, den_RLC_tank)

### Extract magnitude and phase for bode plot
w_ideal_10u, mag_ideal_10u, phase_ideal_10u = signal.bode(H_ideal_10u, w)
w_par_10u, mag_par_10u, phase_par_10u = signal.bode(H_parasitic_10u, w)
w_par_1u, mag_par_1u, phase_par_1u = signal.bode(H_parasitic_1u, w)
w_par_10u_1u_p, mag_par_10u_1u_p, phase_par_10u_1u_p = signal.bode(H_parasitic_10u_1u_p, w)
w_par_10u_1u_s, mag_par_10u_1u_s, phase_par_10u_1u_s = signal.bode(H_parasitic_10u_1u_s, w)
w_par_10u_10u_p, mag_par_10u_10u_p, phase_par_10u_10u_p = signal.bode(H_parasitic_10u_10u_p, w)
w_RLC_tank, mag_RLC_tank, phase_RLC_tank = signal.bode(H_RLC_tank, w)

### Bode Plot
plt.figure()
plt.subplot (2, 1, 1)# Bode Magnitude Plot
# plt.semilogx(w_ideal_10u, mag_ideal_10u) # Bode Magnitude Plot
plt.semilogx(w_par_10u, mag_par_10u)
plt.semilogx(w_par_1u, mag_par_1u)
# plt.semilogx(w_par_10u_1u_s, mag_par_10u_1u_s)
plt.semilogx(w_par_10u_1u_p, mag_par_10u_1u_p)
plt.semilogx(w_par_10u_10u_p, mag_par_10u_10u_p)
# plt.semilogx(w_RLC_tank, mag_RLC_tank)
# plt.title("Bode Plot ideal capacitor")
plt.title("Bode Plot real capacitor")
plt.grid(b=None, which='major', axis='both')
plt.grid(b=None, which='minor', axis='both')
# plt.legend(["Only 10uF MLCC Capacitor", "Only 1uF MLCC Capacitor ", "10uF and 1uF MLCC Capacitor in parallel","10uF and 10uF MLCC Capacitor in parallel"])
plt.legend(["Only 10uF MLCC Capacitor", "Only 1uF MLCC Capacitor ", "10uF and 1uF MLCC Capacitor in parallel","10uF and 10uF MLCC Capacitor in parallel"])
# plt.legend(["Only 10uF Electrolytic Capacitor", "Only 1uF Electrolytic Capacitor ", "10uF and 1uF Electrolytic Capacitor in parallel","10uF and 10uF Electrolytic Capacitor in parallel"])
plt.ylabel("Magnitude (dB)")
plt.xlim(w_start,w_stop)

plt.subplot (2, 1, 2)# Bode Phase plot
# plt.semilogx(w_ideal_10u, phase_ideal_10u)
plt.semilogx(w_par_10u, phase_par_10u)
plt.semilogx(w_par_1u, phase_par_1u)
# plt.semilogx(w_par_10u_1u_s, phase_par_10u_1u_s)
plt.semilogx(w_par_10u_1u_p, phase_par_10u_1u_p)
plt.semilogx(w_par_10u_10u_p, phase_par_10u_10u_p)
```

```
# plt.semilogx(w_RLC_tank, phase_RLC_tank)
plt.grid(b=None, which='major', axis='both')
plt.grid(b=None, which='minor', axis='both')
plt.ylabel("Phase (deg)")
plt.xlabel("Frequency (rad/sec)")
plt.xlim(w_start,w_stop)

plt.show()
```

# C

# Models

## C.1. LTspice model for Capacitor impedance plot

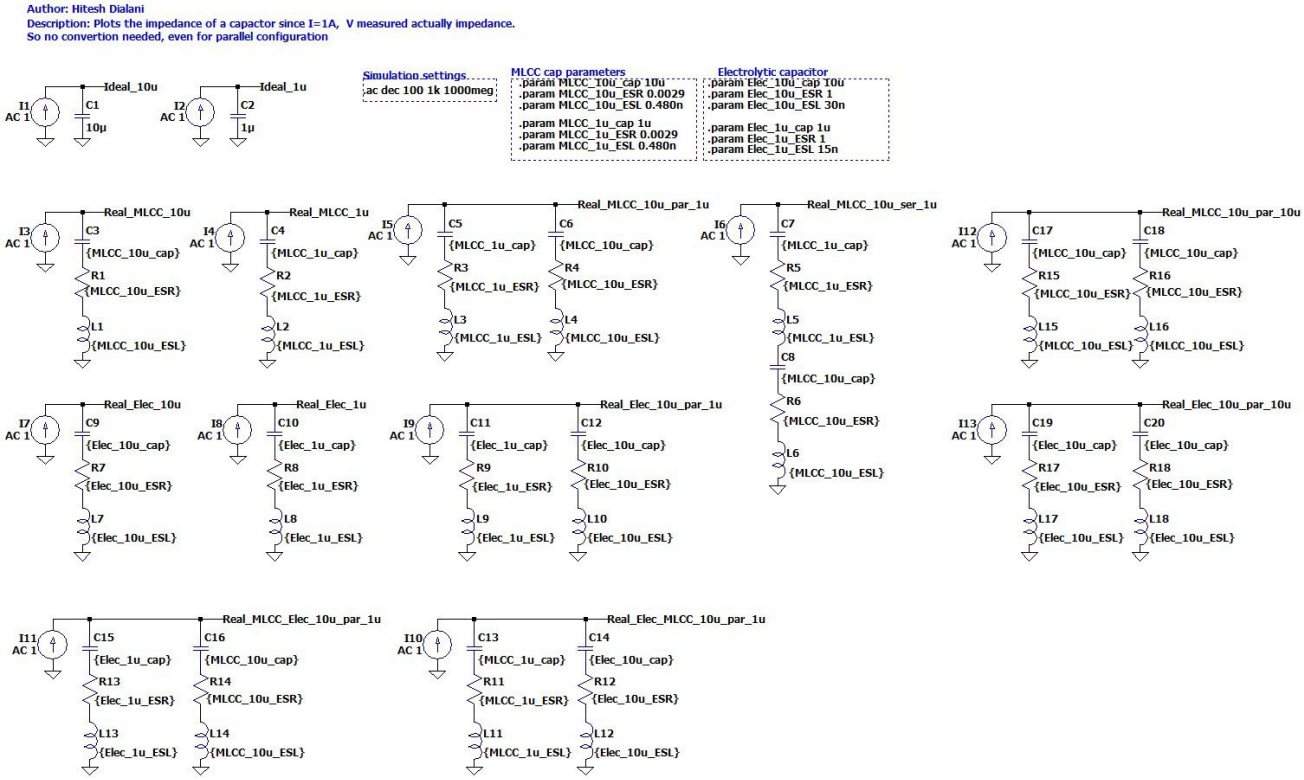



**Figure C.1:** LTspice models to validate mathematical model

# D

# Extra

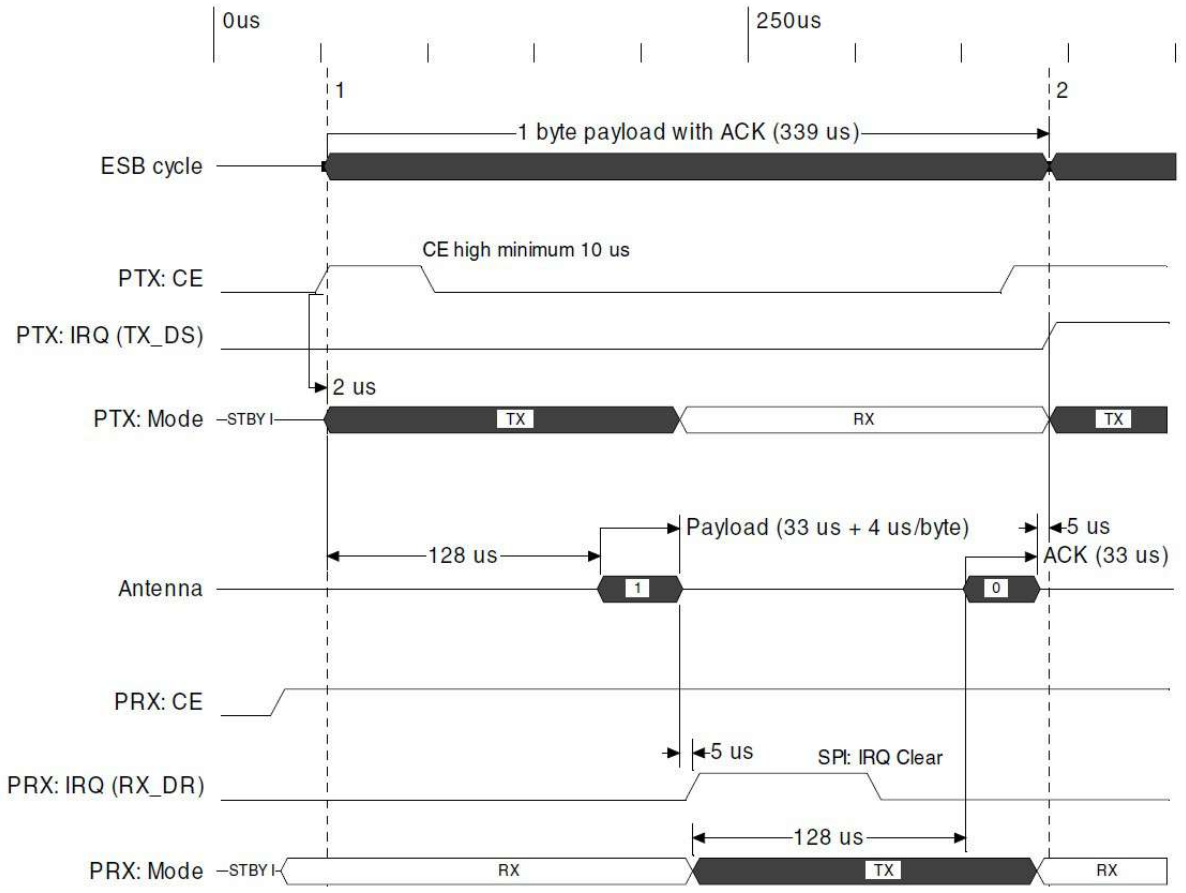



**Figure D.1:** Datasheet latency for nRF24L01+ module

# References


[1] Jamal Muhiyadin Sh-Ali. “Performance of defected ground structure for rectangular microstrip patch antenna”. PhD thesis. Universiti Tun Hussein Onn Malaysia, 2015.

[2] Bruce Archambeault. *Resistive vs. Inductive Return Current Paths*. 2008. URL: https://www.emcs.org/acstrial/newsletters/fall08/tips.pdf (visited on 03/24/2023).

[3] CA Baguley, SG Jayasinghe, and UK Madawala. “Theory and control of wireless power transfer systems”. In: *Control of Power Electronic Converters and Systems*. Elsevier, 2018, pp. 291–307.

[4] Prof.dr.ir. P. Bauer et al. *EE2E11 Electrical Energy Conversion student manual*. Delft University of Technology. 2022.

[5] Eric Bogatin. *Signal and power integrity - simplified*. en. 3rd ed. Philadelphia, PA: Prentice Hall, Jan. 2018.

[6] Eric Bogatin, Archambeault Bruce, and Hubing Todd. *A Simple Demonstration of Where Return Current Flows*. 2020. URL: https://www.signalintegrityjournal.com/articles/1771-a-simple-demonstration-of-where-return-current-flows (visited on 04/21/2023).

[7] Eric Bogatin, Larry Smith, and Steve Sandler. *The myth of three capacitor values*. 2022. URL: https://www.signalintegrityjournal.com/articles/1589-the-myth-of-three-capacitor-values (visited on 04/20/2023).

[8] Roman Bosshard et al. “Modeling and n-a-Pareto Optimization of Inductive Power Transfer Coils for Electric Vehicles”. In: *IEEE Journal of Emerging and Selected Topics in Power Electronics* 3.1 (2014), pp. 50–64.

[9] Yafei Chen et al. “A switching hybrid LCC-S compensation topology for constant current/voltage EV wireless charging”. In: *Ieee Access* 7 (2019), pp. 133924–133935.

[10] S Chopra and P Bauer. “Analysis and design considerations for a contactless power transfer system”. In: *2011 IEEE 33rd International Telecommunications Energy Conference (INTELEC)*. IEEE. 2011, pp. 1–6.

[11] Grant Anthony Covic and John Talbot Boys. “Modern trends in inductive power transfer for transportation applications”. In: *IEEE Journal of Emerging and Selected topics in power electronics* 1.1 (2013), pp. 28–41.

[12] Xin Dai et al. “Maximum efficiency tracking for wireless power transfer systems with dynamic coupling coefficient estimation”. In: *IEEE Transactions on Power Electronics* 33.6 (2017), pp. 5005–5015.

[13] Travis Deyle and Matt Reynolds. “Surface based wireless power transmission and bidirectional communication for autonomous robot swarms”. In: *2008 IEEE International Conference on Robotics and Automation*. IEEE. 2008, pp. 1036–1041.

[14] Tobias Diekhans and Rik W De Doncker. “A dual-side controlled inductive power transfer system optimized for large coupling factor variations and partial load”. In: *IEEE Transactions on Power Electronics* 30.11 (2015), pp. 6320–6328.

[15] Minfan Fu et al. “Analysis and tracking of optimal load in wireless power transfer systems”. In: *IEEE Transactions on Power Electronics* 30.7 (2014), pp. 3952–3963.

[16] Francesca Grazian et al. “Advantages and tuning of zero voltage switching in a wireless power transfer system”. In: *2019 IEEE PELS Workshop on Emerging Technologies: Wireless Power Transfer (WoW)*. IEEE. 2019, pp. 367–372.

[17] David M Hockanson et al. “Quantifying EMI resulting from finite-impedance reference planes”. In: *IEEE Transactions on Electromagnetic Compatibility* 39.4 (1997), pp. 286–297.

[18] Seyed Hossein Hosseini and Ali Yazdanpanah Goharrizi. “Harmonic optimization of Asymmetrical Voltage-Cancellation control for full-bridge series resonant inverters”. In: *2006 SICE-ICASE International Joint Conference*. IEEE. 2006, pp. 4350–4353.

[19] Zhicong Huang, Siu-Chung Wong, and K Tse Chi. “Control design for optimizing efficiency in inductive power transfer systems”. In: *IEEE Transactions on Power Electronics* 33.5 (2017), pp. 4523–4534.

[20] ISO. *ISO/PAS19363:2017*. Standard. Electrically propelled road vehicles - magnetic field wireless power transfer - Safety and interoperability requirements. Jan. 2017.

[21] Chang-Gyun Kim et al. “Design of a contactless battery charger for cellular phone”. In: *IEEE Transactions on Industrial Electronics* 48.6 (2001), pp. 1238–1247.

[22] Nikolaos Korakianitis, Georgios A Vokas, and Georgios Ioannides. “Review of wireless power transfer (WPT) on electric vehicles (EVs) charging”. In: *AIP Conference Proceedings*. Vol. 2190. 1. AIP Publishing LLC. 2019, p. 020072.

[23] Xuan Li et al. “Achieving zero switching loss in silicon carbide MOSFET”. In: *IEEE Transactions on Power Electronics* 34.12 (2019), pp. 12193–12199.

[24] Yong Li et al. “Dual-phase-shift control scheme with current-stress and efficiency optimization for wireless power transfer systems”. In: *IEEE Transactions on Circuits and Systems I: Regular Papers* 65.9 (2018), pp. 3110–3121.

[25] Lifewire. *Yes, You Can Charge your EV Wirelessly and Here’s How — lifewire.com*. https://www.lifewire.com/slug-placeholder-5203675. 2015. (Visited on 07/05/2023).

[26] Altium LLC. *[LIVE] How to Achieve Proper Grounding - Rick Hartley - Expert Live Training (US)*. 2020. URL: https://resources.altium.com/p/us-how-to-achieve-proper-grounding-rick-hartley-expert-live-training (visited on 03/24/2023).

[27] Ruikun Mai et al. “An active-rectifier-based maximum efficiency tracking method using an additional measurement coil for wireless power transfer”. In: *IEEE Transactions on Power Electronics* 33.1 (2017), pp. 716–728.

[28] Christopher Morrison et al. “Comparison of single-and double-sided pulse width modulated signals with non-linear predistortion”. In: *2012 5th European DSP Education and Research Conference (EDERC)*. IEEE. 2012, pp. 271–275.

[29] Zachariah Peterson. *IPC-2221 Calculator for PCB Trace Current and Heating*. 2023. URL: https://resources.altium.com/p/ipc-2221-calculator-pcb-trace-current-and-heating (visited on 03/24/2023).

[30] David M Pozar. *Microwave Engineering*. en. 4th ed. Chichester, England: John Wiley & Sons, Nov. 2011.

[31] *Rail-to-rail input/output 20 MHz GBP operational amplifiers*. TSV991. Rev. 14. STMicroelectronics. June 2019.

[32] Wenli Shi et al. “Design of a Highly Efficient 20-kW Inductive Power Transfer System With Improved Misalignment Performance”. In: *IEEE Transactions on Transportation Electrification* 8.2 (2022), pp. 2384–2399. DOI: 10.1109/TTE.2021.3133759.

[33] Ping Si et al. “A frequency control method for regulating wireless power to implantable devices”. In: *IEEE transactions on biomedical circuits and systems* 2.1 (2008), pp. 22–29.

[34] *Silicon Carbide Power MOSFET C3M MOSFET Technology N-Channel Enhancement Mode*. C3M0021120K. Rev. 1. Wolfspeed. Mar. 2023.

[35] *Single Chip 2.4GHz Transceiver*. nRF24L01+. Rev. 1. Nordic Semiconductors. Sept. 2008.

[36] Kai Song et al. “An impedance decoupling-based tuning scheme for wireless power transfer system under dual-side capacitance drift”. In: *IEEE Transactions on Power Electronics* 36.7 (2020), pp. 7526–7536.

[37] Robert L Steigerwald. “A comparison of half-bridge resonant converter topologies”. In: *IEEE transactions on Power Electronics* 3.2 (1988), pp. 174–182.

[38] *TI Designs – Precision: Verified Design Comparator with Hysteresis Reference Design*. https://www.ti.com/lit/ug/tidu020a/tidu020a.pdf?ts. (Visited on 06/10/2023).

[39] *TMS320F2837xD Dual-Core Microcontrollers*. TMS320F28379D. Rev. 2. Texas Instrumentation. Mar. 2020.

[40] Wenwei Victor Wang, Duleepa J Thrimawithana, and Martin Neuburger. “An Si MOSFET-Based High-Power Wireless EV Charger With a Wide ZVS Operating Range”. In: *IEEE Transactions on Power Electronics* 36.10 (2021), pp. 11163–11173.

[41] Tong Zhang et al. “Optimal load analysis for a two-receiver wireless power transfer system”. In: *2014 IEEE Wireless Power Transfer Conference*. IEEE. 2014, pp. 84–87.

[42] Wei Zhang et al. “Analysis and comparison of secondary series-and parallel-compensated inductive power transfer systems operating for optimal efficiency and load-independent voltage-transfer ratio”. In: *IEEE Transactions on Power Electronics* 29.6 (2013), pp. 2979–2990.

[43] WX Zhong and SYR Hui. “Maximum energy efficiency tracking for wireless power transfer systems”. In: *IEEE Transactions on Power Electronics* 30.7 (2014), pp. 4025–4034.

[44] Gangwei Zhu et al. “A Mode-Switching Based Phase Shift Control for Optimized Efficiency and Wide ZVS Operations in Wireless Power Transfer Systems”. In: *IEEE Transactions on Power Electronics* (2022).

[45] Silvio Ziegler et al. “Current sensing techniques: A review”. In: *IEEE Sensors Journal* 9.4 (2009), pp. 354–376.