[Confidential]

Low Temperature Fabrication of SiO_2 Films Using Liquid Silicon

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Master's Thesis

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Abstract

The use of liquid materials combined with printing techniques is believed to have unique advantages in low-cost integrated circuit manufacturing. It enables the large-area fabrication by non-vacuum processes and shows the potential to produce electronics on flexible substrates. However temperatures required for thermal annealing or oxidation steps are still too high to be compatible with plastic substrates. Organic materials were investigated to solve the problem but they suffered from low mobility and reliability. Liquid silicon based on polysilane is an alternative material to fabricate silicon devices at low temperatures, which has been proved to produce high electrical properties comparable to that made by poly-silicon. One of the factors that dominate the device performance and reliability is the quality of the dielectric film, i.e. the film integrity and interface state density. In this study, quality silicon-dioxide films have been formed using liquid silicon at temperatures ranging to a maximum of 400 ℃.

The experiments start with the film fabrication under the control of various parameters. 0.55% dip etching of a crystallized silicon surface can remove the native oxide and improve the wettability. The liquid silicon containing 50% Cyclopentasilane was spread on the silicon wafer by means of doctor blade coating, which is compatible to a roll-to-roll process. This is followed by exposing the film under UV light for polymerization. After that, a two-step baking process was performed for oxidation. The wafer was first baked in an inert gas environment to an early state of amorphous silicon formation and then transferred out to bake in the open air. The result shows that the O/Si ratio of the film is 1.79 for the samples prepared at 400℃ and 1.67 for samples prepared at 350℃.

MOS capacitors were fabricated using the produced SiO_2 films as dielectric layers for electrical characterization. The defect densities were obtained by comparing the high frequency capacitance versus voltage curve to the theoretical curve simulated using Matlab. The calculation result revealed that both the fixed oxide charges and interface states were in the order of 10^{11} $eV^{-1}cm^{-2}$. The breakdown field strength and resistivity of the film can be extracted from the current versus applied gate voltage curve. The breakdown field strength was 1.7 MV/cm and 1.1 MV/cm for samples prepared at the oxidation temperature of 400℃ and 350℃ respectively. The resistivity of both kinds of films were in the order of 10^{12} Ωcm while the sample prepared at 400℃ provided a slightly higher result.

In this study, a new fabrication method was implemented to convert liquid silicon into silicon dioxide films through non-vacuum and roll-to-roll compatible processes at low temperatures. The electrical characterization of SiO2 films made from liquid silicon was reported for the first time. The lower performance compared to thermal oxide is mainly caused by a lack of oxidation and the uniformity issues which can be improved by Excimer laser annealing and applying more active oxidants.

Key words: low temperature non-vacuum process solution process CPS

Contents

Chapter 1 Introduction

1.1 Topic background

Thin film transistors (TFT) have a wide range of applications and promising prospects in the field of microelectronics due to the following characteristics. To begin with, the substrate of TFTs can be either glass or plastic. Compared to traditional semiconductor fabrication on silicon substrate, which has a limited area and is very expensive in terms of its high purity, glass or plastic-based technology has unique advantages in terms of large-area and low-cost manufacturing. Secondly, with the implementation of plastic materials, a flexible circuit can be realized that shows a potential to make scalable, collapsible and portable electronic products.[1]

Originally, the target application for TFTs was in the field of displays. Amorphous silicon thin film transistors are applied to Liquid crystal displays (LCD). They are used to control the pixels by means of voltage regulation to drive active-matrix LCDs (AMLCD). However their low field effect mobility limits the application from high current driver devices.[2]Polycrystalline Si TFTs are capable of realizing various complex circuits with their high driving ability. Hence their implementation will not only bring about multifunctional displays but it will also reduce the weight and thickness of the displays[3]. However temperature limitations need to be taken into consideration. In large-scale TFT fabrication, the process temperature is limited to 400℃ for glass substrate and it is lower than 250℃ for polymer substrate, both of which cannot sustain polycrystalline-Si TFT formation with current mature technology.

In order to obtain high performance TFTs on the flexible substrate, a variety of research has been performed to solve the temperature compatible problem as well as further reduce the fabrication cost in different respects. For instance this can involve utilizing new film-forming materials that can function as high quality semiconductors to replace poly-Si, implementing new substrate materials that could support high temperature processes and bringing out new methods to realize the crystallization of silicon at low temperatures. Their emergence will not only develop the device performance, integration and reliability but it will also lead to new applications in the field of flexible electronics. A brief introduction will be given in the following context.

1.2 Research status

1.2.1 Low temperature fabrication of TFTs

To begin with, organics based on conjugated polymers, oligomers, or fused aromatics and amorphous oxide semiconductor based on $InGaZnO_4$ or ZrInZnO are flourishing in recent years as an alternative material to single-crystalline inorganic semiconductors for TFT fabrication.

Organic thin film transistors (OTFT) which are compatible with transparent plastic substrates can be made at or close to room temperature. Thus they are competitive candidates for large

areas and low temperature processing because they perform as well as amorphous silicon thin film transistors but at a lower temperature. Applications such as active matrix flat panel displays, organic light-emitting diodes and electronic paper displays have been widely developed in recent years. However, because of the relatively low mobility of organic materials, OTFTs cannot rival the performance of field-effect transistors based on polycrystalline semi-conductors.[4] [5]

Oxide semiconductors including $InGaZnO_4$ or ZrInZnO can be deposited with the help of conventional semiconductor processes at room temperature. Since the channel material is single crystal without grain boundaries, The material is capable to provide uniform device properties over large areas. Meanwhile, the mobility of the device has been developed to be high enough for circuit functions in a higher current. Because of such remarkable characteristics, oxide semiconductor TFTs are widely used in switching elements for large area AMLCD panels, solar cells and optical coatings. However Oxide semiconductor TFTs have their own drawbacks. In the first place, due to their physical properties, they can only make one type of device out of p or n type oxide semiconductors. This limits the function and performance of the circuit when compared to technologies based on compensate devices. In the second place, the reliability of the device still needs to be improved by reducing the defect densities in the material.[6] [7]

In addition to investigating new materials to form the device, new substrate materials that have low surface roughness, higher glass transition temperatures and low thermal expansion coefficients are also attractive because of their high temperature tolerance. Polycarbonate(PC), polyethylene terephthalate(PET) and polyethersulfone(PES) are plastics frequently applied as flexible substrates however they have problems of high temperature shrinkage. Besides, they are also influenced by external chemical agents during fabrication process. For Poly TFTs that require a higher process temperature, polyarylite (PAR) and polyimide(PI) films are now developing, which can maintain a better electrical, physical and mechanical properties over a wider temperature range.[8]

Moreover, innovative TFT fabrication methods are also constantly arising. The highest temperature step required in poly-Si TFT fabrication is the crystallization process which needs over 900 ℃ by thermal annealing. These process temperature can be reduced to a glass or plastic compatible level by means of the Excimer laser. A pulse laser provides energy by emitting photons in the ultra violet spectrum range. Then the energy will be absorbed by the film surface since the absorption coefficient of Si is very high. Therefore the silicon film will melt and resolidify in a fast speed while the substrate will not be elevated. In terms of crystallizing plasma enhanced chemical vapor deposited amorphous silicon films, generally a substrate temperature around 400 ℃ is required to remove hydrogen in the films and prevent their damage from diffusing out. In addition, when crystallize sputtering Si that contains no hydrogen, the substrate temperature can be reduced to 150 ℃ for synthesizing a high-quality and less-defective polysilicon films.[9] [10]

To further reduce the cost during TFT fabrication, scientists not only focus on low temperature

process researches which contribute to the large area fabrication, but also introduce the concept of print circuit to replace the conventional vacuum process. TFTs are generally fabricated with techniques such as photolithography, ion implantation, etching, sputtering, chemical vapor deposition, and high-temperature film growth. These vacuum-based processes adhere very strictly to fabrication norms involving environment, equipment and material. Mass scale fabrication is prevented because of the limited volume of vacuum chambers. On the contrary, solution processing which means using liquid substance to fabricate electronic devices has draw much attention recently because it can go through non-vacuum processes and realize fabrication over large areas. Materials for solution-based techniques have been investigated including organic materials, organic semiconductors and so on[11].

Cyclopentasilane (CPS:Si_5H_{10}) is an alternative material for the solution processing which will be applied in our study. It is a liquid state silicon compound that can be polymerized to hydrogenated polysilane under photo induced condition. The polymer cannot dissolve in most solvents but can dissolve in CPS solution or CPS mixing with an organic solvent. This silicon precursor solution made up of polysilane, CPS and an organic solvent is regarded as liquid silicon. It has been proven that the liquid silicon is capable of forming a quality polysilicon thin film[12]. Subsequent to that study, SiO_2 film processing using liquid silicon was recently reported[13]. Both studies indicate that the polydihydrosilane solution is capable of processing solution-based silicon devices.[14]

1.2.2 Low temperature fabrication of silicon dioxide films

Silicon dioxide has become an significant part in the integrate circuit with its stable physical and chemical properties. Conventionally, it can be thermally grown in an atmosphere containing pure oxygen or steam. The surface layer first oxidizes when oxidation occurs, after that, oxygen or water must pass through the oxide and reach the silicon interface to combine oxygen with silicon. Thus a temperature higher than 800℃ is required since water vapor and oxygen are then able to diffuse easily through the silicon dioxide.[15] Since these high temperatures are not compatible with the requirements for TFT production on glass substrate. What is widely used in TFT fabrication in recent times is tetra-ethyl-ortho-silicate (TEOS) deposited by plasma enhanced chemical vapor deposition (PECVD) at around 350℃. However, the film quality is not as good as thermal grown SiO_2 because the plasma would cause defects on the substrate during process.[16]

Further improvements in thin, high-quality gate oxides are necessary if the requirements of high-performance TFTs are to be met. Remote plasma deposition (RPD) was implemented because of the low plasma damage and low temperature process. However its step coverage is poor and breakdown filed strength is relatively low. Another methods that attract attention is inductively coupled plasma (ICP) enhanced CVD. It is also remote plasma deposition but ion energy can be controlled to reduce the bombardment and form a good interface.[17]

Forming SiO_2 film through a solution process would bring down processing costs and further

develop to print process of silicon device. Materials that are investigated to process solution-based SiO_2 films including polysilazane, CPS and so on. Polysilazane is capable to form dense SiO_2 films at an annealing temperature of 450 ℃. It was reported by Huynh Thi Cam Tu et al. that the leakage current density of polysilazane-processed SiO_2 films was 1×10^{-8} A/cm^2 at 1 MV/cm, which is sufficient to perform well as a gate insulator. Actually Polysilazane-based solution is not convertible to silicon films. In order to realize all-solution-processed TFTs, other solution processing techniques should be combined to form the active layer, such as using a ZrInZnO solution for the active layer as described in Huynh Thi Cam Tu's study[18]. Alternatively, Hideki Tanaka et al. has already formed the silicon dioxide film by spin coating CPS onto a quartz substrate and converting them into SiO_2 through a series of physical and chemical reactions. The highest temperature required during the process is 410 ℃. The electrical properties of TFTs using the film as the gate dielectric layer are comparable with that of TFTs fabricated in conventional methods. Nevertheless, when implemented both the solution processed SiO_2 film and the solution processed Si film in TFTs, the device performance was poorer than expected[13]. Based on his study, there are still some improvement that can be performed. To begin with, Although they reported the transfer characteristics of TFTs using solution processed SiO_2 (SP- SiO_2) as gate dielectric layer, they did not provide the electrical characteristics of the SiO_2 film such as the interface trap density and film integrity, which will be revealed in this study for the first time. Secondly, the film formation behavior of spin coating is not suitable for device printing technique and also suffers from a low material utilization efficiency, further researches are required to make it applicable to the roll-to-roll process. Last but not least, it is possible to further reduce the oxidation temperature in order to make the fabrication procedure compatible with flexible plastic substrates.

1.3 Research purposes

The goal of this project is to investigate the methods to fabricate high quality SiO_2 films on silicon substrate that meets the following requirements:

- Implement with liquid silicon materials in order to realize the solution process.
- Fabrication temperature should be limited to 400 ℃ in order to be compatible with the polyimide substrate.
- A non-vacuum process is required to further reduce the manufacturing cost and to be compatible with the roll-to-roll process.
- The quality of the film such as the interface trap density should be comparable with the oxide made by conventional technology.

MOS capacitors are fabricated using the resulting films to measure their electrical characteristics such as CV curves and IV curves. After that the interface state density, breakdown voltage and resistivity of the films are extracted from the measurement results.

1.4 Outline of the thesis

Chapter 2 provides an introduction on relative concepts and research status of the solution processed silicon dioxide films. In **Chapter 3**, the fabrication procedure of SiO_2 films using liquid silicon is discussed according to variable parameters. **Chapter 4** presents the fabrication process of MOS capacitors using the resultant dielectric films and results of electrical characterization. This is followed by further reducing the oxidation temperature to 350 ℃ in **Chapter 5**. Finally the study ends with conclusions and suggestions in **Chapter 6**.

Chapter 2 Solution Processed SiO_2 Films

This chapter will provide the theoretical basis of fabricating SiO_2 films using liquid silicon. The physical properties of SiO_2 will be given in section 2.1, which is a reference standard for the following measurement results. The physical and chemical reactions during the fabrication process will be described in section 2.2. in the last section, we will present the analysis on factors influencing the resultant film in the literature.

2.1 Properties of SiO_2 films

SiO_2 films serve as high quality electrical insulators in thin film transistors, they are always play an significant role in the integrated circuit technology. Actually the advantages of silicon dioxide were the main reasons why silicon emerged as the major material today for integrated circuit fabrication. As a characteristic feature of device geometries, oxide layers keep decreasing in size with the integrity technology and the quality has become a dominant factor in determining device functions. The same goes for thin film transistors, where the oxide quality governs their performance and stability.

All the SiO_2 properties are related to the preparation process and the crystal structure. The general references are listed in Table 2.1 which mainly for amorphous structures.[19] [20]

Table 2.1 Properties of SiO_2

Density	Related to fabrication processes, 2.2g/cm^3 for amorphous SiO_2
Index of refraction	The higher the density, the larger the refraction index. Approximately 1.45 when the incident light wavelength is 550 nm
Resistivity	Related to the amount of impurities in the film. About $10^{16}\Omega\cdot$cm for dry oxidation films.
Dielectric strength	Representing voltage tolerance， normally between 10^6 and 10^7 V/cm
Dielectric constant	Representing capacitive properties, ε_{SiO2} equal to 3.9.

2.2 Producing SiO2 films from liquid silicon

Cyclopentasilane(CPS), a cyclic silicon compound with chemical formula Si_5H_{10} , is chosen to develop the liquid precursor that can be used to form a silicon or a silicon dioxide film according to the following considerations. Firstly, CPS is a liquid compound in room temperature, which is necessary for a solution process. Secondly, CPS itself excludes carbon and oxygen components, which can reduce the concentration of impurities in the formatted silicon layer. Thirdly, its pentagonal structure is relatively stable compared to other hydrogenated cyclic silanes and finally it is able to undergo ring-opening polymerization upon ultraviolet light irradiation. The strategy of converting CPS into silicon dioxide films was first

reported by Hideki Tanaka et.al that including the following physical and chemical reactions. [12]

Photo-induced ring-opening polymerization

The boiling point of pure CPS is 194 ℃. However, a temperature over 300 ℃ is required to break their silicon and hydrogen bonds and construct a Si network, which means CPS will evaporate before thermal decomposition. Fortunately, one way to address this problem is to apply the photo-induced ring-opening polymerization. When a UV light irradiates on the hydrogenated cyclic silanes, it provides sufficient energy to cleave Si-Si bonds. Thus CPS open their rings and form $–(SiH_2)_5–$ radicals. Theoretically these radicals polymerized by backbiting reaction and a high molecular weight polysilane chain can be obtained.

Compared with fresh CPS, chemical properties of polysilanes are more stable to avoid violent chemical reactions when they encounter water or oxygen molecules. In terms of physical properties, polysilanes have a long chain or even net structure, therefore they possess a relatively higher boiling point to eliminate solution evaporation during annealing. In addition, the solution will become viscous or even be converted into solid state if the exposure time is long enough. Since polysilanes can be dissolved in pure CPS solution or the solution mixing with CPS and an organic solvent. The viscosity of the solution and the concentration of the polysilanes can be adjusted by diluting, which has a great impact on the solution adhesion ability to the silicon surface and the resultant film thickness.[21] [22]

Amorphous silicon formation

After the UV light irradiation, the liquid containing CPS, polysilane and organic solvent was spread on a quartz substrate. Then the wafer was baked on the hot plate in the inert gas environment in order to break Si-H bonds and form the amorphous silicon (a-Si) network. During the heating process, volatile materials such as CPS and organic solvent first evaporated. After that, as the binding energies of Si–Si and Si–H are 224 kJ/mol and 318 kJ/mol respectively, the Si-Si bonds first began to break at a temperature below 280 ℃, releasing some amount of SiH_2 and SiH_3 gas. This was followed by Si-H bonds breakage at around 300 ℃ and a three-dimensional amorphous silicon network start to form. In practice, the film formed at a temperature lower than 300 ℃ was not completely converted into amorphous silicon network. It still contains many hydrogen atoms and is easy to oxidize in the air. The quality of the a-Si network can be further improved by increasing the baking temperature, however the low quality a-Si films could be a good start to form SiO_2 films.[23]

Oxidation

In order to finally obtain the SiO_2 films, the wafer should be taken out from the inert gas atmosphere and be transferred to an environment contain oxygen. To maintain a non-vacuum process, the heating treatment was performed on the hot plate in the open air. The oxidation mechanism has not been fully clarified. There might be two possibilities. One of which is thermal oxidation that the Si-Si bonds break and the oxygen atoms insert in between to form the

bridge bonds. Another possibility is the connection of oxygen atoms and silicon radicals, which result from the previous processing steps.

2.3 Factors affecting the preparation process

The literatures regarding to solution-processed silicon dioxide films fabrication have revealed that there are many factors affecting the SiO_2 preparation. These can involve UV light exposure time, CPS concentration , baking time period, oxidation temperature and so on. We devote this section to discuss their influence.

Environment inside the glovebox

Violent oxidation reaction occurs when CPS exposes in the air or water. Therefore experiments should be done in an inert gas environment. Normally, before the oxidation step, the experiments processed in a glovebox filled with nitrogen gas. Both the oxygen and the water level in the glovebox should be kept less than 0.1p.p.m. It has been reported by [12] that to form an a-Si film, the oxygen content in the resultant film was limited to less than 2000 ppm by strictly maintain the oxygen concentration in the glovebox less than 0.5p.p.m. Once a slight failure occurred in controlling the oxygen level in the glovebox, a silicon film with an oxygen concentration of 8000p.p.m.was generated.

Surface treatment

When a liquid is brought into contact with a solid surface, an intimate molecular contact is established. The ability of the substrate to be covered the liquid, which is referred to as wettability, should be taken into consideration. We first assume that the substrate is an ideal flat surface, then two kinds of forces are applied across the interface at the same time. One is due to the incomplete structures and the dangling bonds on the solid surface, there exists an adhesive force that the liquid molecules are attracted to maintain contact with the solid surface. The other one is the cohesive force resulting from interactions among molecules in the liquid that gather the liquid to form droplets. If the former force is greater than the latter, then the liquid can spread over the solid surface which indicate a wetting situation.

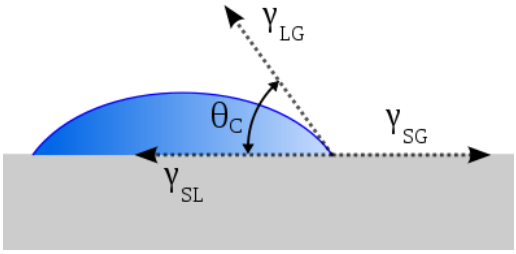


Figure 2.1 Schematic of the contact angle[24]

Contact angle θ_c is introduced to quantify wettability. At the place the liquid, gas and solid state intersect, the system maintains a stable state by balancing surface tensions of solid and liquid,

liquid and vapor as well as solid and vapor state aiming to minimize its total energy. The contact angle θ_c is the angle at the three-phase boundary as shown in Figure 2.1, where γ_{SG}, γ_{SL} and γ_{LG} are solid-vapor, solid-liquid and liquid-vapor interfacial energy, respectively.

A zero degree contact angle represents a complete wetting situation that the liquid can fully spread on the solid surface and form a film thereon. A rather common situation is called partially wetting that the liquid tends to spread on the solid surface with a contact angle less than 90°. When the contact angle is greater than 90°, dewetting happens which means the involved two materials cannot contact well or even exclude each other. In case of water spread on a solid surface, the surface with small contact angle is called a hydrophilic surface and with large contact angle is called a hydrophobic surface.

In reality solid surfaces always contain roughness structures. Different models were built to describe the influence of the surface roughness on the wetting level. For instance Wenzel model assumes that the liquid will fill the grooves of the rough surface and actually increase the contact area between the liquid and the solid substrate. As a result the total liquid–solid interaction will be enhanced and the wettability will be improved. Besides, Cassie-baxter model provides another description regarding to the dewetting situation. As the liquid tends to form droplets on the surface, it may not full fill the roughness structures and the air may be trapped under the liquid. Thus the area between the liquid and the solid is further reduced and the droplets might become more unstable.

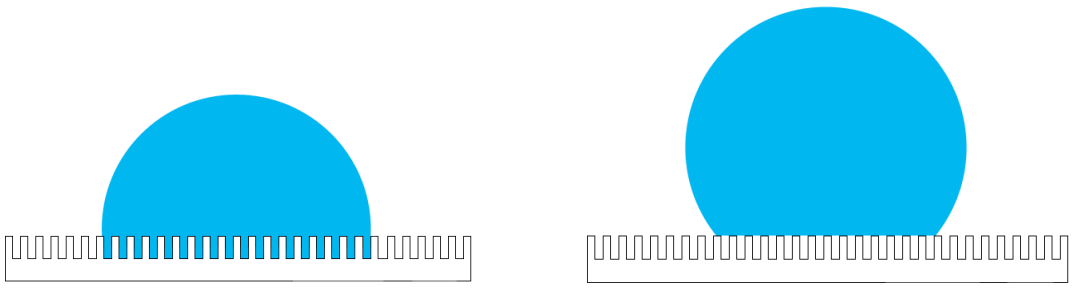


Figure 2.2 Wenzel model (left) and Cassie-baxter model (right) describing the influence of the surface roughness on the wetting level [24]

The surface treatment such as plasma etching or HF dip etching can effectively remove the surface contamination and native oxide, which makes the initial state of the silicon wafer controllable. However, the concomitant surface polarity change is a complex issue. Generally the HF-treated surface exhibits good hydrophobic and oleophilic properties. In contrast, the surface treated with oxygen plasma tend to be hydrophilic because of the presence of hydroxyl (-OH) groups.

Furthermore, wetting level can be improved by increasing temperature. Since temperature rising weakens the cohesive force between liquid molecules and decreases the surface tension of the

liquid. In addition, higher temperatures lead to a better intermixing, and wetting level would be better with greater mutual interpenetration.[25] [26]

UV exposure time

In order to avoid violent evaporation of CPS during thermal decomposition process, polymerization process was applied under the condition of UV irradiation. The cyclic CPS were expected to open their rings and transform into polysilane. However, in practical the reaction is more complicated.

A detailed description was presented by Dong Lim Kim et.al. In general, the photon energy of UV light is large enough to cleave Si-Si bonds of CPS molecules. But if more than one Si–Si bond is broken in a single CPS molecule, small pieces of silicon radicals will be created. These fragments will remain in the solution and the polymer structure will be hard to construct. Besides, although the bond energy of the Si-H bond (76 kcal/mol) is higher than Si-Si bond (53 kcal/mol), the Si-H bonds breakage still occurred almost simultaneously since UV light provided sufficient energy. Those silicon dangling bonds created by hydrogen loss connected with each other and the resulting polysilanes are not in a linear chain shape but in a more complicated form. In short, both the atom concentrations and molecule structures are in dynamic changes during the UV exposure process.

Their research also provided that the amount of broken bonds is associated with the UV exposure time. The breakages of both Si–H and Si–Si bonds will increase with a longer UV light time. While the concentration of hydrogen in the polysilane solution will decrease in the meantime. Nevertheless, large amount of CPS were converted to polysilanes during the photo-induced polymerization procedure. As a result, the solution will become viscous and it will be difficult for polysilanes to dissolve in the solution lack of CPS. In the real process, the exposure time was regulated with the expectation that only part of the CPS is converted into polysilanes and these polysilanes dissolved in the unreacted CPS solution.[22]

Baking time and temperature

In order to determine a proper timing and condition for oxidation, a two-step baking strategy was carried out during the process. The film was first baked in an inert gas environment below 300 ℃. This was followed by an oxidation step that baked the samples in the open air. Due to safety considerations, the baking temperature inside the glovebox had better be higher than 194℃, which is the boiling point of CPS, to ensure that the CPS molecules have completely evaporated before exposing the film in the open air.

To maintain a low temperature process, the state to oxidize the silicon is important. At the time point that the Si-Si bonds have been actived and the a-Si network starts to form, the layer can be transferred to an environment contain oxygen. Oxidize too early will result in a loose oxide film because CPS and polysilane are quite sensitive to oxygen. On the contrary, if the a-Si has been well formed and then the oxidation will require a high temperature.

The quality of resultant amorphous Si films after baking in the glovebox as a function of baking temperature was reported by Takashi Masudaa et al.

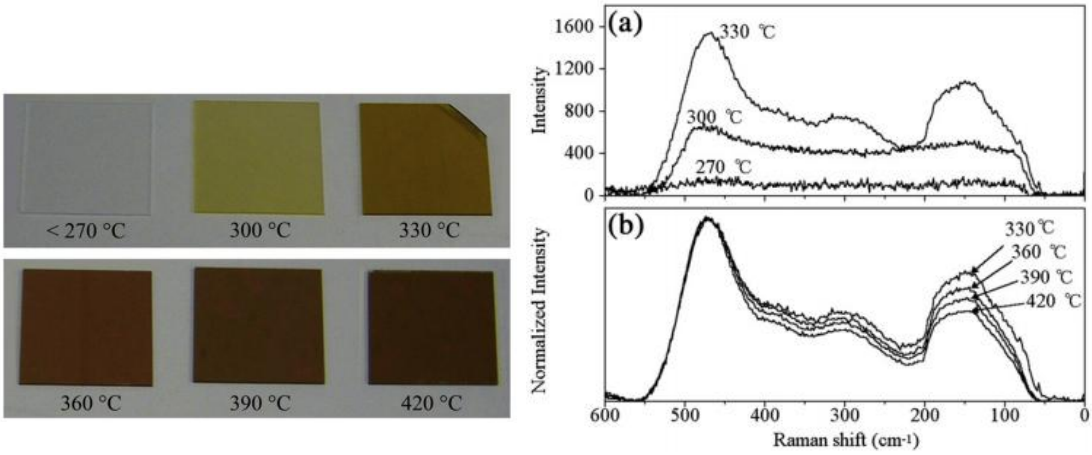
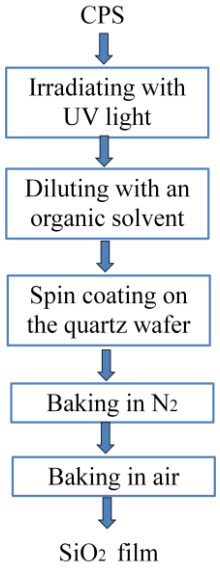


Figure 2.3 Photographic image of solution processed silicon films (left), Raman spectra of SP-Si films prepared in different annealing temperature.[23]

The photographic image of silicon films prepared by liquid silicon is presented in Figure 2.3 (left). The film is fabricated by spin coating the liquid silicon on a 2 by 2 cm^2 quartz substrate. After that the films experienced a polymerization process at temperatures range from 270 to 420 ℃. the apparent colors indicate that the film baked under 270 ℃ is transparent, it turned out to be yellow or brown when the temperature condition for polymerization are higher than 300 ℃. The colors indicate the existence of semiconductor material. It suggested that amorphous silicon structures starts to form at a temperature near 270 ℃.

The Raman spectra test was carried out to prove the inference. The results are shown in Figure 2.3 (Right). The picture (a) provides the Raman spectra of films baked at a lower temperature, on which typical characteristic peaks of amorphous silicon are not obvious. For polymerization temperature higher than 330 ℃, the amorphous silicon Raman spectra can be clearly detected as shown in picture (b). Theoretically, the peaks of a-Si Raman shift at 476, 387, 288, and 154 cm^{-1} have been assigned to transverse optical, longitudinal optical, longitudinal acoustic, and transverse acoustic band, respectively. These measurement revealed that the silicon start to construct a three-dimensional network with the baking temperature near 330 ℃.[23]

Combining the amorphous silicon formation and oxidation process together, according to the study by Hideki Tanaka et al., a complete process flow is presented in Figure 2.4. Although research showed that temperature at least 270 ℃ is required to construct a-Si network, their study suggest that 220 ℃ is sufficient for the first baking step.



	Sample 1	Sample 2	Sample 3
First step (in N_2)	220°C 60 min.	270°C 60 min.	315°C 60 min.
Second step (in air)	410°C 30 min.	410°C 30 min.	410°C 30 min.
Color	colorless	light auburn	auburn

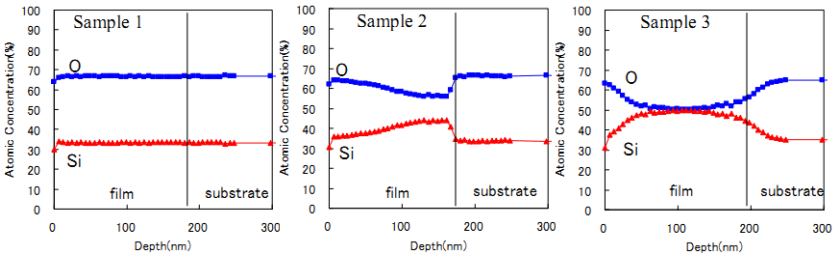


Figure 2.4 Fabrication steps, baking conditions and XPS results of SiO2 films made by H. Tanaka[13]

Three samples were treated for comparison. The baking temperature in Nitrogen atmosphere were 220 ℃, 270 ℃ and 315 ℃ for sample 1 2 and 3 respectively and the same baking condition for the oxidation step. The apparent color after oxidation suggested that sample 1 had been converted into SiO_2 whereas for sample 2 and 3, they were still Si-rich films. The X-ray photoelectron spectroscopy tests also convinced that the oxidation was insufficient in the deep area of sample 2 and 3. Therefore a higher temperature treatment during the first baking step is not necessary. On the contrary, it lead to a well formed a-Si structure and makes the oxidation difficult at low temperatures.[13]

To sum up briefly, silicon-dioxide has become an indispensible part in the integrate circuit with its stable physical and chemical properties. Basic steps of fabricating SiO_2 films using liquid silicon include photo-induced ring-opening polymerization, amorphous silicon formation and oxidation. During the procedure, related parameters such as the UV exposure time, oxidation time and temperature will influence the quality of the final resultant films. Furthermore, these parameters may be adjusted according to specific requirements and fabrication environment that will be discussed in the next chapter.

Chapter 3 Fabrication of SiO_2 Films Using Liquid Silicon

In this chapter we will first present our experiment procedure of preparing liquid-silicon-based SiO_2 films in Section 3.1. The Doctor blade coating method will be implemented to make the process compatible to a roll-to-roll technique. The fabrication parameters as we introduced in chapter 2 will be optimized with the help of many physical property and chemical composition measurements. The measurement instruments and results will be presented in section 3.2 and in section 3.3 we will describe the way we adjusted those fabrication parameters.

3.1 Experiment procedure and phenomena

During the experiments, most operations were carried out in the glovebox. An outside view of the glovebox is shown is Figure 3.1(left). The box is sealed and filled with Nitrogen gas. The water and oxygen levels inside were maintained to be less than 0.1p.p.m. Operations can be down through the gloves by side. We transferred wafers in and out of the glovebox through a vacuum chamber so the inert gas do not need to be refilled after that. Reagents such as CPS and cyclooctane required for the experiments were stored in the glovebox. Besides, equipments including UV light and hot plate were also installed in the glovebox so that UV exposure and hot plate baking processes can be performed in the inert gas environment. The right side picture of Figure 3.1 is the furnace which was used for oxidation. A constant air flow of 4-5 volume changes per minute ensures an adequate oxygen supply in the furnace.

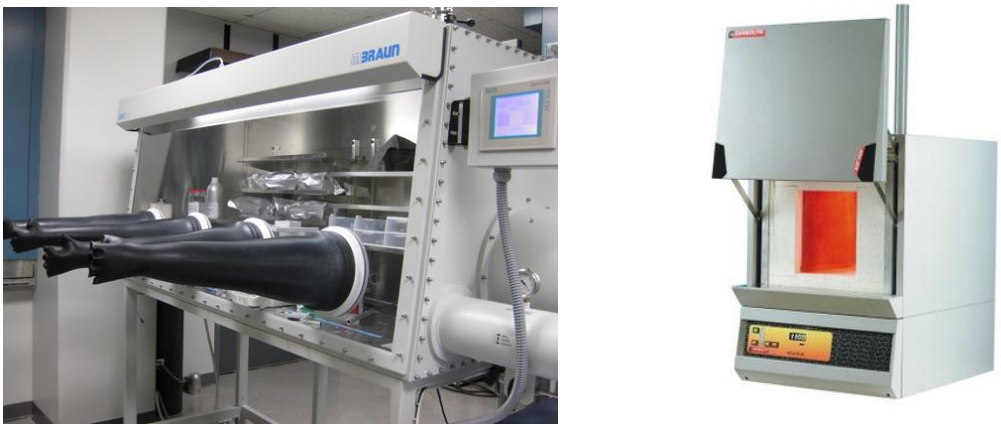


Figure 3.1 Mbraun Glovebox(left) and Carbolite Furnace(right)[2728]

To effectively fabricate SiO_2 films using liquid silicon, several conditions and parameters were tested during the study. An optimized procedure is as follows:

1.The experiment started with the surface treatment of crystalline silicon test wafer. Dip etching the wafer with 0.55% Hydrofluoric acid (HF) for 4 minutes to remove the native oxide and

leave a smooth surface.

2.The wafer was transferred into the glovebox and its surface was cleaned using a N_2 gun before blade coating.

3. The solution was prepared by diluting CPS with cyclooctane to make the CPS concentration approximately 50vol%. Mixing these liquids in a small beaker by putting a stirring bar inside and spinning for 3 minutes.

4. A Silicon Nitride blade was used to spread the mixed solution on the surface at room temperature. Blading 3 to 4 times to make the layer thinner enough while avoid scratches on the surface at the same time.

5. The wafer was placed under UV light irradiation to undergo the photo-induced ring-opening polymerization. During the time the organic solvent evaporated slowly and the film started to solidify.

6. Baking the wafer at 200 ℃ on a hot plate in the inert gas circumstance for 1 hour to form a-Si network. After baking the apparent color of the film was brown and blue. Then the wafer was transferred from the glovebox to the furnace.

7. Baking the wafer in the furnace which contain air inside for the oxidation reaction. The baking temperature is 400 ℃ and baking time is 30 minutes. After that the apparent brown color on the film became lighter while the area of blue part reduced and converted into dark brown.

Factors listed in Table 3.1 were adjusted to determine a combination that provided the best result during the process.

Table 3.1 Fabrication parameters that are controlled during the experiment

Surface treatment	0.55% HF dip etch / Argon plasma / Oxygen plasma
CPS concentration	30% ~100%
Spreading method	Si_3N_4 blade coating / polyimide blade coating / spin coating
UV exposure time	15minutes ~ 30 minutes
Hot plate baking	150 ℃ ~200 ℃
Oxidation time	30 min~3hours
Oxidation temperatures	350 ℃~ 400 ℃
Post annealing	postmetallization anneal / postoxidation anneal

A detailed discussion will be given in section 3.3 after we introduce the measurement methods. We also considered about reducing defect charge densities in the film which related to the post annealing methods presented in the table. This will be discussed in Chapter 4

3.2 Measurement methods

3.2.1 Apparent colors and optical microscope inspection

The thickness of the oxide layer can be estimated by comparing the color of the resultant film with the reference color as shown in Figure 3.2. The reference color is defined based on the structure of the SiO_2 film on top of the silicon. When it is vertically illuminated with fluorescent light, part of the light is reflected by the SiO_2 surface while part of it goes through the oxide film and is reflected by the underlying silicon bulk. Due to the thin film interference principle, constructive interference occurs and enhances a certain wavelength that corresponds to the apparent color on the wafer. Any thickness less than 200 nm is of interest in this experiment. As can be seen from Figure 3.2, SiO_2 film thicker than 20 nm is transparent, it gradually changes from a tanned to a dark brown color where thickness ranging from 50 to 100 nm are concerned, and then turns blue and becomes lighter when it increases to 150 nm. After that the colors vary periodically with the thickness. The apparent colors can also provide an overview of the film uniformity. When some colorful streaks appear on the surface, the formatted film might be in a shape of wave.

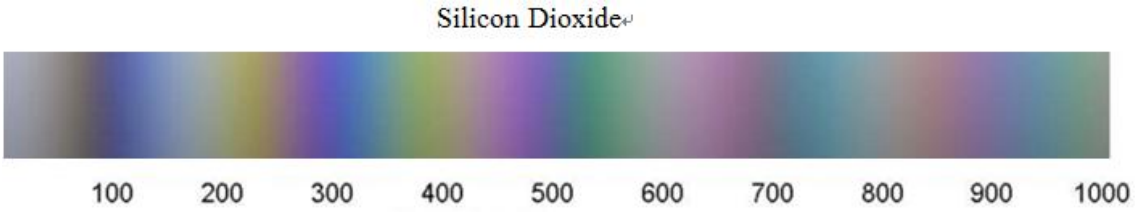


Figure 3.2 Reference color for SiO_2 films corresponds to film thickness in nanometers[29]

It should be noted that the apparent color is a combination of the material's natural color and the color produced by interference. It can always be seen that after oxidation, the color of the film will be lighter than before. Although the thickness of the silicon dioxide will increase after heating up in the open air, the amorphous silicon itself is yellow or light brown while SiO_2 is transparent.

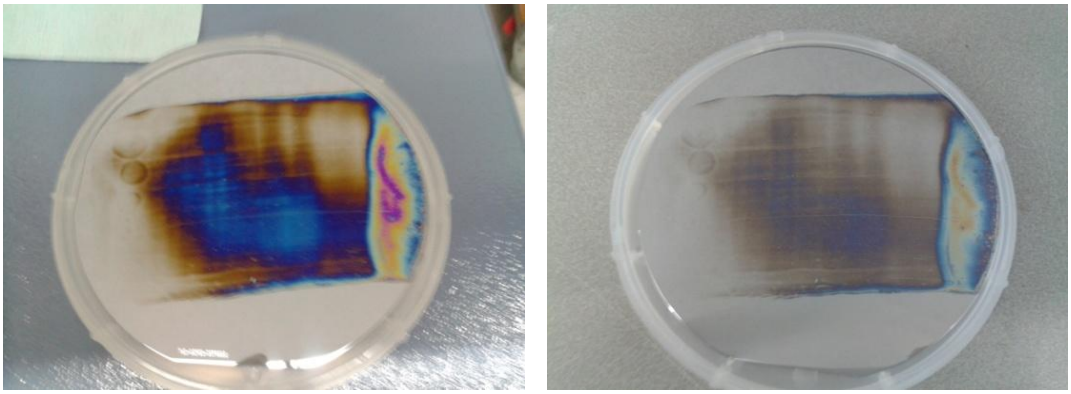


Figure 3.3 Comparison of film colors before and after oxidation

Figure 3.3 gives a comparison of film colors before and after oxidation. The brown and blue color after oxidation indicates the film thickness to be 50-150 nm while there is a thicker part of over 200nm alongside which results from the liquid spreading process.

Through an optical microscope with maximal 100 times magnification, details on the surface of the film can be observed such as cracks, scratches, rings and surface roughness, all of which give a first impression of the film quality.

3.2.2 Thickness measurement using Surface Profiler

Surface profiler can be used to measure the step height of a film. To determine the thickness of the film, a step that connects film surface and bare silicon substrate need to be prepared by means of the following process. First one has to pattern the film with the photoresist, the shape of the pattern is not highly demanded but has to contain clear covered and uncovered areas with straight edges. Subsequently, the SiO_2 area without photoresist coverage was etched away by BHF solution. Finally the photoresist was removed with acetone. The surface profiler implemented in our study is DekTak 150. The measurement results were consistent with the apparent color and would provide a reference of specific thickness ranges for the ellipsometer measurement.

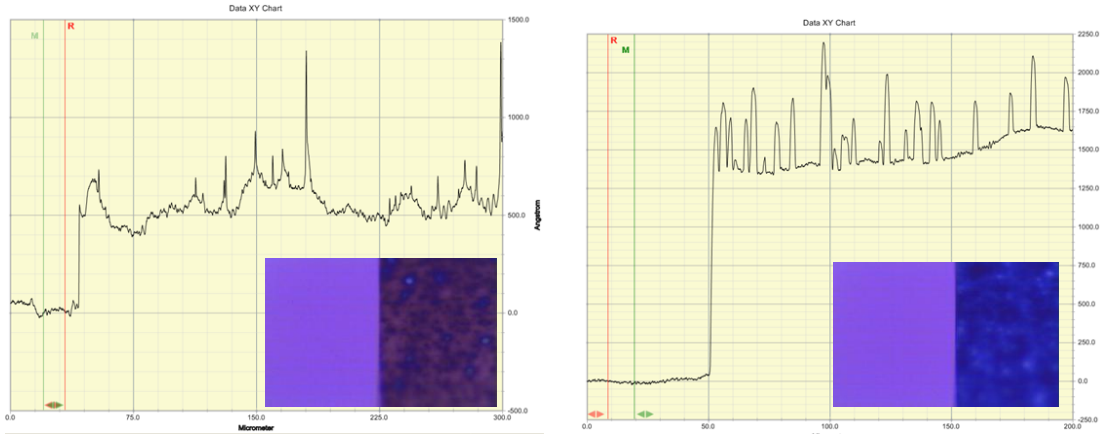


Figure 3.4 Surface Profiler results on the film in brown (left) and the film in blue (right)

As illustrated in Figure 3.4, the brown film is approximately 50 nm and that the film in blue is about 150 nm thick. At the same time, the pictures also reveal a rough surface with hills and valleys that need to be optimized. Since the needle will bounce or be tripped when it goes through some obstacles, the testing result may suggest the surface roughness in general, even though the exact scales of the particles are inaccurate.[30]

3.2.3 Surface morphology measurement using Atomic Force Microscopy

It was always detected under the optical microscope that there were some black dots exist on the surface when the film thickness was less than 100 nm. An atomic force microscope (AFM) test was thus implemented to give a deep view of the phenomena.

The working principle of the AFM involves having a probe mounted at one end of an elastic cantilever. When the probe is scanning on the sample surface, the repulsive force between the atoms of the probe and the sample surface make a slight deformation of the cantilever. A laser incident to the back side of the cantilever and its reflected light is detected by a photo detector. In this way the deformation of the cantilever can be accurately measured and the surface morphology of the film can be determined.[31]

The sample piece taken from the resulting film is shown in Figure 3.5 (left) by a microscope inspection of a 50×50 um^2 area, the corresponding AFM result is presented on the right.

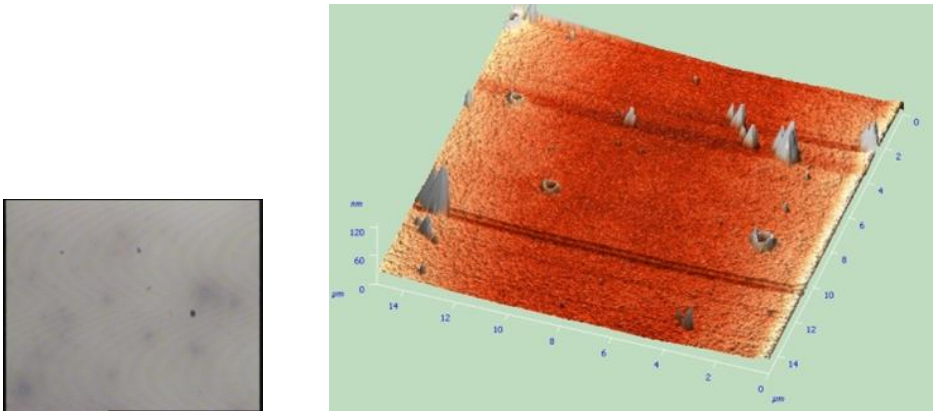


Figure 3.5 AFM result regarding the morphology of the solution processed SiO_2 film surface

The result indicates that the black dots on the surface are actually small peaks and rings. There are many reasons that may lead to these severe defects. For instance an over polymerization under UV light exposure or the evaporation of liquid molecules during baking processes. All of the defects involving pinholes or film thinning, particles, micro-roughness and so on will affect the functions of the film.

3.2.4 Component measurement using the Raman microscope

The Raman spectrum measurement based on the Raman scattering principle, can be used to characterize materials and their structures. Amorphous silicon shows a wide peak on a Raman shift positioned at 480 cm^{-1}. In our experiment, we implement Raman measurements to detect the film state before oxidation.

A solution-processed film was formed on a glass substrate. After baking it for 1 hour at 200 ℃ in an inert gas atmosphere, it was taken out of the glovebox and the Raman measurement immediately continued. The differing results of the thicker and thinner part of the film are shown below.

In the left picture of Figure 3.6, the black line reveals the Raman spectrum of the solution processed film, the thickness of the film is estimated to be more than 100nm. The red line gives the reference amorphous silicon spectrum. Through comparison it can be concluded that in this case the amorphous silicon has begun to form but has quite a low quality.

In the right picture of Figure 3.6, the blue line shows a Raman spectra of the solution processed layer which is less than 100 nm thick. The green line shows the Raman spectra of the bare glass substrate. The overlap of these two lines suggests that the layer has been completely oxidized in the open air at room temperature or that the Raman characterization cannot be detected on a very thin layer.

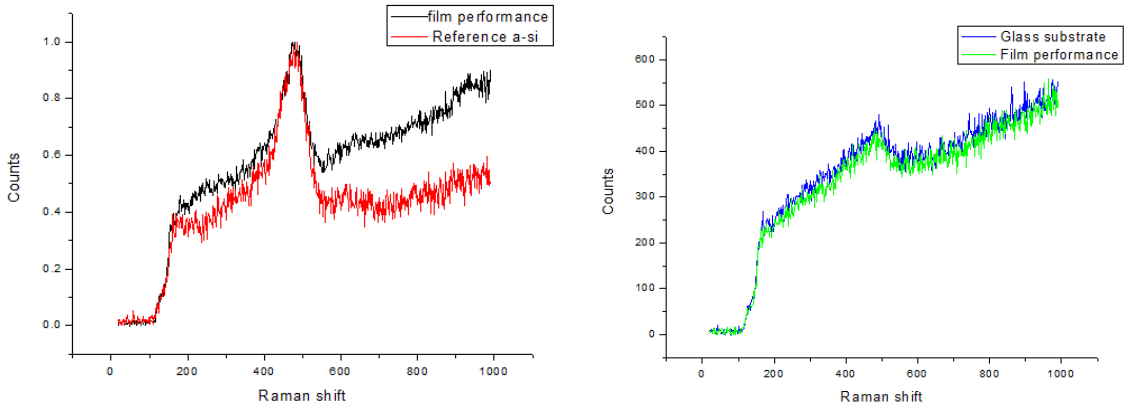


Figure 3.6 The Raman spectrum of the thicker part on the solution processed film compared to the reference amorphous silicon spectrum (left). The Raman spectrum of the thinner part of the solution processed film compared to the spectrum of bare glass substrate (right).

3.2.5 Dielectric constant measurement using Ellipsometer

The optical properties and thickness of the film is measured by ellipsometer, which in principle measure the change in polarization between light reflects or transmits from the layer and the incident light. The polarization change is represented by an amplitude ratio, Ψ, and a phase difference, Δ. commonly given as:

$$\rho = \tan\psi e^{i\Delta} \tag{3.1}$$

The data acquisition process is as follows: An unpolarized light is sent through a polarizer in order to be converted into a linearly polarized light and then incident on the sample surface. It becomes elliptically polarized after reflecting from the film surface. Next, the light goes through an analyzer which is a continuously rotating polarizer that function as filtering out components of the light in different vibration directions. Finally the polarization result is determined by a detector. The polarization change caused by the sample film reflection can be obtained by comparing the result signal with the incident light signal.

With regard to data analysis, it is vital to construct a model which provides theoretical responses of polarization corresponding to films with different thickness and optical constants. In this experiment, Since liquid silicon started to form a-Si films when they were heated up in the insert gas environment, and followed by an oxidation process in the open air in a higher

temperature, under the consideration that the surface of the resulting layer might be converted into SiO_2 while inside the film it might still be a-Si, a model of SiO_2 layer on top of amorphous silicon layer was built in our study.

As we know, optical constant varies with frequency but it is complex to make a disperse definition towards each frequency. Therefore Mathematical models are founded to describe relations of optical constant and wavelength. For SiO_2 which is a transparent material, Cauchy relationship is used to model the refractive index, given as

$$n(\lambda) = A + \frac{B}{\lambda^2} + \frac{C}{\lambda^4} \tag{3.2}$$

where parameter A,B and C can be adjusted to fit the actual index of the material.[32]

In general, the refraction index and the film thickness are both adjusted as fitting parameters in order to characterize the film. A reference factor, Mean Squared Error (MSE), is used to quantify the difference between the measured and the theoretical curves. The profile corresponding to a minimum MSE value is regarded as the final result.

We regarded the MSE value less than 100 as a reasonable matching. In this case the experiment results showed that films with less than 150 nm thickness performed better. This is probably because a relatively thinner layer is easier to oxidize completely and convert from a-Si to SiO_2. For a thicker layer, the situation become more complex and the Si/SiO2 model is too simple to analysis. However, films less than 10 nm are difficult to detect using optical methods since it is hard to determine whether they are SiO_2 or the surface roughness. Even the measurement made a good matching, the gradients of the films still cannot be proved.

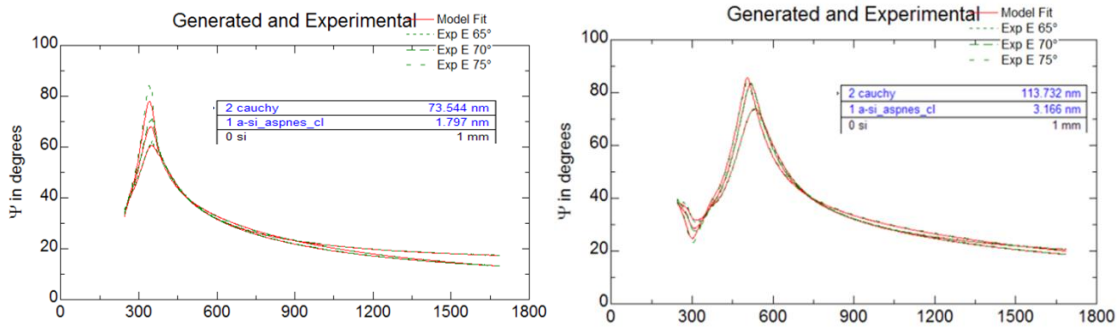


Figure 3.7 Ellipsometer measurement results of a brown part (left) and a blue part (right) on the film

The square of the refractive index is proportional to the relative permittivity. Theoretically the refractive index of SiO_2 is 1.45 and the relative permittivity is 3.9. The smaller the refractive index, the better the insulation of the material. We randomly choose an area of brown and an area of blue on the film for the measurement. The results are shown in Figure 3.7.

The result presented by the left picture of Figure 3.7 is a 73.54 nm SiO_2 layer on top of a 2 nm

thin amorphous silicon layer. The reflection index of SiO_2 in this case is 1.46 and MSE value of this measurement is 12.94. In an area of blue as presented on the right, result shows a thicker film as expected. The SiO_2 layer is 113.73 nm thick under which laid a very thin amorphous silicon layer. The SiO_2 reflection index equal to 1.44 and the MSE is 16.49.

3.2.6 Elemental composition measurement using X-ray photoelectron spectroscopy

X-ray photoelectron spectroscopy is in principle used for identifying the elemental composition at the sample surface. Since X-ray energies exceed the binding energy, when a material is exposed under it, electrons can be emitted from their orbital according to the photoelectric effect. XPS spectra are obtained by measuring the number and kinetic energy of electrons that escape from the surface of the material. XPS is simply suitable for elemental analysis on the surface because electrons excited only from the top 0.5–5 nm of the material are able to eject from the surface. Ion beam sputtering should be implemented to obtain a depth-profiling.[33]

All elements can be detected by means of XPS except hydrogen and helium. This time we focus on the ratio of Si and O atoms in the film and the concentration of carbon impurities. The measurements was performed using monochromatic AlKα-radiation and the spot size is 200 μm in diameter. To measure the depth profile, argon ions were used for ion-etching. The sputter rate is 7.4nm/minutes for pure SiO_2 films.

The detected result of elements and atomic concentrations (in percentage) at the surface are shown below. Two positions on the same sample were chosen for the measurement which gave almost the same results.

Table 3.1 Result of the atomic concentrations (at %) on the surface

position	C	O	Si	O/Si
Sample 1_a	2.2	65.5	32.3	2.03
Sample 1_b	2.3	65.4	32.2	2.03

Table 3.1 Indicates that the concentration ratio of silicon and oxygen atoms on the surface is consistent with the theoretical value. The 2.2% carbon concentration is mainly caused by Carbon dioxide in the air, they react with sodium ions on the film surface to form carbonate, thus carbon were absorbed onto the film.[34]

The depth profile measurement was carried out afterwards. For reference, a calibration sample of 116 nm thermal SiO_2 on Si has been measured as well. The concentration of O, Si and C were followed as a function of sputter time, the result is given in Figure 3.8.

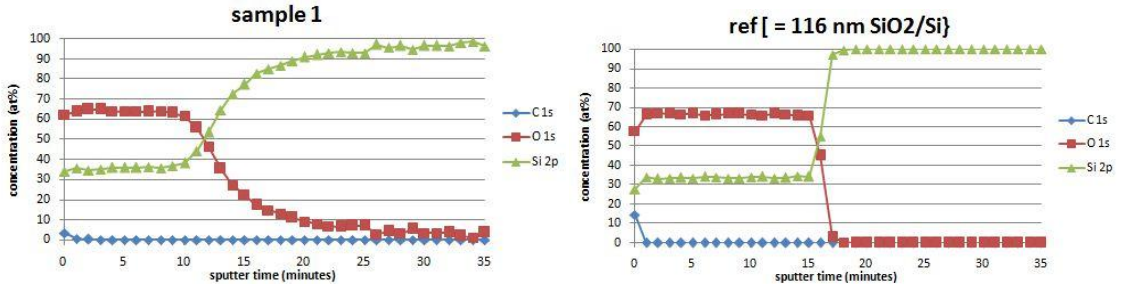


Figure 3.8 Results of the atomic concentrations in depth profile. Left: SP-SiO_2 sample with oxidation temperature of 400℃ , Right: thermal oxide reference sample

As can be seen from the result, no carbon was detected in the sample after 2 minutes of ion-etching, which means that diluting CPS with the organic solvent didn't induce carbon impurities to the resulting film. However, compared with the reference result, the average concentration ratio O / Si is 1.79 in the target sample, which indicates a insufficient oxidation. Furthermore, it should be noticed that in the right side picture of Figure 3.8, the interface between the layer of SiO_2 and the substrate of elementary Si is quite narrow in the reference sample. While a significantly broader interfaces was observed in the sample made from liquid silicon as shown on the left. The reasons may be firstly the in-homogeneities in the layer thickness within the measurement spot of 200 μm in diameter. Secondly, the interface was not oxidized sufficiently so that the O / Si ratio reduced dramatically near the interface.

3.3 Discussions

The films fabricated by liquid silicon various with many parameters and experienced a low reproducibility during the process. Nevertheless some of them are discussed here with regard to surface treatment, CPS concentration, spreading methods, UV light exposure time period, baking time period and baking temperature. The measurement methods we introduced in Section 3.2 would be of great help to evaluate the resultant film quality.

Surface treatment

The wetting ability of the contact surface between the liquid silicon and the solid substrate has a great impact on the quality of the resulting layer. 0.55% HF dip etch, oxygen plasma and argon plasma surface treatment methods were implemented respectively in this project.

The table and pictures in figure 3.9 show a comparation of the experimental results with different surface treatment conditions. Since native oxide are always distributed on the silicon surface loosely and randomly, in order to well control the initial state of the wafer surface, 0.55% HF dip etching was always carried out as the first step. For sample A, this was followed by blade coating directly while for sample B and C, a plasma treatment was added before coating. We first made a drop of pure CPS on the HF dip etched substrate when processing sample A, the contact angle was less than 90 degree which indicate a good adhesion to the silicon surface. Theatrically, if this surface is bombard with oxygen or argon plasma and become rougher, the

wetting ability should be improved according to the Wenzel model described in 2.3. However as to the experimental phenomena of sample B and C, the actual wettability were reduced when we treated the surfaces with plasma. This may due to the fact that the active bonds on the surface also changed because of the plasma treatment and their polarities might affect the interfacial physical and chemical reactions.

Comparing samples A B and C, the appearance of rings on the film draw our attention. These rings always appear during the UV light exposure but the causes are unclear. They may lead to cracks on the film because their existence changes the surface tension. A treatment of oxygen plasma could eliminate the effect. That is the reason why the film integrity of sample C is better than sample A and B. Drawbacks of oxygen plasma treatment is that it would lead to a dewetting situation if the bombard energy is too strong. Moreover, defects would also be induced in the Si-SiO_2 interface which influence the functionality of MOS capacitors when using these films as dielectric layers. An alternative way to eliminate the ring's effect is using a diluted CPS solution. The effect of CPS concentrations on the fabrication result will be discussed in the next section.

Table 3.2 Fabrication parameters for the surface treatment study

	Sample A	Sample B	Sample C
Surface treatment	**0.55% HF dip etch**	**Argon plasma**	**Oxygen plasma**
CPS concentration	100%	100%	100%
Spreading method	Si_3N_4 blade coating	Si_3N_4 blade coating	Si_3N_4 blade coating
UV light time	30 minutes	30 minutes	30 minutes
Hot plate baking	1 hour at 200 ℃	1 hour at 200 ℃	1 hour at 200 ℃
Oxidation	30 min at 400 ℃	30 min at 400 ℃	30 min at 400 ℃

Sample A Sample B Sample C

Figure 3.9 Comparation of the experiment results with different surface treatment conditions

Spreading liquid in a preheating circumstance will improve the wetting level but also lead to liquid evaporation, so the coating temperature should be carefully controlled to balance the situation. Since the wetting level is acceptable in room temperature in this case, we did not preheat the wafer in this study

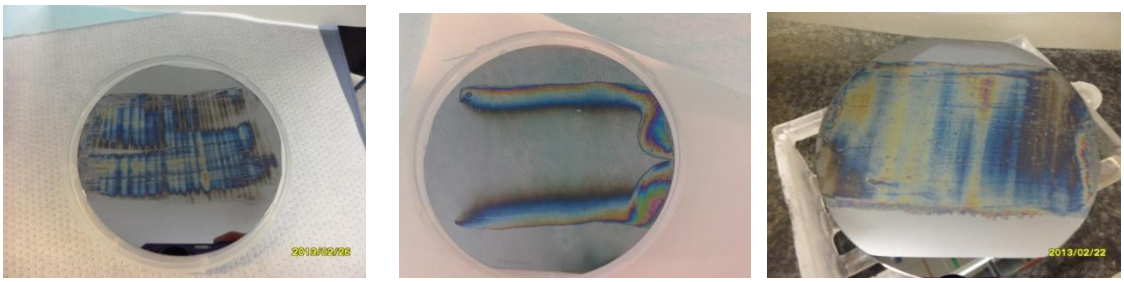
CPS concentration

The concentration of CPS solution influences the resultant film thickness, integrity and oxidation level. We adjusted different solution concentrations during the experiments and there are some phenomena that need to pay attention to.

To begin with, depositing pure CPS or high concentration CPS could result in a thick layer that makes a complete oxidation difficult. If we kept spreading the liquid forth and back in hope to make it as thin as possible, it would lead to many scratches or traces on the surface as shown in sample C. On the contrary, for the solution concentration lower than 30%, CPS will evaporate together with the organic solvent dramatically during baking processes, leaving a thin film less than 10 nm or making the resultant film uneven such as tens of nanometers thick in the middle and hundreds of nanometers by side as shown in sample D. Sample E made a compromise by applying a 50vol% CPS solution and a reasonable film is obtained.

Table 3.3 Fabrication parameters for the CPS concentration study

	Sample C	Sample D	Sample E
Surface treatment	Oxygen plasma	Oxygen plasma	Oxygen plasma
CPS concentration	**100%**	**30%**	**50%**
Spreading method	Si_3N_4 blade coating	Si_3N_4 blade coating	Si_3N_4 blade coating
UV light time	30 minutes	30 minutes	30 minutes
Hot plate baking	1 hour at 200 ℃	1 hour at 200 ℃	1 hour at 200 ℃
Oxidation	30 min at 400 ℃	30 min at 400 ℃	30 min at 400 ℃



Sample C Sample D Sample E

Figure 3.10 Comparation of the experiment results with different CPS concentrations

On the other hand, it is possible to expose the mixed CPS solution under UV light before blade coating. In this case during UV irradiation, the organic solvent would evaporate due to the elevated temperature and polymerization reaction occur at the same time. Consequently, compared with the diluting ratio of the prepared CPS and cyclooctane, the actual solution that spread on the silicon wafer will be much more viscous.

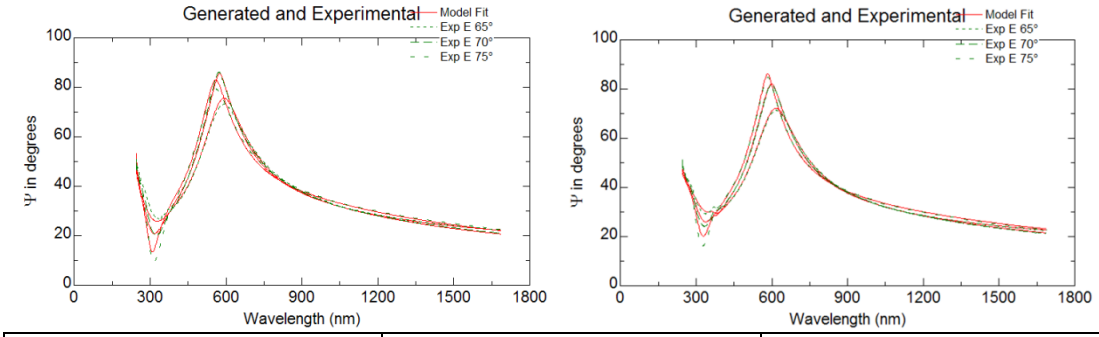
Spreading methods

Before we discuss the time period of UV light irradiation, we devote a paragraph here to consider the spreading methods regarding to spin coating and blade coating. The benefit of spin coating is to form a very uniform film. However, it is not suitable for a viscous solution. Meanwhile, spin coating required a large amount of liquid and is not compatible to a roll-to-roll process. For blade coating, Silicon nitride blade and polyimide blade are used during the research. The wetting level of both blade materials with respect to the liquid silicon are very low, therefore liquid silicon can stay on the silicon surface rather then been stick away by the blade. Polyimide blade is soft and without a sharp edge, so the uniformity of the resultant film can be better compared to the silicon nitride blade. However the applied force is limited due to its soft physical property, thus the resultant film was thicker than the film obtained by silicon nitride blade coating. For silicon nitride blade, on the contrary, a thinner layer can be achieved by multiple blading but steps and scratches will remain on the surface due to the applied unevenness force.[35]

UV light irradiation time

Table 3.4. Fabrication parameters for the study on UV light irradiation time

	Sample F	Sample G
Surface treatment	0.55% HF dip etch	0.55% HF dip etch
CPS concentration	50%	50%
Spreading method	Si_3N_4 blade coating	Si_3N_4 blade coating
UV light time	**15 minutes**	**30 minutes**
Hot plate baking	1 hour at 200 ℃	1 hour at 200 ℃
Oxidation	30 min at 400 ℃	30 min at 400 ℃



	Sample F	Sample G
SiO_2 (Cauchy model)	129.61 nm	143.23 nm
Si	55.69 nm	23.58 nm
reflection index	1.43	1.37
MSE	58.27	24.42

Figure 3.11 Ellipsometer results of the films with different UV irradiation time

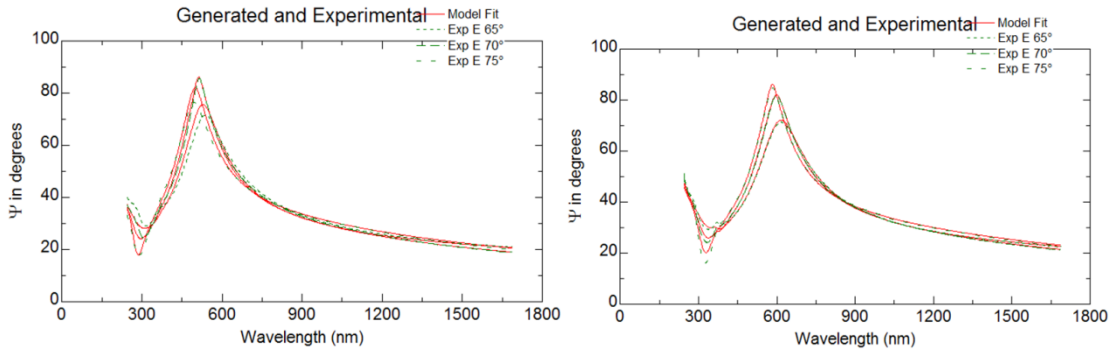
With the surface treatment of simply HF dip for 4 minutes, there were always some big partials formed on the film during UV light exposure and resulted in rings and cracks in appearance. Blade coating with the diluted CPS will reduce this effect however it still exists and influence the final MOS-C performance. Under the consideration that these particles might be big silicon clusters result from over polymerization, UV light irradiation time was adjusted aiming to weaken the effect.

The ellipsometer results of the produced SiO_2 films are presented in figure 3.11. The reduction of UV exposure time lead the CPS solution to be less viscous and the light-induced ring-opening reaction incomplete. Therefore violent evaporation occurred when the sample was heated up on the hot plate. This brought a rough surface as well as a loose polymeric structure. the results obtained from ellipsometer suggests that sample G with UV irradiation of 30 minutes performs slightly better result since its MSE value is lower than sample F. In addition, the phenomenon of rings on the surface still occurred and did not show any difference between those two samples.

In glovebox hot plate baking temperature

Table 3.5 Fabrication parameters for the study on the in-glovebox hot plate baking temperature

	Sample H	Sample G
Surface treatment	0.55% HF dip etch	0.55% HF dip etch
CPS concentration	50%	50%
Spreading method	Si_3N_4 blade coating	Si_3N_4 blade coating
UV light time	30 minutes	30 minutes
Hot plate baking	**1 hour at 150 ℃**	**1 hour at 200 ℃**
Oxidation	30 min at 400 ℃	30 min at 400 ℃



	Sample H	Sample G
SiO_2 (Cauchy model)	121.29 nm	143.23 nm
Si	41.56 nm	23.58 nm
reflection index	1.38	1.37
MSE	66.25	24.42

Figure 3.12 Ellipsometer results of the films with different in-glovebox baking temperature

From the ellipsometer results provided in Figure 3.11, it can be concluded that the film has not been fully oxidized because there existed a thin silicon film close to the silicon substrate. Therefore the in-glovebox hot plate baking temperature was investigated. We reduced the hot plate baking temperature so that the film was more reactive to the oxide. Thus the oxidation might be more complete and thorough.

Because the hot plate baking temperature in this case is lower than the boiling point of the CPS, sample H was placed inside the glovebox for one day before oxidation in hope to make it further solidified. However, apparent volatilization still occurred when putting the wafer into the furnace of 400 ℃. A touch of smoke can be observed when the film first went in contact with the hot air and small blank areas could be seen on the film when the wafer was taken out of the furnace after 1 hour baking. The ellipsometer analysis result is presented in Figure 3.12.

As can be seen from the result, apart from those blank areas on sample H that destroy the film integrity, the optical measurements did not indicate any improvement by means of reducing the hot plate temperature when baking the film in the inert gas environment.

Oxidation time and temperature

Table 3.6 Fabrication parameters for the study on the oxidation temperature

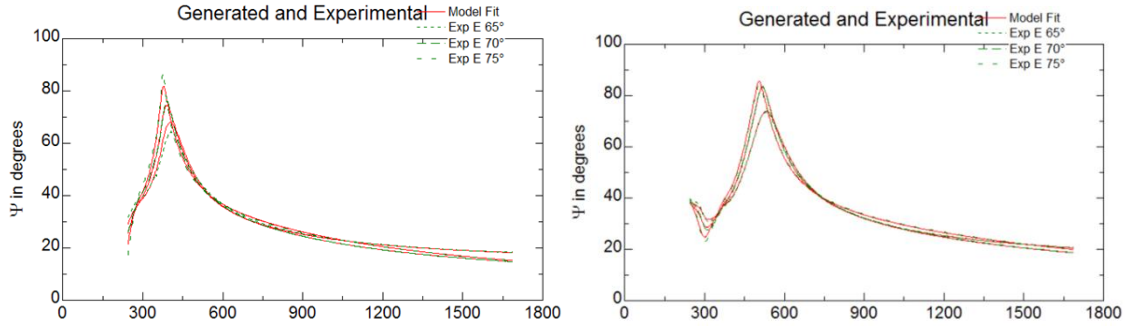
	Sample I	Sample J
Surface treatment	Oxygen plasma	Oxygen plasma
CPS concentration	40%	40%
Spreading method	Si_3N_4 blade coating	Si_3N_4 blade coating
UV light time	30 minutes	30 minutes
Hot plate baking	1 hour at 200 ℃	1 hour at 200 ℃
Oxidation	**30 min at 350 ℃**	**30 min at 400 ℃**

In the last step, the films that fabricated in the same condition in previous steps were annealed in the open air for half an hour in different temperatures as listed in the table. The fitting result of ellipsometer measurement is provided in Figure 3.13.

We compare the results of two samples that have almost the same thickness. It can be concluded that the oxidation is incomplete in 350 ℃ condition because the thickness of the silicon layer underneath the SiO_2 of sample I is larger than that of sample J. Besides, the refraction index of sample I is 1.29 while sample J is 1.44, the later one is more close to 1.45 of SiO_2 which indicate a better silicon and oxide ratio.

The samples were placed back into the furnace after a few days and heated up to 350 ℃ for 3 hours with the expect that the oxide in the open air would have enough time and energy to diffuse into the film and react with the rest of the silicon atoms. Unfortunately, the result afterwards were the same as before. The reasons might be that it is difficult for the oxygen to diffuse through the SiO_2 film in low temperature. Moreover, the amorphous silicon or poly

silicon structure may have been formed near the substrate which makes the bond break even harder.



	Sample I	Sample J
SiO_2 (Cauchy model)	95.66 nm	113.73 nm
Si	33.71 nm	3.16 nm
reflection index	1.29	1.44
MSE	30.5	16.49

Figure 3.13 Ellipsometer results of the films bake at different temperature in the open air

So far we have discussed all the parameters that can be well controlled or adjusted during the process and come to one of the best fabrication profiles as described in Section 3.1. A brief summery based on the above discussions are presented in Table 3.3.

Table 3.3 Summery of the parameters related to the fabrication result

Factors	Descriptions
Surface treatment	0.55% HF dip etching provided a better wetting level. Oxygen plasma etching reduced rings on the surface but induced the defects.
CPS concentration	High concentrations (100%) lead to a thick film. Low concentrations(30%) brought evaporation issues
Spreading method	Silicon Nitride blade coating was capable of forming a thin film. Polyimide blade coating provided a better uniformity.
UV light time	Shorter UV irradiation time (15 min) lead to a less viscous solution.
Hot plate baking (inert)	Low in-glovebox baking temperature cannot provided sufficient energy for a-Si network formation, resulting in a loose structure.
Oxidation	Low temperature (350 ℃) lead to incomplete oxidation.

In spite of these, there are still some uncertain factors that also affect the film quality. First and foremost, blade coating was done manually which means the blading pressure, angle and speed were impossible to quantify. Second, the pure CPS solution was completely fresh in the beginning but slowly oxidized over time even though we have placed them inside the glovebox. These factors limited the reproducibility of the film and need to be improved in the future.

Chapter 4 Electrical Characterization

In order to monitor the properties of the liquid silicon processed SiO_2 film and the SiO_2-Si interface, Metal-Oxide-Semiconductor Capacitors (MOS-C) were implemented due to their simplicity of fabrication and analysis. The dielectric layer of the MOS-C is made from liquid silicon as described in Chapter 3 and the rest steps are compatible with conventional semiconductor fabrication processes. The major specification of SiO_2-Si interface is presented by interface trap density D_{it}, which can be extracted from low frequency and high frequency capacitance versus voltage characteristics of the devices. The SiO_2 film integrity is evaluated by the breakdown field strength E_{bd} obtained from current-voltage (IV) measurements.

4.1 Theory

4.1.1 CV Characteristics of MOS Capacitors

To begin with, a brief introduction of CV measurement method will be presented. As we know, the capacitance is defined by taking derivative of charges on the plate regarding to the voltage across the capacitor, expressed as

$$C = \frac{dQ}{dV} \tag{4.1}$$

A differential voltage is required during the measurement. Thus the applied gate voltage (V_{AG}) consists of two components, a DC step varies voltage (V_{GB}) to set different operation modes or create different depletion width, which superimposed by a small AC voltage ($V_{GB}(\omega)$)to measure the MOS capacitance corresponding to every bias condition.[36]

MOS capacitor has three operating modes: accumulation, depletion and inversion. Start with ideal CV characteristics, one should assume that there is no fixed charge in the oxide and no charge trapped at the oxide-semiconductor interface. Take p-type substrate MOS capacitor for example, when placing a negative bias voltage on the gate, the negative charges will attract holes from the silicon bulk to the surface to form an accumulation layer. In this case, a differential change in the applied voltage will cause the change of the accumulated positive charges. The MOS capacitance per unit area in accumulation mode is the gate oxide capacitance. Expressed as

$$C'(acc) = C_{ox} = \frac{\varepsilon_{ox}}{t_{ox}} \tag{4.2}$$

Where ε_{ox} and t_{ox} are dielectric constant and thickness of the gate oxide, respectively.

When the gate bias is made positive and the MOS capacitor operates in the depletion mode,

holes are repelled to the bulk and the electron density near the silicon surface builds up to generate a space charge region. At this time a differential voltage change will lead changes in both the width of the space charge region and the charge density. The MOS capacitance per unit area in depletion mode is the gate oxide capacitance and depletion region capacitance in series combination. Given as

$$\frac{1}{C'(depl)} = \frac{1}{C_{ox}} + \frac{1}{C_S'} \tag{4.3}$$

In which the depletion region capacitance $C_S' = \varepsilon_{si}/x_d$, and x_d is the width of the depletion region.

Threshold inversion point occurs at the situation that depletion region width reaches its maximum and the charge density of the inversion layer is zero. The minimum capacitance obtained at this time is

$$C_{min}' = \frac{\varepsilon_{ox}}{t_{ox} + \left(\frac{\varepsilon_{ox}}{\varepsilon_{si}}\right) x_{dT}} \tag{4.4}$$

Where x_{dT} is the maximum depletion region width.

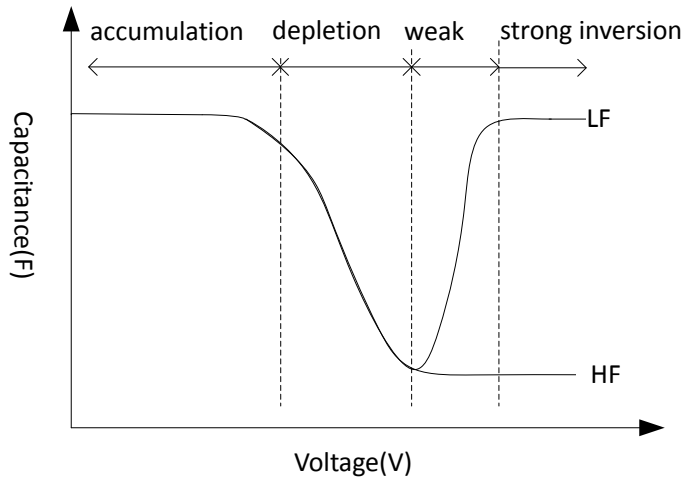


Figure 4.1 Ideal high frequency and low frequency Capacitance-Voltage curves[37]

When the positive gate bias is further increased to inversion condition, depletion region width remains and electrons form a thin inversion layer near the surface. Sources of the electrons are diffusion of minority carriers from the p-type substrate and thermal generation and recombination in the space charge region. Therefore the electron concentration cannot change rapidly. If the differential voltage across the MOS capacitor changes in a low frequency that the electrons could keep pace with, the total capacitance is the gate oxide capacitance. Given as

$$C'(\text{inv}) = C_{ox} = \frac{\varepsilon_{ox}}{t_{ox}} \tag{4.5}$$

Meanwhile, if the applied ac voltage changes in a high frequency, the electrons are not able to response and the capacitance is then stay on C'_{min}. An theoretical CV curve is shown in Figure 4.1. [37]

The above discussion is based on ideal assumptions, while in practice, the existence of charges in the gate oxide and the oxide-semiconductor interface will affect the CV characteristics.

In the following sections, the influence of non-ideal factors on the CV curves will be discussed. Three kinds of defect charges were taken into consideration, namely interface trapped charges, fixed oxide charges and mobile ionic charges.

The interface trapped charges Q_{it}, also known as interface states, origin from the discontinuity of the crystal structure or oxidation-induced defects. They are located at the Si-SiO_2 interface and provide energy states that can capture and emit charges. Those interface trapped charges can follow the slowly varying gate bias voltage and also respond to a low measurement frequencies. On the contrary, they do not contribute a capacitance in the high frequency measurement result. Thus during the measurement procedure, capacitance measured in high frequency can be regarded as a reference curve and the difference between it and the low frequency measurement results are caused by the interface states.

The equivalent circuit in low and high frequencies are presented in Figure 4.2. Cs is the semiconductor capacitance which depends on different operation mode.

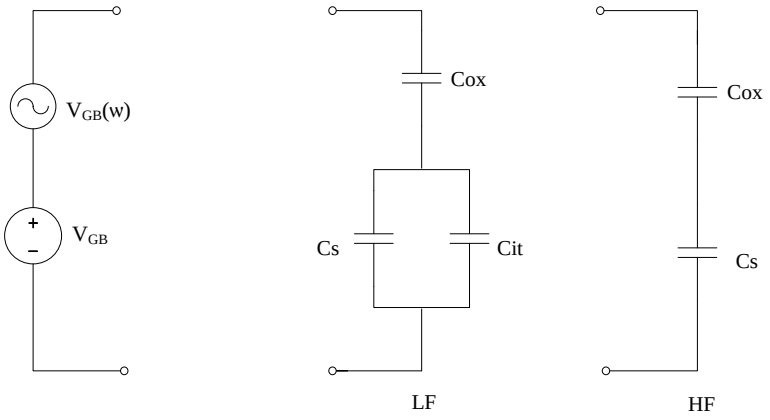


Figure 4.2 Equivalent circuit of applied gate voltage and MOS capacitor in low and high frequencies.[38]

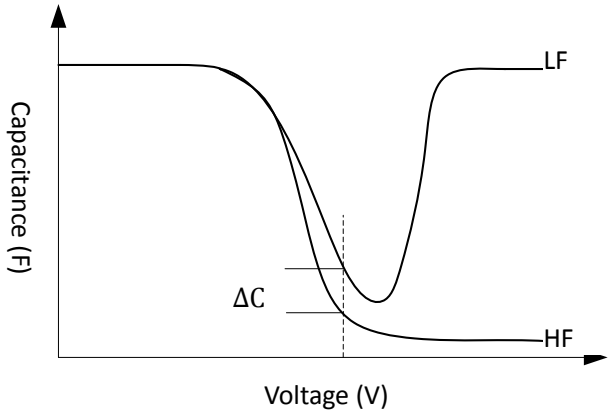


Figure 4.3 CV curve of MOS-C when considering the influence of interface states

Figure 4.3 gives the CV curves of MOS-C when considering the influence of interface states. From the different capacitance between low and high frequencies, the interface state density D_{it} can be extracted with the following calculation. As can be seen from the figure, the capacitance difference various with the gate voltage, thus the value of D_{it} is a function of the applied gate voltage. The MOS-C of low and high frequency measurement can be expressed as

$$C_{lf} = \left(\frac{1}{C_{ox}} + \frac{1}{C_s + C_{it}}\right)^{-1} \tag{4.6}$$

$$C_{hf} = \left(\frac{1}{C_{ox}} + \frac{1}{C_s}\right)^{-1} \tag{4.7}$$

With the knowledge of $D_{it}(V_{AG}) = C_{it}/(q \times A)$ where A is the area of the MOS-C plate, D_{it} can be obtained by:

$$D_{it}(V_{AG}) = \frac{C_{ox}}{q \times A}\left(\frac{C_{lf}/C_{ox}}{1 - C_{lf}/C_{ox}} - \frac{C_{hf}/C_{ox}}{1 - C_{hf}/C_{ox}}\right) \tag{4.8}$$

One should notice that the nature of Cs in the inversion region in low and high frequency measurements are not equal because the minority carrier in the substrate silicon do not response to high frequencies. Therefore Equation 4.8 is not valid in the inversion region.[38]

An alternative way to measure the interface trapped charges density is to compare the slop of HFCV to the theoretical one. Because the presence of interface states lead to a "smearing out" in the experimental curve as shown in Figure 4.4. With the knowledge of silicon dioxide thickness and dielectric constant, an ideal HFCV curve can be calculated based on the assumption that there is not any defect in the film or at the SiO_2-Si interface. The precise detail will be provided in section 4.3.

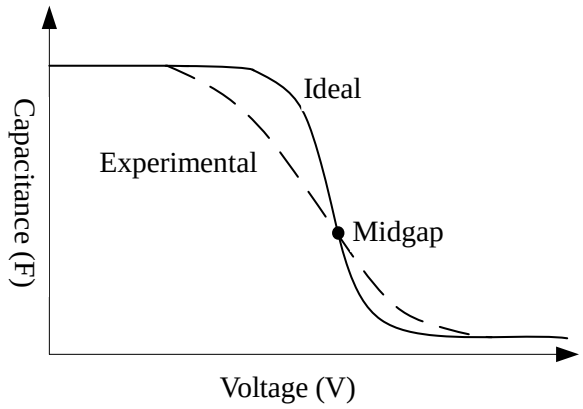


Figure 4.4 HFCV of MOS-C showing the influences of interface states

The fixed charge in the oxide Q_f, which is usually positive and located near the oxide-semiconductor interface, is determined by the conditions of SiO_2 fabrication process such as oxidation temperature and ambient. The fixed oxide charge is not influenced by the gate voltage, therefore it leads a parallel shift along the voltage axis to a negative direction in case of positive oxide charges as illustrated in Figure 4.5. The shift of flat-band voltage can be obtained using the following equation [37]

$$V_{FB} = \phi_{ms} - \frac{Q_f}{C_{ox}} \tag{4.9}$$

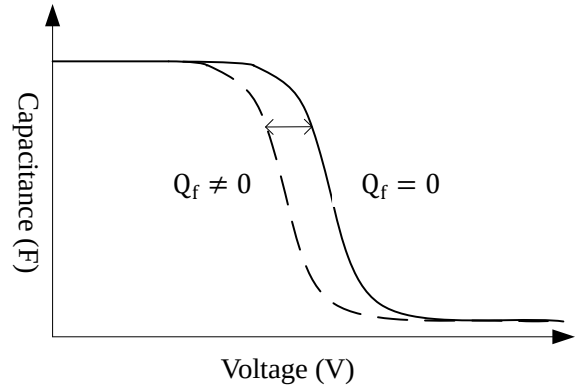


Figure 4.5 HFCV of MOS-C showing the influences of fixed oxide charges[37]

The mobile ionic charges Q_m are generally refer to positively charged alkali metal ions in the film. Among them Na^+ contamination plays the most significant role. It is not only because they can freely move in the film with their small size but also due to their wide range of sources from the fabrication surroundings including facilities used for device fabrication, organic chemical reagents and even human body.

The influence of mobile ionic charges on MOS-C characteristics is more severe in p-type-substrate device than in n-type-substrate device since the inversion layer of a p-type-substrate MOS-C is formed under a positive gate bias. When the applied voltage is positive, those positive mobile charges will be driven to the Si-SiO_2 interface and they attract negative electronics in the silicon. In this way their presence reduce the gate bias voltage required to generate the inversion region.

One way to determine the mobile ionic charge densities is the bias-temperature stress method which generally operates in the following way. First, heating the device to 150 to 250 ℃ and applying a gate bias of approximately 100V/cm for 5–10 min. During the procedure the ionic charges are driven to either the metal-oxide interface or the oxide-semiconductor interface. Then cooling down the device to ambient temperature and measuring its CV curve. After that, the operation is repeated but change the applied voltage polarity. Then the ionic charges are driven to another oxide interface and a new CV curve can be obtained. The mobile charge can be determined according to the flatband voltage difference:[39]

$$Q_m = -C_{ox}\Delta V_{FB} \tag{4.10}$$

An alternative way to detect the mobile charges is to measure the CV curves of MOS-C under the condition of different DC signal scanning direction. Although in this way the strength is not sufficient to drive all the ionic charges, it is able to give an indication of their existence.

4.1.2 Dielectric Breakdown and IV method

Breakdown of the gate oxide is the phenomenon that a low-resistance conduction path is formed in the oxide and the energy stored in the MOS capacitor previously discharged to release a large amount of energy.[40] [41] During the time the gate current Ig, known as the oxide leakage current increase dramatically and the corresponding gate voltage is regarded as the breakdown voltage Vg.

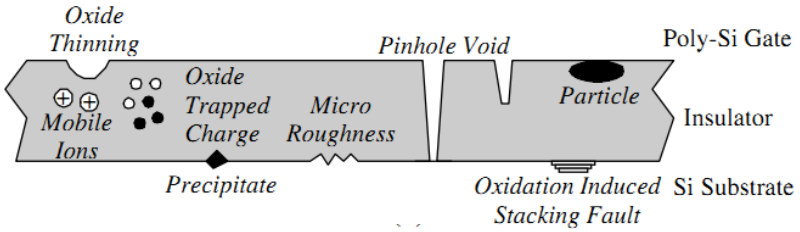


Figure 4.6 Schematic of the defects in the insulator[39]

With the knowledge of the silicon dioxide layer thickness, the breakdown electric fields can be obtained. According to the range of breakdown electric fields, breakdown mechanisms are divided into three modes A,B and C experimentally. For A mode, oxide breakdown at very low electric filed less than 2MV/cm, which is due to the existence of scratches, pinholes and other

serious defects as shown in Figure 4.6. B mode failures with breakdown electric fields range from 2-8MV/cm are commonly attributed to trapped electrons in the oxide. And C mode failures are those dielectric films breaking down at an oxide electric field higher than 9 MV/cm and the reasons for that is always the intrinsic nature of the oxide.[39]

There are many mechanisms describe the conduction process in the insulator of MOS capacitors. Each of them may be the dominate mechanism corresponds to certain insulator qualities, temperature, voltage conditions and so on. In most cases, they are not independent of each other.

In room temperature, when a breakdown voltage stays at a medium level, Frenkel-Poole mechanism can be the major conduction process which is influenced by defects and trap states in the oxide. In principle, the trapped electrons are excited when a large electric field is applied on the oxide film. The electrons gain enough energy to get into the insulator conduction band and are able to move frequently.[42]

The mathematical expression of the Frenkel-Poole current is

$$J_{FP} = A \times E \exp\left(-B + \frac{1}{kT}\sqrt{\frac{q^3 E}{\pi \varepsilon_0 \varepsilon_r}}\right) \tag{4.11}$$

Where A and B are constants related to the trap density, carrier mobility and so on in the oxide film.

The expression suggests that if Frenkel-Poole mechanism governs the leakage current, the plot of ln(J/E) versus $\sqrt{E}$ should be linear. Besides, the dielectric constant of the oxide film can be extracted from the slope of the line.[18]

The intrinsic breakdown mechanism suggests that the injection of charges including electrons and holes break bonds and create traps in the oxide. These traps form a connecting chain of defects that result in a low ohmic path and eventually destruct the oxide. There are two kinds of mathematic expressions based on two slightly different physics structures for the corresponding IV relationship. As can be seen on the band diagram of Figure 4.7, to begin with the left one, when the voltage drop across the oxide layer Vox smaller than the barrier height of electrons $q\varphi_B$, the electrons need to tunnel through the complete oxide thickness and the result current is called direct tunnel current.

The direct tunnel current obey the expression:

$$J_{dir} = \frac{AV_G}{t_{ox}^2}\frac{kT}{q} C \exp\left(-\frac{B(1-(1-qV_{ox}/\varphi_B)^{1.5})}{E_{ox}}\right) \tag{4.12}$$

Where A B and C are constants according to the effective electric mass in the oxide and the effective barrier height. And E_{ox} is the electric field of the oxide

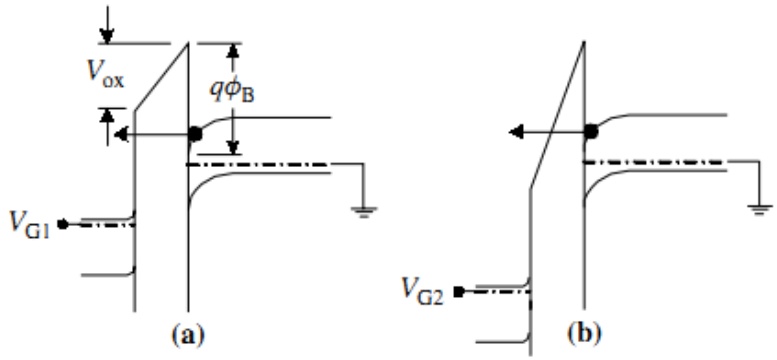


Figure 4.7 Band diagram of different tunneling mechanisms[39]

On the other hand, as shown on the right, when Vox is larger than $q\varphi_B$, the barrier for electrons is a triangle and in this case electrons only need to tunnel through part of the oxide to reach the bulk silicon, which is called Fowler-Nordheim(FN) tunneling. The IV function expressed as

$$J_{FN} = AE_{ox}^2 \exp\left(-\frac{B}{\varepsilon_{ox}}\right) \tag{4.13}$$

As we discussed above, the breakdown characteristics are detected through IV curve. A few more practical issues should be taken into consideration. Firstly, the capacitor should operate on accumulation mode because in this case charges build up near the oxide-semiconductor and metal-oxide interfaces, it will leak through the oxide when the density is too high. Secondly, The breakdown voltage is gate voltage ramp-rate dependent. This dependence is related to the damage created in the oxide during the measurement. For low ramp rates, more time is available to create damage resulting in low breakdown voltage than for higher ramp rates.[39]

4.2 Fabrication and equipment settings

4.2.1 Silicon substrate

Before we fabricate MOS capacitor using SP-SiO_2 as the oxide layer, the bulk silicon properties were adjusted in order to make a better observation.

Under the consideration that to detect a clear capacitance difference between accumulation and depletion, a wafer with low doping level or low conductivity is required to function as a semiconductor. On the other hand, since one of the diode will be placed on the back side of the wafer, a high doped wafer is preferred with the expectation to have a better contact. Hence wafers with different conductivity were tested for comparison. In this study, we fabricated MOS capacitor on p-type Born doped silicon wafers with resistivity 0.1-0.2 Ωcm and 1-5 Ωcm respectively. The SiO_2 layers were made by TEOS. As can be seen from the results, silicon substrate with resistivity 1-5Ωcm is capable of presenting reasonable CV characteristics.

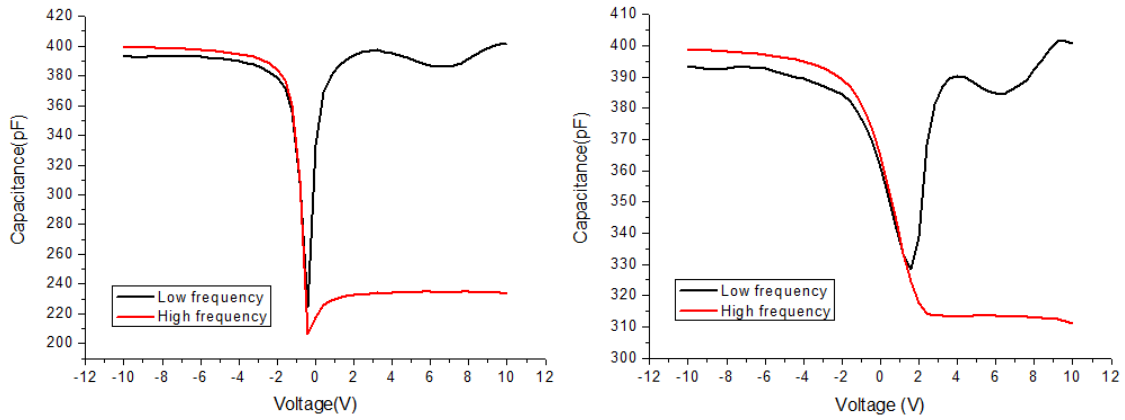


Figure 4.8 HF and LFCV of MOS-C with different substrate silicon resistivity. Left: 1-5 Ωcm, Right: 0.1-0.2Ωcm

4.2.2 MOS-C fabrication procedure

The MOS Capacitors were fabricated in the following steps:

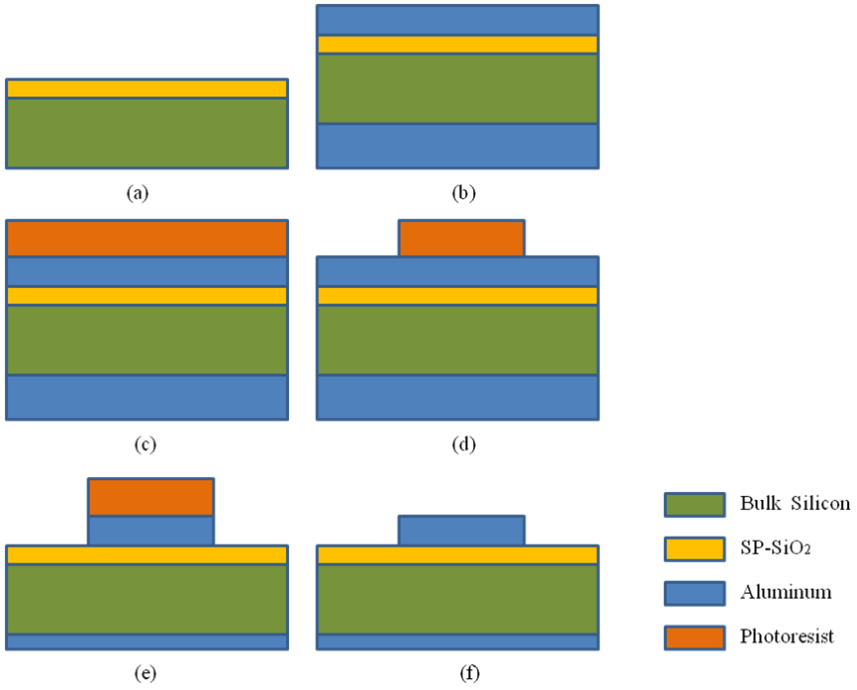


Figure 4.9 MOS-C fabrication procdures

Firstly, alignment marker was made in order to position precisely. Using the automated resist processing system to spin coating the photoresist on the wafer. This was followed by exposing the wafer with a certain pattern (mask) in an automatic wafer stepper. Numbering the wafer by hand and then developing the wafer to remove the unexpected photoresist. After inspection under microscope, the wafer was taken to a plasma etcher for dry etching. In the end, the

photoresist was stripped away by oxygen plasma and the wafer was cleaned to remove the residue resist and possible metals.

Next, the wafer was transferred to the glovebox and a silicon film made from liquid silicon was deposited on top of it. This is followed by an oxidation process to form a SiO_2 film. The detailed procedure has been provided in Chapter 3.

A series of tests such as microscope inspection and ellipsometer measurement were carried out to determine the film thickness and the elements in the film. After that, the wafer was cleaned again as shown in Figure 4.9 (a) and aluminum was deposited on both front and back side of the wafer(b). Actually it was Aluminum with 1% silicon in order to prevent silicon injection and make a better contact between the metal and the oxide. A plasma treatment on the back side was performed before aluminum deposition in order to remove the native oxide. The treatment also increase the surface roughness of the wafer and thus reduce the contact resistance between the metal and the semiconductor. The thickness of the aluminum film on the back side is larger than that of front side since the back side will not be covered in the following wet etching aluminum step. Subsequently, the wafer was spin coated with photoresist(c) and exposed under a mask with square patterns in the wafer stepper, which was followed by development and inspection of the lithography result.(d) After wet etching aluminum in PES solution(e) and cleaning up the resist in acetone(f). the wafer was finally cleaned in the 100% HNO3 solution. The last step of this fabrication process is to place the wafer in a HMDS vapor for ten minutes. In this way the water molecule residues on the wafer was removed and the electron leakage due to water existence could be prevented.

4.2.3 Measurement instruments settings

Probe station

CV measurement was carried out on a probe station in combination with an LCR meter. As can be seen from Figure 4.10, the wafer can be put on a platform and placed inside the probe box. The stage can be illuminated by a small lamp. Through the microscope, the needle-like probes can be placed on the aluminum pad of the device to connect the device to the measurement instrument such as LCR meter or semiconductor parameter analyzer.

For MOS capacitor measurements, the gate electrode is one of the terminals that connected with a probe while the backside of the wafer is regarded as another terminal that contact with the plate. to ensure a good back contact, the stage is made by gold to avoid oxide layers and vacuum can be used to hold the wafer tightly. A dry ambient is required to avoid leakage currents flowing along the oxide surface. This can be achieved by delivering a gentle stream of nitrogen gas on the wafer surface through a small pipe.[38]

Figure 4.10 Probe station

LCR meters

LCR meters can evaluate parameters of various devices accurately. It is mainly applied to measure the capacitors, inductors and so on. The principle of LCR meter is based on the measurement of impedance or admittance, which are presented in the figure 4.11.

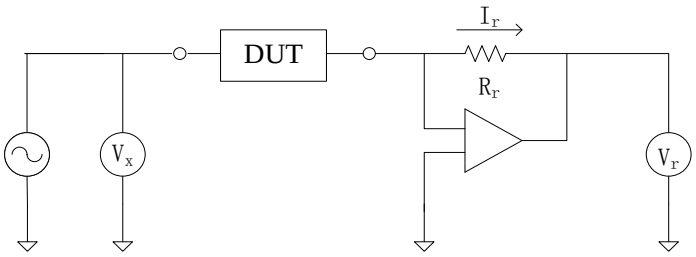


Figure 4.11 Working mechanism of LCR meter

In the figure, Vx and Vr are both vector voltmeter, Rr is an ideal resistor. When DUT (Device under test) is connected in the circuit, the negative feedback configuration of the amplifier makes its input terminal virtual ground automatically. Thus the value of Vx is the voltage across the device since the low potential of DUT is zero. The current Ix can be calculated according to Vr and Rr. Thereby Zx can be obtained.

With the knowledge of the real and the imaginary parts of the impedance, the corresponding capacitance and resistance can be extracted. A suitable profile of parameters needs to be chosen before calculation. Normally people use a two-element model based on a series or parallel circuit connection. The selected combination of parameters must coincide with the physical circuit otherwise the result will be far from the true value. For a MOS capacitor measurement, the non-ideality of the capacitor appear to be a parasitic resistance parameters. Whether it is a series model or a parallel model as shown in Figure 4.12 depends on the value of the capacitance and the real conditions.

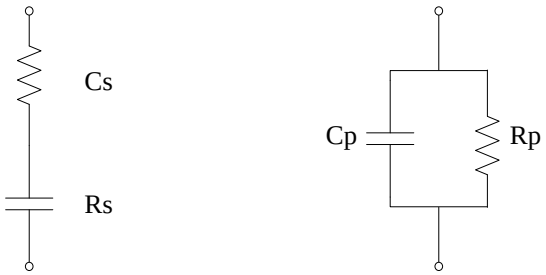


Figure 4.12 Measurement circuit mode

Normally big capacitance yields small impedance. The influence of dividing voltage by a series resistor is larger than that of dividing current by a parallel resistor. Therefore LsRs model is applied. On the contraty, LpRp model is preferred in terms of a relatively smaller capacitor. During real operation, we tested both CpRp and CsRs models. If Rp>10KΩ, we selected the parallel mode and if Rs<10 Ω, a series circuit mode should be used. In short, The LCR meter measures the impedance of the target and converted it into capacitance and resistance value through corresponding modes.[43] [44]

Semiconductor parameter analyzer

The semiconductor parameter analyzer was applied to obtain IV curves of MOS capacitors and detect their breakdown voltage. Basic functions of the semiconductor parameter analyzer is that it either measure the DC voltage across current biased devices or measure the DC current through voltage biased devices. It will display measurement results and capable to do basic calculations on a built-in CRT display. Two source and measurement units (SMU) were applied in our measurement. One of them was programmed to function as a variable DC voltage, the other one was function as a current monitor to measure the current up to 100 mA.[45]

4.3 Post annealing and measurement results

4.3.1 Postmetallization anneal and postoxidation anneal

With regard to charges in the dielectric film that seriously affected the CV performance, some methods could be carried out to reduce their influence. It should be pointed out that these charges are not present independently but have mutual interactions.

There are two annealing methods effective for reducing interface state density D_{it} after thermal oxidation, The low temperature postmetallization anneal and the high temperature postoxidation anneal. To maintain a low temperature process, the formal one is introduced in our experiment. Theoretically, postmetallization anneal method carried out as follows: after pure aluminum has been deposited on the oxide layer. The sample is heated up to 350-500℃ in a hydrogen or non-oxidizing ambient for up to 30 minutes. during the time aluminum reacts with water in the layer to generate aluminum oxide and atomic hydrogen. Then the hydrogen atoms diffuse to the Si-SiO2 interface and passive the interface traps. After that the aluminum is etched away to form gate electrodes. Alternatively, annealing can also be done after gate electrodes have been

defined.[38]

The fixed oxide charge density Q_f is determined by the oxidation environment and temperature. A higher oxidation temperature yields a lower Q_f level. However, since the process should be compatible with plastic substrate, Q_f cannot be improved by increasing baking temperature. Another possibility to reduce the fixed oxide charges is that one can anneal the wafer in a inert gas ambient after oxidation, which is what we referred as postoxidation in this study. The relationship between Q_f and oxidation and annealing temperature is summarized in the "Deal triangle" in Figure 4.13. The hypotenuse of the triangle provided the value of Q_f as a function of oxidation temperature. The vertical bars in the figure represents annealing in the inert gas environment. The behavior of cooling down the wafer in the inert gas is described by the base of the triangle.

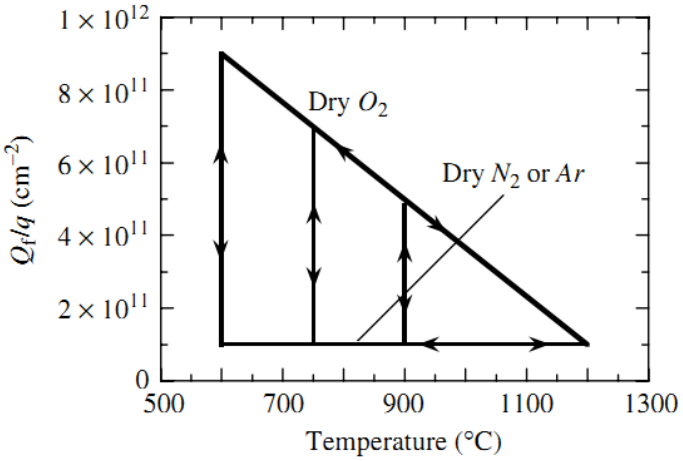


Figure 4.13 Deal triangle[39]

The figure indicated that to optimize the fixed oxide charges, the sample can be transferred to a inert gas for post annealing after oxidation. And cooling down in the same environment. In this way Q_f can be reduced to a constant level.[39]

In terms of mobile oxide charges, normally a treatment of HCl gas in the furnace before oxidation could help to reduce the amount of impurities. However in our experiment, as the oxidation take place in the open air, this step is skipped. Although care had been taken during the fabrication process because any contamination as well as the human body may introduce mobile oxide charges, there is not any specific process carried out to eliminate their effect.[38]

4.3.2 **CV measurement results and analysis**

In this section, we implement some of the methods mentioned above to reduce charge densities in the oxide and detect their performance by CV measurements.

Table 4.1 Fabrication parameters for study on charges reducing methods

	Sample K	Sample L
Resistivity	1-5 Ωcm	1-5 Ωcm
Surface treatment	0.55% HF dip	0.55% HF dip
CPS concentration	50%	50%
UV light time	30 min	30 min
Hot plate baking	1 hour at 200 ℃	1 hour at 200 ℃
Oxidation	30 min at 400 ℃	30 min at 400 ℃
Post annealing	**Place it back to glovebox and bake at 350 ℃ for 30 min after MOS-C structure has been formed**	**Place it back to glovebox and bake at 350 ℃ for 30 min after oxidation in the open air**

The silicon dioxide film fabrication processes was the same as described in chapter 3. For sample K, we applied a low temperature postmetallization anneal after forming MOS capacitors on the wafer. The sample was placed back into the inert gas environment and baked at 350 ℃ for 30 minutes. For sample L, after the film was oxidized in the furnace, it was transferred into the glovebox and baked at 350 ℃ for 30 minutes in order to optimizing the fixed oxide charge level according to "Deal triangle". The MOS-C were built with the film after that.

Sample K

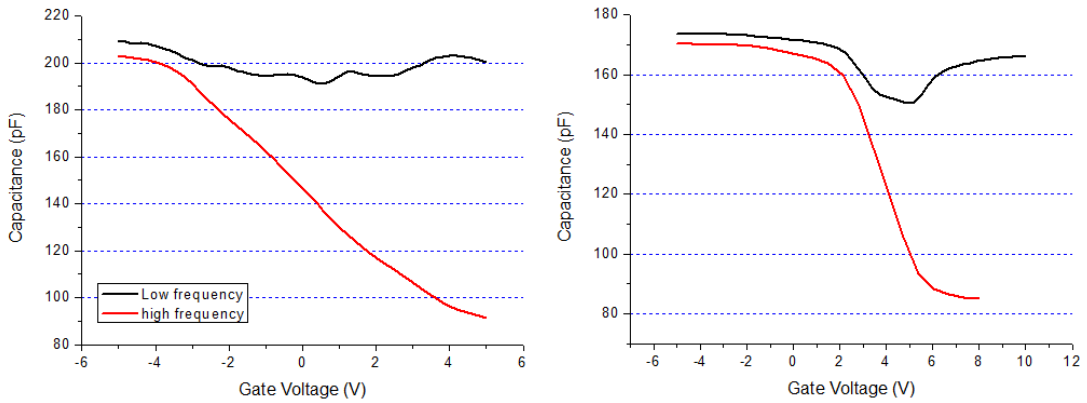


Figure 4.14 HF and LVCV of Sample K showing the improvement before (left)and after(right) postmetallization annealing

Figure 4.14 shows the CV curves of a same device before and after postmetallization anneal in the inert gas environment, which suggested an significant improvement. The red line represents HFCV and the black line is LFCV. Compared to the result on the left, the slope of HFCV on the right is deeper and the LFCV started to provide a reasonable trends. Besides, the capacitance in the accumulation region also changes which indicates a change of SiO_2 reflection index.

Sample L

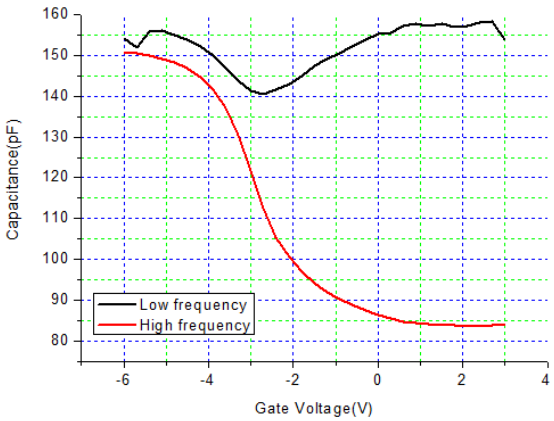


Figure 4.15 HF and LHCV of Sample L after postoxidation annealing

In the study about the influence of postoxidation anneal, we cannot compare the performance of the same device before and after post annealing. Nevertheless the result we abtained from sample K as shown in Figure 4.14 (left) could provide a reference since without the last step, sample K and L were fabricated in the way.

Compared to Figure 4.14 (left), post annealing after oxidation also improve the film quality in terms of a deeper slope and a smaller high-low frequency difference in the depletion region as shown in Figure 4.15. However when we consider about combine these two methods together, the result did not prove an improvement as expected. After MOS-C structures has been formed on sample L, it was put back into the glovebox and baked at 350℃ as postmetallization annealing. However after that the CV result of the device become much worse than before.

In terms of sample K, postmetallization anneal improved the MOS performance however this method was not applicable for sample L. One way to explain this conflict is based on the mechanism of postmetallization. In general, the postmetallization principle is the reaction of aluminum and water in the oxide film which generated hydrogen atoms and passivated the interface traps. However, SiO_2 film of sample L has been baked in the glovebox at 350℃ after oxidation, the content of water in the film thus was very low and hard to react with aluminum.

To quantify the defect density, CV curves obtained from sample L (Figure 4.15) was taken as an example for calculation.

1) Utilizing the *High-Low frequency method* to estimate the interface trap density

High-low frequency capacitance method for the interface trap density measurement was introduced in section 4.1. Basically, it extract the interface trap density by means of comparing the high and low frequency capacitance difference in the depletion region. Since the area of the capacitor is 720um by 720um, the oxide capacitance is approximately 150pF, D_{it} can be obtained according to Equation 4.8.

Table 4.2 Interface trap density result obtained from H-LF method

Vg (V)	C_{lf}(pF)	C_{hf}(pF)	D_{it} ($eV^{-1}cm^{-2}$)
-3.900	149.956	141.742	6.6320E+12
-3.600	146.913	137.167	2.7981E+12
-3.300	143.724	130.502	1.7530E+12
-3.000	141.314	121.736	1.4827E+12

The advantage of the this method is that all the data for the calculation came from experiences. Therefore complex theoretical calculation considering substrate doping profile and surface potential can be avoided. However the inaccuracy of high-low frequency method laid in the assumption that the capacitance difference is simply caused by the interface states. Since the trapped charges or mobile charges in the oxide may also perform differently between high and low frequency conditions, this assumption will bring errors to the result.

2) Utilizing the *High frequency method* to estimate the interface trap density

The high frequency method aiming to extract the interface state density based on the comparison of the theoretical HFCV and the experimental HFCV. Hence an ideal HFCV should be computed prior to the calculation.

To obtain a theoretical CV curve, a few assumptions were made in order to make the comparison more reasonable.

a. There is not any defect and unexpected charge in the silicon-dioxide film.

b. The oxide capacitance Cox is 150pF according to the capacitance measurement result of both high and low frequency conditions in the accumulation region.

c. The doping concentration of silicon substrate Na is 10^{16} cm^{-3} according to the resistivity of the wafer range from 1 to 5Ωcm, which correspond to a p-type doping concentration range from 2.68×10^{15} cm^{-3} to 1.47×10^{16} cm^{-3}.

d. The flat band voltage V_{fb} as well as the work function difference Φ_{ms} are zero since they will simply lead to a shift of the curve along the voltage axis later on.

As we know, the applied voltage Vg on the gate will bring a surface potential on the substrate ψ_s and a voltage drop across the oxide layer Vox. Besides, Vox related to the charges in the semiconductor Qs, given as

$$Vg = \psi_s + Vox = \psi_s - \frac{Qs}{Cox} \tag{4.14}$$

The total charge in the semiconductor including ionized donor and acceptor impurities, and also position-dependent densities of mobile holes and electrons. Qs can be expressed as

$$Qs = \mp\sqrt{2}\,\frac{kT}{qL_D}\varepsilon_s\left\{\left(e^{\frac{-q\psi_s}{kT}} + \frac{q\psi_s}{kT} - 1\right) + \frac{n_0}{p_0}\left(e^{\frac{q\psi_s}{kT}} - \frac{q\psi_s}{kT} - 1\right)\right\}^{1/2} \quad (4.15)$$

From Equation 4.14 and 4.15, the surface potential ψ_s can be extracted when a Vg is given. For simplicity, approximation expressions are provided under different biasing conditions.

Since $\frac{n_0}{p_0} \ll 1$, the related term is negligible.

In the accumulation mode, $\psi_s < 0$, $Qs \approx +\sqrt{2}\,\frac{kT}{qL_D}\varepsilon_s e^{\frac{-q\psi_s}{2kT}}$ (4.16)

In the depletion mode, $0 < \psi_s < 2\phi_B$, $Qs \approx -\sqrt{2}\,\frac{kT}{qL_D}\varepsilon_s\left(\frac{q\psi_s}{kT} - 1\right)^{1/2}$ (4.17)

According to Equation 4.16 and 4.17, Cs can be obtained by taking derivative of Qs with respect to ψ_s

$$Cs = \frac{d|Q_s|}{d\psi_s} \quad (4.18)$$

Finally, the total capacitance is the semiconductor capacitance and the oxide capacitance in series expressed as[38]

$$C = A \times \frac{C_{ox}C_s}{C_{ox} + C_s} \quad (4.19)$$

The work function difference Φ_{ms} between metal (Al) and semiconductor (Na=10^{16} cm^{-3}) is -0.92V. The ideal HFCV is shown in Figure 4.16 in black line whereas the red line is the measurement result.

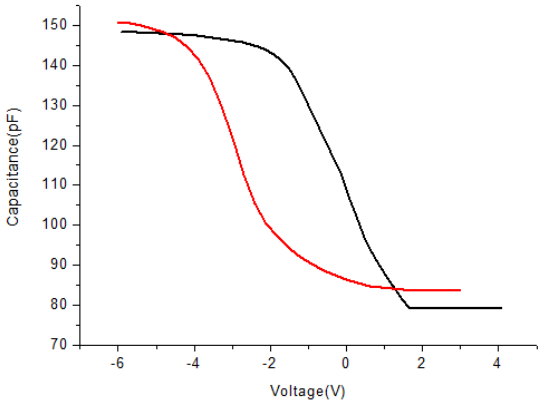


Figure 4.16 Comparison of theoretical and experimental HFCV.

As can be seen from Figure 4.16, there is an obvious shift of the experimental CV curve which indicate that there are positive fixed oxide charges presented in the film. We shifted the red line to make it cross with the black line at the midgap point corresponds to $\psi_s = \phi_B$. the expression

of midgap capacitance is given by

$$C_{Smid} \approx \frac{\varepsilon_s}{\sqrt{2}L_D} \frac{1}{\left(\frac{q\psi_s}{kT} - 1\right)^{1/2}} \tag{4.20}$$

In this experiment, Cmid is approximately 95pF so the red line shifted along the voltage axis for 2 V and came to the result shown in Figure 4.17

According to Equation 4.9, the fixed oxide charge Qs is 3.6×10^{11} $eV^{-1}cm^{-2.}$

Subsequently, the interface trap density can be obtained by comparing the difference of these two curves.

$$D_{it} = \frac{C_{ox}}{q} \frac{d\Delta V_G}{d\psi_s} \tag{4.21}$$

Where ΔV_G =Vg-Vg(ideal).[39]The calculation result is presented in Table 4.3

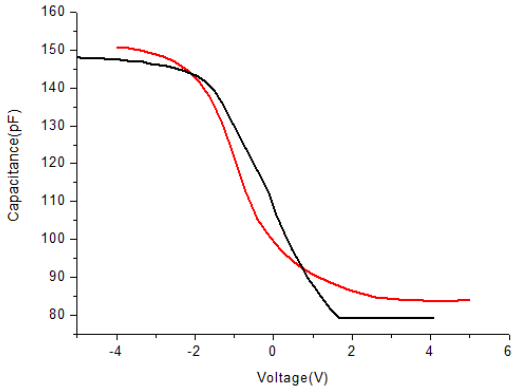


Figure 4.17 HFCV after shifting of the experimental curve

Table 4.3 Interface trap density result obtained from HF method

Vg+2V	C (pF)	ψ_s(V)	Vg(ideal)	ΔV_G(V)	Dit ($ev^{-1}cm^{-2}$)
-0.4	105.42	0.2028	0.1195	-0.51950	1.3650e+11
-0.1	100.434	0.2669	0.3235	-0.42350	2.7085e+11
0.2	96.8973	0.3230	0.4873	-0.28730	4.3905e+11
0.5	94.1984	0.3731	0.6253	-0.12530	5.8476e+11
0.8	92.0252	0.4186	0.7453	0.05470	7.1542e+11
1.1	90.2182	0.4603	0.8515	0.24850	8.4047e+11

Since the surface potential can be represented by bend banding. The band gap energy between the Fermi level E_F and the intrinsic Fermi level E_i near the semiconductor surface can be obtained from ψ_s with the knowledge that the barrier height between E_F and E_i in the bulk is -0.35eV. a plot of D_{it} as a function of band gap energy are displayed in Figure 4.18. The mid-gap is defined as the position where E_F and E_i are overlapped. In general, the interface state density at the mid-gap is approximately 5×10^{11} $eV^{-1}cm^{-2}$. It increases when E_F- E_i becomes more positive, which indicate that the interface state density is larger near the edge of the valence band.

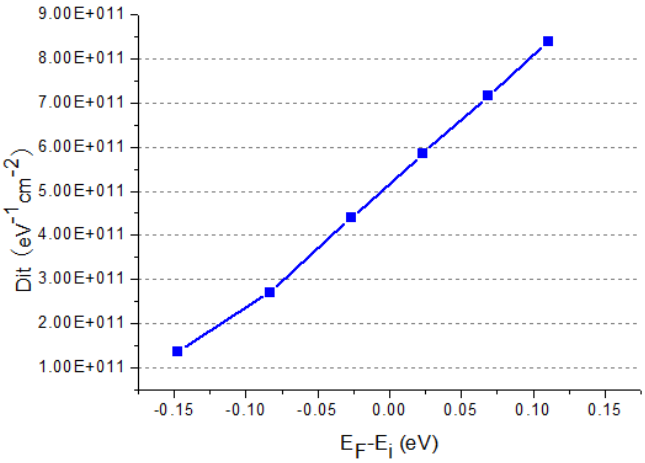


Figure 4.18 Interface state density as a function of silicon band gap energy

A typical interface states distribution throughout the bandgap is in U shape for thermal oxide, where the minimal value occurs at the mid-gap. This is because the condition required to place a interface state at the midgap is more strict than placing one at the conduction or valence band edges. Actually there are many reasons to explain the existence of the interface states. And when this reasons mix together, it is hard to make a prediction of the distribution trend.

Although we are not certain of the real cause of the interface states in this case, some related factors can be discussed. To start with, one of the serious problem in our process is the insufficient oxidation, which result in an interfacial region with a high Si/O ratio. This place is much easier to form structural defeats and the impurity charges could be accumulated in this region. Secondly, research shows that cluster of charges may also produce interface states. Since there is a relatively high concentration of fixed oxide charges in the film as calculated before, interface states may also be provided from them.[38]

Subsequently, an inspection of mobile ionic charges in this device was carried out through CV measurement.

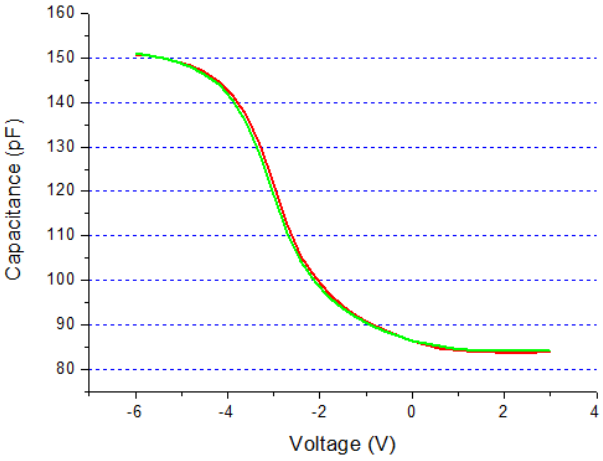


Figure 4.19 Detection of mobile charges in the oxide film

Figure 4.19 gives the HFCV of sample L, the applied DC scanning voltage of the red line was from -6V to 3V, if there are positive mobile ionic charges in the oxide film, they would first be attracted to the oxide-metal interface and do not contribute to the flatband voltage. On the contrary, the green line was obtained by scanning the gate voltage from 3V to -6V. if there exist positive mobile charges, they would first be repelled to the semiconductor-oxide interface when the gate bias is positive. As a result, a larger negative voltage would be required to convert the device in the accumulation region. Apparently, the well overlapping of this two curves suggested that the mobile ionic charge densities in the film can be ignored.

4.3.3 IV measurement results and analysis

The IV characteristic of a device fabricated in the same way as sample L is presented in Figure 4.20. Through the result, the breakdown field strength and resistivity of the film can be extracted.

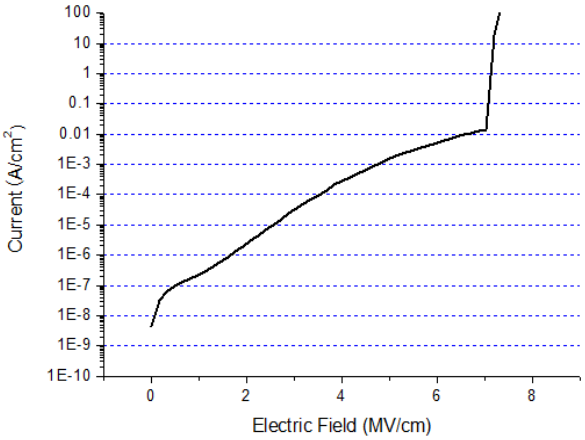


Figure 4.20 IV curve of the device fabricated in 400 ℃

Breakdown is commonly regarded to occur when the current density exceeds 1μA/cm^2. Besides, the resistivity of the film is defined at the applied electric field equal to 1MV/cm. In this way, the breakdown field strength of the device is 1.7 MV/cm. Its resistivity is 8×10^{12} Ωcm.

Compared to the thermal oxide which normally possess a breakdown field strength of over 9MV/cm corresponding to a 100 nm film and a resistivity in the order of 10^{15} Ωcm, the integrity and density of the film fabricated using liquid silicon at low temperature is not favorable. Apparently the low breakdown electric field is not due to intrinsic nature of silicon-dioxide. The dielectric constant was calculated based on Frenkel-Poole model to determine whether this breakdown mechanism fit the trap-related model or caused by other sever defects. The principle and expression of Frenkel-Poole model has been provided in section 4.1.2. in general, if the leakage current is governed by Frenkel-Poole current, the ln(J/E) versus $\sqrt{E}$ plot would be linear. Its slope is expressed as

$$S = \frac{1}{kT}\sqrt{\frac{q^3}{\pi\varepsilon_0\varepsilon_r}} \tag{4.22}$$

With the knowledge of all the contents, the dielectric constant of the film can be obtained [18].

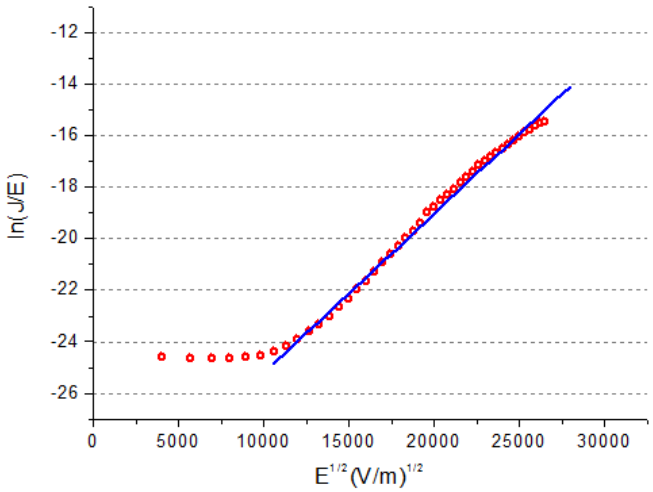


Figure 4.21 Linear fitting of IV characteristics using Frenkel-Poole model

As illustrated in Figure 4.21, a linear characteristic can be detected corresponding to the applied electric filed range from 1MV/cm to 6MV/cm. the curve in red circle is the original data and the linear fitting result is presented by the blue line. The slope of the fitting result is 6.19×10^{-4} through calculation. Hence the dielectric constant equal to 23.1 according to Equation 4.22, which is far from the physical properties of a insulator film. In summary, the Frenkel-Poole breakdown mechanism is not applicable for this film. Furthermore, in this case it is not the trapped electrons or holes in the film that dominate the leakage current.

Looking back to the results form AFM measurement provided in Section 3.2 which suggested a rough surface morphology, and also results from XPS which indicated an incomplete oxidation

of the film, it can be concluded that it is sever defects such as pinholes, oxide thinning and big particles that affected the film function and lead to a low breakdown electronic field. When a large voltage applied on the gate, these defects become the weakest point in the film and a dense conductive path is easy to form through them.

In conclusion, we provided electrical characterization of the liquid silicon processed SiO_2 films in this chapter. These films was prepared with the oxidation temperature of 400 ℃. After a introduction of theoretical background and MOS-C fabrication procedure, the interface state density was obtained by comparing theoretical and experimental HFCV curves. The result was in the order of 10^{11} $eV^{-1}cm^{-2}$ which was dozens of times higher than that of thermal oxide. A low breakdown electric filed was obtained by IV measurement which result from gross defects and a lake of oxidation of the film.

Chapter 5 Low Temperature Fabrication of SiO_2 Films

The oxidation temperature of 400 ℃ just touches the upper limit of the polyimide temperature tolerance range. In order to further reduce the process temperature, the electrical properties of SiO_2 fabricated under the oxidation condition of 350 ℃ will be reported in this chapter.

5.1 SiO_2 film processing

Although not every parameter is altered to optimize the film fabrication process when the oxidation temperature reduced to 350 ℃, the experience obtained from the 400 ℃ process in pervious chapters provide a good reference. Nevertheless, samples with pure CPS and 50vol% diluted CPS respectively were fabricated for comparison. Pure CPS is especially attractive because a diluting step can be skipped by implementing it and thus simplified the process procedure. Addition reason is that using pure CPS reduce the possibility of carbon contamination from organic solvent. Although film thickness is one of the problems, however the evaporation case is different with a lower oxidation temperature. The processing parameters of sample M and N are listed in Table 5.1, where the oxidation step is baking in the open air at 350 ℃ for one hour.

Table 5.1 Processing parameters for low temperature oxidation

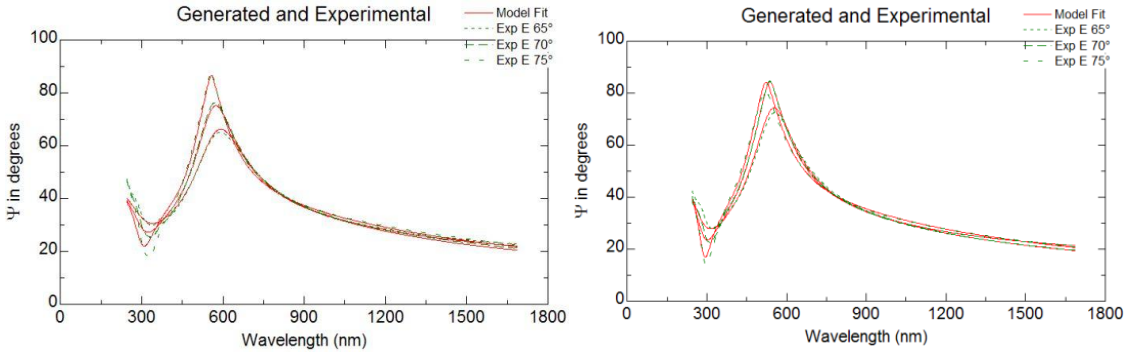
	Sample M	Sample N
Surface treatment	0.55% HF dip	0.55% HF dip
CPS concentration	100%	50%
Coating method	Blade coating	Blade coating
UV light time	30 min	30 min
Hot plate baking	1 hour at 200 ℃	1 hour at 200 ℃
Oxidation	1 hour at 350 ℃	1 hour at 350 ℃
Post metallization annealing	30 min baking at 350 ℃ in the inert gas after MOS-C structure has been formed	30 min baking at 350 ℃ in the inert gas after MOS-C structure has been formed

5.2 Component analysis

Optical instruments including Ellipsometer and X-ray photoelectron spectroscopy were implemented to measure the elemental composition of the film.

Ellipsometer results are presented in Figure 5.1. A SiO_2/Si model was implemented to estimate the film components. As we know, there might be a interfacial region near the silicon substrate due to the incomplete oxidation, which contains Si_xO while the ratio x is hard to determine. The elliposmeter thus cannot provide an accurate result by simply regarding this region as amorphous silicon. Even though, compared with the ellipsometer result given in section 3.2.5

that came from the 400 ℃ oxidation sample, there was a thicker Si film under the SiO_2 film in this case, which indicates that the polysilane or amorphous silicon in the film get less opportunity to be fully oxidized at a lower temperature.



	Sample M	Sample N
SiO_2 (Cauchy model)	137.52 nm	121.876 nm
Si	55.8 nm	49.554 nm
reflection index	1.35	1.43
MSE	61.48	42.54

Figure 5.1 Ellipsometer measurement results of sample M and sample N

XPS testing gave a more accurate result about the silicon, oxygen and carbon concentration in the film. Table 5.2 presented the surface analysis results of sample M and N. Two positions of each sample were tested namely a and b in the table. The ratio of oxygen and silicon of both samples are smaller than the theoretical value, this might because the low oxidation temperature cannot provide sufficient energy to break silicon bonds and insert oxygen atoms.

Table 5.2 Surface analysis of the atomic concentrations (at %)

position	C	O	Si	O/Si
Sample M_a	1.8	63.9	34.4	1.86
Sample M_b	1.8	63.5	34.7	1.83
Sample N_a	1.6	63.0	35.5	1.77
Sample N_b	1.9	63.1	35.0	1.81

The remarkable data is the carbon concentration in the film which is also proved by depth profile as shown in Figure 5.2. Although cyclooctane, which is an organic solvent was implemented in the process to fabricate sample N, compared to sample M which using pure CPS, there is almost no carbon impurities induced from CPS diluting. The detection limit is about 0.3% for the measurement. The results indicated that cyclooctane evaporated completely during the baking process and it is not reactive to CPS or polysilanes.

As can be seen from Figure 5.2, a broader cross between silicon-dioxide and silicon film indicated the incomplete oxidation that lead to a interfacial region with low O/Si ratio. the average O/Si ratio of sample M and N was summarized in Table 5.3. for comparison, we also listed the result of sample 1 which is prepared in the 400 ℃ oxidation condition and a reference result which obtained from thermal oxide film. It can be concluded that the films prepared using liquid silicon were in a relatively low quality since they have not been fully oxidized. Besides, the lower the temperature, the worse the oxidation level.

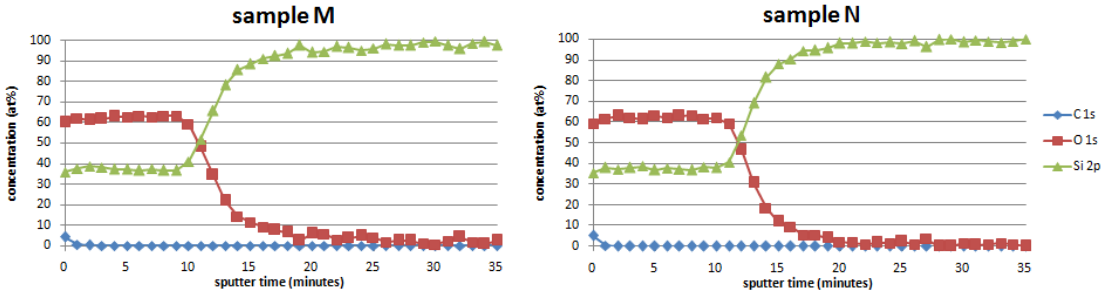


Figure 5.2 *Results of the atomic concentrations in depth profile. Left: sample M, Right: sample N*

Table 5.3 Average concentration ratio O / Si and the sputter times needed to reach the interface

	< O / Si >	$T_{interface}$ (minutes)
Sample 1 (400 ℃ oxidation)	1.79	11.7
Sample M (350 ℃ oxidation)	1.67	10.8
Sample N (350 ℃ oxidation)	1.66	11.7
Reference (thermal oxide)	1.99	15.7

Normally the film thickness can be estimated from the sputter time. In this test, the SiO_2/Si interface is defined at the position where silicon and oxygen concentrations are equal. For the reference sample of a 116 nm thermal grown oxide, it took 15.7 minutes to reach the interface by argon plasma dry etching. The etching rate was approximately 7.4 nm/min. However, although the film thickness should be over 100 nm estimated by the ellipsometer or the apparent blue color, less time is required to etch away the SiO_2 film prepared by liquid silicon.

Two reasons may be possible for explanation, one of them is because there might be silicon rich films in the interfacial place, the place where silicon and oxygen concentration are all 50% by definition may not be the real interface between the bulk silicon and the solution processed film. Another one is due to a low film density, under the same plasma etching energy, the etching rate of the solution processed samples is larger that of the thermal oxide.

5.3 Electrical Characteristics

CV curve and defect density

High frequency method as introduced in 4.3.2 was applied to extract the fixed oxide charge density and the interface state density. The red curve of Figure 5.3 provided the HFCV of a MOS capacitor whose dielectric layer was made by liquid silicon. The fabrication condition was the same as sample N. the black curve was the theoretical curve simulated using Matlab based on the assumption of no defects. Since the capacitance corresponding to the cross point is 105pF whereas the capacitance related to the mid-gap position is 95pF in theory, it indicated the presence of negative fixed oxide charges that cause the experimental curve shift to the positive direction. These charges may be the trapped electrons in the oxide. They will first compensate the influence of positive fixed oxide charges and then lead to an increase of the flatband voltage.

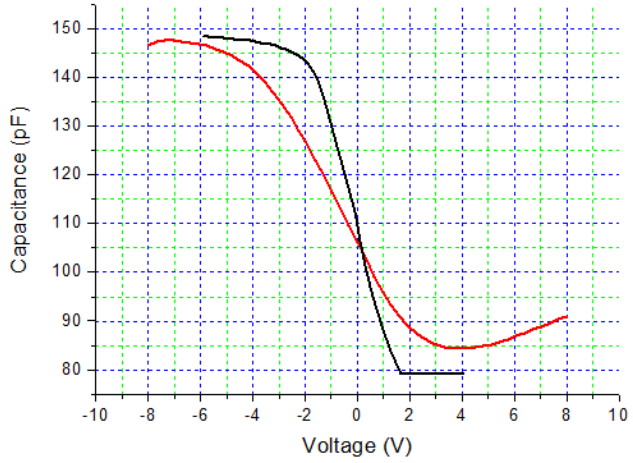


Figure 5.3 HFCV of solution processed film (red) and theoretical curve (black)

It can be obtained through calculation that the fixed oxide charges Qf is -9.1×10^{10} $eV^{-1}cm^{-2}$ in the film. The interface trap density as a function of applied gate voltage are presented in Table 5.4.The plot of D_{it} versus bend gap energy with respect to the intrinsic Fermi level near the silicon surface are given in Figure 5.4, where the interface trapped density is 2×10^{11} $eV^{-1}cm^{-2}$ near the mid-gap.

Table 5.4 Interface trap density as a function of gate voltage

Vg-0.5V	C (pF)	ψ_s	Vg(ideal)	ΔV_G	Dit/cm^{-2}
-0.82	109.703	0.1594	0.0337	-0.7863	1.33e+12
-0.5	106.145	0.1948	0.0924	-0.5924	9.86e+11
-0.18	102.627	0.2367	0.2301	-0.4101	7.83e+11
0.14	99.1817	0.2856	0.3794	-0.2394	6.28e+11
0.46	96.026	0.3385	0.5308	-0.0708	5.74e+11
0.78	93.2715	0.3919	0.6754	-0.1046	1.13E+11
1.1	90.9259	0.4435	0.8091	0.2909	1.37E+12

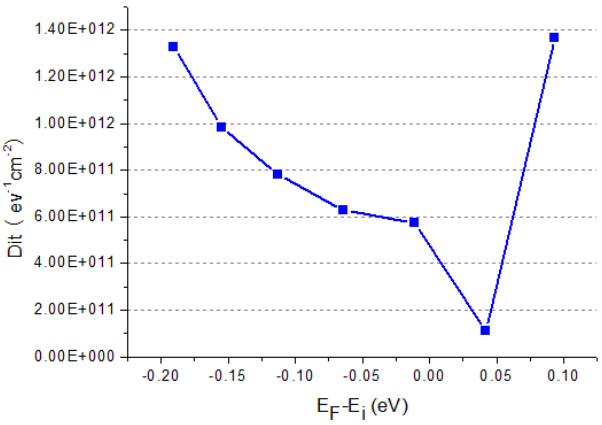


Figure 5.4 Interface trap density as a function of band gap energy

IV curve and breakdown voltage

The IV curve of the device made of low-temperature solution-processed dielectric film is given in Figure 5.5. the breakdown field strength corresponding to the electric filed when the current density exceeds 1uA/cm^2 is 1.12 MV/cm. The film resistivity at 1MV/cm of applied electric field is 1.1×10^{12} Ωcm. There is a slight reduction compared to the 400 ℃ samples.

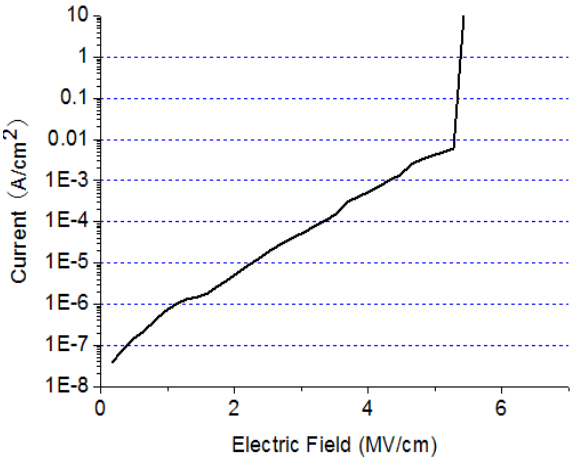


Figure 5.5 IV characteristics of liquid silicon processed film prepared at 350 ℃

So far we have presented the fabrication procedure, component analysis and electrical characterizations of the SiO_2 films prepared at an oxidation temperature of 350 ℃ in this chapter and come to the end of our study. In general, the performance of 350 ℃-oxidation samples did not show obvious differences from samples prepared at 400 ℃. Although a lower temperature lead to an insufficient oxidation, some of the defects created during the process that affected the device functions were not dominated by the oxidation temperature.

Chapter 6 Conclusions and Recommendations

6.1 Conclusions

In this project we have fabricated SiO_2 films through a non-vacuum process at low temperature using liquid silicon. The literature study was first carried out and a brief introduction of research status on low temperature solution processes were provided in Chapter 1. We introduced the properties of SiO_2 and physical chemical reactions during process in Chapter 2. After that, SiO_2 film were prepared as described in Chapter 3. A series of factors that influence the film quality were taken into consideration including surface conditions of silicon substrate, CPS concentration, blade types, heating time and temperature in the inert gas circumstance, heating time and temperature in the open air and so on. Many instruments were implemented to detect the film thickness, dielectric constant and surface morphology involving optical microscope, surface profiler, Raman microscope, ellipsometer, AFM and so on. In Chapter 4, MOS-C were made using the solution processed film as the dielectric layer. The process was carried out in the Class 100 clean room and the procedure has been given step by step in the appendices. The optimization methods such as postmetallization annealing and postoxidation annealing were then discussed. CV and IV curves of the devices were measured to calculate the defect densities and breakdown electric field. The result showed that with the oxidation temperature of 400℃, both oxide fixed charge density and interface trapped density of the film were in the order of 10^{11} $ev^{-1}cm^{-2}$. The breakdown film strength was 1.7MV/cm. With all these experience we obtained above, we further decrease the oxidation temperature to 350℃. A complete fabrication process and results was presented in Chapter 5. The fixed charge density and midgap interface trapped density in this case were -9.1×10^{10} $eV^{-1}cm^{-2}$ and 2×10^{11} $eV^{-1}cm^{-2}$, respectively.

6.2 Recommendations for future work

Liquid silicon is a promising material for a non-vacuum and solution based process however the resultant device quality should be further improved.

1.During the research, form the film by hand blading was one of the severe reason that lead to the non-uniformity and low reproducibility of the result. Therefore a better spreading methods should be investigated in order to not only replace a vacuum process but also maintain the film uniformity.

2.Although we aim to apply the film on a plastic substrate, this research was carried out on the silicon wafer. It limited the implementation of Excimer laser post annealing since the energy will leak away through the silicon substrate. The film quality might be improved by the laser when TFTs are applied on the glass or plastic substrate in the future.

3. A lack of oxidation lead to the oxygen and silicon ratio in the film less than two. This is mainly because that a low oxidation temperature cannot provide sufficient energy to break Si-Si bonds and insert oxygen atoms in between. New oxidation strategies may be applied to solve

the problem. One way is that inducing UV irradiation on the wafer surface during baking the wafer in the open air because oxygen can be converted to ozone by UV light whose chemical properties are more active. The other way that worth to study is the wet oxidation that implement water vapor as the oxidant.

Appendices

Flowchart

MOS Capacitor by Using Liquid silicon processed SiO_2

1. Coating - SPR3012 - zero layer Location: Class 100 clean room

Use the EVG120 system to coat the wafers with photoresist, and follow the instructions specified for this equipment.

The process consists of a treatment with HMDS (hexamethyldisilazane) vapor with nitrogen as a carrier gas, spin coating with SPR3012 positive resist, and a soft bake at 95 ℃ for 90 seconds. The resist will be dispensed with a pump. Always check the relative humidity (48 ± 2 %) in the room before coating.

Use the program "Co – SPR3012 – zero layer" on the coating station

2. Expose - ASM PAS 5500 - Mask COMURK Location: Class 100 clean room

Processing will be performed on the ASM PAS 5500/80 automatic wafer stepper.

Follow the operating instructions from the manual when using this machine.

Expose mask : COMURK, litho job: comurk0.0, layer ID: 1.

Exposure energy: 120, Focus: 0.

3. Numbering the wafers Location: Class 100 clean room

Use the glass pen in the lithography room to supply the wafer with the BATCH and WAFER number. Write the numbers in the resist after development. Do not use a scriber (pen with a diamond tip).

4. Developing - Dev - Single puddle Location: Class 100 clean room

Use the EVG120 system to develop the wafers, and follow the instructions specified for this equipment.

The process consists of a post-exposure bake at 115 ℃ for 90 seconds, developing with Shipley MF322 with a single puddle process, and a hard bake at 100 ℃ for 90 seconds.

Use program "Single puddle" on the developer station.

5. Inspection- Line width and overlay Location: Class 100 clean room

Visually inspect the wafers through a microscope, and check line width and overlay. No resist residues are allowed.

6. Dry Etching - URK_NPD Location: Class 100 clean room

Use the Trikon's Omega 201 plasma etcher.

Follow the operating instructions from the manual when using this machine.

Use sequence URK_NPD(with a platen temperature of 20℃) to etch 120 nm deep structures into the Silicon wafer.

Process conditions of the chamber: recipe URK_NPD

7. Plasma strip - TEPLA - Program 1 Location: Class 100 clean room

Use the Tepla plasma system to remove the photoresist by oxygen plasma.

Follow the instructions specified for the Tepla stripper, and use the quartz carrier.

Recipe: program 1

8. Cleaning procedure - HNO_3 100% and 65% (Si) Location: Class 100 clean room

Cleaning 10 minutes in fuming Nitric acid (Merck: HNO_3 100%) at ambient temperature.

Use wet bench "HNO_3 (100%)" and the carrier with the red dot.

QDR Rinse the wafers in the Quick Dump Rinser with the standard program until the resistivity is 5 MΩ.

Cleaning 10 minutes in concentrated Nitric acid (Merck: HNO_3 65%) at 110 ℃.

Use wet bench "HNO_3 (65%)" and the carrier with the red dot.

QDR Rinse the wafers in the Quick Dump Rinser with the standard program until the resistivity is 5 MΩ.

Drying Use the Semi tool "rinser/dryer" with the standard program, and the white carrier with a red dot.

9. Transport- Change to white box Location: Class 100 clean room

Transfer the wafers from the black box into a white box.

Put the white box into a plastic bag and seal the bag

For use in the glovebox

10. Transport in glovebox Location: MEMSLAB

Use a small wafer carrier to transport your wafer

Check if the antechamber (the transport chamber of the glove box which can be vacuum down) is closed inside of the glovebox

Put the wafers in the antechamber and close the antechamber lid

Vacuum down the antechamber for at least 3 times

Open the lid on the inside of the antechamber, take out the wafers and close the lid

11. Mixing liquid silicon - 50% volume percentage Location: MEMSLAB

For mixing CPS you need fresh CPS in a brown bottle and cyclooctane in a brown bottle

Put 20ul CPS and 20ul Cyclooctane into the glass beaker, volume percentage:50%

Mix the solution with the Teflon stirrer

12. Blade coating - in glovebox Location: MEMSLAB

Apply the solution on the wafer

Spread the solution using a Silicon nitride blade

13. UV light Exposure - in glovebox Location: MEMSLAB

Put the wafer on the platform under the UV light

Turn on the UV Light through the glovebox control panel

UV light exposure time: 30 minutes

14. Baking on hotplate - in glovebox Location: MEMSLAB

Make sure the purge in the glovebox is on

Set the the hotplate to 200 ℃

Baking time: 1 hour

Set the hotplate to room temperature

15. Transport out glovebox Location: MEMSLAB

Check if the antechamber (the transport chamber of the glovebox which can be vacuum down) is closed on the outside of the glovebox

Open the antechamber from inside and transport the wafers out

Check if the lid on the inside is closed

Vacuum down the antechamber for at least 3 times

16. Baking in the furnace – Carbolite Furnace - 400 ℃ Location: MEMSLAB

Clean the furnace with water and IPA

Use a clean test wafer under your process wafer to avoid contamination

Set the set point to T = 400 ℃

Baking time: 30 minutes

Set the temperature back to 300 C

17. Cleaning procedure - HNO_3 100% (Si) Location: MEMSLAB

Cleaning 10 minutes in fuming nitric acid (Merck: HNO3 100%) at ambient temperature.

Use wet bench "HNO3 (100%)" and the carrier with the red dot.

QDR Rinse the wafers until the resistivity is 5 MΩ.

Drying Use the manual dryer

cleaning in MEMS LAB

18. Cleaning procedure - HNO_3 100% and 65% (Si) Location: Class 100 clean room

Cleaning 10 minutes in fuming Nitric acid (Merck: HNO_3 100%) at ambient temperature.

Use wet bench "HNO_3 (100%)" and the carrier with the red dot.

QDR Rinse the wafers in the Quick Dump Rinser with the standard program until the resistivity is 5 MΩ.

Cleaning 10 minutes in concentrated Nitric acid (Merck: HNO_3 65%) at 110 ℃.

Use wet bench "HNO_3 (65%)" and the carrier with the red dot.

QDR Rinse the wafers in the Quick Dump Rinser with the standard program until the resistivity is 5 MΩ.

Drying Use the Semi tool "rinser/dryer" with the standard program, and the white carrier with a red dot.

19. Metallization - 1400 nm Al/Si Location: Class 100 clean room

Use a clean transport wafer under your process wafer to avoid contamination

Use the TRIKON SIGMA sputter coater for the deposition of an Al/Si layer on the wafers.

The target must exist of Al/Si and deposition must be done at 50 ℃ and with an Ar flow of 100 sccm. Follow the operating instructions from the manual when using this machine.

Recipe Al/Si 1400nm @50 No RF

Visual inspection: the metal layer must look shiny.

20. Metallization - 3000 nm Al/Si on backside Location: Class 100 clean room

Use the TRIKON SIGMA sputter coater for the deposition of an Al/Si layer on the wafers.

The target must exist of Al/Si and deposition must be done at 50 ℃ and with an Ar flow of 100 sccm. Follow the operating instructions from the manual when using this machine.

Recipe: Al/Si 3000nm @50 RF

Visual inspection: the metal layer must look shiny.

21. Co - SPR 3017 - 2000 nm Location: Class 100 clean room

Use the EVG120 system to coat the wafers with photoresist, and follow the instructions specified for this equipment.

The process consists of a treatment with HMDS (hexamethyldisilazane)vapor with nitrogen as a carrier gas, spin coating with SPR 3017positive resist, and a soft bake at 95 ℃ for 90 seconds. The resist will be dispensed with a pump. Always check the relative humidity (48 ±2 %) in the room before coating.

Use program "SPR 3017 - 2000 nm"" on the coating station

22. Expose - ASM PAS 5500 - Mask P2688 MINOX Location: Class 100 clean room

Processing will be performed on the ASM PAS 5500/80automatic wafer stepper.

Follow the operating instructions from the manual when using this machine.

Expose mask: P2688 MINOX (box364), litho job: g10a-1, layer ID: 1.

Exposure energy:150, Focus: 0.

23. Developing - Dev - Single puddle Location: Class 100 clean room

Use the EVG120 system to develop the wafers, and follow the instructions specified for this equipment.

The process consists of a post-exposure bake at 115 ℃ for 90 seconds, developing with Shipley MF322 with a single puddle process, and a hard bake at 100 ℃ for 90 seconds.

Use program "Single puddle" on the developer station.

24. Inspection – Line width and overlay Location: Class 100 clean room

Visually inspect the wafers through a microscope, and check line width and overlay. No resist residues are allowed.

25. Wet etching Aluminum - 1400 nm Al Location: Class 100 clean room

Moisten Rinse for 1 minute in the container filled with demi-water containing Triton X-100.

Use the carrier with the yellow dot.

Use wet bench "Aluminum-ets" at 35 ±1 ℃, and the carrier with the yellow dot.

1liter buffered etch fluid contains:

770ml concentrated phosphorus acid (H_3PO_4 85%), 14 ml concentrated nitric acid(HNO_3 65%), 140ml concentrated acetic acid (CH_3COOH 100%) and 76 ml deionized water

Etch time: 20 min

QDR Rinse in the Quick Dump Rinser with the standard program until the resistivity is 5 MΩ.

Drying Use the Semi tool "rinser/dryer" with the standard program, and the orange carrier with a black dot.

26. Cleaning procedure - Acetone Location: Class 100 clean room

Dissolve the photoresist in acetone at 40 ℃. Time: 1 min

Use wet bench "Aceton40C" and the carrier with the two red dots.

27. Cleaning procedure - HNO_3 100% (metal) Location: Class 100 clean room

Cleaning 10 minutes in fuming nitric acid(Merck: $HNO_3$100%) at ambient temperature.

Use wet bench "HNO_3 100% metal" and the carrier with yellow and red dots.

QDR Rinse in the Quick Dump Rinser with the standard program until the resistivity is 5 MΩ.

Drying Use the Semi tool "rinser/dryer" with the standard program, and the white carrier with a black dot.

28. HMDS Location: Class 100 clean room

Use the EVG120 system put a thin layer of HDMS on the wafers, and follow the instructions specified for this equipment.

The process consists of a treatment with HMDS (hexamethyldisilazane)vapor with nitrogen as a carrier gas.

Always check the relative humidity (48 ±2 %) in the room before.

Use program "HMDS only"" on the coating station

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