An Energy-Recycling Inductive Power Converter for Battery-Powered CMUT-Based Ultrasound Wearables

Innovative, Unique and On Point

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TU Delft

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by

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Abstract

Wearable ultrasound systems hold significant potential for continuous health monitoring but face challenges in minimizing energy consumption and device size. This research investigates the design and simulation of an energy-recycling inductive power converter for CMUT-based wearable ultrasound applications. A comparison between conventional class-D and resonant pulsers highlights the trade-off between operational flexibility and energy efficiency, emphasizing the critical impact of high-voltage bias generation, which can consume hundreds of times more energy than a single transmit pulse.

A novel four-switch converter topology is proposed, enabling both high-voltage biasing and pulsing with energy recycling. Unlike traditional buck–boost converters, the proposed converter operates in a unique regime: it only functions during the initial charging of capacitive loads, after which the output can be fully decoupled, allowing the inductor to perform other tasks. This places the design in a fundamentally different and largely unexplored operating point within power-converter research. It also facilitates energy recycling, allowing the recovered energy to be reused after pulse-acquisitions in other systems where power is required.

System-level simulations explore the influence of inductor sizing, switch dimensioning, and current optimization on efficiency, while break-even analysis indicates that conventional pulsers may remain more practical for typical pulse counts due to lower complexity. Circuit-level implementation in Cadence confirms functional operation, high-voltage generation, pulsing and energy recycling.

This work identifies the primary sources of energy inefficiency and proposes control strategies, including optimized switch timing and parasitic energy recovery, to enhance performance. The study provides a validated foundation for future experimental research and practical implementation, demonstrating the feasibility of energy-efficient wearable ultrasound systems using 180nm technology.

Acknowledgements

This project has meant more to me than just obtaining my degree. After a period of hard and challenging moments, I can finally transition from being a student to embracing a new phase: citizenship. Believe it or not, I am looking forward to it. Although my ambitions sometimes went further than what was realistic, such as the idea of achieving a tape-out, I now look back with pride at what has been accomplished and how the project was set up.

First of all, I would like to sincerely thank my supervisors, Michiel Pertijs and Imad Bellouki. Michiel, thank you for your sharp questions, creative solutions, and the way you truly involve students in the department. You always managed to provide direction and gave us a real sense of belonging. Imad, your daily guidance, enthusiasm, and genuine interest made working on this project not only very instructive but also truly enjoyable. I will not easily forget our weekly meetings with the three of us: your energy, problem-solving skills, and curiosity were a constant source of inspiration. Thanks to both of you, my learning curve this year has been remarkable, and for that I am deeply grateful.

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Furthermore, I am thankful to my friends and family for their support during this year. Without the nice lunches, the workouts, the evening distractions, including 'Pieletjes gooien' (throwing darts) at Café Bergpolder, and all the fun activities in between, I would not have made it through this project. In particular, I want to thank my parents, who have always supported me through everything; I sincerely hope they can soon enjoy a well-deserved retirement. And finally, to my dear girlfriend Kyra: thank you for your unconditional support, day in and day out. I could not have done this without you.

Martin Geertjes
Delft, September 2025

Contents

Acronyms

- BB – Back-to-Back (switch configuration)
- BCD – Bipolar-CMOS-DMOS (in TSMC 180nm BCD Gen2 technology)
- BVD – Butterworth-van Dyke Model (CMUT Model)
- Cadence – EDA software
- CMUT – Capacitive Micromachined Ultrasound Transducer
- CP – Conventional Pulser / Class-D Pulser
- DAC – Digital-to-Analog Converter
- DC – Direct Current
- ESD – Electrostatic Discharge
- FEM – Finite Element Modeling
- FSM – Finite State Machine
- HV – High Voltage
- LNA – Low-Noise Amplifier
- LV – Low Voltage
- MATLAB – MathWorks software
- MOSFET – Metal-Oxide-Semiconductor Field-Effect Transistor
- NMOS – N-channel Metal-Oxide-Semiconductor
- PDK – Process Design Kit (in context of TSMC 180nm BCD-Gen2 PDK)
- PMOS – P-channel Metal-Oxide-Semiconductor
- Q-factor – Quality Factor
- RP – Resonant Pulser / Resonant Pulsing
- RxTx – Receive/Transmit
- SNR – Signal-to-Noise Ratio
- SR-latch – Set-Reset Latch
- T/R – Transmit/Receive
- TSMC – Taiwan Semiconductor Manufacturing Company
- TX – Transmit
- US – Ultrasound

1 Introduction

1.1. Motivation

Ultrasound (US) imaging is a widely used technique in both medical diagnostics and industrial applications. By transmitting short acoustic pulses and analyzing their echoes, ultrasound systems can generate real-time images of internal structures, quantify volumes, or track motion using Doppler-based methods. Despite these advantages, conventional ultrasound devices are still bulky, multifunctional, and require trained professionals for operation. [1] [2]

Imagine this technique tool while focussing on just one single application, to fit the device in a wearable patch that can continuously monitor your heart or which is able to detect early signs of specific diseases. This all while running on a single battery charge for weeks. This provides 24/7 health insights and enables remote patient monitoring, reducing the need for frequent hospital visits and potentially lowering healthcare costs. Moreover, the pressure on the healthcare system can be reduced.

There is a growing interest in developing compact, portable ultrasound systems for point-of-care diagnostics and wearable health monitoring. [2] [3] This thesis focuses on enabling ultrasound for wearable applications in an energy-efficient manner.

1.2. Background and Prior Art

An Ultrasound Imaging System generates sound waves and listens for reflections from within a medium, such as the human body. By analyzing these reflections, it can construct data of internal structures and moving liquids or material. To illustrate the operation of such a system, a simplified overview of the system is shown in Figure 1.1. It can be divided in five sub-systems: first, an energy source is applied to supply to the entire system, typically a low-voltage battery in wearable applications. Power converters ensure that all subsystems operate under the correct electrical conditions. The core subsystems include the pulser system, receiver, ultrasound transducer (CMUT), and a logic unit that controls the system and optionally processes the received data.

Recent work has shown a new technique for half-sine energy-efficient pulsing of capacitive micro-machined ultrasound transducers (CMUT) called Resonant Pulsing (RP) [4]. This technique enables pulsing with energy recycling from the paracitic transducer capacitance during ultrasound pulsing using a single external inductor, potentially leading to significant pulse energy savings up to 76.8%. However, the RP architecture is still in its infancy and lacks many features compared to conventional pulsers. Consecutive work has demonstrated continuous-wave beamforming [5] and explored methods for generating pulse-trains [6], both of which are important for wearable applications: beamforming allows the ultrasound energy to be focused on a specific region of interest [1], while pulse-trains improve acoustic pressure and enable coded excitation techniques that can enhance the signal-to-noise ratio (SNR) up to 24.8dB [1, 7, 8]. Such performance gains cannot be achieved to the same extent on the receiving side, or would otherwise entail a significant energy cost, making them particularly attractive for wearable devices. Improvements in SNR are especially important since recent work in ultrasound

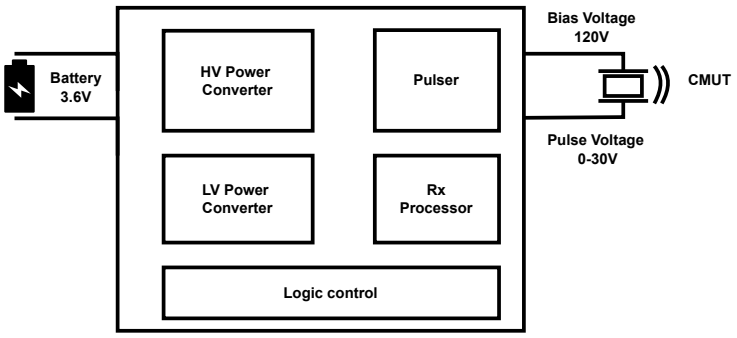


Figure 1.1: Simplified US Transceiver System

systems has shown that the low-noise amplifier (LNA) at the receiver front-end dominates the overall system power consumption, typically operating in the milliWatt range [9, 10]. Nonetheless, studies on resonant pulsers show that the technique requires complex trimming and calibration to function reliably, and its functionality remains restricted by the reliance on a single inductor—although minimizing external components is an advantage for wearables in terms of cost and area efficiency. Moreover, CMUT devices require high-voltage biasing, which incurs additional energy losses and is not addressed in these studies.

1.3. CMUT-Transducer

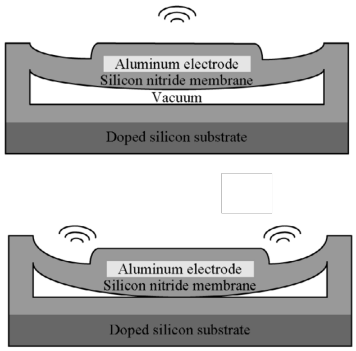


Figure 1.2: CMUT Device Illustration [11]

Figure 1.2 illustrates a CMUT device. CMUTs consist of a membrane suspended over a cavity, forming a capacitor. By applying a high-voltage bias, the CMUT can be set in collapse mode, which enhances its sensitivity and bandwidth, and also results in a higher acoustic output [11, 12]. These are important advantages for achieving higher signal-to-noise ratios and improving energy efficiency in wearables. However, generating this high DC-bias voltage in a low-voltage environment remains both challenging and energy expensive. When combined with the limitations of resonant pulsing, this raises the question of whether the resonant pulser technique is currently the right path forward for ultrasound wearable devices.

Figure 1.3 shows the Butterworth-van Dyke (BVD) model for the CMUT. This model consists of four elements arranged in two parallel branches and describes both the mechanical and electrical dynamics of the transducer [13]. Here, R_m captures the mechanical dissipation and is directly linked to the energy transfered into the ultrasound pressure waves. The static capacitance C_e accounts for the parasitic electrical capacitance of the CMUT electrodes. The static capacitance C_e accounts for the electrical parasitic capacitance of the CMUT device. This branch dominates the capacitive CV^2 losses, and is therefore often used to characterize the electrical energy losses in the device.

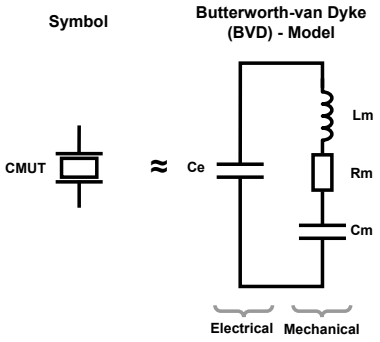


Figure 1.3: CMUT Symbol and equivalent BVD Model

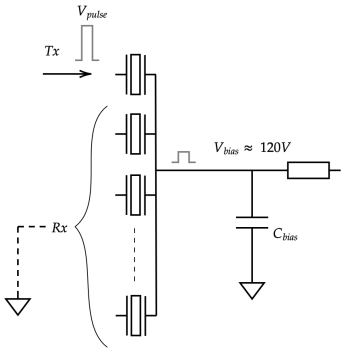


Figure 1.4: CMUT element Coupling

In Figure 1.4 a CMUT device is illustrated existing of an array of CMUT elements. Each element can be pulsed independently, but they all share a common biasing node connected to a single biasing capacitor C_{bias}. When considering the size of the biasing capacitor, it is important to note if all elements of the array are connected on the same biasing node as illustrated.

Depending on the ratio between the biasing capacitance and the transducer capacitance, multiple elements may be charged together.

As an example, consider an array with 64 elements. If one element is excited, the remaining 63 elements are still connected to the common bias node through their transducer capacitances. In this case, the bias capacitor C_{bias} is effectively in parallel with the sum of the other 63 transducer capacitances.

The electrical pulse amplitude that appears across the idle elements is determined by the capacitive divider ratio as given in equation 1.1:

$$V_{\text{pulse-coupling}} = V_{\text{tx}} \cdot \frac{C_{\text{tx}}}{C_{\text{bias}} + (N-1)C_{\text{tx}}} \text{ [V]} \tag{1.1}$$

where V_{tx} is the applied transmit pulse on the active element, C_{tx} is the capacitance of a single transducer cell, C_{bias} is the bias capacitor, and N is the total number of elements (e.g., $N = 64$).

Figure 1.5 illustrates the power dissipated in the transducer elements due to this coupling effect. It shows unwanted transmission by the other elements which causes an extra parasitic plane wave during the pulse acquisition. This effect can lead to reduced signal integrity.

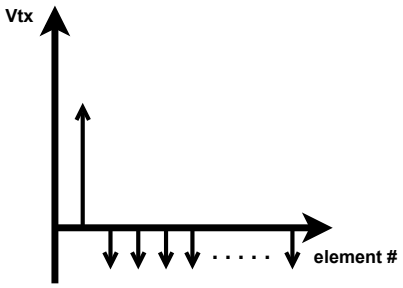


Figure 1.5: CMUT Coupling between elements

1.4. Power Converter

Given that we still aim to use a single inductor, it becomes relevant to investigate whether it is better to continue with the resonant pulser architecture, where the inductor is fixed by the resonance frequency, or to switch to a conventional class-D pulser combined with a buck-boost converter and an optimized inductor. Both architectures consist of a 4-switch topology as shown in Figure 1.6, which are comparable topologies used in buck-boost converters.

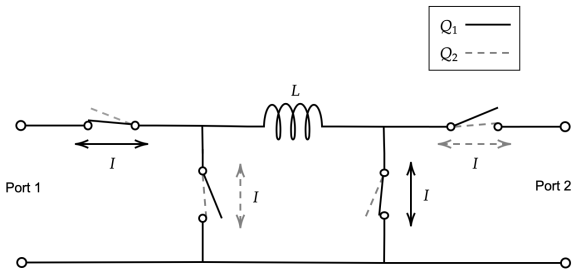


Figure 1.6: 4-Switch Topology

As illustrated with two operating modes, the topology enables power conversion between two ports charging and discharging the inductors magnetic field while redirecting the inductor current to either the input or output port. From this perspective, the resonant pulser can be seen as a special case of the 4-switch topology, where the switches are controlled to create a specific resonance frequency. Combining these two functions in a single topology is an interesting approach to explore, since it could potentially lead to energy recycling from capacitive output loads while also enabling the generation of a high-voltage bias. It is conceivable that this could be an opportunity for wearable applications, given the expectation that for specific applications the intensity of measurements will be lower, while the daily frequency will be higher. Otherwise, the energy required to build up the bias voltage would be lost multiple times a day, which would reduce the system's efficiency.

However, when comparing the operation of a conventional buck–boost converter, an important distinction becomes apparent. In theory, a buck–boost converter operates into a resistive load and continuously delivers an average power to maintain the output voltage. To reduce ripple, an output capacitor is typically added, as illustrated in converter start-up waveforms where the output capacitor is charged and the output voltage is regulated. This concept is illustrated in Figure 1.7.

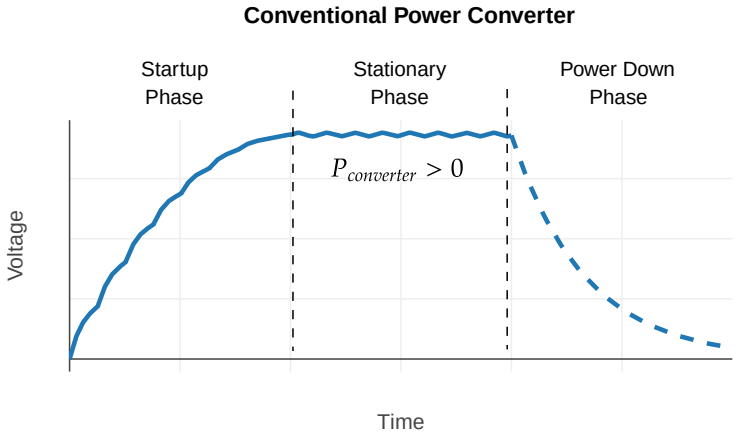


Figure 1.7: Operational illustration of a conventional buck-boost converter.

In contrast, as illustrated in Figure 1.8, the US power converter is only required for charging the capacitive loads. While charging this load, the converter only operates during the 'start-up phase' of the

conventional buck-boost converter. After charging, the output can be fully decoupled and the inductor can be used for other tasks, such as pulsing or charging other capacitors. Decoupling the output has the added benefit of preventing the output from system noise or other disturbances induced by the converter. Afterwards, even full discharge of the bias capacitor back through the converter would be possible, enabling energy recycling.

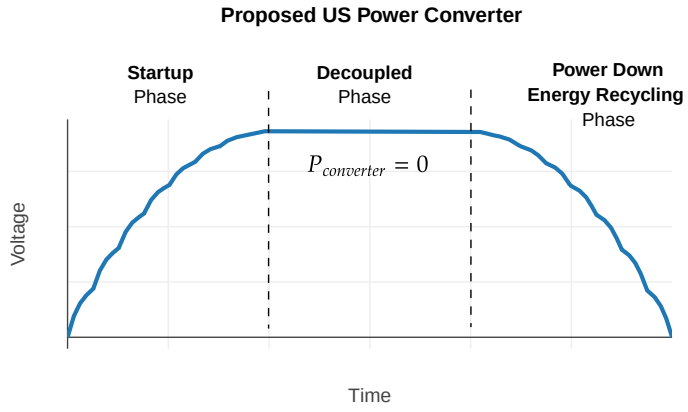


Figure 1.8: Operational illustration of the proposed converter.

Comparing the operating phases, the proposed converter would never operate in an equivalent steady-state regime whereon buck-boost converters are optimized. This makes this ultrasound power-converter system unique in its operation and places it in an unexplored area of power-converter research. Unlike a buck–boost converter, its objective and operating point are fundamentally different. To summarize, the difference between a conventional buck-boost converter and the proposed converter is shown in figures 1.9 and 1.10. The arrows indicate the energy flow during operation.

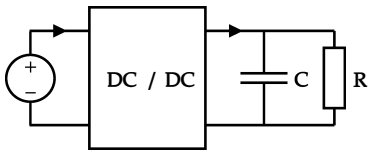


Figure 1.9: Conventional buck-boost converter: simplified diagram.

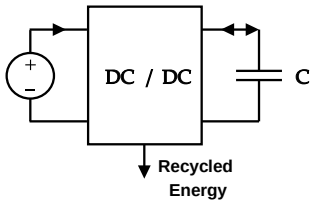


Figure 1.10: Proposed converter: simplified diagram.

The proposed converter is able, when using multiple output switches, to charge multiple capacitive loads. This could be used to charge the bias capacitor and to pulse the transducer. When considering the energy efficiency of the proposed converter, it is important to note that the energy required to charge the bias capacitor is significantly higher than that needed for a single pulse on the transducer. Assuming that the biasing capacitor (C_{bias}) is 50 times larger than the transducer capacitance (C_{tx}), we can compare the required energy for a 30V pulse on C_{tx} with the energy needed to charge C_{bias} to 120V, as shown in the following equation:

$$\left.\begin{aligned} E_{c,\text{bias}} &= \tfrac{1}{2} C_{\text{bias}} V_{\text{bias}}^2 \text{ [J]} &&= \tfrac{1}{2} \cdot 50 C_{\text{tx}} \cdot 120^2 \text{ [J]} &&= 360000\, C_{\text{tx}} \text{ [J]} \\ E_{c,\text{tx}} &= \tfrac{1}{2} C_{\text{tx}} V_{\text{tx}}^2 \text{ [J]} &&= \tfrac{1}{2} C_{\text{tx}} \cdot 30^2 \text{ [J]} &&= 450\, C_{\text{tx}} \text{ [J]} \end{aligned}\right\} \Rightarrow E_{c,\text{bias}} = 800\, E_{c,\text{tx}} \text{ [J]} \qquad (1.2)$$

This means that the energy required to charge the bias capacitor is approximately 800 times larger than that needed for a single pulse on the transducer. Because the inductor is fixed in the resonant pulser, it is not possible to optimize it for buck-boost operation. This can make a significant difference in the efficiency of the converter. From this perspective, it is the question whether the resonant pulser technique is still the right path forward, or if a conventional power converter in combination with a class-D pulser supplied by a high-voltage capacitor would be more energy efficient.

1.5. Problem Statement

The main question addressed in this thesis is the development of an energy-efficient ultrasound system suitable for wearable applications. For a wearable it is important that the system has minimal off-chip components and it must be energy-efficient. The resonant pulser technique is efficient in generating high-voltage pulses but requires complex calibration, or lacks features which improves imaging performance, such as beamforming and pulse-trains. Conventional class-D pulsers can provide these features, but have full CV^2 losses. Additionally, the efficient generation and management of high-voltage biasing for CMUTs from low-voltage supplies remains a challenge. Because the energy required to build up the bias voltage is significantly higher than that needed for a single pulse on the transducer, the question arises if it is not more efficient to recycle the bias energy, instead of pulsing energy.

The operating region of the proposed converter is fundamentally different from conventional converters, which opens up a new field of research. Combined with the need for energy recycling, this makes it crucial to explore the proposed converter architecture and its potential for wearable ultrasound systems. More generally, the central question is whether a deeper understanding of the converter load and its behavior can be used to optimize the architecture towards higher energy efficiency, and ultimately energy recycling, particularly for wearable US applications.

1.6. Research Objectives and Approach

The objective of this thesis is to investigate and develop a power converter and pulser architecture that enables energy-efficient ultrasound operation in wearable devices. The approach includes:

- Studying and comparing different converter and pulser topologies for their suitability in wearables.
- Designing and implementing a prototype based on the most promising architecture.
- Evaluating the performance through circuit-level simulations and comparing the results to the requirements for wearable ultrasound systems.

1.7. Design Scope

This section outlines the scope and limitations of the design work presented in this thesis. The focus is on the conceptualization, prototyping, and simulation of the power converter and pulser architecture for wearable ultrasound applications.

Design

- The design focuses on application-specific ultrasound (US) wearable devices.
- Example in healthcare: a US skin-patch device capable of measuring bladder volume.
- The design must demonstrate improvement or introduce a novel technique.
- Use of off-chip components must be minimized.
- The overall volume and area of the device must be acceptable for wearable applications.
- The focus should be on demonstrating new methods or functionalities in the new architecture; therefore, limitations depending on available technologies or devices will not be a show-stopper. However, it must be functionally demonstrated that the entire system can work.

Technology

- The design must be implementable with the technologies available for this project:
  - **TSMC 180nm BCD Gen 2 Technology**
    - Given Design Limitations
      - Maximum gate width: $10.000 \mu m$
    - Technology Limitations
      - Voltage limited to maximum of 65 V
  - **Xiver Collapse mode CMUT Transducer Types:**

* **CM5**: f = 2.6 MHz, C_e = 120 pF
* **CM8**: f = 5 MHz, C_e = 80 pF
* **CM12**: f = 8 MHz, C_e = 20 pF
* **Xiver CM5 transducer has been selected** based on the following considerations:
  - (+): Lowest operation frequency, best performing penetration depth.
  - (-/+): high capacitance, this will lead to higher energy losses which makes innovation in energy recycling methods more important.
  - (–): Lowest operation frequency, lower resolution. Assuming US wearables would be application specific so data efficient, this should not be a problem. In the meantime, lower frequency means lower data-rate, which is also an advantage for wearables.

Power Converter

- Must enable to operate the system on a low-power energy source, such as a single lithium cell with a voltage of 3.6 V.
- Must provide output voltages in ranges from 0 to 120 V for CMUT biasing .
- Must provide output voltages in ranges from 0 to 30 V for pulser operation.
- Must enable energy recycling between high- and low-voltage power stages.
- Must be able to supply recycled energy to other parts of the system. Either to improve efficiency or to eliminate limitations of batteries such as non-rechargeability or complicated charging and discharging specifications.

Ultrasound Pulse Acquisition

- Transmission/Reception method: Synthetic Aperture (SA).
- Transmission: single-channel.
- Reception: multi-channel.
- Ability to switch between Tx and Rx modes.
- Transceiver capabilities:
  - Transmission up to 64 channels (expected usage: 4 channels).
  - Tx pulse-train functionality (expected length: 5 pulses).

Xiver Collapse mode CM5 Transducer

The Xiver CM5 is a Collapse mode CMUT transducer that consists of a lin64 elements (channels), with 33 CMUT drums per element. For a bias voltage of 120 V, the corresponding transducer parameters per element are summarized in Table 1.1.

Parameter	Value
Bias Voltage (V_{bias})	120 V
Electrical Capacitance (C_e)	118.8 pF
Mechanical Capacitance (C_m)	56.1 pF
Mechanical Inductance (L_m)	68 μH
Mechanical Resistance (R_m)	1.6 kΩ
Resonance Frequency	2.58 MHz
Drums per Element	33
Number of Elements	64
Active Area	12×21 mm^2
Pitch	315 μm

Table 1.1: Xiver CM5 CMUT Parameters

Other considerations

- Operating temperature range: 20–40 °C (body temperature range).

1.8. Thesis Outline

The report is structured as follows:

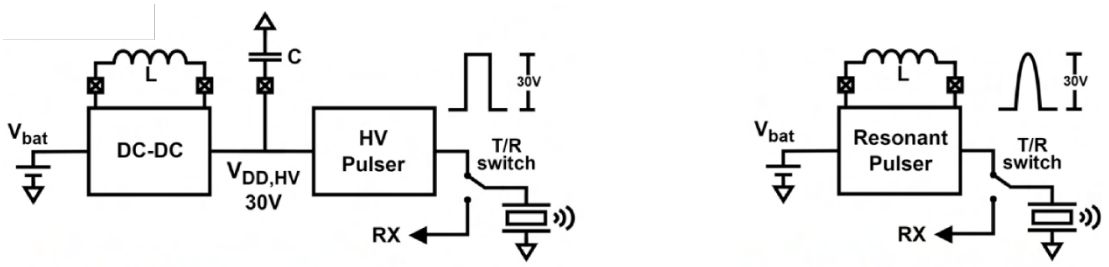
- **Chapter 2: Architecture Study**
  This chapter reviews the requirements and explores possible system architectures for energy-efficient ultrasound in wearable applications. It compares different converter and pulser topologies, and motivates the selection of the most promising approach for further development.
- **Chapter 3: Prototype Design**
  Here, the chosen architecture is translated into full system implementation with detailed circuit design. The chapter discusses the design choices, implementation challenges, and integration of the power converter and pulser within the constraints of the selected technology.
- **Chapter 4: Circuit-Level Simulations**
  This chapter presents simulation results of the designed circuits. It evaluates the performance, efficiency, and functionality of the prototype under various operating conditions, and compares the results to the initial requirements.
- **Chapter 5: Conclusion and Future Work**
  The final chapter summarizes the main findings, discusses the limitations of the current work, and suggests directions for future research and improvements.

2

Architecture Study

2.1. Prior Art

Conventional class-D ultrasound (US) pulsers as described in [14] are highly developed and offer a wide range of functionalities, including advanced features such as beamforming and pulse-train generation. However, a recently developed technique called Resonant Pulsing (RP) [4] enables energy recycling during ultrasound pulsing in capacitive micromachined US transducers (CMUT). Despite its potential for energy savings, this technology is still in its infancy and lacks many features compared to conventional pulsers. Additionally, CMUT devices require high voltage biasing, which can entail significant energy losses and is not yet included in the RP design.



(a) Conventional Class-D Pulser

(b) Resonant Pulser

Figure 2.1: Introduction to Resonant and Conventional Class-D Pulsers

Theoretically, by adding a single switch to the output of the RP design, it should be possible to use the same architecture to charge and discharge the biasing capacitance while maintaining energy recycling capabilities. However, a significant drawback exists: since the inductor size is determined by the resonance frequency relative to the CMUT, charging and discharging this biasing capacitance may not be efficient. This is particularly problematic considering that the energy stored in the bias capacitance is estimated to be thousands times larger than the energy needed for a single pulse in the CMUT.

Given these limitations of the RP design, it raises the question whether resonant pulsing is the right path forward. Investigating from a wearable system perspective, it remains unclear whether the energy savings from pulse recycling outweigh the limitations of the RP architecture. Additionally, alternative energy recycling techniques applied elsewhere in the system may address larger energy losses.

For these reasons, a new architecture has been composed. Like the resonant pulser, it incorporates a 4-switch configuration with a single inductor. However, instead of directly driving CMUTs as the load, it features a multi-output design to charge and discharge DC capacitors for biasing and DC voltages. This allows a conventional pulser to be used, powered through charge-sharing principles from the DC capacitance. Under this configuration, it becomes possible to efficiently select the inductor, potentially yielding energy gains. Furthermore, well-developed techniques become available through the use of the

class-D pulser, such as pulse trains that improve signal-to-noise ratio (SNR) and can therefore provide energy savings in pulse acquisition. A drawback of this architecture is that a conventional class-D pulser introduces full CV^2 energy losses, which are largely recycled in the resonant pulser.

2.2. Problem Statement

This simulation study aims to determine which architecture, resonant pulsing or the new multi-output converter with conventional class-D pulser, is more energy-efficient for wearable ultrasound applications. The comparison will focus on several key aspects:

- **Energy efficiency analysis**: Quantifying the total energy consumption per ultrasound acquisition, including both pulse generation and biasing energy requirements.
- **Design optimization**: Identifying the optimal design variables for each architecture, such as inductor sizing or switch sizing.
- **Architecture trade-offs**: Evaluating when each architecture performs better under different operating conditions and system .specifications.

The primary metric for comparison will be the net energy consumption, taking into account both the charged, pulsed and recycled energy losses inherent to each architecture. However, comparing both architectures without selecting (reasonable) optimal design variables, will provide a unfair comparison. That is why this simulation study will also focus on identifying the optimal design variables for each architecture, such as inductor sizing or switch sizing. After determining the optimal architecture, a more detailed simulation is performed to identify design-keys and architecture performances usefull for prototyping.

2.3. Method

This chapter outlines the approach taken to compare the energy efficiency of the two architectures. First, an analytical approach is used to identify both systems in terms of energy efficiency, associated design parameters and their boundaries. Also identified design risks or conflicts will be discussed. Consequently, this section will conclude the main considerations and motivation for choosing a simulation-based approach. At the end, the simulation models are introduced whereafter the simulation setup for each architecture will be described.

2.3.1. Fundamental Analysis

Architectures

As introduced, two scenarios are considered: (1) using the resonant pulser architecture for charging the biasing capacitor with fixed inductor size, which means efficient pulsing up to 76.8% energy loss reduction [4], but at cost of inefficient biasing. Or (2) using a conventional DC/DC converter with class-D pulser architecture, which has full capacitive pulse energy losses but offers higher efficiency for both charging and recycling energy to biasing capacitor and the DC capacitor used for pulsing.

Since pulsing energy losses have already been well described in literature, this chapter focuses primarily on the energy flow related to DC capacitors using the 4-switch configuration. In general, the energy stored in a capacitor is given by the equation 2.1, where C is the capacitance and V is the voltage across the capacitor. The energy stored in a inductor is given by the equation 2.2, where L is the inductance and I is the current through the inductor.

$$E_C = \frac{1}{2}CV^2 \quad [15] \tag{2.1}$$

$$E_L = \frac{1}{2}LI^2 \quad [15] \tag{2.2}$$

The assumption is made that to charge a capacitor to a certain energy level, for a chosen energy stored in L minus the associated energy losses, we need N_c charge-discharge cycles for L, as shown in equation 2.3. Combining these three equations results in equation 2.4, which states that, for a fixed output capacitance

C_{out} and output voltage V_{out}, the stored energy at the load capacitor depends on the number of cycles N_c, the inductor size and peak current I_{pk} through the inductor.

$$N_c(E_L - E_{loss}) = E_C \tag{2.3}$$

$$N_c \cdot (\frac{1}{2}LI_{pk}^2 - E_{loss}) = \frac{1}{2}C_{load}V_{load}^2 \tag{2.4}$$

Charging the inductor from an initial state of zero energy, the peak current is given by formula 2.5. Where V is the voltage across the inductor, L is the inductance and T is the time needed to charge or discharge the inductor. In reality the discharging step can be described by a second order differential equation between the inductor and capacitor.

Assuming the energy losses are mainly induced by resistive and gate switching losses, the energy losses are approximated by equation 2.6. Other losses to mention are losses which occurs in surrounding systems or layout by resistive connections and parasitic capacitances, but are left for now assuming they are less dominant.

$$\mid \Delta I \mid = \mid I_{pk} \mid = \frac{V_{source}}{L}T_{charge} \approx \frac{V_{load}}{L}T_{discharge} \quad [16] \tag{2.5}$$

$$E_{loss} \approx E_R + E_{gsw} \tag{2.6}$$

The resistive losses are induced by the current through the on-resistances of the switches and inductor. While this resistances are in each operation of the system always in series, the equivalent series resistance R_s can be obtained. Obviously as illustrated in equation 2.5 and 2.7, the losses becomes higher at higher currents or resistances. Additionally, V_{load} will differ per cycle, which indicates varying losses over time when energy transfers between L and C.

$$E_{loss-R} = \int_{t_0}^{t_0+T_{charge}} R_{s1}I(t)^2dt + \int_{T_{charge}^+}^{T_{charge}+T_{discharge}} R_{s2}I(t)^2dt \quad [15] \tag{2.7}$$

The next sub-section will briefly outline the individual components.

MOSFET Device

Energy losses in MOSFET devices are typically caused by resistive and switching losses. The switching losses are mainly caused by gate driver stages and CV^2 energy losses used for driving the gate capacitance per switching event of the MOSFET device. The optimal number of stages to drive the switch gate is related to the inter- and outer-stage fan-out f and F as shown in equation 2.8 and 2.9.

$$N = \log_f(F) \quad [17] \tag{2.8}$$

$$F = \frac{C_{gg}}{C_{in}} \quad [17] \tag{2.9}$$

The inter-stage fan-out f is an adjustable variable which is a trade-off between speed and power consumption. Typically values around 4 are close to optimal [17], which should be a good starting point. When the number of stages is defined and round to an integer, the total dynamic power dissipation in driver and gate capacitance can be approximated by equation 2.10. With C_{gg} being the total input capacitance at the gate of the MOSFET, and V_g the gate drive voltage and N the number of driver stages.This is the energy loss per switching event of the MOSFET.

$$E_{driver-gate} = \sum_{k=0}^{N} \frac{1}{4^{(N-k)}} \cdot C_{gg} V_g^2 \quad [17] \tag{2.10}$$

Resistive losses are caused by the on-resistance R_{on} of the MOSFET device. The resistive losses are given by equation 2.11, where R_{on} is the on-resistance and I the current through the MOSFET device over time.

$$E_{loss-Ron} = \int_{t_0}^{t_1} R_{on} I(t)^2 dt \tag{2.11}$$

To conclude, the MOSFET switch devices should have a minimized V_g, R_{on} or C_{gg}. This conflicts with the physical characteristics of the MOSFET as explained in [17, 18]. Investigating the on-resistance and gate capacitance, they have conflicting interests in the physical dimensions of the device as shown in equation 2.12 and 2.13. In this formulas are C_u and R_u the capacity and resistance per unity area. Minimal device lengths are in favour of both minimal resistance and capacities. However, larger device widths results in less on-resitance but larger gate (and parasitic) capacitances and vice-versa. So sizing the device is an optimization problem between E_{gsw}, $E_{loss-Ron}$. Then, for most MOSFET devices used as switch, the gate drive voltage is typically recommended or set dependent of process technology. This means that if the choice is possible, devices with lowest possible gate voltages should be considered.

$$C_{gg} \approx W \cdot L \cdot C_u \quad [17] \tag{2.12}$$

$$R_{on} \approx \frac{L}{W} \cdot R_u \quad [17] \tag{2.13}$$

Inductor

The inductor is a critical component in both architectures, as it stores and transfers energy between the source and the load. Although in the first approximations the inductor is assumed to be ideal or with fixed resistances, it is important to consider the limitations, parasitics and design variables of a real inductor to understand or prevent problems in later stages of the design.

Assuming a solenoid inductor, the inductance is given by equation 2.14. Where N is the number of turns, A is the cross-sectional area, and l is the length of the inductor. The inductance can be maximized by increasing both the number of turns, the cross-sectional area or the length of the solenoid. Increasing the number of turns is at costs of the wire resistance as showed in equation 2.15, where ρ is the resistivity of the wire material, l is the length of the wire, and A_w is the cross-sectional area of the wire.

$$L = \frac{\mu_0 N^2 A}{l_s} \quad [19] \tag{2.14}$$

$$R_L = \rho \frac{l_{wire}}{A_{wire}} \quad [19] \tag{2.15}$$

In favour of both higher inductance and lower wire resistance, larger areas are preferred. However, larger areas also increase the size of the inductor, which is a critical limitation in wearable applications. An engaging effect is increase of parasitic capacitances between between the wires, which can limit the operating frequency or the self-resonance frequency of the inductor it self. Additionally favour for inductance and resistance is the use of materials with low resistances or high (core) permeabilities. This could also benefit in lowering the total area or volume of the inductor, but this will depend on availability or budget.

A general approach to indicate the quality of an inductor is the Q-factor 2.16. This is a frequency dependent ratio between the inductance and the DC wire resistance of the inductor. A higher Q-factor indicates a better quality inductor with lower losses at a certain frequency. Note that higher Q-factors will conflict with the physical size of the inductor. When choosing a real inductor, the Q-factor could be maximized for the frequency of operation and maximum allowed physical size of the inductor.

$$Q = 2\pi f \cdot \frac{L}{R_L} \quad [15][19] \tag{2.16}$$

The total energy stored in the inductor is given, as mentioned before in equation 2.14, in the following equation:

$$E_L = \frac{1}{2}LI^2 \quad [15] \tag{2.17}$$

On-Chip wires are typically small, which results in low inductance values and high resistances. The expectation is, as indicated above, this leads to low Q-factors, making them inefficient for energy storage and transfer. This is why off-chip inductors are preferred.

Capacitor

The capacitor is a critical component in both architectures, as it stores and releases energy between the source and the load. Although in first-order approximations the capacitor is assumed to be ideal, it is important to consider the limitations, parasitics and design variables of a real capacitor to understand or prevent problems in later stages of the design.

The amount of charge that can be stored on a capacitor is directly proportional to both its capacitance and the voltage applied across it. This relationship is expressed as

$$Q = C \cdot V \quad [15] \tag{2.18}$$

where Q is the charge in coulombs, C is the capacitance in farads, and V is the voltage in volts. A larger capacitance or higher voltage allows more charge to be stored. Assuming a parallel-plate capacitor, the capacitance is given by equation 2.19. Where ϵ is the permittivity of the dielectric material, A is the plate area, and d is the separation between the plates. The capacitance can be maximized by increasing the plate area or decreasing the distance between the plates. However, reducing the plate spacing is limited by breakdown voltage of the material.

$$C = \epsilon \frac{A}{d} \quad [15] \tag{2.19}$$

In favour of both higher capacitance and higher voltage ratings, larger plate areas are preferred. However, larger areas also increase the physical size of the capacitor, which is a critical limitation or very costly for on-chip applications.

From the extracted values of the TSMC 180 nm PDK, the capacitance density for a 'CFMOM' type capacitor is found to be approximately $1.30\,\mathrm{fF}/\mu\mathrm{m}^2$. This implies that to realize a capacitance in the nanofarad range, an area of about $1000 \times 1000\ \mu\mathrm{m}^2$ (i.e. $1\,\mathrm{mm}^2$) would be required for 1 nF. Such an area is technically feasible but very large for on-chip integration in 180 nm technology. Therefore, in practical circuit design, a trade-off must be made between placing capacitors on-chip, where integration and parasitic reduction are beneficial, or off-chip, where much higher capacitance values can be achieved without significant area penalties.

2.3.2. Simulation Models

This section describes the simplified models used for both architectures, highlighting their similarities and key differences in terms of circuit topology and operation. The models were specifically developed to allow implementation and simulation in MATLAB, enabling flexible analysis and efficient exploration of a large number of parameters. Since the architectures can be simulated in a step-by-step manner, they can be broken down into simple subsystems. By deriving the corresponding state-space models for each subsystem and sequentially combining them while sharing their state variables, the complete cycle of both architectures can be simulated in a structured and straightforward way. This approach allows for detailed investigation of various parameters and components, and enables analysis of their impact on the energy efficiency of both architectures.

The following section outlines practical consideration and explains the structure of the implemented models. After introducing the models, the simulation setup for both architectures will be described. Finally, it will be detailed how the different operating cycles of both systems are simulated using these models.

Practical Considerations and Implemented Architecture Models

In TSMC 180nm BCD Gen2 technology, the maximum safe operating voltage is limited to 65 V. Exceeding this value risks permanent damage to the substrate. However, the CMUT requires a bias voltage of up to 120 V, which is well beyond the intrinsic voltage tolerance of the technology. A pragmatic solution is chosen that allows the desired bias voltage to be reached while remaining fully compatible with the available technology and project objectives. A floating capacitor configuration in combination with a diode can be employed for isolation, as shown in Figure 2.2. This configuration makes use of two capacitors connected in series. The charging process can be compared to a two-stage rocket. During the first stage, indicated by ϕ_1 in red, the upper capacitor is charged from the inductor current while the switch is closed. Subsequently, the switch opens, and the lower capacitor is charged, causing the voltage of the upper capacitor to float along. This process finally results in a combined voltage of 120 V across the series connection after both capacitors are charged to 60 V.

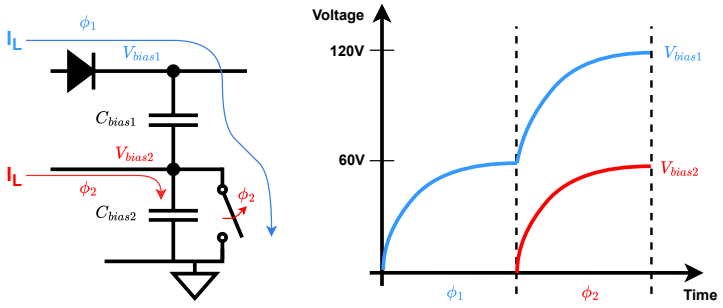


Figure 2.2: Floating capacitor configuration for generating a 120 V bias from a 65 V-limited technology

In order to protect the on-chip components from direct exposure to voltages higher than 65 V, the diode is placed between the high-voltage node of the floating capacitor stage and the system output. This provides isolation and ensures that the 120 V bias can be safely achieved with the available technology. However, this approach also comes with trade-offs. The diode prevents current from flowing back into the system, which is an advantage in terms of safety and reliability, but it also means that the stored energy in the upper capacitor is effectively trapped and cannot be recovered. Additional drawbacks are the voltage drop with resistive losses across the diode and the requirement for an extra output channel to bias the CMUT.

Furthermore, the use of two capacitors in series introduces an additional consideration regarding the effective capacitance. In general, the equivalent capacitance of capacitors connected in series is given by

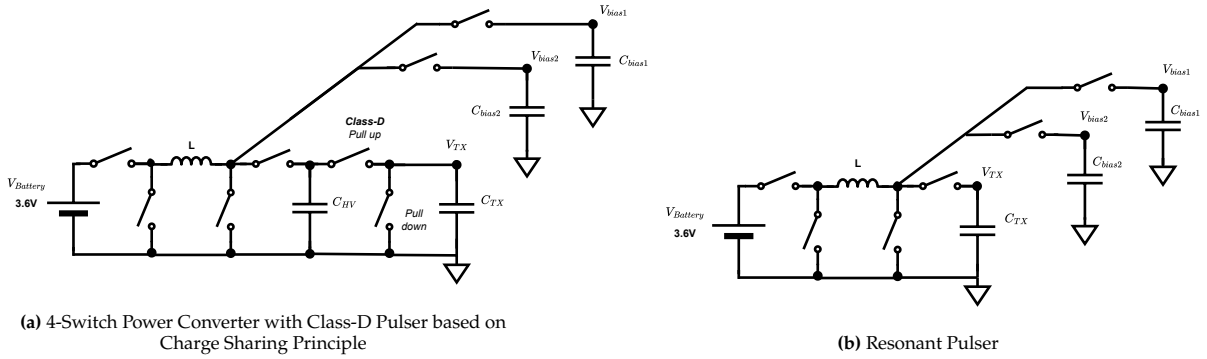
$$\frac{1}{C_{\text{eq}}} = \sum_{i=1}^{n} \frac{1}{C_i}. \tag{2.20}$$

For the case of two identical capacitors with capacitance C, this reduces to

$$C_{\text{eq}} = \frac{C}{2}. \tag{2.21}$$

This reduction in capacitance is not a fundamental limitation, but must be taken into account during the design phase. Because this configuration addresses the practical limitations of the TSMC technology rather than a fundamental constraint of the proposed architecture, these drawbacks are not considered an obstacle for this work. With this approach, the primary objective can still be achieved, namely to demonstrate the feasibility of the architecture. In future implementations, when CMUT devices are innovated with lower biasing voltages or technology processes with higher voltage tolerances may be available, these practical workarounds will no longer be required.

That is why in this project this practical solution will be used, which means that a power converter capable of charging two bias capacitors is required. As illustrated in Figure 2.3, both architectures consist of a 4-switch power converter with a single inductor used to drive capacitive loads. The schematic to charge- and discharge the biasing capacitor are similar. The main difference lies in inductor optimization and the pulser design: the conventional class-D pulser uses a charge-sharing principle, whereas the resonant pulser drives the transducer at its resonant frequency using the same 4-switch configuration.



(a) 4-Switch Power Converter with Class-D Pulser based on Charge Sharing Principle

(b) Resonant Pulser

Figure 2.3: Simplified Schematics of Architectures

MOSFET Switch Characteristics

This section describes the used switching models and key characteristics of the MOSFET devices. During switching and conduction, power losses occur in the switches, as previously explained in Section 2.3.1. These losses are determined by both type and size of the selected MOSFET. Based on these input variables, relevant characteristics of each MOSFET including driver losses are calculated at the start of the simulation.

During simulation are switching losses calculated by counting the number of switching events. In the meantime, the on-resistance of the switches is included in the equivalent series resistance. This combined resistance is incorporated into the transient state-space models described in the following sections.

All device parameters have been extracted from the TSMC 180nm BCD-Gen2 process design kit (PDK) using Cadence simulation tools. Table 2.1 summarizes the most relevant unity parameters for the selected devices, including on-resistance and various parasitic capacitances.

It is important to note that devices rated for higher voltages inherently exhibit higher on-resistances and larger gate capacitances. For example, the 65V devices show significantly higher $R_{\mathrm{on-u}}$ and $C_{\mathrm{gg-u}}$ values compared to the 5V low-Ron devices. These characteristics directly impact the conduction and switching losses in the converter and must be carefully considered during the design and optimization process.

The table also includes the total drain and source capacitances ($C_{\mathrm{dd-u}}$ and $C_{\mathrm{ss-u}}$), as well as the gate length (L_{gate}) for each device. While these parameters are not directly used for accurate modeling of the switching behavior, they are important for validating simulation results afterwards.

All values in Table 2.1 are obtained from the PDK device models and reflect the typical performance in simulation. These characteristics form the basis for the subsequent selection and sizing of switches in both the low-voltage and high-voltage sections of the converter, which will be discussed in detail in the following sections.

It is important to note that the HV switches inherently exhibit higher on-resistances and capacitances. This is crucial for later analyses and validation of the simulations.

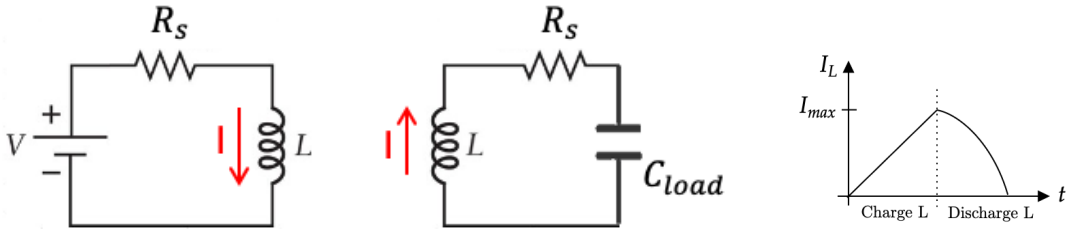
Device Name	Voltage Rating [V]	R_{on-u} [$\Omega \cdot \mu$m]	C_{gg-u} [F/μm]	C_{dd-u} [F/μm]	C_{ss-u} [F/μm]	L_{gate} [μm]
nch_5_switch_low_ron_mac	5	1798	1.72×10^{-15}	9.04×10^{-16}	1.14×10^{-15}	0.550
pch_5_switch_low_ron_mac	5	5131.5	1.42×10^{-15}	8.48×10^{-16}	1.05×10^{-15}	0.470
nld65_g5b_mac	65	11726	4.61×10^{-15}	2.52×10^{-15}	3.92×10^{-15}	0.700
nld65_g5b_mac_BB	65	23451	9.21×10^{-15}	–	–	–

Table 2.1: Overview of unity parameters for MOSFET devices in 180nm BCD-Gen2 technology, including voltage ratings, drain and source capacitances. Values extracted from Cadence PDK simulations for indicated gate lengths.

2.3.3. Transient Models

Store Energy to Load Capacitor

To charge a load capacitor, both architectures follow a similar process. Initially, the inductor is charged from the source until it reaches a maximum current, whereafter the inductor is switched to discharge its current or energy into the capacitive load. After all energy from the inductor is discharged, if current zero-crosses, the output switch is turned off and all energy is transferred to the load capacitor. The submodels used are illustrated with current behavior in Figure 2.4. These steps are repeated until the output voltage reaches the desired level. This model is used for charging the biasing capacitor in both architectures, as well as for charging the DC load capacitor in the class-D pulser architecture.



(a) step 1 - charge L from Source

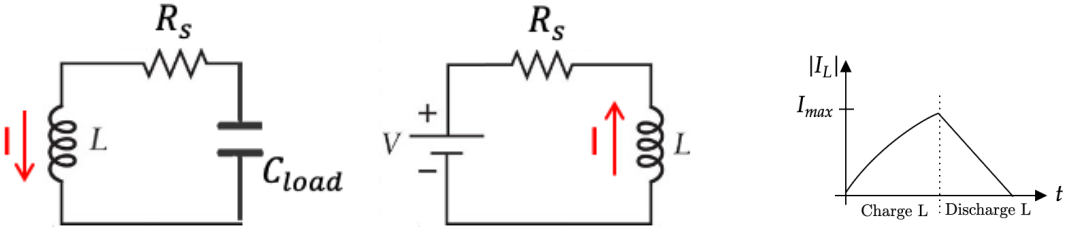
(b) step 2 - store energy to Load Capacitor

(c) Current Behavior

Figure 2.4: Sequential sub-models Charging Load Capacitor Cycle

Recycle Energy from Load Capacitor

Discharging the load capacitor is similar, but the other way around. For this case, initially, the inductor gets charged with energy stored at the capacitive load, whereafter it is switched to the source to discharge its energy back. This process repeats itself until energy is transfered and nothing is left on the capacitor. It is measured when the output voltage crosses zero while charging the inductor from the load capacitor. This means that the end time of charging the inductor from the load capacitor is triggered by both maximum current and zero-crossing of the output voltage. This process is illustrated in Figure 2.5 and used for energy recycling.



(a) step 1 - charge L from Load Capacitor

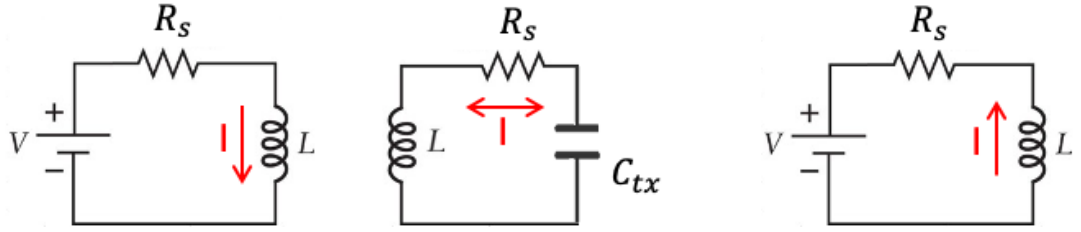
(b) step 2 - recycle energy to Source

(c) Current Behavior

Figure 2.5: Sequential sub-models Recycle Energy from Load Capacitor Cycle

Resonant Pulse Cycle

Merging previously mentioned models and leaving out switching off the load capacitor in between, it follows that charged energy on the load capacitor will flow back into the inductor. This mechanism is used for resonant pulsing the capacitive transducer. This can be modelled by a charging step for the inductor by pre-calibrated time or maximum current, whereafter the stored energy in the inductor wil resonate with the load capacitor. When the energy is fully bounced back to the inductor, the inductor is switched and the energy flows back to the source. The result is a half sine pulse at half time of the resonating frequency between L and C. The pre-calibrated time or maximum current is related to the pulse amplitude as explained in [4]. The sequential model with voltage and current graph are illustrated in Figure 2.6 and 2.7.



(a) Step 1 - charge L from Source

(b) Step 2 - Resonate L with C_{tx}

(c) Step 3 - recycle energy to Source

Figure 2.6: Sequential sub-models Resonant Pulse Cycle

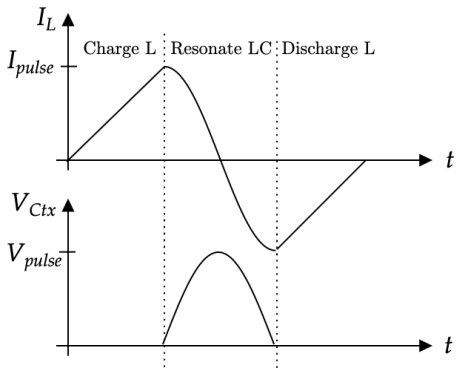
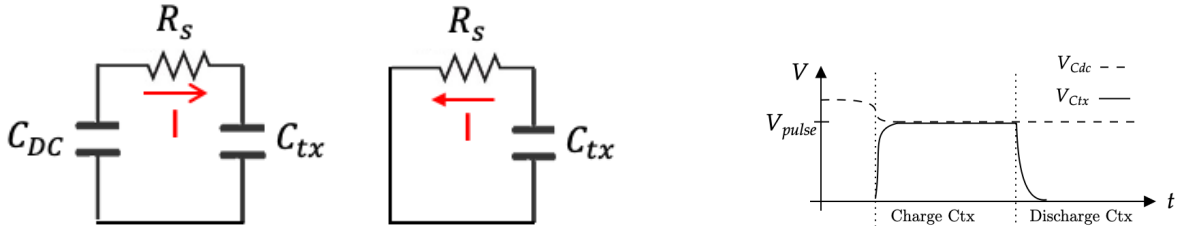


Figure 2.7: Voltage and Current Behavior of Resonant Pulse Cycle

Class-D Pulse Cycle

At the end, the model for class-D pulser based on charge sharing is presented. Before this model is used, the DC capacitor is charged as explained before. This model contains charge sharing principle between DC capacitor and transceiver, whereafter the pulse length the charge is resetted to ground. This sub-models and steps are illustrated in Figure 2.8.



(a) step 1 - charge Ctx from Cdc

(b) step 2 - discharge Ctx to GND

(c) Voltage Behavior

Figure 2.8: Sequential sub-models Class-D Pulse Cycle

The voltage drop over the DC capacitor after each pulse can be calculated using the law of conservation of charge, as shown in equation 2.25. [15]

Assuming an initial voltage $V_{dc-initial}$ on the DC capacitor, and zero voltage on the transducer capacitor, then the initial total charge over both capacitors is given by equation 2.22. After charge sharing, the total charge must be equal, and the new voltage can be calculated by equation 2.24. Combining these equations results in equation 2.25, which describes the voltage drop over the DC capacitor after each pulse.

The voltage drop over the DC capacitor after each pulse can be calculated using the law of conservation of charge, as shown in equation 2.25. [15]

Assuming an initial voltage $V_{dc-initial}$ on the DC capacitor, and zero voltage on the transducer capacitor, the initial total charge over both capacitors is given by

$$Q_{\text{total}} = C_{\text{DC}} V_{dc-initial} + C_{\text{TX}} \cdot 0 = C_{\text{DC}} V_{dc-initial} \tag{2.22}$$

After charge sharing, the total charge must be equal, and the new voltage on both capacitors can be calculated by

$$Q_{\text{total}} = (C_{\text{DC}} + C_{\text{TX}}) V_{\text{final}} \tag{2.23}$$

Solving for the final voltage gives:

$$V_{\text{final}} = \frac{C_{\text{DC}}}{C_{\text{DC}} + C_{\text{TX}}} V_{dc-initial} \tag{2.24}$$

Combining these equations results in the voltage drop over the DC capacitor after the first pulse is given by:

$$\Delta V_{\text{DC}} = V_{dc-initial} - V_{\text{final}} = \frac{C_{\text{TX}}}{C_{\text{DC}} + C_{\text{TX}}} V_{dc-initial} \tag{2.25}$$

or stepwise for sequential pulses as used in pulse-trains:

$$\boxed{\Delta V_{\text{DC}}^{(n)} = \frac{C_{\text{TX}}}{C_{\text{DC}} + C_{\text{TX}}} V_{\text{DC}}^{(n-1)}} \tag{2.26}$$

Assuming Cdc = 100xCtx and Vdc-initial = 30V, the voltage drops for the first pulses are approximatley:

$$\Delta V_{\text{DC}} \approx \frac{1}{1 + 100} \cdot 30 \approx 0.3\,\text{V} \tag{2.27}$$

Table 2.2 shows the voltage drop over the DC capacitor for different ratios between the DC capacitor and transducer capacitance when choosing an initial voltage of 30V. These values can be used to verify the simulation results.

Table 2.2: Voltage drop over the DC capacitor for 5 pulses ($C_{\text{DC}} = 100\,C_{\text{TX}}$, $V_{dc\text{-initial}} = 30$ V)

Pulse #	$V_{\text{DC, initial}}$ [V]	$V_{\text{TX}} = V_{\text{DC, final}}$ [V]	ΔV [V]
1	30.000	29.703	0.297
2	29.703	29.407	0.296
3	29.407	29.113	0.294
4	29.113	28.822	0.291
5	28.822	28.532	0.290

Setup Sub-Models per Architecture

By combining all described steps and sub-models, the complete operating cycle of both architectures can be simulated, as summarized in Table 2.3 and Table 2.4. Executing these steps in the correct sequence enables a transient simulation that accurately reproduces the behavior of both systems. This approach allows for easy simulation across a wide range of variables, and additional models can be incorporated or extended where needed. Since the models are implemented using simple state-space representations, they can be solved efficiently under predefined conditions or constrains. Moreover, the simulation provides detailed insight into each step of the operation, including when and where energy losses occur, allowing for a clear comparison of the energy efficiency of both systems.

Step	Description	Finish Condition
1	Store Energy to Biasing Capacitor1	$V_{bias} > V_{target-bias}$
2	Store Energy to Biasing Capacitor2	$V_{bias} > V_{target-bias}$
3	Store Energy to DC Capacitor	$V_{dc} > V_{target-dc}$
4	Class-D Pulser	Repeat N Pulses
5	Recycle Energy from Biasing Capacitor	$V_{bias} \leq 0$
6	Recycle Energy from DC Capacitor2	$V_{hv} \leq 0$

Table 2.3: Steps for Class-D Pulser Architecture

Step	Description	Finish Condition
1	Store Energy to Biasing Capacitor1	$V_{bias} > V_{target-bias}$
2	Store Energy to Biasing Capacitor2	$V_{bias} > V_{target-bias}$
2	Resonant Pulse	Repeat N Pulses
3	Recycle Energy from Biasing Capacitor2	$V_{bias} \leq 0$

Table 2.4: Steps for Resonant Pulser Architecture

Note that in both configurations, the energy stored in the first bias capacitor cannot be recovered due to the presence of the diode as explained in section 2.3.2.

2.4. Architecture Simulations

This chapter presents a comprehensive simulation study of the power converter architectures and their key design variables. The following sections discuss the switch configuration and technology choices, the main simulation parameters, and the impact of inductor size, output capacitance, and output voltage on energy efficiency. Both the resonant and conventional pulser architectures are analyzed and compared, including detailed optimization of switch sizes and system currents. The results include break-even analyses, practical component selection, and a summary of the final configuration with detailed energy and timing breakdowns. Altogether, the results highlight the key trade-offs and design choices that determine power conversion efficiency in the next prototype of wearable ultrasound systems.

All simulations are performed using a basic four-switch topology as shown in the following figure. This schematic indicates the main voltages and component names. Naturally, the output names for the voltage and capacitor depends on the application, for example, when used for pulsing, the output voltage is called V_{tx} and the output capacitor C_{tx}, while for biasing, these are called V_{bias} and C_{bias} respectively.

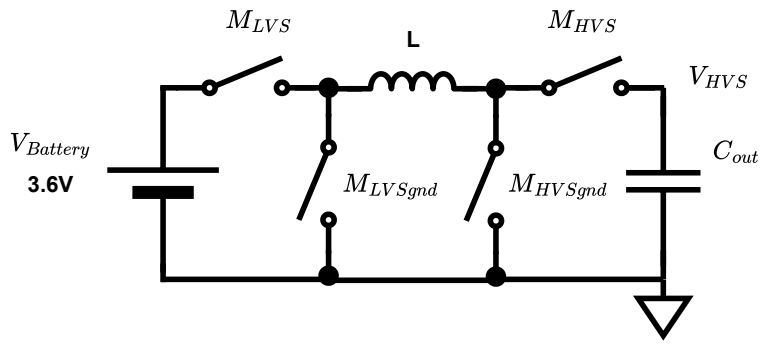


Figure 2.9: Basic four-switch topology used for simulations of both architectures

2.5. Resonant Pulser versus Conventional Pulser

2.5.1. Bias Circuit 65V Simulations

This section describes the simulations performed to analyze the bias circuit. The focus is on how different parameters affect the performance of the power converter in charging and discharging the output capacitor. In this section are the following aspects investigated in advantage of energy efficiency:

1. The effect of inductor size
2. The influence of output capacitance
3. The impact of varying output voltage

The specific switch configuration used in the biasing power converter is summarized in Table 2.5. This table lists the device types selected for each switch position in the four-switch topology, based on the requirements for voltage rating and on-resistance as discussed above. The chosen configuration ensures reliable operation within the voltage limits of the technology, while minimizing conduction and switching losses. The use of a back-to-back device for the high-voltage output switch further improves isolation and prevents unwanted current paths during operation.

Switch Name	Device Type
LVSgnd	nch_5_switch_low_ron_mac
LVS	pch_5_switch_low_ron_mac
HVSgnd	nld65_g5b_mac
HVS	nld65_g5b_mac_BB

Table 2.5: Switch configuration for biasing power converter

Inductor Optimization

In this simulation, different inductor sizes are evaluated. Assuming equal series resistance, from section 2.1, it is expected that larger inductances will lead to lower energy consumption. The first question to be answered is while charging and discharging the (biasing) output capacitor, how much the energy consumption can be reduced by increasing the inductance. Then it must be determined how this competes with the profit in energy energy efficiency during pulse acqusitions using the resonant pulser.

The inductance is swept between 27μ H and 1000μ H, then the energy consumption is minimized by optimizing switch size and appropriate maximum current through the circuit.

A Monte Carlo simulation is performed to find the global minimum energy consumption by randomly sampling switch sizes and maximum current values for each inductor size. The results are shown in figure 2.10, where the inductance is plotted against the corresponding converter losses using optimal switch size system currents.

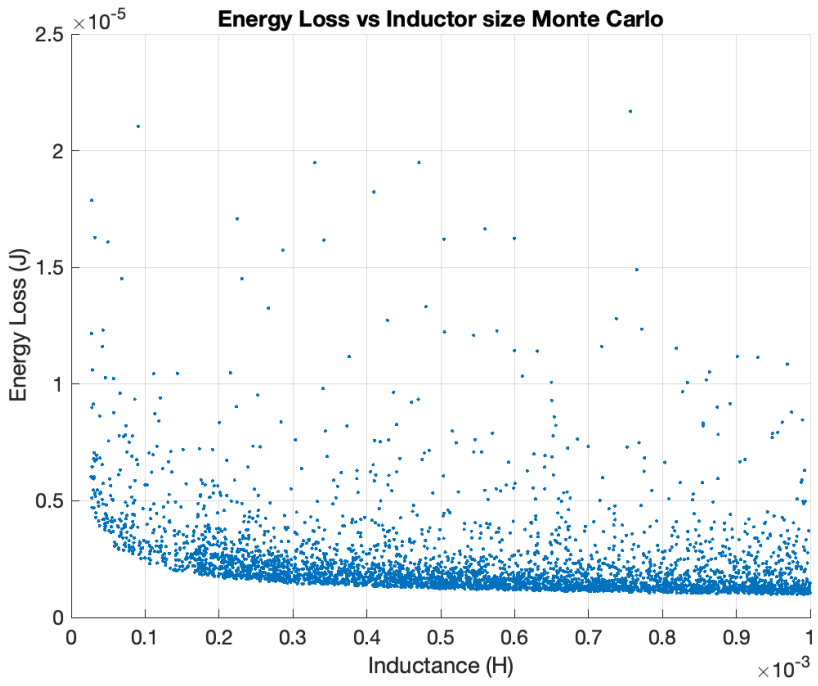


Figure 2.10: Bias Configuration - Monte Carlo Inductor size and corresponding energy loss

This simulation shows that the energy consumption decreases with increasing inductance, and so the largest inductor of 1000μH provides the lowest energy consumption.

To compare with the resonant pulser, which uses a 27μH inductor, the energy consumption is much lower when a larger inductor is used. For a single charge and discharge cycle, the energy consumption decreases from 4.42μJ to 0.97μJ, representing a reduction of approximately 78%. The energy losses, optimal switch sizes, and maximum current for both inductance values are summarized in Table 2.6. This table includes the energy consumption for two full cycles, as a 2-step charging method is used to charge the bias.

Inductor [μH]	**Switch Size [μm]**	**I_{max} [mA]**	**Energy Loss [μJ]**	**2x Energy Loss [μJ]**
27	4000	60	4.422	8.844
1000	10000	40	0.973	1.946

Table 2.6: Overview of energy loss for different inductor values with corresponding optimal switch sizes and maximum current

The difference in energy consumption is

$$\Delta E = 8.84 - 1.94 = 6.90\,\mu J$$

per charge and discharge cycle. By comparing this difference to the total transducer CV^2 pulse losses, it can be estimated that a converter with an optimally sized inductor and a class-D pulser is more energy efficient, as long as fewer than 65 pulses are transmitted per acquisition. This number is within the typical range for wearable applications. The energy efficiencies of both pulser configurations are further investigated in the following sections.

$$N_{tx} = \frac{\Delta E}{E_{\text{pulse}}} = \frac{(E_{L=27\mu H} - E_{L=1000\mu H})}{C_{tx} V_{pulse}^2} = \frac{6.90\,\mu J}{0.10692\,\mu\text{J}} \approx 65 \text{ pulses} \tag{2.28}$$

At this point, it became clear that the impact of inductor size on energy consumption is significant, and that the largest possible inductance should be selected. To determine the actual difference with the

resonant pulser, both the switch size and the maximum current through the inductor must be optimized for each configuration.

First, this optimization was performed for the resonant pulser circuit, using the inductor as in the resonant pulser project. The results are shown in Figure 2.11 and Figure 2.12.

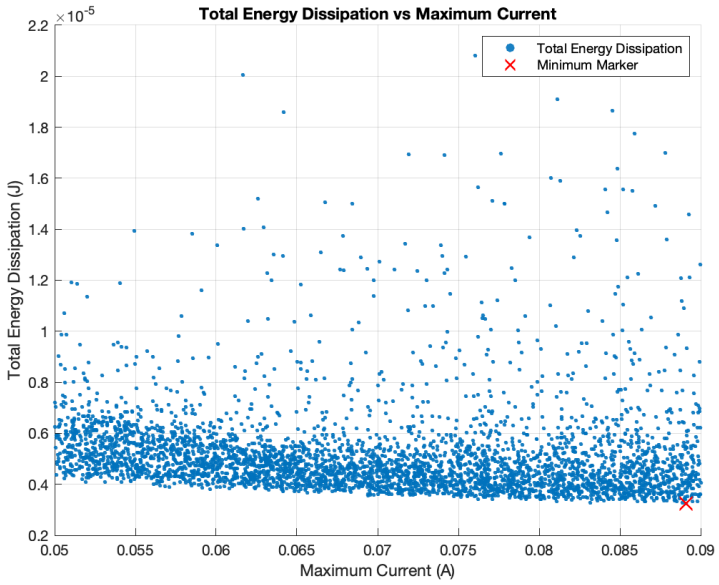


Figure 2.11: Energy loss versus maximum current for the resonant pulser inductor size

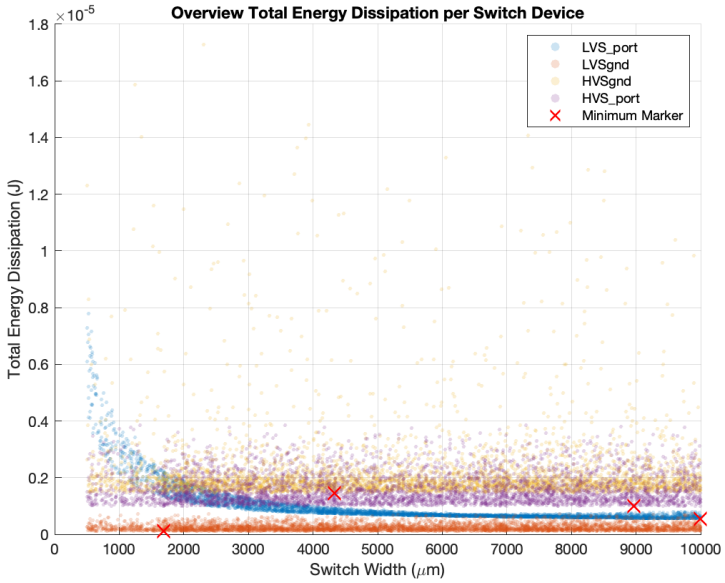


Figure 2.12: Switch sizes versus energy loss for the resonant pulser inductor size

Next, the same optimization was performed for the conventional pulser with a 1000μH inductor. For this, a commercially available inductor was selected: the B82472P6105M0000 from TDK [20], with a physical size of 7.3 mm × 7.3 mm × 4.5 mm, an inductance of 1000μH, a series resistance of approximately 3.85 Ω, and a Q-factor of 22 at 14.6 kHz. The maximum Q-factor for this inductor is 78 at 200 kHz, which suggests it may not be fully optimal for this application. If future results show that the energy

savings for a larger inductor are less than expected, further investigation into alternative inductors may be warranted.

The results for the conventional pulser are shown in Figure 2.13 and Figure 2.14.

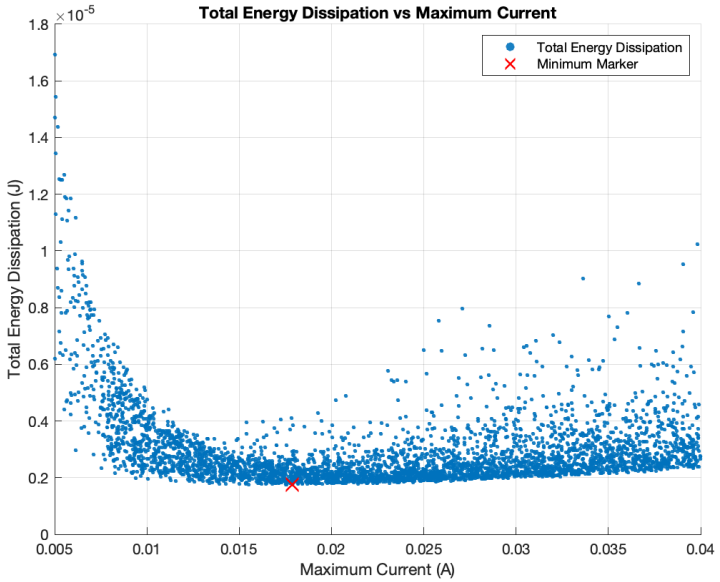


Figure 2.13: Energy loss versus maximum current for the conventional pulser inductor size

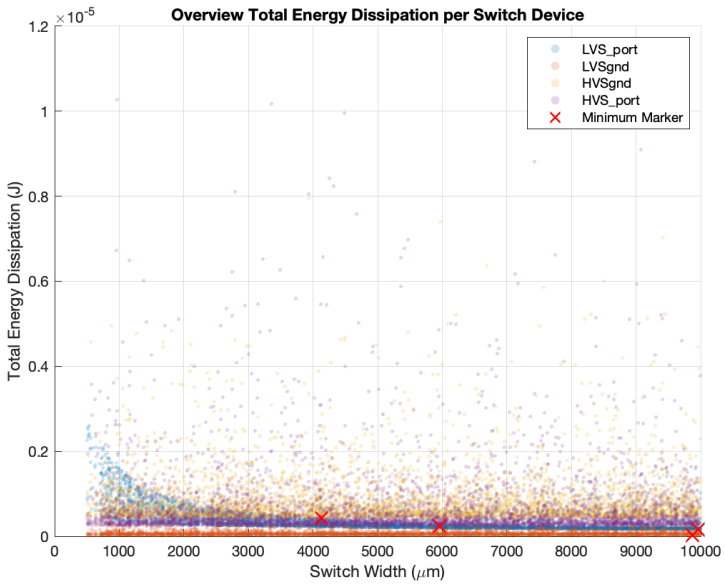


Figure 2.14: Switch sizes versus energy loss for the conventional pulser inductor size

For both optimizations, the best results based on minimal energy losses are summarized in Table 2.7. This table shows that, even with a higher inductor resistance, the power converter with a large inductor still consumes 54% less energy than the converter with a small inductor. Notably, by optimizing the switches, the converter with the small inductor now consumes 27% less energy than in the previous simulation in Section 2.5.1. The simulation also shows that the optimal current shifts to a higher value, mainly due to the larger gate switches that are selected. Apparently, these were far from optimal in the

previous simulation, resulting in significant resistive losses. By reducing the resistance, higher currents are allowed in the circuit, and the switches need to operate less frequently.

Inductor		**Switch Size [μm]**				**I_{max} [mA]**	**Energy [μ J]**	**2x Energy [μ J]**
L [μH]	R_L [Ω]	LVS	LVSgnd	HVSgnd	HVS			
27	0.085	9639.9	3833.9	8710.1	3816	89	3.24	6.48
1000	3.85	7865.3	1743.1	5543.8	1963.2	18	1.75	3.50

Table 2.7: Overview of simulation results for different inductor and switch configurations

2.5.2. Resonant Pulser Simulations

This section describes the simulations performed to analyze the resonant pulser. The focus is on finding the optimal parameters to ultimately compare the energy consumption with the conventional pulser configuration.

In this configuration, the inductor size depends on the transducer capacitance and operating frequency, as shown in Equation 2.29. An inductance of 27 μH with a series resistance of 0.085 Ω is used in this simulation, matching the values used in the resonant pulser project [4]. In this circuit, there is no optimal current value, since the inductor must be charged in a single step to deliver the required pulse voltage.

$$f_{res} = \frac{1}{2\pi\sqrt{LC_{tx}}} \Rightarrow L = \frac{1}{(2\pi f_{res})^2 C_{tx}} = 31.8\mu \rightarrow \approx 27\mu H \tag{2.29}$$

The inductor for the RP was deliberately chosen larger to tolerate ±20% variations in L and other capacitive parasitics while keeping $f_0 = f_{res}$ accurate. With a larger L, even in the worst case (both L and C +20%), there remains sufficient margin for frequency calibration to reliably generate the 2.6 MHz pulse. Although this slightly reduces efficiency, it ensures stable, power-efficient calibration that does not drift over time [4].

Unlike the conventional pulser, the resonant pulser does not require a back-to-back switch at the output port. This is because the energy is always resonated back to create a complete pulse, so there is no need to isolate a high voltage at the output from the internal circuit. However, the switch must still withstand up to 65 V, as it is connected to the same node as the switch used to charge the bias capacitor. Therefore, the switches in the resonant pulser are configured as shown in Table 2.8.

Switch Name	**Device Type**
LVSgnd	nch_5_switch_low_ron_mac
LVS	pch_5_switch_low_ron_mac
HVSgnd	nld65_g5b_mac
HVS	nld65_g5b_mac

Table 2.8: Switch configuration for the resonant pulser power converter

The following aspects are investigated with a focus on energy efficiency:

1. The optimal switch values for the resonant pulser to minimize energy consumption.
2. The expected energy consumption with individually optimized switch sizes.
3. With these optimal switch sizes, the energy consumption for different pulse counts.

A Monte Carlo simulation was performed to find the optimal switch values. The individual switch sizes were randomly chosen within the range of 0.18 to 10,000 μm. The results of this simulation are shown in Figure 2.15, where the individual switch sizes are plotted against the total energy consumption. The total energy loss in the switches is the sum of gate losses and conduction losses. If an optimum is found within the range, this indicates a global minimum, where resistive and switching losses are balanced.

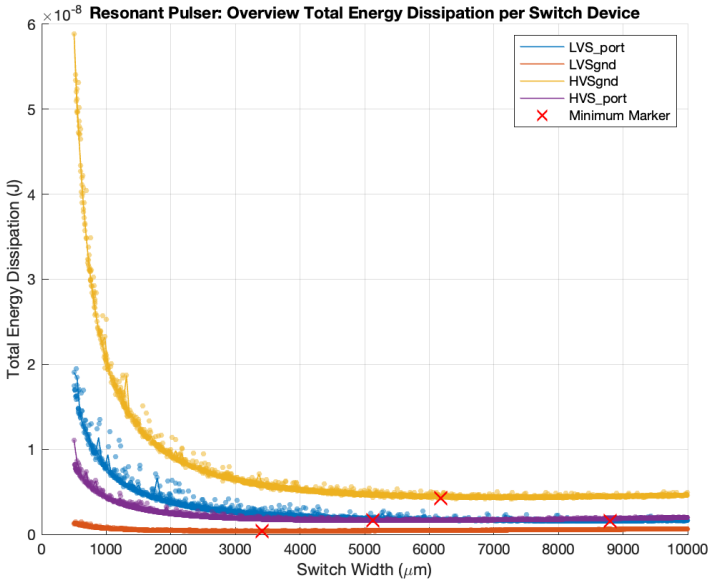


Figure 2.15: Energy loss versus pulse count for the resonant pulser

From this simulation, the configuration with the minimum energy loss was selected, with values shown in Table 2.9. The resulting energy consumption is 8.10 nJ per pulse, or, when scaled to CV^2, a dissipation of 0.08 $C_{tx}V^2_{pulse}$.

LVS [μm]	**LVSgnd [μm]**	**HVSgnd [μm]**	**HVS [μm]**	**Energy [nJ]**
8606.8	3390.5	7577.2	5194.2	8.10

Table 2.9: Optimale switchwaardes en energieverbruik voor de resonante pulser

Next, with these optimal switch values, the energy consumption was investigated for different pulse counts. As expected, this results in a linear relationship. The results are shown in Figure 2.16, which confirms that the energy consumption increases linearly with the number of pulses, as each pulse consumes the same amount of energy.

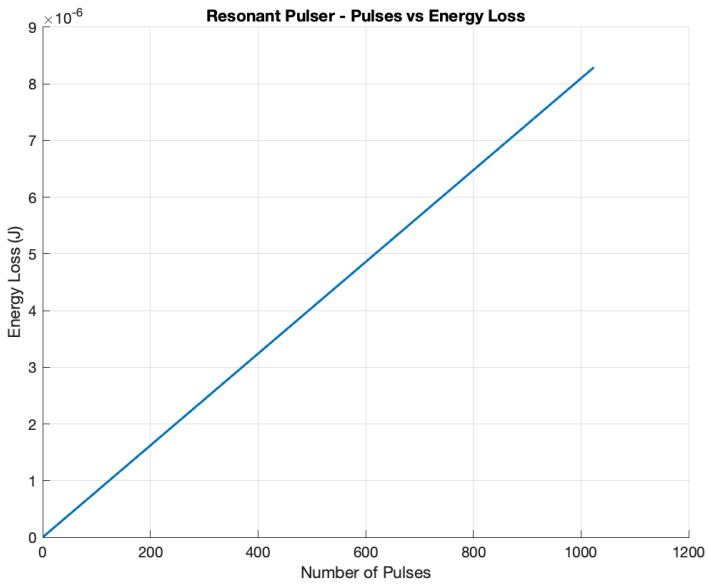


Figure 2.16: Energy loss versus pulse count for the resonant pulser

2.5.3. Conventional Pulser Simulations

This section describes the simulations performed to analyze the power converter in combination with a conventional pulser. In these simulations, the high-voltage capacitor is first charged, after which the pulser is activated, and finally, the remaining energy on the high-voltage capacitor is recovered. The focus is on finding the optimal parameters to ultimately compare the energy consumption with the resonant pulser configuration.

In this configuration, the inductor size can be freely chosen. As shown in the previous section, a larger inductor leads to lower energy consumption. Therefore, a 1000 μH inductor with a series resistance of 0.085 Ω is used in these simulations, matching the values used in the resonant pulser simulations. This ensures that the inductor resistance does not influence the comparison between both pulser configurations. It should be noted, however, that a 1000 μH inductor with the same resistance will be physically larger than a 27 μH inductor, which is an important consideration for the final inductor selection.

In this circuit, a back-to-back switch is required at the output port to isolate the high voltage from the internal circuit. Therefore, the switches in the conventional pulser are configured as shown in Table 2.10.

Switch Name	Device Type
LVSgnd	nch_5_switch_low_ron_mac
LVS	pch_5_switch_low_ron_mac
HVSgnd	nld65_g5b_mac
HVS	nld65_g5b_mac_BB

Table 2.10: Switch configuration for the conventional pulser power converter

The following aspects were investigated with the focus on energy efficiency:

1. The optimal switch values for the conventional pulser to minimize energy consumption.
2. The expected energy consumption with individually optimized switch sizes.
3. With these optimal switch sizes, the energy consumption for different pulse counts.

Again, a Monte Carlo simulation was performed to find the optimal switch values. Here, the individual switch sizes were randomly chosen within the range of 0.18 to 10,000 μm. The results of this simulation are shown in Figure 2.17, where the individual switch sizes are plotted against the total energy

consumption. The total energy loss in the switches is the sum of gate losses and conduction losses. If an optimum is found within the range, this indicates a global minimum, where resistive and switching losses are balanced.

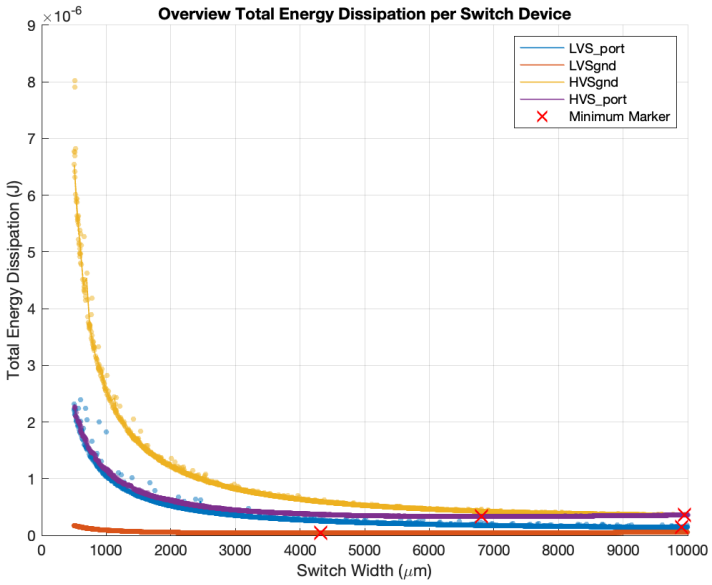


Figure 2.17: Energy loss versus pulse count for the conventional pulser

From this simulation, the configuration with the minimum energy loss was selected, with values shown in Table 2.11. The resulting energy consumption is 999.91 nJ per pulse, or, when scaled to CV^2, a dissipation of 9.35 $C_{tx}V^2_{\text{pulse}}$. Comparing this to the resonant pulser, which dissipates 0.08 $C_{tx}V^2_{\text{pulse}}$, the conventional pulser consumes significantly more energy per single pulse.

LVS [μm]	LVSgnd [μm]	HVSgnd [μm]	HVS [μm]	Energy [nJ]
9178.7	4814.2	9928.5	6346.6	999.91

Table 2.11: Optimal switch sizes and energy consumption for the conventional pulser

Next, with these optimal switch values, the energy consumption was investigated for different pulse counts. Since this configuration must charge and discharge the supply capacitor for each pulse acquisition, it is expected that the energy consumption per pulse will converge towards CV^2. The results are shown in Figure 2.18.

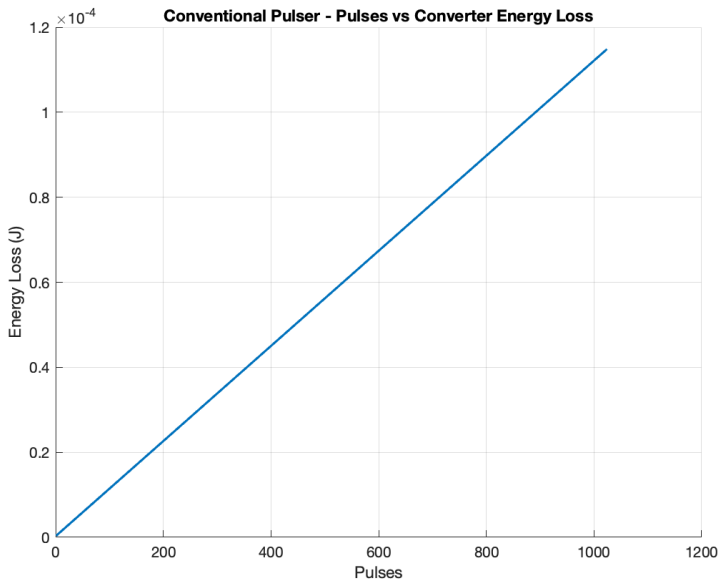


Figure 2.18: Energy loss versus pulse count for the conventional pulser

2.5.4. Final results: break-even analysis

Extensive simulations have been performed to analyze and optimize the power converters for both the resonant pulser and the conventional pulser architectures, each with their respective inductor sizes. One limitation of the current simulation approach is the assumption that all energy stored in the output capacitance can always be recycled. In practice, this is not always the case, especially for a single biasing capacitor which high voltage is isolated by a diode. However, since the biasing capacitances are equal for both configurations, the energy remaining on the capacitor itself will be the same and does not affect the comparison of which configuration is more efficient. A rough estimation is that, instead of all energy being dissipated, only half of the energy is lost when charging the second bias capacitor. This scenario has also been included in the simulations.

Figures 2.19,2.20 and 2.21 show three scenarios: (1) when charging and recycling a single bias capacitor up to 60V, (2) when charging and recycling two bias capacitors up to 60V (factor 2), and (3) when charging two bias capacitors and only recycling the second bias capacitor (factor 1.5). The corresponding break-even pulse counts are approximately 12 for factor 1, 19 for factor 1.5, and 26 for factor 2.

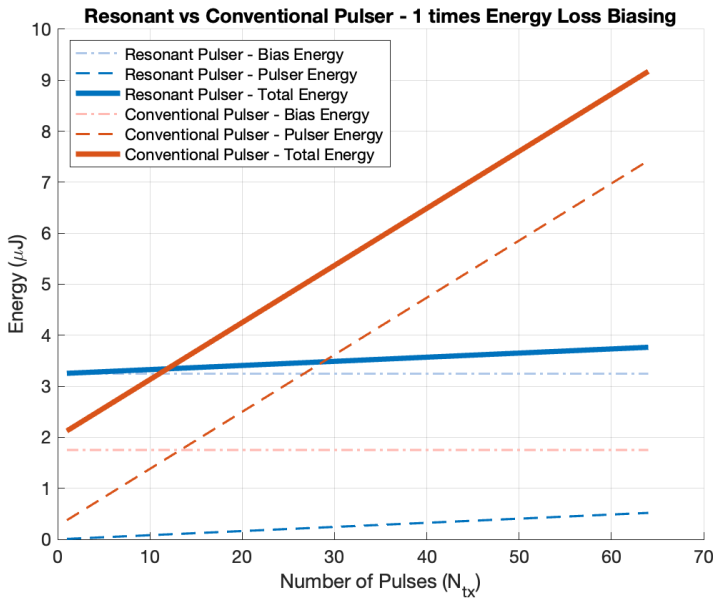


Figure 2.19: Break even: full recycle of one bias capacity, and full charge/discharge of the second bias capacity

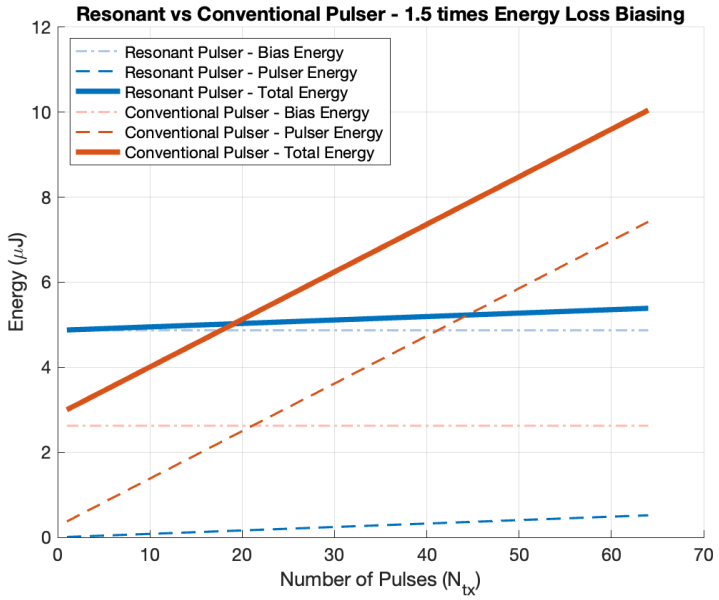


Figure 2.20: Break even: full recycle of one bias capacity, and half charge/discharge of the second bias capacity

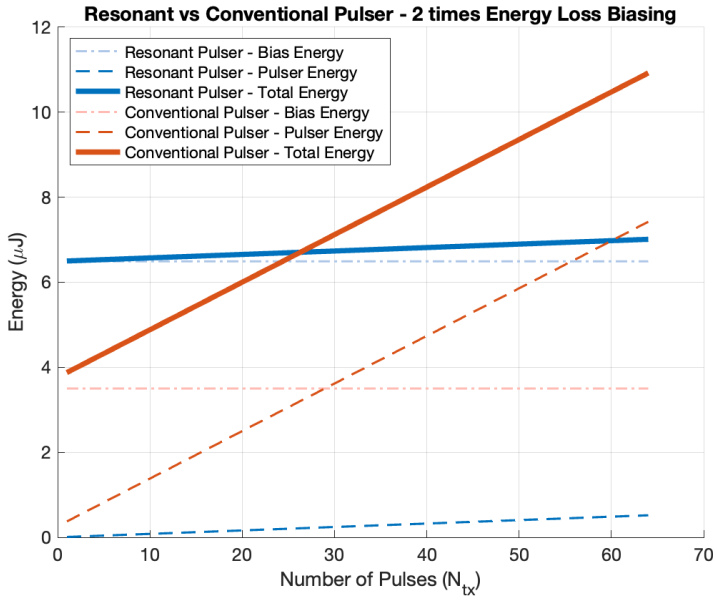


Figure 2.21: Break even: full recycle of both bias capacities

These results indicate that for a low number of pulses, the conventional pulser configuration is the most energy-efficient. However, as the number of pulses increases and more energy can be recycled, the resonant pulser becomes more efficient. When full energy recycling is possible for both bias capacitors, the break-even point is reached at around 26 pulses. Therefore, when selecting between the two architectures, it is important to consider the expected number of pulses per acquisition. For applications with a low pulse count, as assumed for US wearables, the conventional pulser is generally more energy efficient.

In summary, the final architecture is determined by carefully balancing energy efficiency, component size, and practical implementation constraints. The simulation results show that selecting a larger inductor with low series resistance significantly reduces energy losses, but this comes at the cost of increased physical size, which may not always be feasible for wearable applications. Additionally, optimizing the switch sizes and maximum allowed system current further improves efficiency for both the bias circuit and the pulser. Ultimately, the optimal configuration depends on the specific requirements of the application, such as available space, desired pulse count, and acceptable energy consumption.

Interestingly, the required number of pulses for this project, which is around 20 pulses per acquisition, is very close to the break-even point between both architectures. This means that, in theory, either the resonant or the conventional pulser could be suitable. However, due to the higher system complexity and limited pulsing capabilities of the resonant pulser, the conventional pulser is ultimately selected as the optimal solution for this application. This choice offers similar energy efficiency at the relevant pulse count, while providing greater flexibility and a simpler implementation. Moreover, the conventional pulser allows for advanced pulsing techniques that can improve the signal-to-noise ratio (SNR), which is advantageous for the total energy efficiency. These findings provide a solid foundation for the design and implementation of efficient power converters in future ultrasound wearable devices.

2.5.5. Impact of other design variables on 4-switch power converter

In this part the focus lays on:

1. The influence of output capacitance
2. The impact of varying output voltage

Simple parameter sweeps are performed to illustrate the energy consumption versus switch size and maximum current. These results are shown in figures 2.22 and 2.23. The optimal switch size and

maximum current are indicated with red markers at the minimum of the curves.

When all switch sizes are generalized and set to the same value, the optimal switch size is found at 10000μm. It can be observed that from 3000μm onwards, the energy consumption does not change significantly as long as a suitable inductor or current is chosen. To save area or to avoid unnecessarily large parasitic capacitances around the switches, switch sizes starting from 3000μm could also be good options. In table 2.6, the optimal switch sizes for different inductor values are summarized.

The optimal maximum current is found to be approximately 40mA, although this value strongly depend on the final inductor and switch values.

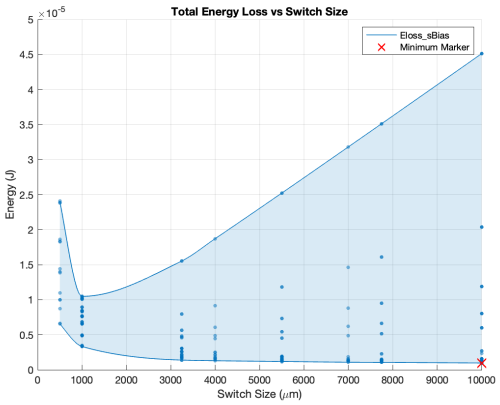


Figure 2.22: Bias Configuration - switch size and corresponding energy

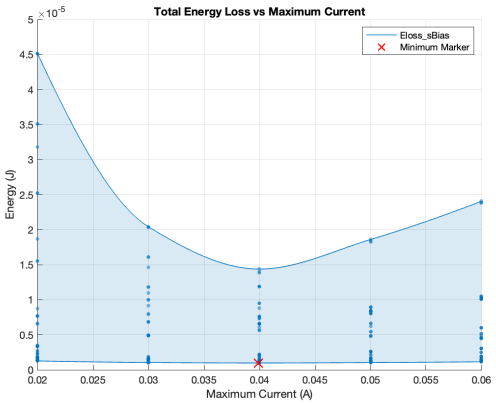


Figure 2.23: Bias Configuration - maximum current and corresponding energy

Output Capacitance Influence

This simulation investigates how the size of the output capacitance affects the performance of the bias circuit. Various capacitance values are simulated to analyze their impact on energy consumption and efficiency. The inductor size is set on 1000μH.

The simulations were performed for capacitance values corresponding to a single element, 50 elements, 100 elements, and 200 elements. In the meantime the switch sizes and current through the system are optimized. From section 2.1, it is known that the energy stored on a capacitor is linearly dependent on the capacitance value. This agrees with the results shown in figure 2.24, where the energy loss increases linearly with increasing output capacitance.

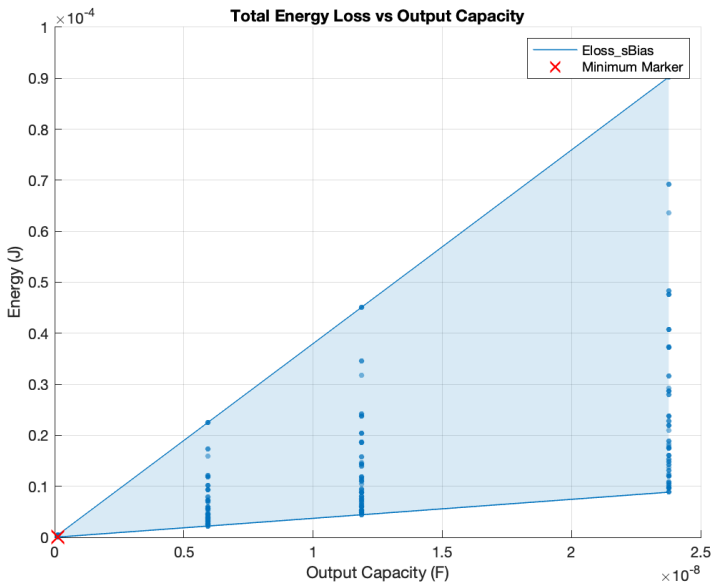


Figure 2.24: Bias Configuration - Varying Output Capacitance and corresponding energy loss

Output Voltage Variation

In this simulation, the effect of varying the output voltage is studied. The bias circuit is simulated for different output voltage levels to observe changes in energy usage and overall system behavior. The inductor size is set on 1000μH.

The simulations were performed for output voltage ranges from 15V up to 120V while optimizing the switch sizes and current through the system. From section 2.1, it is known that the energy stored on a capacitor is quadraticaly dependent on the voltage across. This agrees with the results shown in figure 2.25, where the energy loss increases linearly with increasing output capacitance.

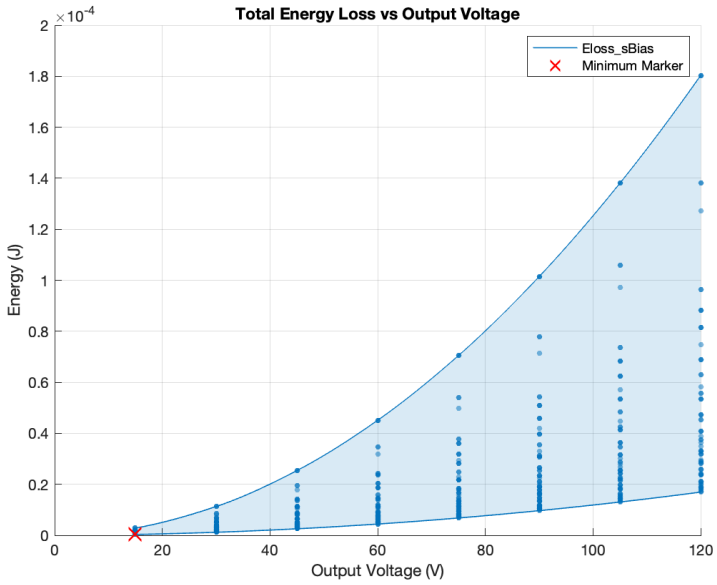


Figure 2.25: Bias Configuration - Varying Output Voltage and corresponding energy loss

2.6. Final Configuration and Detailed Simulation Results

This section presents the final configuration and a detailed overview of the simulation results for the optimized conventional pulser architecture. The main results of the switch and inductor optimization are summarized in Table 2.12. Here, the optimal values for both the biasing and pulser stages are shown, including the selected inductor, series resistance, switch sizes, maximum system current, and resulting energy loss per cycle.

Configuration	**L [μH]**	**RL [Ω]**	**LVS [μm]**	**LVSgnd [μm]**	**HVSgnd [μm]**	**HVS [μm]**
Biasing	1000	3.85	7865.3	1743.1	5543.8	1963.2
Pulser	–	–	9178.7	4814.2	9928.5	6346.6

	I_{max} [mA]	**Energy Loss [μJ]**
Biasing	18	1.75
Pulser	–	1.00

Table 2.12: Overview of optimal switch sizes, inductor values, and energy consumption for both bias circuit and pulser configurations.

For the final implementation, no duplicate switches are used per port in order to save area and reduce circuit complexity. Therefore, fixed switch values have been chosen that represent a compromise between the requirements of both the biasing and pulser stages. Additionally, the system current for the following simulations is set to 30 mA. This value is chosen to ensure that, even with expected parasitic capacitances, there is sufficient energy available to transfer to the output. This parameter can be further optimized in future work.

Table 2.26 lists the key simulation variables and their values for the final configuration, as used in the detailed Matlab simulations. These include supply voltages, capacitor values, inductor and resistance, switch sizes, and the number of pulses per acquisition.

L [μH]	**R_L [Ω]**	**LVS [μm]**	**LVSgnd [μm]**	**HVSgnd [μm]**	**HVS [μm]**
1000	3.85	10000	6000	10000	3000

I_{max} [mA]	**N_{tx}**	**Pulser Mode**	**V_{bat} [V]**	**V_{Cbias} [V]**	**V_{HV} [V]**
30	20	recharge	3.6	65	30

Ctx [pF]	**Cbias1 [pF]**	**Cbias2 [pF]**	**Chv [pF]**
118.8	11880	11880	11880

Figure 2.26: Simulation parameters for the final conventional pulser configuration, split into (top) inductor, resistance, and switch sizes, and (bottom) system and capacitor parameters.

Figure 2.27 shows the full-cycle simulation waveform, including the charge, pulse, and recovery phases. This figure illustrates the voltage and current behavior throughout the entire operation, as well as the pulsing dynamics.

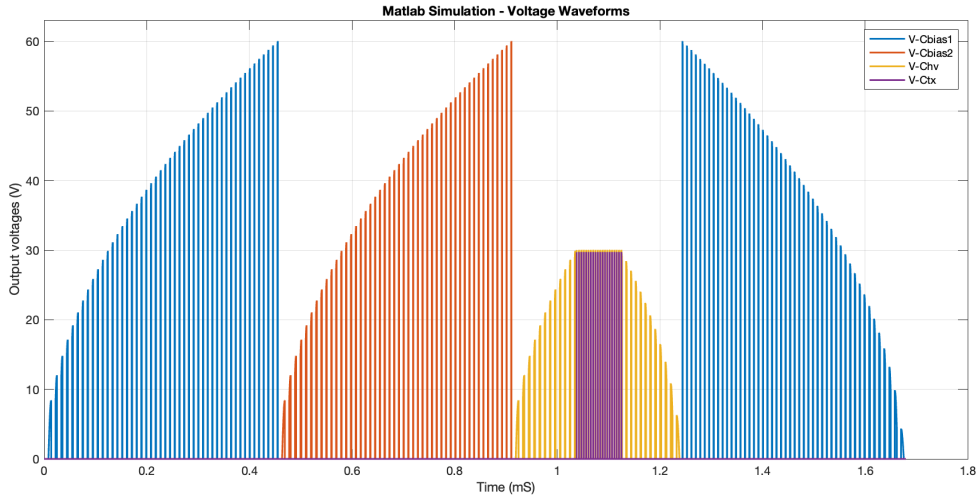


Figure 2.27: Full-cycle simulation waveform for the conventional pulser: charge, pulse, and recovery phases.

The next results provide a detailed breakdown of the energy flows and losses in the system. Table 2.13 summarizes the efficiency of the power converter during each system state, including charging the bias capacitors, pulsing, and recycling. Remarkable is that the efficiency for charging and discharging Chv is lower, likely because the converter is optimized for charging the biasing capacitor up to higher voltages.

System State	Active LVS Port [uJ]	Active HVS Port [uJ]	Gatedriver Energy [uJ]	Efficiency
CBias1 chargeC	22.3	21.4	0.157	0.935
CBias2 chargeC	22.3	21.4	0.157	0.935
CBias2 recycleC	20.6	21.4	0.157	0.936
Chv chargeC	5.61	5.35	0.0426	0.859
Chv recycleC	5.02	5.25	0.0393	0.855
Pulsing pulseCP	0	2.11	0.00354	0
Pulsing rechargeC	2.05	2.01	0.0622	0.754

Table 2.13: Measured Energy flows with total system efficiency during system presets.

Table 2.14 summarizes the energy supplied by the battery and 5V gatedrivers to each major process in the cycle. The largest contributions are from charging the bias capacitors, as expected.

System State	Supply Battery [uJ]	Supply 5V - Gatedrivers [uJ]
CBias1 chargeC	22.3	0.157
CBias2 chargeC	22.3	0.157
CBias2 recycleC	0	0.157
Chv chargeC	5.61	0.0426
Chv recycleC	0	0.0393
Pulsing pulseCP	0	0.00354
Pulsing rechargeC	2.05	0.0622
Total	52.26	0.61864

Table 2.14: Energy supplied by the battery and 5V gatedrivers to each process.

Tables 2.15 and 2.16 provides a comprehensive energy breakdown, including resistive and gatedriver losses, trapped charge, pulser losses, recycled energy, and other minor contributions.

Supply Sources	Energy [uJ]
Battery	52.2
Gatedrivers_5V	0.6

Table 2.15: Energy Breakdown Supplies

System Category	Energy [uJ]
Recycled_Energy	25.6
Trapped_Cbias1	21.4
Resistive_Loss	3.1
Pulser_Loss	2.1
Gatedriver_Loss	0.6
Others	-0

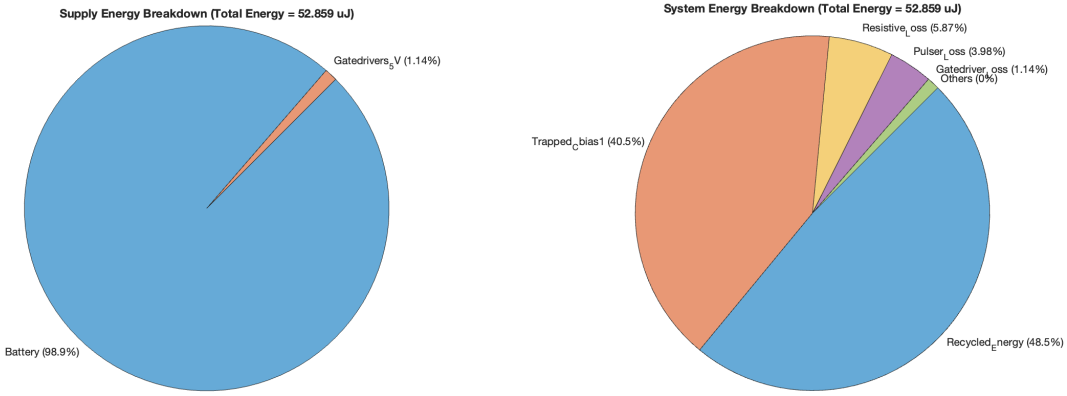
Table 2.16: Energy Breakdown System

The largest loss is due to trapped charge in the bias capacitor, while a significant portion of energy is also successfully recycled. The total energy loss by dissipation is approximated by:

$$E_{loss} \approx \sum E_{supplies} - E_{recycled} - E_{trappedCbias1} = 6.2\mu J \tag{2.30}$$

Which is a bit higher than optimal approximated at $5\mu J$, as indicated in the break-even Figure 2.20. But close enough for a proof of concept, with room for further optimization.

Figure 2.28 visualizes the same data as Table 2.16 in the form of a pie chart, making it easier to see the relative contributions of each loss mechanism.



(a) Supplies energy breakdown

(b) System energy breakdown

Figure 2.28: Pie charts showing the energy breakdown for the full-cycle simulation: (a) supplies, (b) system.

Finally, Table 2.17 summarizes additional statistics from the simulation, such as the number of steps, total time, minimum and maximum step times, and maximum output voltage for each system state. Notably, the charge and recycle phases for the bias capacitors take the most simulation steps and time, while the pulsing phase is extremely fast.

System State	Steps	Total Time (uS)	Min Step Time (uS)	Max Step Time (uS)	Max State Voltage (V)
CBias1 chargeC	96	455.4	0.4998	8.532	60.06
CBias2 chargeC	96	455.4	0.4998	8.532	60.06
CBias2 recycleC	96	435.5	0.5028	8.147	60.06
Chv chargeC	26	127.2	0.3028	8.532	30.02
Chv recycleC	24	118.8	1.03	8.147	29.74
Pulsing pulseCP	40	0.1058	0.002645	0.002645	30.04
Pulsing rechargeC	38	87.12	0.4816	4.277	30.04
Total	416	1679.5258	NaN	NaN	NaN

Table 2.17: Additional simulation statistics for each system state.

In summary, these detailed simulation results confirm the effectiveness of the chosen configuration and provide insight into the energy flows, losses, and timing throughout the full operating cycle of the system.

2.7. Conclusion

A fundamental analysis was first performed to understand the operating principles and energy behavior of both pulser architectures. Based on these insights, a MATLAB simulation was developed to systematically investigate the influence of key design parameters on energy efficiency. The simulation study systematically compared the energy efficiency of the proposed power converter in combination with the conventional pulser (CP) and the resonant pulser (RP) architectures for biasing and pulsing in wearable ultrasound systems. Key design parameters such as inductor size, output capacitance, and switch sizing were varied and optimized for both architectures.

The results show that:

- CP architecture is more energy efficient for low pulse counts (below 12 to 26 pulses per system cycle).
- The RP architecture becomes more efficient at higher pulse counts, due to its ability to recycle energy during each pulse.
- Increasing the inductor size and optimizing switch sizes significantly reduces energy losses.
- optimizing the maximum system current (Imax) is crucial for minimizing losses.
- For the expected use case (~20 pulses per acquisition), both architectures are close in efficiency, but the CP architecture offers greater flexibility and simpler implementation.

For wearable ultrasound systems with low to moderate pulse counts, the conventional class-D pulser architecture is the preferred choice. It combines high energy efficiency with practical advantages such as easier implementation, support for pulse trains, and potential for beamforming. The resonant pulser may become advantageous in future applications requiring very high pulse rates or when CMUT devices do not require biasing anymore.

3

Prototype Design

This chapter provides an overview of the prototype design for the proposed ultrasound wearable system concluded from the architecture study. Firstly , the overall concept of the ultrasound wearable prototype is introduced, this overview shows the top-level system for future designs in ultrasound wearables. This prototype aims to meet the design requirements outlined in introduction chapter ...

Then the top-level architecture is splitted up and elaborated in more detail to a functional prototype design. The goal of this prototype is prove and demonstrate the feasibility of high-voltage supply from low-voltage for US wearables in an energy efficient way. This means that biasing to high-voltage, pulse generation and energy recycling are all included in the prototype.

Finally, the system implementation is described, highlighting its key features and functionalities. Subsequently, a detailed overview of the architecture is presented, which is implemented to circuitlevel in the next chapter.

3.1. Overview of US Wearable System

The proposed ultrasound wearable system consists of several key components, as illustrated in figure 3.1. The system is powered by a low-voltage battery, which supplies energy to the entire system.The low-voltage to high-voltage power converter provides the neccessary high-voltage biasing and pulse voltage. After pulse acquisition, the power converter enables energy recycling from the capacitive outputs back to the low-voltage supply system. In this way the recycled power can be used for data processing or communication, enhancing the overall efficiency of the system.

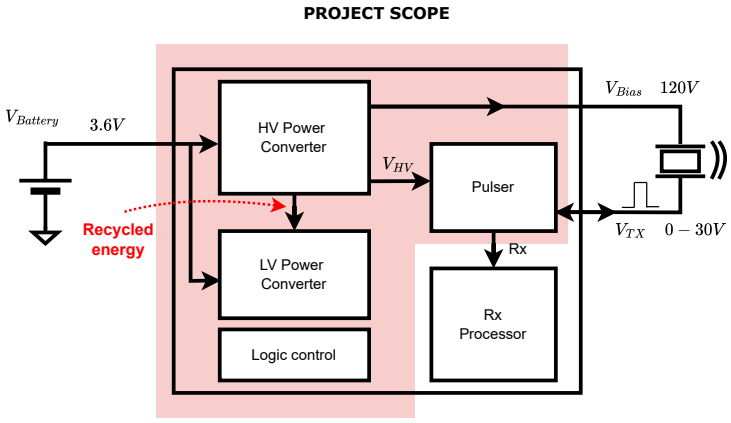


Figure 3.1: Overview of proposed ultrasound wearable system architecture

As illustrated, processing of the received ultrasound signals is included in the system, but excluded from this project. The focus of this work is on the power converter with energy recycling in combination with US pulse generation.

It should be emphasized that the presented architecture serves as the target for future ultrasound wearable systems. To achieve such a system, it is first necessary to demonstrate a method that can efficiently generate high-voltage from a low-voltage supply, while enabling energy recycling. The prototype described in the following sections is therefore an essential step towards realizing the envisioned system architecture introduced above.

3.2. Overview of Prototype

The main objective of the prototype is to demonstrate the feasibility and functionality of the proposed system architecture. In designing the prototype, a clear distinction has been made between components that must be implemented on-chip and those that may remain off-chip. The power converter, class-D pulser, and logic system could be implemented on-chip, while the battery, a single inductor, three capacitors, one diode, and the CMUT transducer are off-chip components. This approach is chosen to minimize the on-chip area required for large capacitors or inductors and to maintain flexibility in design choices for the prototype.

Special attention is given to time-critical functions, which are implemented on-chip to ensure reliable operation. In meantime the same attention holds for off-chip components, for example in cases where connections or systems such as DACs do not meet the required speed, then multiple DACs may be used. Furthermore, practical constraints such as the maximum number of available connections must be considered; a smaller chip area allows for fewer wires and limits the number of external connections, whereas increasing the chip area would result in unnecessary costs. From this perspective, a more detailed overview of the implemented prototype is presented in Figure 3.2.

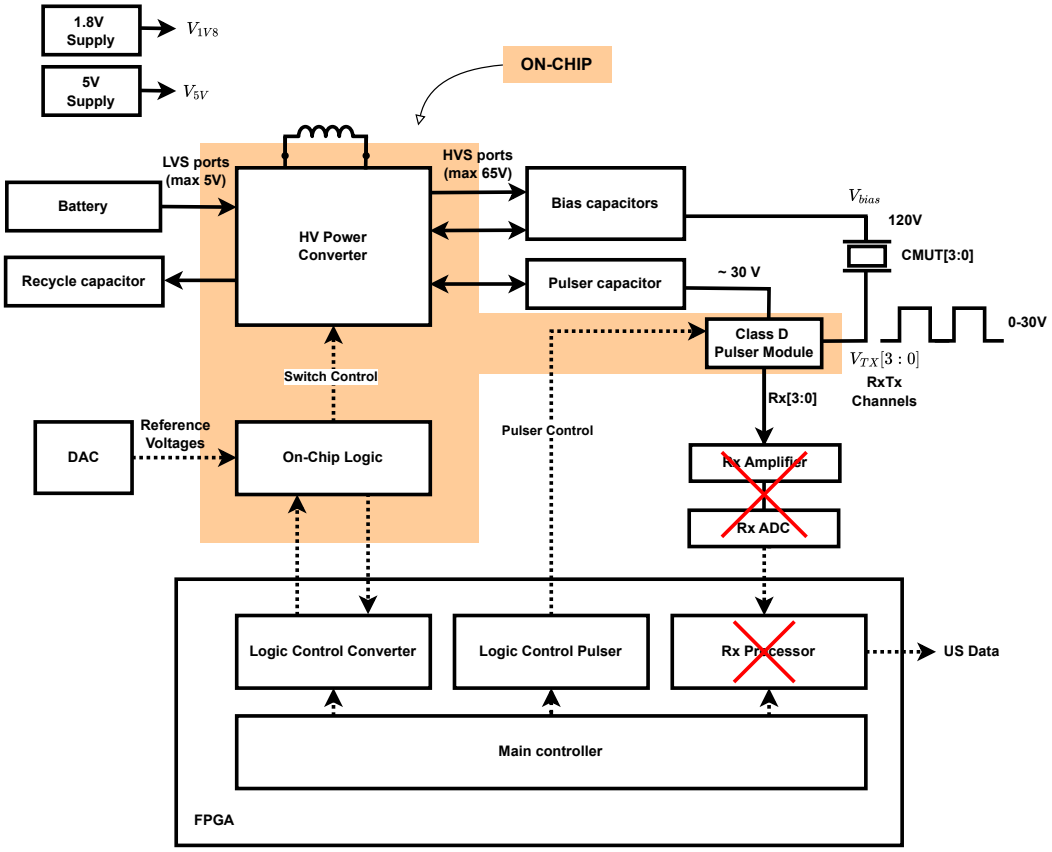


Figure 3.2: Overview of Detailed On-Chip Prototype Implementation

As shown in Figure 3.2, non-time-critical control, low-voltage supplies, and reference voltages are implemented off-chip. In contrast, part of the logic is realized on-chip, while another part remains off-chip. The on-chip implementation is reserved for time-critical functions or those required for safety. For example, this ensures that the prototype is protected against potential damage in case of incorrect switch control.

At the bottom of the figure, the FPGA used to control the prototype is depicted. Within the FPGA, the various submodules are programmed as shown. Driven by the main controller, different preset routines can be executed. During these routines, the main controller coordinates the converter controller, pulser controller, and any additional modules as needed.

In the following subsections the different blocks of the prototype are explained in more detail.

3.3. Power Converter

The power converter is the central element of the prototype, responsible for generating high-voltage bias and pulse voltages from a low-voltage supply. The converter uses a four-switch buck-boost topology, enabling efficient energy transfer and recycling to multiple outputs with only one off-chip inductor. This is essential for wearable applications, where minimizing off-chip components and power consumption is a key requirement.

Both charging and recycling of energy at the output involve the same steps: charging and discharging the inductor. Two control strategies are considered: time-based control and current/voltage level-based control. Time-based control can be estimated using the equations in Section 2.5, but variations in input or output voltage affect the required timing. This can lead to inefficiencies, so current level detection is preferred, as it ensures the inductor is always charged to the correct current regardless of voltage

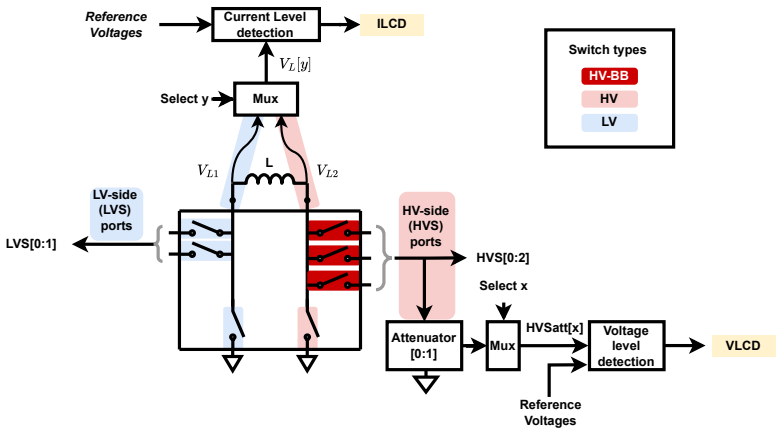


Figure 3.3: Detailed overview of the implemented power converter architecture

variations.

During the discharge phase, the system must switch states when the inductor is fully discharged and so the current reaches zero. Poor timing can result in incomplete discharge or even reverse charging, which impacts energy efficiency. Therefore, accurate current level detection is preferred for discharging.

Compared to resonant pulser architectures [21, 5], this design requires different timing, as the output voltages vary and switching times are not constant. The final architecture, shown in Figure 3.3, includes current and voltage level detection using comparators with reference voltages for both charging and discharging the inductor.

The inductor current can be measured either by the voltage difference across the inductor ($|V_{L2} - V_{L1}|$) or by measuring the voltage at the nodes V_{L1} or V_{L2} , dependent of which switch is active to ground. The second method is preferred, as it avoids the need for differential measurement circuits and additional HV to LV attenuators.

Some important points for level detection at the active switch are:

- The voltage across the switch is determined by its resistance and the current flowing through it. Low on-resistance is chosen to minimize losses, but this also means the voltage is low and can be difficult to measure accurately. The switch resistances are ranges of ohms, the current flow is in range of tenths of milli-amps, resulting in expected measuring voltages in tenths of millivolts.
- During discharge, the voltage across the switch becomes negative, requiring zero-crossing detection from negative to positive. This feelds counter-intuitive behavior, as the voltage is expected to be positive when current flows.

The chosen architecture is shown in Figure 3.3.

3.3.1. Finite State Machine

The corresponding finite state machine (FSM) that controls the states of the power converter is shown in Figure 3.4. Its operation will be explained with an example below.

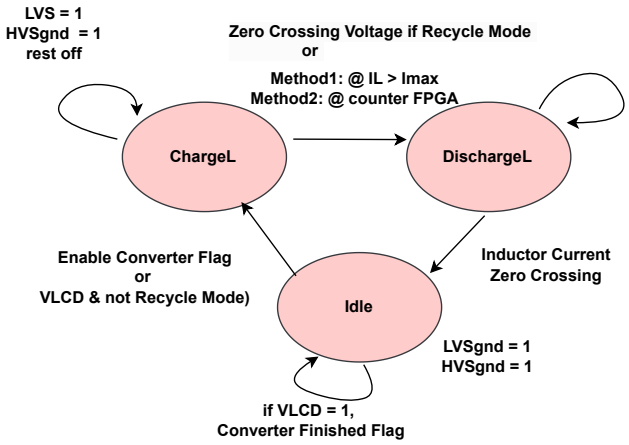


Figure 3.4: FSM for controlling the states of the power converter

The operation can be explained with the following example, where energy is transferred from the low-voltage side (LVS) to the high-voltage side (HVS).

- When charging the inductor, switches LVS and HVSgnd are closed, applying a voltage across the inductor.
- As soon as the voltage at node V_{L2} equals the reference voltage Vref_ILCD (i.e., the inductor current reaches the desired value), the ILCD signal goes high and the inductor charge (chargeL) state is complete.
- Next, the converter transitions to the dischargeL state, closing switches SW_INgnd and SW_OUT to discharge the inductor to discharging the inductor into the high-voltage side. When the voltage at node V_{L1} equals the reference voltage Vref_ILCD_ZC, the set voltage at which the inductor current should be zero, the ILCD signal goes high again and the converter cycle is finished.
- The controller then decides whether to start a new cycle or not, based on the output voltage V_HVS.
- For energy recycling, the principle is the same, but during HV output discharge, and during charging the inductor, the zero-crossing of the output voltage must be used as a trigger to move to the next (dischargeL) state.

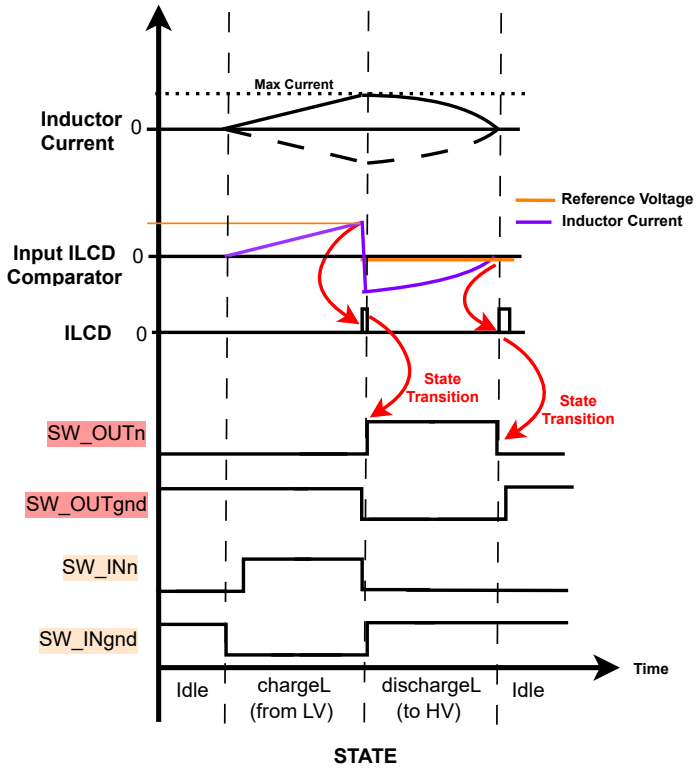


Figure 3.5: Logic schematic for the power converter

3.4. Floating Level-Shift Gate Driver

The design of the floating level-shift gate driver posed one of the major challenges in this project. The complexity comes from the behavior of the intermediate node V_{L2} and the output node. Both nodes can reach high voltages, up to 65V.

It is important to note that MOSFET switches inherently contain bulk (body) diodes. Since both nodes connected by the switch can reach high voltages, a single switch would allow current to flow through the body diode when one node is at a higher potential than the other. To prevent unintended conduction via these body diodes, the switch must be implemented as a back-to-back configuration, where two MOSFETs are connected with their sources tied together. This arrangement ensures that neither body diode can conduct, regardless of the voltage difference between the nodes. Figure 3.6 illustrates this back-to-back switch configuration.

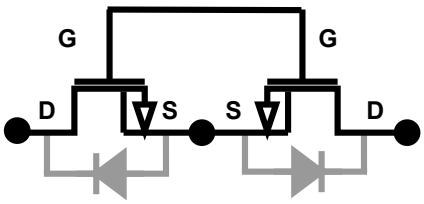


Figure 3.6: Back-to-back MOSFET switch configuration with sources connected

There are several difficulties to overcome. In order to switch on the device, a voltage difference of $V_{GS} = 5V$ is required. However, the source node co-moves with the output voltage or the V_{L2} node. This implies that the gate voltage must track the source node accordingly. Another challenge is to return V_{GS} back to 0 V when the source node is at its maximum voltage. A further issue arises when the source node must be pulled to ground earlier than V_{L2}. Otherwise, substrate currents will flow from source to drain through the body diode, causing unexpected circuit behavior.

Multiple approaches are presented in the literature to address these issues. Some level shifters have comparable situations but assume the existence of a fixed high-voltage supply for the gate driver [14], [22], [23]. In our case, however, the design aims at an energy-efficient high-voltage supply that recycles capacitive energy. Therefore, providing an additional dedicated high-voltage supply for the gate driver is undesirable.

An alternative solution is the use of a bootstrap capacitor to create the required 5 V differential voltage [5], [24], [22]. Initially, the bootstrap capacitor (also called flying or floating capacitor) is charged to 5 V. After switching, it floats with the source node. By means of a capacitively coupled latch circuit between logic and gate driver, the gate can then be toggled even when the system is isolated at high voltage. A disadvantage of this approach is that the energy stored in the bootstrap capacitor cannot be recycled, which introduces losses. Moreover, leakage currents may prevent the gate voltage from reaching the required 5 V [22]. This increases switch resistance and thereby raises resistive energy losses.

In this work, the floating level-shift gate driver proposed in [5] is implemented. To pull the intermediate node of the back-to-back configuration to ground, a high-voltage switch is added between the sources and ground which enables to pull the floating ground to zero. This ensures that the back-to-back switches can bi-directionally isolate V_{L2} and the output node V_{HVS} without risk of substrate currents. Figures 3.7 and 3.8 illustrate the switching scheme of the floating ground node. After the floating switch is turned of, the floating ground (FGDN) is pulled to ground, whereafter V_{L2} must can pulled down safely.

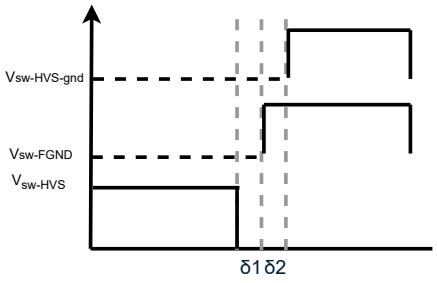


Figure 3.7: Switching illustration of the floating ground node

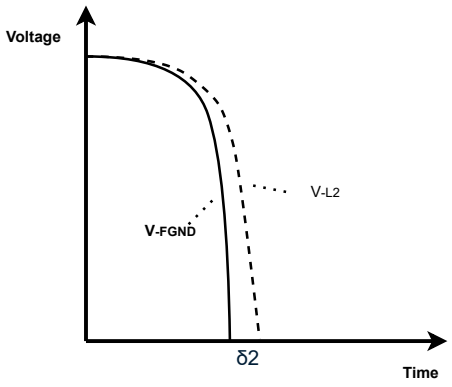


Figure 3.8: Switching scheme of the floating ground node

The floating driver is powered by a bootstrap capacitor, which is tied to the source node of both switches. This node is later denoted as the floating ground (FGDN). Figure 3.9 shows the complete schematic. For orientation, the bootstrap capacitor C_{BST} is highlighted in red. The HV switches are shown at the bottom left and bottom right, consistent with Figure 3.10.

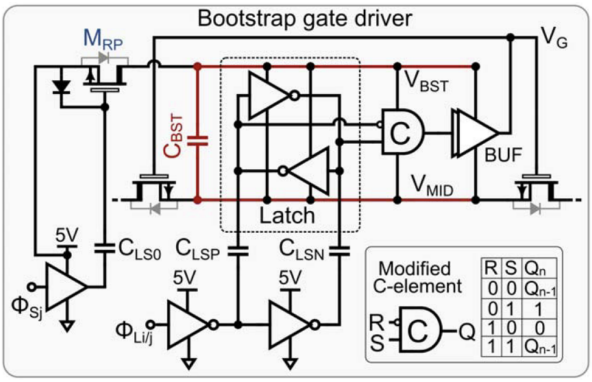


Figure 3.9: Bootstrap Supply with floating levelshift Gate Driver Circuit [5]

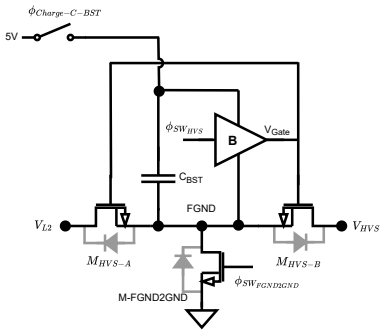


Figure 3.10: Bootstrap supply for floating gate driver [5]

The subsystem to the left of the bootstrap capacitor, controlled by S_j, is responsible for charging C_{BST}. Each time the floating ground node is returned to ground, the capacitor is recharged to 5 V. The input of the latch is capacitively coupled to the underlying logic level shifter and inverter, driven by $L_{i/j}$. When the logic input changes, a positive or negative current is injected through the capacitors into the latch input. This mechanism effectively generates the R and S signals for a modified C-element, allowing level shifting from 1.8 V to 5 V and then to the (variable) high voltage. The C-element ensures that the latch holds its state even when both inputs toggle simultaneously. The latch output finally drives the HV switch gate.

The bootstrap capacitor is sized at 716 pF, which results in a voltage drop of 0.2V and so drive voltage of 4.8 V. This leads to an increase in R_{on} of approximately 10% is expected by simulations.

3.4.1. On-Chip Logic

The on-chip logic is responsible for the time-critical functions of the power converter, ensuring safe and reliable operation. It includes the finite state machine (FSM) that controls the power converter states, as well as safety features to prevent damage from incorrect switch control.

As may have been noticed, the ground and port switches on each side toggle, alternating with each other. These switches must never be activated simultaneously, as this would create a short circuit. Therefore, the internal logic is designed to control the switches on each side with a single signal: SW_LVS and SW_HVS. When this signal is high, the port switch is activated; when low, the ground switch is activated. This design ensures that both switches on one side can never be turned on at the same time.

From this perspective, the surrounding logic has also been implemented. The correct control of the switches depends on whether power needs to be transferred from left to right or vice versa. Since the 4-switch topology is fully symmetrical, the same logic can be used for both directions, and the signal

from the FSM only needs to be inverted. Finally, the control signals must be correctly routed to the appropriate input and output switches.

To further ensure safe operation and prevent short circuits between the port and ground switches, a non-overlapping clock circuit has been implemented. This circuit introduces a delay between switching events, guaranteeing that the active switch is fully turned off before the next switch is activated. The delay of the non-overlapping clock must be sufficiently large to avoid any overlap, which could otherwise result in a direct short from port to ground.

This functional description is ultimately implemented by the logic shown in Figure 3.11.

Finally, dedicated signals are included to reset the output attenuators during system initialization, and to switch the floating ground of the level shifters to ground when required. These features are essential for proper startup and safe operation of the prototype.

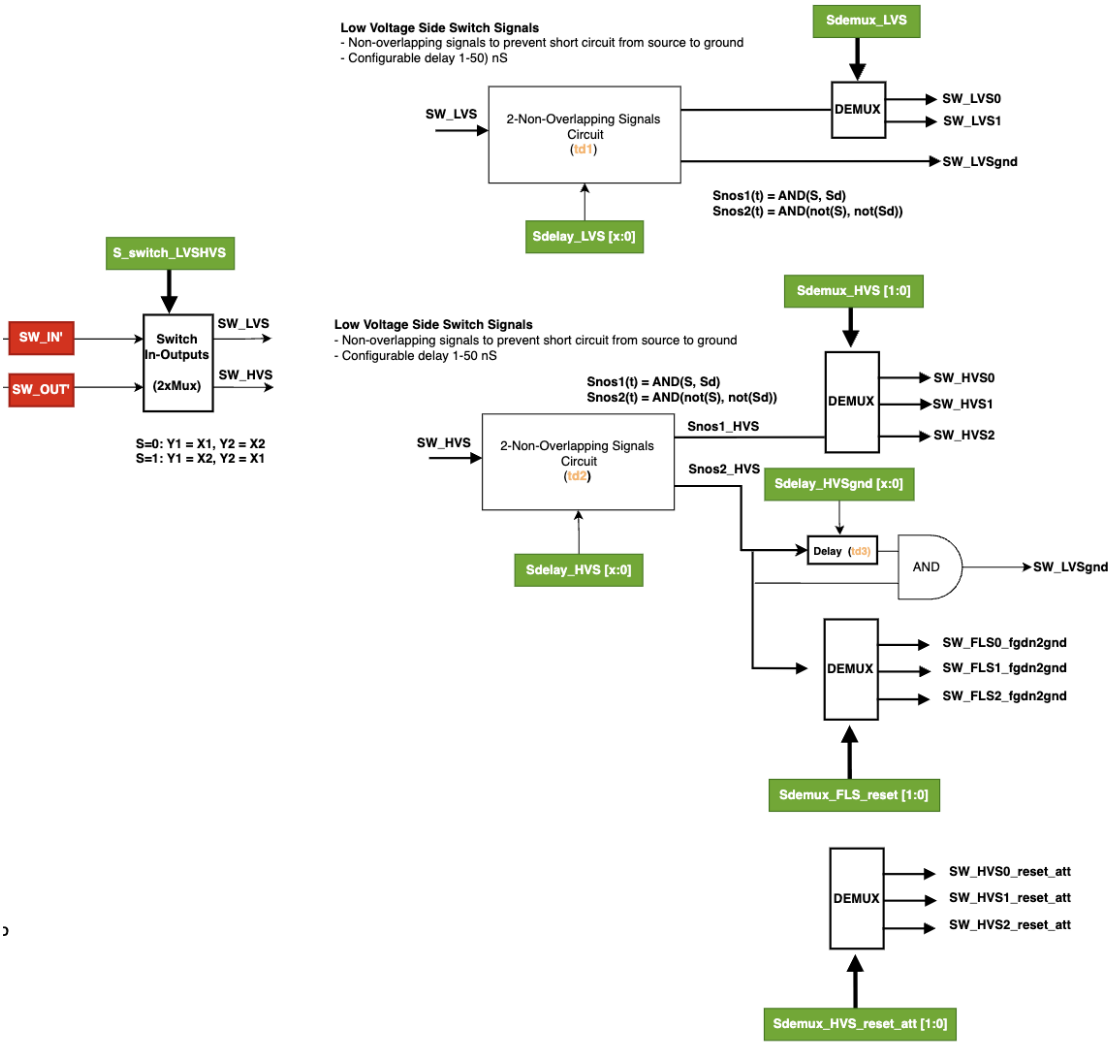


Figure 3.11: On-chip logic control for the power converter

The FSM and logic also take into account time-critical and non-time-critical signals. Non-time-critical signals can be controlled by a shift register during a logic control or idle state of the controller. This approach helps to minimize the number of wires required.

Another feature enabled by this implementation is an auto-switch circuit that can be implemented. This circuit can be inserted between the SW signal from FSM and the on-chip logic control. It consist of a

simple truthtable that can be set to automatically toggle the SW signal or port and ground switches based on the ILCD and VLCD signals. This feature allows for low clock frequencies or even the use of power-saving modes for the controller during operation. This can provide advantages for future designs of the US wearable system by saving energy. While this system is invented, it is not used for the current design or prototype.

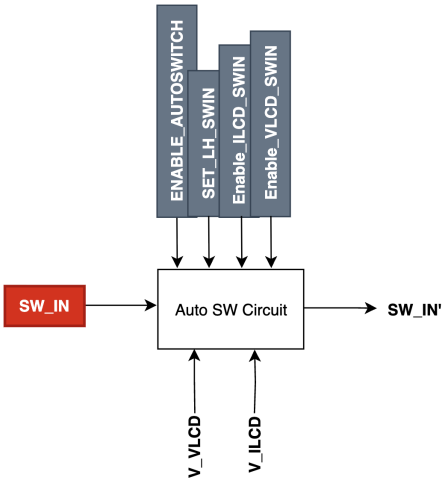


Figure 3.12: On-chip logic with auto-switch feature for the power converter

3.5. Current Level Detection

The system level illustration of the current level detection circuit (ILCD) is shown in Figure 3.13. The ILCD circuit measures the voltage at node V_{L2} or V_{L1}, depending on which switch is active to ground. This voltage is then compared to a reference voltage (Vref_ILCD) using a comparator. When the measured voltage exceeds the reference voltage, the ILCD output signal goes high, indicating that the inductor current has reached the desired level.

The comparator is implemented using a folded cascode with a common-source stage architecture. To ensure correct operation for input ranges near zero, a PMOS input pair is chosen. For accurate zero-crossing calibration and to avoid the need for negative reference voltages, the comparator is designed with an offset of 50 mV. This means the reference voltage must be set 50 mV higher than the desired voltage level. This approach enables proper calibration in both directions around zero.

While the measured voltages are always low, it is important to note that the analog multiplexer is connected to both high-voltage and low-voltage nodes. This requires different switch types and makes the charge-injection behavior of the multiplexer more complex. Charge injection from the analog multiplexer can cause significant voltage spikes at the input of the comparator, which may lead to false triggering. To mitigate this issue, a transition detection circuit is implemented that activates a small pull-up switch at the input of the comparator. This pull-up switch holds the input voltage high, preventing false triggering during transitions.

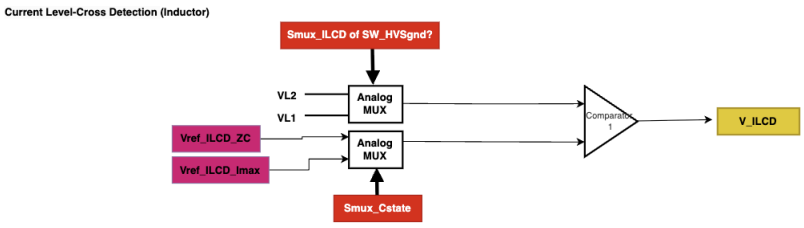


Figure 3.13: Current Level Detection Circuit

3.6. Voltage Level Detection

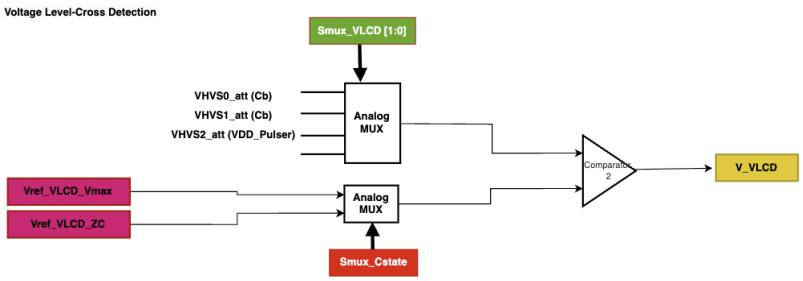


Figure 3.14: Voltage Level Detection Circuit

3.7. Class-D Pulser

The Class-D pulser is responsible for generating the high-voltage pulses required to drive the CMUT transducer. In this prototype, a Xiver CM5 CMUT transducer is used, which features the same type of CMUT drums as described in [9].

To demonstrate the new architecture, an existing Class-D pulser module was reused. However, there is a key difference in the transducer configuration: while [9] describes the actuation of a single CMUT element in 2D, this project drives a 1D array with X drum elements per channel. As a result, the pulser must be able to handle a load that is X times larger. To achieve the desired frequency of 2.6 MHz, it was only necessary to scale the pulser drivers accordingly.

3.7.1. Pulser Core

The operation of the pulser is based on the design developed in [14], with the basic core shown in Figure 3.15. The high-voltage supply (VDDHV) is directly provided from C_{HV}. The T/R signal sets the pulser in either transmit or receive mode. In transmit mode (T/R = high), HVp and HVn are used to generate a high or low signal at the output. This principle was also explained earlier in Section 2.3.3. By disabling the T/R switch and enabling HVn, the CMUT signal is routed to the receiver. If the receive mode is disabled, the output remains at zero.

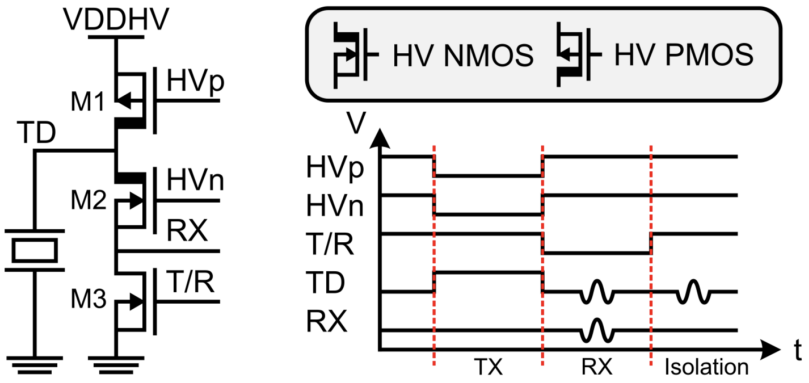


Figure 3.15: Class-D Pulser Core Circuit [14]

For charging the biasing capacitor, the pulser must be in transmit mode with HVn enabled and HVp disabled. In this way, the CMUT is connected to ground and the biasing capacitor can be charged. This is also referred to as the isolation state, as shown in Figure 3.15.

To switch the high-side PMOS device, a floating level shifter circuit is used, as shown in Figure 3.16. This circuit consists of a flip-flop combined with an SR-latch. During pulser startup, special attention is needed: since VDDHV is connected to a capacitor that may not yet be charged, the state of the PMOS

switch can be undefined at power-up. This can cause issues during biasing, such as charge sharing between the biasing and high-voltage capacitors. To ensure correct operation, VDDHV must first be brought above 5 V before the level shifter can function properly.

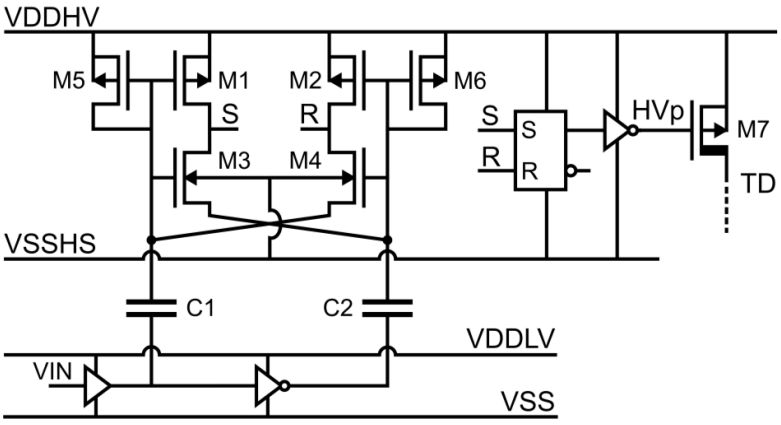


Figure 3.16: Floating Level Shifter Circuit [14]

3.7.2. Pulser Module

Surrounding the core, additional logic safely controls the pulser and buffers the data. Together with the biasing circuit and this logic, four pulsers are combined into one module, which is the configuration used in this project. The module is shown in Figure 3.17. The RxTx signal is equivalent to the T/R signal described earlier, allowing the pulser to be set to transmit or receive mode. The Data signal determines the output of the pulser.

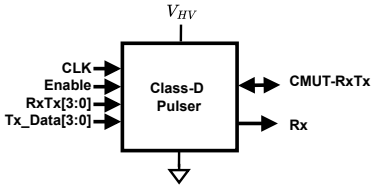


Figure 3.17: Class-D Pulser Module

Both RxTx and Data are buffered by a synchronous clear D-flip-flop. This ensures that these signals are synchronized with the clock, which is important for correct timing. The synchronous clear function guarantees that when the reset is high, the outputs are forced low at the next active clock edge. In other words, the reset is also synchronized with the clock to ensure proper operation. The reset of the flip-flop is connected to the Enable signal, so a low Enable is required to activate the pulser.

After buffering, the pulser outputs the data at the next clock cycle. The clock frequency determines the maximum pulse frequency and possible phase differences. Although phase differences are not used in this project, they could be interesting for future work, for example for time delays between pulse trains or beamforming. For energy efficiency, the clock frequency is kept as low as possible, in this case 2.6 MHz.

It is important to note that this pulser is not optimized for power consumption in a wearable device. In idle mode, the module consumes significant power, as shown in Table 3.1, mainly due to the internal bias circuit that generates the VSSHV supply. The VSSHV voltage must be minus 5 V with respect to VDDHV to supply the floating level shifter and ensure correct switching of the high-side PMOS. For future work, this module should be revisited to optimize for lower power consumption.

Supply	Voltage	Idle Power	Pulsing Power (Single Element)
VDD HV	30 V	1.98 mW	323 mW
VDD 5V	5 V	2.13 mW	2.47 mW
VDD 1V8	1.8 V	70.1 μW	71.1 μW

Table 3.1: Average Power Consumption of Class-D Pulser Module in Idle and Pulsing Mode

3.8. Layout and Pinout

The total area of the circuit is estimated by summing the areas of the individual components, including the (HV) switches, capacitors, and logic. This yields an approximate total area of 100 μm^2. This is just for indication, layouting and wirebounding will increase this area. Total pins are estimated at 61, which can be reduced by using shift registers for non-time-critical signals. A summary of the area and pin count is provided in Table 3.2.

Pin Category	Number of Pins
In-Output Connections	16
Logic Controller	24
Converter Signals	4
Output Logic Signals	2
Class-D Pulser	15
Total	61

Table 3.2: Estimated Pin Count Summary

4

Circuit Level Simulation

In this chapter, we present the prototype circuit-level simulations of our system using Cadence simulation software. The results are compared to the expectations set by the design scope and specifications. After this comparison, energy breakdowns and heatmaps from the Cadence simulations are introduced, followed by a comparison of these results with the MATLAB simulations.

Figure 4.1 shows an overview of the complete working system simulated in Cadence. The plotted signals are: `HVS0_Vout_Bias` (blue), `HVS1` (purple), and `HVS2` (yellow). The graph illustrates how the output voltages are built up over time, remain temporarily stable during pulsing, and then discharge again.

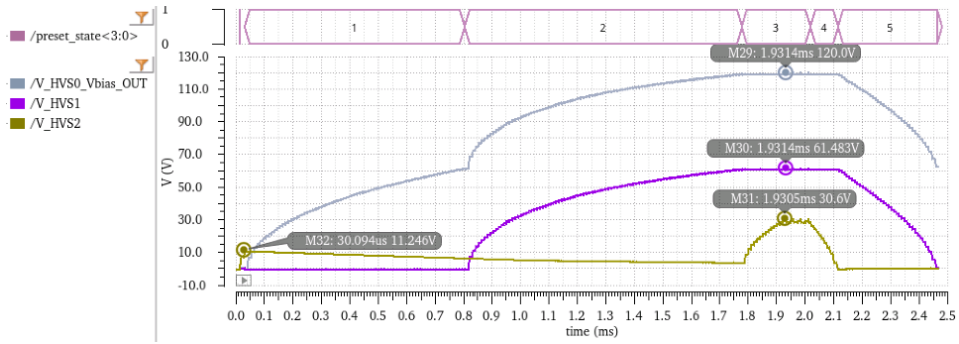


Figure 4.1: System output voltages during operation

After charging the output capacitors, the system repeatedly pulses the pulse-trains across the four different CMUT TXRX elements. At the bottom of the figure, the `main_state` indicates the states of the main controller: state 4 means the pulser is active, and state 3 indicates that the system has activated the power converter to recharge the high-voltage pulser capacitor. Afterwards, the system begins discharging the outputs capacitors indicated with state 4 and 5.

The total cycle duration is 2.5 ms. Compared to the 1.7 ms simulated in MATLAB, this is slightly longer. This difference is partly due to the main controller, which also takes time during the converter and pulser processes, for example during system initialization or when decisions must be made between different states. Additionally, there are extra losses that make the converter work slightly longer to bring the output capacitors to the desired voltage. Nevertheless, the additional steps are limited: counting the cycles for HVS1 during charging results in approximately 99 steps, compared to 96 in MATLAB. Discharging occurs in about 35 steps, versus 38 in MATLAB. This indicates that slightly more energy is lost during charging than expected, and probably less energy is recycled than predicted.

In the following sections, first, the pulser operation will be validated, then the energy breakdowns will be shown and finally the Cadence results will be compared to the MATLAB simulations.

4.1. Pulser

In this section, we validate the operation of the pulser circuit. Figure 4.2 shows four pulse trains of 5 pulses using four different CMUT elements. At the bottom of the figure, the `main_state` indicates the states of the main controller: state 4 means the pulser is active, and state 3 indicates that the power converter is enabled to recharge the high-voltage pulser capacitor.

Validating the pulse-train pulses itself, figure 4.3 shows a zoomed-in view of the pulse train on TXRX element 0.

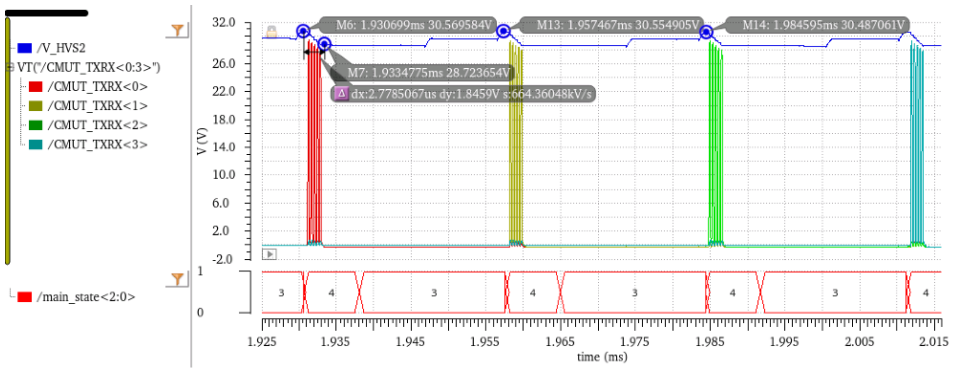


Figure 4.2: Simulation results of pulsing pulse trains on 4 elements

In blue, the HV DC voltage of the supply capacitor connected to the HVS2 port of the converter is shown. This voltage drops from 30.57 V to 28.72 V after the first pulse train. After each recharge session, the voltage is restored to approximately 30.50 V without much variation.

Figure 4.3 shows a zoomed-in view of the pulse train on TXRX element 0.

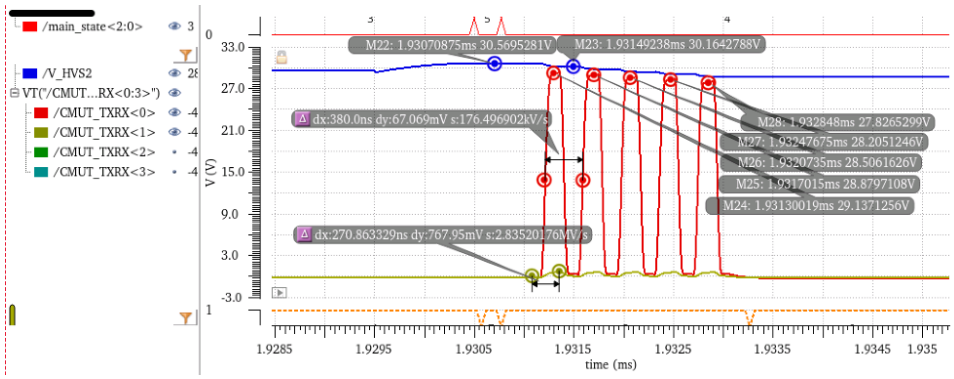


Figure 4.3: Characteristics of the generated pulse trains

In red, a pulse train of five pulses on TXRX element 0 is shown. The pulse spacing is 380 ns, corresponding to the transducer frequency of 2.6 MHz. This indicates that the pulser can drive the transducer at its resonant frequency.

Similar to the capacitive voltage drop, the peak voltages also decrease during the pulse train. The consecutive voltages are 29.13 V, 28.88 V, 28.51 V, 28.21 V, and 27.83 V. The maximum voltage drop of 1.3 V after five pulses roughly matches the expectations from the fundamental research (section 2.3.3, table 2.2).

Finally, the bottom of the graph shows the voltage on the other elements, here represented by the yellow line for TXRX element 1. During pulsing, the coupling effect described in the introduction is observed. The resulting pulse voltage on the inactive element is about 760 mV. According to equation 1.1 from the introduction, this would be estimated as:

$$V_{\text{pulse-coupling}} = V_{\text{tx}} \cdot \frac{C_{\text{tx}}}{C_{\text{bias}} + (N-1)C_{\text{tx}}} = 30 \cdot \frac{1}{53} \approx 0.57 \text{ V} \tag{4.1}$$

This cadence results shows slightly higher voltages than expected, the reason for this discrepancy was not further investigated.

4.2. Energy Consumption Breakdown

This section presents the energy breakdown and efficiency results from the Cadence simulations. The tables are formatted similarly to those in the MATLAB simulation section 2.6. After presenting these results, they will be compared and discussed with the MATLAB simulations.

The following results provide a detailed view of the energy flows and losses in the system. Table 4.1 summarizes the efficiency of the power converter during each system state, including charging the bias capacitors, pulsing, and recycling energy.

System State	Active LVS port [uJ]	Active HVS port [uJ]	Other Supplies [uJ]	Efficiency
0 Pre Charge Chv	0.957	0.858	0.149	0.776
1 Charge Bias1	34.3	23.5	2.51	0.638
2 Charge Bias2	43.1	22.8	3.15	0.493
3 Charge Chv and Pulse	9.37	7.51	0.671	0.748
4 Recycle Bias2	17.1	22.8	0.654	0.729
5 Recycle Chv Pulser	3.53	4.05	0.162	0.838

Table 4.1: Measured energy flows and total system efficiency during different system presets.

Table 4.4 summarizes the energy supplied by the different supply rails during each system state.

StateValue	Duration [uS]	1V8 [uJ]	5V [uJ]	Battery [uJ]	Total [uJ]
0 Pre Charge Chv	30.6	0.0299	0.119	0.957	1.11
1 Charge Bias1	746	0.72	1.79	34.3	36.8
2 Charge Bias2	937	0.903	2.25	43.1	46.3
3 Charge Chv and Pulse	239	0.232	0.439	9.37	10
4 Recycle Bias2	343	0.336	0.318	-0.00731	0.647
5 Recycle Chv Pulser	85.8	0.0849	0.0776	-0.00201	0.16
6 FINISHED	0.324	0.000345	0.000323	2.49e-09	0.000668
StateTotal	2380	2.31	4.99	87.8	95.1

Figure 4.4: State statistics for different presets and supply rails.

Table 4.5 provides a comprehensive total energy breakdown. This includes resistive and gate driver losses, trapped charge, pulser losses, recycled energy, and other minor contributions.

Supply Sources	Energy [uJ]
1V8	2.31
5V	4.99
Battery	87.8
Total	95.1

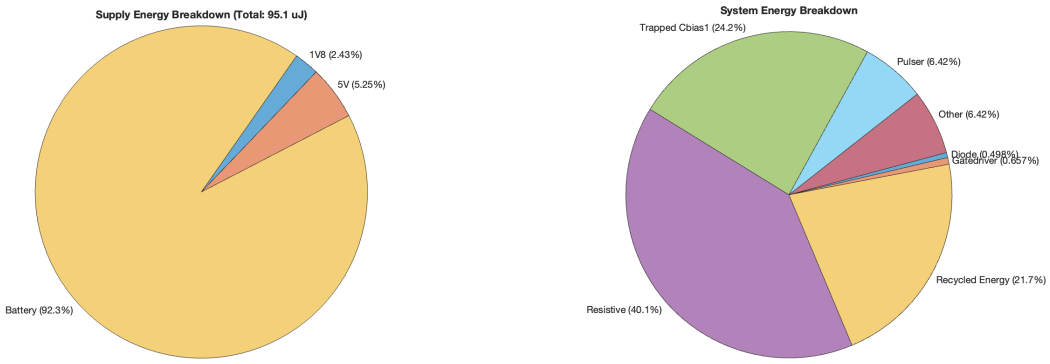
(a) Energy breakdown by supply

Category	Energy [uJ]
Diode	0.473
Gatedriver	0.624
Recycled Energy	20.6
Resistive	38.1
Trapped Cbias1	23
Pulser	6.1
Other	6.1

(b) Energy breakdown by system component

Figure 4.5: Comparison of energy breakdown: (a) by supply and (b) by system component.

Figure 4.6 shows pie charts of the same energy breakdown, making it easier to visually compare contributions from different supplies and system components.



(a) Supplies (b) System

Figure 4.6: Pie charts showing the energy breakdown for (a) supplies and (b) system components.

4.3. Heatmap Analysis

To gain a clear overview of the energy usage during different phases of the system, heatmaps were generated for each preset state. These heatmaps provide insight into the energy flows and identify which components consume the most energy during specific states of the power converter system. This helps to verify correct system operation and detect potential inefficiencies.

The energy was calculated by recording power data during the simulations and then integrating (or summing) it over time. Due to the large amount of data, visualizing it directly becomes complex. To simplify this, the data for each power converter state was compressed into five steps. With these five steps, the energy usage during a specific state can be visualized, including the beginning of the state (with associated switch transitions) and the intermediate steps of the state progression. It is important to note that the heatmaps do not show the total energy over a fixed time interval, but the energy usage during a specific state. Summing the energy values across all steps should correspond to the total energy usage shown in the energy breakdown tables.

Energy per step was calculated as follows: the state is divided into six points—t0 (start of state), t1 (20% of state duration), t2 (40%), t3 (60%), t4 (80%), and t5 (end of state). The energy is then obtained by integrating the power over each time interval:

$$E = \int P(t)dt \tag{4.2}$$

Figure 4.7 shows an example of a heatmap for the initialization phase of the pulser system. In this phase, the high-voltage capacitor is charged so that the pulser can be correctly configured while charging the bias capacitors.

On the left, the recorded power signals during the simulation are shown; at the bottom, the state of the power converter is indicated; on the right, the color map shows the energy usage. Red or green colors indicate higher energy flow or dissipation during a specific state.

Signals starting with `Pp_` represent the power flowing into and out of the power converter. These signals indicate how much energy has flowed into or out of the system during each step. Signals starting with `P_` represent the internal components of the system, such as the coil or individual MOSFET devices. These signals do not represent energy flow but show energy dissipation within the component.

It is important to note that these signals can be positive (green), indicating power flowing out of the converter, or negative (red), indicating power supplied to the system during the state.

The sum of the incoming port energy minus the dissipation of the individual components should correspond to the outgoing energy of the system.

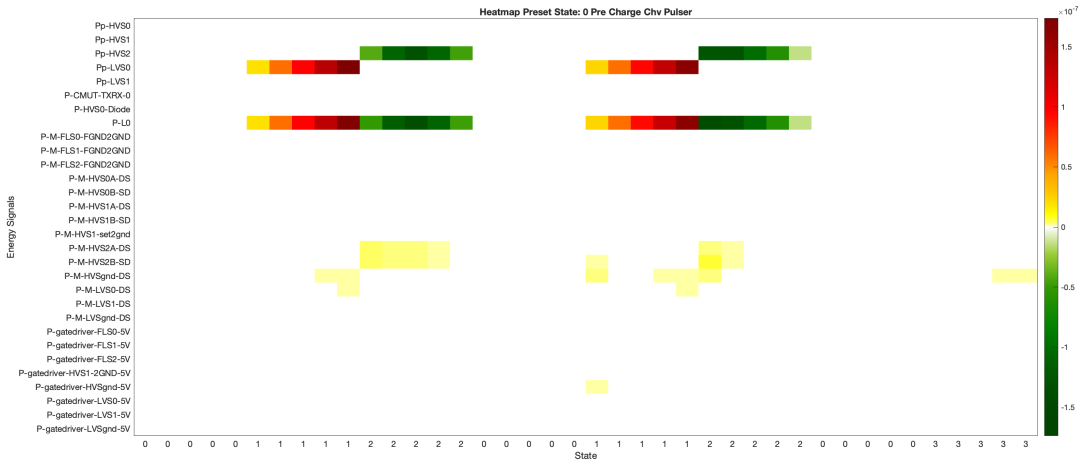


Figure 4.7: Heatmap showing energy flows and dissipation during the Pre Charge Chv Pulser state.

In the appendix, the heatmaps are included for all different charging and recycling states.

4.4. MATLAB versus Cadence Results

This section focuses on comparing the energy differences between the MATLAB and Cadence simulations. The results were examined globally to see how they relate to the theoretical expectations and the MATLAB simulations. Due to the large amount of results, the focus is on the most notable observations.

4.4.1. Overall Simulation Comparison

Table 4.8 compares the energy breakdown by supply for both the MATLAB and Cadence simulations, presented side by side for direct comparison.

Supply Sources	Energy [uJ]
Battery	52.2
Gatedrivers_5V	0.6

(a) MATLAB Simulation

Supply Sources	Energy [uJ]
1V8	2.31
5V	4.99
Battery	87.8
Total	95.1

(b) Cadence Simulation

Figure 4.8: Comparison of energy breakdown by supply for MATLAB (left) and Cadence (right) simulations.

Table 4.9 compares the energy breakdown by system component for both simulations.

System Category	Energy [uJ]
Recycled_Energy	25.6
Trapped_Cbias1	21.4
Resistive_Loss	3.1
Pulser_Loss	2.1
Gatedriver_Loss	0.6
Others	-0

(a) MATLAB Simulation

Category	Energy [uJ]
Diode	0.473
Gatedriver	0.624
Recycled Energy	20.6
Resistive	38.1
Trapped Cbias1	23
Pulser	6.1
Other	6.1

(b) Cadence Simulation

Figure 4.9: Comparison of energy breakdown by system component from (a) MATLAB and (b) Cadence simulations.

The total energy per cycle is 53 μJ in MATLAB versus 95 μJ in Cadence, an increase of 79%. Resistive losses are notably high, about 12 times higher than expected, accounting for 38 μJ or roughly 40% of the total energy consumption. Part of this increase was expected due to an estimated 10% higher R_{on} from lower V_{gs} in the back-to-back (BB) switch configuration. However, this does not fully explain the observed factor. This will be investigated further in the following section.

Other contributions, such as gate driver losses, recycled energy, and trapped bias capacitor energy, differ by roughly 20%, which is within an acceptable range. The recycled energy is about 20% lower than expected, while roughly 10% could be explained by idle losses of the pulser, which is not optimized for low energy consumption. As discussed in section 3.7.2, the pulser can consume up to 4 mW in idle. Assuming it is active for 1.5 ms, this already accounts for 6 μJ per cycle, excluding the pulsing energy itself, which was estimated at around 2 μJ. Combined, this roughly matches the values shown in the energy breakdown tables. Given that this extra consumption accounts for more than 6% of the total energy, it significantly impacts the overall efficiency and is worth optimizing in the future.

Tables 4.2 and 4.3 compare the power converter efficiency for MATLAB and Cadence simulations.

System State	Active LVS Port [uJ]	Active HVS Port [uJ]	Gatedriver Energy [uJ]	Efficiency
CBias1 chargeC	22.3	21.4	0.157	0.935
CBias2 chargeC	22.3	21.4	0.157	0.935
CBias2 recycleC	20.6	21.4	0.157	0.936
Chv chargeC	5.61	5.35	0.0426	0.859
Chv recycleC	5.02	5.25	0.0393	0.855
Pulsing pulseCP	0	2.11	0.00354	0
Pulsing rechargeC	2.05	2.01	0.0622	0.754

Table 4.2: Efficiency of power converter during each system state (MATLAB).

System State	Active LVS port [uJ]	Active HVS port [uJ]	Other Supplies [uJ]	Efficiency
0 Pre Charge Chv	0.957	0.858	0.149	0.776
1 Charge Bias1	34.3	23.5	2.51	0.638
2 Charge Bias2	43.1	22.8	3.15	0.493
3 Charge Chv and Pulse	9.37	7.51	0.671	0.748
4 Recycle Bias2	17.1	22.8	0.654	0.729
5 Recycle Chv Pulser	3.53	4.05	0.162	0.838

Table 4.3: Measured efficiency for different simulation presets (Cadence).

4.4.2. Resistive Loss Analysis

To understand the source of these resistive losses, they were further broken down, as shown in Table 4.4.

Resistive Component Signal	Energy [uJ]
L0	2.44
M_FLS0_FGND2GND	1.65
M_FLS1_FGND2GND	2.35
M_FLS2_FGND2GND	0.343
M_HVS0A_DS	0.19
M_HVS0B_SD	4.33
M_HVS1A_DS	0.676
M_HVS1B_SD	13.8
M_HVS1_set2gnd	0.0238
M_HVS2A_DS	0.177
M_HVS2B_SD	1.33
M_HVSgnd_DS	10.4
M_LVS0_DS	0.311
M_LVS1_DS	0.071
M_LVSgnd_DS	0.0394

Table 4.4: Detailed resistive loss breakdown.

The largest contribution comes from the B switches in the BB configuration, which are connected to the external output. Heatmap analysis shows that losses in these switches occur mainly when the high-voltage side nodes are connected to the output node. If the output node is at high voltage, charge flows into the internal parasitic capacitances of the converter to bring them to the same voltage, resulting in a large current peak through the B switches, which explains the high losses.

Two questions arise: why does the same dissipation not occur in the A switches, and why is the converter more efficient during energy recycling than during output capacitor charging?

The hypothesis is that this can be explained by the intermediate floating ground node in the BB configuration. When the configuration is switched on, this node is initially at zero volts. It must first be charged before the internal VL2 node is charged, so no large current peak occurs through the A switches compared to the B switches. This situation is illustrated in Figure 4.10, which shows the relevant nodes and switch configuration of the HVS converter section.

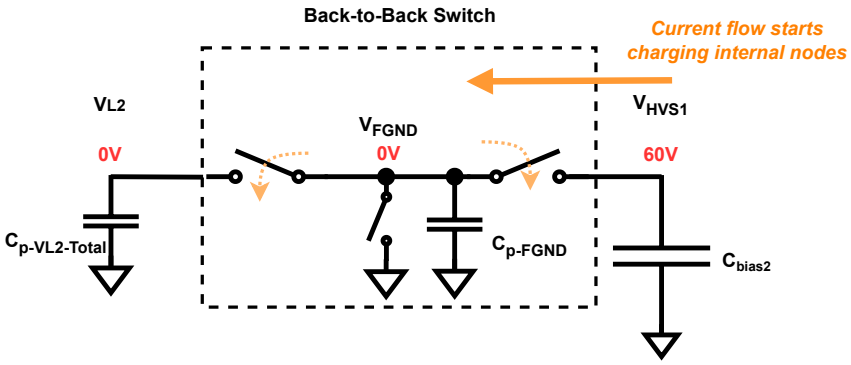


Figure 4.10: Schematic of the HVS converter section, showing the BB switch configuration and relevant nodes voltages

To ensure this is not a short circuit effect due to wrong switch control, the parasitic capacitances and corresponding energy losses were estimated using the unity drain and source capacitances of the HV MOSFETs (Table 4.5).

Device Name	$R_{\text{on–u}}$ **[**$\Omega \cdot \mu$**m]**	$C_{\text{gg–u}}$ **[F/**μ**m]**	$C_{\text{dd–u}}$ **[F/**μ**m]**	$C_{\text{ss–u}}$ **[F/**μ**m]**	L_{gate} **[**μ**m]**
nld65_g5b_mac	11726	$4.61 \cdot 10^{-15}$	$2.52 \cdot 10^{-15}$	$3.92 \cdot 10^{-15}$	0.700

Table 4.5: Unity parameters for HV-MOSFET devices in 180nm BCD-Gen2 technology.

The chosen switch sizes for HV switches are 10.000 μm for the ground switch and 3.000 μm for each BB switch. Figure 4.11 shows the schematic of the HV section of the converter, including the relevant nodes for parasitic capacitance estimation.

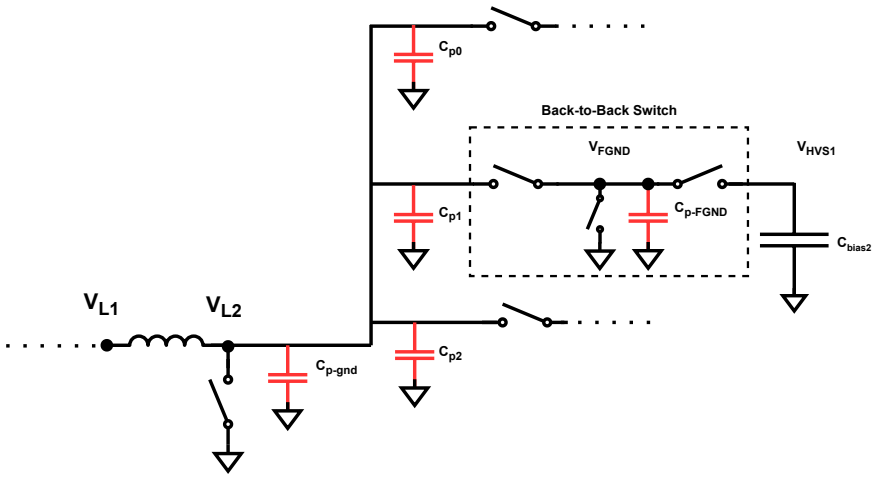


Figure 4.11: Simplified Schematic HVS Converter, showing relevant parasitic capacitances

Parasitic capacitances on the VL2 node can be estimated as:

$$C_{p-\text{VL2-Total}} = C_{dd-u} \cdot \left(M_{\text{HVS\_gnd}} + M_{\text{HVS1}} + M_{\text{HVS2}} + M_{\text{HVS3}}\right) = 2.52{\times}10^{-15} \cdot 19000{\times}10^{-6} \approx 4.788{\times}10^{-11}\,\text{F} \tag{4.3}$$

The floating ground node capacitance is estimated as:

$$C_{p-\text{FGND}} = C_{ss-u} \cdot (M_{\text{HVS1\_A}} + M_{\text{HVS1\_B}}) = 3.92 \times 10^{-15} \cdot 6.000 \times 10^{-6} \approx 2.352 \times 10^{-11}\,\text{F} \tag{4.4}$$

The energy required to charge both nodes can be calculated as:

$$E = \frac{1}{2}\left(C_{p-\text{VL2}} + C_{p-\text{FGND}}\right) V_{\text{out}}^2 = 0.5 \cdot (4.788 + 2.352) \times 10^{-11} \cdot 60^2 \approx 0.26\ \mu J \tag{4.5}$$

Assuming a linear voltage change during charging and discharging over approximately 150 steps, the total additional loss is approximated per single charge and discharge cycle as:

$$E_{\text{total}} = 0.5 \cdot 150 \cdot 0.26\ \mu J \approx 20\ \mu J \tag{4.6}$$

Heatmap data confirms this, showing B-switch dissipation during the final charging step around 0.158 μJ and at the start of recycling 0.179 μJ, consistent with the theoretical estimates.

Voltage drops on the output node during charging are shown in Figure **??**, confirming the source of high B-switch losses. As side note, also the coupling effect during pulsing is visible in this figure, as explained in earlier sections.

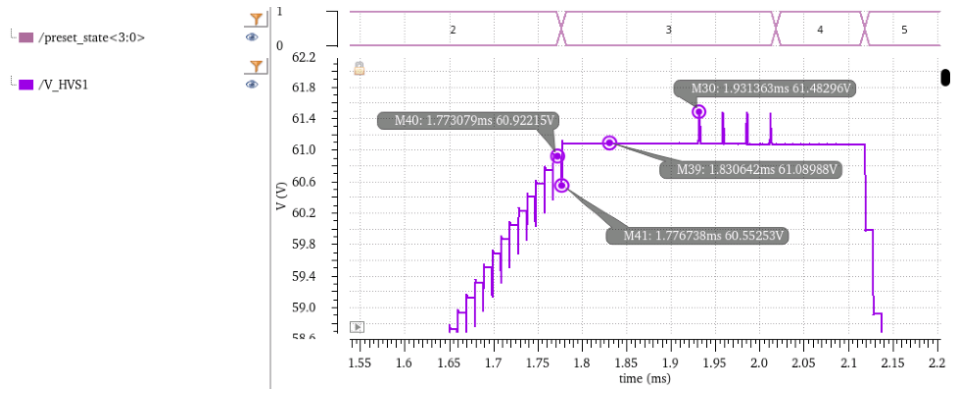


Figure 4.12: Voltage drops observed on the HVS1 output during charging the output capacitor.

The higher efficiency during recycling is explained by energy stored in the internal parasitic capacitances being transferred to the coil instead of dissipated as illustrated in the following figure:

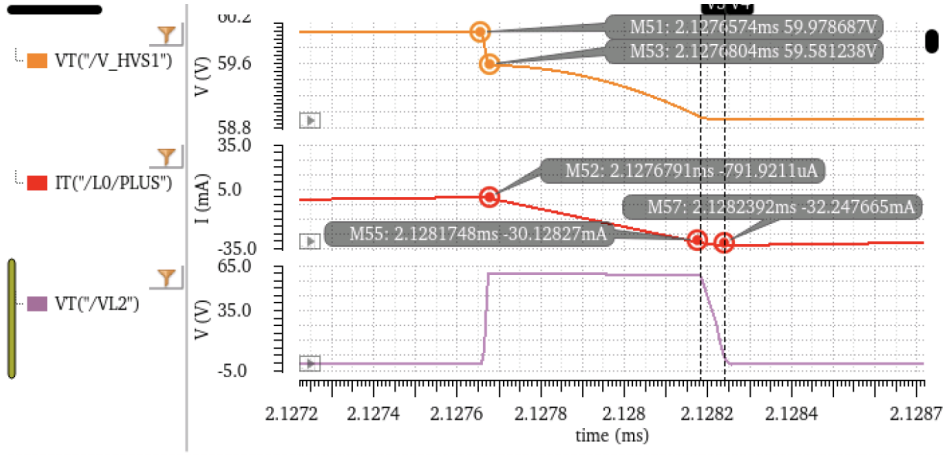


Figure 4.13: Discharging of the internal VL2 node during the discharge phase.

In orange, the output node HVS1 is shown; in red, the current through the inductor; and in purple, the voltage on the internal high-voltage node VL2 connected to the inductor. Notably, during the charging of the internal node—when the converter starts charging the inductor—a voltage drop is observed on the output. This voltage drop is approximately equal to the drop previously observed during output capacitor charging. Next, a sinusoidal discharge is seen, indicating the coupling between the capacitor and the inductor, followed by a linear increase in current as the inductor charges. When the inductor current reaches 30 mA, the output node is disconnected. Interestingly, the inductor current continues to increase linearly, while at that moment the VL2 node voltage decreases with a slight curvature. This indicates that the energy stored in the parasitic capacitance of the VL2 node is indeed absorbed by the inductor. This could explain why this phase is significantly more efficient. At the same time, it demonstrates that by properly timing the switch transitions, it is possible to recycle the energy stored in the parasitic capacitances around the inductor.

These observations highlight the benefit of carefully timing the ground switch and independently controlling BB switches to improve overall converter efficiency by recycling energy from parasitic HV switche capacitances.

4.5. Summary of key findings

Key findings from the Cadence circuit-level simulations are summarized below:

- **System operation validated:** The Cadence circuit-level simulations confirm correct operation

of the proposed US wearable system prototype, with output voltages and pulse characteristics matching the project scope, theoretical expectations and MATLAB results.

- **Energy efficiency insights:** The total energy per cycle is higher in Cadence (95 μJ) than in MATLAB (53 μJ), mainly due to increased resistive losses and idle power consumption in the pulser.
- **Detailed Simulation Data and Heatmap analysis:** Detailed simulation data and heatmaps are provided to give insight into when and where energy is dissipated.
- **Resistive losses:** Resistive losses are the dominant contributor to total energy consumption, accounting for about 40% of the total. These losses are primarily caused by the B switches in the back-to-back (BB) configuration, especially during charging of the output capacitor.
- **Parasitic capacitance effects:** Parasitic capacitances on internal nodes (VL2, FGND) lead to additional energy losses during charging, but can be partially recycled during energy recovery phases if switch timing is optimized.
- **Switch timing and control:** Careful timing of the ground switch and independent control of BB switches enables recycling of energy stored in parasitic capacitances, improving overall efficiency.
- **Recommendations:** Further efficiency improvements can be achieved by optimizing system current, switch sizes, reducing idle losses in the pulser, and implementing advanced switch control strategies to maximize energy recycling from parasitic capacitances.

In summary, the circuit-level simulations provide a comprehensive understanding of the energy flows, losses, and optimization opportunities in the power converter and pulser system. The findings highlight the importance of both device-level design choices and system-level control strategies for achieving high energy efficiency in future implementations.

5

Conclusion and Future Work

This research has investigated the design and simulation of an energy-recycling inductive power converter for CMUT-based wearable ultrasound systems. By combining theoretical insights, MATLAB simulations, and Cadence circuit-level validation, the work provides a detailed evaluation of the opportunities and challenges in enabling energy-efficient and compact ultrasound wearables.

The need for energy-efficient ultrasound pulsers in wearable health monitoring devices was established. It compared conventional class-D and resonant pulsers, highlighting a fundamental trade-off between flexibility and energy efficiency. The discussion for pulser architectures underlined the importance of high-voltage biasing, which dominates the energy budget. The proposed four-switch converter topology emerged as a promising solution, enabling both biasing and pulsing with energy recycling. The operating region of the converter was shown to differ significantly from traditional buck-boost converters, wherein a new field in research is opened and demonstrated. By understanding the characteristics and behaviour of the load, the converter can be optimized to operate in a fundamentally different way than traditional converters. Finally, energy recycling makes it possible to re-use this energy in other sub-systems, which is a promising new direction for power-converters in wearable applications.

System-level Matlab simulations clarified the influence of inductor sizing, switch dimensioning, and current optimization on efficiency. A break-even analysis showed that, for the relevant pulse count (20 pulses per acquisition), the conventional pulser is more practical than the resonant alternative, offering similar efficiency with lower complexity. These results demonstrated the central role of component trade-offs in optimizing for proposed power converter and provided a validated foundation for circuit-level design.

Circuit-level implementation results in Cadence simulation software demonstrate that the prototype design can operate correctly, generating the required high-voltages and enabling energy recycling. In doing so, the work successfully bridges the gap between a purely theoretical model and a detailed circuit-level implementation in commercial TSMC 1810nm BCD-Gen2 Technology. However, the simulations also revealed that the total energy consumption per cycle is significantly higher than predicted by MATLAB. This discrepancy is largely explained by resistive losses, especially in the back-to-back switches, and by parasitic effects not fully captured in earlier models. Crucially, the detailed analysis not only identified the root cause of the excess energy but also led to the proposal of a new control method. By optimizing switch timing and exploiting the possibility of partial energy recovery from parasitic capacitances, the study provides a concrete path toward improving the converter's efficiency in future implementations.

With this work, the characteristics and optimization strategies of an inductive power converter operating in previously unexplored regimes have been investigated and exposed. Based on this understanding, a new converter design was proposed and validated. The circuit-level implementation in Cadence simulations demonstrated that the converter not only functions correctly, but also enables energy recycling while meeting the requirements of a CMUT-based ultrasound wearable. Importantly, this

proof-of-concept shows that such a system can be realized in commercially accessible TSMC 180nm BCD-Gen2 technology.

5.1. Future Work

While this thesis has demonstrated the feasibility and potential of an energy-recycling inductive power converter for wearable ultrasound systems, several opportunities remain for further improvement and exploration. The following points outline promising directions for future research and development, aimed at increasing efficiency, reducing system complexity, and bridging the gap between simulation and practical implementation.

- Investigating energy recycling from the parasitic capacitances of the high-voltage nodes must be further explored. This could be achieved by optimizing the timing of the switch control. This enables energy stored in parasitic capacitances to be recycled back into the system, for example by keeping LVSgnd enabled longer during a transition before enabling HVSgnd. Assuming that all energy dissipated by the B switches are caused by charging the internal nodes, this could lead to a energy improvement of half of the energy lost in the B switches, which is about 20% of the total energy.
- Subsequentially, it could be investigated whether it is possible to charge the high-voltage side internal node to output voltage from the inductor. An imagineable method could be by delaying the activation of the BB output switches, before energy from the inductor is used to charge the output capacitor. If this is possible, it could lead to savings of ordinary high resistive losses from the B switches, which enables the other 20% energy savings.
- Implementing independent control of the switches in the back-to-back configuration enables energy recycling and charging the parasitic capacitances of the source nodes by the inductor, as mentioned above and demonstrated in the Cadence simulations. Additionally, this enables reduction of switching losses, because dependent in how the BB switch has to isolate the in- and output ports, not always both switches need to be switched.
- Further optimization of the pulser in context of power efficiency is needed to use in wearable applications. The idle power consumption of the pulser is significant high and consumes 6% of the total energy consumption.
- Adding power management control to selectively enable or disable specific subsystems per state, in order to minimize unnecessary power consumption.
- The current design is based on buck-boost mode. Future work could investigate the possibilities of operating in either buck or boost mode only. This may result in lower switching losses and could also reduce the complexity of the internal high-voltage nodes that need to be switched repeatedly. Exploring these different modes and their impact on efficiency and system complexity is an interesting next step.
- Bridging the gap between simulation and practical implementation by layouting and fabricating a physical prototype.

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A

Appendix

A.1. Cadence Simulation: System Preset Heatmaps

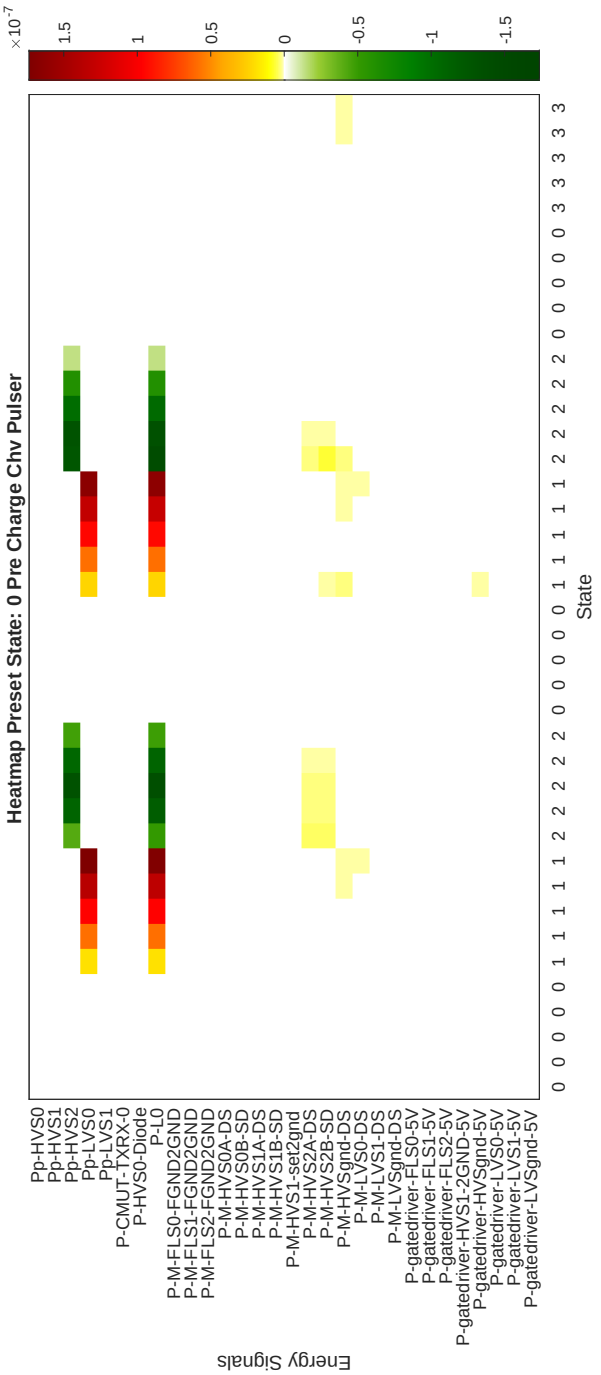

Figure A.1: Heatmap: PresetState 0 0 Pre Charge Chv Pulser

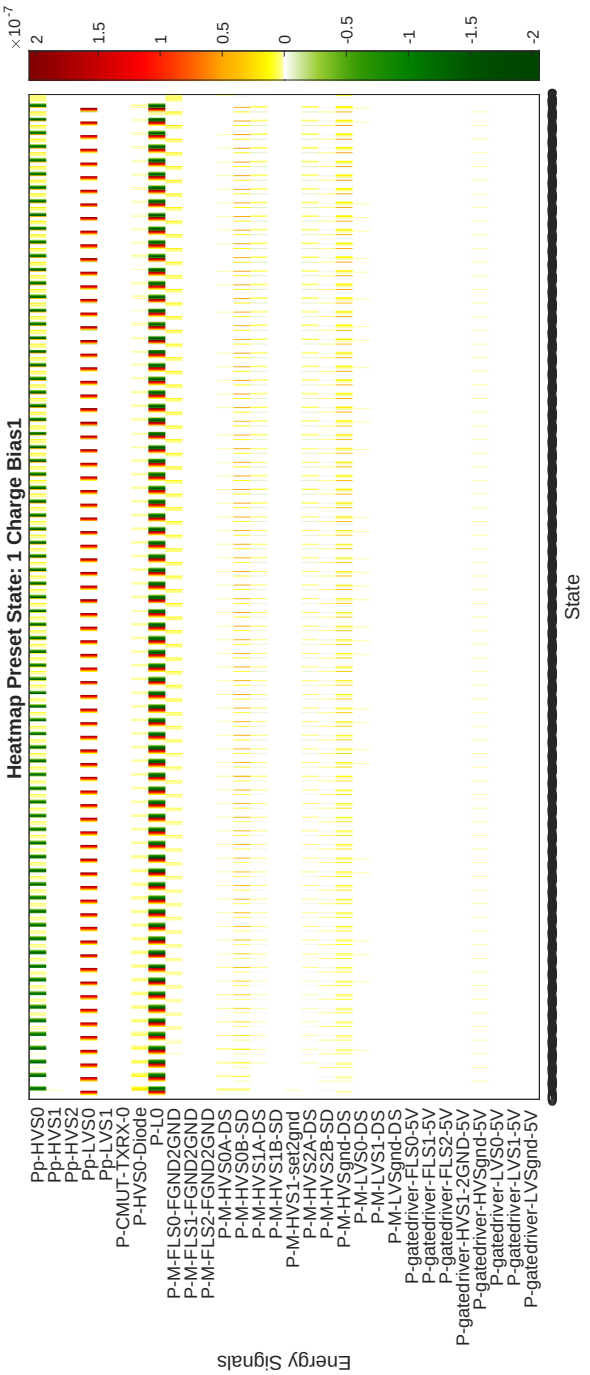

Figure A.2: Heatmap: PresetState 1 1 Charge Bias1

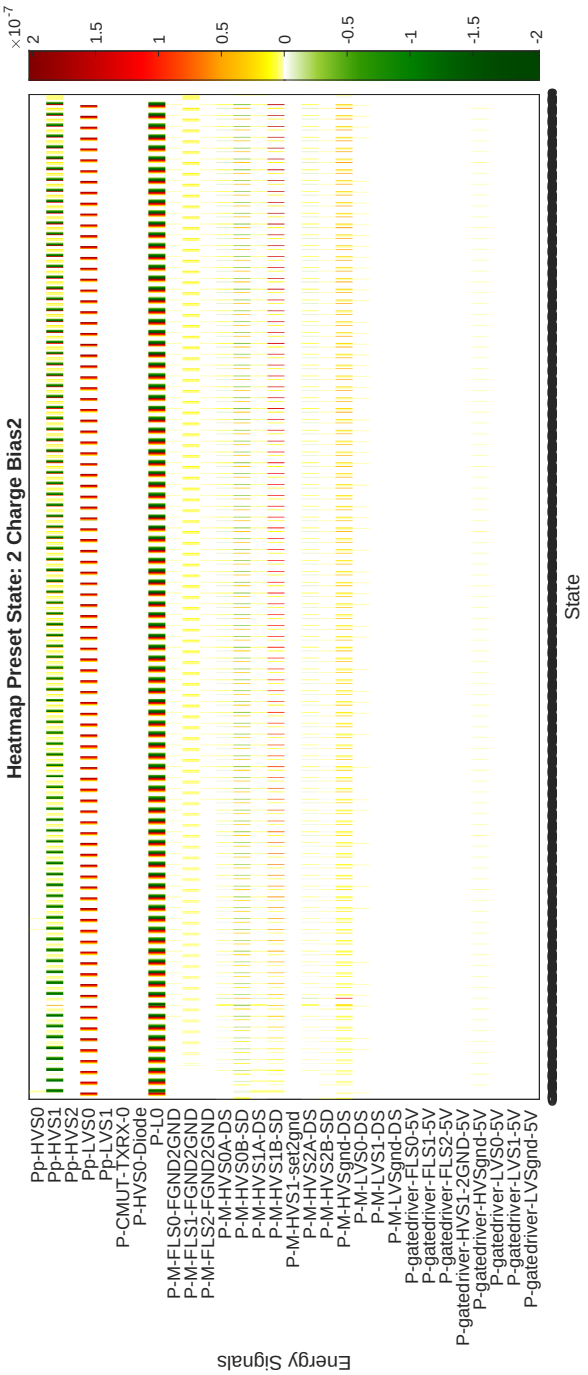

Figure A.3: Heatmap: PresetState 10 2 Charge Bias2

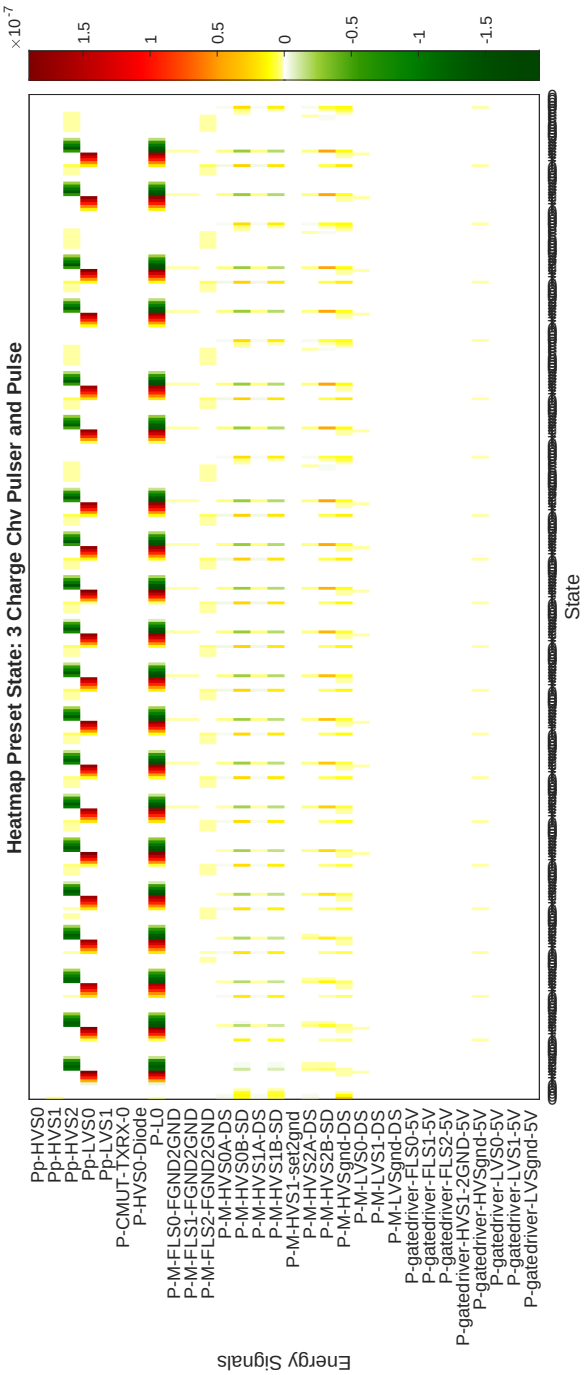

Figure A.4: Heatmap: PresetState 11 3 Charge Chv Pulser and Pulse

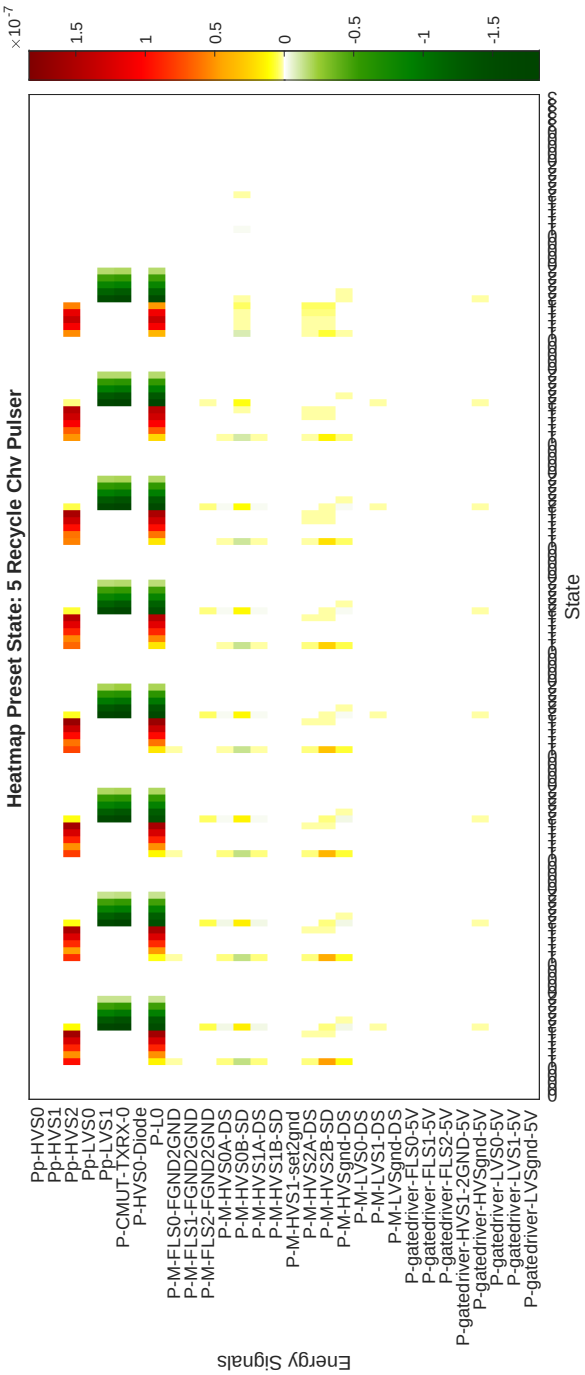

Figure A.5: Heatmap: PresetState 101 5 Recycle Chv Pulser

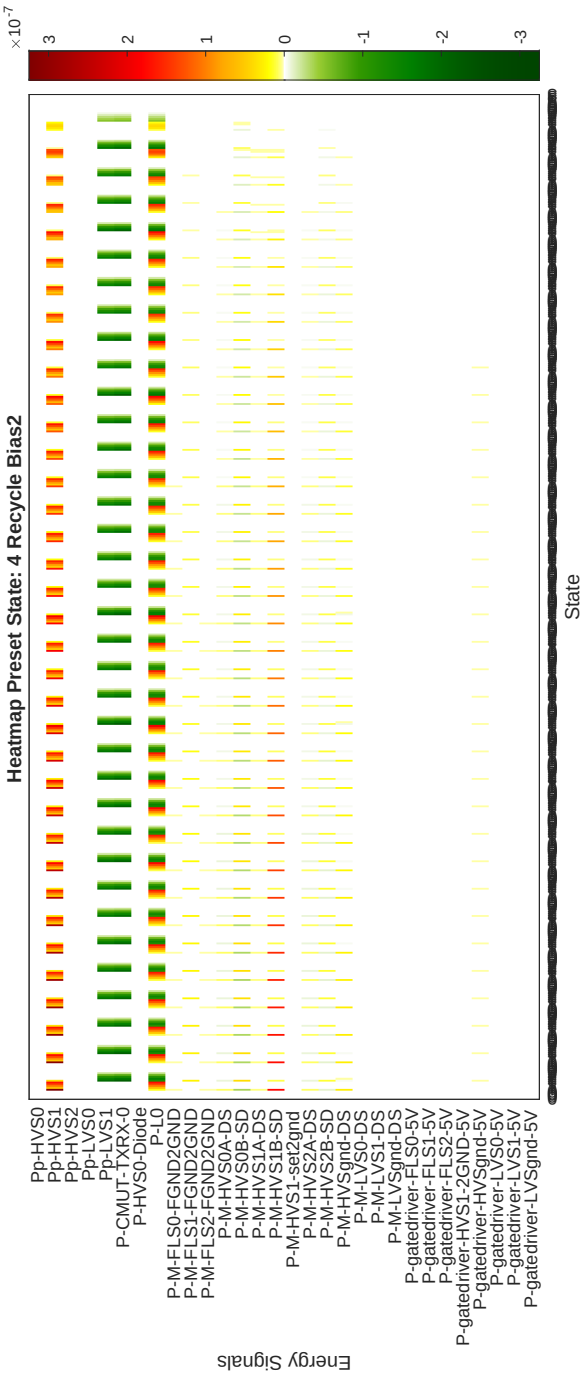

Figure A.6: Heatmap: PresetState 100 4 Recycle Bias2