An FM Chirp Waveform Generator and Detector for Radar

Sawtooth Generator and FM Detector

by

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Abstract

The "FM Chirp Waveform Generator and Detector for Radar" is a Bachelor graduation project with an educational purpose. In this thesis, two modules of the whole system are designed and simulated. In particular, the sawtooth generator and the FM detector. The sawtooth generator is used to generate a linearly increasing signal, which can be used to make a chirp signal. The FM detector is used to extract the original information signal from the received FM signal. The used procedure consisted of determining possible implementations, setting up the design equations, choosing component values and simulating the circuits in ADS. The sawtooth generator was implemented using a ramp generator, Schmitt trigger and a voltage clamper while the FM detector was implemented using a balanced slope detector and a differential-to-single-ended converter. The results showed that the sawtooth generator can successfully produce a sawtooth waveform and that the FM detector can successfully retrieve it.

It was concluded that both the modules satisfy all the requirements, meaning that they should work as expected in the whole system. Finally, the future steps were listed which, among others, include improving the linearity of the sawtooth generator and the FM detector.

Preface

The purpose of this thesis is to finalise the 3 year-long Bachelor programme in Electrical Engineering by designing an FM chirp transceiver for radar applications. The whole system was divided into three main parts and distributed among groups of 2 students. In this thesis, the design and simulation of the sawtooth generator and FM detector can be found.

The thesis was written in the spring of 2020, during the COVID-19 pandemic. Due to these circumstances, a physical implementation could not be made, and all communication had to take place online. Nevertheless, good teamwork and efficient planning resulted in a feasible design, where a lot was learned. In total, 9 weeks were given for this project, in which a literature study was done, a design was made, simulations were done and a thesis was written.

We would like to thank our supervisors dr. S. M. Alavi and dr. M. Babaie for helping us throughout the duration of the whole project. During the weekly online meetings, they gave us a lot of useful feedback and helpful information for realising the project. Additionally, we would also like to thank our good friends and members of our project group: Dimme de Groot, Lars Bouman, Abbas Sabti and Roderick Tapia Barroso. They provided continuous support and kept us motivated even in these troubled times.

Youri Blom
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Contents

Part I

System overview

1. Project Introduction

In this project, an FM chirp generator and detector for radar is developed [1].

RAdio Detection And Ranging (radar) is a technique used to determine range, angle and velocity of objects [2]. Currently, radar is mostly used to detect objects such as aircraft, ships and cars. It has applications in astronomy, geology, and weather forecasting amongst others [2], [3].

A schematic overview of a radar system can be seen in Figure 1.1. The principle on how radar operates is by radiating an Electromagnetic (EM) wave towards an object and measuring the reflected wave.

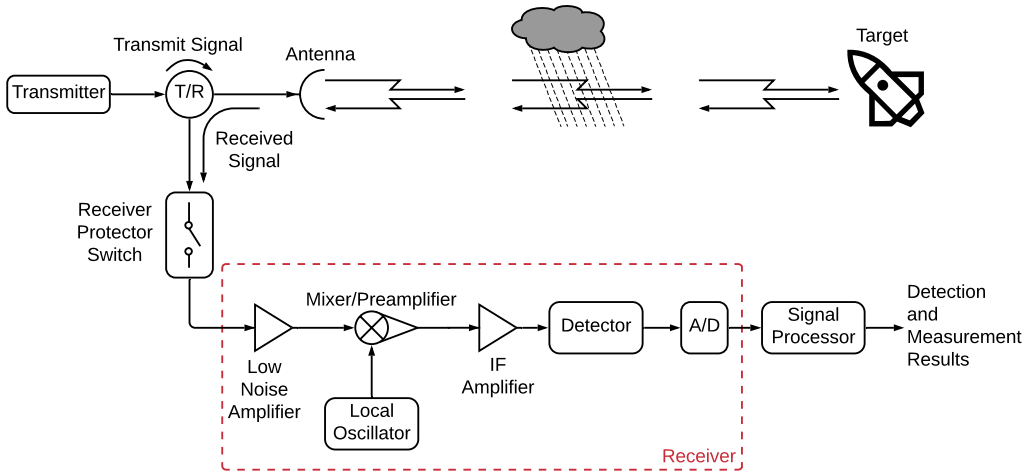


Figure 1.1: Major elements of the radar transmission/reception concept (based on [4]).

With the growing interest for autonomous vehicles, radar has come to play an important role in the automotive industry. Frequency-Modulated Continuous-Wave (FMCW) is often used in these radar systems [5]. State-of-the-art radar systems and a basic explanation on their operation can be found in Section 2.2.

The system designed in this project consists of two main parts, the first part is the transmitter (generally referred to as TX), which is used for generating and transmitting the chirp signal. The second part is the receiver (generally referred to as RX), which is used to receive and recover the sawtooth signal by demodulating the chirp signal. A top-level block-diagram of the two parts is given in Figure 1.2.

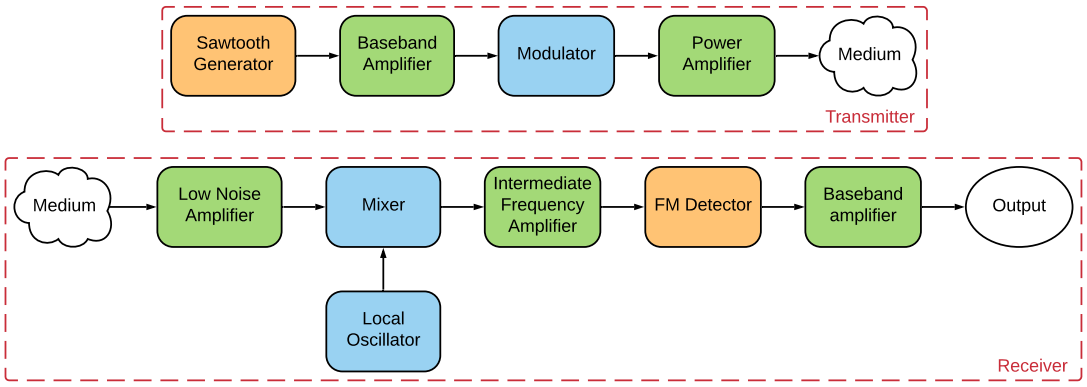


Figure 1.2: A top-level block-diagram of the receiver and transmitter architecture.

As can be seen, the system consists of many parts. These parts can be divided in a few subgroups, which are briefly described below.

- **The sawtooth generator** is formed by the sub-block depicted on the upper left of Figure 1.2. As the name states, it is used to generate a sawtooth waveform. The generated signal is also referred to as the baseband signal.
- **The amplifiers** are used to amplify the signal at different places in the system. In Figure 1.2, five amplifiers are depicted. The baseband and the Intermediate Frequency (IF) amplifier are used to amplify signals in the baseband frequency and in the IF, respectively. Both frequencies are lower than the transmit (or radio) frequency. A Power Amplifier (PA) is used to amplify the FM-signal and also forms the interface with the antenna. At the receiver side, a Low Noise Amplifier (LNA) is used to amplify the received signal. Both the PA and LNA operate at the Radio Frequency (RF). Finally, a baseband amplifier is used to buffer the signal at the output of the FM detector.
- **The modulator** and the **FM detector** are respectively used to modulate and demodulate the signal. The modulator oscillates at the RF, with the instantaneous frequency being determined by the amplitude of the baseband signal. This ultimately results in a chirp signal at the output. The detector is used to recover the original baseband signal. This is achieved by extracting the message signal from the phase of the IF signal to create a baseband signal.
- **The mixer** and the **Local Oscillator (LO)** are used to shift the frequency of the output of the LNA to an IF. This simplifies the design of subsequent stages in the receiver. It should be noted that, just like the modulator, the LO is a Voltage Controlled Oscillator (VCO).

1.1 Project Objective and Problem Definition

The rise of autonomous vehicles has sparked the interest in high-end radar sensors from industry. This project aims to introduce students to RF circuit design from an educational perspective.

As the attentive reader might have noticed, the proposed system architecture does not actually resemble a complete radar system. Because the development of a full radar system lies beyond the scope of a Bachelor thesis, this project constrains itself to the development of a separate receiver and transmitter part. Ultimately, the goal is to be able to modulate a sawtooth signal and transmit this over a range of at least five meters, after which the sawtooth signal should successfully be recovered at the output.

To facilitate designing the system in three subgroups, the previously described modules are split into three parts.

1. The amplifiers
2. The mixer, modulator and local oscillator
3. The FM detector and the sawtooth generator

This thesis focuses on the development and simulations of the sawtooth generator and FM detector.

1.2 Methodology

In order to arrive at a working transceiver design, it is important to have the means to reliably simulate and validate the designed circuits. For this purpose, Advanced Design System (ADS) is used. ADS is a software package developed by Keysight technologies. Furthermore, MATLAB is

used for processing the data obtained from ADS. It is also used to generate figures of the data for aesthetic reasons. Finally, Lucidchart is used to make figures with illustrative purposes.

Note that, under normal circumstances, the designed circuits would have been validated by the means of a physical prototype. However, in light of the current COVID-19 pandemic, the circuit validation is also done in ADS.

1.3 Thesis synopsis

This thesis is divided into three parts. The first part contains information, which is important for both the FM detector and the sawtooth generator. This includes the theory of FM, the project requirements and the transistor choice.

The second part explains the design of the sawtooth generator. Firstly, theoretical information is presented and implementation choices are made. After that, the design equations are derived and trade-offs are discussed, which are used to calculate the component values of the circuit. Finally, simulations in ADS are presented and discussed.

The third part explains the design of the FM detector. Similar to the second part, theoretical information and implementation choices are discussed first. Then the design equations and trade-offs are discussed, which are used to calculate the component values. Finally, simulations in ADS are shown and discussed.

The fourth and final part is the appendix, where all the extra information can be found that did not make it into the main part of the thesis. This includes: schematics of the sawtooth generator and the FM detector, all the simulated intermediate signals between the sub-modules, the integration with interfacing modules, the MATLAB code and the Bill of Materials (BoM).

2. Frequency Modulation

In radio technology, signals are typically modulated before transmissions using different modulation techniques. An advantage of using modulation techniques is that a specific bandwidth can be assigned to every user, such that there is little interference. One of the modulation techniques is Frequency Modulation (FM), which is used for this project. An advantage of FM is that the amplitude of the carrier is constant which means that the power is constant. Another advantage is that the information is not present in the amplitude of the signal meaning that it is less susceptible to noise [6]. This is not the case for Amplitude Modulation, where the information signal is incorporated in the amplitude of the carrier.

2.1 The mathematical theory

In FM, the instantaneous frequency of the transmitted signal is changed according to the information signal, as shown in Equation (2.1) and Equation (2.2) found in [7].

$$s(t) = A_c \cos\left[\omega_c t + \theta(t)\right] \tag{2.1}$$

where

$$\theta(t) = D_f \int_{-\infty}^{t} m(\tau) d\tau \tag{2.2}$$

where D_f is the frequency deviation constant, $m(t)$ is the information signal and ω_c is the carrier frequency.

The instantaneous frequency of the signal is $f_i(t) = f_c + \frac{1}{2\pi} D_f m(t)$. To make sure that the frequency range does not interfere with other neighbouring signals, the deviation of the frequency should not be too large. The frequency deviation can be determined by Equation (2.3).

$$\Delta F = \frac{1}{2\pi} D_f V_p \tag{2.3}$$

where

$$V_p = \max\left[m(t)\right] \tag{2.4}$$

A practical example of FM can be seen in Figure 2.1 where a carrier wave is being modulated by a sawtooth signal. The frequency range of the transmitted signal is centred around ω_c. At the receiver, this signal has to be demodulated to obtain the original signal.

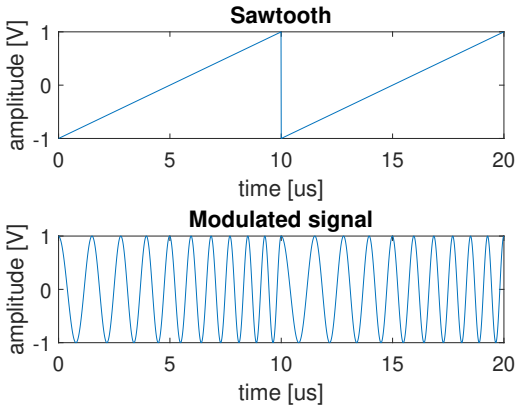


Figure 2.1: The waveform of the sawtooth signal and the modulated signal.

2.2 Frequency-Modulated Continuous-Wave

Frequency-Modulated Continuous-Wave (FMCW) is a special type of FM where the modulation signal is a periodic wave. The reflected signal can be used to estimate the speed and distance to objects. The transmitter and receiver are placed at the same location and the receiver will receive the reflected signal that was sent by the transmitter. When comparing the difference between the received signal and the transmitted signal, the distance can be determined. A visualisation of the relevant parameters is shown in Figure 2.2.

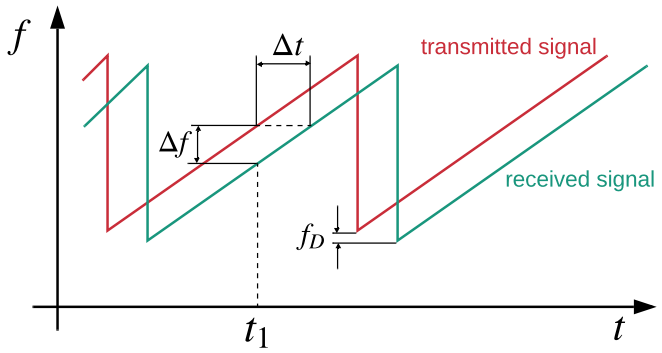


Figure 2.2: The relevant parameters for determining the distance using FMCW.

From Figure 2.2, it can be seen that the received signal has a phase shift compared to the transmitted signal caused by the propagation time. Since the signal is propagating with the speed of light c_0, the distance R can be determined using Equation (2.5) [8].

$$R = \frac{c_0|\Delta t|}{2} = \frac{c_0|\Delta f|}{2\frac{df}{dt}} \tag{2.5}$$

There is a maximal distance that can be measured, given by Equation (2.6), due to the fact that the signal is periodic. This equation is derived in [9, p. 17]. If the phase shift is larger than the period time T, it cannot be distinguished from which period the signal originated.

$$R_{max} = \frac{c_0 T}{2} \tag{2.6}$$

FMCW is not only limited to measuring the distance, but also the speed can be measured. Due to the Doppler effect [10], the frequency spectrum of a signal will shift by an amount of f_D. This frequency shift can be measured and therefore be used to determine the speed. For this project, a sawtooth is used as the modulation signal, for which the Doppler effect has a negligible influence [8] and cannot be distinguished from Δf. Therefore, the transceiver of this project cannot be used to accurately determine the distance of moving objects nor their speed.

3. Programme of Requirements

The goal of the project is to design an FM chirp generator and detector. The application in mind would be to integrate the design in cars for remote sensing applications. The complexity of the design for such an application lies outside the scope of this Bachelor project, since it requires the design to be in the GHz range (FMCW) with IC technology. For educational purposes, the requirements will be simplified. The operational frequency must be in the FM radio band and only discrete components are allowed. Needless to say, the end result of this project will not be near an applicable nor commercially competitive consumer product. The legal limit of power transmission in the FM radio band without a license will therefore also not be considered.

3.1 System requirements

The following specifications and requirements apply to the full transceiver system. The requirements are given by, or derived from, the specifications provided by the project supervisor [1]. Requirements governing the performance of the modules are discussed in the respective parts, and follow from the following:

Functional requirements:

- SYS0: The transceiver must be composed of only discrete components.
- SYS1: Frequency Modulation (FM) must be used.
- SYS2: The modulation signal must be a sawtooth waveform.
- SYS3: The sawtooth waveform must be recoverable over a minimum distance of 5 m.
- SYS4: The receiver must drive the recovered signal over a 50 Ω dummy load.

Non-Functional requirements:

- SYS5: The Radio Frequency (RF) carrier wave must be tuneable from 88 MHz to 108 MHz.
- SYS6: The FM modulation bandwidth must be between 180 kHz and 400 kHz.
- SYS7: The receiver noise figure must be lower than 5 dB.
- SYS8: The Signal-to-Noise Ratio (SNR) at the receiver output must be greater than 30 dB.
- SYS9: The transmitted power must be at least 100 mW.
- SYS10: The transmitter efficiency must be higher than 50%.
- SYS11: The total power consumption of the transceiver must be less than 10 W.
- SYS12: The transceiver must operate on a 12 V power supply.
- SYS13: The antennas provide a 50 Ω resistive load or source impedance.

3.2 Assumptions and disclaimers

- The detected waveform is only used to drive a 50 Ω dummy load. Processing the signals to perform distance measurements is outside the scope of the project.
- Antennas are assumed to be 50 Ω purely resistive: This simplifies the project to fit in the available timespan.
- The specified transmission power in the FM radio band is illegal [11]. However, the design will not be physically realised.
- The power consumption limit and supply voltage are chosen with the idea to be suitable for car applications.

4. Transistor choice

In this project, two types of transistors are being used: a PNP bipolar transistor and NPN bipolar transistors. For the choice of the PNP transistor, only one working PNP bipolar transistor was found in the libraries available, which was the BFQ149 [12]. Its parameters are shown in Table 4.1. In this project, BJTs are used, since they offer a wide selection for many applications and are more suitable for high speed circuits compared to MOSFETs [13]. A disadvantage of BJTs compared to MOSFETs is that BJTs typically use more power, since they need a base current, whereas MOSFETs use a base voltage. Therefore the MOSFET uses almost no current [13].

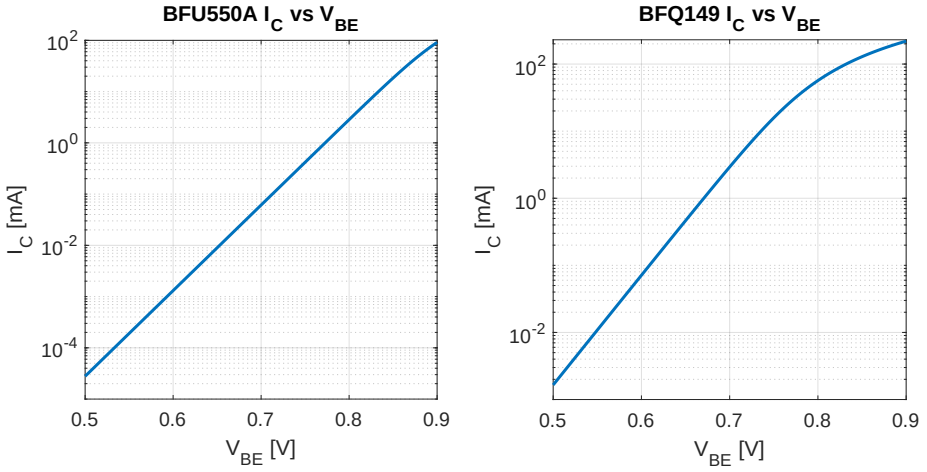
For the choice of the NPN transistor, three different transistors have been considered and compared in Table 4.1. The h_{FE} is defined as the common-emitter current gain while the f_T is the transistor cut-off frequency [14, Ch. 12]. The CE and CB in Table 4.1 refer to the collector-emitter and collector-base voltage respectively.

Table 4.1: Comparison of different transistors. Above are the NPN transistors [15], [16], [17] and below is the PNP transistor [12]

Type	$\mathbf{h_{FE}}$	$\mathbf{f_T}$ **[GHz]**	**Max Current [mA]**	**Max Voltage [V]**	**Price [€]**
BFR92P	100	5	$I_C = 45$, $I_B = 5$	CE = 15, CB = 20	0.46
BFR35AP	100	5	$I_C = 45$, $I_B = 5$	CE = 15, CB = 20	0.37
BFU550A	95	11	$I_C = 50$	CE = 12, CB = 24	0.09
Type	$\mathbf{h_{FE}}$	$\mathbf{f_T}$ **[GHz]**	**Max Current [mA]**	**Max Voltage [V]**	**Price [€]**
BFQ149	50	5	$I_C = 100$	CE = -15, CB = -20	1.35

Since the BFU550A has the highest current rating and it is the cheapest, this transistor is chosen. The maximum voltage ratings are higher than it could encounter during operation, so the lower voltage rating compared to the other two does not influence the decision. A higher current rating is desired, since this provides less restrictions during the design. A cheaper transistor price is also desired, since it will lower the total manufacturing costs.

Before the transistors can be used, the V_{BE} and V_{CE} need to be determined. Since these values are not constant, curves need to be made using ADS, which are shown in Figure F.1 and Figure 4.1.



(a) (b)

Figure 4.1: The I_C vs V_{BE} curve of the: (a) BFU550A and (b) BFQ149 for $V_{CE} = 8$ V.

Part II

Sawtooth generator

5. Introduction

In order to make a chirp signal, the frequency needs to increase linearly. As explained in Chapter 2, a sawtooth signal is therefore required, since the instantaneous frequency changes linearly with the amplitude of the modulation signal. Mathematically speaking, a sawtooth is defined as a linear line, which instantly switches to the minimum value when it reaches the maximum value. Since this is not possible in reality, a sawtooth is defined as a signal with a positive slope and a large negative slope. The difference between a mathematical and a realistic sawtooth waveform is shown in Figure 5.1.

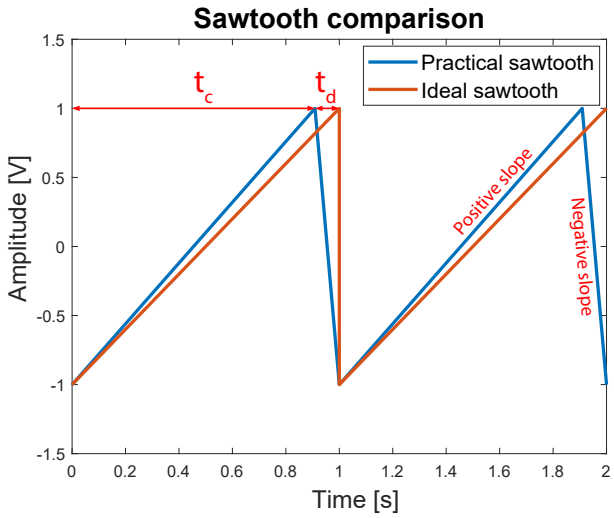


Figure 5.1: The difference between a mathematical sawtooth and a realistic sawtooth.

In this project, the sawtooth signal is generated by charging and discharging a capacitor. The amplitude of the signal is increasing in the charging time (t_c) and decreasing in the discharging time (t_d).

As specified by requirement SG0, the frequency of the sawtooth signal is 10 kHz. Using Equation (2.6), this results in a maximum theoretical range of approximately 15 km. It should be noted that the actual range for this project is much smaller due to the limited output power of the transmitter.

5.1 Requirements

The requirements for the sawtooth generator can be found in Table 5.1. These requirements are defined together with the groups whose modules interface with the sawtooth generator. The derivation of the requirement for the power consumption can be found in Appendix A.

Table 5.1: The requirements for the sawtooth generator

Tag	Description	Value
SG0	Sawtooth frequency	10 kHz
SG1	Sawtooth peak-to-peak voltage	3 V
SG2	Maximum output current	40 μA
SG3	Linearity	$>$ 40 dB
SG4	Power consumption	$<$ 150 mW
SG5	Sawtooth rise/fall ratio	10:1
SG6	Free-running	True

6. Possible implementations

For the sawtooth generator, two possible implementations are considered. The first implementation is an astable multivibrator whose output is coupled to a constant current ramp generator and the second implementation is a constant current ramp generator coupled to a Schmitt trigger and a voltage clamper which form a closed loop, as can be seen in Figure 7.1. The specific sub-modules will be elaborated in Chapter 7.

The astable multivibrator is a circuit, which is often used to produce square wave signals [18, Ch. 8]. The circuit is shown in Figure 6.1. The basic working principle is that two transistors are switching states, creating a square wave at both the collectors of the transistors. If the moment before Q_1 turning on is considered, the voltage across C_2 is $V_{CC} - V_{BE2}$, since Q_1 is not conducting. At the moment when Q_1 switches on, V_{QC1} will be pulled to ground. Since the voltage over C_2 cannot change instantaneously, V_{QB2} will also drop. This turns Q_2 off and the capacitor will slowly start discharging via R_{B2}. When V_{QB2} reaches V_{BE2}, Q_2 will turn on and the same procedure is repeated for Q_1. This pulse shaped output can then be provided to the input of a constant current ramp generator to create a sawtooth signal.

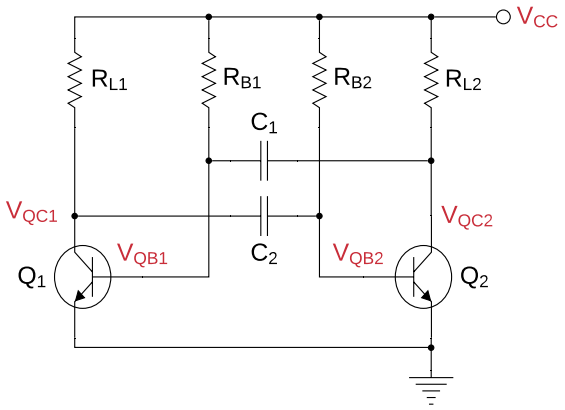


Figure 6.1: A schematic of an astable multivibrator.

A constant current ramp generator is a simple circuit where a constant current charges a capacitor. In parallel with the capacitor, a transistor is placed, which can be turned on in order to discharge the capacitor. This circuit requires a pulse-shaped input signal in order to control the charging and discharging of the capacitor.

6.1 Implementation choice

While both implementations satisfy requirement SG6, the second implementation is chosen. The main reason is that the astable multivibrator with a constant current ramp generator does not have feedback and can be considered an open-loop system. This means that the output could "drift" away if the capacitor is not discharged completely every cycle. This would violate requirements SG0 and SG1.

7. Top-level overview

The sawtooth generator can be divided into three different sub-modules, which are shown in Figure 7.1. Due to the feedback from the voltage clamper, no external input is required. The output of the sawtooth generator is the output of the ramp generator.

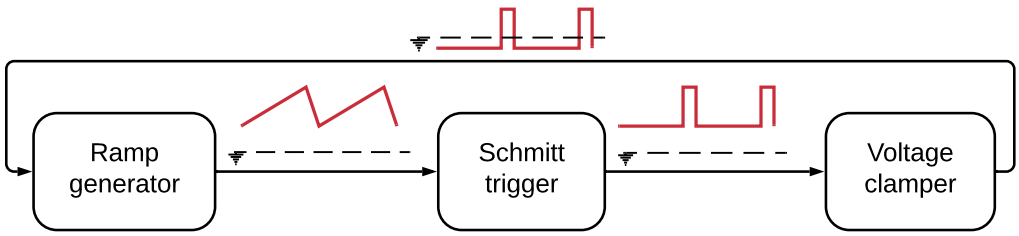


Figure 7.1: An overview of the sawtooth generator.

7.1 Ramp generator

The ramp generator consists of a Constant Current Source (CCS) and a capacitor in parallel with a transistor, as shown in Figure 7.2. The voltage across a capacitor is given in Equation (7.1) and (7.2). If the input voltage V_{in} is low, the transistor will be off, this means that all the current from the current source will flow into the capacitor and therefore start charging the capacitor. The voltage over the capacitor will increase linearly, due to the constant current.

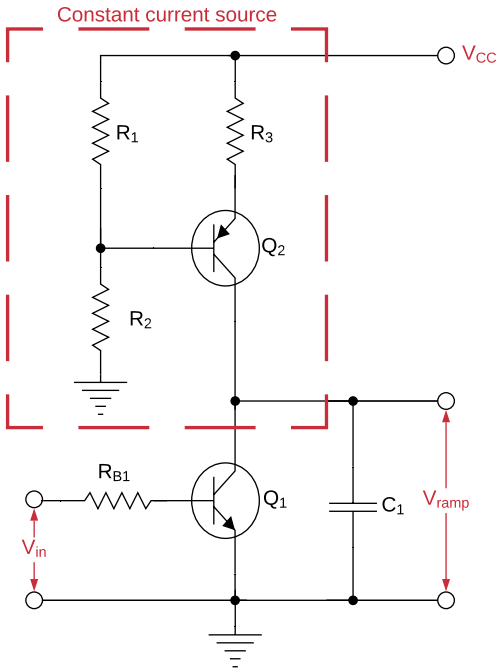


Figure 7.2: The schematic of the ramp generator.

If the input voltage V_{in} is high, the transistor will start conducting and the capacitor will

discharge, since the transistor will act as a very small resistor in parallel with the capacitor.

$$V = \frac{Q}{C} \tag{7.1}$$

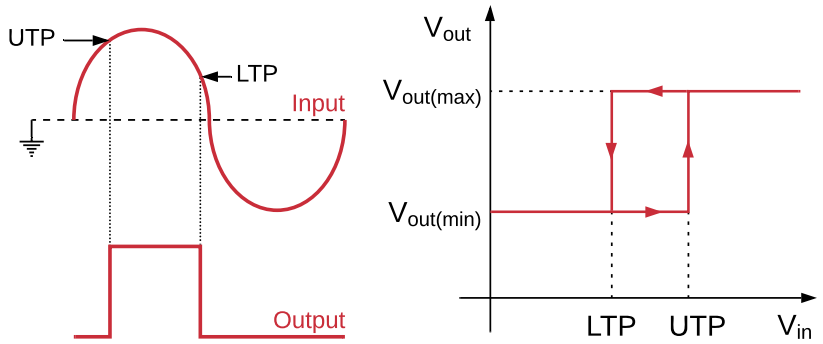
If the current is constant, Equation (7.1) can be rewritten as:

$$V(t) = \frac{I \cdot t}{C} \tag{7.2}$$

In order for the ramp to be linear, the current flowing into the capacitor should be constant [18, Ch. 7]. Therefore, a constant current source is needed, which consists of three resistors and a PNP transistor. Resistors R_1 and R_2 will bias the transistor and set the voltage across resistor R_3. This voltage will create a current through R_3, which is approximately equal to the current flowing into the capacitor. It should be noted that the current is only constant if the transistor stays in forward active mode [19], which means that the voltage of the ramp can never reach the value of V_{CC}.

7.2 Schmitt trigger

The Schmitt trigger will produce a high or low output based on the voltage level of its input. The output becomes high when the Upper Trigger Point (UTP) is reached and will become low when the Lower Trigger Point (LTP) is reached, as shown in Figure 7.3a. Therefore, it is insensitive to small deviations around the threshold value. This input/output relationship is commonly referred to as hysteresis [20], as shown in Figure 7.3b.



(a) (b)

Figure 7.3: (a) The output waveform of a Schmitt trigger for a sinusoidal input and (b) The hysteresis of the Schmitt trigger, where the input/output relationship is dependent on the path.

The transistor implementation is shown in Figure 7.4. There are two states that need to be considered [18, Ch. 6]:

- State 1 - The output is high, which means the LTP is the active threshold value.
- State 2 - The output is low, which means the UTP is the active threshold value.

In State 1, transistor Q_3 is on and transistor Q_4 is off. Therefore, no current flows through Q_4 and R_{L2}, so the output voltage is equal to V_{CC}. Since Q_3 is on, there will be a voltage drop over R_{L1}. This decreases the base voltage of Q_4, which makes the transistor Q_4 go into cut-off since the emitter voltage of Q_4 is higher than the base voltage of Q_4. The LTP is defined as the point at which Q_3 turns off and Q_4 turns on. The full derivation of the LTP can be found in Section 8.2.

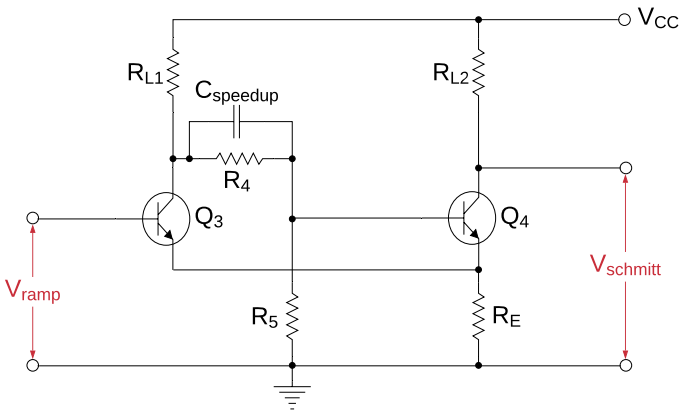


Figure 7.4: The BJT implementation of the Schmitt trigger.

In State 2, transistor Q_3 is off and transistor Q_4 is on. Therefore, current flows through Q_4, which will create a voltage drop over R_{L2}. This makes the output voltage go low. The UTP is defined as the point when Q_3 turns on. The full derivation of the UTP can be found in in Section 8.2.

When the circuit is in State 1 and the input voltage (the ramp voltage) starts decreasing, the current through Q_3 is decreasing. This makes the voltage drop over R_{L1} also decrease, since less current is flowing through this resistor. Therefore, the collector voltage of Q_3 rises, which increases the base voltage of Q_4. At the point where the input voltage equals the base voltage of Q_4 the circuit will switch states and this is defined as the LTP. The capacitor $C_{speedup}$ is placed in parallel with R_4 to allow faster switching time, as explained in [18, Ch. 4]. $C_{speedup}$ will act as a short circuit for high frequency signals, which enables the current to flow faster on the switching moments.

When the circuit is in State 2 and the input voltage starts increasing, transistor Q_3 will turn on, if the input voltage is equal to the emitter voltage of Q_4 plus the base-emitter voltage V_{BE3}. When this point is reached, a current through Q_3 will flow and create a larger voltage drop across R_{L1}. This decreases the collector voltage of Q_3, and therefore also decreases the base voltage of Q_4, causing transistor Q_4 to turn off.

Since the collector voltage of Q_4 is used as the output voltage, the Schmitt trigger is non-inverting. This means that an input voltage larger than UTP corresponds to a high output voltage.

7.3 Voltage clamper

The Schmitt trigger's output voltage is typically between $\frac{1}{2}V_{CC}$ and V_{CC}, which is not suitable as an input for the transistor of the ramp generator, as it would never turn the transistor off. Therefore, a voltage clamper needs to be implemented, which lowers the DC offset. A circuit implementation is shown in Figure 7.5.

The amplitude of the signal will not change, only the DC offset will change, as explained in [18, Ch. 3] and shown in Figure 7.5. If the input voltage changes, the output voltage will increase or decrease with the same amount, since the voltage drop over C_{clamp} cannot change instantaneously. When there is no change, the capacitor will discharge over R_{clamp}, causing the output voltage to decrease. If the values of R_{clamp} and C_{clamp} are chosen correctly, this decrease is negligible compared to the amplitude of the signal.

The diode D_1 will conduct if the output voltage becomes lower than $-V_F$. This makes sure that the output voltage will not become lower than $-V_F$ and that the capacitor will charge to a value of

$V_{low} + V_F$, as shown in Figure 7.5.

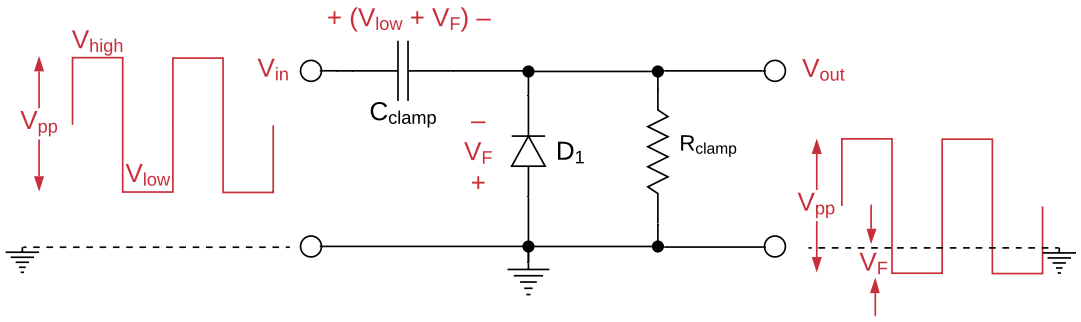


Figure 7.5: The schematic of a clamping circuit together with its input/output characteristic.

7.3.1 Other implementations

Another way to change the DC offset of the Schmitt trigger is by using a buffer with AC coupling. However, this method is not considered, since the buffer would consume extra power. Additionally, AC coupling lowers the DC offset of the pulse waveform to 0 V. This would make the low value of the pulse waveform more negative, resulting in a larger switching time due to the residual charge at the base of the transistor [18, Sec. 4.4]. The voltage clamper prevents the low value of the pulse waveform from going below -V_F, proving to be the better option. A disadvantage of the voltage clamper is that it will produce a tilt on the high value of the output waveform due to the discharging of the capacitor C_{clamp}. However, since the duration of the high value is only a tenth of the duration of the low value, as specified by requirement SG5, this tilt will not have a significant influence on the performance.

8. Sawtooth generator design

In this chapter, the design of the three different sub-modules of the sawtooth generator will be covered. This includes setting up the design equations and determining the component values.

8.1 Ramp generator design

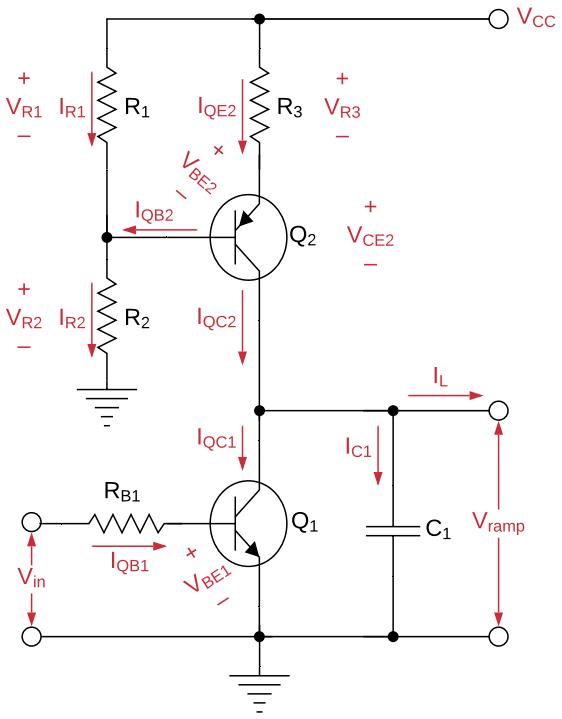


Figure 8.1: The schematic of the constant current ramp generator.

The design in this section is based on the circuit of Figure 8.1. First, the capacitor charging current I_{C1} has to be determined. In order to keep the ramp linear, I_{C1} should remain constant throughout the whole charging time of the capacitor. To ensure that changes in the load current I_L do not affect I_{C1} by a substantial amount, the inequality $I_{C1} \gg I_{L(max)}$ should hold. This is achieved by taking the following approximation:

$$I_{C1} \approx 100 I_{L(max)} \tag{8.1}$$

Knowing that the current through a capacitor is equal to $i(t) = C\frac{dv(t)}{dt}$ and that the charging current is approximately constant, the capacitor value C_1 can be determined using the simplified expression:

$$C_1 = \frac{I_{C1} t_c}{\Delta V} \tag{8.2}$$

Where:

- ΔV - the difference between the maximum and minimum voltage of the sawtooth
- t_c - the charging time of the capacitor equal to the duration of the positive slope

For transistor Q_2 to provide the constant current I_{C1}, the transistor should be operating in the forward active mode. To ensure that the transistor stays in the forward active mode, the voltage V_{CE2} should not fall below 3 V [18]. Using KVL, the voltage drop V_{R3} over resistor R_3 can be determined:

$$V_{R3} = V_{CC} - V_{ramp(max)} - V_{CE2(min)} = V_{CC} - V_{ramp(max)} - 3 \tag{8.3}$$

It should be ensured that V_{R3} is a couple times larger than V_{BE2} in order to prevent deviations in V_{BE2} from having a large influence on the collector current I_{QC2} which is the current provided by the constant current circuit.

Taking the approximation that $I_{QC2} \approx I_{C1}$ and using the fact that $I_{QE2} = I_{QC2} + I_{QB2}$, the necessary resistor value R_3 can be determined:

$$R_3 = \frac{V_{R3}}{I_{QE2}} \approx \frac{V_{R3}}{I_{C1} + I_{QB2}} = \frac{V_{R3}}{I_{C1}(1 + \frac{1}{h_{FE2}})} \tag{8.4}$$

In order to determine the biasing resistor values R_1 and R_2, the voltage drop over R_1 must be known and is calculated as:

$$V_{R1} = V_{R3} + V_{BE2} \tag{8.5}$$

To keep the biasing of transistor Q_2 stable, it should be ensured that $I_{R1} \gg I_{QB2}$. A rule of thumb is to set the current through R_1 ten times larger than the base current I_{QB2}:

$$I_{R1} = 10 I_{QB2} = 10 \frac{I_{QC2}}{h_{FE2}} \approx 10 \frac{I_{C1}}{h_{FE2}} \tag{8.6}$$

In this way, the current I_{QB2} has less influence on the base voltage that is provided by R_1 and R_2.

From the current obtained above, the resistor value R_1 can be determined as:

$$R_1 = \frac{V_{R1}}{I_{R1}} \tag{8.7}$$

The voltage drop over resistor R_2 is then found to be:

$$V_{R2} = V_{CC} - V_{R1} \tag{8.8}$$

Using the voltage V_{R2} found earlier, the resistor value R_2 is determined by:

$$R_2 = \frac{V_{R2}}{I_{R2}} = \frac{V_{R2}}{I_{R1} + I_{QB2}} \tag{8.9}$$

To determine the capacitor discharge current, which is the collector current I_{QC1}, a simplified formula can be used. If the charging current I_{C1} charges the capacitor C_1 in time t_c then to discharge the capacitor in time t_d the discharge current should be $\frac{t_c}{t_d}$ times larger than the charging current I_{C1} [18]. Since the discharging current should also sink the charging current, a more accurate expression is:

$$I_{QC1} \approx \left(1 + \frac{t_c}{t_d}\right) I_{C1} \tag{8.10}$$

The above approximation holds when the charging and discharging currents are constant and the absolute value of ΔV is the same in both cases.

Knowing the collector current I_{QC1}, the base current I_{QB1} can be determined using the relation:

$$I_{QB1} = \frac{I_{QC1}}{h_{FE1}} \tag{8.11}$$

Finally, the base resistance R_{B1} can be determined using the voltage drop over R_{B1} and the base current:

$$R_{B1} = \frac{V_{in(max)} - V_{BE1}}{I_{QB1}} \tag{8.12}$$

Where $V_{in(max)}$ is the maximum voltage at the input of the ramp generator. The derivation of this value is shown in Equation (8.42).

8.2 Schmitt trigger design

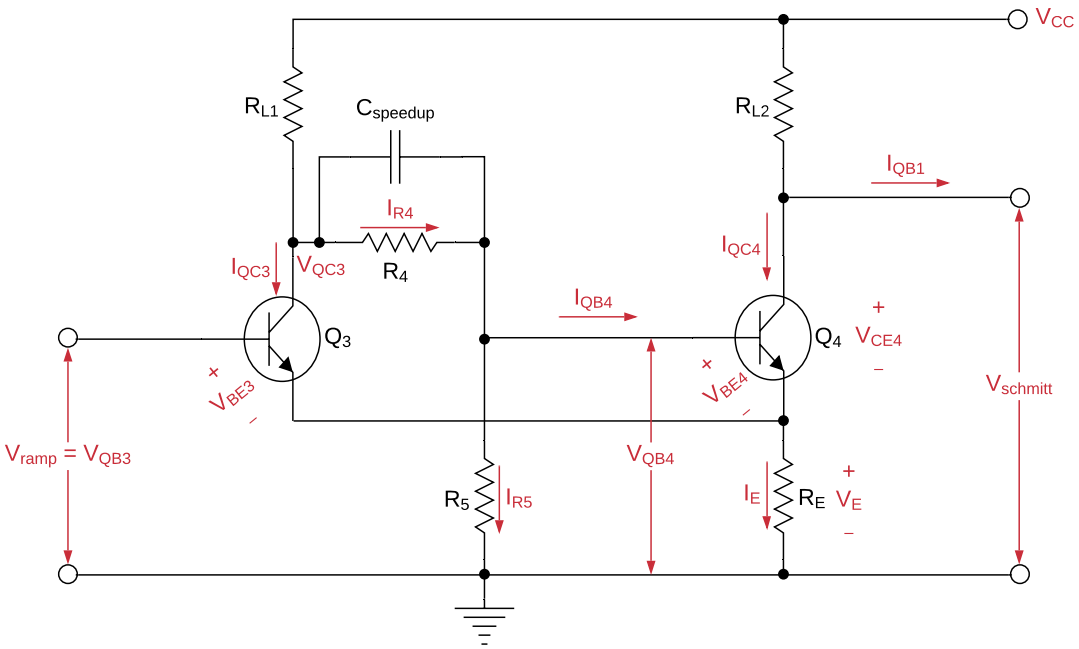


Figure 8.2: The schematic of the Schmitt trigger.

The design of the Schmitt trigger can be split into two parts [21] and is based on the circuit of Figure 8.2. This is possible because the UTP and LTP are almost independent of h_{FE} and the temperature [22].

First, it is assumed that transistor Q_4 is conducting while transistor Q_3 is in cut-off. This means that the design is based around the UTP.

As stated before, at the boundary condition, the following equality holds:

$$V_{QB4} = UTP \tag{8.13}$$

Where UTP is the maximum value of the sawtooth waveform.

Using this knowledge, the voltage drop over resistance R_E is determined:

$$V_E = V_{QB4} - V_{BE4} \tag{8.14}$$

Taking the approximation that $I_E \approx I_{QC4}$, the resistor value R_E can be calculated:

$$R_E = \frac{V_E}{I_E} \approx \frac{V_E}{I_{QC4}} \tag{8.15}$$

Using KVL, the voltage drop over resistor R_{L2} can be determined together with the value of the resistance:

$$R_{L2} = \frac{V_{CC} - V_E - V_{CE4(sat)}}{I_{QC4}} \tag{8.16}$$

In order to determine the values for the voltage divider, consisting of R_4 and R_5, two aspects have to be considered. Firstly, R_4 and R_5 need to be large enough to avoid overloading R_{L1}. If this is not the case then the Q_3 collector current will not have a large impact on V_{QB4} when Q_3 is turned on. Secondly, the values should not be too large because then the current I_{QB4} would create a large voltage drop over R_4 when Q_4 is switched on. A good rule of thumb is [18]:

$$I_{R5} = \frac{1}{10} I_E \approx \frac{1}{10} I_{QC4} \tag{8.17}$$

Using the previously obtained current, the resistor value R_5 is calculated:

$$R_5 = \frac{V_{QB4}}{I_{R5}} = \frac{UTP}{I_{R5}} \tag{8.18}$$

The base current of transistor Q_4 can be obtained using the following relation:

$$I_{QB4} = \frac{I_{QC4}}{h_{FE4}} \tag{8.19}$$

From here, the current through resistor R_4 can be determined as:

$$I_{R4} = I_{R5} + I_{QB4} \tag{8.20}$$

Finally, the voltage drop over the series connection of R_{L1} and R_4 can be calculated:

$$R_{sum} = R_{L1} + R_4 = \frac{V_{CC} - V_{QB4}}{I_{R4}} \tag{8.21}$$

In order to determine the exact values of R_{L1} and R_4, the LTP should be taken into consideration. In all further steps, it is assumed that Q_3 is conducting while Q_4 is in cut-off. As mentioned before, it is known that at the boundary condition $V_{QB3} = V_{QB4} = LTP$. Using this knowledge, the current through resistor R_4 can be calculated:

$$I_{R4} \approx \frac{V_{QB4}}{R_5} = \frac{LTP}{R_5} \tag{8.22}$$

By taking the approximation that $I_{QC3} \approx I_E$, the collector current of Q_3 is found:

$$I_{QC3} \approx I_E = \frac{V_{QB3} - V_{BE3}}{R_E} = \frac{LTP - V_{BE3}}{R_E} \tag{8.23}$$

Using KVL and the fact that $I_{QB4} \approx 0$, the following equation can be formed:

$$V_{CC} = R_{L1}(I_{QC3} + I_{R4}) + I_{R4}(R_4 + R_5) \tag{8.24}$$

From the above equation, the resistor value R_{L1} can be determined:

$$R_{L1} = \frac{V_{CC} - I_4(R_{sum} + R_5)}{I_{QC3}} \tag{8.25}$$

Knowing the value of R_{L1}, the resistance of R_4 is then easily obtained:

$$R_4 = R_{sum} - R_{L1} \tag{8.26}$$

Often in practice, a speed-up capacitor is used to increase the switching speed between the two states. When Q_3 is in cut-off, the equivalent resistance seen from the ports of the capacitor $C_{speedup}$ is equal to:

$$R_{eq} = R_4||(R_{L1} + R_5) \tag{8.27}$$

To be more precise, the above equation is an approximation because the input resistance of Q_4 is in parallel with R_5 but it is very large compared to R_5 so it can be ignored [18].

Finally, the value of the speed-up capacitor $C_{speedup}$ is determined such that it charges to 90% of its final voltage during the interval between switching from Q_4 off to Q_4 on [18]:

$$C_{speedup} = \frac{t_d}{2.3R_{eq}} \tag{8.28}$$

The constant 2.3 from Equation (8.28) comes from the fact that a capacitor needs 2.3τ to charge to 90% of its final voltage.

The last step is to determine the high and low value of the pulse wave that is generated by the Schmitt trigger. The low value is determined as:

$$V_{schmitt(min)} \approx V_{CC} - R_{L2}I_{QC4} \tag{8.29}$$

And the high value as:

$$V_{schmitt(max)} \approx V_{CC} - R_{L2}I_{QB1} \tag{8.30}$$

8.2.1 Restrictions on the UTP and LTP

There are a few restrictions regarding the choice of the UTP and LTP. Obviously, the values have to be between 0 V and V_{CC}, since the threshold values are equal to a possible value of V_{QB4}, which is always between these boundaries.

Another requirement comes from the ramp generator. For the charging current to be constant, the collector voltage of Q_2 (which is the input of the Schmitt trigger), cannot become too high, as it would cause Q_2 to enter saturation mode.

The last requirement is that the ratio of the UTP and LTP can not be too large. This is because both values are determined by different values of V_{QB4}. If State 2 is considered (Q_3 is off and Q_4 is on), V_{QB4} is equal to:

$$V_{QB4} = UTP = \frac{R_5}{R_{L1} + R_4 + R_5}V_{CC} \tag{8.31}$$

In State 1 (where Q_3 is on and Q_4 is off), V_{QB4} is equal to:

$$V_{QB4} = LTP = \frac{R_5}{R_4 + R_5}V_{QC3} \tag{8.32}$$

where V_{QC3} can be written as the following using KVL:

$$V_{QC3} = V_{CC} - R_{L1}\left(I_{QC3} + \frac{V_{QC3}}{R_4 + R_5}\right) \tag{8.33}$$

Rearranging the terms gives:

$$\begin{aligned} V_{QC3}\left(1 + \frac{R_{L1}}{R_4 + R_5}\right) &= V_{CC} - I_{QC3}R_{L1} \\ V_{QC3} = \frac{V_{CC} - I_{QC3}R_{L1}}{1 + \frac{R_{L1}}{R_4+R_5}} &= \frac{(V_{CC} - I_{QC3}R_{L1})(R_4 + R_5)}{R_4 + R_5 + R_{L1}} \end{aligned} \tag{8.34}$$

Combining Equation (8.32) and (8.34) gives:

$$V_{QB4} = LTP = \frac{R_5}{R_{L1} + R_4 + R_5}(V_{CC} - I_{QC3}R_{L1}) \tag{8.35}$$

The ratio of UTP and LTP can be written as:

$$\frac{UTP}{LTP} = \frac{V_{CC}}{V_{CC} - I_{QC3}R_{L1}} \tag{8.36}$$

If this ratio becomes large, it means $I_{QC3}R_{L1}$ will approach V_{CC}. Since $R_{L1}I_{QC3}$ is the voltage drop over R_{L1}, there will be almost no voltage drop over the transistor $Q3$, which is needed for the circuit to work. Therefore the ratio of UTP and LTP cannot be arbitrary.

8.3 Voltage clamper design

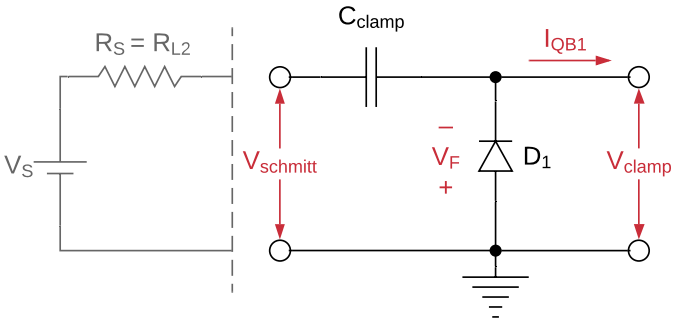


Figure 8.3: The schematic of the clamping circuit.

The clamping circuit, shown in Figure 8.3, is designed such that the capacitor C_{clamp} becomes completely charged during about 5 cycles [18]. A capacitor takes approximately 5 time constants ($\tau = CR$) to charge so:

$$\begin{aligned} 5C_{clamp}R &= 5PW \\ C_{clamp}R &= PW \end{aligned} \tag{8.37}$$

Where PW is the duration of the pulse that forward biases the diode and causes the capacitor to charge.

The resistance R is the sum of the diode forward resistance R_F and the source resistance R_S. Because $R_S \gg R_F$, the Equation (8.37) simplifies to:

$$C_{clamp}R_S = PW \tag{8.38}$$

Knowing that the diode is forward biased during the positive slope of the sawtooth t_c and that the capacitor is charged by the source via the resistor R_{L2}, the capacitor value can be calculated:

$$C_{clamp} = \frac{t_c}{R_{L2}} \tag{8.39}$$

In this case, a discharging resistor for C_{clamp} is not used because the capacitor is being discharged by the base current I_{QB1} of the ramp generator. The voltage drop over the capacitor due to discharging can be determined:

$$\Delta V_{clamp} = \frac{I_{QB1} t_d}{C_{clamp}} \tag{8.40}$$

This voltage difference will cause a tilt in the output voltage of:

$$\text{tilt} = \frac{\Delta V_{clamp}}{V_{schmitt(max)} - V_{schmitt(min)}} \tag{8.41}$$

Knowing that the clamping circuit preserves the amplitude of the input signal but just shifts the low level value to $-V_F$, the maximum voltage can be determined:

$$V_{in(max)} = (V_{schmitt(max)} - V_{schmitt(min)}) - V_F \tag{8.42}$$

This is also the maximum voltage that is presented at the input of the ramp generator.

8.4 Power savings

According to requirement SG4, the power consumption of the sawtooth generator should be lower than 150 mW. In order to lower the power consumption of the sawtooth generator, several design parameters can be changed. It should be noted that changing a design parameter to decrease power will also affect other performance aspects of the circuit.

8.4.1 Base-bias current ratio

As explained in Section 7.1, a transistor is used that acts as a CCS. However, this current is not entirely constant, due to voltage changes at the collector of the transistor. The deviation in the collector current will cause a deviation in the base current I_{QB2} of Figure 8.1. During the design in Section 8.1, it was assumed that $I_{R1} \gg I_{QB2}$. This is achieved by setting $I_{R1} = MI_{QB2}$, where M is a constant. If M is not large enough, I_{QB2} will create a varying voltage over R_2. The voltage over R_2 determines the voltage over R_3, thus determining the current of the current source. A varying voltage of R_2 causes a varying current at the current source. By choosing a higher value of M, the base current I_{QB2} will have less impact on V_{R2}, but it increases I_{R1} causing an increase in power consumption. If the value of M is chosen lower, the power consumption will decrease, but I_{QB2} will have a larger influence on V_{R2}, causing a larger deviation of I_{C1}.

Different values for the current ratio M have been tested and the results are shown in Table 8.1. The current ratio that is chosen is 10, since it can be considered to be the "optimal" value. Lowering the ratio to 5 will substantially increase ΔI while only slightly decreasing the power consumption. Similarly, changing it to 50 will substantially increase the power consumption, whereas the decrease of ΔI is marginal.

Table 8.1: The influence of the base-bias current ratio M on the power consumption and current deviation

Current ratio M	**Power [mW]**	**ΔI [μA]**
5	108.67	138.5
10	114	87
50	138.6	48.8
100	166.1	46.8

8.4.2 Schmitt trigger current

The current flowing out of the Schmitt trigger is used to feed the voltage clamper. The output current, together with I_{QC4}, forms the current that flows through R_{L2}. Allowing I_{QC4} to be larger, will increase the amplitude of the output square wave and decrease the influence of the output current on the minimum output voltage. However, a larger current also increases the power consumption. In Table 8.2, the influence of the current I_{QC4} on the power consumption, the output amplitude and the deviation of the minimum voltage can be seen. I_{QC4} is chosen to be 3 mA, since it uses the least power with a reasonable $\Delta V_{schmitt(min)}$. By increasing I_{QC4}, the power consumption would be too high and for a lower I_{QC4}, the $\Delta V_{schmitt(min)}$ would be too high, resulting in non-accurate calculations.

Table 8.2: The influence of the Schmitt trigger current I_{QC4} on the power consumption, the amplitude of the square wave and the deviation of the minimum output voltage

Current [mA]	**Power [mW]**	**Amplitude [V]**	**$\Delta V_{schmitt(min)}$ [mV]**
1	67	3.3	383
2	79	5.3	139
3	91.5	6.1	84
4	104	6.5	66.9
5	117	6.7	54.4
6	129	6.8	46.8

8.4.3 Load-charging current ratio

The output of the sawtooth generator is attached to the baseband amplifier which acts as a load. Since the output of the sawtooth generator is the voltage over capacitor C_1, the load current is drawn from this capacitor. This means that the actual charging current is $I_{QC2} - I_{load}$. A disadvantage is that the load current is dependent on V_{C1}, which is varying from 2 V till 5 V. This means that I_{load} is not constant, which means that the charging current is also not constant. To minimise this, the charging current is designed to be much larger than I_{load}, such that its effect is negligible. Therefore, I_{QC2} can be written as $I_{QC2} = NI_{load}$, where N is a constant. Choosing this constant large, will increase the linearity[1], but will also increase the power consumption. In Table 8.3, the results are shown for different values of N. Since linearity is an important aspect, the constant N is chosen to be 100. In this way, higher linearity of the sawtooth waveform is ensured while only marginally increasing the power consumption.

Table 8.3: The influence of the load-charging current ratio N on the power consumption and the linearity of the circuit

Current ratio N	**Power [mW]**	**Linearity [dB]**
100	88.37	54.3
90	83.55	54.1
80	78.77	53.7
70	73.88	53.4

8.5 Component values

After the design equations have been derived, the individual component values can be determined. In order to facilitate fast iterations and changes to the circuit, a MATLAB script is made to calculate

[1]The linearity is defined as: $20\log_{10}\left(\frac{\text{amplitude}}{\text{error}}\right)$

the component values based on the defined parameters. This script can be found in Section I.1. The full schematic of the sawtooth generator can be found in Section B.1.

The first parameters that need to be defined are the UTP and LTP. These are set to 5 V and 2 V respectively in order to satisfy requirement SG1. Next is the frequency of the sawtooth which is set to 10 kHz to satisfy requirement SG0. The power supply voltage V_{CC} is set to 12 V which satisfies requirement SYS12. In order to determine the base-emitter voltage V_{BE}, the curves of Figure 4.1 are used. From those curves it is approximated that $V_{BE1} = V_{BE3} = V_{BE4} = 0.8$ V and $V_{BE2} = 0.7$ V which are obtained by looking at the collector current I_{QC} that will flow through the transistors. From the transistor curves of Figure F.1, the collector-emitter saturation voltage is determined to be $V_{CE(sat)} = 0.2$ V. The current gain of the transistors is set to $h_{FE} = 80$ according to the datasheet [17]. Finally, the maximum load current of the sawtooth generator is set to $I_{load(max)} = 40$ μA to satisfy requirement SG2.

With the use of the above mentioned parameters and the use of the design equations from Section 8.1, 8.2 and 8.3, the component values are determined that can be seen in Table 8.4.

Table 8.4: Sawtooth generator calculated component values

	$\mathbf{R_1}$	$\mathbf{R_2}$	$\mathbf{R_3}$	$\mathbf{R_{B1}}$	$\mathbf{C_1}$	$\mathbf{R_{L1}}$
Value	9.4 kΩ	13.27 kΩ	987 Ω	9.4 kΩ	133.33 nF	8.76 kΩ
	$\mathbf{R_{L2}}$	$\mathbf{R_4}$	$\mathbf{C_{speedup}}$	$\mathbf{R_5}$	$\mathbf{R_E}$	$\mathbf{C_{clamp}}$
Value	2.53 kΩ	11.97 kΩ	485.42 pF	16.67 kΩ	1.4 kΩ	35.88 nF

8.5.1 Component selection

Not all component values from Table 8.4 are available. Therefore, standard component values need to be selected. For the selection of components, the search engine Octopart [23] is used. The final values are listed in Table 8.5. For some resistors, the notation "X Ω + Y Ω" is used. This notation indicates that a resistor of X Ω is chosen in series with a variable resistor that has a range from 0 to Y Ω. The need for these variable components is explained in Section 8.5.2. The Bill of Materials (BoM) is listed in Section G.1.

Table 8.5: Sawtooth generator selected component values

	$\mathbf{R_1}$	$\mathbf{R_2}$	$\mathbf{R_3}$	$\mathbf{R_{B1}}$	$\mathbf{C_1}$	$\mathbf{R_{L1}}$
Value	9.4 kΩ	13.3 kΩ	715 Ω + 500 Ω	5 kΩ + 5 kΩ	150 nF	8 kΩ + 2 kΩ
	$\mathbf{R_{L2}}$	$\mathbf{R_4}$	$\mathbf{C_{speedup}}$	$\mathbf{R_5}$	$\mathbf{R_E}$	$\mathbf{C_{clamp}}$
Value	2.52 kΩ	12 kΩ	470 pF	16 kΩ + 5 kΩ	1.4 kΩ	33 nF

8.5.2 Placement of variable components

Since components have standard values, they cannot have the exact values that were calculated. This difference in component values will cause small deviations from the designed parameters. Therefore, several potentiometers are used, such that important parameters can be modified after manufacturing.

Two important parameters are the LTP and UTP. In order to modify these, R_{L1} and R_5 have a potentiometer placed in series since both of these resistors determine the LTP and UTP. This can be confirmed by looking at Equation (8.31) and (8.35).

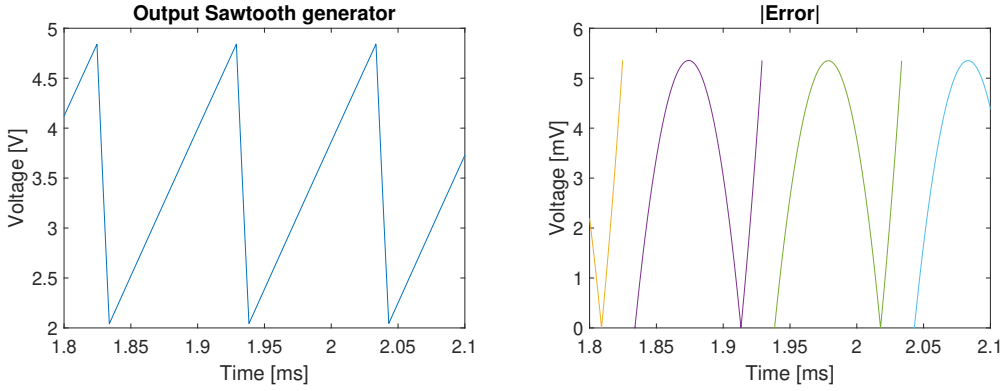
Another important parameter is the frequency of the sawtooth. The frequency is directly determined by t_c and t_d. The t_c is dependent on R_3, as shown by Equation (8.4), where I_{C1} is the charging current. In order to modify t_c, a potentiometer is placed in series with R_3. Similarly, t_d is dependent on R_{B1}, shown by Equation (8.12), where I_{QB1} determines the discharging current. In order to modify t_d, a potentiometer is placed in series with R_{B1}.

9. Simulation results

After designing the circuit, multiple transient simulations are preformed in ADS to ensure that the circuit satisfies the requirements. To simulate requirement SG2, a resistance of 125 kΩ is placed at the output, such that $I_{out(max)} = \frac{5\text{ V}}{125\text{ k}\Omega} = 40\ \mu\text{A}$.

9.1 Simulation using calculated component values

In Figure 9.1a, the output of the sawtooth generator using the calculated component values from Table 8.4 is shown.



(a) (b)

Figure 9.1: (a) The output waveform of the sawtooth generator with calculated values and (b) the absolute error of the output compared to a linear approximation.

Figure 9.1a shows that the output amplitude ranges from 2.05 V to 4.84 V and that the frequency is 9.55 kHz. These results come close to the 3 V and 10 kHz defined by requirement SG1 and SG0. The charging (rise) time is found to be $t_c = 95\ \mu$s and the discharging (fall) time $t_d = 9.7\ \mu$s. This gives a ratio of approximately 10:1 which satisfies requirement SG5.

The absolute error of the simulated sawtooth compared to a theoretical sawtooth is shown in Figure 9.1b. It can be concluded that the maximum absolute error is equal to 5.4 mV, resulting in a linearity[1] of 54.3 dB which satisfies requirement SG3.

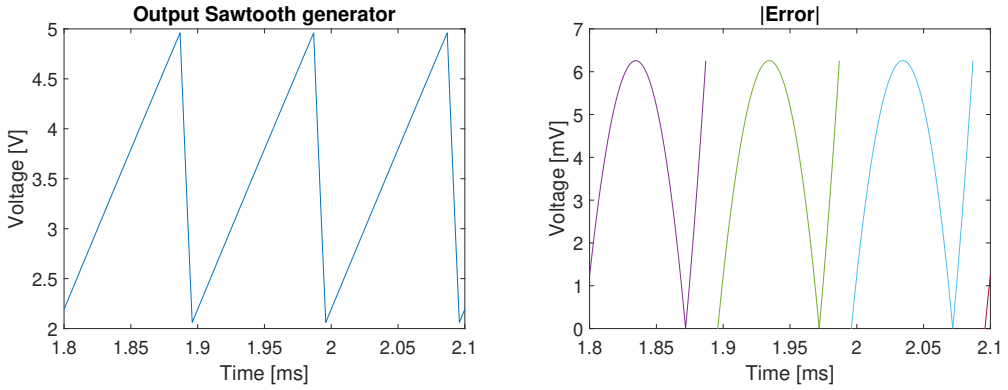
9.2 Simulation using selected component values

Since the calculated values from Table 8.4 are not standard values that can be bought, the circuit was updated with fixed standard values and variable standard values in places that require fine-tuning. The circuit was again simulated using ADS but this time with the values from Table 8.5. The output waveform of the sawtooth generator can be seen in Figure 9.2a.

From Figure 9.2a, it can be concluded that the output amplitude ranges from 2.06 V to 4.96 V and that the frequency is 10 kHz. Both results satisfy requirement SG1 and SG0. The charging time $t_c = 90.9\ \mu$s and the discharging time $t_d = 9.08\ \mu$s give a rise/fall ratio of approximately 10:1 which satisfies requirement SG5.

In Figure 9.2b, the absolute error of the sawtooth waveform compared to a theoretical sawtooth is shown. It can be observed that the maximum absolute error is equal to 6.3 mV, providing a linearity of 53.3 dB which satisfies requirement SG3.

[1] The linearity is defined as: $20\log_{10}\left(\frac{\text{amplitude}}{\text{error}}\right)$



(a) (b)

Figure 9.2: (a) The output waveform of the sawtooth generator with selected components and (b) the absolute error of the output compared to a linear approximation.

The power consumption of the circuit is found to be 102 mW which satisfies requirement SG4.

It can be seen from Table 9.1, that all of the requirements are satisfied. Furthermore, it is shown that the actual results are still reasonable, even though many calculated values are not available. It is also shown that due to the potentiometers, it is possible to achieve more accurate results than using fixed components only, since the frequency, amplitude and rise/fall ratio are easily adjustable during operation.

All the intermediate signals from the three sub-modules of the sawtooth generator can be found in Appendix C. The simulation results of the integration with the baseband amplifier can be found in Section E.1.

Table 9.1: The comparison between the requirements for the sawtooth generator and the results obtained using calculated values and selected values

Tag	**Description**	**Value**	**Calculated values**	**Selected values**
SG0	Sawtooth frequency	10 kHz	9.55 kHz	10 kHz
SG1	Sawtooth peak-to-peak voltage	3 V	2.79 V	2.90 V
SG3	Linearity	> 40 dB	54.3 dB	53.3 dB
SG4	Power consumption	< 150 mW	91.6	102 mW
SG5	Sawtooth rise/fall ratio	10:1	9.79:1	10:1

10. Discussion

The simulations of Chapter 9 are done with exact component values. However, in reality the components can have a small tolerance, as shown in Section G.1, which could affect the performance. As explained in Section 8.5.2, several potentiometers are placed at positions where accurate values are needed in order to compensate for tolerances in component values. This means that if, due to tolerances, the sawtooth waveform has a different frequency or amplitude, it can easily be adjusted to the correct value using the potentiometers.

During the design of the sawtooth generator, several trade-offs have been made. As discussed in Section 8.4, multiple choices can be made to choose between power consumption or linearity. This project has only an educational purpose and has therefore no clear application. If this product would be designed for a specific application, the trade-offs can be made differently in order to have better linearity or lower power consumption.

Requirement SG2 is designed to be the worst-case scenario. This means that, in reality, the output current will be lower than what was simulated in ADS. Since a lower output current will increase the linearity, the actual linearity could be higher than the linearity shown in Table 9.1.

One trade-off from Section 8.4 should be discussed in more detail. The ratio of the charging current and the output current is chosen to be 100, even though other ratios were also reasonable to use. The reason for this, is the fact that the sawtooth generator is at the beginning of the block diagram. Therefore, it is desirable that this part is as linear as possible, since every non-linearity will be propagated to the output of the transceiver.

An important restriction in this project is the time limit. For the project eleven weeks were given, which includes literature study, thesis writing and defence preparation. If more time could be spent on the project, better research can be done and more implementations can be considered.

11. Conclusion

As shown in Table 9.1, all of the requirements are met by the designed circuit. This means that the sawtooth generator is able to generate a sawtooth with an amplitude of 3 V, with a frequency of 10 kHz and with a linearity of 53 dB. Therefore, it can be concluded that the sawtooth generator should work with the rest of the modules without any issue.

11.1 Recommendation and future work

There are several improvements or extensions that can be made for the sawtooth generator. As discussed in Chapter 10, the time limit was an important restriction for the project. Due to the time limit, not all possible implementations could be considered for the sawtooth generator. It is recommended to make an even greater comparison between different sub-modules and their possible implementation.

The linearity of the sawtooth generator could be improved using a different type of CCS since most of the non-linearity is caused by variations in the capacitor charging current in the ramp generator sub-module. Instead of a simple one-transistor current source, a Wilson current mirror, from Section 13.3.2, could be used to reduce the variations in the charging current.

A topic for future work could be the implementation of multiple waveforms. For this project, a sawtooth was used but this is not the only waveform that can be used for FMCW. Other options are a triangular wave, a sine wave or a square wave. Each of these signals has different advantages and disadvantages and therefore it can be useful to switch between different waveforms.

Another topic that can be studied more profoundly is the use of electrical tuning. To modify the frequency and amplitude, several potentiometers were used and those need to be tuned mechanically. An improvement to the design could be to make the amplitude and frequency of the sawtooth electrically tunable by an external voltage source.

More research can be done in the restrictions of the LTP and UTP. As explained in Section 8.2, there is a restriction regarding the ratio of these values. However, for this project, it is not determined what this boundary ratio exactly is. If this ratio is known, the choice of the LTP and UTP could be made differently in order to lower the DC offset or to increase the amplitude, if this would be desired. For this project, however, this is not necessary, since the requirements can still be achieved without knowing the exact boundary ratio.

Finally, since this was the first time that the authors used ADS for simulating a circuit, not all possible simulations could be made in the limited time span. It is recommended that a PCB is designed in order to perform more realistic simulations that take into account the physical properties of the PCB.

Part III

FM detector

12. Introduction

As stated in Chapter 1 and shown in Figure 1.2, the FM detector is located between the IF amplifier and the baseband amplifier. The input signal of the FM detector is an FM signal centred around the IF. To be more precise, the input is a chirp signal, as this is provided by the transmitter. The output of the FM detector should therefore be a sawtooth. To work properly, the FM detector needs to have a linear relationship between the input frequency and the output voltage, as shown in Figure 12.1.

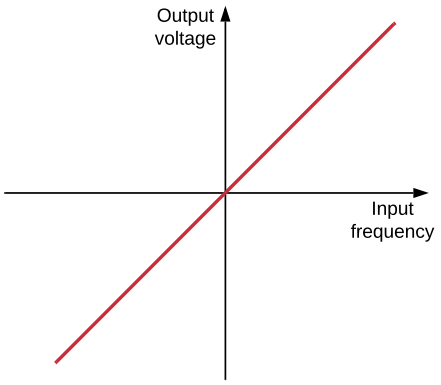


Figure 12.1: The characteristics of an FM detector.

12.1 Requirements

The requirements for the FM detector can be found in Table 12.1. These requirements are established together with other members of the project group in order to define the interface between subsequent modules and to satisfy the system requirements described in Chapter 3. The derivation of the requirement for the power consumption can be found in Appendix A.

Table 12.1: The requirements for the FM detector

Tag	**Description**	**Value**
FMD0	Intermediate Frequency (IF)	10 MHz
FMD1	Maximum frequency deviation	400 kHz
FMD2	Linearity	> 30 dB
FMD3	Peak-to-peak output voltage at maximum input voltage	≥ 1 V
FMD4	Input current draw	< 2 mA
FMD5	Maximum peak-to-peak input	5 V
FMD6	Maximum output current	330 μA
FMD7	Power consumption	< 150 mW

13. Top-level overview

The block diagram of an FM detector can be seen in Figure 13.1. An FM detector can be split into two to three different sub-modules which all perform a different task [24, Ch. 10]. The frequency-to-amplitude converter is used to convert the FM signal to an AM signal. This AM signal is then fed into the envelope detector which will provide a baseband signal at its output equal to the envelope of the AM signal at its input.

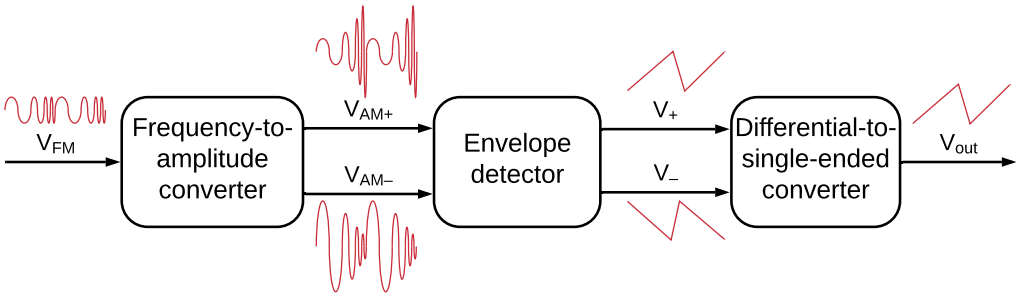


Figure 13.1: The block diagram of an FM detector.

The output signal of the frequency-to-amplitude converter can be single-ended or differential. If a differential signal is used, then the third sub-module is needed to convert the differential signal to a single-ended signal.

13.1 Frequency-to-amplitude converter

The FM signal should be converted into an AM signal, such that the envelope detector can filter out the original signal, as shown in Figure 13.1. There are several methods to achieve this function [25, Sec. 12.3].

13.1.1 Direct differentiation

The direct differentiation method leverages the fact that the current through a capacitor is the derivative of the voltage across it, as can be concluded from Equation 13.1.

$$i_i(t) = C\frac{dv_i(t)}{dt} \tag{13.1}$$

This means that the capacitor will act as a differentiator with the differentiation constant equal to C. The Clarke-Hess frequency demodulator [25] uses this principle in order to demodulate FM signals.

13.1.2 Frequency domain differentiation

In the frequency domain differentiation method, a network is used which has a linear sloping magnitude over the frequency band of interest. The implementation of such a network is normally a filter, due to the frequency-dependent transfer function. In order to filter out frequencies that lie outside the frequency range of interest, a bandpass filter is often used. A bandpass filter can be implemented using a simple RLC circuit, as shown in Figure 13.2.

The working principle is shown in Figure 13.3. The centre frequency of the bandpass filter is slightly higher or lower than the carrier frequency of the FM signal, such that the frequency deviation takes place on the approximately linear part of the magnitude response. Therefore, this frequency-to-amplitude converter is also called a slope detector. If the slope of the filter is approximately linear,

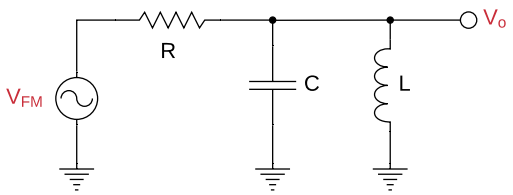


Figure 13.2: A simple RLC circuit implemented as a bandpass filter.

the amplitude of the output will change linearly with the change in frequency, which reassembles Figure 12.1.

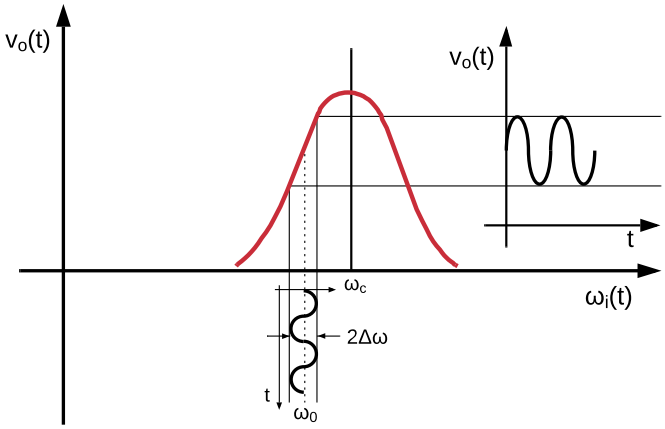


Figure 13.3: The working principle of a slope detector.

13.1.3 Time-delay differentiator

The definition of a derivative is shown in Equation (13.2). A circuit performing the function of a derivative can be made when, from the original signal, a slightly delayed version of itself is subtracted. Finally, the signal is multiplied by $\frac{1}{t_0}$ to provide the necessary scaling. A block diagram implementation of a derivative is shown in Figure 13.4.

$$\frac{dv(t)}{dt} = \lim_{t_0 \to 0} \frac{v(t) - v(t - t_0)}{t_0} \tag{13.2}$$

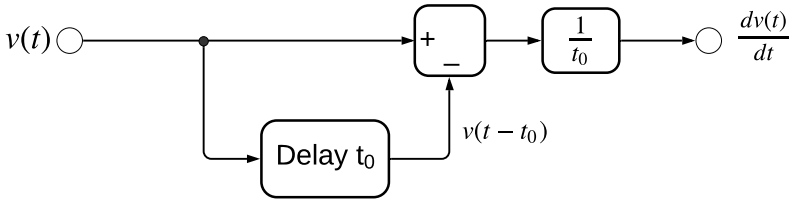


Figure 13.4: A block diagram implementation of a derivative.

A famous implementation of a time-delay differentiator is the Foster-Seeley discriminator [26]. Note that this circuit is a full FM detector that consists of the time-delay differentiator and an envelope detector, as can be seen in Figure 13.5. A slight variation of the Foster-Seeley discriminator is the Ratio detector, which has almost the same working principle. The only difference is that it is less susceptible to AM on the input [27].

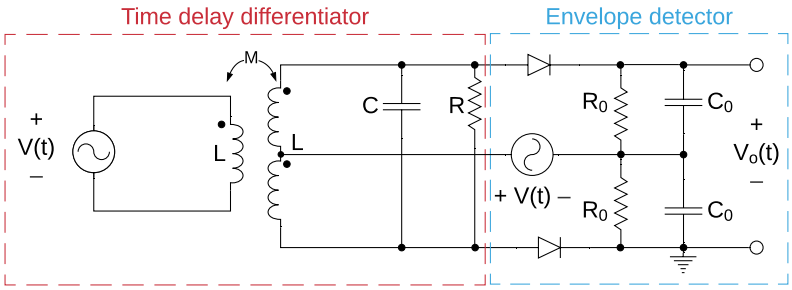


Figure 13.5: The Foster-Seeley discriminator.

The transformer's primary and secondary sides are tuned to the same resonant frequency and the voltage over the top secondary winding is 180° out of phase with the voltage over the bottom secondary winding. If the input frequency is equal to the resonant frequency, the voltage of the top and bottom branch will be equal in magnitude which results in an output voltage of 0 V. If the frequency at the input deviates from the resonant frequency, the voltages of the two branches will not be equal in magnitude and the output voltage will change linearly as a function of the frequency deviation. The working principle of the Foster-Seeley discriminator is more deeply explained in [25, Ch. 12] and [28].

13.1.4 Balanced detectors

In order to improve the characteristics of an FM detector, a balanced implementation can be used. A balanced detector has an output voltage equal to 0 V when $\omega_i(t) = \omega_0$ which is not the case for the non-balanced counterpart. A balanced detector can be implemented by introducing a second detector and taking the difference between the outputs of the two detectors. A balanced circuit is also less sensitive to small amplitude modulations, since both sides are affected the same. The magnitude response of a balanced detector can be seen in Figure 13.6. An implementation of a balanced detector is already shown in Figure 13.5, where the top and bottom branches can be considered to be two separate detectors and the output is taken as the difference between their outputs.

13.1.5 Frequency-to-amplitude converter choice

Before the actual design of the FM detector can start, a choice for the frequency-to-amplitude converter has to be made. Since the maximum frequency deviation is much smaller than the IF, as specified by requirement FMD1 and FMD0 respectively, the slope detector is chosen. The performance of a slope detector decreases for higher frequency deviations. In this case, because the frequency deviation is small, the linearity of the slope detector and its cheap implementation made it the choice of this project. To further improve the linearity and to reduce the effect of small amplitude modulation on the output, a balanced slope detector is chosen.

Even though time-delay differentiators like Foster-Seeley or the Ratio Detector offer better linearity and better AM rejection, they are not suitable for the FM chirp application because they

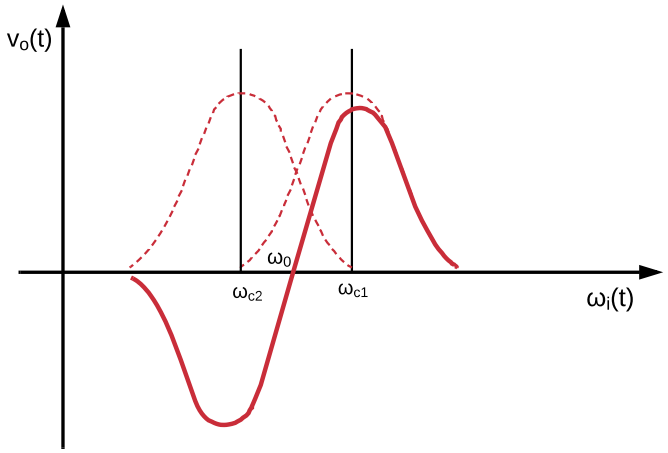


Figure 13.6: The magnitude response of a balanced detector.

introduce a delay [25]. The output signal of the detector will be delayed and this will introduce an error in the determination of the distance to an object.

The direct differentiation method is not chosen, since it transfers a voltage input into a current output. This is not desired because the envelope detector requires a voltage at its input. Additionally, this method does not have a bandpass characteristic. This means that low frequencies and high frequencies far from the IF will also be present at the output, which is not desirable.

13.2 Envelope detector

After the FM signal has been converted to an AM signal, the original signal can be obtained using an envelope detector. An envelope detector consists of a diode and a simple RC circuit, as shown in Figure 13.7.

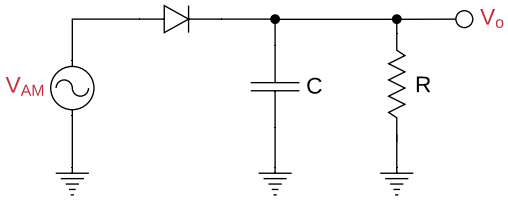


Figure 13.7: The envelope detector.

The function of the diode is to rectify the signal or, in other words, make sure the AM signal can only charge the capacitor. The capacitor will always follow the AM signal if this is higher than the capacitor voltage plus the forward voltage drop over the diode. If the AM signal becomes lower than the capacitor voltage, the capacitor will slowly discharge over the resistor, as shown in Figure 13.8.

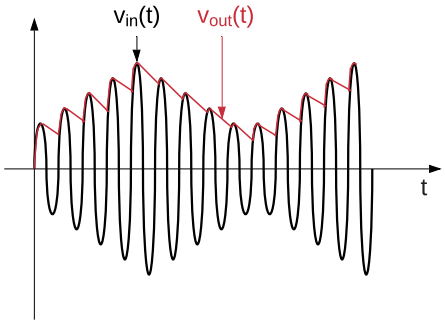


Figure 13.8: The working principle of an envelope detector.

13.3 Differential-to-single-ended converter

The most commonly used differential-to-single-ended converter is the differential pair or the long-tailed pair. A representation of this circuit can be seen in Figure 13.9. The two differential voltages are applied to the base of the two transistors. If both voltages V_+ and V_- are equal, the current of the Constant Current Source (CCS) will be split evenly between both branches and the output voltage will have the value $V_{CC} - \frac{1}{2}IR_C$. If the voltage V_- is increased, the collector current of Q_2 will increase, thus making the output voltage V_{out} decrease. On the other hand, if V_+ increases, it will increase the collector current of Q_1 making the collector current of Q_2 decrease. This will cause the output voltage V_{out} to increase. This basic working principle allows the conversion of differential voltages to a single-ended voltage. The function of R_E is to increase the linear region, as it provides emitter degeneration which reduces the gain of the transistors.

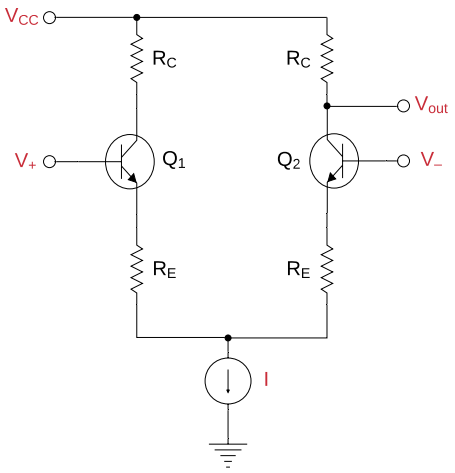


Figure 13.9: The schematic of a differential pair with emitter degeneration.

13.3.1 Current source choice

The four candidates that are considered for the CCS are: current mirror, cascode current mirror, Wilson current mirror and Widlar current mirror. The Widlar current mirror is taken out of consideration because its output current is much lower than its reference current [29], which means that the power consumption would increase drastically. Equation (13.3), (13.4) and (13.5) show

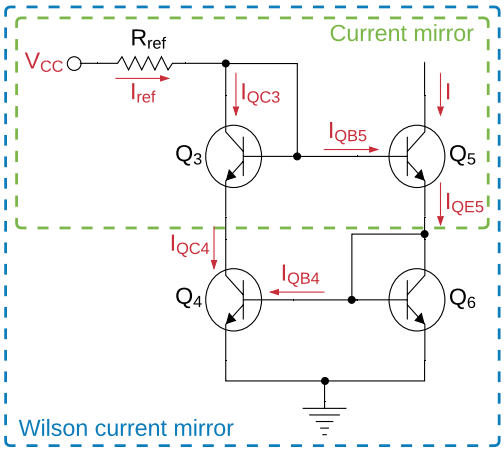


Figure 13.10: The circuit of a Wilson current mirror.

the systematic gain error for the current mirror, cascode current mirror and Wilson current mirror respectively [30]. From those equations, it can be concluded that the Wilson current mirror has the smallest error for finite h_{FE} resulting in a more constant output current. This is the reason why the Wilson current mirror is chosen.

$$\epsilon_{mirror} \approx \frac{V_{CE2} - V_{CE1}}{V_A} - \frac{1 + \frac{I_{S2}}{I_{S1}}}{h_{FE}} \tag{13.3}$$

$$\epsilon_{cascode} \approx -\frac{4}{h_{FE} + 4} \tag{13.4}$$

$$\epsilon_{Wilson} \approx -\frac{2}{h_{FE}^2 + 2h_{FE} + 2} \tag{13.5}$$

13.3.2 Wilson current mirror

To implement a CCS, a current mirror is often used. A current mirror is a two-port device, which mirrors the current from the input port to the output port [30, Sec. 4.2]. The working principle of a current mirror is deeply explained in [30, Sec. 4.2], but the main takeaway is that the base-emitter voltage of one transistor is copied onto the other, forcing them to have the same collector current.

The main limitation of the current mirror is that the output current is dependent on the current gain h_{FE} that is not constant and also dependent on temperature. To reduce the error caused by this dependence, a Wilson current mirror can be used. The Wilson current mirror is an extension of the current mirror, as shown in Figure 13.10.

The fundamental reason why the Wilson current mirror has a better performance is because it provides feedback. For example, if the output current I decreases, the current I_{QE5} will decrease as well. This decrease will cause the base current I_{QB4} to decrease which in turn decreases the collector current I_{QC4}. The decrease of I_{QC4} will also cause I_{QC3} to decrease. Since the reference current I_{ref} is constant, this will cause the base current I_{QB5} to increase which will counteract the initial decrease of the output current I. For a more in-depth explanation, the reader is referred to [30, Sec. 4.2.6]. A requirement for the Wilson current mirror, to ensure a constant current, is that all transistors need to be in the forward active mode. This requires that the voltage at the output port is higher than $V_{BE6} + V_{CE5(sat)}$. Another requirement is that all the transistors must have the same parameters, such that the same V_{BE} will result in the same collector current I_{QC} for all transistors.

14. FM detector design

In this chapter, the design of the three different sub-modules of the FM detector will be covered. This includes setting up the design equations and determining the component values.

14.1 Balanced slope detector design

A balanced slope detector, also known as Travis detector [31], consists of two bandpass filters both centred at different frequencies that convert the FM signal to two AM signals. After the conversion, the AM signals are then passed through two envelope detectors that will provide a baseband output. Therefore, the design will be split into two parts, as seen in Figure 14.1.

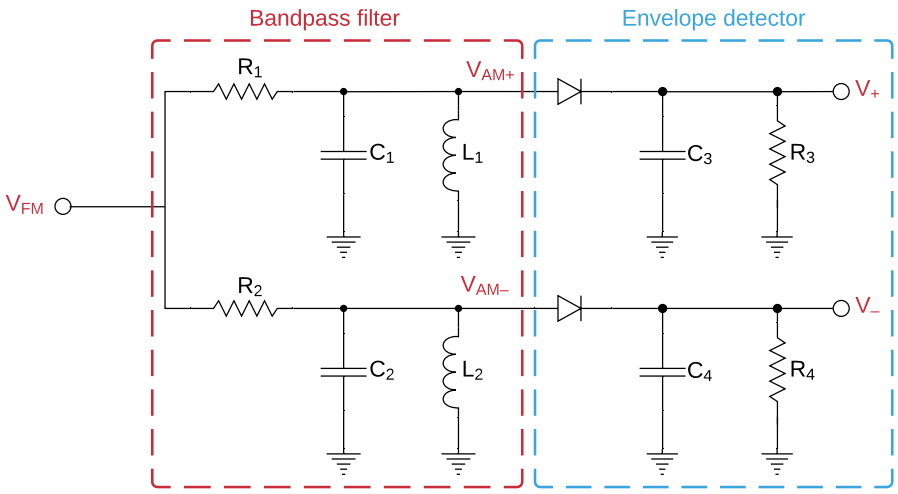


Figure 14.1: The schematic of a balanced slope detector.

14.1.1 Bandpass filter design

The differential output voltage of the bandpass filter can be expressed as:

$$\begin{aligned} v_o(t) &= V_{AM+}(t) - V_{AM-}(t) \\ v_o(t) &= V_{FM}|H_1[j\omega]| - V_{FM}|H_2[j\omega]| \\ v_o(t) &= V_{FM}|H_T[j\omega]| \end{aligned} \tag{14.1}$$

Where $|H_T[j\omega]|$ is the total magnitude response consisting of the two magnitude responses from the bandpass filters:

$$|H_T[j\omega]| = |H_1[j\omega]| - |H_2[j\omega]| \tag{14.2}$$

Combining the two bandpass filters will give a magnitude response with an odd symmetry around ω_0. Taylor expansion around the intermediate frequency ω_0 gives:

$$|H_T[j\omega]| = |H_T[j\omega_0]|'(\omega - \omega_0) + |H_T[j\omega_0]|'''\frac{(\omega-\omega_0)^3}{3!} + |H_T[j\omega_0]|^V\frac{(\omega-\omega_0)^5}{5!} + ... \tag{14.3}$$

Note that only odd order terms are present due to the odd symmetry around ω_0.

If $Q > 10$ for both the bandpass filters then the total magnitude response can closely be represented as:

$$|H_T[j\omega]| = \frac{1}{\sqrt{1+\left(\frac{\omega-\omega_{c1}}{\alpha_1}\right)^2}} - \frac{1}{\sqrt{1+\left(\frac{\omega-\omega_{c2}}{\alpha_2}\right)^2}} \tag{14.4}$$

with:

$$\alpha_{1,2} = \frac{1}{2R_{1,2}C_{1,2}} = \frac{BW_{1,2}}{2} \tag{14.5}$$

Equation (14.4) is derived via a method described in [25, Sec. 2.2]. In order to ensure that $v_o(t) = 0$ V for $\omega_i(t) = \omega_0$, the total magnitude response at the intermediate frequency $|H_T[j\omega_0]|$ should be zero. This is achieved by taking $\alpha_1 = \alpha_2 = \alpha$, $\omega_{c1} = \omega_0 + \delta\omega$ and $\omega_{c2} = \omega_0 - \delta\omega$.

The next step is to determine the value of the frequency difference $\delta\omega$. In order to achieve maximum linearity, the third order term $|H_T[j\omega_0]|'''$ should be equal to zero:

$$|H_T[j\omega_0]|''' = \frac{-3(2\Omega_1^3 - 3\Omega_1)}{\alpha^3(1+\Omega_1^2)^{\frac{7}{2}}} + \frac{3(2\Omega_2^3 - 3\Omega_2)}{\alpha^3(1+\Omega_2^2)^{\frac{7}{2}}} = 0 \tag{14.6}$$

where $\Omega_{1,2} = \frac{(\omega_0 - \omega_{c1,2})}{\alpha}$. This results in two conditions:

$$-2\Omega_1^3 + 3\Omega_1 = 0 \quad \text{and} \quad 2\Omega_2^3 - 3\Omega_2 = 0 \tag{14.7}$$

Substituting the definition of $\Omega_{1,2}$ and using the definition $\omega_{c1,2} = \omega_0 \pm \delta\omega$, the frequency difference $\delta\omega$ is determined as:

$$\delta\omega = \sqrt{\frac{3}{2}}\alpha \tag{14.8}$$

Taking the required derivatives and substituting all the obtained values into Equation (14.3), the following equation is obtained (note the disappearance of the third order term):

$$|H_T[j\omega]| = \frac{4}{5}\sqrt{\frac{3}{5}}\left[\frac{\omega-\omega_0}{\alpha} - \frac{54}{625}\left(\frac{\omega-\omega_0}{\alpha}\right)^5 + ...\right] \tag{14.9}$$

Requiring that the fifth order term is less than 1% of the first order term, the following inequality is obtained:

$$\frac{\Delta\omega}{\alpha} \leq 0.584 \tag{14.10}$$

Where $\Delta\omega = \omega - \omega_0$. However, a value of $\frac{\Delta\omega}{\alpha} = 0.584$ puts a strain on the quasi-static approximation [25]. Therefore, it is commonly chosen as:

$$\begin{aligned} \frac{\Delta\omega}{\alpha} &= \frac{1}{2} \\ \alpha &= 2\Delta\omega \end{aligned} \tag{14.11}$$

The final equation necessary to design the bandpass filters is the centre (resonant) frequency $\omega_c = \frac{1}{\sqrt{LC}}$. Since the two bandpass filters have different centre frequencies, the values for the inductors will not be the same. By fixing one parameter of the circuit, the rest can be calculated using Equation (14.12), (14.13) and (14.14).

$$C_{1,2} = \frac{1}{2\alpha_{1,2}R_{1,2}} = \frac{1}{4\Delta\omega R} \tag{14.12}$$

$$L_1 = \frac{1}{\omega_{c1}^2 C_1} = \frac{1}{(\omega_0 + \sqrt{6}\Delta\omega)^2 C_1} \tag{14.13}$$

$$L_2 = \frac{1}{\omega_{c2}^2 C_2} = \frac{1}{(\omega_0 - \sqrt{6}\Delta\omega)^2 C_2} \tag{14.14}$$

Knowing that the quality factor of a parallel RLC circuit is $Q = \omega_c RC$ and using Equation (14.12), the quality factor can be rewritten to:

$$Q = \frac{\omega_c}{4\Delta\omega} \tag{14.15}$$

From Equation (14.15), it can be concluded that the quality factor of the filters should be decreased if it is desired to increase the linear region $\Delta\omega$ of the detector. Keep in mind that the quality factor should not fall bellow 10 or else the approximation of Equation (14.4) does not hold.

14.1.2 Envelope detector design

The envelope detector can be seen as a half-wave rectifier connected to a low pass filter. The main design problem is centred around choosing the correct value for the resistor and capacitor or, in other words, choosing the cut-off frequency of the low pass filter. A trade-off has to be made between the amount of ripple at the output and the ability to follow the waveform at steep slopes. In particular, it should be ensured that the inequality of Equation (14.16) holds.

$$f_m \ll \frac{1}{2\pi\tau} \ll f_c \tag{14.16}$$

Where:

- f_m - the bandlimited frequency of the modulation signal
- τ - the time constant of the RC network
- f_c - the carrier frequency

The inequality of Equation (14.16) becomes difficult to satisfy when the modulation signal is a sawtooth. A sawtooth has a high number of harmonics because of the sharp negative slope causing the bandlimited frequency to become multiple times higher than the fundamental frequency. Meaning that, if good following of the waveform at sharp slopes is desired, the ripple of the output voltage will have to be higher. Good following of the waveform is achieved when the inequality of Equation (14.17) is satisfied [32].

$$\frac{dv_{env}(t)}{dt} \geq -\frac{v_{env}(t)}{RC} = -\frac{v_{env}(t)}{\tau} \tag{14.17}$$

With:

$$\frac{dv_{env}(t)}{dt} \approx \frac{\Delta v_{env}}{\Delta t} = \frac{v_{env(min)} - v_{env(max)}}{\Delta t} \tag{14.18}$$

Where $v_{env}(t)$ is the envelope of the AM input signal.

If the boundary condition is taken, to keep the ripple minimal, and the worst-case input voltage is used $v_{env}(t) = V_{in(max)}$ then the maximum time constant τ_{max} can be determined using Equation (14.19).

$$\tau_{max} = -\frac{V_{in(max)}}{\frac{dv_{env}(t)}{dt}} \tag{14.19}$$

With the time constant τ known, the maximum peak-to-peak output ripple can be determined using Equation (14.20) [32].

$$\Delta v_{out} = \frac{V_{in(max)}}{f_c RC} = \frac{V_{in(max)}}{f_c \tau} \tag{14.20}$$

In Table 14.1, several different values of τ have been compared. Note that there are two different capacitor discharging slopes for the two different envelope detectors, as seen in Figure D.2. This means that both envelope detector have a different boundary. As shown in Equation (14.20), τ is desired to be as large as possible, since it minimises the ripple. For the positive envelope detector, the slope is $\frac{dv_{env}(t)}{dt} = -\frac{V_{env}}{t_d}$ and for the negative envelope detector it is $\frac{dv_{env}(t)}{dt} = -\frac{V_{env}}{t_c}$. Where V_{env} is the peak-to-peak voltage of the envelope of the input AM signal. The values for the peak-to-peak voltage and slope, as seen in Table 14.1, are obtained from Figure D.2.

Table 14.1: The comparison of different time constants τ

Positive envelope detector		**Negative envelope detector**	
V_{env}	0.41 V	V_{env}	0.41 V
$\frac{dv_{env}(t)}{dt}$	$-4.52 \cdot 10^4$ V/s	$\frac{dv_{env}(t)}{dt}$	$-4.48 \cdot 10^3$ V/s
τ_{max}	$2.79 \cdot 10^{-5}$ s	τ_{max}	$2.81 \cdot 10^{-4}$ s
Ripple for $1.0\tau_{max}$	1.10%	Ripple for $1.0\tau_{max}$	0.110%
Ripple for $0.9\tau_{max}$	1.22%	Ripple for $0.9\tau_{max}$	0.122%
Ripple for $0.8\tau_{max}$	1.38%	Ripple for $0.8\tau_{max}$	0.138%
Ripple for $0.7\tau_{max}$	1.57%	Ripple for $0.7\tau_{max}$	0.157%

For the choice of the time constant, taking τ_{max} is not optimal, since this is a critical upper bound that should not be crossed. To ensure that the boundary is always met, for both envelope detectors a time constant of $0.9\tau_{max}$ is chosen. In this way, some headroom is left to account for inaccuracies in component values. This means that the ripple is 1.2% for the positive envelope detector and 0.12 % for the negative envelope detector. Since both of these values are acceptable, they will be used in the component selection. It should be noted that for the envelope detectors, a different τ is chosen, since the negative envelope detector has a higher boundary, thus giving the possibility of reducing the ripple more than for the positive envelope detector.

14.2 Differential-to-single-ended converter design

The schematic of the differential-to-single-ended converter on which the design is based is shown in Figure 14.2. A resistive load R_C and emitter degeneration resistor R_E are used since the input voltage difference is much larger than the thermal voltage V_T [30]. If emitter degeneration and resistive loads are not used, the output would be clipping due to the high gain of the transistors. In the following steps, an ideal current source is used to simplify the design. At the end of this section, the Wilson current mirror will be added to complete the design.

By applying KCL to the circuit, the following equations can be derived:

$$\frac{V_{QE1} - V_1}{R_E} + \frac{V_{QE2} - V_1}{R_E} = I \tag{14.21}$$

$$\frac{2V_1}{R_E} = \frac{V_{QE1}}{R_E} + \frac{V_{QE2}}{R_E} - I \tag{14.22}$$

$$V_1 = \frac{1}{2}(V_{QE1} + V_{QE2} - IR_E) \tag{14.23}$$

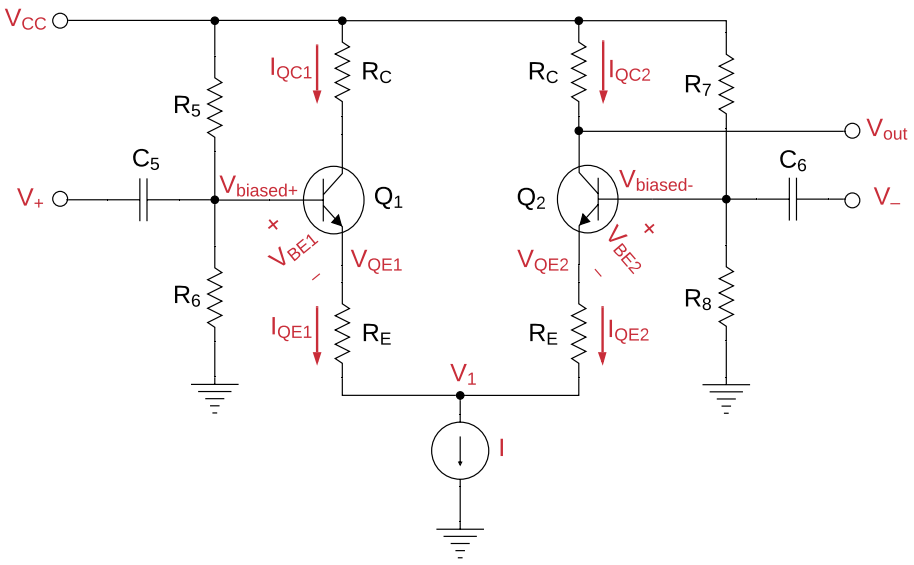


Figure 14.2: The schematic of the differential-to-single-ended converter.

where $V_{QE1} = V_{biased+} - V_{BE1}$ and $V_{QE2} = V_{biased-} - V_{BE2}$.

The output voltage of the differential-to-single-ended converter is given by:

$$V_{out} = V_{CC} - I_{QC2}R_C \tag{14.24}$$

Taking the approximation that $I_{QC2} \approx I_{QE2}$ and making use of Equation (14.23) yields in the following expression:

$$I_{QC2} \approx I_{QE2} = \frac{V_{QE2} - V_1}{R_E} = \frac{V_{QE2} - \frac{1}{2}(V_{QE1} + V_{QE2} - IR_E)}{R_E} = \frac{V_{QE2} - V_{QE1} + IR_E}{2R_E} \tag{14.25}$$

Finally, substituting Equation (14.25) into Equation (14.24) results in:

$$V_{out} = V_{CC} - \frac{R_C}{2R_E}(V_{QE2} - V_{QE1} + IR_E) \tag{14.26}$$

$$V_{out} = V_{CC} - \frac{IR_C}{2} + \frac{R_C}{2R_E}(V_{QE1} - V_{QE2}) \tag{14.27}$$

It can be seen from Equation (14.27) that the output voltage is linearly and positively related to V_{QE1} and linearly and negatively related to V_{QE2}. Knowing that $V_{QE1} = V_{biased+} - V_{BE1}$, $V_{QE2} = V_{biased-} - V_{BE2}$ and that $V_{biased+}$ and $V_{biased-}$ are just V_+ and V_- with different DC offsets respectively, results in an single-ended output voltage that is proportional to the difference of the two input voltages V_+ and V_-. This confirms that the circuit of Figure 14.2 indeed represents a differential-to-single-ended converter.

Resistors R_5, R_6, R_7 and R_8 are used to bias the differential pair. As explained in Section 13.3.2, the voltage over the CCS cannot be lower than $V_{BE6} + V_{CE5(sat)}$. Therefore, the transistors are biased to ensure that $V_1 > V_{BE6} + V_{CE5(sat)}$.

14.2.1 Wilson current mirror design

The output current of the Wilson current mirror from Figure 13.10 can be adjusted by changing the value of R_{ref}. The CCS current can be expressed using Equation (14.28).

$$I = I_{ref} = \frac{V_{CC} - 2V_{BE}}{R_{ref}} \tag{14.28}$$

As specified by requirement FMD6, the maximum output (load) current is 330 μA. To make the output voltage independent of the output current, the CCS current I needs to be designed such that it is much larger than $I_{out(max)}$. A downside of making the current I larger is that it will cause a larger power consumption, as shown in Table 14.2.

Table 14.2: The effect of the CCS current I on the power consumption of the FM detector

I [mA]	**Current ratio**	**Power [mW]**
1	3	12
5	15	60
10	30	120

A value of 5 mA is chosen, since it holds that $I \gg I_{out(max)}$ while not increasing the power consumption by a substantial amount.

14.2.2 Boundaries for component values

In order to ensure that the circuit will work properly in the operating range, boundaries need to be determined for the component values.

One boundary is the fact that the output cannot exceed V_{CC}. The effect this has on the value of R_E is shown in Equation (14.30).

$$\begin{aligned} &V_{out} \leq V_{CC} \\ &V_{CC} - \frac{IR_C}{2} + \frac{R_C}{2R_E}(V_{QE1} - V_{QE2}) \leq V_{CC} \\ &\frac{IR_C}{2} \geq (V_{QE1} - V_{QE2})\frac{R_C}{2R_E} \end{aligned} \tag{14.29}$$

$$I \geq \frac{V_{diff}}{R_E} \tag{14.30}$$

where $V_{diff} = V_{QE1} - V_{QE2}$. Since Equation (14.30) needs to hold during the operation of the circuit, the lower boundary for R_E is obtained when rewriting Equation (14.30) into Equation (14.31). This equation is commonly found in literature covering differential pairs with emitter degeneration [30, p. 216].

$$R_E > \frac{V_{diff(max)}}{I} \tag{14.31}$$

Another boundary for R_E is imposed because V_1 cannot fall below a certain value, since it will saturate the CCS from Section 13.3.2. To prevent this from happening, it should be ensured that $V_1 > V_{BE6} + V_{CE5(sat)}$ which provides an upper boundary for R_E. Together with Equation (14.23),

Equation (14.33) can be derived.

$$\begin{aligned} &V_{1(min)} > V_{BE6} + V_{CE5(sat)} \\ &\frac{1}{2}(V_{QE1(min)} + V_{QE2(min)} - IR_E) > V_{BE6} + V_{CE5(sat)} \\ &\frac{1}{2}(V_{QE1(min)} + V_{QE2(min)}) - V_{BE6} - V_{CE5(sat)} > \frac{IR_E}{2} \end{aligned} \tag{14.32}$$

$$R_E < \frac{V_{QE1(min)} + V_{QE2(min)} - 2V_{BE6} - 2V_{CE5(sat)}}{I} \tag{14.33}$$

Finally, it should be ensured that Q_1 and Q_2 are always operating in the forward active mode. Due to symmetry, only Q_1 is considered, but the same applies for Q_2. To prevent Q_1 from going into saturation, the collector-emitter voltage of Q_1 should not fall below $V_{CE1(sat)}$. In other words, the resistor R_C has an upper boundary as show in Equation (14.35).

$$\begin{aligned} &V_{CC} - IR_C > V_{QE1(max)} + V_{CE1(sat)} \\ &IR_C < V_{CC} - V_{QE1(max)} - V_{CE1(sat)} \end{aligned} \tag{14.34}$$

$$R_C < \frac{V_{CC} - V_{QE1(max)} - V_{CE1(sat)}}{I} \tag{14.35}$$

14.3 Component values

After the design equations have been set up, a MATLAB script has been written to generate values for the bandpass filters. This script can be found in Section I.2. For the full schematic of the FM detector, the reader is referred to Section B.2. As specified by requirement FMD0 and FMD1, the IF frequency is set to 10 MHz and the frequency deviation is set to 400 kHz. Since the resistor values of the bandpass filters are free to choose, the value of R_1 and R_2 is set to 2 kΩ in order to decrease the current draw such that it satisfies requirement FMD4.

For the positive envelope detector, a time constant of $\tau = 2.51 \cdot 10^{-5}$ s is chosen while, for the negative envelope detector, a time constant of $\tau = 2.53 \cdot 10^{-4}$ s is chosen. The choice for the time constants is elaborated in Section 14.1.2. According to [25, Ch. 12], the capacitors impedance needs to have a large value at the message frequency. A value of 400 pF is chosen, such that the impedance at 10 kHz is $|Z| = \frac{1}{2\pi \cdot 10 \cdot 10^3 \cdot C} \approx 40k\Omega$, which is considered to be large enough to not load the circuit substantially. The values for R_3 and R_4 that correspond to the time constants mentioned above are shown in Table 14.3.

For the differential-to-single-ended converter, the current of the Wilson current mirror is designed to be 5 mA. This ensures that the current of the CCS is much larger than 330 uA, which is the maximum output load current as specified by requirement FMD6. In this way, the influence of the output current on the operation of the circuit can be neglected. Using Equation (14.28), the value of R_{ref} can be determined which can be found in Table 14.3. Using Equations (14.31), (14.33) and (14.35), the following restrictions for R_E and R_C can be made:

$$\begin{aligned} 100\ \Omega < R_E < 1.94\ \text{k}\Omega \\ R_C < 1.16\ \text{k}\Omega \end{aligned} \tag{14.36}$$

The coupling capacitors C_5 and C_6 are designed such that they have a 1 Ω impedance at 40 kHz (the fourth harmonic of the sawtooth) causing them to behave as a DC block. The bias resistors R_5, R_6, R_7 and R_8 are chosen to be 50 kΩ in order to keep the DC base voltage at 6 V. This will prevent the Wilson current mirror from saturating due to low voltage at the collector of Q_5. All the calculated component values for the FM detector are listed in Table 14.3.

Table 14.3: The calculated component values for the FM detector. The notation (2x) indicates that two components have the same name

	$\mathbf{R_1}$	$\mathbf{R_2}$	$\mathbf{C_1}$	$\mathbf{C_2}$	$\mathbf{L_1}$	$\mathbf{L_2}$
Value	2 kΩ	2 kΩ	99.47 pF	99.47 pF	2.31 μH	2.82 μH
	$\mathbf{R_3}$	$\mathbf{R_4}$	$\mathbf{C_3}$	$\mathbf{C_4}$	$\mathbf{R_5}$	$\mathbf{R_6}$
Value	62.7 kΩ	632 kΩ	400 pF	400 pF	50 kΩ	50 kΩ
	$\mathbf{R_7}$	$\mathbf{R_8}$	$\mathbf{R_C(2x)}$	$\mathbf{R_E}$ **(2x)**	$\mathbf{R_{ref}}$	$\mathbf{C_{5,6}}$
Value	50 kΩ	50 kΩ	800 Ω	300 Ω	2.12 kΩ	40 μF

14.3.1 Component selection

Not all calculated component values from Table 14.3 are available. Therefore, standard values need to be selected. For the selection of components, the search engine Octopart [23] is used. The final values are listed in Table 14.4. Tuneable inductors are used in the position of L_1 and L_2 to modify the centre frequencies of the bandpass filters and to tackle inaccuracies caused by tolerances in capacitors C_1 and C_2. This allows fine-tuning of the magnitude response to improve the linearity of the FM detector. The final Bill of Materials is listed in Section G.2.

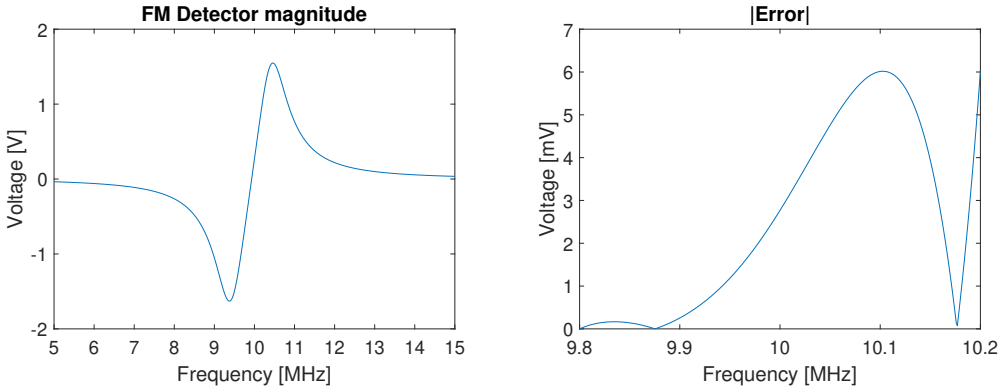
Table 14.4: The selected component values for the FM detector. The notation (2x) indicates that two components have the same name

	$\mathbf{R_1}$	$\mathbf{R_2}$	$\mathbf{C_1}$	$\mathbf{C_2}$	$\mathbf{L_1}$	$\mathbf{L_2}$
Value	2 kΩ	2 kΩ	100 pF	100 pF	1.54-2.86 μH (0.72 Ω)	2.13-4.29 μH (1.05 Ω)
	$\mathbf{R_3}$	$\mathbf{R_4}$	$\mathbf{C_3}$	$\mathbf{C_4}$	$\mathbf{R_5}$	$\mathbf{R_6}$
Value	62 kΩ	626 kΩ	400 pF	400 pF	50 kΩ	50 kΩ
	$\mathbf{R_7}$	$\mathbf{R_8}$	$\mathbf{R_C(2x)}$	$\mathbf{R_E}$ **(2x)**	$\mathbf{R_{ref}}$	$\mathbf{C_{5,6}}$
Value	50 kΩ	50 kΩ	800 Ω	300 Ω	2.12 kΩ	39 μF (0.88 Ω)

15. Simulation results

In order to ensure proper operation, multiple simulations of the FM detector circuit are performed in ADS. The first simulation is an AC sweep with an amplitude of 2.5 V, as specified by requirement FMD5. The result of this simulation can be seen in Figure 15.1a. During the simulations, a load resistance of 35 kΩ is used in order to simulate a 330 μA load current. This satisfies requirement FMD6.

To determine the linearity in the frequency range of interest (9.8 MHz till 10.2 MHz), the simulation results are exported to MATLAB and the absolute error with respect to a linear approximation is obtained, which can be seen in Figure 15.1b. From the figure, it can be concluded that the maximum absolute error is equal to 6 mV, resulting in a linearity[1] of 48.1 dB.



(a) (b)

Figure 15.1: (a) The frequency response of the FM detector and (b) the absolute error of the frequency response compared to a linear approximation for the region of interest.

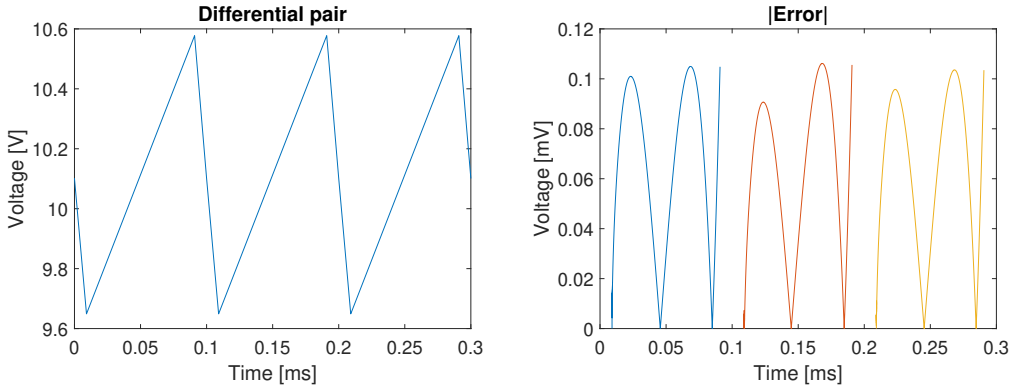
After the frequency response was obtained, a transient simulation is performed on the differential-to-single-ended converter to determine its linearity. To the inputs of the differential-to-single-ended converter, pulse sources were connected that produced an ideal sawtooth. The output waveform of the differential-to-single-ended converter can be seen in Figure 15.2a. From Figure 15.2b, the maximum absolute error is found to be 0.11 mV which results in a linearity of 78.5 dB.

15.1 Simulation using calculated component values

The next simulation is a transient simulation which is used to obtain the output waveform of the whole FM detector. In order to simulate the FM signal at the input, a sawtooth waveform with a frequency of 10 kHz and an amplitude of 1 V is applied to a VCO block in ADS. The VCOs parameters are set up in such a way that the centre frequency is 10 MHz with a deviation of ±200 kHz, as defined by requirement FMD0 and FMD1 respectively. The amplitude of the IF is set to 2.5 V as defined by requirement FMD5. The results of this simulation using the calculated values from Table 14.3 can be seen in Figure 15.3a.

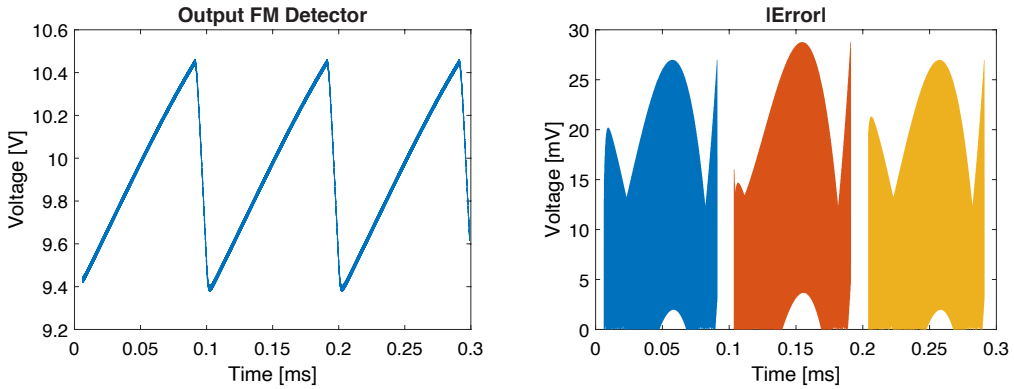
The absolute error of the output waveform compared to a linear approximation can be seen in Figure 15.3b. From the figure, it can be concluded that the maximum absolute error is equal to 28.74 mV, resulting in a linearity of 30.8 dB. This satisfies requirement FMD2.

[1] The linearity is defined as: $20 \log_{10}\left(\frac{\text{amplitude}}{\text{error}}\right)$



(a) (b)

Figure 15.2: (a) The output of the differential-to-single-ended converter and (b) the absolute error of the output compared to a linear approximation.



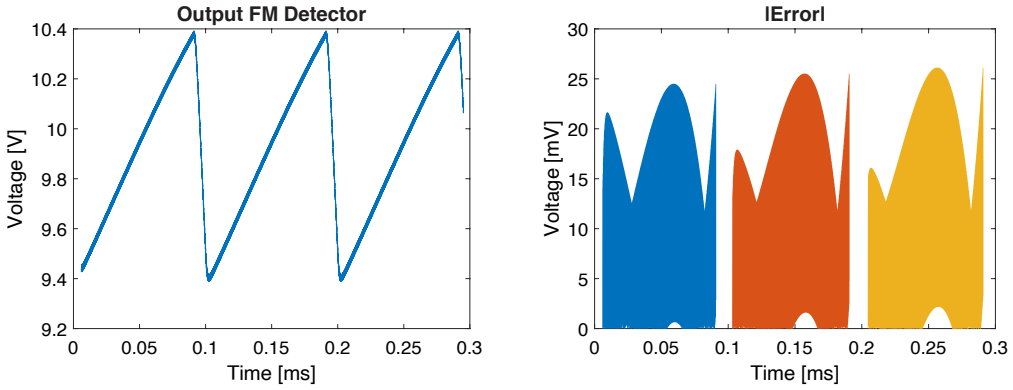
(a) (b)

Figure 15.3: (a) The output waveform of the FM detector with calculated component values and (b) the absolute error of the output compared to a linear approximation.

15.2 Simulation using selected component values

The last simulation is a transient simulation using selected component values from Table 14.4. The output waveform of the FM detector can be seen in Figure 15.4a. From the figure, it can be seen that the peak-to-peak output is 1 V which satisfies requirement FMD3.

The absolute error with respect to a linear approximation is shown in Figure 15.4b. Looking at the figure, it can be concluded that the maximum absolute error is 26.1 mV, which results in a linearity of 31.7 dB. This satisfies requirement FMD2.



(a) (b)

Figure 15.4: (a) The output waveform of the FM detector with selected components and (b) the absolute error of the output compared to a linear approximation.

From the results of Figure 15.3b and 15.4b, it can be seen that the voltage ripple of the envelope detector has a drastic impact on the error. It approximately quadruples the error with respect to the error caused by the bandpass filters. Unfortunately, this is a trade-off that has to be made in order to still allow for good waveform following.

In Table 15.1, the comparison between the results of the FM detector and the corresponding requirements is shown. It can be concluded that the design meets all the requirements.

Table 15.1: The comparison between the requirements for the FM detector and the results obtained using calculated values and selected values

Tag	**Description**	**Value**	**Calculated values**	**Selected values**
FMD2	Linearity	> 30 dB	30.8 dB	31.7 dB
FMD3	Peak-to-peak output	≥ 1 V	1.1 V	1 V
FMD4	Input current draw	< 2 mA	1.5 mA	1.5 mA
FMD7	Power consumption	< 150 mW	122.7 mW	123.9 mW

All the intermediate signals of the FM detector can be found in Appendix D. The simulation results of the integration with the IF amplifier and the baseband amplifier can be found in Section E.2 and E.3 respectively.

16. Discussion

The simulations in Chapter 15 are all done with components that have exact values. However, in reality, components have a tolerance, as shown in Section G.2, which can result in deviations from the desired performance. For the bandpass filters, this could mean that $\alpha_1 = \alpha_2$ does not hold anymore. This means that the difference between V_+ and V_- is not 0 V when $\omega_i(t) = \omega_0$. For the differential-to-single-ended converter, this does not pose a problem since it has a linear region for a maximum input difference of ± 1.5 V, which is approximately 3 times larger than what it encounters during normal operation. A variation of R_1, R_2, C_1 or C_2, would thus simply change the DC offset of the output signal. A variation of C_1 or C_2 would also not change the centre frequencies of the bandpass filters, since those can be adjusted by changing the inductance of L_1 and L_2.

For the envelope detectors, small variations in component values would not affect the performance significantly. The choice of τ is made such that the upper boundary will not be violated due to small variations. The ripple of the output can be affected, but this would not have a drastic effect, since the ripple scales linearly with any variation of R or C.

For the differential-to-single-ended converter, small variations in component values will also not affect the performance significantly. Although some resistors have the same name (R_C and R_E), it is not crucial that their values are exactly the same. The left resistor R_C of Figure 14.2 does not influence the output voltage. This means that the two resistors labelled R_C do not need to have the exact same value. A mismatch of R_E would however result in different weights of V_+ and V_-, but this mismatch would not affect the circuit significantly, since the tolerance of R_E is 0.5%, as can be seen in Section G.2.

For the FM detector, several choices and trade-offs are made. The most important choice is the choice of the frequency-to-amplitude converter. As explained in Section 13.1, a balanced slope detector is chosen. This choice is made, since the slope detector was found to be best suited for the goal of the project. However, for other projects using FM detection, a different choice could have been made.

Since this project has only an educational purpose, there is no clear application. If an application was chosen, the trade-offs could have been made differently. For most trade-offs, a reasonable linearity was chosen while keeping the power consumption as low as possible. For different applications, some aspects have a different weight than others, resulting in different choices.

As shown in Figure 15.4, the error is mostly due to the ripple of the envelope detector. The ripple is caused by the IF, since it is not filtered out completely. The ripple can be made smaller by choosing a larger time constant, but this would limit the range of frequencies that can be followed. In other words, it will filter the sharp negative slope of the sawtooth signal as well. This causes problems for continuous distance measurements, but it is acceptable if only a few points are measured on the positive slope.

As the reader could have noticed, the linearity of the differential-to-single-ended converter is much higher than the linearity of the other two sub-modules. This is due to the proper design of the CCS which provides an almost constant current and due to the approximately three times larger linear region than required.

As shown in Section G.2, the FM detector is expensive due to the tuneable inductors. Compared to all the other components, the prices are extremely high. However, the reason these inductors are chosen is that it is difficult to find inductors with a specific inductance, which makes it difficult to have the centre frequency exactly at the desired frequency. Moreover, inductors typically have a large tolerance, which means that the centre frequency could be shifted significantly from the desired value. Since the linearity is dependent on the location of the centre frequencies, a tuneable inductor is chosen. This allows the centre frequency to be fine-tuned with a spectrum analyser during operation.

17. Conclusion

As shown in Table 15.1, the designed FM detector meets all the requirements. This means that the FM detector can successfully detect a sawtooth of 10 kHz modulated at the IF of 10 MHz with a frequency deviation of 400 kHz while providing a linearity of 31.7 dB.

17.1 Recommendation and future work

For the FM detector, the greatest improvement can be made in the envelope detector, since this causes the most non-linearity. To improve the linearity, an extra low pass filter can be made after the envelope detector, in order to reduce the IF component. However, this filter needs to be sharp, since it should not affect the high-frequency components of the sawtooth. Another option is to choose a different kind of AM detector, for example, a synchronous detector. This could also result in a lower ripple at the output and a better linearity.

Another improvement that can be made is electric tuning. Instead of tuning the tunable inductors mechanically, a solution can be found in order to modify the centre frequencies by an external voltage source, for example, using varactors. This solution would be more elegant.

Due to the project timeline, not all possible implementations have been considered. Better research can be done into different implementations and those implementations can be tested. If more implementations are simulated, a better comparison can be made, which could result in a better performance. However, this was not feasible for this project due to the limited time span.

Finally, it is recommended that a PCB is designed in order to preform more realistic simulations which take into account the physical properties of the PCB. In this way, a more realistic behaviour of the circuit can be obtained and non-idealities can be compensated for during design.

Part IV

Appendices

A. Power Budget

The complete system has the power requirements SYS9, SYS10 and SYS11. In order to meet these requirements, some system level calculations on the power budget have to be done.

For the transmitter, the total transmitted power should be at least 20 dBm (100 mW). To understand how much power this would give at the receiver, the free space transmission equation is used (Equation (A.1), obtained from [33]).

$$\frac{P_r}{P_t} = D_t D_r \left(\frac{\lambda}{4\pi d}\right)^2 \tag{A.1}$$

For this purpose, the equation is rewritten into its dB counterpart:

$$P_{r,dB} = P_{t,dB} + D_{r,dB} + D_{r,dB} + 20\log_{10}\left(\frac{\lambda}{4\pi d}\right) \tag{A.2}$$

In this bachelor project, isotropic antennas with a 50 Ω impedance are used. For isotropic antennas, the directivity is 0 dB and the directivity components can be removed from Equation (A.2). For the final design, the transmission frequency will vary from 88 MHz to 108 MHz. In this case, the worst case scenario of 108 MHz is assumed. The transmission distance should be 5 m, which results in a received power of -27 dBW. This is enough to be detected at the receive antenna, but when transmitting 20 dBm, requirement SYS10 can not be met due to the power consumption of the signal generation in the transmitter. To calculate the transmit power required to achieve a 50% efficiency, Equation (A.3) is used.

$$\eta_t = \frac{P_t}{\frac{P_t}{\eta_{PA}} + P_{budget}} \tag{A.3}$$

With η_{PA} the efficiency of the power amplifier, η_t the efficiency of the complete transmitter, and P_{budget} the power used by the other stages in the transmitter. The power amplifier is assumed to have a 70% efficiency, and P_{budget} is assumed to be 300 mW. Solving for a transmission efficiency of 50% results in a required minimum transmission power of 525 mW (27.2 dBm). Since this requirement is higher than the previous one, this one is considered. Each component in the transmitter will have their own power requirements, based on the total power budget available. The power division for the transmitter and receiver can be seen in Table A.1.

Table A.1: Estimated power consumption for each component

Component	**Estimated power**	**Component**	**Estimated power**
LNA	100 mW	Sawtooth generator	150 mW
Mixer	50 mW	Modulator	100 mW
IF amplifier	200 mW	BB1	50 mW
FM Detector	150 mW	Power amplifier	(4.5 W)
BB2	200 mW		
Local Oscillator	100 mW		
Total	**800 mW**	**Total**	**300 mW (4.8 W)**

In this table, the power amplifier is assumed to have a transmit power of 3 W, and an efficiency of 70%. The reader is referred to [34] for the reasoning behind these values.

The total power consumption of the transceiver results in 5.5 W, which satisfies requirement SYS11.

B. Schematics

B.1 Sawtooth generator schematic

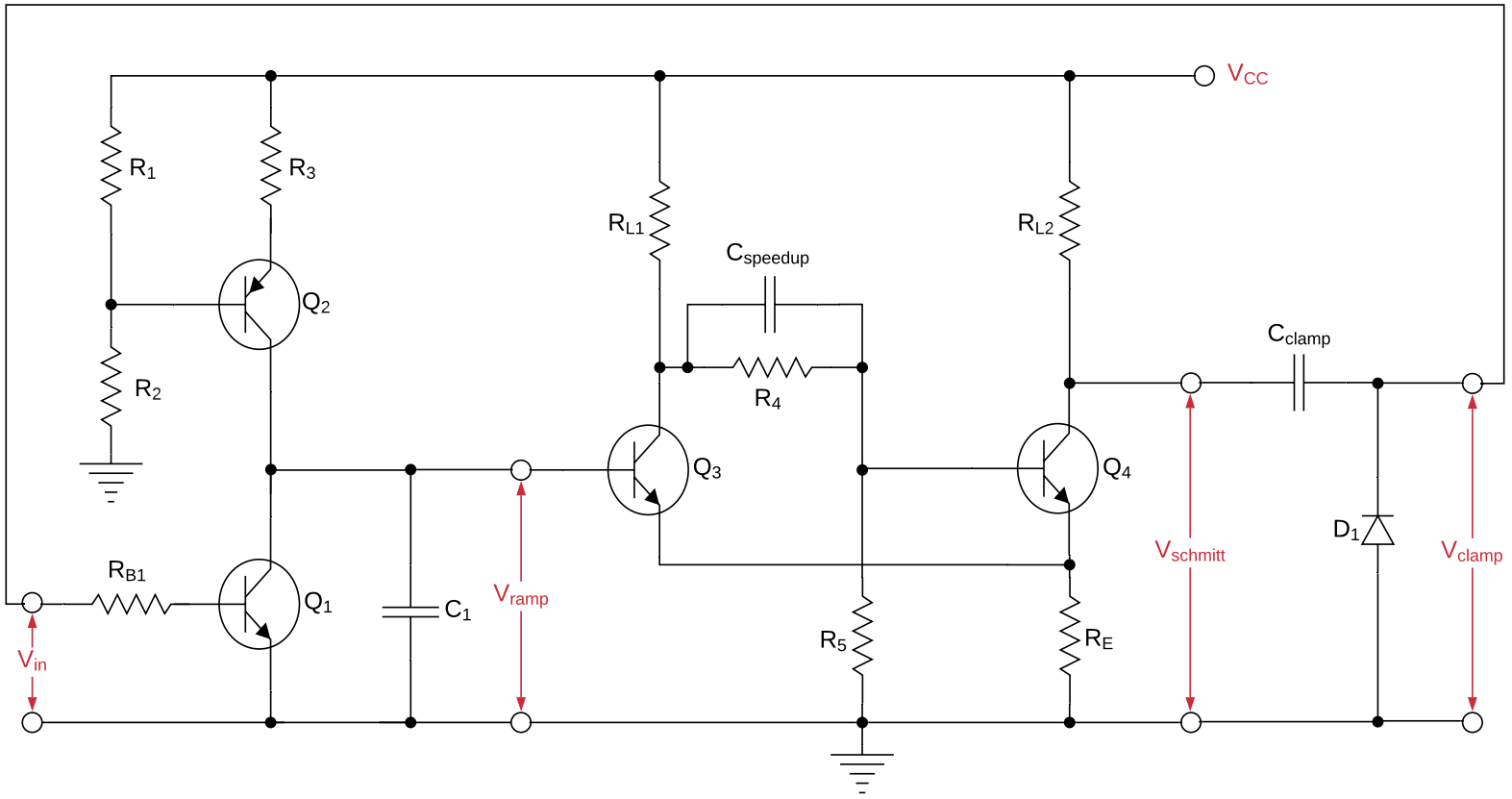


Figure B.1: The schematic of the sawtooth generator.

B.2 FM detector schematic

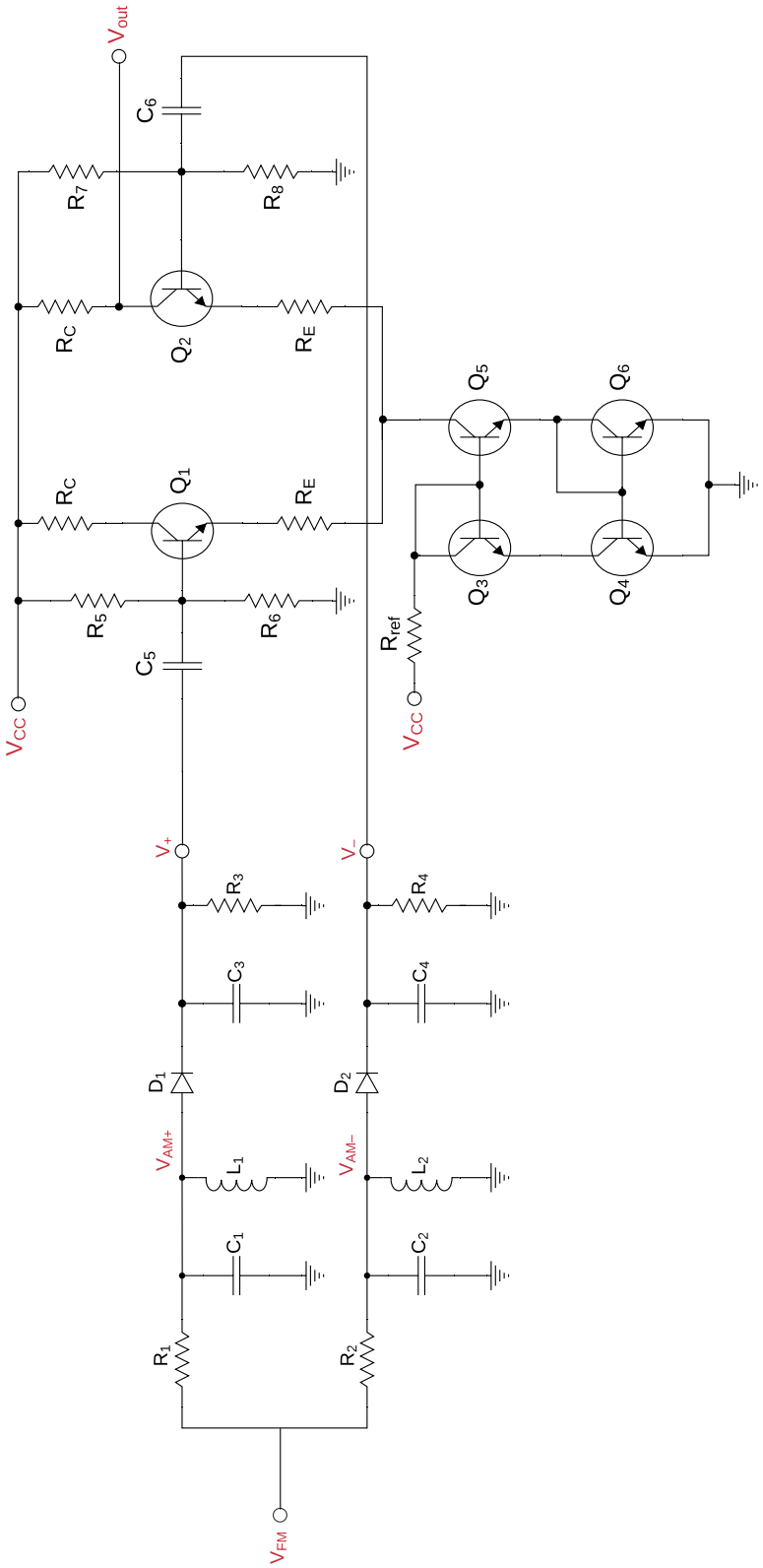


Figure B.2: The schematic of the FM detector.

C. Sawtooth generator plots

In this appendix, the intermediate simulation results of the sawtooth generator can be found.

C.1 Schmitt trigger characteristic

As discussed in Section 7.2, the Schmitt trigger needs to have hysteresis in order to function properly. In Figure C.1, the input/output relationship of the Schmitt trigger is shown where hysteresis can be seen.

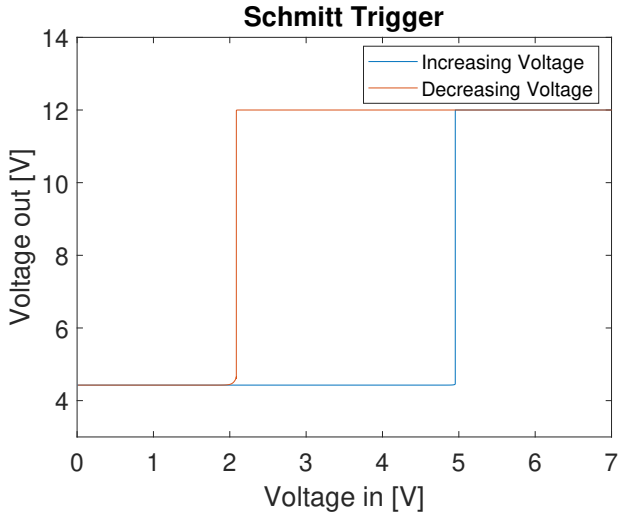


Figure C.1: The input/output relationship of the Schmitt trigger.

C.2 Schmitt trigger output

The Schmitt trigger is used to generate a square wave signal as shown in Figure C.2. Since this output is too high to turn off the transistor of the ramp generator, this signal will go to a voltage clamper to reduce its DC offset.

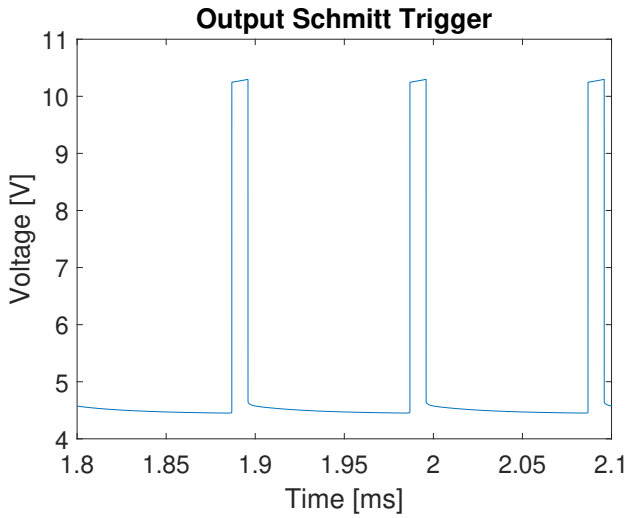


Figure C.2: The output of the Schmitt trigger.

C.3 Voltage clamper output

The voltage clamper is used to lower the DC offset of the Schmitt trigger, as shown in Figure C.3. This signal is used to turn the transistor of the ramp generator on and off.

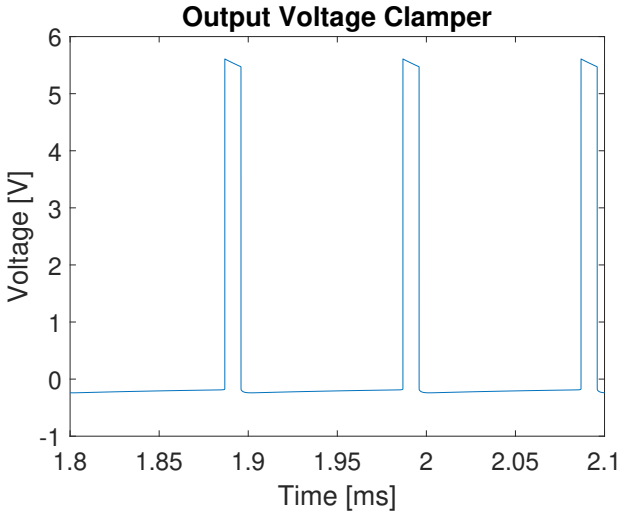


Figure C.3: The output of the voltage clamper.

D. FM detector plots

In this appendix, the intermediate simulation results of the FM detector can be found.

D.1 Frequency response of the bandpass filters

The bandpass filters are designed in such a way that they cancel their non-linearites around 10 MHz. The frequency response of both filters is shown in Figure D.1, which was made by doing an AC sweep with an amplitude of 2.5 V.

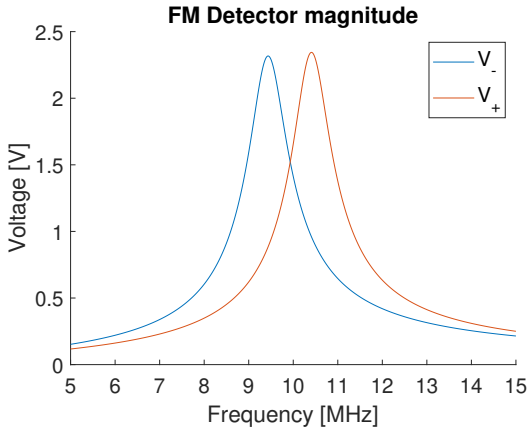
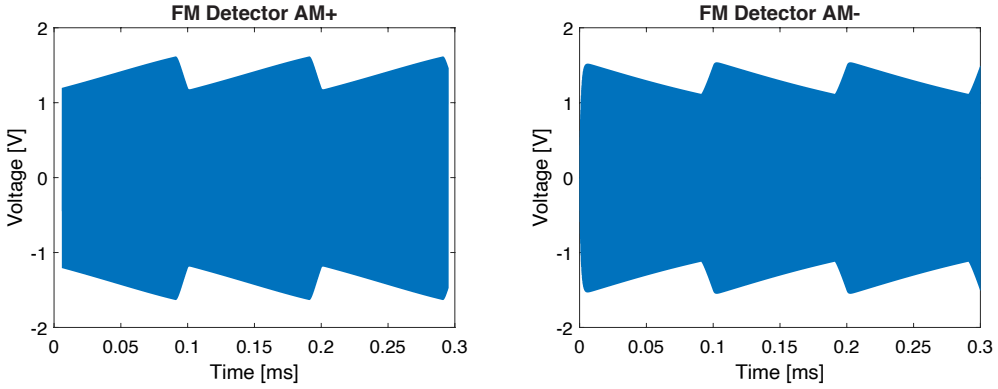


Figure D.1: The frequency response of the bandpass filters.

D.2 Amplitude modulated signals

In Figure D.2, the two amplitude modulated signals are shown. A sawtooth envelope can clearly be distinguished. These AM signals are then provided to the input of the envelope detectors.



(a) (b)

Figure D.2: (a) The output of the first bandpass filter, which is responsible for the positive input (b) The output of the second bandpass filter, which is responsible for the negative input.

D.3 Envelope detector signals

The envelope detector will filter out the IF while keeping the original sawtooth signal untouched, as shown in Figure D.3. These signals will then be biased to a higher DC offset and then provided at the input of the differential-to-single-ended converter.

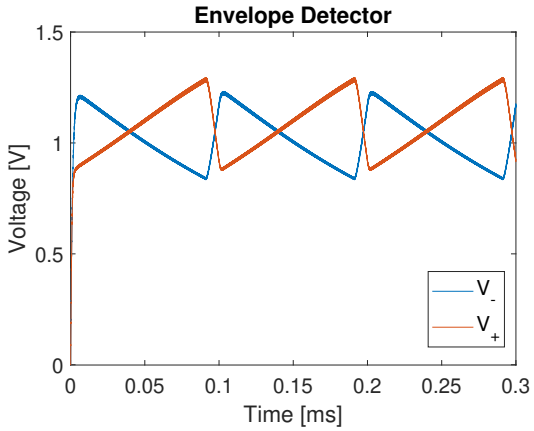


Figure D.3: The output of the envelope detectors.

D.4 Differential-to-single-ended converter signals

Since the output of the envelope detector is not high enough to ensure proper operation of the differential-to-single-ended converter, the signals need to be biased to a higher voltage, as shown in Figure D.4.

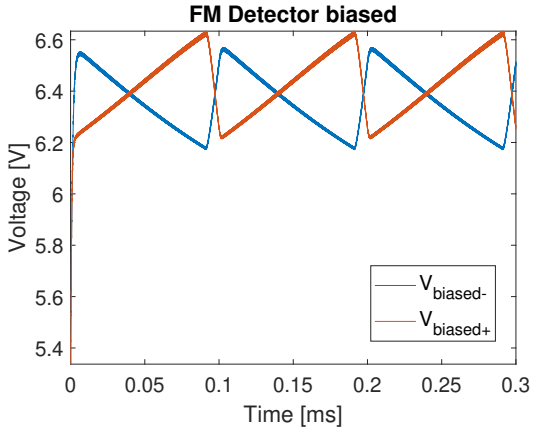


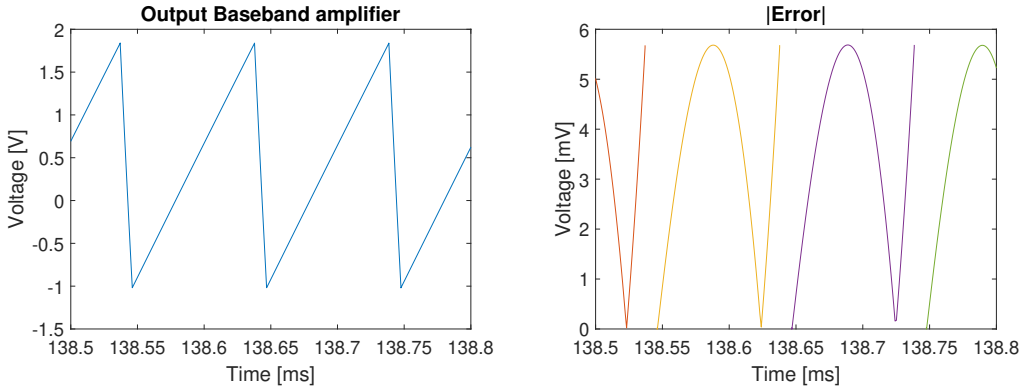
Figure D.4: The DC biased inputs of the differential-to-single-ended converter.

E. Integration with other modules

In this appendix, the simulation results can be found for the sawtooth generator and the FM detector together with modules that interface with them.

E.1 Sawtooth generator and baseband amplifier

As shown in Figure 1.2, the sawtooth generator is preceding the baseband amplifier. The output waveform, after combining these modules, is shown in Figure E.1a, which has an amplitude of 2.87 V. The maximum absolute error is 5.69 mV, as can be seen from Figure E.1b, which result in a linearity of 54.1 dB.

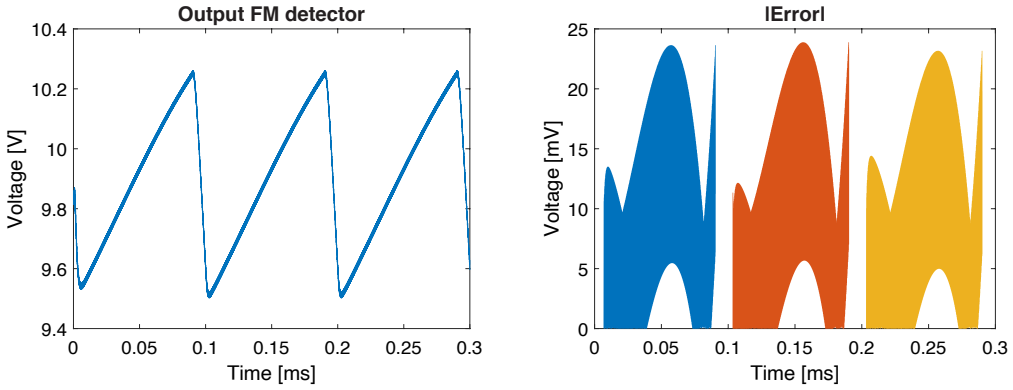


(a) (b)

Figure E.1: (a) The output of the baseband amplifier together with the sawtooth generator (b) the absolute error of the output compared to a linear approximation.

E.2 FM detector and IF amplifier

As shown in Figure 1.2, the FM detector is preceded by the IF amplifier. These two modules are combined and a transient simulation is performed. The output waveform of the FM detector can be seen in Figure E.2a, which has an amplitude of 0.76 V. The maximum absolute error is 23.9 mV, as can be seen in Figure E.2b, which results in a linearity of 30.1 dB.

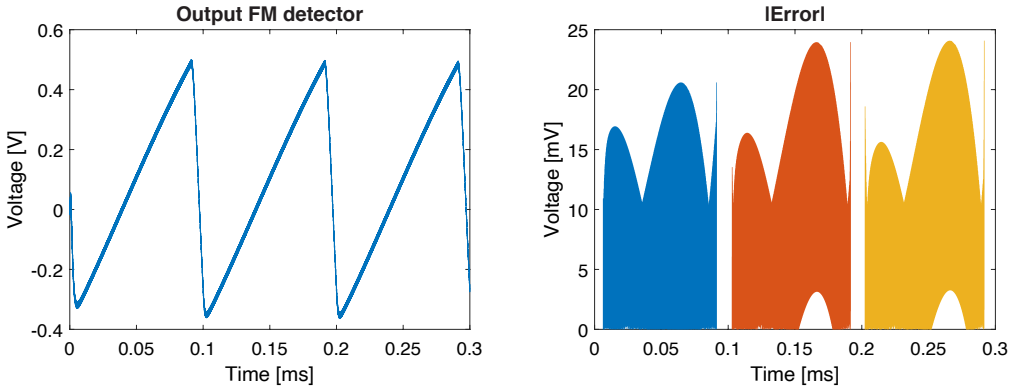


(a) (b)

Figure E.2: (a) The output of the FM detector together with the IF amplifier (b) the absolute error of the output compared to a linear approximation.

E.3 FM detector and baseband amplifier

As shown in Figure 1.2, the FM detector is preceding the baseband amplifier. These two modules are combined and a transient simulation is performed. The output waveform of the baseband amplifier can be seen in Figure E.3a, which has an amplitude of 0.86 V. The maximum absolute error is 24 mV, as can be seen in Figure E.3b, which results in a linearity of 31.1 dB. Note that this result is obtained with an ideal input at the FM detector and not with the IF amplifier in front of it.

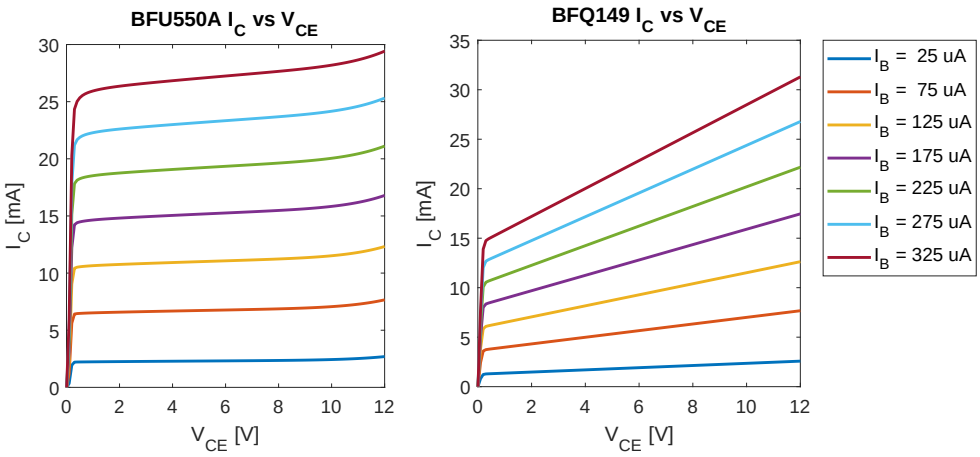


(a) (b)

Figure E.3: (a) The output of the baseband amplifier together with the FM detector (b) the absolute error of the output compared to a linear approximation.

F. Transistor Curves

For this project, two different transistors are used. The NPN transistor is chosen to be the BFU550A and the PNP transistor is chosen to be the BFQ149. The I_C vs V_{CE} curves of both transistors are shown in Figure F.1.



(a) (b)

Figure F.1: The I_C vs V_{CE} curve of the: (a) BFU550A and (b) BFQ149.

G. Bill of Materials

In this appendix, the Bill of Materials (BoM) can be found for the two modules that were designed. The BoM includes the component names, part numbers, values, tolerances and prices. The prices are based on the data from Octopart on the date of writing.

G.1 Sawtooth generator

The BoM for the sawtooh generator can be seen in Table G.1.

Table G.1: BoM of the sawtooth generator

Name	**Part number**	**Value**	**Tolerance**	**Price**
R_1	1-1614895-3	9.4 kΩ	0.1%	€0.12
R_2	RT0603FRE0713K3L	13.3 kΩ	0.1%	€0.01
R_{3A}	NRC06F7150TRF	715 Ω	1%	€0.01
R_{3B}	67WR500LF	500 Ω		€0.68
R_{B1A}	CRCW08055K00FKTA	5 kΩ	1%	€0.04
R_{B1B}	3296X-1-502LF	5 kΩ		€1.09
R_{L1A}	RT0603BRE078KL	8 kΩ	0.1%	€0.07
R_{L1B}	3296W-1-202LF	2 kΩ		€1.30
R_{L2}	RT0603BRD072K52L	2.52 kΩ	0.1%	€0.05
R_4	RT0603DRE0712KL	12 kΩ	0.5%	€0.01
R_{5A}	RT0603FRE0716KL	16 kΩ	1%	€0.01
R_{5B}	3296X-1-502LF	5 kΩ		€1.09
R_E	RT0603FRE071K4L	1.4 kΩ	1%	€0.01
C_1	PHE450SR6150JR06L2	0.15 uF	5%	€1.97
$C_{speedup}$	PME295RB3470MR19T0	470 pF	20%	€0.64
C_{clamp}	F450DD333J1K6C	33 nF	5%	€0.71
Q_1	BFU550A			€0.09
Q_2	BFQ149			€1.53
Q_3	BFU550A			€0.09
Q_4	BFU550A			€0.09
D_1	HSMS-2800-TR1G			€0.22
Total				€9.83

G.2 FM detector

The BoM for the FM detector can be seen in Table G.2.

Table G.2: BoM of the FM detector

Name	Part number	Value	Tolerance	Price
R_1	RNCF0805TKE2K00	2 kΩ	0.01%	€0.46
R_2	RNCF0805TKE2K00	2 kΩ	0.01%	€0.46
C_1	C0603C101F5GACTU	100 pF	1%	€0.15
C_2	C0603C101F5GACTU	100 pF	1%	€0.15
L_1	9405R-16	1.54 - 2.86 μH (720 mΩ)		€35.14
L_2	9405R-18	2.13 - 4.29 μH (1.05 Ω)		€35.14
R_3	RT0603FRE0762KL	62 kΩ	1%	€0.01
R_4	PTN1206E6263BST1	626 kΩ	0.1%	€0.72
C_3	12101U401JAT2A	400 pF	5%	€0.21
C_4	12101U401JAT2A	400 pF	5%	€0.21
R_5	MCU08050D5002BP100	50 kΩ	0.1%	€0.18
R_6	MCU08050D5002BP101	50 kΩ	0.1%	€0.18
R_7	MCU08050D5002BP102	50 kΩ	0.1%	€0.18
R_8	MCU08050D5002BP103	50 kΩ	0.1%	€0.18
C_5	EEEFK1H390SP	39 μF (0.88 Ω)	20%	€0.12
C_6	EEEFK1H390SP	39 μF (0.88 Ω)	20%	€0.12
R_C	WSF2515800R0DKEB	800 Ω	0.5%	€1.02
R_C	WSF2515800R0DKEB	800 Ω	0.5%	€1.02
R_E	RR1220P-301-D	300 Ω	0.5%	€0.01
R_E	RR1220P-301-D	300 Ω	0.5%	€0.01
R_{ref}	NTR10D2101DTRF	2.1 kΩ	0.5%	€0.01
D_1	HSMS-2800-TR1G			€0.22
D_2	HSMS-2800-TR1G			€0.22
Q_1	BFU550A			€0.09
Q_2	BFU550A			€0.09
Q_3	BFU550A			€0.09
Q_4	BFU550A			€0.09
Q_5	BFU550A			€0.09
Q_6	BFU550A			€0.09
Total				€76.65

H. Schematics with chosen components

H.1 Sawtooth generator schematic

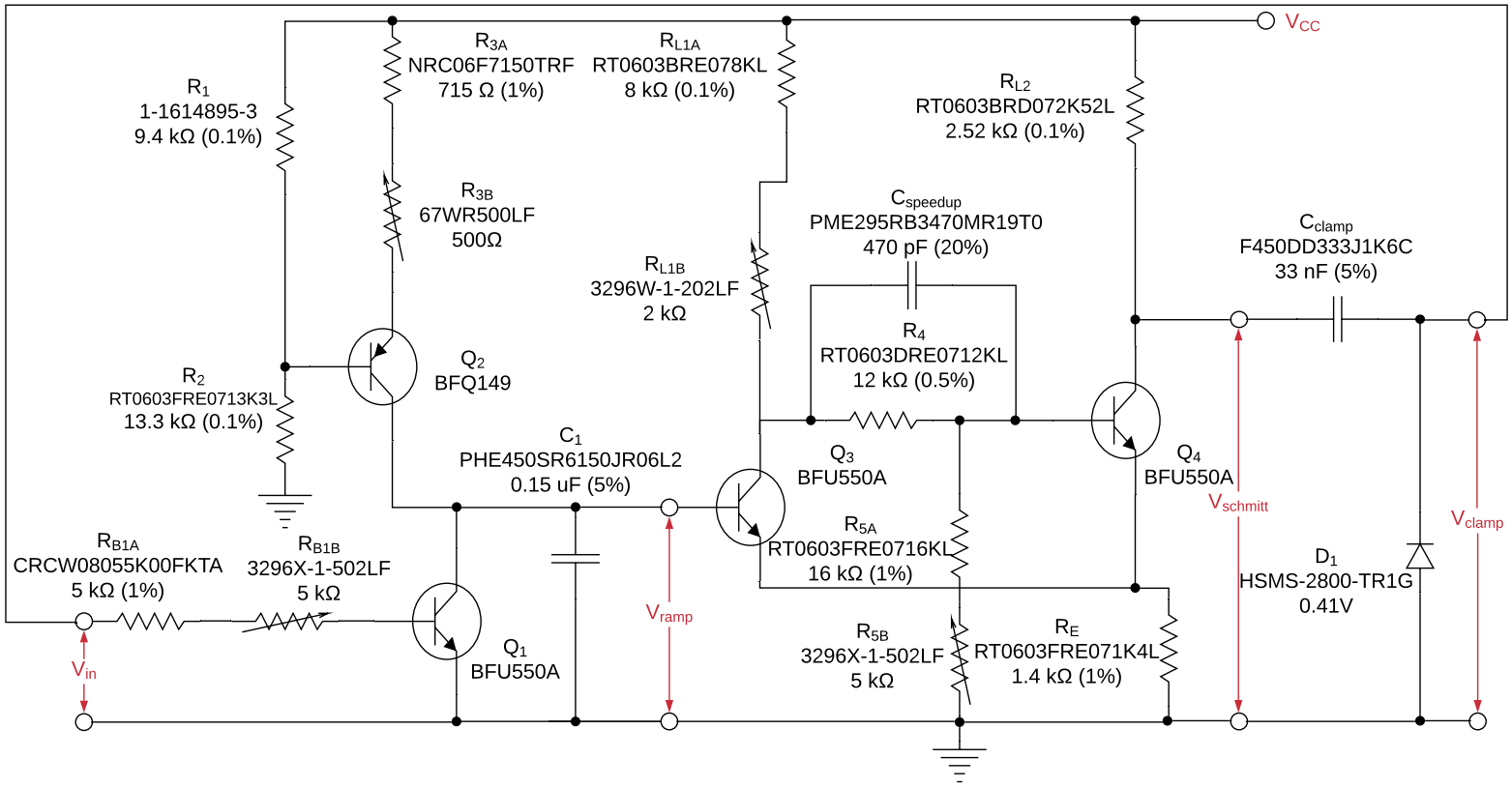


Figure H.1: The schematic of the sawtooth generator with the chosen components.

H.2 FM detector schematic

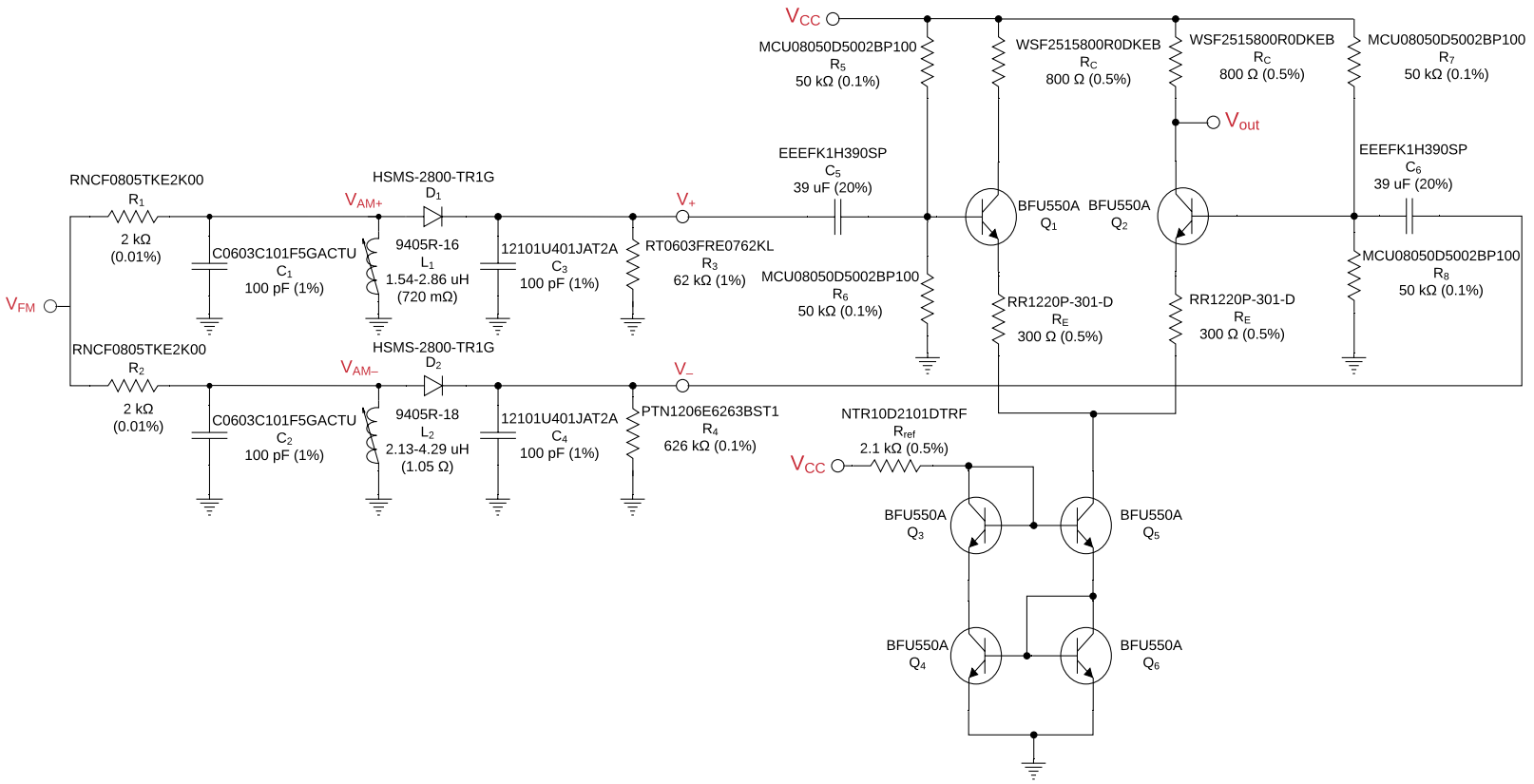


Figure H.2: The schematic of the FM detector with the chosen components.

I. MATLAB code

In this appendix, the MATLAB code can be found that was used during the design of the two modules.

I.1 Sawtooth generator

The MATLAB code used to calculate the component values of the sawtooth generator.

```
%Authors:        Youri Blom & Filip Bradaric
%Description:   This code is used in order to calculate the component values of the sawtooth
%               generator. First all the parameters need to be defined and then the script will
%               automatically calculate all the component values and display them to the user
close all;
clear all;

%Parameters
V_UTP = 5;
V_LTP = 2;
f = 1e4;
h_FE1 = 80;
h_FE2 = 80;
h_FE4 = 80;
V_CC = 12;
V_BE1 = 0.80;
V_BE2 = 0.70;
V_BE3 = 0.80;
V_BE4 = 0.80;
I_QC4 = 3e-3;
V_ceSat = 0.2;
t_c = 1/(1.1*f);
t_d = 0.1*t_c;
I_load = 40e-6; %Max load current
I_c_max = 50e-3; % Max transistor collector  current
current_factor = 100; % load-charging current ratio
source_factor = 10;   % base-bias current ratio


%Schmitt trigger design
%considering UTP:
V_E = V_UTP- V_BE4;
R_E = V_E/I_QC4;
R_L2 = (V_CC - V_E - V_ceSat)/I_QC4;
I_R5 = I_QC4/10;
R_5 = V_UTP/I_R5;
I_QB4 = I_QC4/h_FE4;
I_R4 = I_R5 + I_QB4;
R_sum = (V_CC-V_UTP)/I_R4;
%considering LTP:
I_R4 = V_LTP/R_5;
I_QC3 = (V_LTP-V_BE3)/R_E;
R_L1 = (V_CC - I_R4*R_5 - I_R4*R_sum)/I_QC3;
R_4 = R_sum-R_L1;
%The speedup capacitor
```

```
R_eq = 1/((1/R_4)+(1/(R_L1+R_5)));
C_speedup = t_d/(2.3*R_eq);




%Ramp generator design
I_C1 = current_factor*I_load;
V_R3 = V_CC - 3 - V_UTP;
C1 = I_C1/(f*(V_UTP-V_LTP));
I_QB2 = I_C1/h_FE2;
R_3 = V_R3/(I_C1+I_QB2);
V_R1 = V_R3 + V_BE2;
I_R1 = source_factor*I_QB2;
R_1 = V_R1/I_R1;
R_2 = (V_CC-V_R1)/(I_R1+I_QB2);
I_QC1 = I_C1*(1+t_c/t_d);
I_QB1 = I_QC1/h_FE1;


% Schmitt output voltage
V_schmitt_high = V_CC - R_L2*I_QB1;
V_schmitt_low = V_CC - R_L2*I_QC4;
%Clamp max output voltage
Vin_max = (V_schmitt_high - V_schmitt_low) - 0.23;


%Clamp
C_clamp = t_c/R_L2;         %Rs is approximatially equal to R_L2
tilt = ((I_QB1*t_d)/C_clamp)/(V_schmitt_high - V_schmitt_low);

% Ramp generator base resistor
R_B1 = (Vin_max- V_BE1)/I_QB1;

if(I_QC1 > I_c_max)
    disp(['Warning, discharge current too large!']);
else

    disp(['R1: ', num2str(R_1)]);
    disp(['R2: ', num2str(R_2)]);
    disp(['R3: ', num2str(R_3)]);
    disp(['R_B1: ', num2str(R_B1)]);
    disp(['C1: ', num2str(C1)]);
    disp(['R_L1: ', num2str(R_L1)]);
    disp(['R_L2: ', num2str(R_L2)]);
    disp(['R4: ', num2str(R_4)]);
    disp(['C_speedup: ', num2str(C_speedup)]);
    disp(['R5: ', num2str(R_5)]);
    disp(['R_E: ', num2str(R_E)]);
    disp(['C_clamp: ', num2str(C_clamp)]);
end
```

I.2 FM detector

The MATLAB code used to calculate the component values of the FM detector.

```
%Authors:        Youri Blom & Filip Bradaric
%Description:   This code is used to calculate the component values of the
%               bandpass filters for the FM detector

close all;
clear all;

% Parameters
f_if = 10e6;
delta_f = 400e3;
R = 2000;

f_dev = delta_f/2;
omega_0 = 2*pi*f_if;
omega_dev = 2*pi*f_dev;

d_omega = 2*sqrt(3/2)*omega_dev;

omega_c1 = omega_0 + d_omega;
omega_c2 = omega_0 - d_omega;
f_c1 = omega_c1/(2*pi);
f_c2 = omega_c2/(2*pi);

C_1 = 1/(4*omega_dev*R);
C_2 = C_1;

L_1 = 1/(omega_c1^2*C_1);
L_2 = 1/(omega_c2^2*C_2);

Q_1 = omega_c1/(4*omega_dev);
Q_2 = omega_c2/(4*omega_dev);

if((Q_1 < 10) || (Q_2 < 10))
    disp('Warning, quality factor is not above 10!');

else
disp(['Q_1: ', num2str(Q_1)]);
disp(['R1: ', num2str(R)]);
disp(['C_1: ', num2str(C_1)]);
disp(['L_1: ', num2str(L_1)]);

disp(['Q_2: ', num2str(Q_2)]);
disp(['R2: ', num2str(R)]);
disp(['C_2: ', num2str(C_2)]);
disp(['L_2: ', num2str(L_2)]);
end
```

I.3 Waveform and error plotter

All of the simulations are done in ADS and the results are exported to MATLAB. The plots of the waveforms and errors are made using this script. First, a block diagram is shown in Figure I.1, which helps to understand the functionality of the code.

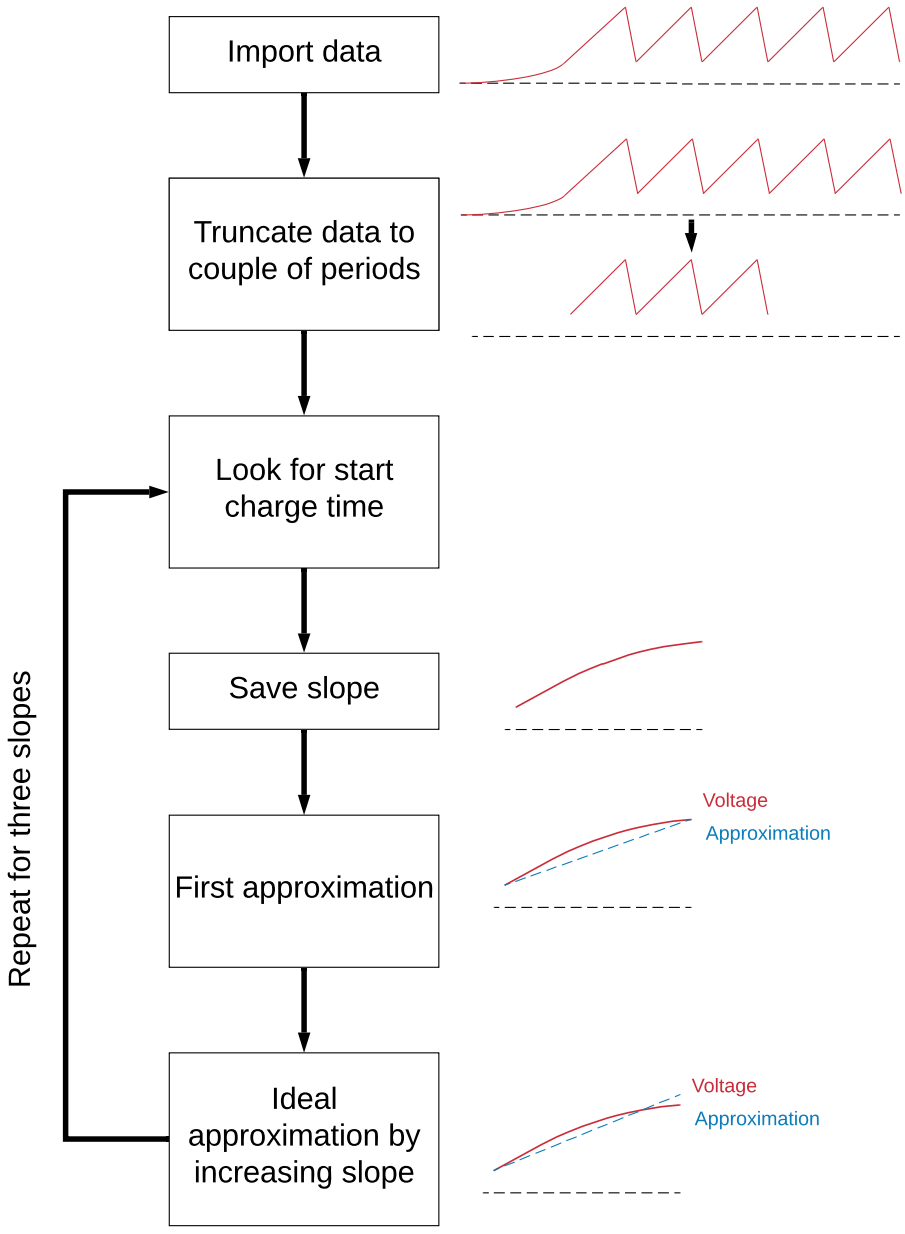


Figure I.1: A block diagram of the MATLAB code to plot the error. Note that the non-linearity is exaggerated to make the explanation more clear.

```
%Authors:        Youri Blom & Filip Bradaric
%Description: This script is used to plot ADS simulations and determine
%the error compared to a linear approximation

close all;
clear all;

%The simulation is saved in a time array and voltage array
fileID = fopen('Simulation_1.txt','r');
formatSpec = '%f';
A = fscanf(fileID,formatSpec);
for i = 1: length(A)
   if mod(i,2) == 1
       time((i+1)/2) = A(i);
   else
       voltage(i/2) = A(i);
   end
end

%The full simulation is truncated to a few periods
begin_graph = 16420;
end_graph = 27910;

voltage_new = voltage(begin_graph : end_graph);
time_new = time(begin_graph:end_graph);

%The sample size for determining the ideal linear approximation
sample_size = 1e4;

%The first eight slopes are used to determine the linearity


%Looks when the first slope starts
i = 1;
while voltage_new(i+1) < voltage_new(i)
    i= i+1;
end
begin = i + 1;
%%First slope
voltage_slope1(1) = voltage_new(begin);
time_slope1(1) = time_new(begin);
for i = 2: length(voltage_new)
    if voltage_new(i+begin) < voltage_new(i-1+begin)
        break;
    else
    voltage_slope1(i) = voltage_new(i+begin);
    time_slope1(i) = time_new(i+begin);
    end
end
a1 = (voltage_slope1(end)-voltage_slope1(1))/(time_slope1(end)-time_slope1(1));
b1= voltage_slope1(1)-a1*time_slope1(1);

```

```
approx1 = b1 + a1*time_slope1;
error1 = abs(voltage_slope1-approx1);

%Optimize best a and b
max_error = max(error1);
ideal_k = 1;
for k = 1 : sample_size
    better_a1(k) = a1 + 0.01*a1/sample_size*k;
    better_b1(k) = voltage_slope1(1)-better_a1(k)*time_slope1(1);
    better_approx1 = better_b1(k) + better_a1(k)*time_slope1;
    better_error1 = abs(voltage_slope1 -better_approx1);
    max_error1(k) = max(better_error1);
    if max_error1(k) < max_error
       max_error = max(better_error1);
       ideal_k = k;
    end
end
ideal_approx1 = better_b1(ideal_k) + better_a1(ideal_k)*time_slope1;
ideal_error1 = abs(voltage_slope1-ideal_approx1);

%Look when slope2 starts
i = i+begin;
while voltage_new(i+1) < voltage_new(i)
    i= i+1;
end
begin = i + 1;
%%Second slope
voltage_slope2(1) = voltage_new(begin);
time_slope2(1) = time_new(begin);
for i = 2: length(voltage_new)
    if voltage_new(i+begin) < voltage_new(i-1+begin)
        break;
    else
    voltage_slope2(i) = voltage_new(i+begin);
    time_slope2(i) = time_new(i+begin);
    end
end
a2 = (voltage_slope2(end)-voltage_slope2(1))/(time_slope2(end)-time_slope2(1));
b2= voltage_slope2(1)-a2*time_slope2(1);

approx2 = b2 + a2*time_slope2;
error2 = abs(voltage_slope2-approx2);

%Optimize best a and b
max_error = max(error2);
for k = 1 : sample_size
    better_a2(k) = a2 + 0.01*a2/sample_size*k;
    better_b2(k) = voltage_slope2(2)-better_a2(k)*time_slope2(2);
    better_approx2 = better_b2(k) + better_a2(k)*time_slope2;
    better_error2 = abs(voltage_slope2 -better_approx2);
    max_error2(k) = max(better_error2);
    if max_error2(k) < max_error
       max_error = max(better_error2);
```

```
        ideal_k = k;
    end
end
ideal_approx2 = better_b2(ideal_k) + better_a2(ideal_k)*time_slope2;
ideal_error2 = abs(voltage_slope2-ideal_approx2);

%Look when slope 3 starts
i = i+begin;
while voltage_new(i) < voltage_new(i-1)
    i= i+1;
end
begin = i + 1;
%%Third slope
voltage_slope3(1) = voltage_new(begin);
time_slope3(1) = time_new(begin);
for i = 2: length(voltage_new)
    if voltage_new(i+begin) < voltage_new(i-1+begin)
        break;
    else
    voltage_slope3(i) = voltage_new(i+begin);
    time_slope3(i) = time_new(i+begin);
    end
end
a3 = (voltage_slope3(end)-voltage_slope3(1))/(time_slope3(end)-time_slope3(1));
b3= voltage_slope3(1)-a3*time_slope3(1);

approx3 = b3 + a3*time_slope3;
error3 = abs(voltage_slope3-approx3);
%Optimize best a and b
max_error = max(error3);
for k = 1 : sample_size
    better_a3(k) = a3 + 0.01*a3/sample_size*k;
    better_b3(k) = voltage_slope3(3)-better_a3(k)*time_slope3(3);
    better_approx3 = better_b3(k) + better_a3(k)*time_slope3;
    better_error3 = abs(voltage_slope3 -better_approx3);
    max_error3(k) = max(better_error3);
    if max_error3(k) < max_error
       max_error = max(better_error3);
       ideal_k = k;
    end
end
ideal_approx3 = better_b3(ideal_k) + better_a3(ideal_k)*time_slope3;
ideal_error3 = abs(voltage_slope3-ideal_approx3);


%The voltage is plotted
plot(time_new*1000, voltage_new)
xlim([1.8 2.1]);
title('Output Sawtooth generator','fontsize',20)
xlabel('Time [ms]','fontsize',15);
ylabel('Voltage [V]','fontsize',15);
set(gca, 'Fontsize', 15)
figure
```

```
159 box on
160 hold on
161 %The error is plotted
162 plot(time_slope1*1000, ideal_error1*1000)
163 plot(time_slope2*1000, ideal_error2*1000)
164 plot(time_slope3*1000, ideal_error3*1000)
165 title('|Error|','fontsize',20);
166 xlabel('Time [ms]','fontsize',15);
167 ylabel('Voltage [mV]','fontsize',15);
168 set(gca, 'Fontsize', 15)
```

Acronyms

f_T transistor cut-off frequency.

h_{FE} common-emitter current gain.

t_c charging time.

t_d discharging time.

AC Alternating Current.

ADS Advanced Design System.

AM Amplitude Modulation.

BJT Bipolar Junction Transistor.

BoM Bill of Materials.

CCS Constant Current Source.

DC Direct Current.

EM ElectroMagnetic.

FM Frequency Modulation.

FMCW Frequency-Modulated Continuous-Wave.

IF Intermediate Frequency.

KCL Kirchoff's Current Law.

KVL Kirchoff's Voltage Law.

LNA Low Noise Amplifier.

LO Local Oscillator.

LTP Lower Trigger Point.

PA Power Amplifier.

radar RAdio Detection And Ranging.

RF Radio Frequency.

SNR Signal-to-Noise Ratio.

UTP Upper Trigger Point.

VCO Voltage Controlled Oscillator.

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