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Power-Efficiency Evolution of Capacitive Sensor Interfaces

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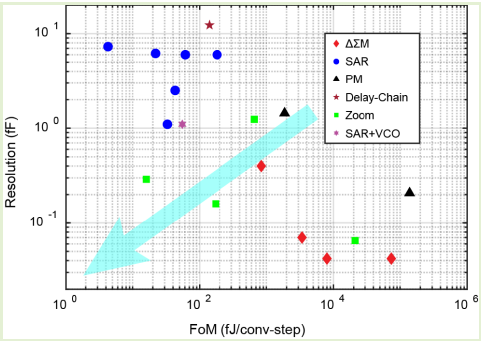
***Abstract*—Recent years have witnessed an improvement in the energy efficiency of capacitive sensor interfaces by more than three orders of magnitude. This article reviews the architectural and circuit innovations that have contributed to this progress. The fundamental limit on the energy consumption of capacitive sensor interfaces is discussed, as well as the widely used figure-of-merit (FoM). Interfaces based on period modulation feature simple circuitry, but their power efficiency at higher resolution deteriorates. Those employing ΔΣ modulation achieve high resolution with improved efficiency but require operational transconductance amplifiers that do not easily scale with process and supply voltage. Interfaces using successive approximation techniques feature mostly digital circuitry achieving good power efficiency at medium resolution. To achieve higher resolution, they can also be employed as the front-end in a hybrid architecture, where a back-end based on ΔΣ modulation or a voltage-controlled oscillator (VCO) performs a fine measurement on the front-end's residue, resulting in high resolution and excellent energy efficiency simultaneously.**



***Index Terms*—Capacitive sensor, energy efficiency, period modulation, SAR, ΔΣ modulation, VCO, zoom.**

I. Introduction

CAPACITIVE sensors have been known for almost three centuries now. Today they are used for sensing a large variety of quantities with an extremely wide range of application requirements, ranging from simple applications such as proximity and touch sensing to challenging applications such as picometer displacement measurement. Capacitive sensors are used for the direct conversion of a measurand into capacitance (humidity, position, liquid level, etc.), as well as converting the essential elements of other sensing devices such as pressure sensors, accelerometers, vibration sensors, etc. The popularity of capacitive sensors is due to their simplicity, relatively low cost, and excellent performance. The name "capacitive" reflects the way they are viewed in electrical circuits: as a variable capacitance. In this sense, the main task of capacitive sensor electronic interfaces is to convert the variable capacitance into an electrical signal (voltage, current, charge), followed by analog-to-digital conversion.

The first capacitive sensor, referred to as the "Leyden Jar," was discovered in the distant 1745 by the Dutch scientist Pieter van Musschenbroek, who was trying to store static electricity in a jar of water. The power efficiency of the interface of this sensor is still unmatched, as no electrical circuit is employed at all, but rather a direct sensor-human interface is applied. The amount of charge stored in the sensor is measured by the strength of the electric shock received by the human upon touching one of the electrodes. As one can guess, despite the ultimate "power efficiency" of this kind of interface, it is very impractical and also hazardous from today's point of view [1].

In modern times, with the advancement of electronic technology, we are witnessing a remarkable evolution of the capacitive sensor interface principles and solutions. In the era of "hot" electronics (vacuum bulbs) and the "bipolar" period of solid-state electronics, capacitive sensors were considered a "modulating" type of sensor. They used harmonic (sinusoidal) excitation signals with a fixed frequency, the amplitude of which was modulated by the reactance of the capacitive sensor. This approach involved a demodulation step, which, together with the excitation signal generation,

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was quite power-consuming [2]. Alternatively, LC harmonic oscillators were also employed to convert capacitance into frequency/period, which was then digitized by using counters or PLL (phase-locked loops) [3].

The introduction of MOS technology, offering excellent MOS switches, dramatically changed the capacitive sensor interface approach. Instead of converting the sensor capacitance into voltage/current by using harmonic excitation, a fixed voltage, or a constant current for a fixed time, was applied to the sensor capacitor and the stored charge was measured. Approximately at this same time, the switched capacitor technique started gaining popularity. 2nd-order LC oscillators were largely replaced by 1st-order RC oscillators. This "self-oscillating" interface principle became quite popular in the 1990s, as the output frequency could directly be digitized using the pulse counting or period measurement capabilities of microcontrollers, avoiding the use of analog-to-digital converters, which at that time were considered too expensive, power-consuming, and not very accurate. A basic disadvantage of the self-oscillating approach is that the conversion time is not fixed and depends to a large extent on the value of the converted capacitance. For many applications, such as servo loops, this is not feasible.

Currently, the most popular interface principle is based on a capacitance-to-charge conversion, followed by a charge-to-digital conversion. For the charge-to-digital conversion, the charge balancing technique is most often applied. Strictly speaking, "charge balancing" is achieved by using another "reference" charge. However, in the broader sense, charge balancing can be considered the supply and removal of equal portions of charge to and from the sensor capacitance, for instance: in 1st-order RC oscillators providing sustained oscillation; in single/multi-slope modulators; and even in so-called "charge amplifiers," for which a more proper name could be: charge-to-voltage converters.

At the beginning of this century, the term "capacitance-to-digital converter" (CDC) gained popularity. A significant number of scientific papers have reported original solutions based on the CDC principle. Such integrated CDCs can also be found in COTS (custom off-the-shelf) products [4]. The term "CDC" might be confusing, as it implies that the sensor capacitance is directly converted into a digital code, which is certainly not the case. Instead what is meant here is that one of the already existing capacitors in the analog-to-digital converter (ADC) is replaced with the sensor capacitor, or the sensor capacitor is additionally included in the ADC so that the output digital code becomes dependent on the sensor capacitance while keeping the usual analog input signal of the ADC constant. A simple criterion to determine whether the interface is based on a capacitance-to-analog conversion followed by an analog-to-digital conversion, or is based on a direct capacitance-to-digital conversion is: can the two conversions be executed independently from one another, or not?

Further in our review, we discuss the latest advances in capacitive sensor interface techniques by presenting solutions which offer a substantial improvement in energy efficiency. Although a significant number of recent publications report interesting capacitive sensor interfaces based on COTS electronic components, we shall not consider them, as, unfortunately, they are not competitive with respect to power efficiency. Our review will focus on integrated interface solutions which are designed for power efficiency and are mostly targeting specific applications: ASICs (application-specific integrated circuits). To a large extent, such solutions are published in solid-state-related journals and conferences, where the energy efficiency is quantified using figures-of-merit (FoMs), the most popular of which is borrowed from the ADC world: the Walden (also called ISSCC) FoM. This FoM gives the energy used to obtain 1 bit of information. It is worth mentioning that this FoM does not take into account the "quality" of the obtained information expressed in terms of precision, accuracy, stability, thermal drift, crosstalk, susceptibility to external interferences, etc.

In Section II, an analysis is given of the minimum energy consumption of thermal noise limited interfaces followed by an introduction of the Walden FoM. Section III presents prominent examples of the most popular charge-balancing interface techniques based on (1) self-oscillating circuits, (2) switched capacitor circuits, (3) capacitive bridges, and (4) capacitance-to-digital converters. The paper will be concluded in Section IV.

II. Energy Consumption of the Capacitive Sensor Interface

Over the years, considerable effort has been made to reduce the energy consumption of capacitive sensor interfaces for a given resolution. This is mainly due to the proliferation of battery-powered sensing systems, e.g., in mobile and IoT applications [5]–[11], for which power consumption is critical. In precision mechatronic systems, the maximum allowable power consumption is also limited to avoid errors due to self-heating [12]–[14]. The power consumption for a given resolution and speed is determined by the power needed to suppress thermal noise. In this section, the fundamental low energy boundary for general thermal noise limited capacitive sensor interface circuits will be derived, and the figure of merit (FoM) that has been widely used to evaluate the energy efficiency of such circuits will be discussed.

A. Minimum Energy Consumption Analysis of the Thermal Noise Limited Interface

The signal variation in most capacitive sensor applications has a bandwidth of less than several hundreds of kHz and includes the static/initial level (0 Hz). To convert the sensor capacitance into a charge that can be subsequently measured by the readout circuit, a periodic excitation (incessant recharging of the sensor capacitance) is widely preferred, as in this way, the input offset and drift of the readout electronics are easily eliminated. Ideally speaking, capacitive sensors do not dissipate static power (assuming no loss in capacitance). In this case, the fundamental lower boundary is given by the energy consumption associated with the periodic excitation. As shown in Fig. 1, there are mainly two ways to excite a capacitive sensor: the discrete-time (DT) approach, which charges the capacitive sensor and then sampling its charge,

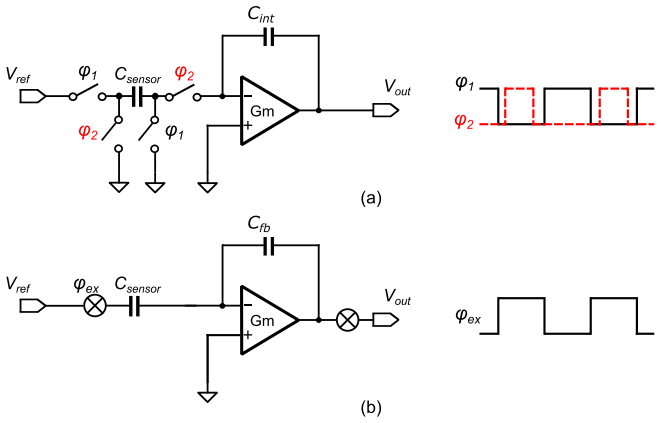

Fig. 1. Capacitive sensor with the (a) DT interface approach and (b) CT interface approach.

and the continuous-time (CT) approach, which simultaneously recharges the sensor capacitance and senses the charge. The energy consumed in one clock cycle to charge and discharge the sensor, which, for both the DT and CT approaches, is given by:

$$E = C_{sensor} V_{ref}^2. \tag{1}$$

Here, it is assumed that the resolution is limited by the thermal noise. For the DT approach (Fig. 1a), the required energy is limited by the noise charge sampled at the end of ϕ_1 and the noise of the OTA during ϕ_2. This sums up to $(1+\gamma)\cdot kTC_{sensor}$, where the factor γ accounts for the excess noise contribution of the OTA and equals 4/3 for an OTA whose noise is dominated by an input differential pair in strong inversion [15]. As explained in [12], the signal-to-noise ratio (SNR) is given by:

$$SNR = \frac{Q_{sig}^2}{(1+\gamma)\cdot kTC_{sensor}} = \frac{C_{sensor}V_{ref}^2}{(1+\gamma)\cdot kT} = \frac{E}{(1+\gamma)\cdot kT}. \tag{2}$$

Hence, the minimum energy for a given SNR is:

$$E_{DT} = (1+\gamma)\cdot kT\cdot SNR. \tag{3}$$

In practice, many capacitive sensors have a certain parasitic capacitance C_{p} which contributes to the noise charge, further increasing the minimum required energy to:

$$E_{DT,p} = (1+\gamma)\cdot kT\cdot SNR\cdot\left(\frac{C_{sensor}+C_p}{C_{sensor}}\right)^2. \tag{4}$$

Therefore, minimizing C_{p} is critical in energy-constrained applications. This makes the system-level integration an attractive solution for energy efficiency of capacitive sensing systems [5], [10]. Although Eqs. (2) and (4) only consider a single charge transfer, they remain valid for conversions with multiple charge transfers since N-fold oversampling increases both the energy consumption and the SNR by a factor of N [16].

In contrast, the CT approach does not suffer from kTC noise. Therefore, its minimum energy consumption for a given SNR is lower. The SNR of the CT approach is mainly limited by the noise of the charge amplifier (Fig. 1b). Here, the same OTA as the one used in the DT approach is used. At the output of the charge amplifier, the output noise density v_{no} is given by:

$$v_{no}^2 = 4kT\cdot\frac{\gamma}{g_m}\cdot\left(\frac{C_{sensor}+C_{fb}}{C_{fb}}\right)^2, \tag{5}$$

where g_m is the transconductance of the input MOS transistors whose input and output capacitance are not considered here. Assuming the bandwidth is determined by the transconductance g_m of the OTA and the sensor capacitance C_{sensor}, the effective noise bandwidth BW is given by:

$$BW = \frac{g_m}{4\cdot C_{sensor}}. \tag{6}$$

The input-referred noise charge is, therefore:

$$q_{noise,CT}^2 = \frac{v_{no}^2\cdot BW\cdot C_{sensor}^2}{Gain^2} = \gamma kT\cdot\frac{(C_{fb}+C_{sensor})^2}{C_{sensor}}. \tag{7}$$

Then, the energy consumption, E_{CT}, can be written as:

$$E_{CT}^2 = \gamma kT\cdot SNR\cdot\left(\frac{C_{fb}+C_{sensor}}{C_{sensor}}\right)^2. \tag{8}$$

Considering the parasitic capacitance, C_p, of the sensor and the input capacitance C_{ia}, this energy equals:

$$E_{CT,p}^2 = \gamma kT\cdot SNR\cdot\left(\frac{C_{fb}+C_{sensor}+C_p+C_{ia}}{C_{sensor}}\right)^2. \tag{9}$$

Usually, due to the voltage gain of the charge amplifier, the value of $C_{fb}+C_{ia}$ is negligible compared to that of $C_{sensor}+C_p$. Therefore, E_{CT} can be simplified to:

$$E_{CT,p}^2 = \gamma kT\cdot SNR\cdot\left(\frac{C_{sensor}+C_p}{C_{sensor}}\right)^2. \tag{10}$$

Eq. (10) shows that to achieve the same resolution, the energy limit of the CT approach must be smaller than that of DT by a factor of about $\gamma/(1+\gamma)$. Moreover, when a low pass filter is used after the charge amplifier, the effective noise bandwidth could be further limited, resulting in even less energy consumption for a given resolution. In practice, as described in Section III, since sampling the charge simplifies the circuit required for subsequent processing, DT interfaces are still widely used.

It is worth mentioning that, theoretically, it would be sufficient to use a single charging of the sensor capacitance at a certain voltage to determine the initial value of the measurand, and then only monitor the charge variations (by maintaining constant the voltage over the sensor capacitance) resulting from variations in the measurand around its initial value. This would dramatically decrease the minimum energy consumption related to the sensor itself (Eq. 1). However, this would not only require a capacitive sensor without any leakage but would also introduce significant additional requirements to the readout electronics, which would lead to much more power being consumed in the readout electronics than would be saved from recharging the sensor capacitance. An interesting capacitive sensor interface is presented in [33], which

is an intermediate solution between recharging the sensor capacitance at every reading, and a single initial charging. This solution demonstrates the best power efficiency FoM (see Table I).

B. Energy Efficiency Metrics

As indicated in [16], one way to quantify the progress in capacitive sensor interface designs is to track the FoM adopted from ADCs, given by:

$$FoM = \frac{E}{2^{ENOB}}. \tag{11}$$

where the *ENOB* is defined as:

$$ENOB = \frac{SNR - 1.76dB}{6.02dB}. \tag{12}$$

For simplicity, nonlinearity is ignored. Eq. (11) indicates that to obtain 2x better resolution, the energy consumption needs to be doubled to maintain a constant FoM. However, this is only valid for quantization noise-limited designs, such as SAR CDCs. When the design is thermal noise limited, the energy consumption needs to quadruple to achieve 2x better resolution. Although the Schreier FoM (FoM_S), a complement to the Walden FoM_W for thermal noise limited ADCs, is popular in the field of ADC design, it has not been widely adopted so far in capacitive sensor interface circuits.

Moreover, as discussed above, the C_p of the sensors would increase the minimum energy consumption for a given SNR. Also, when the measured capacitive sensor has a much larger baseline capacitance, a significant part of the energy is burned on charging and discharging the baseline capacitance, and not extracting the signal, leading to substantial degradation of the FoM. While most of the reported application-oriented capacitive sensor interfaces include information about the inevitable parasitic and baseline capacitance, this is often not the case with other reported solutions operating in an ideal environment. This makes it difficult to compare their power efficiency fairly.

Notably, most CDC designs which achieve high energy efficiency in terms of the FoM are either SAR CDCs or hybrid CDCs, which utilize a SAR architecture and are measured with a programmable on-chip capacitive array to minimize the degradation due to parasitic capacitance [6]–[9].

III. State-of-the-Art Capacitance Sensor Interfaces

A. Self-Oscillating Capacitive Sensor Interfaces

A widely used approach to sense capacitance is to modulate the sensing capacitance into another physical quantity that can be easily quantized by modern electronic systems. One popular solution is to transfer the capacitance to a time signal that can be digitized with a time-to-digital converter (TDC). A simple capacitance-to-time converter is illustrated in Fig. 2. The unknown capacitance is discharged by a controlled current source I_{int} resulting in a modulated time period that can be

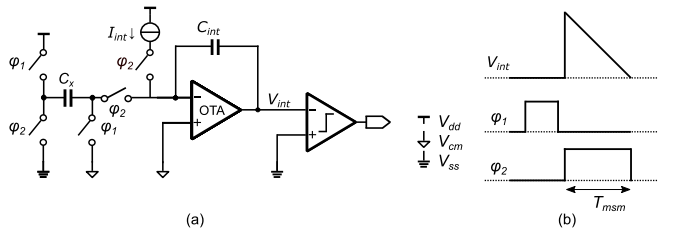

Fig. 2. (a) Circuit and (b) timing diagram of a simple capacitance-to-time converter [2].

calculated in terms of the power supply voltage V_{dd} and sensor capacitance C_x:

$$T_{msm} = \frac{V_{dd}}{I_{int}} \cdot C_x. \tag{13}$$

Researchers have explored various techniques to quantize this time information. Solutions include pulse width modulation (PWM) [17], [18] and period modulation (PM) [19]–[23], where the sensed physical capacitance is proportional to the pulse duration and pulse period, respectively.

PM-based designs have drawn researchers' attention due to their simplicity and compactness. A basic period modulator is realized with a relaxation oscillator that consists of a capacitance-to-time converter and a comparator. Since the oscillator frequency is inversely proportional to T_{msm}, the capacitance value can be extracted by counting the number of output periods using a simple digital divider [20]–[22]. This provides great flexibility, as measurement time can easily be traded for resolution. In addition, it is operated asynchronously and does not require a clock signal. The interface can be deployed close to the sensor and be connected to a remote microcontroller using a limited number of wires.

However, as indicated in (1), T_{msm} depends on the absolute values of V_{dd} and I_{int}, resulting in an ill-defined sensitivity to the sensing capacitance. One widely used auto-calibration scheme is shown in Fig. 3 [19]–[21]. In addition to the sensing element C_x, an auxiliary capacitance C_o,which controls the sampling phase, and a reference capacitance C_{ref}, are connected to the sensing network. This interface converts C_o, C_x, and C_{ref} into three time periods: T_o, T_x, and T_{ref} respectively. Finally, the following ratio metric output can be obtained:

$$M = \frac{T_x - T_o}{T_{ref} - T_o} \cdot C_{ref}. \tag{14}$$

This auto-calibration technique naturally realizes dual-slope operation, and thus, the measured result is independent of V_{dd} and I_{int}. In addition, it cancels any offset and gain errors in the time periods, thus greatly relaxing the circuit design requirements.

Nevertheless, the sensing capacitance range is still limited by the size of C_{int}, as indicated in Fig. 2, to prevent any possible overload of the integrator input. Heidary and Meijer [23] reported a negative feedback embedded design to extend the dynamic range of the capacitance sensor interface without a large on-chip capacitor C_{int}. As illustrated in Fig. 4, instead of switching the bottom plate of the sensing capacitor directly between V_{dd} and ground, this work applies negative feedback

TABLE I
COMPARISON OF STATE-OF-THE-ART CDCS

	Architecture	Process (nm)	Range (pF)	Power (μW)	Meas. Time (μs)	Resolution (fF)	Energy (nJ)	SNR (dB)	FoM (fJ/conv-step)
2013 Jiang [46]	SAR	180	0-9.6	9.4	5	2.5	0.047	62.6	43
2014 Ha [7]		180	2.5-75.3	0.16	4000	6	0.64	81.8	183
2017 Omran [6]		180	0-12.66	6.44	16	1.1	0.103	70.6	33
2019 Xin [34]		65	2.97-7.67	0.024	20	6.19	0.0048	48.6	22
2019 Hussaini [11]		180	0-10.8	0.33	100	6	0.033	56.5	61
2020 Xin [33]		65	0.46-5.89	0.093	10	7.3	0.00094	48.4	4.3
2013 Tan [5]	ΔΣM	160	0.54-1.06	10	800	0.07	8	83.9	3400
2017 Yang [13]		350	6.0-22.0	760	10500	0.042	7980	102.6	74000
2017 Narasimman [47]		180	0-10	50.4	125	0.4	6.3	79.2	840
2020 Jiang [14]		180	0-10	560	1	0.042	560	98.5	8000
2012 Xia [12]	Zoom-SAR+ΔΣM	350	8.4-11.6	1490	20	0.065	418	84.8	21000
2014 Oh [41]		180	0-24	33.7	230	0.16	7.75	94.7	175
2019 Park [10]		180	0-18.12	2.92	850	1.24	2.63	74.3	660
2019 Tang [8]		40	0-5	6.64	12.5	0.29	0.083	75.8	16
2012 Tan [19]	PM	350	0-6.8	211	7.6	0.208	1603	83.03	138600
2015 He [24]		160	0-8	14	210	1.44	2.94	65.6	1870
2015 Jung [26]	Delay-Chain	40	0.7-11.3	1.84	19	12.3	0.035	49.7	140
2017 Sanyal [45]	SAR +VCO	40	0-5	75	1	1.1	0.075	64.2	55

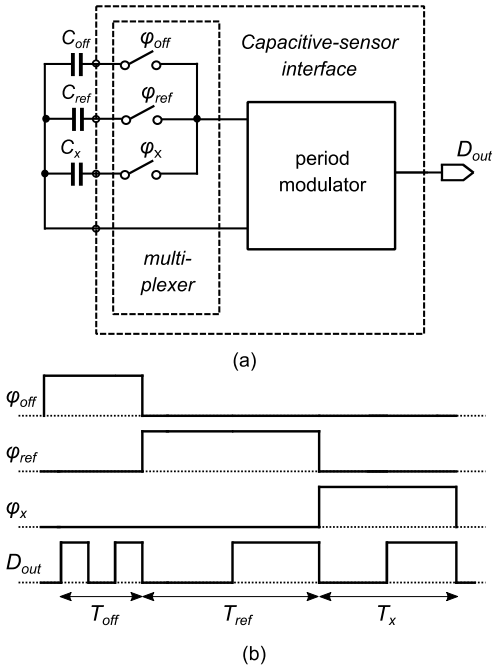

Fig. 3. (a) Circuit diagram and (b) associated timing diagram of the period-modulation-based interface employing three-signal autocalibration [15]–[17].

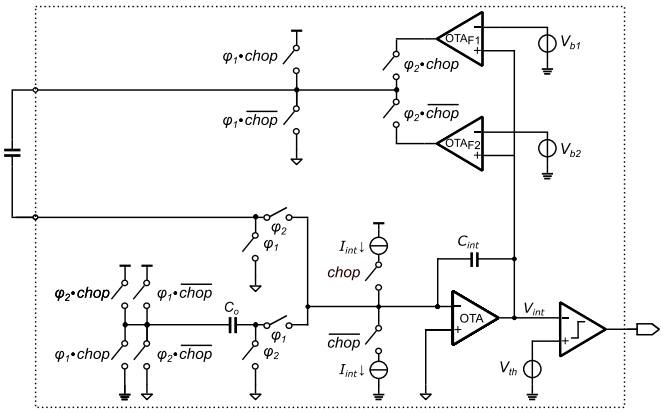

Fig. 4. Block diagram of the period modulator-based capacitive sensor interface with negative feedback [15], [19].

to control the switching circuitry, which dynamically adjusts the charging or discharging speed to prevent overload. As a result, a sensing capacitor larger than C_{int} can be supported in such a design.

To boost energy efficiency, Tan *et al.* [19] combined the negative feedback loop with a chopping and auto-calibration technique. Errors due to low-frequency noise and offset of the interface circuit are eliminated by chopping. The auto-calibration technique eliminates offset errors due to comparator delay, and thus, a low-speed energy-efficient comparator can be used. Combining these merits, it enables simple energy-efficient analog implementation that reduces the energy consumption of a PM-based design by two orders of magnitude. It achieves a 15-bit resolution with a 6.8 pF input capacitance range while consuming 64 μA from a 3.3 V supply. On top of that, He *et al.* [24] further improved the energy efficiency by driving C_x with a switched current source. It replaces the OTAs in the feedback loop with two comparators that can be implemented by simple Schmitt triggers. Also, dual-integrator capacitors are adopted to reduce the jitter accumulation. This interface achieves 13.1 ENOB with an input range of up to 8 pF while consuming only 14 μA from a 1 V supply. The measurement time is 6.9 ms.

Another key limiting factor for the interface to achieve sufficient resolution with high energy efficiency is the need to charge and discharge the large baseline capacitance. Oh *et al.* [25] employed iterative charge subtraction using a configurable capacitor bank to cancel the baseline capacitance. It equivalently zooms in and amplifies the variable input region, thus reducing the conversion time and energy. Dual-precision comparators are adopted to reduce comparator power while maintaining high accuracy during slope conversion. As a

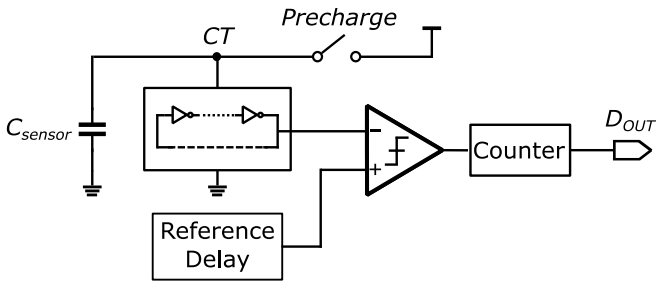

Fig. 5. Delay chain-based capacitance sensor interface [22].

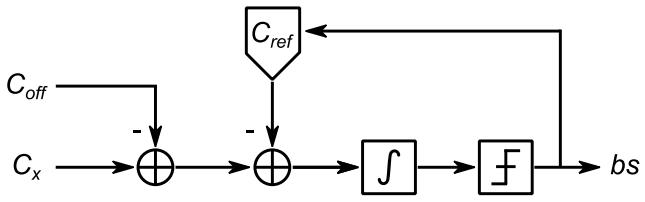

Fig. 6. Example of a capacitance sensor interface based on a $\Delta\Sigma$M.

result, it extends the conversion range up to 30 pF with good energy efficiency.

In [26], Jung *et al.* reported another capacitance-to-time conversion scheme, as shown in Fig. 5. In this work, a delay chain is used to discharge the sensing capacitor. The time taken for the delay in the inverter chain to catch up with the reference delay is proportional to the sensed capacitance. This technique extends the sensing range to 10 nF without a significant hardware cost. It is highly digital, presenting great energy efficiency reaching 141 fJ/conversion step. However, its resolution is limited to an ENOB of 8 due to nonlinearity in the delay chain discharge.

In summary, PM-based capacitance sensor interfaces have been widely used due to their simplicity. Efforts have been devoted to improving the resolution (e.g., 15 bits) and input capacitance range (e.g., 30 pF). However, achieving high resolution requires a highly oversampled digital counter with a clock frequency that doubles with every extra bit of resolution. Hence, the use of these interfaces is limited to energy-constrained applications, especially those powered by energy harvesters or coin batteries in modern sensor nodes.

To improve energy efficiency while maintaining a good conversion resolution, researchers have explored $\Delta\Sigma$ techniques that can operate at modest clock frequencies. They are inherited from $\Delta\Sigma$ modulators ($\Delta\Sigma$Ms), which naturally suit high-resolution applications [5], [27]–[30]. A simplified model is illustrated in Fig. 6, where a single-bit quantizer and a reference capacitor C_{ref} are adopted. It converts the sensed capacitance into a pulse-density modulated bit-stream through $\Delta\Sigma$ operation. The baseline capacitance of the sensing element is compensated by switching an offset capacitor C_{off} with a polarity opposite to C_x. Every clock cycle, a charge $V_{ref} \cdot (C_x - C_{off})$ is added to the integrator. The reference capacitor adds or subtracts a charge $V_{ref} \cdot C_{ref}$ to or from the integrator. After N clock cycles, negative feedback ensures that the charge from the sensing capacitor will be balanced by the charge delivered by the reference capacitor:

$$(C_x - C_{off}) - \mu \cdot C_{ref} + (1 - \mu) \cdot C_{ref} = 0 \qquad (15)$$

where μ represents the density of ones in the bit-stream. Then, the sensing capacitance can be calculated as:

$$C_x = C_{ref} \cdot (2\mu - 1) + C_{off} \qquad (16)$$

Thanks to the noise shaping feature of the $\Delta\Sigma$M, the conversion time, which is captured by the oversampling ratio (OSR), can be reduced by increasing the loop filter order without changing the resolution of the quantizer. Compared to the aforementioned PM-based interfaces, this provides another degree of freedom to improve resolution. Hence, it reduces power consumption by obviating the high-frequency clock.

The power of a $\Delta\Sigma$ capacitance sensor interface is dominated by the power-hungry OTAs used in the loop filter, which defines the thermal noise limited resolution. To improve the OTA's energy efficiency, Tan *et al.* [5] reported a current-starved cascoded inverter-based OTA, which realizes current-reuse to achieve noise reduction and boost the energy efficiency by two times [31]. To reduce the required OSR while maintaining high resolution, a 3rd-order loop filter is employed in this design. The entire system is auto-zeroed to reduce offset errors due to charge injection from the switches. Owing to the energy-efficient OTA design and the reduced OSR (e.g., 200), it improved the energy efficiency by more than two times compared to the state-of-the-art at that time. The capacitance interface achieves an effective resolution of 12.5 bits in a measurement time of 0.8 ms while consuming 8.6 μA from a 1.2 V supply.

Capacitance sensor interfaces based on the $\Delta\Sigma$M have also been widely adopted in the market. For example, the AD7745 [4] is a 24-bit capacitance interface (21 ENOB) with an accuracy of $\pm$4 fF and a nonlinearity of 0.01%. Such ICs are quite useful for building standalone measurement systems for capacitive sensors within the range of $\pm$4 pF. There are also low power $\Delta\Sigma$M-based CDCs available, such as the AD7151, which only consumes 70 μA while providing 12-bit resolution [32].

Although $\Delta\Sigma$Ms have improved substantially compared to their PM-based high-resolution predecessors, their energy efficiency is still limited by the power-hungry OTAs in their high-order loop filters. Moreover, the sensing elements are repeatedly charged and discharged due to the OSR required in the conventional single-bit $\Delta\Sigma$ loop, which consumes considerable power.

B. SAR-Based Capacitive Sensor Interfaces

The successive approximation register (SAR) analog-to-digital converter (ADC) is well known for its excellent energy efficiency when targeting applications with medium resolution and medium speed requirements. As a switched capacitor feedback digital-to-analog converter (DAC) is typically used in a SAR ADC, the SAR approach can be conveniently used for capacitance sensing. By taking advantage of the great energy efficiency of the SAR approach, SAR-based capacitive sensor interfaces [6], [7], [33], [34] also achieve excellent energy

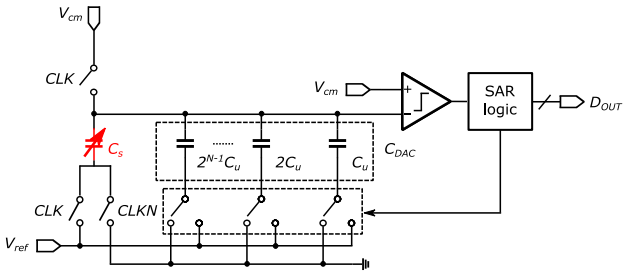

Fig. 7. Basic architecture of a direct SAR capacitive sensor interface [35].

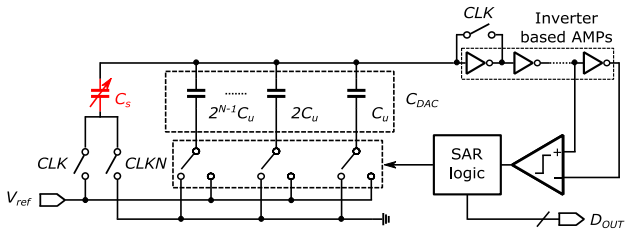

Fig. 8. Direct SAR capacitive sensor interface with a chain of inverter-based amplifiers [6].

efficiency amongst other capacitive sensor interface architectures. In general, SAR-based capacitive sensor interfaces can be divided into two categories: 1) direct SAR capacitive sensor interfaces and 2) capacitive sensor interfaces, which include a capacitance to voltage front-end (CVFE) and a SAR ADC. In this sub-section, several SAR-based capacitive sensor interfaces from both categories will be reviewed.

1) Direct SAR Capacitive Sensor Interface: The direct SAR capacitive sensor interface [35] resembles a conventional SAR ADC, as shown in Fig. 7. The sensing capacitor C_s is directly incorporated into the DAC capacitor array of the SAR ADC. After the sampling phase (enabled by *CLK*), the sensor interface performs a binary search algorithm to approximate the C_s value with the DAC capacitors C_{DAC} in N steps, where N is the number of bits of the sensor interface. An N-bit binary digital output D_{out} is produced directly after the conversion. Furthermore, since the entire sensor interface consumes only dynamic power (except for leakage) when a dynamic comparator is used, ultra-low absolute power consumption can be achieved inherently at a low sampling rate. Power consumption as low as 4.2 nW has been reported [36].

As has been discussed in [6], the conventional direct SAR capacitive sensor (Fig. 7) suffers from comparator offset induced error, which is a function of C_s and its parasitic capacitance. As a consequence, the sensing resolution is degraded, thereby degrading the energy efficiency. To tackle this issue, [6] proposed to insert a chain of open-loop amplifiers (Fig. 8) between the DAC and the comparator latch. Thanks to this approach, the aforementioned error can be reduced by a factor of A (open-loop gain of the amplifiers), which significantly improves the achievable resolution. Cascode inverter-based amplifiers are used in [6] for higher open-loop gain and better energy efficiency, and the amplifiers are duty-cycled to minimize the static power consumption.

When compared to a standalone SAR ADC, a direct SAR capacitive sensor interface with similar performance (e.g., effective number of bits) usually consumes more energy per conversion, especially when C_s is large. This is mainly due to two reasons: firstly, an extra amount of energy per conversion is consumed to charge C_s in a direct SAR capacitive sensor interface. Secondly, relatively large DAC capacitors are needed in a direct SAR capacitive sensor interface when dealing with large C_s values, while for a standalone SAR ADC, the size of C_{DAC} is determined by the noise and/or the matching requirements, which usually leads to smaller DAC capacitors and less energy consumption.

2) Switched Capacitor Integrator CVFE Followed by a SAR ADC: Besides the direct SAR approach, the SAR-based capacitive sensor interface can also be implemented with a CVFE and a SAR ADC. Fig. 9 shows an architecture [7] that uses a switched capacitor (SC) integrator as the CVFE. The correlated double sampling (CDS) technique (Fig. 9) is employed in that design to reduce 1/f noise and offset of the operational transconductance amplifier (OTA) and to provide a differential signal to the differential SAR ADC. After the two sampling phases (enabled by *CLK1* and *CLK2* respectively), a differential voltage equal to $2 \cdot (C_s - C_r) \cdot V_{DD}/C_{DAC}$ is sampled on the C_{DAC} (aggregated DAC capacitance of the SAR ADC). Then, the ADC starts the conversion and produces the digital outputs after a conversion delay. Instead of comparing C_s with the ADC DAC capacitors as in the direct SAR approach, a reference capacitor C_r is used for comparison. Therefore, large C_s values can be easily supported by adjusting the value of C_r, while a small C_{DAC} can be used to minimize the energy consumption of the SAR ADC. Furthermore, thanks to the virtual ground created by the OTA, the readout result is not sensitive to the parasitic capacitance of C_s.

3) Capacitive Bridge CVFE Followed by a SAR ADC: The architecture shown in Fig. 9 provides a nice way to separate C_s from the DAC capacitors of the SAR ADC, such that the energy efficiency of the SAR ADC can be better optimized. However, an OTA is needed for charge transfer. The fully dynamic architecture proposed in [34] avoids using power-hungry amplifiers, as shown in Fig. 10. It includes a single-armed capacitive bridge and a 10-b differential asynchronous SAR ADC. Instead of using an SC integrator for charge transfer, the bridge output is directly sampled on the C_{DAC} through passive charge sharing. As indicated by the waveforms in Fig. 10, a passive CDS approach is used to provide a differential voltage to the SAR ADC. Similar to the SC integrator CVFE, the capacitive bridge CVFE also separates C_s from the ADC DAC capacitors. A small C_{DAC} is not only beneficial in minimizing the SAR ADC energy consumption, but it also helps to reduce signal attenuation caused by the charge sharing between the capacitive bridge and C_{DAC}. As shown in [34], the total DAC capacitance is only 300 fF with 250 aF unit capacitors to save ADC energy while achieving sufficiently low kT/C noise and sufficient linearity. The asynchronous dynamic logic in [37] is used to minimize the number of logic gates, which helps to reduce both active and leakage power. Furthermore, the leakage power of the entire sensor interface is minimized down to only 0.1 nW such that the energy

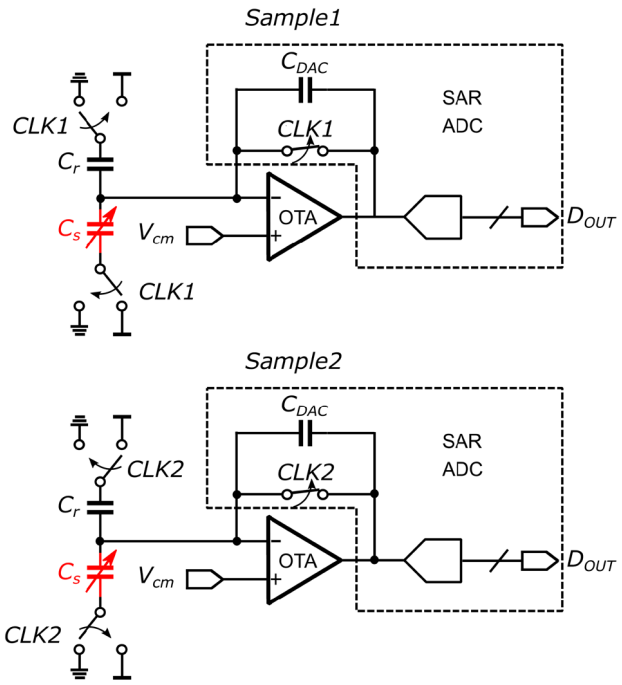

Fig. 9. Capacitive sensor interface architecture that includes a switched capacitor integrator CVFE, SAR ADC [7], and illustration of the correlated double sampling technique.

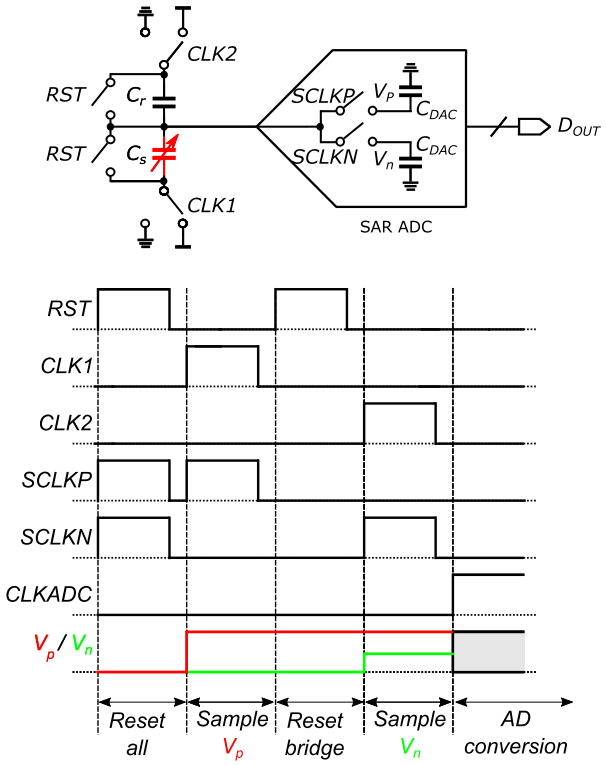

Fig. 10. Capacitive sensor interface architecture that includes a capacitive bridge CVFE, a SAR ADC [34], and its operation waveforms.

efficiency can be well maintained even at very low sampling rates. It should be noted that this architecture is especially beneficial when the parasitic capacitance of C_s is relatively small ($<C_s$), as a large parasitic capacitance would degrade the readout SNR due to signal attenuation during the passive charge transfer. Although no amplifiers are used, and the SAR ADC can be fully optimized in this architecture, the overall energy efficiency of the sensor interface is still worse than that of a standalone SAR ADC. This is mainly because the capacitive bridge needs to be reset to ground and then charged to VDD twice in a complete measurement. Consequently, the energy consumption of the sensor interface could be dominated by the capacitive bridge when C_s is large, which becomes the bottleneck to further improving energy efficiency.

To reduce the energy consumption of the capacitive bridge, thus improving the FoM of the capacitive sensor interface towards the FoM of a standalone SAR ADC, [33] proposed an energy-efficient charge reuse technique. The concept of charge reuse in a capacitive bridge CVFE is shown in Fig. 11 (a). Instead of resetting the capacitive bridge for each measurement, the reset phase is only applied in the first measurement of a group of N measurements. After measurement 1 is finished, all the charge is preserved by floating the capacitive bridge and resetting the C_{DAC} to the state before conversion. The preserved charge is then reused in the subsequent measurements (measurement 2 to N), which do not have a reset phase. Thus, the capacitive bridge only needs to be fully charged once over N measurements, which means the bridge energy consumption on average can be reduced by a factor of N. Due to the leakage from the reset switch, the preserved charge will slowly decline over time, which will cause errors in measurements with charge reuse. Thus, measurements with a reset should be performed from time to time (once every N measurements) to remove the accumulated error. In order to maximize N while not causing large errors, small high-V_{th} NMOS transistors are used as the reset switches to reduce its leakage current during charge preservation, and a reference bridge is further used to partially compensate for the leakage error in the sensing bridge, as shown in Fig. 11(b). As a result, charge reuse over 80 consecutive measurements is achieved, which greatly reduces the bridge energy consumption. Thanks to this approach, a record low FoM of 4.3fJ/conv-step is achieved in [33].

C. Hybrid Capacitive Sensor Interfaces

$\Delta\Sigma$Ms reach high resolution but suffer from low energy efficiency. In contrast, SAR-based designs achieve admirable energy efficiency with moderate conversion resolution. An attractive direction that hybridizes those architectures and combines their merits has been reported recently. The sensing capacitance is first converted by a coarse SAR for the MSB decisions. The residue is then processed by a $\Delta\Sigma$ loop to realize fine LSB conversions. This provides a more balanced trade-off between conversion accuracy and energy consumption.

Xia *et al.* [12] pioneered an early implementation of this design. Their work adopts a 6-bit SAR to cancel the baseline capacitance of the sensing element, equivalently performing a coarse quantization of C_x. By doing so, it realizes an offset cancellation capacitor varying between 8.4 pF and 11.6 pF in steps of 50 fF. In a normal conversion, the sensing element

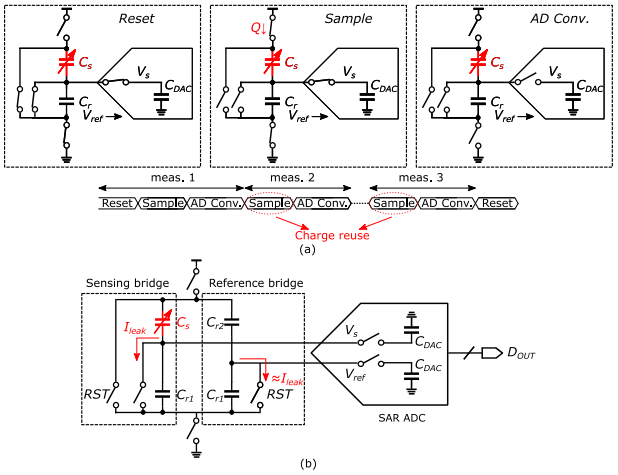

Fig. 11. (a) Concept of charge reuse in a capacitive bridge CVFE, and (b) architecture of the capacitive sensor interface with energy efficient charge reuse [33].

is converted by a 3rd-order $\Delta\Sigma$ loop to achieve 15.3 ENOB while consuming 4.5 mA from a 3.3 V supply.

Inspired by the zoom-ADCs [38-40], Oh *et al.* [41] reported a zoom capacitance sensor interface that further leverages the merits of the energy-efficient SAR. It adopts a 9-bit SAR first-stage for the $\Delta\Sigma$ loop to zoom into a sufficiently small residue for the fine quantization. It only requires an OSR of 32 with a 2nd-order loop filter to reach 13.8 ENOB. The power-hungry OTAs are bypassed during the SAR conversion to save energy. Thanks to the moderate order number and low OSR, it achieves an energy efficiency of 175 fJ/conversion step, representing the state-of-the-art at that time.

To further reduce the quantization noise, Park *et al.* [10] reported a dual-quantization-based design. In the second-step fine quantization, on top of the single-bit $\Delta\Sigma$ loop, it cascades an extra SAR converter to realize a 1-0 MASH architecture that reduces the system quantization noise [42]. However, it requires an additional SAR quantizer, and the MASH architecture imposes stringent matching requirements on the cascaded paths.

Although the zoom architecture lowers the $\Delta\Sigma$M power consumption by reducing the loop filter order and the required OSR, e.g., the 3rd-order loop with 200 OSR in [5] to the 2nd-order loop with 32 OSR in [41], it still dominates the overall interface. One can embed a multi-bit quantizer to further simplify the loop filter design. However, to ensure conversion linearity, dynamic element matching (DEM) is usually required to address mismatch in the multi-bit feedback DAC, which consumes extra power and area.

Recently, time domain (TD) analog signal processing techniques have become popular due to their power efficiency in advanced CMOS technologies. They represent signals using time-related variables, such as frequency and phase, which can be processed through mostly digital circuits, thus benefiting from transistor scaling. Recent advancements in $\Delta\Sigma$Ms [43], [44] have replaced the conventional OTA-based active-RC integrator with a voltage-controlled oscillator (VCO)-based integrator, which offers several key advantages: 1) the VCO is mostly digital and consumes low power; 2) it provides infinite DC gain in the phase domain and thus is well-suited for high

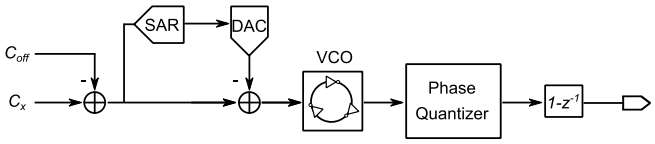

Fig. 12. Two-step design adopting the open-loop VCO-based $\Delta\Sigma$M [41].

precision applications that demand high DC loop gain; 3) it has intrinsic spatial phase quantization enabling simple multi-bit quantization using only digital gates.

Sanyal and Sun [45] introduced the time domain signal processing to the capacitance sensing field with an open-loop VCO-based design, as shown in Fig. 12. It achieves low power consumption by eliminating power-hungry OTAs. With the intrinsic phase quantization, a 3-bit quantizer is implemented only by XOR gates, which enables a low OSR design (e.g., 3) and further reduces the energy consumption. However, the PVT-sensitive VCO gain variation causes inter-stage gain error, which degrades the conversion accuracy. A background calibration loop is implemented to track the VCO gain, which increases the design complexity making it unsuitable for single-shot measurement in sensor node applications due to the long convergence time.

To further improve the energy efficiency as well as the PVT robustness, Tang *et al.* [8] reported an incremental zoom capacitance sensor interface with a closed-loop time domain $\Delta\Sigma$ modulator (TD$\Delta\Sigma$M), as shown in Fig. 13. In contrast to the previous two-step designs, it only requires a one-time charge transfer that converts the sensing capacitance into a voltage signal, which saves considerable energy. Then the zoom operation is performed by an 8-bit SAR and a closed-loop TD$\Delta\Sigma$M. By operating the TD$\Delta\Sigma$M in the closed-loop, the inter-stage gain is defined by the capacitor ratio, which is accurately matched by merging SAR and $\Delta\Sigma$M DACs. Thus, the VCO gain variation has a negligible impact on the conversion performance, and it is PVT-robust and calibration-free. A phase and frequency detector (PFD)-based phase quantizer is adopted to obtain an extra quantization bit. Hence, the 7-stage ring oscillator realizes a 4-bit time domain quantizer, which further reduces the required OSR for the target resolution. The dual-VCO integrator brings the intrinsic clocked averaging (ICLA) capability to address the $\Delta\Sigma$M feedback DAC mismatches and obviate the need for a dedicated DEM block. To suppress the flicker noise and offset, system-level chopping is performed. As a result, this work realizes 12.3 ENOB with only a 1st-order loop filter and a low OSR of 15. It achieves an FoM of 16 fJ/conversion-step with a 5-pF input capacitance range, advancing state-of-the-art energy efficiency by two times among designs with similar resolution.

IV. Discussion

Optimizing the power efficiency of a capacitive sensor aimed at a target resolution requires a thermal noise limited design. This means that quantization noise should be suppressed below thermal noise with only a fraction of the total power, while most of the power is consumed achieving the target thermal noise level. This can be seen from Fig. 14, which plots the resolution and FoM of capacitive sensors of the

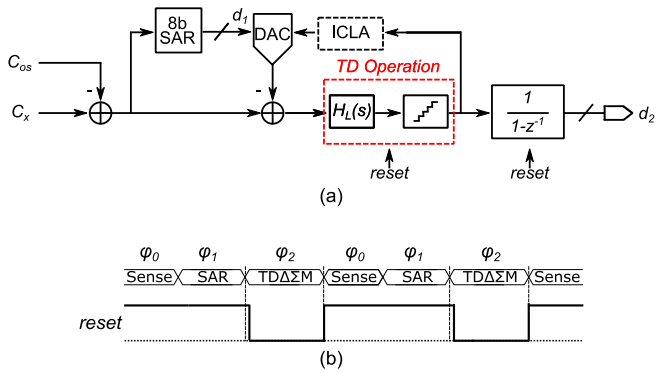

Fig. 13. (a) Architectural diagram and (b) timing diagram of the zoom CDC with the closed-loop TDΔΣM [4].

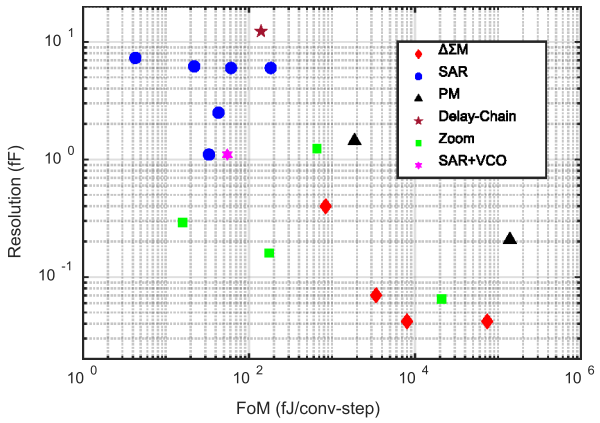

Fig. 14. Capacitance resolution versus FoM of state-of-the-art CDCs.

various architectures reviewed in this article. The performance of each design is summarized in Table I.

In the high-resolution space (<0.1 fF), ΔΣM-based readout circuits demonstrate the best efficiency. With a front-end circuitry similar to those described in Section II, they inherently achieve a thermal noise limited design.

For medium to low resolution, on the other hand, SAR CDCs stand out because, with every extra comparator decision, their quantization noise is reduced by half, helping them quickly approach the thermal noise limited regime. Their use for high resolution is limited because a low noise comparator would be required, despite there being only one thermal noise critical comparator decision. As a result, power is wasted in the noncritical bit decisions. Also, mismatch in their DAC must also be tackled, significantly increasing power and complexity.

The zoom architecture, employing a SAR front-end and back-end based on the ΔΣM, offers the best of both worlds. The SAR front-end reduces quantization noise in a very efficient manner while the job of suppressing thermal noise is left to the back-end stage. Hence, the SAR comparator no longer needs to be designed for low noise. Indeed, as shown in Fig. 14, zoom designs extend the efficient operation of SAR CDCs to higher resolutions.

V. Conclusion

In this article, the architecture and circuit techniques for high resolution and low power readout circuits for capacitive sensors are reviewed, and an analysis of the thermal noise limited fundamental limit for energy consumption per conversion is presented. A survey of recent state-of-the-art CDC designs shows that the SAR and ΔΣM approaches achieve the best performance for low-to-medium and high resolution, respectively, while the advantages of the two can be combined in the zoom architecture. Since we are approaching the absolute theoretical efficiency limits, defined by the power dissipation of the capacitive sensors' excitations, the remaining part to explore is to make the capacitive sensor interfaces "smarter" and "customized to application." This is promising to further extend the ultra-high energy efficiency at system level.

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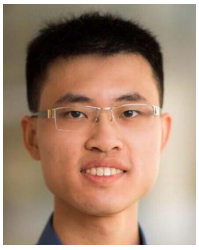

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