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***Abstract*— The 4H-silicon carbide (SiC) exhibits excellent material characteristics, particularly in high-temperature, high-power, high-frequency applications. However, the reliability of SiC-based devices operating in harsh environments is a critical concern. While time-dependent dielectric breakdown (TDDB) in conventional SiC devices has been extensively studied, its behavior in SiC MOSFETs within CMOS technology remains largely unexplored. In this work, we analyzed the effect of temperature and device size on TDDD failure time while employing failure analysis to identify two distinct failure structures. The finding of this research enhances the understanding of TDDB failure mechanisms and provides valuable insights for improving device reliability.**

Keywords—4H-SiC, Reliability, CMOS technology, Time-dependent dielectric breakdown

I. INTRODUCTION

The 4H-silicon carbide (SiC) exhibits excellent material characteristics, including wide bandgap, high breakdown electric field, thermal stability, and radiation resistance. The following Fig. 1 intuitively shows the comparison of the characteristics between silicon carbide and silicon. Thanks to its superior properties, SiC devices, such as MOSFETs, have been widely used in power electronics to cope with harsh operating conditions. Despite the success in power electronics, the development of SiC low-voltage integrated circuits (ICs) is still in the infant phase. The integration of SiC devices can provide an opportunity to develop advanced circuits with improved performance and reliability.

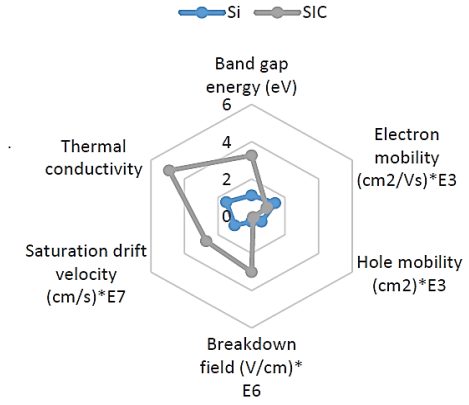

Fig. 1. Comparison between fundamental material properties SiC vs Si.

Recently, people have developed low-voltage SiC CMOS technology and demonstrated that it could be an excellent solution for harsh-environment ICs [1-3]. However, the reliability of MOSFET devices in this technology was not discussed yet, which is a critical concern when operating in a harsh environment. One of the major concerns in the reliability of SiC devices is time-dependent dielectric breakdown (TDDB) [4]. While the dielectric layer used in both SiC and Si devices is identical, the inherent properties of SiC can cause reliability issues with the device gate oxide layer. Specifically, SiC has a wide bandgap, indicating smaller conduction band offset values between SiO2 and 4H-SiC than SiO_2 on silicon substrate [5, 6]. This results in a significantly higher Foweler-Nordheim tunneling current. In the study conducted by B. J. Schlund et al., the dielectric breakdown phenomenon, especially under high electric fields, has been attributed to the involvement of Fowler-Nordheim tunneling [7]. Additionally, the imperfections of the SiO_2/SiC interface quality and the instinct defects in the gate oxide layer lead to gate oxide degradation [8]. To optimize the interface, post-oxidation annealing is a widely-used method, and nitric oxide (NO) [9, 10] and nitrous oxide (N_2O) [11, 12] are popular gases in the annealing process.

While TDDB has been extensively researched on classic SiC MOSFETs and MOS capacitors, there is no study on TDDB of 4H-SiC MOSFETs in this CMOS technology. Kevin Matocha et al. performed constant-voltage TDDB measurements on SiC MOS capacitors and DMOSFETs, and they found the effect of the acceleration parameter on the failure mechanism [13]. Cheng-Tyng Yen et al. conducted the TDDB test for MOS capacitors, and they found that the large number of oxide traps in the gate may not affect the gate oxide [14]. Amna Siddiqui et al. reviewed the performance of various high-k dielectrics in SiC MIS devices and provided a future perspective on dielectric materials [15]. The study conducted by K. Fujihiraa et al. compared the TDDB lifetime of thermal oxide and chemical-vapor-deposited oxide in SiC MOS capacitors [16].

This paper presents comprehensive TDDB characterization in 4H-SiC MOSFETs in CMOS technology, analyzing the temperature and device size effect on TDDB behavior. Also, we conducted the failure analysis of the damaged sample after the breakdown. The results of experimental data can further understand the

failure mechanism of TDDB and provide guidance for improving the reliability of SIC-based circuits in harsh operational environments.

II. Experiment

A. Sample Preparation

The silicon carbide CMOS process was conducted at Fraunhofer IISB. The cross-section view of TDDB test samples is shown in Fig. 2. In the fabrication process, MOSFET were fabricated on 4°-off 4H SiC (0001) substrates with a nitrogen-doped epitaxial layer grown on top. After the ion implantation to form N-well (NW), p-well (PW), shallow-p (SP), and shallow-n (SN), thermal annealing at 1700 °C is carried out to reduce the lattice damage. A 55 nm thick gate oxide was grown by dry oxidation at 1300°C. Subsequently, an annealing process in an atmosphere containing NO gas was carried out for 1 hour to enhance the interface state density. The gate electrode was a 500 nm thick poly-Si layer following the gate oxide deposition. Ohmic contacts on top pf n+ region and p+ region were achieved by alloying NiAl and Ti/Al at 980 °C. Finally, a multilayer Ti/Al/Ti metal stack was deposited and patterned.

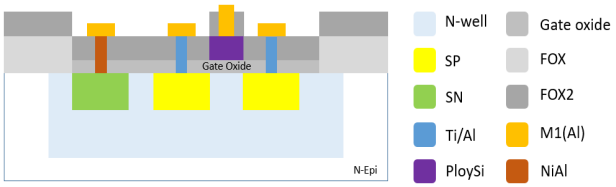

Fig. 2. A cross-section view of PMOS in Fraunhofer IISB CMOS technology.

B. Failure characterization

Time-dependent dielectric breakdown (TDDB) measurements were performed using a dedicated high-temperature measurement setup, as shown in Fig. 3. The microprobe chamber can be pumped down to 10^{-6} mbar and provide vacuum conditions. The temperature controller ensures the chamber can be heated up to 750 °C. And the monitoring of the leakage current behavior is achieved by the Keithley 2634B source measure unit (SMU). This setup allows for a detailed characterization of the leakage current behavior under various operating conditions. Besides, the failure analysis of failed samples is performed by focused ion beam (FIB) and scanning electron microscope (SEM) imaging.

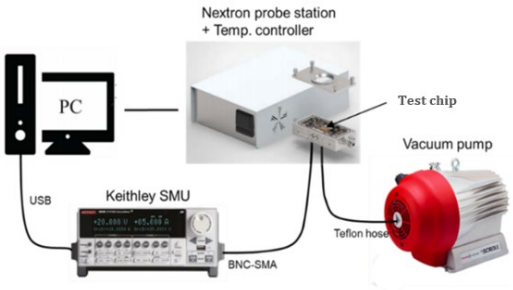

Fig. 3. The schematic overview of the test setup.

III. Results and Discussions

A. Size effect

The TDDB tests were conducted on various SiC MOSFET areas under 9 MV/cm electric fields. Fig. 4 presents the experiment results, indicating the relationship between the failure time and device size. The results revealed that smaller devices have prolonged TDDB lifetime compared to larger ones. This can be explained by the large device area increasing the potential for defects or impurities. And the existence of defects generated higher electric field intensity in localized areas, accelerated breakdown, and reduced the device reliability.

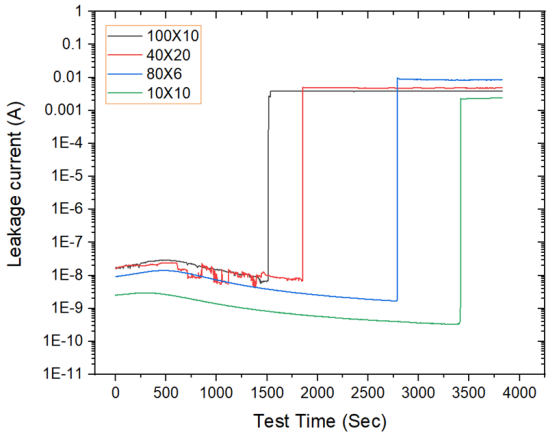

Fig. 4. The effect of device size on the gate leakage current.

B. Temperature effect

In addition to the study of device size effect on TDDB, the influence of temperature on TDDB behavior was investigated. The measurements were conducted at different temperatures and subjected to electric fields of 9 MV/cm. As shown in Fig. 5, the failure time decreased significantly with the increasing applied temperature. This observation is consistent with previous research on TDDB in SiC-based devices, where the elevated temperature expedites the gate oxide degradation [17]. At 200 °C, the device exhibited an extremely long lifetime compared to the higher temperature of 300 °C and 450 °C. This result indicates that the gate oxide degradation is less pronounced at low operating temperatures. However, when the applied temperature increased to 450 °C, the device breakdown failure time was significantly reduced. This result can be explained by the fact that when the load temperature is excessively high during the accelerated experiment, the failure mechanism of the device can change.

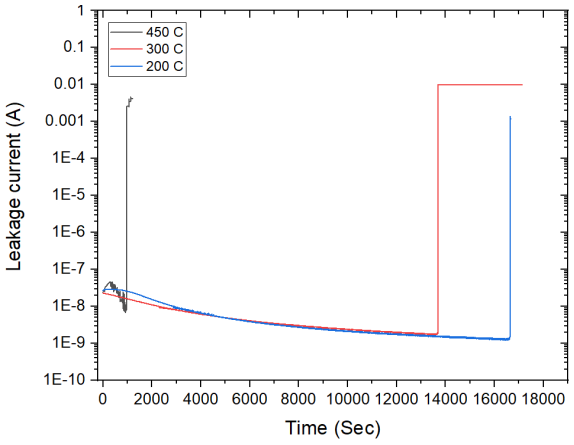

Fig. 5. The effect of operating temperature on the gate leakage current.

C. *Failure Modes*

The FIB-SEM analyzed the failure morphology of the SiC MOSFETs at different temperatures after the TDDB failures. Notably, a clear difference in failure morphology was observed at 200 °C and 450 °C. Fig xx shows the optical microscope and SEM images of SiC PMOS after TDDB test failure at 200 °C. From the optical image, shown in Fig. 6, the failure point on the gate surface is not apparent, and the cross-section image shows that the gate oxide degradation is less severe with voids in the oxide layer. However, no apparent failure point is evident in the substrate or gate layers.

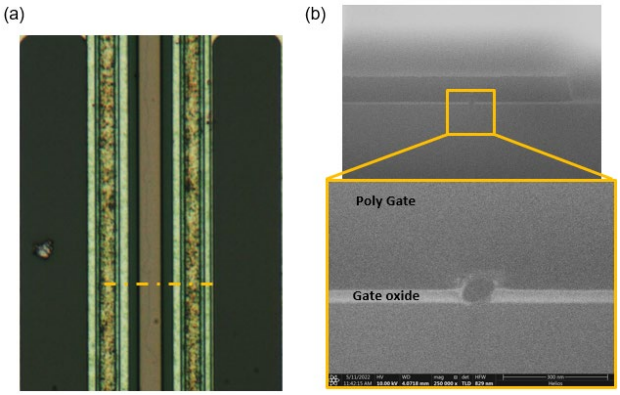

Fig. 6. (a) Optical microscope image of the breakdown PMOS device. A Dark crack at the gate area is shown. (b) Cross-section view of the failure device. Severe failure is in the gate oxide layer.

In contrast, at 450 °C, a different failure morphology was observed. As shown in Fig. 7 (a) and (b), small voids appear next to the device gate area. The SEM images, Fig. 7 (c) and (d), show the structural collapse in the polysilicon gate layer and the oxide layer, accompanied by the apparent voids in the gate layer. These morphologies are different from those observed at 200 °C, suggesting that the failure mechanism at high temperatures may involve thermal-induced degradation and breakdown.

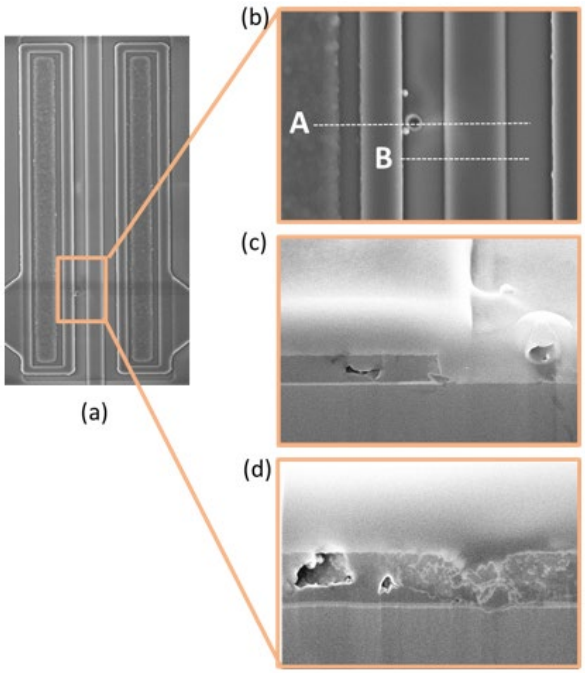

Fig. 7. (a) The SEM image of a breakdown PMOS device. A failure point is shown between the source terminal and the gate area. (b) Zoom in the image of the failure point. A failure void is close to the source. (c) SEM cross-section image of point A. Voids formed on the poly-Si area. (d) SEM cross-section image of point B. Poly gate area, oxide layer has structural collapse

IV. Conclusions

Time-dependent dielectric breakdown measurements have been used to characterize the gate oxide reliability of 4H-SiC MOSFETs in CMOS technology. The results show that the TDDB failure depends on the temperature and device size. At higher temperatures, the lifetime of devices is significantly reduced, indicating the temperature dependence of TDDB. Besides, the failure time is prolonged for smaller devices, suggesting a higher possibility of defects in large devices. The failure analysis of TDDB measurement at 200 °C and 450 °C shows two failure structures and suggests the different failure mechanisms at higher temperatures. These findings contribute to a better understanding of TDDB failure mechanisms and provide valuable information about the reliability of 4H-SiC MOSFETs in CMOS technology.

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References

[1] J. Mo, J. Li, Y. Zhang, J. Romijn, A. May, T. Erlbacher, G. Zhang, S. Vollebregt, A Highly Linear Temperature Sensor Operating up to 600° C in a 4H-SiC CMOS Technology, Ieee Electron Device L (2023).

[2] J. Romijn, L.M. Middelburg, S. Vollebregt, B. El Mansouri, H.W. van Zeijl, A. May, T. Erlbacher, G. Zhang, P.M. Sarro, Resistive

and CTAT temperature sensors in a silicon carbide CMOS technology, 2021 IEEE Sensors, IEEE, 2021, pp. 1-4.

[3] J. Romijn, S. Vollebregt, L.M. Middelburg, B. El Mansouri, H.W. van Zeijl, A. May, T. Erlbacher, G. Zhang, P.M. Sarro, Integrated digital and analog circuit blocks in a scalable silicon carbide CMOS technology, IEEE Transactions on Electron Devices 69(1) (2021) 4-10.

[4] J. Wang, X. Jiang, Review and analysis of SiC MOSFETs' ruggedness and reliability, IET Power Electronics 13(3) (2020) 445-455.

[5] B. Schlund, C. Messick, J. Suehle, P. Chaparala, A new physics-based model for time-dependent-dielectric-breakdown, IEEE 1995 International Integrated Reliability Workshop. Final Report, IEEE, 1995, pp. 72-80.

[6] R. Waters, B. Van Zeghbroeck, Temperature-dependent tunneling through thermally grown SiO 2 on n-type 4H–and 6H–SiC, Applied Physics Letters 76(8) (2000) 1039-1041.

[7] A.K. Agarwal, S. Seshadri, L.B. Rowland, Temperature dependence of Fowler-Nordheim current in 6H-and 4H-SiC MOS capacitors, Ieee Electr Device L 18(12) (1997) 592-594.

[8] B.-Y. Tsui, Y.-T. Huang, T.-L. Wu, C.-H. Chien, Time-dependent dielectric breakdown of gate oxide on 4H-SiC with different oxidation processes, Microelectronics Reliability 123 (2021) 114186.

[9] G. Gruber, C. Gspan, E. Fisslthaler, M. Dienstleder, G. Pobegen, T. Aichinger, R. Meszaros, W. Grogger, P. Hadley, Impact of the NO Anneal on the Microscopic Structure and Chemical Composition of the Si ‐ Face 4H ‐ SiC/SiO2 Interface, Advanced Materials Interfaces 5(12) (2018) 1800022.

[10] G. Chung, C. Tin, J. Williams, K. McDonald, M. Di Ventra, S. Pantelides, L.C. Feldman, R. Weller, Effect of nitric oxide annealing on the interface trap densities near the band edges in the 4H polytype of silicon carbide, Applied Physics Letters 76(13) (2000) 1713-1715.

[11] T. Kimoto, H. Kawano, M. Noborio, J. Suda, H. Matsunami, Improved dielectric and interface properties of 4H-SiC MOS structures processed by oxide deposition and N2O annealing, Materials science forum, Trans Tech Publ, 2006, pp. 987-990.

[12] K. Fujihira, Y. Tarui, M. Imaizumi, K.-i. Ohtsuka, T. Takami, T. Shiramizu, K. Kawase, J. Tanimura, T. Ozeki, Characteristics of 4H–SiC MOS interface annealed in N2O, Solid-State Electronics 49(6) (2005) 896-901.

[13] K. Matocha, G. Dunne, S. Soloviev, R. Beaupre, Time-Dependent Dielectric Breakdown of 4H-SiC MOS Capacitors and DMOSFETs, IEEE Transactions on Electron Devices 55(8) (2008) 1830-1834.

[14] C.T. Yen, H.Y. Lee, C.C. Hung, C.Y. Lee, L.S. Lee, F.J. Hsu, K.T. Chu, Oxide Breakdown Reliability of SiC MOSFET, 2019 Ieee Workshop on Wide Bandgap Power Devices and Applications in Asia (Wipda Asia 2019) (2019).

[15] A. Siddiqui, R.Y. Khosa, M. Usman, High-k dielectrics for 4H-silicon carbide: present status and future perspectives, Journal of Materials Chemistry C 9(15) (2021) 5055-5081.

[16] K. Fujihira, S. Yoshida, N. Miura, Y. Nakao, M. Imaizumi, T. Takami, T. Oomori, TDDB measurement of gate SiO2 on 4H-SiC formed by chemical vapor deposition, Materials Science Forum, Trans Tech Publ, 2009, pp. 799-802.

[17] E. Ugur, F. Yang, S. Pu, S. Zhao, B. Akin, Degradation assessment and precursor identification for SiC MOSFETs under high temp cycling, IEEE Transactions on Industry Applications 55(3) (2019) 2858-2867.