Reliability and Ageing of Insulated Metal Substrate PCBs

in High-Voltage Power Electronic Applications

G.W. Lagerweij

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PRODRIVE TECHNOLOGIES

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by

G.W. Lagerweij

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TU Delft HIGH VOLTAGE TECHNOLOGIES PRODRIVE TECHNOLOGIES

Abstract

Insulated metal substrate (IMS) printed circuit boards (PCBs) are an attractive alternative to conventional FR4-based PCBs and power modules due to their good thermal performance, low cost, and compatibility with the reflow soldering processes. In this thesis, the dielectric performance of IMS PCBs is characterised to validate their use in high-voltage power electronic applications and ensure that an acceptable lifetime and reliability can be reached. In particular, the high-frequency degradation of the dielectric is investigated.

The IMS dielectric was characterised using breakdown tests with various voltage waveforms and frequencies to closely approximate their use-case in power electronic converters. Two high-voltage generators were designed and realised to generate high-frequency square-wave and sinusoidal waveforms. In addition, diagnostic tests were performed to identify the effect of electrical ageing on the dielectric properties.

The designed high-voltage test sources allowed for ramp breakdown and lifetime tests up to 100 kHz and 10 kV_{pk}. These tests showed that the dielectric degrades extremely fast under high-frequency voltage stress, most likely due to localised high partial discharge activity and electrical treeing. As a result, no reasonable lifetime can be expected when operating above the discharge inception voltage. For thick dielectrics (>100 µm), surface discharges are the dominant degradation mechanism with an inception voltage of 2.4 kV_{pk}. The maximum nominal voltage should be limited to approximately 1.5 kV_{pk} to ensure the reliable operation of the IMS PCBs.

Keywords: Printed circuit boards, reliability, high-voltage testing, electrical ageing.

Preface

Before you lies my master thesis titled “Reliability and Ageing of Insulated Metal Substrate PCBs in High-Voltage Power Electronic Applications”, written to fulfil the graduation requirements of the Electrical Engineering program at the TU Delft. This project was a collaboration between Prodrive Technologies and the High Voltage Technologies group of the TU Delft.

Besides being a scientific report, this document is also an account of my rather unexpected journey into the world of high voltage. Since I started my Electrical Engineering education, my passion and interest have been in power electronics. So much so that I tailored my master’s courses almost entirely to that subject, did two internships on semiconductor power modules (at Alstom Transport in 2019 and Prodrive Technologies in 2020), and planned to do my graduation project on power electronics. By chance, I also chose two courses on high-voltage engineering (High Voltage Technologies and High Voltage DC), which would lead to a growing interest in this domain. When an opportunity came to combine both of my fields of interest, I jumped on it, resulting in this thesis.

I want to thank Prodrive Technologies and my supervisors, Joost van Straalen and Dr. Helm Jansen, for giving me ample freedom to create my own path through this project, allowing me to investigate many aspects of the topic. Thank you for the (almost) biweekly feedback on my work. A special thanks to my colleagues, and in particular Christian Schylander, Sjors van Osch, Sjors Verkamman, and Marco Drabbe, for the discussions and suggestions.

Most of the experimental work presented in this report was performed in the High Voltage Laboratory of the TU Delft. To the lab technicians Paul van Nes and Imke Splinter, my sincere gratitude for helping me build and operate my test setups. It would not have been possible without the tireless help of Wim Termorshuizen. Thank you for your creativity, enthusiasm, and willingness to help the students. I hope you keep fighting for the group and the High Voltage lab. Of course, the lab would be empty without the other PhD and master students, most importantly, Weichuan, Xuliang, Ewout, and Shibanni. I want to thank my supervisor, Dr. Mohamad Ghaffarian Niasar, for the encouragement and countless discussions both during and after office hours. Thanks to Prof. Peter Vaessen and Dr. Jianning Dong for being part of the committee and reviewing the thesis.

Finally, I am grateful to my family for taking care of me, supporting, and inspiring me during my journey through university. To Shibanni, thank you for you patience, and for adding a bit of colour to my life.

Gijs Lagerweij
Eindhoven, July 2023

Contents

1 Introduction

To satisfy the ever-growing demand for power converters with high power density and efficiency, all components are shrinking. Power semiconductor dies and packages have significantly reduced in size, dramatically increasing the dissipated power per area (known as the heat flux). The advent of wide bandgap (WBG) devices especially resulted in a 30 to 40 % decrease in cooling area [1]. Improved cooling solutions are necessary to handle this increased heat flux effectively.

In many cases, the semiconductor devices and the heatsink must be electrically isolated for electrical safety and to reduce radiated electromagnetic emissions. The cooling solution largely determines where this isolation barrier must be located. Therefore, a trade-off must often be made between cooling performance and electrical insulation.

1.1. Power Electronic Cooling Solutions

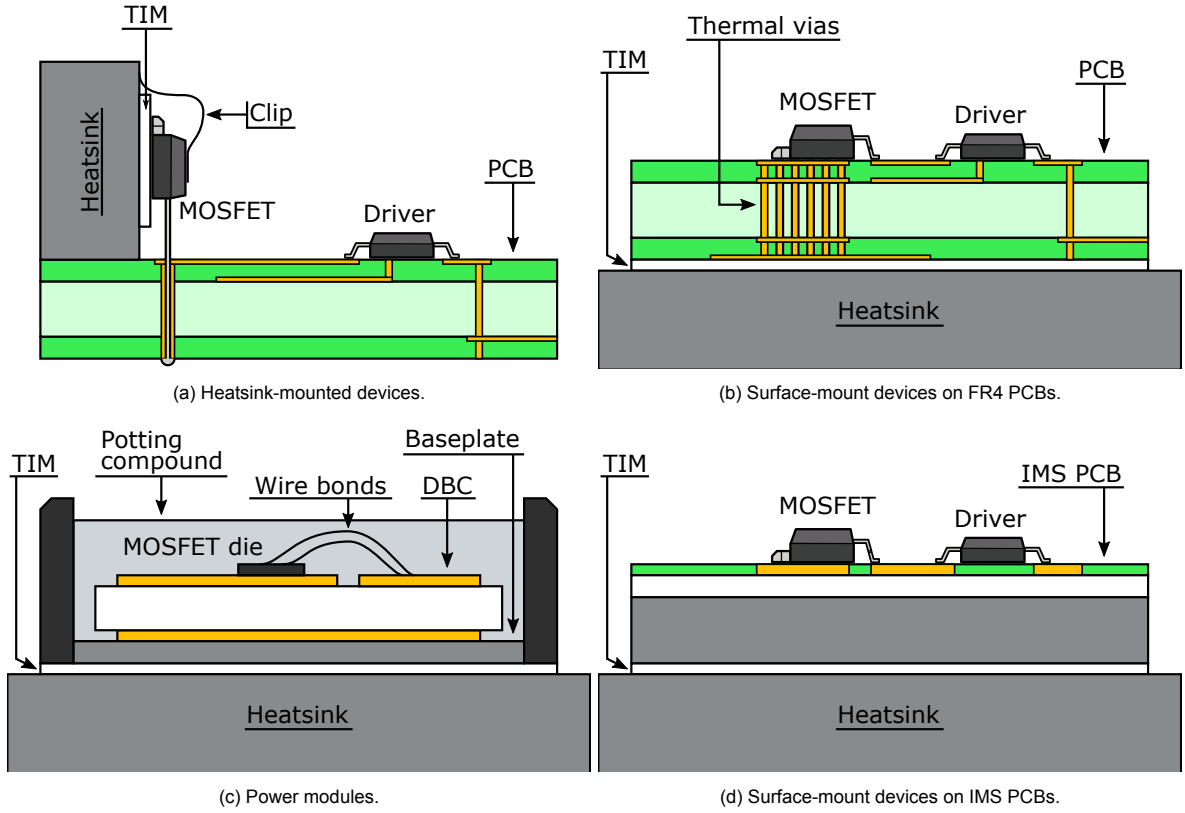
Figure 1.1 schematically shows four concepts with which power dissipated in the semiconductor devices can be extracted and transported to the heatsink or coldplate. The cooling performance of a concept is usually expressed using the thermal resistance R_ϑ (or the thermal impedance Z_ϑ for pulsed power dissipation) between the semiconductors and the ambient surroundings.

Heatsink-Mounted Devices The most common method is by using heatsink-mounted semiconductors in two-, three- or four-pin through-hole (THT) packages. The majority of converters use this principle because of the simplicity of the design. However, the production process for this concept is difficult to automate and requires manual labour. The thermal interface material (TIM) must provide the main electrical insulation, which typically increases the total thermal resistance [2].

Surface-Mount Devices on FR4 PCBs Surface-mount devices (SMD) generally offer lower parasitics and better electrical performance than THT devices. If SMD semiconductors are used, the dissipated power must be extracted through the printed circuit board (PCB). The thermal conductivity of FR4 (glass fibre-reinforced epoxy) PCBs is relatively low, so additional techniques must be applied to improve the R_ϑ: thermal vias and copper inlays [3]. In this case, an insulating TIM is still required between the PCB and the heatsink.

Power Modules Power modules based on a ceramic substrate are often used for high-power applications. The ceramic, often alumina (Al_2O_3) or aluminium nitride (AlN), provides excellent cooling performance (low thermal resistance), as well as good electrical insulation. However, power modules are expensive and difficult to manufacture due to the need for cleanroom environments and specialised manufacturing steps like sintering, vacuum soldering, and wire bonding. The ceramic substrate is fragile and may fracture if mishandled, necessitating a thick metal baseplate [4].

Surface-Mount Devices on IMS PCBs Insulated metal substrate (IMS) PCBs offer good cooling performance and electrical insulation like the power modules while still being cheap, mechanically



(a) Heatsink-mounted devices.

(b) Surface-mount devices on FR4 PCBs.

(c) Power modules.

(d) Surface-mount devices on IMS PCBs.

Figure 1.1: Cooling solutions.

robust, and compatible with standard SMD production processes. This makes IMS PCBs an attractive option for high-power applications where SMD components on FR4 PCBs are not feasible [3].

IMS PCBs consist of a metal baseplate (normally aluminium or copper), a 50 to 350 µm thick layer of insulating material, and a layer of etched copper. The insulating material is designed for a thermal conductivity approx. $10\times$ higher than that of FR4. Originally, these PCBs were intended and optimised for high-power LED applications, which require high cooling performance but use relatively low DC voltages [5] (as opposed to AC or switching voltages). Since then, the technology has been adapted for application in power electronic converters.

1.2. Research Objectives

With the increased adoption of IMS PCBs in power electronic converters in the low-voltage segment (DC link voltage $<$1000 V), these PCBs are now starting to be used at higher voltages as well. However, there is little information about the reliability of IMS PCBs in these applications, where various electrical, mechanical, and environmental stresses can occur.

Therefore, the general goal of this research project is to gain some insight into the reliability of IMS PCBs in high-voltage power electronic applications. More specifically, it is *to investigate the effect of high-frequency voltage stresses on the insulating materials of IMS PCBs.* This goal can be subdivided into the following four research objectives:

1. Investigate the insulating materials used in IMS PCBs and their dielectric properties.

2. Generate high-frequency test voltages representing the waveforms encountered in power electronic equipment.

3. Identify and characterise the main (high-voltage) failure modes which may occur on IMS PCBs.

4. Identify the ageing mechanism(s) that occur under high-frequency voltage stress.

1.3. Outline

The remainder of this thesis is composed of four chapters and several supporting appendices. In Chapter 2, the construction of IMS PCBs is investigated in detail. Failure and ageing mechanisms that may occur under power electronic converters' stresses are presented. Chapter 3 describes various tests that are performed to investigate the dielectric properties of IMS PCBs and tools to process the results. The results of these tests are presented and analysed in Chapter 4. Conclusions are drawn about the suitability of IMS PCBs for the described application in Chapter 5.

Appendix A contains a list of used abbreviations, mathematical symbols and constants. Appendices B and C deal with the design of two high-voltage, high-frequency test sources for square wave and sinusoidal voltages. In Appendix D, a detailed analysis of several recorded partial discharge patterns is presented to support the conclusions about the discharges and their implications for the ageing mechanism drawn in the main text. Appendix E contains several derivations that are too detailed for the main text.

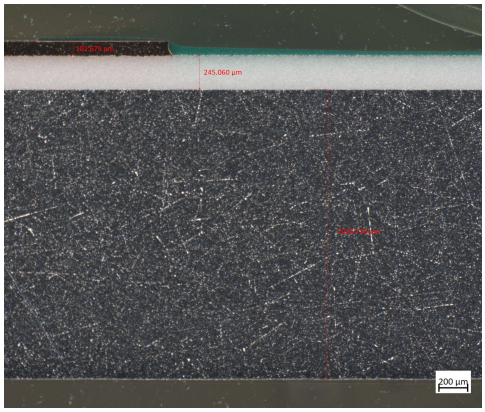
2

Insulation Materials

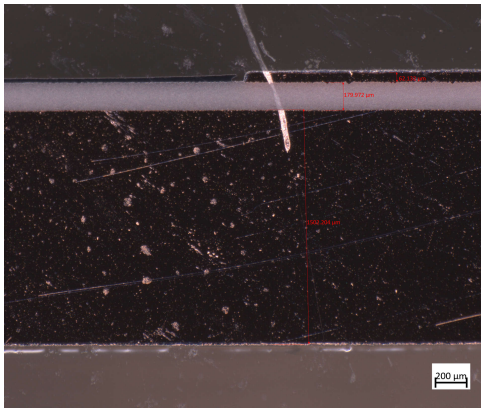
This chapter discusses the insulation materials used in insulated metal substrate (IMS) PCBs and their dielectric, mechanical, and thermal properties. The high-voltage failure modes that can occur on PCBs are presented. Finally, the electrical and environmental stresses in the power converters under study are reviewed to derive appropriate characterising tests in Chapter 3.

2.1. Insulation in IMS PCBs

Insulated metal substrate PCBs consist of an aluminium or copper baseplate, a 50 to 350 µm thick layer of dielectric, and a layer of etched copper (see Figure 2.1). The dielectric composition is manufacturer-specific, with varying dielectric, thermal, and mechanical properties. Typically, the insulating layer comprises an epoxy resin and dense inorganic fillers. Epoxy by itself, called “neat” epoxy, has a thermal conductivity of roughly 0.35 W/(m K). Ceramic fillers significantly increase the thermal conductivity up to about 3 to 4 W/(m K). The obtainable increase depends on the composition, size, and shape of the filler, as well as the ratio of filler to epoxy resin [6].



(a) 2 mm aluminium base, 230 µm dielectric, 3 oz copper.



(b) 1.5 mm copper base, 180 µm dielectric, 2 oz copper.

Figure 2.1: Cross-sections of IMS PCBs (photographs by Prodrive Technologies).

It appears that inorganic fillers not only improve the thermal conductivity but also modify the dielectric constant ε_r (micro-fillers increase it, while nano-fillers decrease it) and increase the loss tangent $\tan\delta$ due to Maxwell–Wagner polarisation effects [7, 8]. The breakdown voltage has a non-linear relation to filler content which tends towards that of the ceramic at high volume fractions [9]. Nano-fillers have been shown to significantly improve partial discharge resistance, space charge characteristics, and dielectric strength due to an increased deep trap density. Micro-fillers promote shallow traps and tend to have the opposite effect on these properties [10–12].

2.1.1. Materials

A selection of IMS insulation materials available on the market is presented in Table 2.1. As explained above, the dielectrics consist of an epoxy with inorganic fillers, with variations in the type, percentage, and size of the filler(s) responsible for the considerable variation in properties. Filler composition is not specified in the datasheets, “ceramic” filler is reported if the composition is unknown.

Table 2.1: Dielectric materials for IMS PCBs.

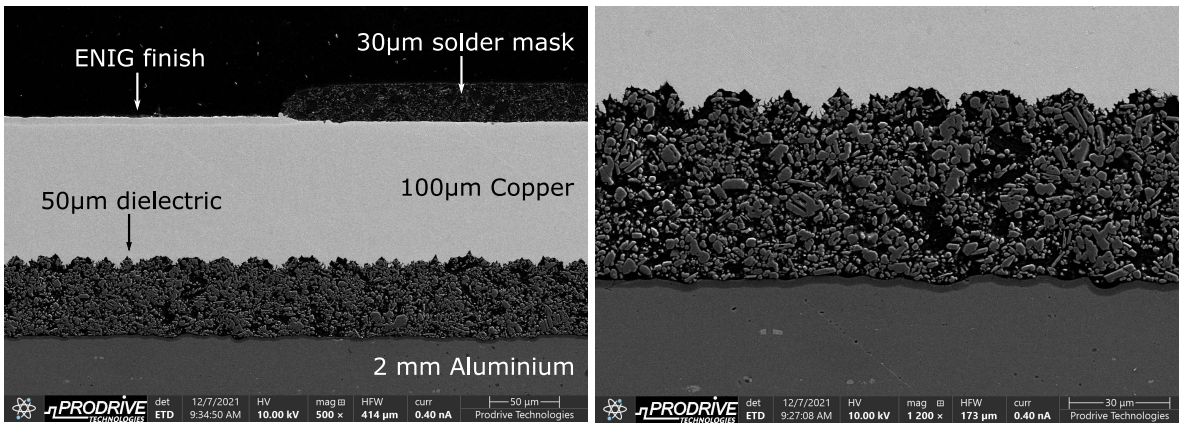
Name	Composition	k_ϑ [W/(m K)]	ε_r	$\tan\delta$	T_g
Arlon 92ML [13]	Ceramic-filled epoxy	1.7	5.3	110×10^{-4}	160 °C
Laird Tlam 1KA [14]	Ceramic-filled epoxy	3.0	4.1	350×10^{-4}	105 °C
Denka M-2 [15]	Ceramic-filled epoxy	2.0	4.4	40×10^{-4}	120 °C
Denka TH-1 [15]	Ceramic-filled epoxy	4.0	7.7	50×10^{-4}	165 °C
Goldenmax GL12 [16]	SiO_2-filled epoxy	1.1	1.8[a]	140×10^{-4}	125 °C
NipponRika H6 [17]	Ceramic-filled epoxy	5.7	7.3	88×10^{-4}	194 °C
NipponRika H10 [17]	Ceramic-filled epoxy	14.4	7.9	27×10^{-4}	205 °C
TCLAD HPL [18]	Ceramic-filled epoxy	3.0	6.6	50×10^{-4}	185 °C
TCLAD HT [19]	Ceramic-filled epoxy	2.2	7.0	130×10^{-4}	150 °C
Ventec VT-4B3 [20]	Al_2O_3-filled epoxy	3.0	4.8	160×10^{-4}	130 °C
Ventec VT-4B5 [21]	Al_2O_3-filled epoxy	4.2	4.8	160×10^{-4}	120 °C

[a] Datasheet gives incorrect value, see measurements in Section 2.1.3.

Because of the application in power electronics, it is desirable to minimise parasitic capacitance while maximising thermal performance, i.e., minimising ε_r and maximising the thermal conductivity k_ϑ. As for any PCB technology, the materials should not be used close to or above the glass temperature T_g because the coefficient of thermal expansion (CTE) increases significantly, causing thermo-mechanical stress on the dielectric, laminated interfaces, components, and solder joints [22].

2.1.2. Ventec VT-4B3

The VT-4B3 material is a ceramic-filled epoxy laminate with a thickness of 50 to 230 µm. The microscopic topology of a finished PCB with 50 µm insulation and 100 µm/3 oz copper is shown in Figure 2.2a. The dielectric consists of an epoxy matrix and a ceramic filler. The Al_2O_3 (alumina) particles are irregularly shaped and have a 1 to 10 µm diameter. The dispersion of the particles is not uniform, which can be seen in Figure 2.2b. Some parts of the micro-fillers may be $Al(OH)_3$ (aluminium hydroxide), which has good fire-retardant and smoke-suppressant properties. The surface of the dielectric has a peak-peak roughness of approximately 10 µm to ensure a good bond between the copper and insulation, resulting in high peel strength and low thermal resistance.

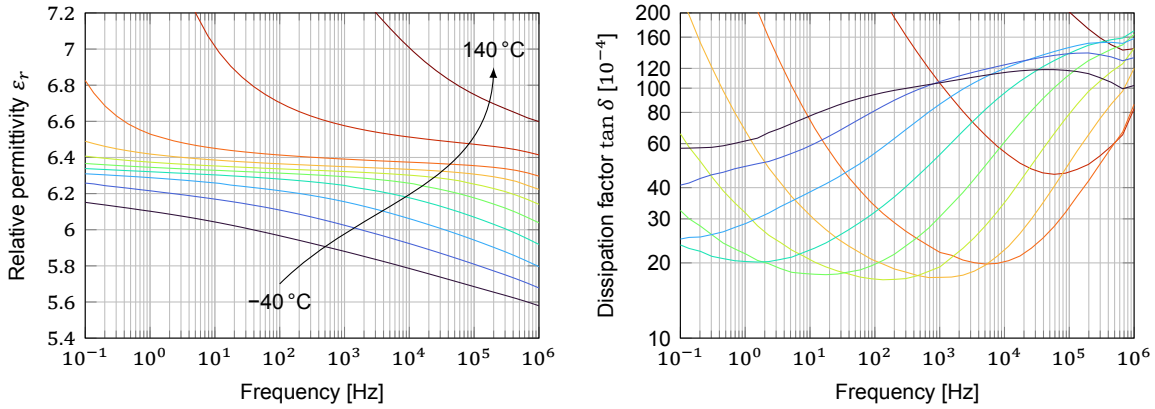


(a) Overview (b) Dielectric

Figure 2.2: SEM micrograph of IMS PCBs with Ventec VT-4B3 laminate (thickness 50 µm).

The dielectric response in Figure 2.3 is measured (see Section 3.1.3). It shows a complex behaviour

over frequency and temperature due to the composite nature of the dielectric (epoxy and ceramic filler). Most importantly, the dielectric loss increases by orders of magnitude at temperatures close to the glass temperature T_g. Thermal runaway becomes a risk when the dielectric reaches >100 °C. The response exhibits α-relaxation (low-frequency peak due to main chain motion), β-relaxation (high-frequency peak due to polar group motion, e.g., OH and NH groups), and Maxwell–Wagner–Sillars polarisation.



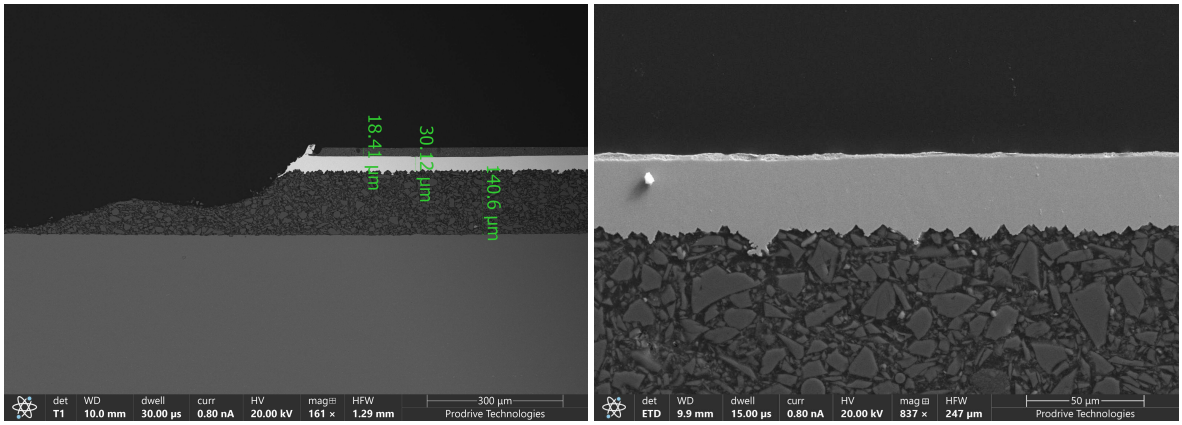
(a) Relative permittivity ε_r.

(b) Dissipation factor $\tan\delta$.

Figure 2.3: Dielectric response of Ventec VT-4B3 laminate. Colors indicate the temperature of the measurement: −40 °C (dark blue) to 140 °C (dark red) in 20 °C steps.

2.1.3. Goldenmax GL12

The Goldenmax GL12 material has significantly different electrical properties than the other materials shown in Table 2.1. The microscopic topology of a finished PCB with 140 µm insulation and 35 µm/1 oz copper is shown in Figure 2.4a. The dielectric is constructed using a similar principle as the Ventec material. However, the main filler consists of big irregularly-shaped silica crystals (SiO_2). The volume fraction of filler is relatively high, which is in line with the thermal conductivity being close to that of bulk silica. The copper plane protrudes into the dielectric to ensure a good mechanical bond.

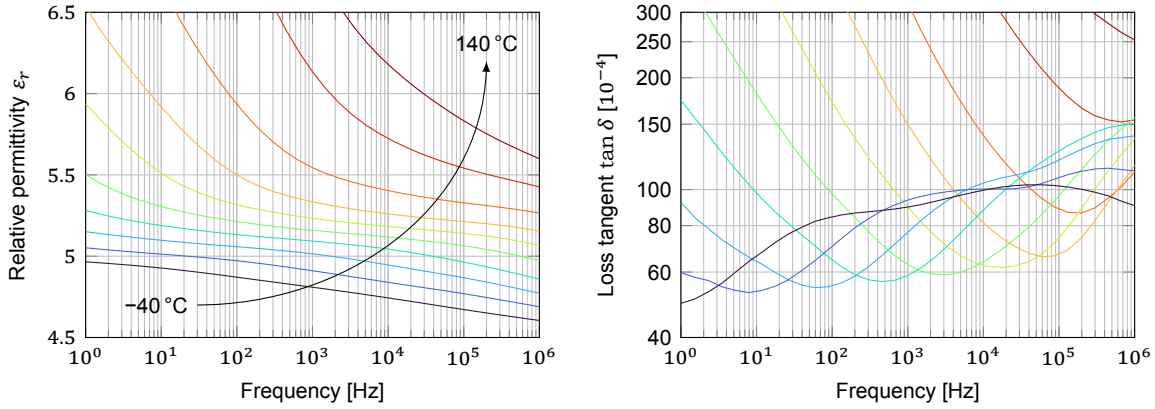


(a) Overview

(b) Dielectric

Figure 2.4: SEM micrograph of IMS PCBs with Goldenmax GL12 laminate (thickness 140 µm).

The dielectric response of 140 µm Goldenmax GL12 is measured, and the relative permittivity and loss tangent are presented in Figure 2.5. The dielectric constant at low frequencies ($\varepsilon_r = 4.85$ at 1 MHz) is much higher than what is advertised in the datasheet (Table 2.1, $\varepsilon_r = 1.8$ at 1 MHz). Combined with the inferior electrical and thermal properties of the SiO_2 filler, this material is less suitable for high-voltage, high-power applications than anticipated. It will not be considered further.



(a) Relative Permittivity ε_r.

(b) Dissipation factor $\tan\delta$.

Figure 2.5: Dielectric response of Goldenmax GL12 laminate. Colors indicate the temperature of the measurement: −40 °C (dark blue) to 140 °C (dark red) in 20 °C steps.

2.2. Failure Mechanisms in High-Voltage PCBs

Printed circuit boards are a complex construction consisting of multiple layers of etched copper and dielectric (prepreg and core), which are laminated. The production process can greatly affect the (dielectric) performance. Analysing PCBs from a high-voltage point of view shows three potential failure mechanisms [23].

– Dielectric failure: the dielectric layer between the layers of copper can break down if the electric field is too large. This phenomenon can be nearly instantaneous, puncturing the dielectric during some voltage transient, or part of a slow degradation process due to, e.g., thermo-mechanical ageing or partial discharges. Breakdown is highly dependent on the operating conditions.

– Surface flashover and tracking: electrical breakdown may also occur along the surface of the PCB between two conductors. The flashover is initiated at a triple point between copper (traces, pads, or plated through-holes), dielectric or solder mask, and air. The flashover can cause permanent damage to the surface of the PCB in the form of carbonised “tracking” paths.

– Air breakdown: if the field strength is high enough, the air may break down, forming an arc between two conductors.

The first two mechanisms are highly dependent on the properties of the insulating material and PCB stack-up. Flashover and surface tracking (Figure 2.6b) are not limited to PCBs, and quite some

(a) Dielectric failure.

(b) Surface tracking.

Figure 2.6: PCB high-voltage failure modes.

research is available regarding insulation coordination. Creepage is defined by tracking due to long-term voltage application. Clearance corresponds to flashover due to (non-repetitive) impulse or surge voltages. For example, IEC 60664 [24] deals with insulation coordination for electrical equipment, and part 4 [23] provides details specifically for high-frequency voltage stress (>30 kHz). The probability of surface flashover may be reduced significantly by applying a conformal coating to the PCB, especially in heavily polluted environments.

Therefore, the remainder of this thesis will focus on investigating the dielectric failure mode (Figure 2.6a). It will only briefly touch upon surface tracking during the study of partial discharges (Section 4.4), highlighting the importance of considering both failure modes during the design of the PCB and its insulation system.

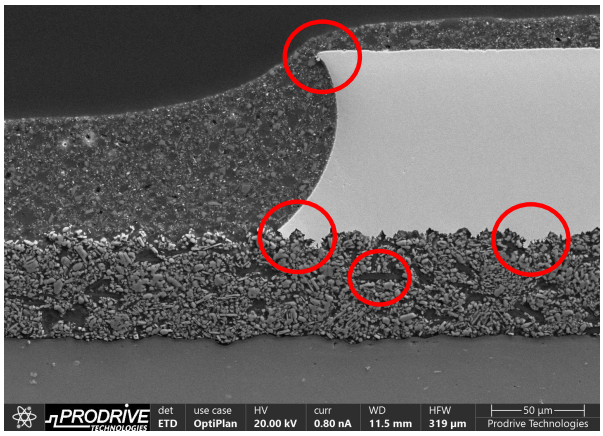


Figure 2.7: Locations of potential field enhancement: Trace edge (3 oz/100 µm copper, 50 µm VT-4B3).

One of the biggest problems when using PCBs for high-voltage applications is the extreme field enhancement encountered at the copper traces. The etching process leaves sharp corners and edges on the copper traces and planes, as shown in Figure 2.7, especially for thicker copper layers (≥2 oz/70 µm), which are typically used in power applications. A similar situation may occur at improperly reworked solder joints and SMD component casings. As a result, surface breakdown usually originates from the edges of the copper traces and small SMD components.

2.3. Ageing under Power Electronic Stress

In power conversion systems, the insulation is subjected to various voltage stresses: combinations of AC, DC, and high-frequency pulse-width modulated (PWM) voltages regularly occur. Especially with modern wide bandgap (WBG) devices, the switching frequencies can increase up to the MHz range, leading to higher high-frequency content of the voltage. Besides the voltage stress, the insulation can be exposed to high operating temperatures, pollution, and humidity for extended periods of time.

2.3.1. Mains-Frequency AC Voltage

Mains-frequency (50/60 Hz) AC voltage is typically encountered in grid interfaces such as rectifiers and inverters. The three-phase line-to-line voltages are in the range of 220 to 600 V, which means that the (peak) voltage to ground is <500 V, assuming symmetry around earth. The nominal voltage levels here do generally not present any danger to the insulation system, provided the applicable standards for creepage and clearance are followed and the component ratings are adequately selected. Transients and surges (in the range of 1 to 2.5 kV_{pk}) require additional insulation coordination.

2.3.2. High-Frequency Voltage

In general, the lifetime of the insulation decreases with increasing voltage, frequency, and faster voltage transients (i.e., decreasing rise time) [25]. It is important to note that the impact of the latter has yet to be fully clarified in the literature. Varying degrees of degradation caused by the rise time are reported. This topic is predominantly explored in research on electrical machines and solid-state transformers. The following paragraphs will discuss the sources of degradation that arise with high-frequency voltages.

Partial Discharges Most scientific sources agree that partial discharges (PD) are one of the leading causes of degradation and reduction of breakdown strength under high-frequency square wave voltages. However, the reported PD patterns and their relation to lifetime are different. Materials are divided into Type I (organic) and Type II (organic/inorganic compound) insulation. Type II materials show much higher resistance to PD and hence reduced degradation under high-frequency voltages [26–29].

The partial discharge magnitude is inversely proportional to rise time [28, 30], which is attributed to the fact that the over-voltage ratio (i.e., the ratio between the actual voltage and the inception voltage) is larger for short rise times. Nevertheless, the lifetime seems mostly independent of rise time. Instead, because the PD frequency is roughly proportional to the switching frequency for short rise times, the switching frequency has a much more significant effect on the lifetime [31, 32].

PD with Multi-Level Excitation The behaviour of partial discharges under multi-level PWM excitation is relevant for state-of-the-art power converters. Hammarström shows experimentally that the PD magnitude and frequency reduce significantly when increasing the number of levels in the PWM waveform [33]. As the number of levels becomes large (such as might be the case in modular multi-level converters), the PD behaviour tends to that of the modulating sinusoidal waveform [34, 35].

Dielectric Heating A time-varying electric field creates losses in the dielectric due to polarisation and dipolar relaxation processes. These losses depend on the dielectric response $\varepsilon_r(\omega)$ of the material and are described by

$$P_d(\omega) = \omega\varepsilon_0 \left(\varepsilon_r''(\omega) + \frac{\sigma}{\omega\varepsilon_0} \right) |\boldsymbol{E}|^2, \tag{2.1}$$

where the loss consists of the imaginary part ε_r'' and the conductivity of the dielectric σ. The loss depends on the square of the electric field E [36]. For voltage waveforms containing harmonics, such as those produced by power electronics, the dielectric losses can be expressed by summing expression (2.1) over the frequency components of the waveform. Rewriting in terms of the voltage U, capacitance $C'(\omega)$, and loss factor $\tan\delta(\omega)$, (2.2) is obtained [37].

$$P_d = \sum_{n=1}^{\infty} n\omega_0 C'(n\omega_0) \tan\delta(n\omega_0) U_n^2 \tag{2.2}$$

The heat generated by high-frequency signals may accumulate in the dielectric and accelerate its degradation. In particular, the increased temperature allows for easier inception of partial discharges [29, 36, 38] and accelerates thermal degradation (see Section 2.3.4). Below the PD inception voltage, the acceleration of thermal ageing can be the determining factor for the lifetime of the insulation system [37]. Usually, thermal breakdown does not occur because the generated heat power is much lower than the fracture energy of the polymer bonds (on the order of 3 to 7 eV = 300 to 700 kJ/mol) [29, 39].

Space Charge Although the injection of space charge is typically neglected for non-DC applications, space charge can accumulate due to partial discharge activity [36] and electron emission (field-assisted or thermionic) at electrode protrusions [40]. Under high-frequency voltage waveforms, not all charge can recombine before the period of opposite polarity, causing local field enhancement, which facilitates the inception of PDs [32, 36, 41] and the inception and growth of electrical trees [40].

Rise Time versus Slew Rate This report will distinguish between the effect of the "rise time" t_r and "slew rate" dU/dt, which are used interchangeably in the literature. In Section 2.4, it is shown that the insulation lifetime depends on the harmonic content of the voltage waveform. In the context of ramp voltage tests (see Section 3.4), the rise time is taken as a test variable since the harmonic content stays constant for a given voltage and rise time. This claim is further elaborated in Appendix E.1.

2.3.3. DC Voltage

In general, the lifetime of insulation materials under DC excitation is much longer than that under AC or high-frequency voltage stresses. This makes testing the DC lifetime much more difficult. Furthermore, the short-term and long-term ageing mechanisms are often quite different. Brown et al. report that

short-term breakdown results from field enhancement caused by highly mobile space charge, whereas long-term breakdown is related to low-mobility or trapped space charge [42]. The sources of insulation degradation under DC voltage are discussed in the following paragraphs.

Electromechanical Strain Electromechanical strain has been reported as one of the main mechanisms of electrical degradation under DC voltages. The electrostatic force created by high local fields results in the deformation of polymer chains and the breaking of Van der Waals bonds [43].

Partial Discharges As mentioned above, partial discharges are one of the leading causes of degradation under AC and HF voltage stresses. However, the repetition rate of PDs under DC voltage is much lower: on the order of several discharges per minute in the resistive stage, as opposed to several thousand or more per second under AC voltage. As a result, the damage to the insulation is limited [44].

Cavity and surface PDs under pure DC or DC with superimposed AC voltages may be modelled using the well-known abc-model with RC elements. This model also reflects the differences between the capacitive and resistive stage [45].

Space Charge Under DC voltage stress, space charges are crucial in the electric field distribution and ageing mechanisms. The charge injection, transport, and extraction mechanisms define the behaviour of charges in the insulation medium. Space charges can be injected from the electrodes (field-assisted or thermionic emission) or by partial discharges [44, 46].

The accumulation of space charges can lead to highly localised electric field enhancement, accelerating the ageing process and potentially initiating electrical trees.

2.3.4. Temperature and Thermal Cycling

Increased temperature accelerates chemical reactions, which (thermally) ages the dielectric. The lifetime as a function of the temperature follows an Arrhenius relation

$$L(T) = L_0 \exp\left(\frac{E_a}{k_B T}\right), \tag{2.3}$$

where k_B is the Boltzmann constant, T is the temperature, and the activation energy E_a is expressed in eV [47]. Excessive temperature (above the glass temperature T_g) can cause morphological changes to the polymer insulation material, significantly changing its properties [43]. In most power-electronic insulation systems, thermal breakdown does not play a significant role because the dielectric losses given by (2.1) are usually quite small [31]. When the temperature increases above T_g, thermal breakdown becomes a risk for some materials [29, 48].

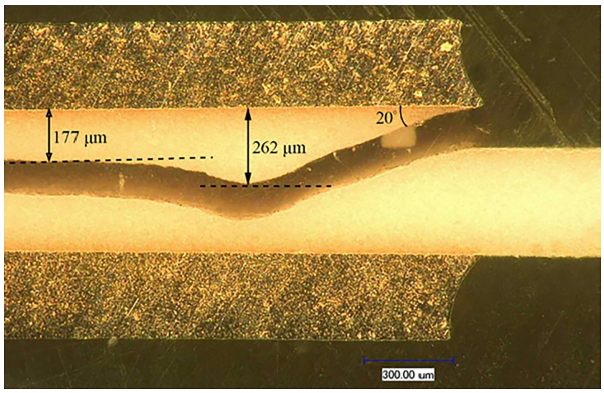


Figure 2.8: DBC delamination and cracking due to thermal cycling (Xu et al. [49]).

Although thermal cycling does not have a significant electrical effect, it leads to thermo-mechanical degradation of the dielectric. The effect may be worsened if several materials with different thermal expansion coefficients are used. At the end of life, thermo-mechanical ageing may result in delamination (see Figure 2.8), crazing, or fracturing of the dielectric [49, 50]. Even though the ageing mechanism is not electrical, it may cause electrical breakdown.

2.3.5. Humidity and Moisture

When polymer dielectrics are exposed to a humid atmosphere, moisture will gradually diffuse into the dielectric. The presence of water molecules is known to catalyse the breakdown of the polymer chains by hydrolysis, reducing the lifetime of the insulation [51]. According to the IEC 60664-4 standard, insulation materials intended for high-frequency use shall not be exposed to humidity higher than 92 %RH for long periods of time. Only materials that do not absorb moisture (e.g. glass and ceramics) are not subject to this limit [23].

Moisture has a pronounced effect on the properties of most dielectric materials, and PCB laminates are no exception. Therefore, it is crucial to include the effect of moisture on the dielectric properties in this research. After manufacturing, PCBs are typically vacuum sealed with a desiccator inside the packaging to preserve their solderability and prevent rapid out-gassing during the reflow soldering. This means that, while the PCBs are completely moisture-free when unpacked, they may absorb a significant amount of moisture during their lifetime, reducing the dielectric strength.

2.3.6. Pollution

Pollution may lead to a reduction in the surface breakdown strength of an insulation system. Most pollution can become (semi)conductive under the influence of humidity, further reducing the dielectric strength of the insulation system. This problem is often resolved on PCBs by adding a layer of conformal coating covering the PCB and components. Other solutions include the complete encapsulation or potting of the high-voltage component, commonly done with silicone in power modules [52]. However, pollution-driven degradation and breakdown may still occur on coated PCBs [53]. Polluting particles may be attracted to the regions of high electric field by electrophoresis [54].

2.4. Electrical Lifetime Model

Under AC voltage excitation, the electrical lifetime can generally be modelled using the inverse power law (2.4). The slope of the lifetime curve is related to the power law exponent (by $^{-1}/_{n}$), which can change if the ageing mechanism changes. For example, n may change at the partial discharge inception voltage [55].

$$L(U) = L_0 \left(\frac{U}{U_0} \right)^{-n} \tag{2.4}$$

where U_0 is a normalising constant and L_0 is the lifetime at $U = U_0$. A normalising constant $U_0 = 1\,\mathrm{kV}$ will be chosen because this is representative of the applications under consideration. The power law may also be written in terms of the electric field E and E_0.

The electrical lifetime under high-frequency PWM voltages depends on the magnitude, frequency, and rise time of the waveform. This notion may be extended to other waveforms, such as high-frequency sinusoidal or pulsed voltages, in terms of their harmonic content, see (2.5) [31].

$$L = L_0 \cdot K_p^{-n_p} \cdot K_{rms}^{-n_{rms}} \cdot K_s^{-n_s} \tag{2.5}$$

The terms represent the peak, root mean square (RMS), and harmonic components of the voltage waveform. Sometimes, the lifetime as a function of frequency is modelled using an inverse power law (2.6). The value of k varies between studies and depends on the frequency and rise time. It has been reported to be in the range $k \approx 1 - 1.4$ and generally increases with rise time [28, 56].

$$L(f) = L_0 \left(\frac{f}{f_0} \right)^{-k} \tag{2.6}$$

2.5. Conclusion

In this chapter, the construction of insulated metal substrate PCBs has been described. The thin insulating layer consists of an epoxy resin with various inorganic micro- and nanofillers, often ceramics, improving thermal and electrical properties. Dielectric breakdown and surface tracking were identified as the main failure mechanisms on PCBs for high-voltage applications. Under high-frequency excitation, the ageing processes can be accelerated dramatically. Other failures of PCBs may be related to thermo-mechanical stresses, causing delamination or cracking of the insulating layer, solder joints, or components.

3

Insulation Testing

This chapter introduces the test methods applied to study the characteristics of PCB insulation. Both destructive (breakdown) and diagnostic tests are used to investigate the effect of high-frequency voltage stress. PCB samples are designed to test the breakdown strength and electrical lifetime of the IMS insulating materials. Procedures are presented for tests to investigate the effect of various parameters on the dielectric properties and electrical lifetime. Finally, statistical methods are developed to process the test results.

3.1. Test Methods

The quality and dielectric strength of insulation systems can be examined destructively in two ways:

- Static tests: several identical samples are subjected to a constant voltage U, and the time to breakdown t_{bd} is recorded. Usually, a maximum test duration is imposed, leading to censoring.
- Dynamic tests: several identical samples are subjected to a linearly increasing voltage $U(t)$, and the breakdown voltage u_{bd} is recorded. The maximum voltage is limited by the test setup.

Because of the statistical nature of these tests, a large number of samples is required to obtain any statistical significance. It has been proven by Dissado et al. that both test methodologies can yield equivalent information about the parameters characterising the system. However, dynamic testing is usually preferred in a laboratory environment because the variation in the measured results is less than for static testing [57], and the test duration is shorter.

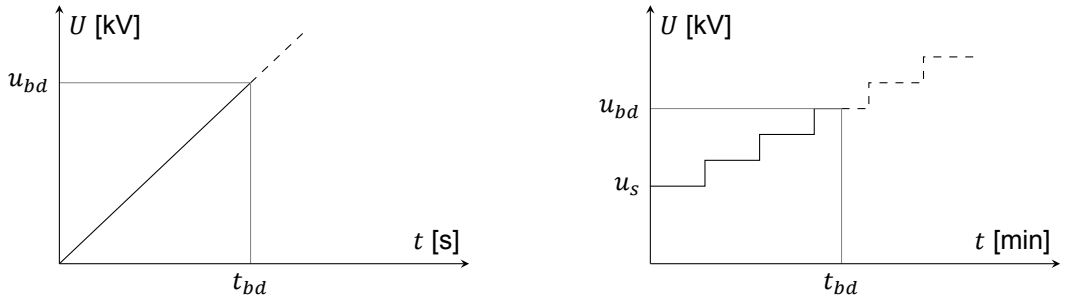
3.1.1. Short Breakdown Tests

Short breakdown tests are used to determine and compare the quality of insulation under certain stress conditions (voltage, frequency, environmental). The short testing time allows for variation and investigation of the effect of various test parameters. As noted before, the spread in test results is less than for long-term tests, reducing the required number of samples.

This study uses short breakdown tests to understand the electrical breakdown characteristics of the insulation. This information will be used to formulate representative lifetime testing conditions in Section 3.5. Short-term tests are dynamic tests, performed with a voltage ramp in the range of 0.01 to 1 kV/s or a step voltage waveform with steps of ≈1 kV/min. The latter is usually used when the device under test has a relatively high breakdown voltage (tens of kV) or when the test source cannot be ramped up continuously. Step voltage tests are usually started at a voltage u_s close to 50 % of the expected breakdown voltage. Typical test voltage waveforms are illustrated in Figure 3.1.

Limitations The main drawback of short-term breakdown tests is that high acceleration levels, e.g., voltages greatly exceeding the nominal voltage, can result in test conditions that no longer accurately represent the normal usage profile. This can lead to the following issues [58]:

- Extraneous failure modes: High acceleration levels produce failure modes that would never have occurred at lower stress values. In the case of breakdown tests, this is manifested as a change



(a) Ramp voltage.

(b) Step voltage.

Figure 3.1: Short breakdown test waveforms.

in the slope of the lifetime curve. The lifetime may be seriously underestimated if tests are only performed above the transition point.

– Masked failure modes: a highly accelerated lifetime test focusing on one failure mode may mask the occurrence of a second failure mode. This is more common in tests focusing on parameters such as temperature.

3.1.2. Lifetime Testing

Long-term static tests or lifetime tests are also performed to ensure that the correct conclusions about lifetime are drawn from the data. Various voltage levels below the ramp breakdown voltage are selected for the long-term tests. An added benefit of this type of combined short and long-term testing is that the confidence bounds at lower voltage stress levels can be made much narrower, leading to a more accurate estimation of the component lifetime.

Lifetime tests can also be performed with slow ramping or step voltages, but this is typically only done if there is a large spread in breakdown times to prevent excessive censoring. By continuously increasing the voltage, degradation is accumulated and will lead to breakdown. However, the statistical theory behind such cumulative-stress testing is much more complicated.

Limitations The same limitations are applicable for lifetime testing as for short breakdown tests. The goal of lifetime testing is to estimate the lifetime that can be expected under nominal operating conditions based on a series of accelerated tests. Therefore, if the results are extrapolated too far, the dominant ageing mechanism may be over- or underestimated. It is typical for the power law coefficient n to change with the voltage level (e.g., at the PD inception voltage).

3.1.3. Diagnostic Tests

Besides the destructive measurements presented in the previous sections, non-destructive diagnostic tests can be used to obtain valuable information about the properties and state of a dielectric.

Partial Discharge Analysis Partial discharge measurements give insight into the defects inside the insulation and at its surface. Measurement results may take many forms, such as inception/extinction voltage, phase-resolved patterns (PRPD, ϕ-q-n and variants), and time-resolved PD pulses [55]. PD measurements will be performed using a conventional Hipotronics DDX9101 detector and a setup suitable for high-frequency voltages (see Appendix C.3).

Dielectric Frequency Response (DFR) The dielectric frequency response shows the complex permittivity $\varepsilon^*(\omega)$ as a function of the frequency. It may be split into two parts: the dielectric constant $\varepsilon_r(f)$, and the dissipation factor $\tan\delta(f)$, which give information about the relaxation and polarisation processes in a dielectric. For example, composite materials will exhibit relaxation peaks corresponding to Maxwell–Wagner polarisation [8], and polymers may show α-relaxation behaviour at low frequency and elevated temperatures due to increased polymer chain mobility [59]. Bulk chemical changes, e.g., due to chain scission, will be reflected in the DFR.

Isothermal Relaxation Current (IRC) The IRC method is a variant of the polarisation/depolarisation current (PDC) measurement, which allows for determining (a part of) the trap distribution in the dielectric. The theory behind the method was introduced by Simmons et al. [60]. The depolarisation current i_d versus time is plotted on a $i_d t$ versus $\log t$ plot. The axes can then be transformed to the trap density $N(E)$ and trap depth ΔE using

$$\Delta E = k_B T \ln \nu t, \tag{3.1}$$

$$N(E) = \frac{2}{k_B T f_0 d A} i_d t, \tag{3.2}$$

where k_B is the Boltmann constant, T is the temperature in [K], ν is the attempt-to-escape frequency, f_0 is the initial trap occupancy assumed to be 0.5, d is the dielectric thickness, and A is the sample area. The units of $N(E)$ are [eV^{-1} m^{-3}].

Besides providing information about the depth and density of traps, changes in the trap distribution are indicative of physical or chemical changes in the dielectric, similar to DFR. The DFR and depolarisation current measurement investigate the same physical phenomena in different frequency ranges (DFR: mHz to MHz, IRC: µHz to Hz). Nevertheless, the IRC technique only covers a small portion of the band gap, and deep traps could be challenging to detect. In the future, a technique like TSDC (thermally stimulated depolarisation current) could yield more information about the trap distribution and the role of traps in the degradation of electrical insulation.

3.2. Samples

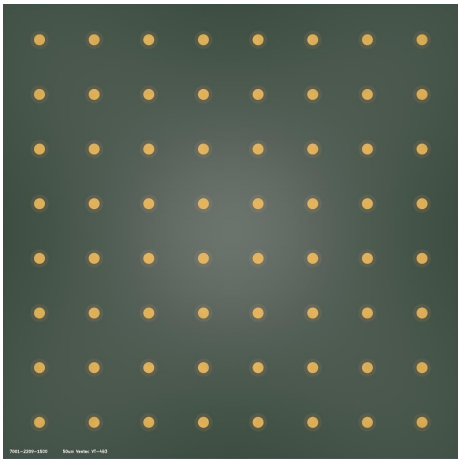
Based on the literature review, it was decided that the insulation breakdown failure mode (see Section 2.2) is the most important to characterise. Circular samples are designed to test the electrical breakdown strength of the dielectric. The dielectric material can be stressed by applying a voltage to the electrode and grounding the aluminium substrate until breakdown occurs. An overview of the samples and their critical parameters is given in Table 3.1. All samples have a 2 mm aluminium substrate and 3 oz/100 µm copper since this is most representative of the actual use-case of these PCBs.

Table 3.1: List of sample configurations.

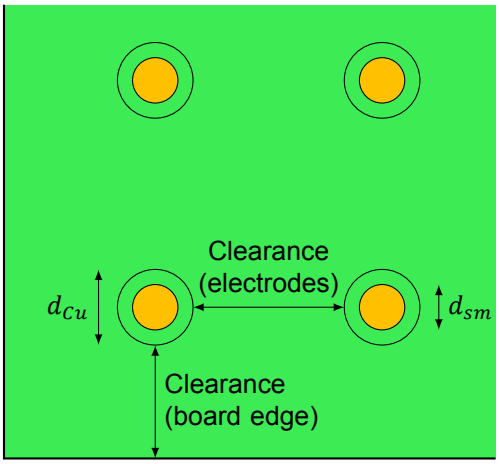
Sample	Dielectric	Electrode diameter d_{Cu}	Clearance (board edge)	Clearance (electrodes)
A	50 µm VT-4B3	10 mm	15 mm	20 mm
B	150 µm VT-4B3	10 mm	20 mm	22.5 mm
C	230 µm VT-4B3	10 mm	20 mm	22.5 mm
D	140 µm GL12	10 mm	15 mm	20 mm
E	75 µm VT-4B3	10, 20, and 30 mm	15 mm	≥15 mm
F	100 µm VT-4B3	10, 20, and 30 mm	15 mm	≥15 mm

The electrodes are drawn in a square grid on a 250 × 250 mm circuit board. The resulting layout of sample A is shown in Figure 3.2a. The dimensions of the samples are defined in Figure 3.2b. Ideally, there should be no interaction between neighbouring electrodes. If the electrodes are energised individually, there will be no noticeable effect on the electric field distribution. However, the non-energised electrodes may attain some voltage due to capacitive coupling. Nevertheless, flashover occurs (between electrodes and over the edge of the PCB) at a certain voltage, and the PCBs must be tested in oil. This is further discussed in Section 4.1.

For a brief investigation in Section 4.4, several PCB samples of type B and C were conformally coated with UV-curable DSL 1600 E-FLZ. Conformal coating is typically used to improve the surface tracking and flashover characteristics, especially in polluted or humid environments. The coating protects the PCB surface against moisture, condensation, and corrosion.



(a) Sample PCB A with 8×8 electrodes.



(b) Sample dimension definitions.

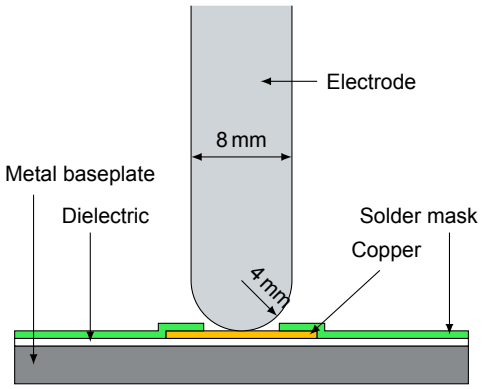
Figure 3.2: PCB samples for testing dielectric breakdown.

3.3. Test Setup

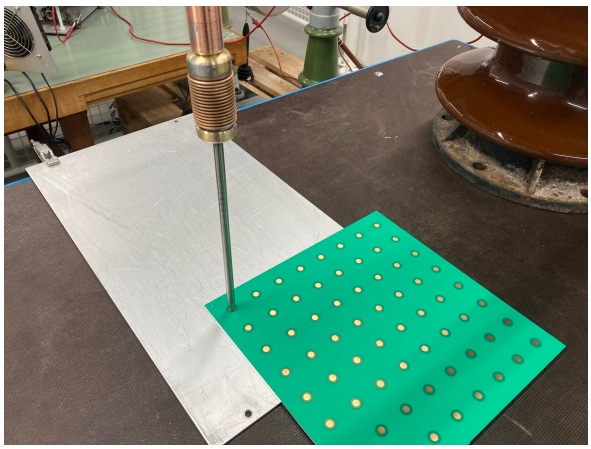
The breakdown test setup comprises two main parts, which are described in the following paragraphs: (i) the electrode connection system, which applies the test voltage to the sample, and (ii) the test voltage generation for AC, DC, and high-frequency voltages.

3.3.1. Electrode Arrangement

The test voltage has to be applied to the electrodes on the sample PCB. Because each PCB contains multiple electrodes, the setup should allow for quick changing of the electrode. The electrode arrangement is shown in Figure 3.3. For the tests in this research, the samples are immersed in oil.



(a) Schematic representation.



(b) Electrode arrangement with a sample PCB.

Figure 3.3: Electrode arrangement for testing circular samples.

The electrode setup consists of a large metal pipe mounted on a 100 kV insulator, to which a small stainless steel electrode is connected through a spring. By lifting the spring and moving the PCB, each sample electrode is easily accessible. The shape of the rod electrode is not critical as long as it has a smaller diameter than the copper electrodes. The ground connection to the metal baseplate is provided through a metal plate placed under the PCB.

3.3.2. AC Voltage

The setup for applying 50 Hz AC voltage is shown in Figure 3.4. It consists of a 220 V/50 kV high-voltage transformer with 75 kΩ current-limiting resistor, the previously described electrode arrangement, and a control unit consisting of a variac and protection/interlock box. The voltage is measured using a 28 kV_{rms} high-voltage probe (TESTEC HVP 40) and multimeter.

(a) HV transformer and sample.

(b) Variac and protection box.

Figure 3.4: Test Setup for 50 Hz AC Voltage

3.3.3. High-Frequency Square-Wave Voltage

Square-wave voltages are closest to the waveforms that the dielectric will be subjected to during operation in PE converters. Ideally, testing should be performed at the correct frequency (25 to 100 kHz) and rise time (10 to 100 ns) to obtain representative results. The voltage is increased above its nominal level to accelerate the tests. In general, there are three ways to perform breakdown tests with high-frequency PWM voltages:

1. Using a half- or full-bridge configuration with solid-state switches:
   (a) Low-voltage Si/SiC MOSFETs/IGBTs: high frequency and short rise times but limited output voltage. For example, Agarwal et al. use 3.3 kV SiC switches to reach 50 kHz and 60 kV/µs at a maximum voltage of 2 kV [56].
   (b) High-voltage switches: high output voltage but limited frequency and rise time. For example, Mirza et al. use 33 kV switches to test up to 5 kV and 4 kHz [61].
2. Using a pulse transformer driven by a half- or full-bridge converter: high voltages and high frequencies are achievable, but the leakage inductance of the transformer limits the rise time. This approach has been used to test oil-paper insulation at 20 kV_{pp} and 50 kHz for use in solid-state transformers [62–65].

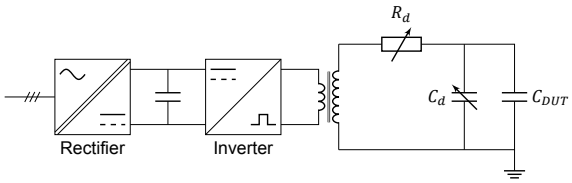
The second approach is most suitable because sufficiently high voltages and frequencies can be generated (see Table 3.2) to allow for representative tests. Although the achievable rise time is limited, this is not necessarily a problem because it was found to have a secondary effect on the electrical lifetime (see Section 2.3.2).

Table 3.2: Comparison of PWM test methods.

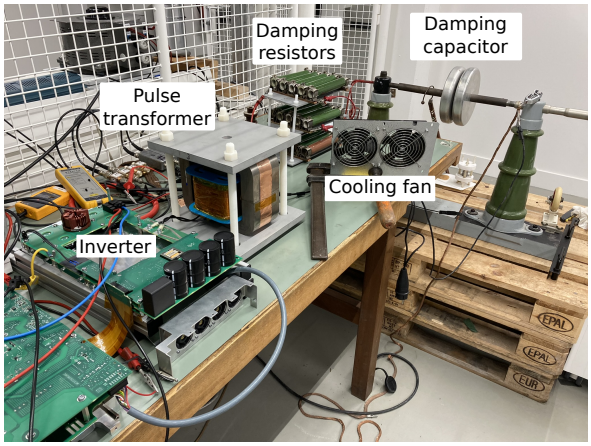
Method	Voltage	Frequency	Rise time
Full bridge with SiC MOSFET	–	+	+
Full bridge with HV switches	+	–	–
Pulse transformer	+	+	–

The test setup is presented in Figure 3.5. The low-voltage side consists of a bipolar pulse generator (full-bridge inverter) supplied by a variable DC voltage source. The pulses are then amplified by the

pulse transformer and applied to the device under test (DUT). The damping resistor R_d and capacitor C_d are used to tune the rise time and overshoot. More detailed information, calculations, and simulations are presented in Appendix B. Operation up to 100 kHz, 16 kV_{pp} with a rise time of 750 ns is possible.



(a) Schematic

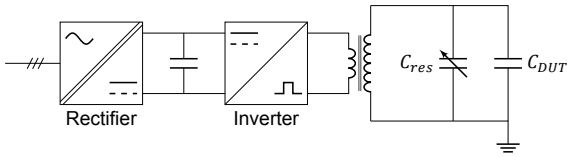


(b) Photograph

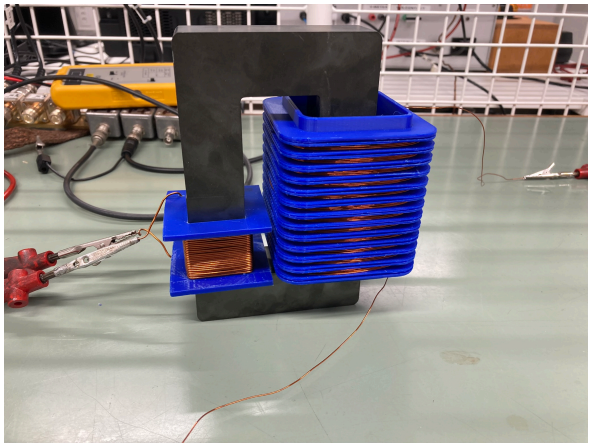
Figure 3.5: Test Setup for square-wave voltage.

3.3.4. High-Frequency Sinusoidal Voltage

Standards [23] and literature [26, 31] suggest that lifetime testing may be performed with sinusoidal instead of square wave voltages, as long as the fundamental frequency is correct. To compare the two approaches, an HV generator for HF sinusoidal voltages is designed (see Figure 3.6). The generator uses the principle of resonance to create high voltages by circulating energy between the DUT capacitance and transformer inductance. As a result, much less power is required than for the square-wave generator. The details of the setup design are presented in Appendix C.



(a) Schematic

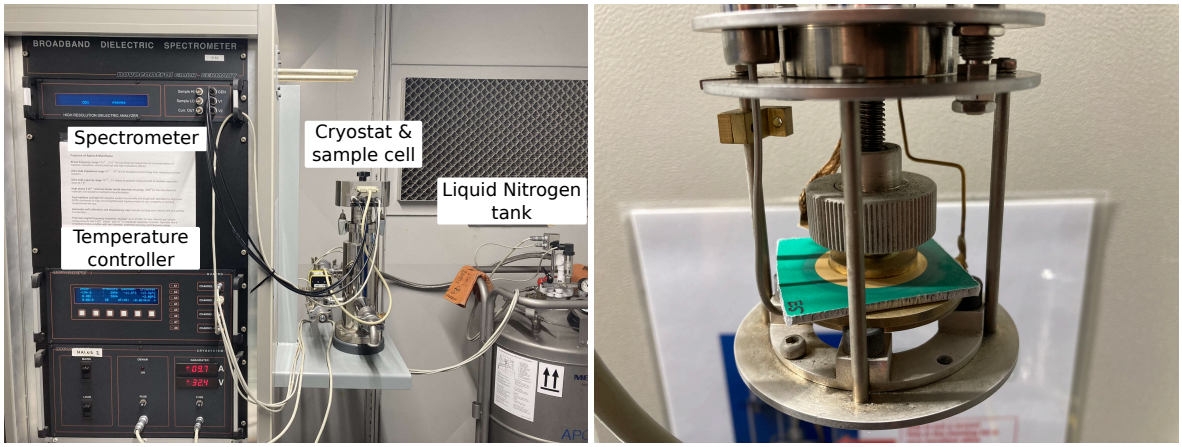


(b) Photograph of resonant transformer.

Figure 3.6: Test setup for HF sinusoidal voltage.

3.3.5. Dielectric Frequency Response

Dielectric response measurements are performed with a Novocontrol Alpha dielectric spectrometer with a ZGS active sample cell and Quatro Cryosystem for highly accurate temperature control (<0.1 °C). The setup is shown in Figure 3.7. A modified ⌀30 mm PCB electrode was made with a much wider opening in the solder mask to ensure compatibility with the sample cell (see Figure 3.7b).



(a) Novocontrol Dielectric Spectrometer and Quatro Cryosystem. (b) ZGS Active Sample Cell with PCB sample.

Figure 3.7: Measurement setup for dielectric frequency response (DFR).

3.4. Short Breakdown Testing

In this section, the procedures for the ramp breakdown tests are described. These tests aim to determine the relationship between the dielectric strength of the insulating material and several parameters: the voltage waveform and frequency, moisture, and the volume effect.

3.4.1. Test 1: Effect of Frequency

After the voltage magnitude, the frequency of the waveform has the most significant effect on the breakdown strength of insulation materials, as discussed in Section 2.3.2. The HF test setups (Section 3.3.3) generate high-frequency voltages across the dielectric. Tests are performed at several representative frequencies to get a good overview of the effect of the frequency: 25, 50, and 100 kHz. Additionally, an AC ramp test extends the frequency range down to 50 Hz.

Preconditioning The PCB samples are preconditioned before the tests to ensure comparable environmental properties. Some standards indicate that samples should undergo moisture preconditioning before such breakdown tests, but the effect of moisture will be investigated separately in Section 3.4.2.

Preconditioning procedure B from the ASTM D618 standard is taken to limit the influence of other environmental parameters. The samples are conditioned in a circulating-air oven at 50 °C for 48 h [66]. After removing the samples from the oven, they are cooled to room temperature in a vacuum oven for at least 5 h since no desiccator of the right size was available.

Test Procedure The breakdown tests are performed as follows:

1. Precondition the samples according to the described procedure based on ASTM D618 procedure B: 48/50 + Des. Ensure that the samples have settled to ambient conditions before testing.

2. Place the sample in the electrode setup as shown in Figure 3.3.

3. Apply a 500 V/s voltage ramp using one of the test setups presented in Section 3.3.

4. Record the breakdown voltage or time to breakdown and the approximate location of breakdown on the sample (e.g., the edge or middle of the electrode).

3.4.2. Test 2: Effect of Moisture

As noted in Section 2.3.5, moisture can considerably affect the dielectric strength of the PCB. The PCBs will be preconditioned for this test in a high-temperature, high-humidity environment.

Preconditioning The IPC test method for the dielectric strength of PCBs specifies a preconditioning phase consisting of immersion in distilled water for 48 h at 50 °C, followed by 30 to 240 min at ambient temperature [67]. According to the underlying ASTM D149 standard, it is essential to ensure that the dielectric is saturated with moisture [68]. This procedure is based on Procedure E of ASTM D618 [66]. The IPC method will be used in this short test since it represents the worst-case condition of complete saturation. Whether this is realistic in practice will be discussed for the lifetime testing (Section 3.5).

Test Procedure The test procedure is identical to that presented for test 1 (Section 3.4.1). Care must be taken to ensure that the sample is wiped dry. If any moisture is present on the surface of the sample, it may affect the results of the test.

3.4.3. Test 3: Volume Effect

An increase in the volume of the insulation while the field distribution stays the same (e.g. when increasing the size of the copper electrode) causes a decrease in breakdown voltage. Assuming that the density of defects in the insulation is constant, increasing the volume leads to an increased number of defects [55]. For the Weibull distribution, η_n is related to η_1 by

$$F_n(x) = 1 - (1 - F_1(x))^n \implies \eta_n = \eta_1 \cdot n^{-1/\beta_1}, \tag{3.3}$$

where n indicates the volume increase (derivation in Appendix E.5). To be able to extrapolate the measurements on the small samples to larger, more realistic copper planes, this volume effect must be investigated.

Test Procedure Samples E and F have three sizes of electrodes for 75 µm and 100 µm dielectric thickness (see Table 3.1). Combined with the results from sample A, this will allow for the determination of the volume effect due to electrode scaling and the thickness of the dielectric. Therefore, the tests are performed according to the procedure for Test 1.

3.5. Lifetime Testing

In this section, the procedures for the lifetime tests are described. These tests aim to determine the behaviour of the dielectric strength of the insulating material with the voltage application time. The lifetime under normal operating conditions can be extrapolated if sufficient tests are performed.

Due to limitations in time, the lifetime tests performed in this research will be relatively short (typically less than an hour). Although this limits the extent to which the results can be safely extrapolated, it makes it possible to perform more tests and achieve higher statistical accuracy. Therefore, it is proposed in Section 5.2 to perform reliability demonstrations on real hardware. These demonstrations can be planned appropriately using the results obtained during the highly accelerated lifetime tests.

The lifetime tests are performed at the same frequencies as the short breakdown tests (50 Hz, 25, 50, and 100 kHz), but only using sinusoidal voltages due to limitations in the square-wave generator (see Appendix B). Because the moisture absorption of the insulation is low (see also results in Section 4.2.3), the PCBs are preconditioned for the lifetime test following the procedure of short breakdown test 1: 48/50 + Des. Due to the duration of the tests, the PCB may absorb some moisture before all samples can be tested. This is deemed acceptable since it is similar to what the PCB undergoes during regular operation.

Lifetime tests are performed the same way as the short breakdown tests, except that the voltage is kept constant during the test, and the time to breakdown is recorded to analyse the results.

3.6. Weibull Analysis

The Weibull distribution is often used for the analysis of the test results. The cumulative distribution function (CDF) of the two-parameter Weibull distribution for a random variable X is given by

$$F(x) = P(X < x) = 1 - \exp\left[-\left(\frac{x}{\eta}\right)^{\beta}\right], \tag{3.4}$$

where η is the scale parameter which has the same units as X and β is the unitless shape parameter. In breakdown testing, x often represents time (in static tests) or voltage/field strength (in dynamic tests).

3.6.1. Rank Regression (RR)

The data is ranked in ascending order to derive the parameters of the Weibull distribution from a series of measurements using rank regression. The unreliability F_i assigned to data sample i of N can be estimated using the median rank estimator (3.5) recommended by the IEEE [69].

$$F_i \approx \frac{i - 0.44}{N + 0.25} \tag{3.5}$$

Then, the Weibull parameters are estimated by performing a linear least-squares regression on the data points (x_i, F_i). Rank regression is used extensively because it is computationally cheap and easy to implement.

3.6.2. Maximum Likelihood Estimation (MLE)

Maximum likelihood estimation techniques are much more flexible than rank regression and can provide better estimates in case of censoring. This is especially the case when supplemental information or Bayesian analysis are included [58, 70]. MLE also allows for the implementation of regression models.

For log-location-scale distributions (such as the lognormal and Weibull distributions), the likelihood for n independent exact or right-censored observations can be expressed as

$$L(x) = \prod_{i=1}^{n} \left[\frac{1}{\sigma x_i} f\left(\frac{\ln x_i - \mu}{\sigma} \right) \right]^{\delta_i} \left[1 - F\left(\frac{\ln x_i - \mu}{\sigma} \right) \right]^{1-\delta_i}, \tag{3.6}$$

where x_i are the observations, μ and σ are the mean and standard deviation of the distribution, and δ_i indicates whether the observation is exact $(= 1)$ or right-censored $(= 0)$ [58]. To calculate the ML estimate for a Weibull distribution, f and F are the PDF and CDF of the smallest extreme value (SEV) distribution. The Weibull and SEV distributions are related by

$$\eta = \exp(\mu) \qquad \beta = \frac{1}{\sigma} \qquad \Leftrightarrow \qquad \mu = \ln \eta \qquad \sigma = \frac{1}{\beta}$$

3.6.3. Regression Models with MLE

Sometimes, explanatory variables are available in addition to the failure-time data. This explanatory data can be included in the statistical analysis using a regression model [58]. Explanatory variables could be continuous (e.g., voltage, temperature), discrete (e.g., number of cycles), or categorical (e.g., manufacturer). The CDF of the regression model (3.7) is written in terms of the log-location-scale CDF.

$$F_r(t; \mu, \sigma) = F\left[\frac{\ln t - \mu}{\sigma} \right] \tag{3.7}$$

For example, assuming an inverse power law relation between lifetime and voltage, the mean may be expressed as a function of the explanatory variable U_j representing the test voltage of sample j. The new parameters L_0, n, and σ can be determined through maximum likelihood estimation.

$$L(U) = \frac{L_0}{U^n} \qquad \Longrightarrow \qquad \mu_j = \ln L_0 - n \ln U_j \tag{3.8}$$

In doing this, several assumptions are made about the data, underlying distributions function, and regression model. If the assumptions are not validated, the results could be misinterpreted. The following paragraphs present the tools needed to validate the assumptions. This analysis is based on Meeker et al. [58]. The 50 Hz lifetime test (Section 4.3) is used as example.

Likelihood Comparison To validate the implementation of the regression model, it must be shown that two likelihood models, represented by log-likelihood functions $\mathcal{L}_1(x)$ and $\mathcal{L}_2(x)$, are good fits for the data. That is, it must be shown statistically that the likelihood of both models is the same or similar.

Akaike Information Criterion When comparing MLE models, the likelihoods L (or log-likelihood $\mathcal{L}$) cannot be compared directly. Instead, the Akaike information criterion (AIC) also incorporates the number of degrees of freedom:

$$\mathrm{AIC} = -2\mathcal{L} + 2m, \tag{3.9}$$

where $\mathcal{L}$ is the log-likelihood value of the MLE procedure and m is the number of estimated model parameters. The model with the lowest AIC is the best fit for the data. The term $2m$ penalises models with more parameters.

LR Test To show that two MLE models have the same likelihood, a likelihood ratio test (LR) can be performed. If the models have similar characteristics, this ratio should be close to one (or the difference of the log-likelihoods close to zero). The LR test of a model with p parameters is as follows. The null hypothesis (θ_0) is rejected at a confidence level of 100α % if

$$\lambda = -2\log\left[\frac{L(\theta_0)}{L(\hat{\theta})}\right] > \chi^2_{(1-\alpha;m)} \tag{3.10}$$

where χ^2_ν denotes the Chi-square distribution with ν degrees of freedom. Conversely, the p-value of the test is given by (3.11). If $p < \alpha$, the hypothesis should be rejected.

$$p = \mathrm{P}\left[\chi^2_m > \lambda\right] \tag{3.11}$$

Implementation The 50 Hz AC lifetime test results for 50 µm dielectric were taken to demonstrate the described approach. The data consists of four test series at 4.6, 5.0, 5.3, and 5.6 kV. Three estimation models are defined:

– SepDists: Each test series follows a separate distribution with its own Weibull parameters.

$$\theta = [\eta_1, \eta_2, \eta_3, \eta_4, \beta_1, \beta_2, \beta_3, \beta_4]$$

– EqualSig: Each distribution has its own η parameter, but $\beta = 1/\sigma$ is the same for all. This is expected when the ageing mechanism is the same for the selected voltage levels.

$$\theta = [\eta_1, \eta_2, \eta_3, \eta_4, \beta]$$

– RegrModel: The data is described by a single Weibull distribution ($\eta(U)$, β) where η follows an inverse power law with parameters L_0 and n (see Eq. 3.7), and normalising by $U_0 = 1$ kV.

$$\theta = [L_0, n, \beta]$$

The ML estimates of the parameters from each of these models, as well as the corresponding confidence intervals, are presented in Tables 3.3, 3.4, and 3.5. Observe that the confidence interval on β becomes much better by assuming it is equal between all distributions because three times as much data is available for estimation.

Table 3.3: Results of MLE for SepDists model.

U_{test}	Param.	Estim.	95 % CI	
4.6 kV	η_1	485.8	290.2	813.4
	β_1	0.93	0.67	1.50
5.0 kV	η_2	542.4	325.7	903.5
	β_2	1.04	0.73	1.85
5.3 kV	η_3	288.4	166.5	499.6
	β_3	0.94	0.65	1.66
5.6 kV	η_4	74.3	37.6	146.9
	β_4	0.74	0.53	1.19

Table 3.4: Results of MLE for EqualSig model.

U_{test}	Param.	Estim.	95 % CI	
4.6 kV	η_1	476.0	282.3	802.7
5.0 kV	η_2	522.4	289.6	942.2
5.3 kV	η_3	283.1	160.9	498.0
5.6 kV	η_4	82.7	47.7	143.4
	β	0.88	0.73	1.11

Table 3.5: Results of MLE for RegrModel.

Param.	Estim.	95 % CI	
$\ln L_0$	19.67	12.38	26.97
n	8.62	4.14	13.11
β	0.84	0.70	1.05

Table 3.6 compares the three MLE models. The likelihoods corresponding to each are quite close, and the LR tests show that both assumptions hold: (i) the Weibull β parameters for the test series do not differ appreciably, and (ii) the inverse power law is a relatively good fit for the 50 Hz lifetime test results.

Table 3.6: Comparison of MLE models for inverse power law

Model	$-2\mathcal{L}$	AIC	#Parameters
SepDists	622.3	638.3	8
EqualSig	623.9	633.9	5
RegrModel	628.2	634.2	3
Comparison	**LR stat.**	**dof**	**p-value**
SepDists vs EqualSig	1.637	3	0.6510
EqualSig vs RegrModel	4.339	2	0.1142

An additional advantage of using the regression model is that tests need no longer be performed at several pre-defined voltage levels. Instead, tests can be performed at any voltage level and still be considered in the statistical analysis. Nevertheless, care must be taken since this approach makes changes in the slope n difficult to detect.

3.7. Conclusion

This chapter describes several destructive and non-destructive test methods to evaluate the properties of dielectric materials. Most importantly, the concepts of static (long-term) and dynamic (short-term) breakdown tests have been introduced, along with the statistics that are required to process the results. Maximum likelihood estimation procedures with regression models are implemented to derive, e.g., the voltage-life curve.

Samples are designed to test the breakdown strength of the insulated metal substrate PCBs under study. A test setup is built, comprising an electrode arrangement to connect the high voltage and ground to the samples, as well as three high-voltage generators: (i) a conventional 50 Hz HV test transformer, (ii) a pulse transformer-based square wave generator for 25 to 100 kHz and up to 8 kV peak output voltage, and (iii) a resonant transformer to generate sinusoidal voltages up to 10 kV at 25 to 100 kHz. Finally, test procedures are outlined to characterise the material samples and investigate the effect of frequency and voltage waveform, moisture, and volume on electrical breakdown characteristics.

4

Tests Results

In this chapter, the results of the previously described tests are presented. With these results, some conclusions can be drawn regarding the voltage endurance of the IMS PCBs under study. First, several challenges, which were encountered during the first breakdown tests, are discussed. Second, the short breakdown tests show relations between the breakdown voltage, environmental and operating conditions, and PCB geometry. Finally, lifetime tests show the devastating effect of high-frequency voltages on the lifetime of solid insulation.

4.1. Breakdown Testing Challenges

While performing the initial breakdown tests using 50 Hz AC voltage, the testing voltage was limited by flashover (electrode–electrode and electrode–ground over the edge of the PCB). Flashover may occur, even with the designed clearance, because of the highly inhomogeneous field at the edges of the copper electrodes.

4.1.1. Testing in Air

AC breakdown tests in air were possible up to 7 kV (50 µm dielectric) and 11 kV (150 µm dielectric). A flashover occurs between electrodes at this voltage, obscuring the desired insulation breakdown event.

4.1.2. Testing in Oil

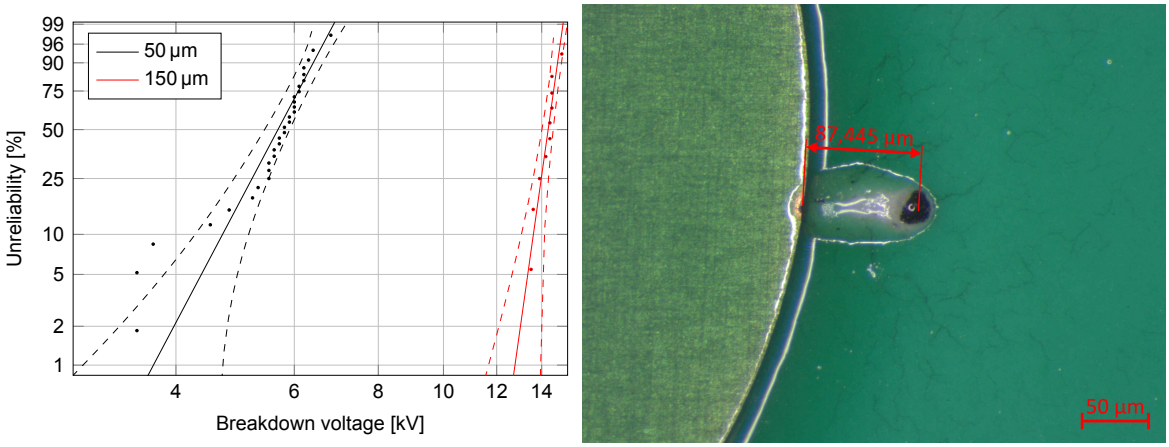
Therefore, the remainder of the AC breakdown tests has been performed under oil, especially for the thicker samples. One concern with this approach is the absorption of oil in the solder mask and insulation. However, because the insulation comprises a cured epoxy, this risk is minimal if the tests are performed quickly.

Transformer Oil During the first breakdown tests under Nynas transformer oil, flashover to nearby electrodes and over the edge of the PCB was prevented due to the higher breakdown strength of the oil. The results for 50 µm were identical to those obtained in air (except for those points where flashover occurred). Nevertheless, three observations cast doubt on the validity of the obtained breakdown voltages for thicker dielectrics.

1. The Weibull plots for 50 µm (in air, no flashover) and 150 µm (in oil) are compared in Figure 4.1a. The breakdown voltage of 150 µm showed minimal variation, resulting in an extremely high value of $\beta \approx 40$. The apparent change in β indicates a change in the breakdown mechanism.

2. Inspection under the microscope shows that breakdown does not occur right at the edge of the copper, which would be the location of the highest field strength. Instead, the breakdown path follows the surface for several 100s of µm before puncturing the dielectric (see Figure 4.1b). Lichtenberg figures are observed all around the electrode.

3. The breakdown voltages obtained for 150 µm and 230 µm under transformer oil are identical.



(a) Weibull plot of breakdown voltage.

(b) Micrograph of insulation and solder mask breakdown.

Figure 4.1: Observations for breakdown tests in transformer oil

These observations hinted toward rapid degradation caused by surface discharges in oil, obscuring the insulation material's actual breakdown. This is feasible because the geometry of the copper highly enhances the field (e.g., as discussed in Section 2.2).

Silicone Oil Silicone oil was used in an attempt to improve oil-induced degradation. The breakdown strength of the available oils was measured with an OPG-100A Isolierölprüfgerät according to the IEC 60156 [71] standard for breakdown voltage of insulating liquids. The results show that silicone oil provides a higher breakdown strength than transformer oil.

Table 4.1: Breakdown strength of oil types measured according to IEC 60156.

	η [kV/mm]	β	$-2\mathcal{L}$
Transformer oil	20.3 ± 0.9	16.6	21.0
Silicone oil	29.2 ± 1.5	13.7	28.2
Polyisobutylene	38.4 ± 1.4	16.5	39.2

Testing under silicone oil gives a slight increase in breakdown voltage (15 to 16 kV), but not anywhere near the expected $1.5\times$ improvement. An even better insulator is used to investigate this further.

Polyisobutylene Polyisobutylene (PIB) is an insulating liquid sometimes used in oil-filled terminations. It has a very high viscosity, which gives it a higher breakdown strength than transformer and silicone oil (see Table 4.1). Even with this insulator, the same phenomenon occurs, albeit at a slightly higher voltage (16 to 17 kV).

After a few breakdowns, moisture gets trapped in the oil due to repeated electrode movement while switching samples. This moisture significantly degrades the insulating properties of PIB.

4.1.3. Conclusion

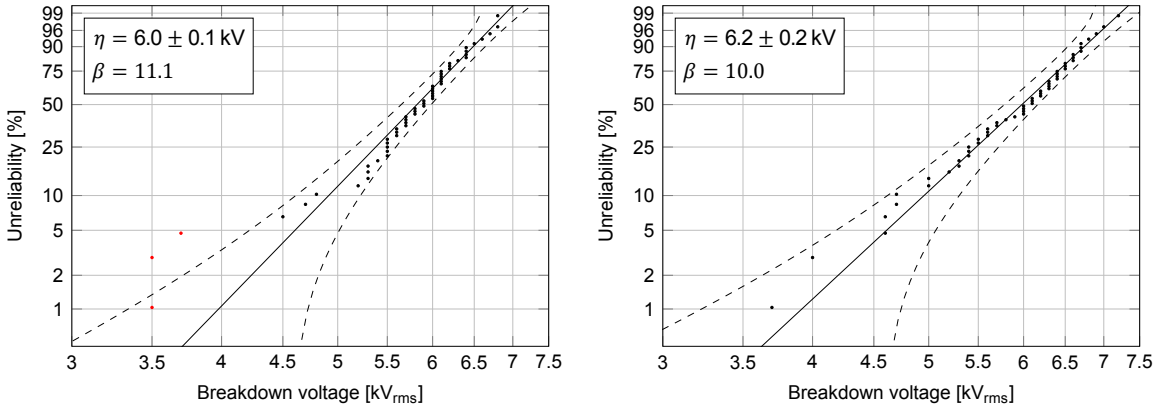
Since changing the oil did not give the expected increase in breakdown voltage, this is less likely to be the actual problem. Instead, the second component of the interface becomes suspicious: the solder mask. Typically, the dielectric strength of the solder mask is not specified since it is not intended to withstand any high voltage. Therefore, the observed surface discharges and resulting degradation are caused by the localised breakdown of the solder mask. This limits the achievable AC testing voltage to approx. 10 kV.

4.2. Short Breakdown Tests

Short breakdown tests are performed with a ramp voltage of 500 V/s. The following sections investigate the effect of the voltage frequency and waveform, exposure to moisture, and the volume effect.

4.2.1. 50 Hz Reference Measurements

Sample A Breakdown tests with conventional 50 Hz AC voltage provide an upper bound on the breakdown voltage since the dielectric is expected to degrade under high-frequency voltage. The Weibull plot for the 50 Hz results (Figure 4.2a) shows several outliers, which means that the data does not fit well with the Weibull statistics. The two most likely causes are: (i) two concurrent breakdown processes, or (ii) "bad" samples with abnormal defects. If the breakdown process around 3.5 kV is slower, it may be masked by the faster process at 6.0 kV if the voltage is increased too fast. Therefore, breakdown tests are performed at a reduced voltage slope (250 V/s) to rule out the first hypothesis.



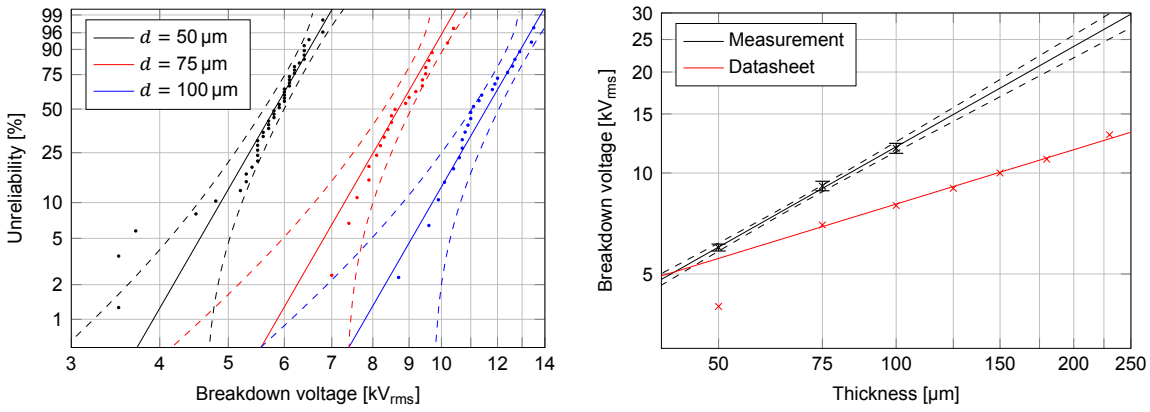
(a) Ramp breakdown with 500 V/s.

(b) Ramp breakdown with 250 V/s.

Figure 4.2: 50 Hz AC breakdown voltage.

The results in Figure 4.2b show that the first hypothesis is unlikely. Otherwise, twice as many failures would be expected around 3.5 kV. Considering the construction of the PCB (protrusions on the electrode and the highly inhomogeneous nature of the dielectric, Figure 2.2), some samples may have defects. The datasheet [20] does not specify the maximum variation in insulation thickness.

Dependence on Dielectric Thickness Through measurements on the 10 mm electrodes of samples A, E, and F, the breakdown voltage was found to increase approximately linearly with the dielectric thickness (power law exponent $k = 0.994 \pm 0.056$), which means that the breakdown field does not depend on thickness. The datasheet values [20], shown in red, have different behaviour. This may be because the datasheet values were obtained using the IPC-TM-650 2.5.6.3 test method, which uses smooth electrodes on insulation material samples. Tests in this report use an asymmetrical configuration with an etched copper HV electrode and aluminium ground plane (see Section 3.2).



(a) Weibull probability plot.

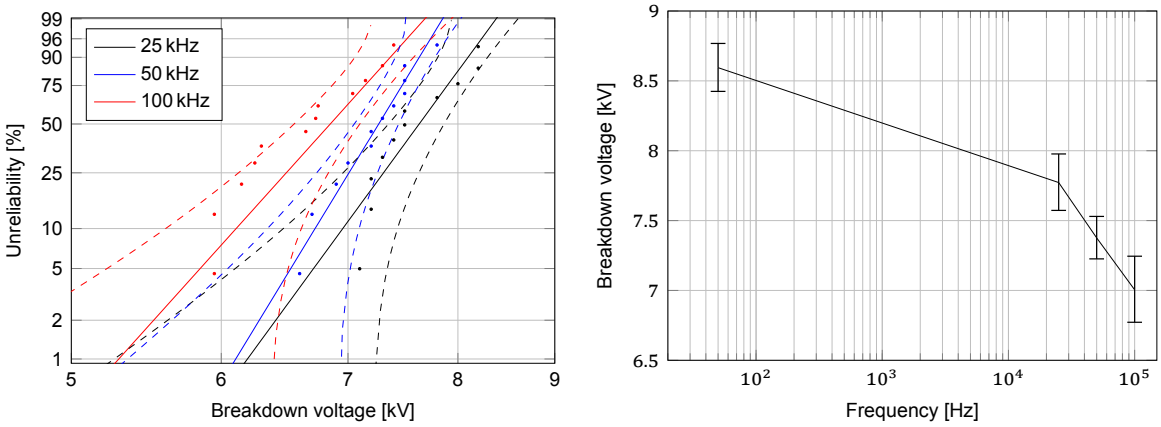
(b) Breakdown voltage vs thickness.

Figure 4.3: Short breakdown dependence on dielectric thickness d for 10 mm electrode.

4.2.2. Test 1: Effect of Frequency

The first test investigates the effect of frequency and voltage waveform on the ramp breakdown voltage. Tests are performed with high-frequency square-wave and sinusoidal voltages and compared to the results presented in the previous section.

Comparison AC and HF Sine Wave Next, the effect of frequency is investigated using sinusoidal waveforms. Tests are performed at 25, 50, and 100 kHz and compared to the results obtained for 50 Hz in Figure 4.4. As expected, the breakdown voltage decreases with increasing frequency. It is likely that the degradation only starts at a certain frequency f_{crit} and follows an inverse power law from there [23].

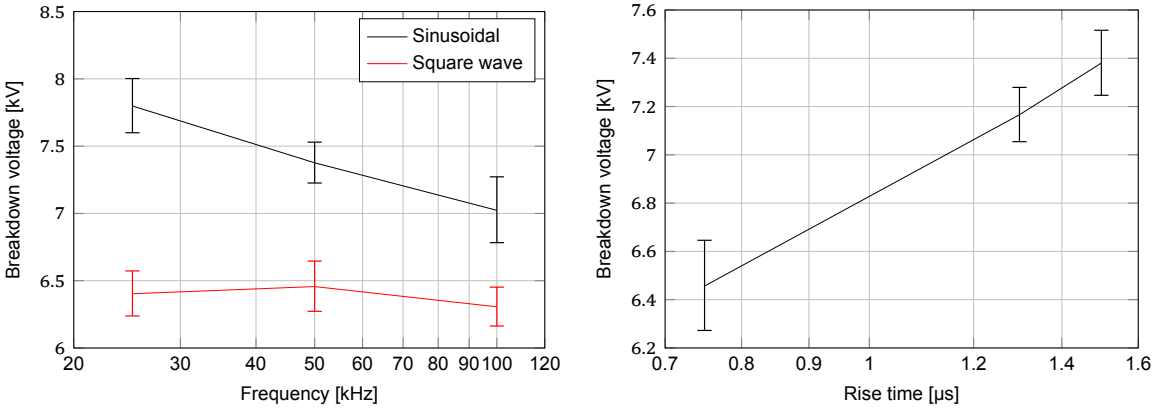


(a) Weibull probability plot for Sample A.

(b) Breakdown voltage vs frequency.

Figure 4.4: Effect of frequency (AC and HF sinusoidal voltage).

Comparison HF Sine and Square Wave To investigate the effect of harmonics in the voltage waveform, the breakdown results for sinusoidal and square wave voltages (at 25, 50, and 100 kHz) are compared in Figure 4.5. The square-wave breakdown results indicate a strong dependency on the rise time (i.e., the harmonics of the waveform), whereas it is nearly independent of frequency in the tested range. This behaviour is investigated in detail in Section 4.7.



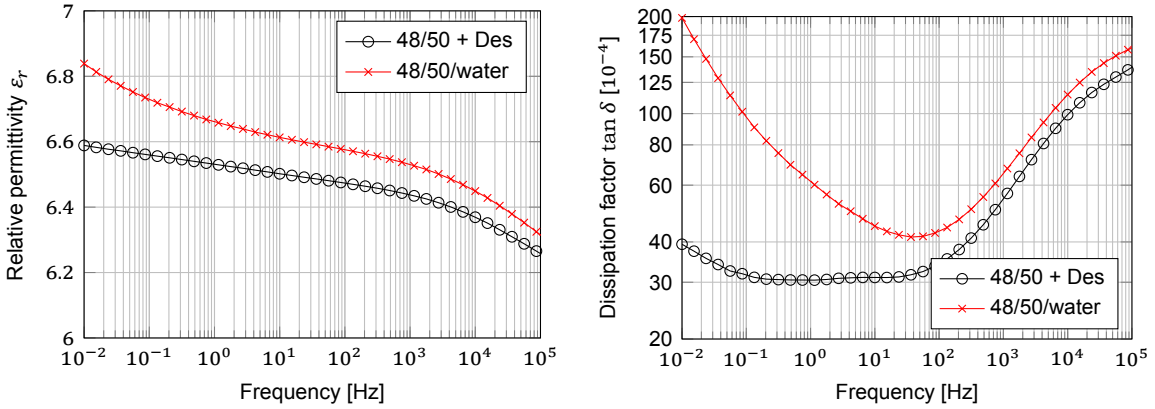
(a) Breakdown voltage vs frequency (square wave has t_r = 750 ns).

(b) Breakdown voltage vs rise time (f = 50 kHz).

Figure 4.5: Comparison of sinusoidal and square wave voltage.

4.2.3. Test 2: Effect of Moisture

The dielectric response (Figure 4.6, measured with Novocontrol dielectric response analyser) shows that a significant amount of water has been absorbed: a low-frequency relaxation peak has appeared below 10 mHz (increase in both ε_r and $\tan\delta$ at low frequency). Quantitative measurement of the moisture content could not be performed, but the preconditioning procedure asserts complete saturation of the insulation [66, 67].

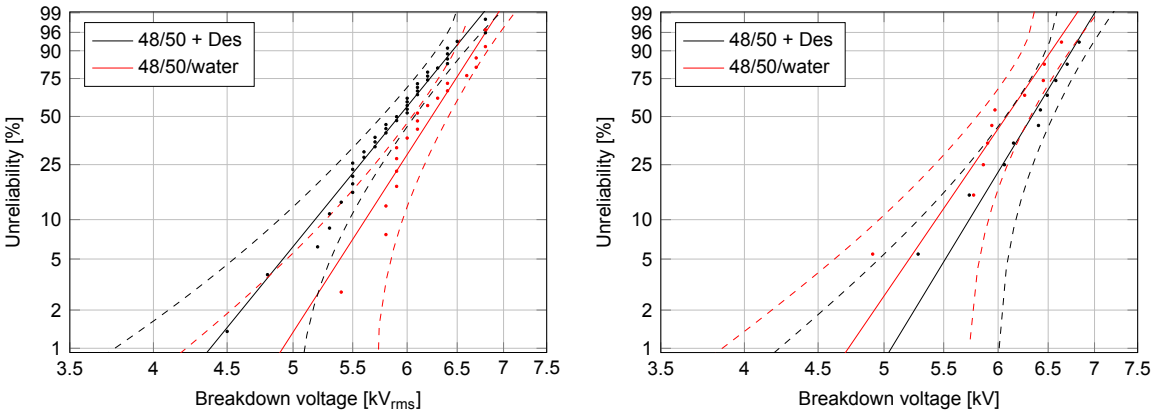


(a) Relative permittivity ε_r.

(b) Dissipation factor $\tan\delta$.

Figure 4.6: Dielectric response of sample A before and after moisture preconditioning (as described in Section 3.4.2).

Short breakdown tests are performed with 50 Hz AC and 50 kHz square wave voltage. The results are compared against dry PCB samples from test 1 in Figure 4.7. The lack of degradation due to moisture at 50 Hz is entirely unexpected and not in agreement with data shared by the manufacturer, based on which a 50 % decrease in breakdown strength was expected. This is likely due to a difference in testing method: the measurements were performed under oil, mostly eliminating the degradation of the solder mask and preventing surface discharges (as described in Section 4.1). If the manufacturer performed tests in air, the moisture might have influenced the withstand strength of the solder mask, leading to lower breakdown voltages.



(a) Weibull probability plot (50 Hz AC).

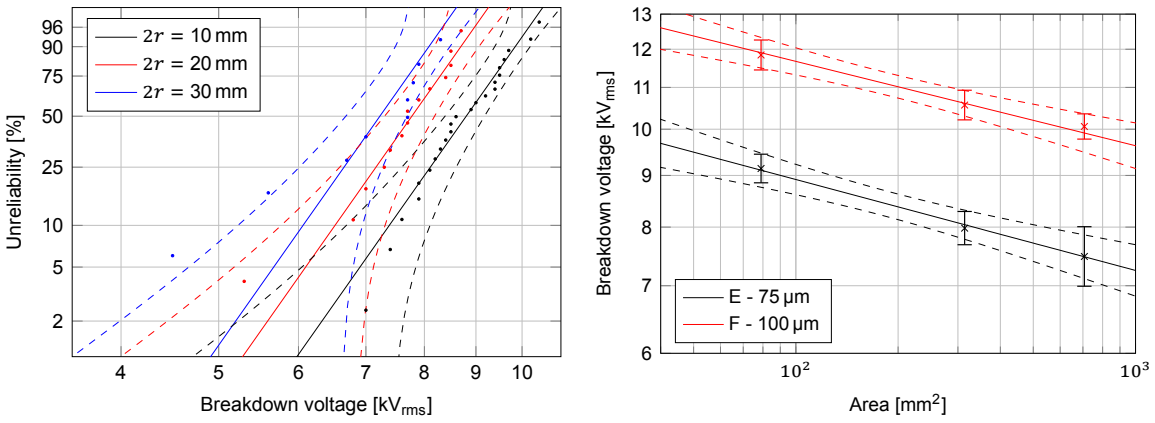
(b) Weibull probability plot (50 kHz square wave).

Figure 4.7: Results of test 2: Effect of moisture.

It can be seen that the breakdown voltage does decrease more rapidly with frequency after moisture saturation. Under dry conditions, the breakdown voltage drops by 24 % from 50 Hz AC to 50 kHz square wave. After moisture saturation, the breakdown voltage decreased by 31 %. This may be attributed to the increased $\tan\delta$, which increases the dielectric loss after moisture saturation.

4.2.4. Test 3: Volume Effect

According to statistical theory, the breakdown voltage of a configuration should decrease when the insulation volume increases. Provided that the field distribution stays the same, the decrease was shown to be $n^{-1/\beta}$ in Appendix E.5, where n is the volume increase. In this case, the electrode area A is varied by making samples with three electrode diameters: 10, 20, and 30 mm. Figure 4.8 shows the resulting Weibull plots and the breakdown voltage versus electrode area.



(a) Weibull probability plot for Sample E (diameter $2r$)

(b) Breakdown voltage vs area.

Figure 4.8: Results of test 3: Volume effect.

The predicted relationship is verified statistically by assuming that (i) all measurement series have equal β, and (ii) the $\eta(A)$ are related by a power law with exponent k. The results in Tables 4.2 and 4.3 show that both assumptions are true and $k \approx -1/\beta$.

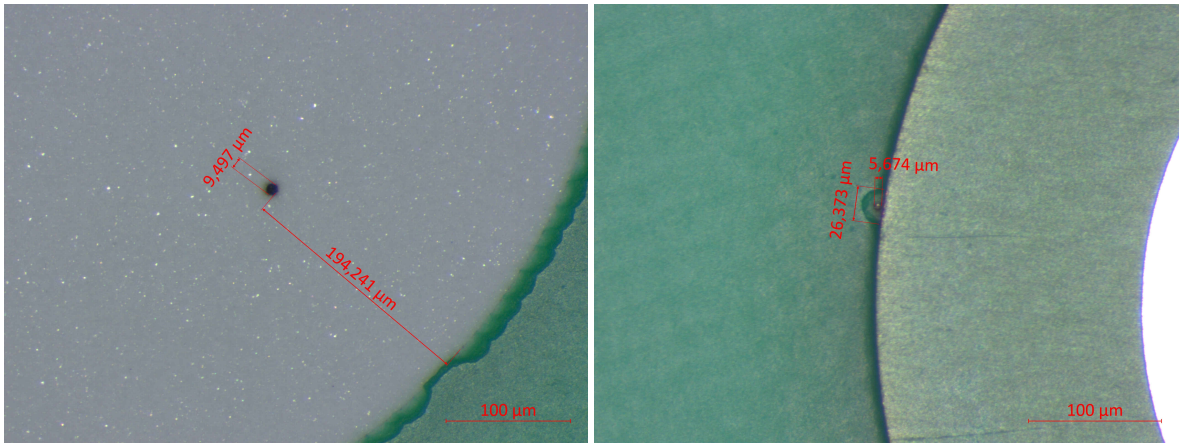
Table 4.2: Comparison of MLE models – Volume effect on Sample E.

Model	$-2\mathcal{L}$	AIC	#Parameters
SepDists	118.8	130.8	6
EqualSig	119.9	127.9	4
RegrModel	120.2	126.2	3
Comparison	**LR stat.**	**dof**	**p-value**
SepDists vs EqualSig	1.1225	2	0.5705
EqualSig vs RegrModel	0.3317	1	0.5647

Table 4.3: Results of test 3: Volume effect.

d [µm]	η_{10} [kV]	η_{20} [kV]	η_{30} [kV]	$1/\beta$	k
75	9.1 ± 0.3	8.0 ± 0.3	7.5 ± 0.5	0.093 ± 0.018	−0.090 ± 0.025
100	11.8 ± 0.4	10.6 ± 0.4	10.1 ± 0.3	0.083 ± 0.016	−0.084 ± 0.022

For these 50 Hz measurements, almost all breakdown events occur at a random location under the electrode. However, when performing breakdown tests using HF sinusoidal voltage, most breakdowns were recorded at the edge of the electrode (see Figure 4.9). This suggests that the breakdown voltage at high frequency should scale with the circumference of the electrode instead of its area.



(a) Breakdown under electrode (50 Hz sine, copper removed).

(b) Breakdown at electrode edge (25 kHz sine).

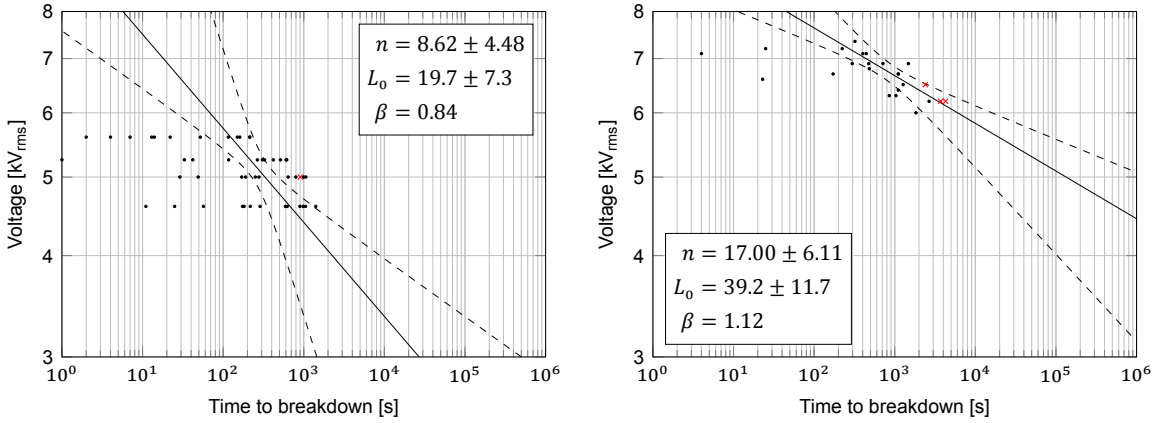
Figure 4.9: Micrographs of broken samples.

4.3. Lifetime Tests

Lifetime tests are performed with 50 Hz AC and HF sinusoidal voltages to evaluate the impact of frequency on the useful electrical life of the dielectric.

4.3.1. AC Voltage

First, lifetime tests are performed with 50 Hz AC voltage to provide a reference for the high-frequency measurements. Tests are performed at several voltage levels for samples A, E, and F. The results are processed statistically using the procedure described in Section 3.6.3. Test results are presented in Figure 4.10. Table 4.4 gives a summary of the derived parameters.



(a) Lifetime curve for Sample A ($d = 50\,\mu m$).

(b) Lifetime curve for Sample E ($d = 75\,\mu m$).

Figure 4.10: Lifetime test results with 50 Hz AC voltage. Dots (·) and crosses (×) indicate full and censored observations. The dashed lines indicate the 95 % confidence bands.

Table 4.4: Lifetime results for 50 Hz AC voltage and $d = 10$ mm. The lifetime L_0 is normalized to $U = 1\,kV_{rms}$.

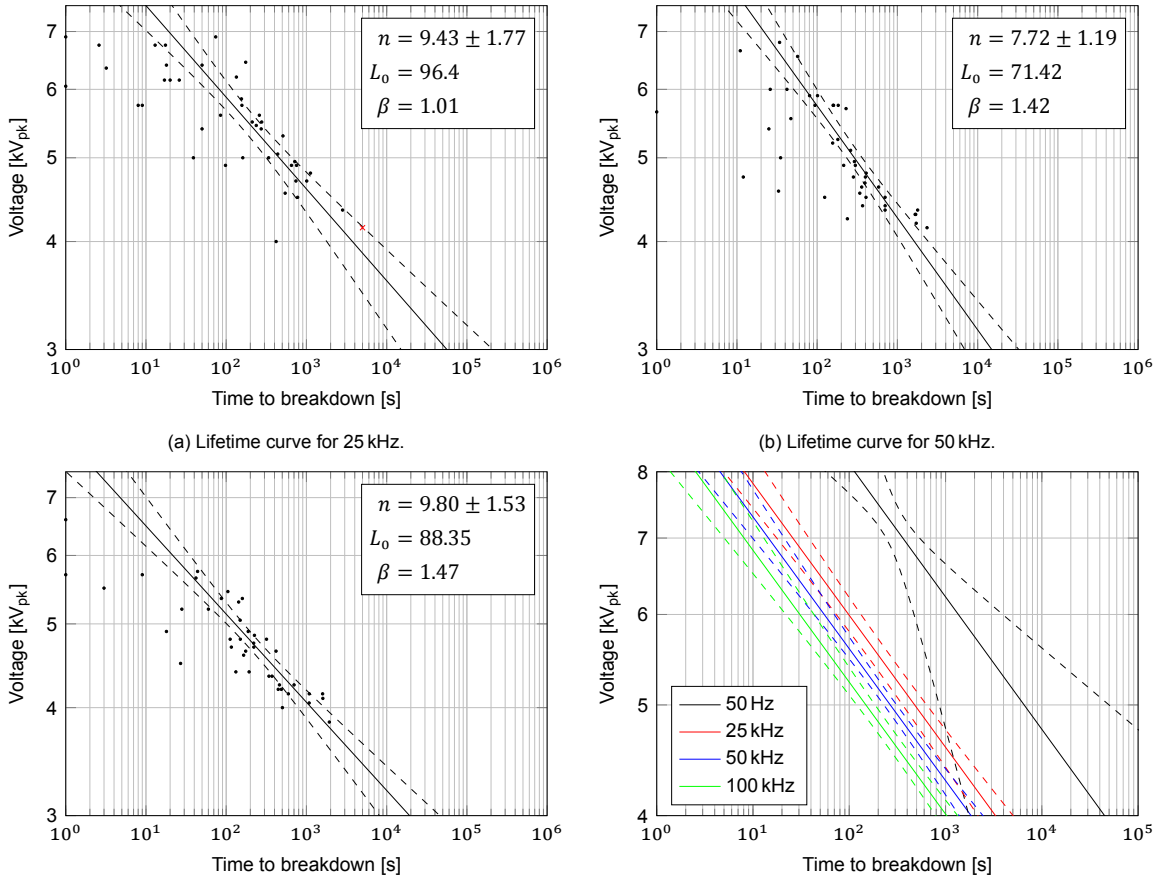
d	n	L_0	β
50 µm	8.62 ± 4.48	19.7 ± 7.3	$0.84^{+0.21}_{-0.14}$
75 µm	17.00 ± 6.11	39.2 ± 11.7	$1.12^{+0.51}_{-0.27}$
100 µm	25.80 ± 9.98	63.7 ± 22.3	$0.77^{+0.28}_{-0.16}$

The power law exponent n indicates the level of degradation. It corresponds to the slope $-1/n$ of the

lifetime curve. The typical range of n for high-voltage constructions is 10 to 20 and higher n is better. Observe that the exponent n and lifetime at the reference voltage of 1 kV increase significantly with increasing dielectric thickness.

4.3.2. High-Frequency Sinusoidal Voltage

Next, lifetime tests are performed under high-frequency sinusoidal voltage stress with the resonant setup. The lifetime curves for sample A are shown in Figure 4.11.



(a) Lifetime curve for 25 kHz.

(b) Lifetime curve for 50 kHz.

(c) Lifetime curve for 100 kHz.

(d) Comparison of lifetime curves using frequency power law model.

Figure 4.11: Lifetime test results for sample A with HF sinusoidal voltage. Dots (·) and crosses (×) indicate full and censored observations. The dashed lines indicate the 95 % confidence bands.

In the frequency range 25 to 100 kHz, the confidence intervals of the measured lifetime curves overlap significantly. In the literature, it is reported that the slope n is approximately frequency-independent and lifetime inversely proportional to frequency for composite organic/inorganic insulation (such as the IMS material discussed here) [31]. Although this is not immediately obvious from the measured curves, these statements can be verified statistically by defining three MLE estimation models, similar to the implementation of the power law regression:

- SepDists: Each of the three investigated frequencies has its own regression model distribution as explained in Section 3.6.3. This results in nine MLE parameters: $\theta = [L_1, L_2, L_3, n_1, n_2, n_3, \beta_1, \beta_2, \beta_3]$.
- EqualN: The first statement (n is frequency-independent) will be verified by assuming that $n_1 = n_2 = n_3 = n$, yielding seven MLE parameters: $\theta = [L_1, L_2, L_3, n, \beta_1, \beta_2, \beta_3]$.
- RegrModel: The second statement (lifetime is inversely proportional to frequency) will be verified by assuming that the lifetime follows an inverse power law versus frequency, as described in Section 2.4. The resulting six MLE parameters are: $\theta = [L_0, k, n, \beta_1, \beta_2, \beta_3]$.

These three models are compared in Table 4.5, which shows that both assumptions hold. The first assumption has a low p-value because the slope of the 50 kHz curve is quite different. Nevertheless, the hypothesis cannot be rejected at any reasonable confidence level. The frequency exponent is $k = 0.84 \pm 0.25$, which is close to the expected inverse relationship ($k = 1$). The lifetime slope is $n = 8.65 \pm 0.87$, which is very similar to the slope at 50 Hz.

Table 4.5: Comparison of MLE models.

Model	$-2\mathcal{L}$	AIC	#Parameters
SepDists	1551.2	1569.2	9
EqualN	1556.0	1570.0	7
RegrModel	1557.8	1569.8	6
Comparison	**LR stat.**	**dof**	**p-value**
SepDists vs EqualN	4.837	2	0.0890
EqualN vs RegrModel	1.748	1	0.1861

Tests at 25 kHz are also performed for a thicker dielectric (sample E, 75 µm) to verify whether the lifetime slope will again be equal for 50 Hz and high-frequency stress. The other samples (with $d > 75$ µm) could not be broken using the resonant setup because of its limited output voltage. The comparison of the results is shown in Table 4.6. For sample E, the slope of the lifetime curve appears to be much lower at high frequency, whereas no significant difference is observed for sample A. This could again be related to the two competing failure modes, as shown in Figure 4.9.

Table 4.6: Comparison of lifetime curves for Samples A and E.

d	f	n	L_0	β
50 µm	50 Hz	8.62 ± 4.48	22.7 ± 10.8	$0.84^{+0.21}_{-0.14}$
	25 kHz	8.65 ± 0.87	20.1 ± 1.8	$1.02^{+0.25}_{-0.18}$
	50 kHz	8.65 ± 0.87	19.5 ± 1.7	$1.32^{+0.36}_{-0.23}$
	100 kHz	8.65 ± 0.87	18.9 ± 1.6	$1.49^{+0.41}_{-0.27}$
75 µm	50 Hz	17.00 ± 6.11	45.0 ± 16.9	$1.12^{+0.51}_{-0.27}$
	25 kHz	9.48 ± 1.91	23.1 ± 3.6	$1.09^{+0.31}_{-0.20}$

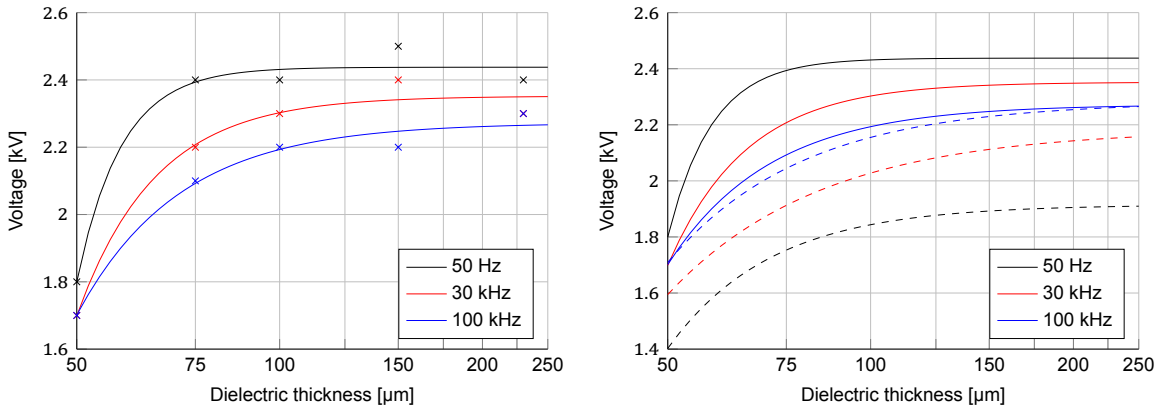
4.4. Partial Discharge Analysis

PD analysis is performed to investigate the observations in the previous sections further. Some conclusions can be drawn about the ageing mechanisms that occur in the dielectric. The setup discussed in Section C.3 is used for the high-frequency PD measurements. For the reference measurements at 50 Hz, a Hipotronics DDX9101 is used with an AQS9110a measurement impedance. Surface and internal discharges are investigated separately. Appendix D presents a detailed analysis of the patterns.

4.4.1. Surface Discharges

All breakdown tests were performed under oil, as explained in Section 4.1, to avoid flashover on the PCBs. Surface discharges are present as a precursor to flashover and may initiate tracking. Literature and prior experience suggest that the initiation of tracking (or the formation of electrical trees on the surface of the solder mask) is drastically accelerated by high-frequency excitation. The inception and extinction voltages of these surface discharges are recorded in Figure 4.12. From the results for 150 µm and 230 µm samples, it seems that the insulation thickness is not necessarily the dominant factor in determining the inception and extinction voltages. The thickness of the solder mask, which is usually not very well-defined, is also critical.

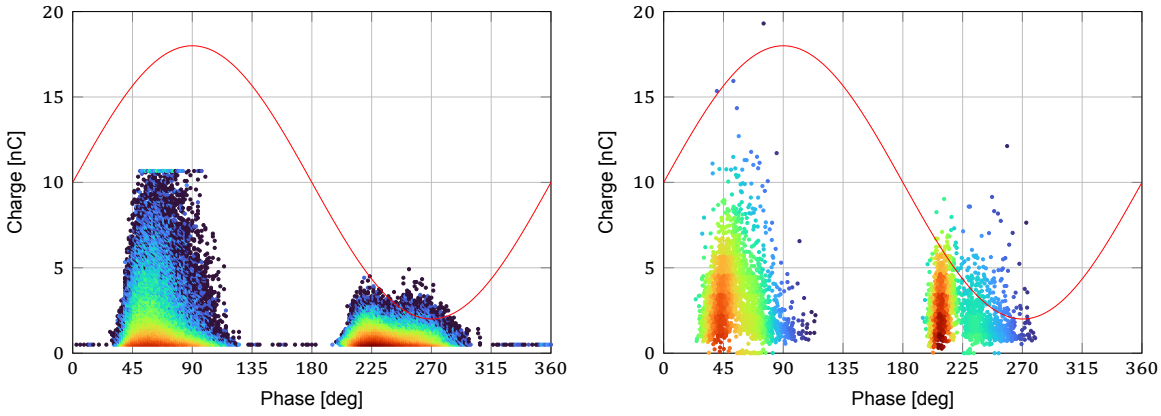
PRPD patterns of the surface discharges on sample A (50 µm) recorded at 50 Hz and 25 kHz are presented in Figure 4.13. As predicted by the theory, the magnitude of the discharges under HF excitation is larger than that under 50 Hz. Additionally, the discharges are concentrated around 40° and 210°,



(a) Inception voltage vs dielectric thickness.

(b) PDIV (solid) and PDEV (dashed)

Figure 4.12: Surface discharge inception and extinction voltages (peak).



(a) 1.7 kV_{pk} at 50 Hz.

(b) 1.7 kV_{pk} at 25 kHz.

Figure 4.13: PRPD patterns for surface discharges on Sample A. Color indicates the number of events per cycle (red: high).

as opposed to the much wider bands around 45° to 90° and 210° to 270° for 50 Hz. The discharge pattern is asymmetric, skewed towards the positive half-cycle in both cases due to the configuration of electrodes (small HV electrode, large ground plane).

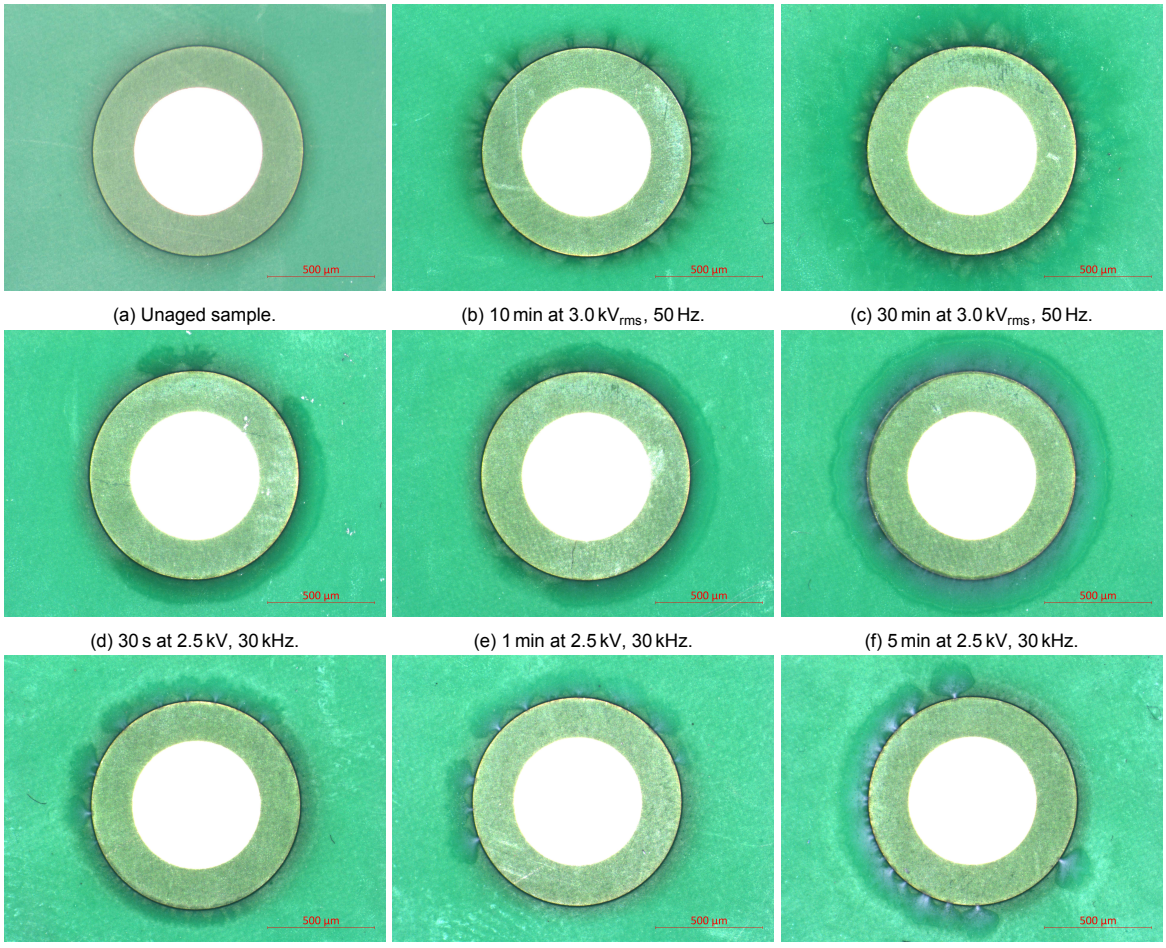
Conformal Coating Conformal coating provides an extra layer of insulating material over the solder mask and copper traces, reducing the field strength in the air. In addition, it protects the surface against pollution and humidity. Therefore, a conformal coating can increase the surface discharge inception voltage, as shown in Table 4.7.

Table 4.7: Surface discharge inception and extinction voltages (peak) for coated PCBs.

d	50 Hz	30 kHz
150 µm	3.3 kV/2.4 kV	3.0 kV/2.5 kV
230 µm	4.0 kV/3.7 kV	3.3 kV/2.9 kV

Surface Degradation While measuring the surface discharge behaviour over longer periods of time, a fine white residue built up around the electrode. Photographs at various frequencies and ageing times are presented in Figure 4.14. Several minutes under high-frequency excitation just above the PDIV was enough to cause significant whitening. At 50 Hz, no residue was seen even after 30 min, although the onset of degradation is already clearly visible. This phenomenon is also observed at 50 Hz

on normal FR4 PCBs (e.g., by Emersic et al. [53]) after several hundred hours of ageing. This confirms that high-frequency voltages accelerate surface degradation significantly since the PD repetition rate is proportional to the voltage frequency.



(a) Unaged sample. (b) 10 min at 3.0 kV_{rms}, 50 Hz. (c) 30 min at 3.0 kV_{rms}, 50 Hz.

(d) 30 s at 2.5 kV, 30 kHz. (e) 1 min at 2.5 kV, 30 kHz. (f) 5 min at 2.5 kV, 30 kHz.

(g) 30 s at 2.5 kV, 100 kHz. (h) 1 min at 2.5 kV, 100 kHz. (i) 5 min at 2.5 kV, 100 kHz.

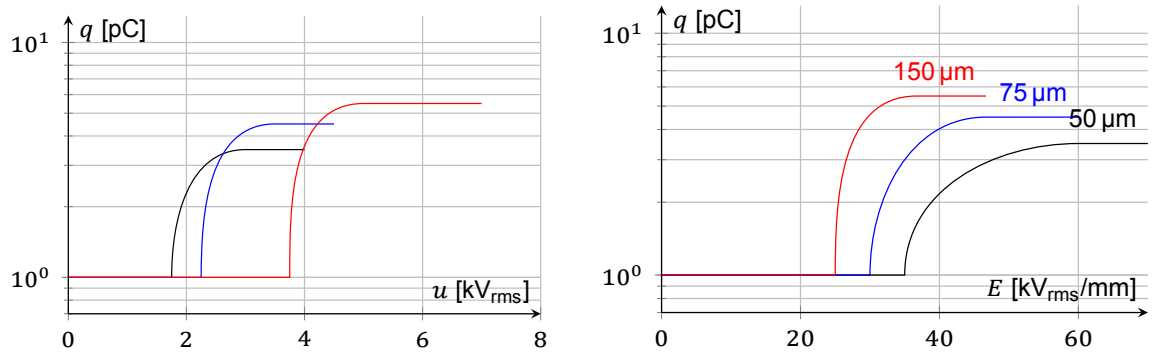
Figure 4.14: Surface degradation on Sample B (150 µm dielectric, 3 oz copper).

The white powder can be wiped off quite easily, but the surface is irreversibly damaged. It is most likely a by-product of the chemical degradation of the solder mask. Reactions with ozone result in chain scission and may generate peroxides, ketones, aldehydes, and carboxylic acids [72, 73].

4.4.2. Internal Discharges

Submerging the PCBs in oil eliminates the surface discharges until a certain voltage. This allows for the detection of internal discharges (if present), which could give some insight into the underlying ageing and breakdown mechanisms. PD tests were performed at 50 Hz for samples A (50 µm), E (75 µm), and B (150 µm). The discharge magnitude is small, making it difficult to determine the inception voltage. The measured (average) discharge magnitude versus voltage is presented in Figure 4.15, which shows that discharges appear above the 1 pC noise floor at a field strength which decreases with increasing dielectric thickness. Based on the inception voltages, the cavities have a size of 3 to 4 µm [54], which could be the case given the microstructure of the dielectric.

Partial discharge patterns over time for sample E at 4.3 kV_{rms} are presented in Figure 4.16. The pattern shows characteristics of cavity discharges (e.g., rabbit-ear pattern) and a certain degree of instability: larger, wing-like discharges appear occasionally. This, combined with the detailed analysis in Appendix D, suggests that the PDs are a combination of cavity and treeing discharges. Similar patterns are observed for the other tested samples.

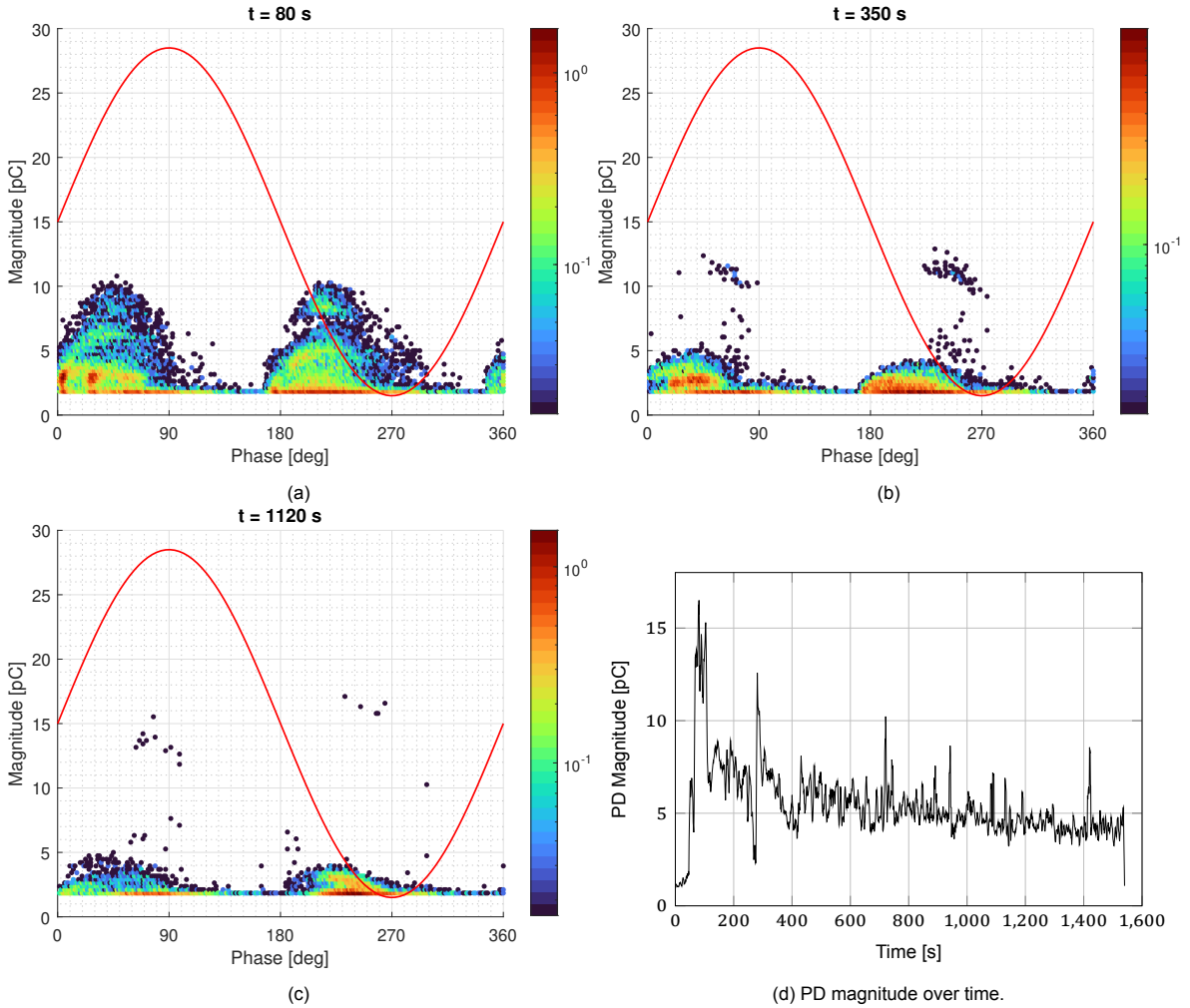


(a) Discharge magnitude vs voltage.

(b) Discharge magnitude vs field strength.

Figure 4.15: Internal discharge inception.

The discharge magnitude decreases over time, as presented in Figure 4.16d. Initially, the cavity contains fresh gas and no space charges, resulting in large streamer discharges. As the discharges degrade the cavity, shallow traps are formed on the cavity surface, and it becomes more conductive, resulting in a decreasing PD magnitude [74].



(a)

(b)

(c)

(d) PD magnitude over time.

Figure 4.16: PRPD of Sample E at 4.3 kV$_{rms}$

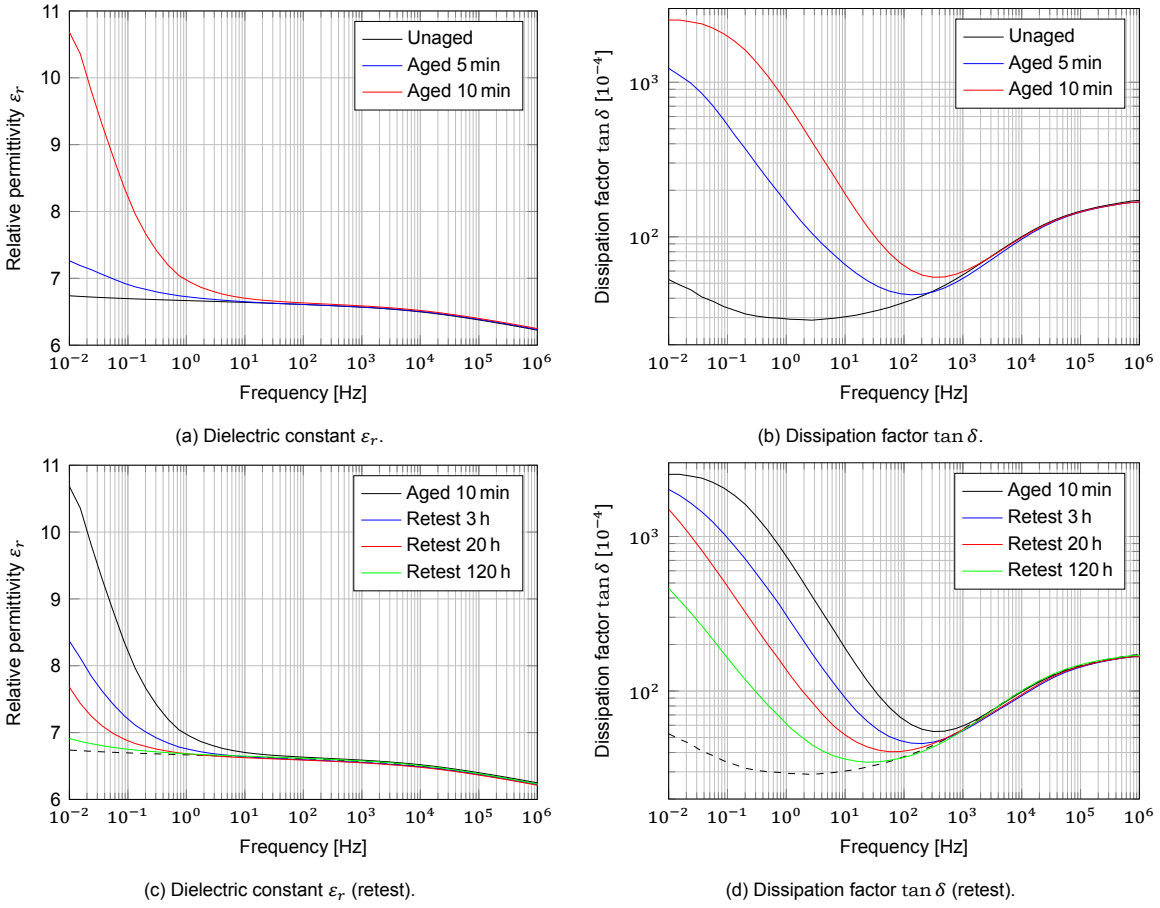
Because of the small magnitude of the discharges, they could not be detected using the high-frequency PD setup. The sensitivity of the detector should be improved to investigate HF internal PD.

4.5. Dielectric Response Analysis

To further investigate the internal processes leading to electrical breakdown, PCB samples are electrically aged. Afterwards, the dielectric frequency response (DFR) is recorded using the Novocontrol Alpha dielectric spectrometer. The dielectric response can show the accumulation of space charge in the dielectric by the appearance of a low-frequency relaxation peak which dissipates over time [75]. Bulk changes to the properties of the polymers (relaxations and conductivity) are also visible.

4.5.1. Space Charge Accumulation under Surface PD

Samples of 50 µm dielectric thickness were aged at 3.5 kV_{rms} 50 Hz and 1.7 kV 25 kHz in air, which is well above the surface PDIV. A DFR measurement is taken (Figure 4.17) before ageing and after ageing for 5 and 10 min. The aged samples are retested several times.



(a) Dielectric constant ε_r.

(b) Dissipation factor $\tan\delta$.

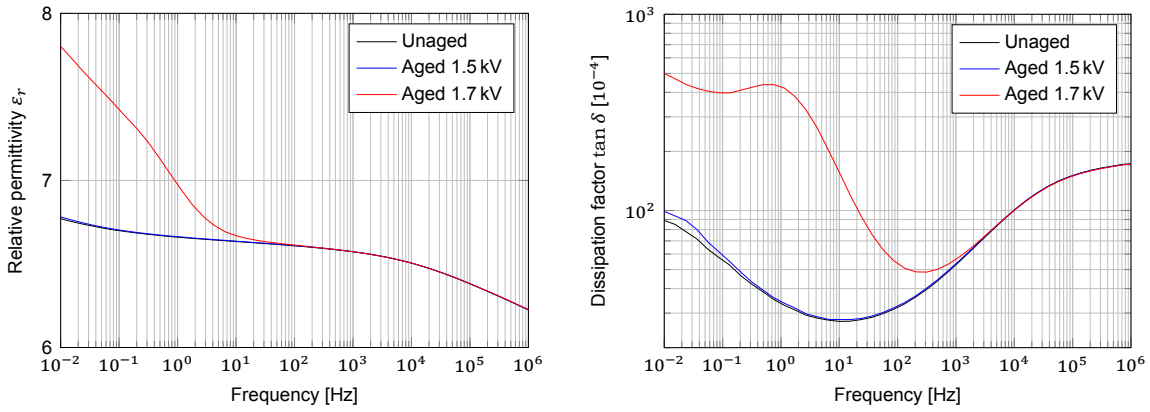
(c) Dielectric constant ε_r (retest).

(d) Dissipation factor $\tan\delta$ (retest).

Figure 4.17: DFR before and after electrical ageing at 3.5 kV_{rms}, 50 Hz AC.

After electrical ageing, the low-frequency ε_r and $\tan\delta$ have increased significantly compared to the unaged sample. The low-frequency relaxation peak in the $\tan\delta$ spectrum indicates that this is due to the accumulation of space charge in the dielectric [75]. The fact that the changes are partially reverted in the retests confirms this. Space charge may accumulate in the dielectric due to injection at the electrodes (field- or thermionic emission) or partial discharge activity [44].

Performing the ageing at voltages slightly below and above the surface PDIV (Figure 4.18) shows that the hypothesis presented above is true: the charges accumulate due to PD activity, in this case on the surface of the dielectric. Here, the relaxation peak is even more apparent than at 50 Hz, but the magnitude of the deposited charge is less since the testing voltage is much lower.



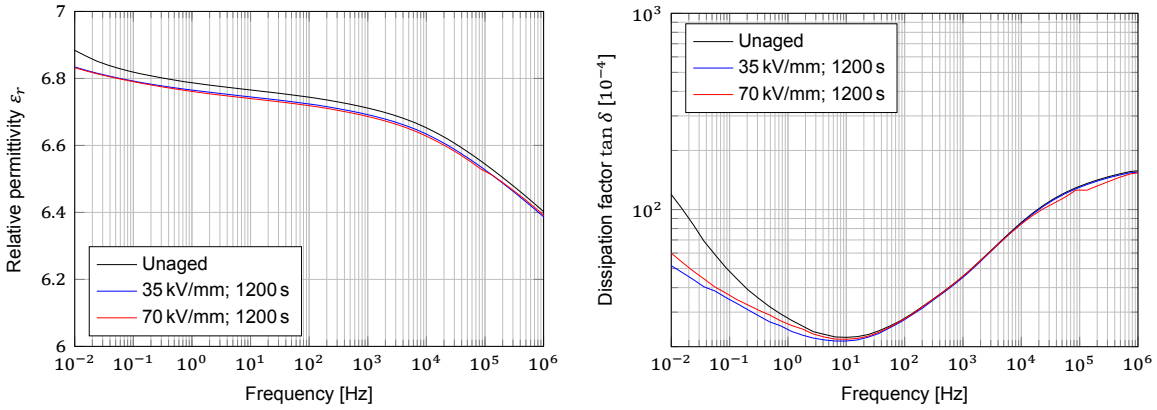
(a) Dielectric constant ε_r.

(b) Dissipation factor $\tan\delta$.

Figure 4.18: DFR before and after electrical ageing with 25 kHz sinusoidal voltage for 10 min.

4.5.2. Ageing with 50 Hz AC Voltage

Surface PD was eliminated by performing the following tests under oil. Samples of type F (100 µm dielectric) are aged under several high electric field strengths. After ageing, the DFR measurements in Figure 4.19 show a lower $\tan\delta$ and slightly lower ε_r. The conductivity of the sample has decreased for 35 kV/mm, and from there slightly increased for 70 kV/mm. This is consistent with the formation of deep traps due to, e.g., partial discharge activity [76, 77]. In addition, PD activity in cavities results in the formation of shallow traps on the cavity surface [74].



(a) Dielectric constant ε_r.

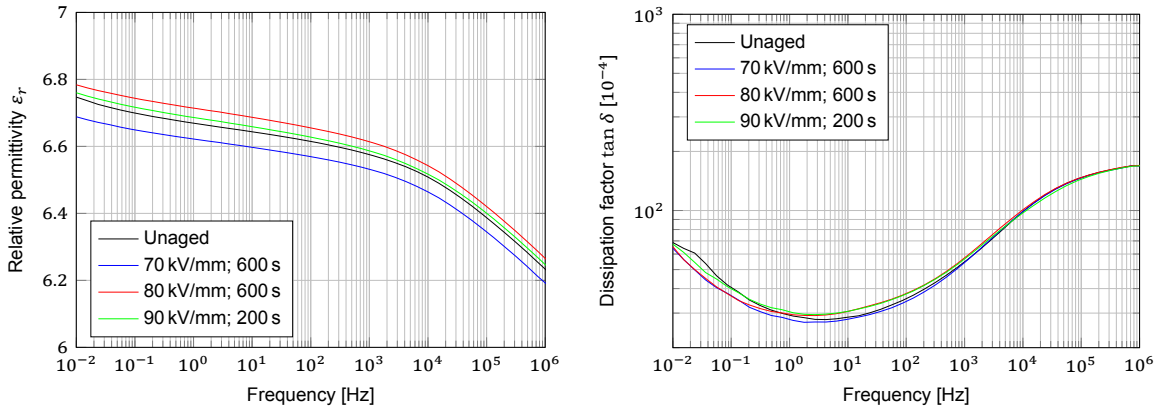
(b) Dissipation factor $\tan\delta$.

Figure 4.19: DFR before and after electrical ageing with 50 Hz AC voltage.

Until a certain point, deep traps reduce the conductivity of the dielectric by trapping charges and preventing them from taking part in the conduction process. However, when the deep trap density increases further, the distance between the trapping sites becomes small enough for tunnelling (e.g., through the Poole–Frenkel effect) the conductivity and leakage current increase, eventually leading to breakdown when a critical trap density is reached [76].

4.5.3. Ageing with 25 kHz Sinusoidal Voltage

Samples of 50 µm dielectric thickness were aged at 25 kHz. The DFR measurements in Figure 4.20 before and after ageing show no significant changes. The small variation in ε_r is due to thickness variation between samples. The lack of changes in the DFR could indicate (i) no PD activity and chemical degradation, or (ii) very localised degradation (since the DFR measures the bulk properties).



(a) Dielectric constant ε_r.

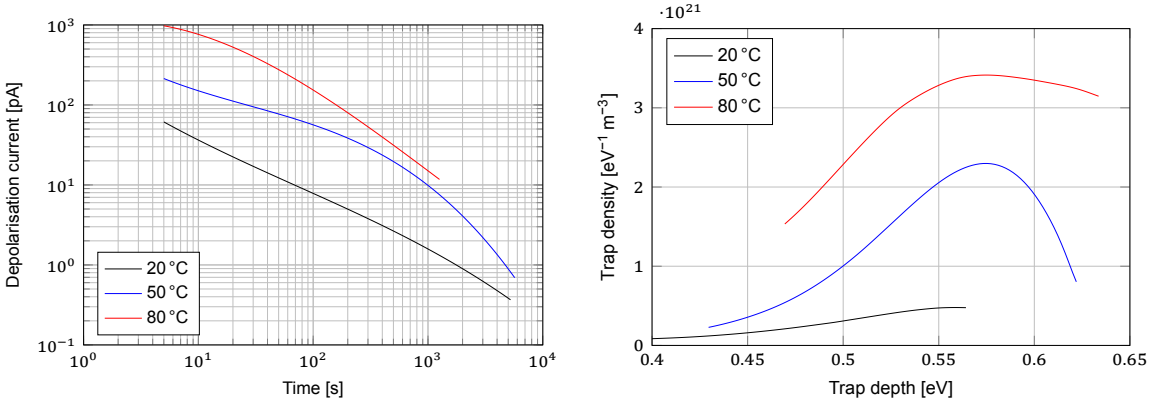
(b) Dissipation factor $\tan\delta$.

Figure 4.20: DFR before and after electrical ageing with 25 kHz sinusoidal voltage.

4.6. Isothermal Relaxation Current Analysis

The isothermal relaxation current (IRC) method allows for the derivation of trap energy levels and density from a relatively simple depolarisation current measurement, as described in Section 3.1.3. The DFR measurements in the previous section are extended using the IRC method to investigate whether the trap structure of the dielectric is altered due to electrical ageing.

Figure 4.21a shows the depolarisation current measured for an unaged PCB sample at three temperatures. Using the relations derived by Simmons et al. [60], the attempt-to-escape frequency ν and the trap distribution are derived and shown in Figure 4.21b. The calculated $\nu \approx 10^6\,\mathrm{Hz}$ is orders of magnitude lower than the 10^{11}–10^{13} Hz suggested in most literature. However, this range of ν was measured for inorganic semiconductors, and much lower values of ν have since been measured for various polymers [78, 79] and ceramics [80].



(a) Depolarisation current

(b) Trap distribution using $\nu = 10^6$ Hz

Figure 4.21: IRC of unaged Sample A at 20, 50, and 80 °C, E_{pol} = 10 kV/mm.

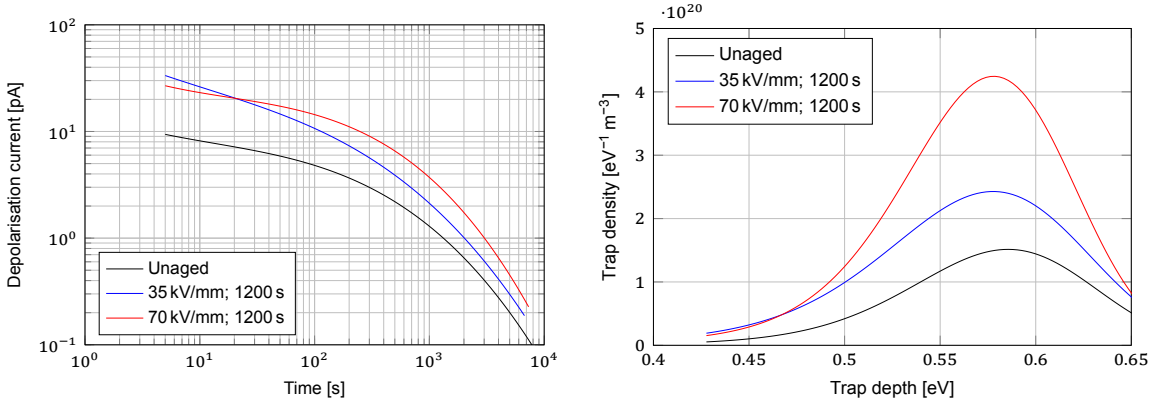
The unaged material contains traps with a depth of 0.57 eV, typically classified as shallow traps. This value of trap depth matches well with measurements on epoxy and epoxy-mica composites in literature [81]. Literature suggests that there should also be deep traps around 0.9 to 1.0 eV. However, these cannot be measured with the existing setup due to the required depolarisation time. Since epoxy is a polar dielectric, observed peaks in the $i_d t$–$\ln t$ spectrum may also be due to the α- and β-relaxations (i.e., main chain and side chain/polar groups). However, this should not be the case here since tests are performed much below T_g, and the trap depth differs from the activation energies expected for α- and β-relaxation.

As the temperature increases, the trap density seems to increase. This artefact of the measurement procedure indicates that the polarisation time of 5000 s is insufficient to fill the traps completely.

Therefore, the trap densities reported in the following paragraphs should only be compared to samples that have undergone identical polarisation conditions (time, field, and temperature).

4.6.1. Ageing with 50 Hz AC Voltage

The samples from Section 4.5.2 were further analysed using the IRC method. Figure 4.22 shows that the density of shallow traps increased due to electrical ageing. This is typically attributed to an increase in the number and severity of physical defects. Deep traps, on the other hand, correspond to chemical degradation [82]. Shallow traps may appear on the surface of cavities after exposure to PD [74].



(a) Depolarisation current

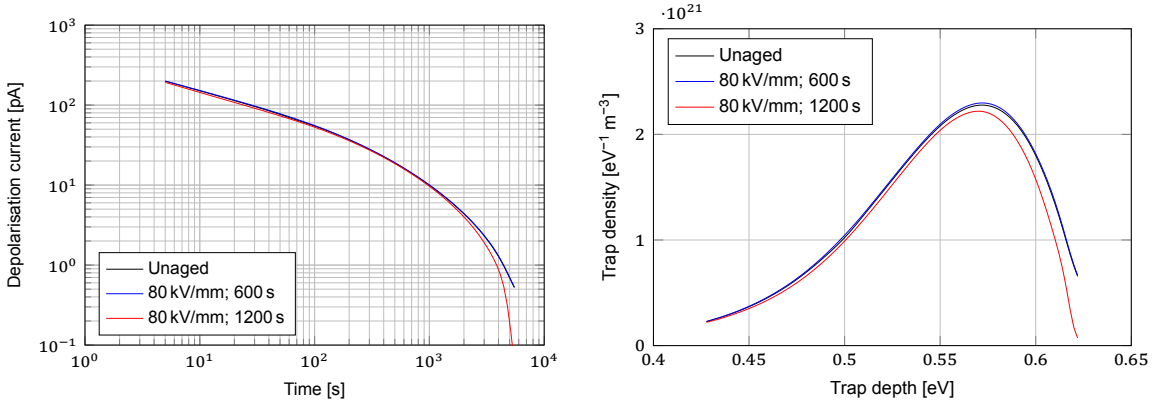
(b) Trap distribution using $\nu = 10^6$ Hz

Figure 4.22: IRC of aged Sample F at 50 °C, $E_{pol} = 5\,\mathrm{kV/mm}$.

Based on the DFR results, the trap density of the deep traps is also expected to increase. However, this cannot be verified with these IRC measurements. A method like TSDC is required to obtain the full trap distribution.

4.6.2. Ageing with 25 kHz Sinusoidal Voltage

Similarly, the samples from Section 4.5.3 were analysed using the IRC method (see Figure 4.23). This confirms that there is no bulk effect on the trap distribution due to high-field electrical ageing with high-frequency voltage.



(a) Depolarisation current

(b) Trap distribution using $\nu = 10^6$ Hz

Figure 4.23: IRC of aged Sample A at 50 °C, $E_{pol} = 10\,\mathrm{kV/mm}$.

4.7. High-Frequency Breakdown and Ageing Mechanisms

The data presented in the previous paragraphs show several trends that may give insight into the electrical breakdown and ageing mechanisms that occur in the IMS dielectric. The two most common failure mechanisms (see, e.g., Section 2.3) are (i) thermal breakdown, and (ii) partial discharge erosion.

4.7.1. Thermal Breakdown

Typically, under 50 Hz AC conditions, thermal breakdown is the leading cause during short ramp tests, and partial discharge erosion only becomes relevant after a longer time period. However, thermal breakdown is unlikely in the situation under study. First, the insulating material is optimised for thermal performance and low thermal resistance. This means that high losses are required to cause a thermal breakdown. Second, the dielectric loss in Figure 4.24 shows a large dependence on the fundamental frequency but not the rise time. This does not agree with the observed breakdown voltages (Figure 4.5), which depend heavily on the rise time.

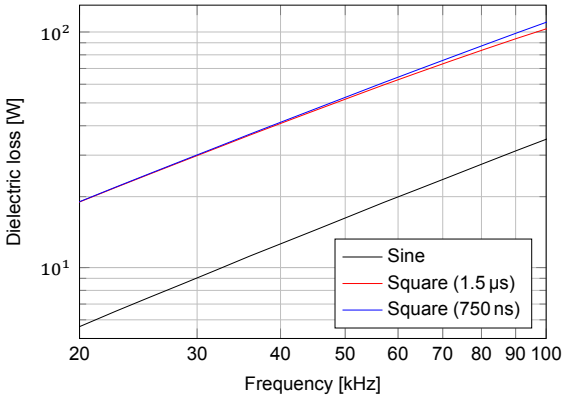


Figure 4.24: Dielectric loss calculated at 6.5 kV for sample A (d = 50 µm, r = 5 mm).

From the data obtained from testing with a square-wave voltage, it is clear that the high-frequency components are the dominant factor determining the breakdown voltage, which is incompatible with the thermal breakdown mechanism.

4.7.2. Partial Discharge Erosion

On the other hand, it has been shown that the PD magnitude is inversely proportional to rise time [28, 30]. Together with the observation that the PD repetition rate is extremely high under high-frequency voltages (≥ 1 PD event per cycle) [26] makes PD erosion a plausible ageing mechanism, even for short breakdown tests. In this case, it can be expected that the sinusoidal breakdown voltage will tend to that of the square wave at higher frequency.

In Section 4.4.2, low internal PD activity (several pC) was detected at 50 Hz. Due to the limited sensitivity of the HF PD setup, internal discharges could not be detected at 25 kHz. Nevertheless, PD activity should be accompanied by space charge and chemical changes to the polymer due to chain scission. Despite being subjected to high levels of electrical field stress during short breakdown and accelerated lifetime tests, the DFR does not exhibit any noticeable changes due to ageing (Figure 4.20). It is possible that the degradation is highly localised due to the short ageing time and thus has no effect on the bulk properties measured with the DFR. It has been shown that the DFR of some plastics is not affected by PD ageing, which may also be the case here [83].

4.7.3. Electrical Treeing

The literature has shown experimentally that the inception and growth of electrical trees under high-frequency voltages with short rise times are much more severe than under, e.g., sinusoidal voltages. Inception is likely to occur within 5 min of voltage application, and the tree growth rate is on the order of 3 to 7 µm/min. The growth rate depends more on rise time than frequency [40]. The resulting time to treeing failure is on the same order of magnitude as the performed lifetime tests.

The following observations further support this hypothesis. The PD measurements show small cavity discharges with occasional glimpses of a pattern similar to electrical treeing. The DFR and IRC measurements do not change even after severe electrical ageing, suggesting that the degradation is not a bulk effect but very localised.

4.8. Recommendations for the Use of IMS PCBs

The test results presented in Chapter 4 indicate that the dielectric strength of the investigated insulating materials is extremely high. Instantaneous breakdown occurs at around 100 to 120 kV_{rms}/mm for 50 Hz AC voltages. For high-frequency voltages, the breakdown strength may decrease by 20 % and the lifetime by several orders of magnitude. Therefore, the following recommendations indicate the limits of the IMS PCBs and can be used to determine the PCB stackup.

If partial discharges are present under high-frequency electrical stress, the lifetime of the dielectric cannot be guaranteed—see Section 4.3 and the IEC 60664-4 standard [23]. Therefore, the voltage is limited by the inception of partial discharges:

– Internal discharges (greater than 1 pC) ignite at field strengths in the range of 25 to 35 kV/mm depending on the dielectric thickness. A safety factor of 1.1 can be taken for the HF PDIV.

– Surface discharges ignite at voltages approx. 30 % higher than the reported repetitive inception voltages, 1.7 to 2.5 kV_{pk}. The repetitive PDIV is used for the following calculations.

A safety factor of 50 % ($F_1 \times F_3 = 1.2 \times 1.25 = 1.5$, see IEC 60664-1 [24]) is taken to ensure that transient overvoltages and variations in PDIV do not lead to accidental ignition of PDs. The maximum nominal voltage that may be used is then shown in Figure 4.25.

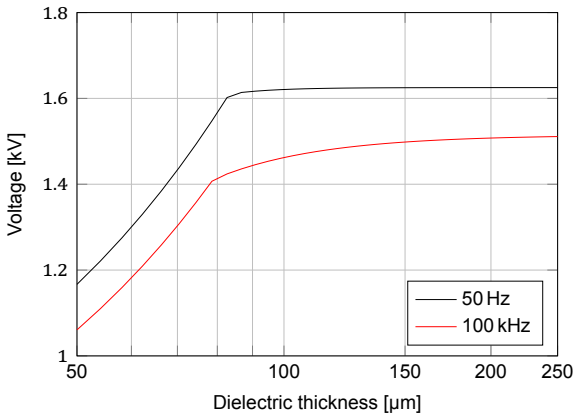


Figure 4.25: Maximum nominal voltage vs dielectric thickness.

4.9. Conclusion

In this chapter, the results of the tests described in Chapter 3 are presented and analysed. Short breakdown and lifetime tests show significant degradation of the insulating properties under high-frequency excitation. Nevertheless, the performance of the Type II dielectric is much better than purely organic Type I materials. Tests with various insulation thicknesses and electrode sizes suggest that there are two competing breakdown mechanisms: (i) breakdown under the electrode is dominant for small electrode sizes at 50 Hz, and (ii) breakdown at the electrode edge is dominant for thicker dielectrics, larger electrode sizes, and high frequency.

Surface discharges occur at voltages much lower than the breakdown voltage and cause significant surface degradation at high frequencies. Analysis of the internal PD patterns shows low-level cavity discharges with superimposed treeing discharges. The presence of electrical treeing is verified by DFR and IRC measurements which show no degradation after high-field electrical ageing, suggesting a highly localised ageing mechanism.

5

Conclusion and Recommendations

This chapter presents the conclusions that may be drawn from this study on high-voltage testing of metal-core printed circuit boards, particularly for power electronic applications. Limitations of the research are indicated, and corresponding recommendations for future work on this subject are formulated.

5.1. Conclusions

In this research project, the effect of high-frequency high-voltage stress on insulated metal substrate PCBs is quantified, resulting in a good insight into the various (high-frequency) effects that can compromise the reliability of the PCB and lead to catastrophic failure of the equipment. Therefore, the objective of this thesis has been met, and the main conclusions are summarised according to the research objectives.

Investigate the insulating materials used in IMS PCBs and their dielectric properties It was shown that the thin insulating layer in IMS PCBs consists of an epoxy resin with various inorganic microfillers, often ceramics, and nanofillers, to improve the thermal and electrical properties.

Microfillers provide the bulk of thermal conductivity and are typically found in high volume fractions. However, the dielectric properties are generally worsened: higher ε_r and $\tan\delta$, lower dielectric strength, and increased shallow trap density and space charge accumulation. On the other hand, nanofillers have a low volume fraction and do not significantly improve thermal performance. Their unique nanostructure provides deep traps that lower the leakage current and improve dielectric strength and partial discharge resistance.

Generate high-frequency test voltages representing power-electronic waveforms The main voltages encountered in the power electronic converters under consideration are pulse-width modulated and DC voltages. In some cases, low- or medium-frequency AC is also found. Three test generators were used to replicate these voltages: (i) a conventional 50 Hz HV test transformer, (ii) a pulse transformer-based square wave generator for 25 to 100 kHz and up to 8 kV peak output voltage, and (iii) a resonant transformer to generate sinusoidal voltages up to 100 kHz and 10 kV. The latter two were designed specifically for this project. High-frequency sinusoidal voltages have proven to be very valuable in evaluating the effect of high frequencies on dielectrics.

Identify and characterise the main (high-voltage) failure modes which may occur on IMS PCBs Dielectric breakdown and surface tracking were identified as the main failure mechanisms on PCBs for high-voltage applications. Under high-frequency excitation, the ageing processes can be accelerated dramatically, leading to a lifetime that is orders of magnitude lower than under 50 Hz AC. Other failures of PCBs may be related to thermo-mechanical stresses, causing delamination or cracking of the insulating layer, solder joints, or components. Further investigation focused on the dielectric breakdown characteristics and mechanisms of filled epoxy under high-frequency voltage stress.

PCB samples were designed to test the dielectric breakdown failure mode, and a test setup was made comprising an electrode arrangement to connect the high voltage and ground to the samples, as well as one of the three high-voltage generators discussed above. Short breakdown and lifetime tests show significant degradation of the insulating properties under high-frequency excitation. Nevertheless, the performance of the Type II insulated metal substrate dielectric is much better than purely organic Type I materials.

Tests with various insulation thicknesses and electrode sizes suggest that there are two competing breakdown mechanisms: (i) breakdown under the electrode is dominant for small PCB electrode sizes at 50 Hz, and (ii) breakdown at the electrode edge is dominant for thicker dielectrics, larger PCB electrode sizes, and high frequency.

The maximum usable voltage is derived in Section 4.8. Assuming no reasonable lifetime can be achieved with high-frequency voltages when partial discharges are present, the nominal operating voltage should be well below the PDIV. Based on this, a maximum voltage of approx 1.5 kV_{pk} is obtained at 100 kHz (see Figure 5.1).

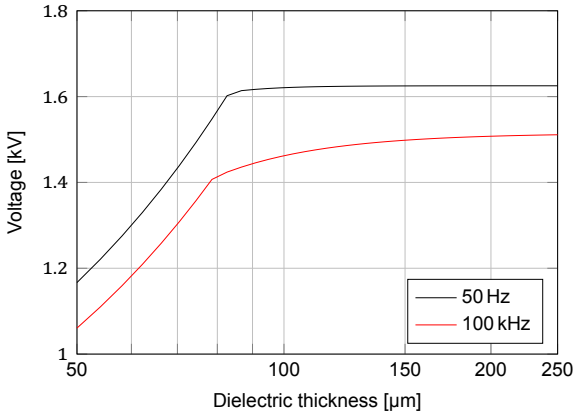


Figure 5.1: Maximum nominal voltage vs dielectric thickness (repeated from Figure 4.25).

Identify the ageing mechanism(s) that occur under high-frequency voltage stress Surface discharges occur at voltages much lower than the breakdown voltage and cause significant surface degradation at high frequencies. Analysis of the internal PD patterns shows low-level cavity discharges with superimposed treeing discharges. Although the high-frequency stress results in significantly increased dielectric losses, the high thermal conductivity of the insulation prevents thermal breakdown. Nevertheless, the increased temperature will exacerbate the partial discharge and electrical treeing activity.

During high-frequency ageing, no change in the bulk dielectric properties was measured using the DFR and IRC techniques, even though an increase in shallow and deep traps was apparent for 50 Hz ageing tests. This indicates a highly localised ageing mechanism.

5.2. Recommendations for Future Work

In the following paragraphs, recommendations for future work are given based on some notable observations and the limitations of the present research. Most importantly, several environmental and process-related influences must still be quantified.

5.2.1. Effect of (Multi-Level) Square-Wave Voltage on Ageing

In this thesis, the dielectric of IMS PCBs has been tested using 50 Hz AC voltage and high-frequency sinusoidal and square-wave voltages. However, the square-wave generator could not perform lifetime tests because of thermal limitations (Section B.1.6). Literature suggests that lifetime tests can be performed with an HF sinusoidal voltage, but this has never been verified experimentally. In the future, it would be valuable to know how the lifetime under square-wave voltage excitation relates to that measured using sinusoidal voltages. With the increased adoption of multi-level converters, the effect of multi-level square waves on the lifetime and PD characteristics should also be verified.

5.2.2. Effect of Soldering Thermal Stress

The tests in this thesis were performed on PCBs as delivered by the manufacturer (and pre-conditioned depending on the test). In reality, the PCB will undergo high thermal stress (up to approx. 260 °C for reflow soldering) once or twice during the soldering process. Since the thermal stress is well above the glass temperature, it may induce some physical changes in the insulation material. Therefore, it is recommended that a (sub)set of the tests in this thesis is repeated after subjecting the PCB to a representative solder temperature profile. Chemical changes may be detected using the DFR or IRC methods presented in Section 3.1.3.

5.2.3. Surface Tracking and Conformal Coating

It was shown in Section 4.4.1 that surface discharges start at relatively low voltages (1.7 to 2.5 kV) due to the high field concentration at the edges of copper planes and traces. This inception voltage was measured for a single copper plane, but more research is required to identify the voltage/electric field limitations in more complex configurations with multiple planes/traces. Since the surface degradation under high-frequency voltage stress is very fast, it is recommended that the partial discharge inception voltage is increased to a safe level (typically some 50 % above the nominal voltage). Two methods which may be used to achieve this are: (i) the application of a conformal coating, and (ii) manufacturing PCBs with a well-defined, thicker solder mask. The effect of trace spacing, voltage frequency, solder mask, and conformal coating on the PDIV and electrical lifetime should be evaluated.

5.2.4. Reliability Demonstration

The lifetime tests in this thesis have been performed for relatively high (voltage) acceleration levels. Although a testing time of more than 80 h was accumulated during the various tests, with a maximum test duration of nearly 2 h, this does not come close to the desired operating lifetime of any actual product. A reliability demonstration must be performed to ensure that the correct conclusions are drawn about the suitability of IMS PCBs in the described applications (see, e.g., [58]). This demonstration can be planned—testing time, number of samples, and acceleration factors—using the lifetime data obtained in this thesis.

5.2.5. PD Measurement

Partial discharge measurements have been performed at 50 Hz AC, and a high-frequency PD measurement setup has been proposed and implemented as part of the resonant test setup. However, the sensitivity of the HF PD measurement was limited to approx. 50 pC because of several issues, which must be addressed to improve the sensitivity and be able to detect internal discharges at high frequency. First, the coupling capacitance (formed by the resonant capacitor) was relatively small. Second, heavy filtering and mismatched protection devices significantly lowered the available bandwidth and reduced the PD current signal. Third, disturbances of similar magnitude as the PD current were present and coupled to the input of the amplifier. A balanced detection circuit could reduce the amount of external interference.

A

Definitions and Abbreviations

A.1. List of Physical Constants

Symbol	Description	Value
ε_0	Permittivity of vacuum	8.854 187 812 8(13) × 10^{-12} F/m
k_B	Boltzmann constant	1.380 649 × 10^{-23} J/K
		8.617 333 262 × 10^{-5} eV/K
q	Elementary charge	1.602 176 634 × 10^{-19} C

A.2. List of Symbols

Symbol	Units	Description
A	[m^2]	Area
B	[T]	Magnetic flux density
C	[F]	Capacitance
d	[m]	(Dielectric) thickness;
E	[V/m]	Electric field
E_a	[eV]	Activation energy
ΔE	[eV]	Trap depth
f	[Hz]	Frequency
f_0	[-]	Initial trap occupancy
$f(\cdot)$	[-]	Probability density function (PDF)
$F(\cdot)$	[-], [%]	Cumulative distribution function (CDF); unreliability
$H_n(\phi)$	[pC]	Discharge count distribution ($\phi - n$)
$H_{qn}(\phi)$	[pC]	Mean discharge height distribution ($\phi - \bar{q}$)
I, i	[A]	Current
i_d	[pA]	Depolarization current
J_θ	[-]	Jacobian versus parameter vector θ
k_ϑ	[W/(m K)]	Thermal conductivity
L	[H]	Inductance
	[h]	Lifetime
L_m	[H]	Magnetizing inductance
L_{11}, L_{21}	[H]	Primary and secondary leakage inductance
$L(x, \theta)$	[-]	Likelihood function with data x and parameter vector θ
$\mathcal{L}$	[-]	Log likelihood
n	[-]	Lifetime power law exponent
$N(E)$	[eV^{-1} m^{-3}]	Trap density distribution
P	[W]	Power
P_d	[W], [W/m^3]	Dielectric loss (density)

Symbol	Units	Description
q	[C]	Charge; PD magnitude
r	[m]	Radius
R	[Ω]	Resistance
$R(\theta)$	[-]	Profile likelihood function w.r.t. θ
t	[s]	Time
t_r	[s]	Rise time
$\tan\delta$	[-]	Dissipation factor
T	[°C], [K]	Temperature
T_g	[°C], [K]	Glass transition temperature
U	[V]	Voltage; Electric potential
Z	[Ω]	Impedance
α	[-]	Confidence level
β	[-]	Weibull shape parameter
ε	[F/m]	Permittivity
ε_r	[-]	Relative permittivity
ζ	[-]	Damping factor
η	[-]	Weibull scale parameter
μ	[-]	Mean
ν	[Hz]	Attempt-to-escape frequency
σ	[S/m]	Conductivity
	[-]	Standard deviation
ω	[rad/s]	Angular frequency

A.3. List of Operators

Symbol	Description
x'	Real part of complex number x
x''	Imaginary part of complex number x
se_X	Standard error of X
$\mathrm{Cov}[X,Y]$	Covariance between X and Y
$\mathrm{Ku}[X]$	Kurtosis of X
$\mathrm{P}[X]$	Probability of X
$\mathrm{Sk}[X]$	Skewness of X
$\mathrm{Var}[X]$	Variance of X
cc	Cross-correlation operator
mcc	Modified cross-correlation operator
Q	Charge asymmetry operator

A.4. List of Abbreviations

Abbreviation	Description
AC	Alternating current
AIC	Akaike information criterion
ALT	Accelerated lifetime test
CDF	Cumulative distribution function
CTE	Coefficient of thermal expansion
DBC	Direct bonded copper substrate
DC	Direct current
DFR	Dielectric frequency response
DUT	Device under test
EDX	Energy dispersive X-ray
ENIG	Electroless nickel immersion gold
ETD	Everhart–Thornley detector
FR4	NEMA grade designation for glass-reinforced epoxy laminate material

Abbreviation	Description
HASL	Hot air solder level
HF	High frequency
HFCT	High-frequency current transformer
HV	High voltage
IGBT	Insulated-gate bipolar transistor
IMS	Insulated metal substrate
IRC	Isothermal relaxation current
LV	Low voltage
MLE	Maximum likelihood estimation
MOSFET	Metal–oxide–semiconductor field-effect transistor
MSE	Mean squared error
PCB	Printed circuit board
PD	Partial discharge
PDF	Probability density function
PDEV	Partial discharge extinction voltage
PDIV	Partial discharge inception voltage
PRPD	Phase-resolved partial discharge
PWM	Pulse-width modulation
RMS	Root mean square
RR	Rank regression
SEM	Scanning electron microscope
SEV	Smallest extreme value distribution
SMD	Surface-mounted device
THT	Through-hole technology
TIM	Thermal interface material
WBG	Wide-bandgap semiconductors
UV	Ultraviolet

B

Pulse Test Setup

The pulse test setup used in this research was built at the TU Delft. The earlier designs are documented by Mathew et al. [63, 64] and Kaparapu [65]. The setup is modified to make it suitable for the tests described in this thesis. Most significantly, the rise time requirements are more stringent to ensure representative test waveforms. The schematic of the setup is repeated in Figure B.1.

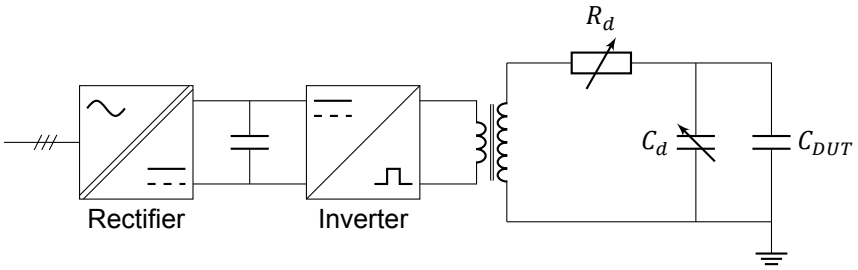


Figure B.1: Schematic test setup for pulse voltage (repeated Figure 3.5).

B.1. Pulse Transformer

The pulse transformer amplifies the low-voltage (0 to 400 V) bipolar square wave generated by the inverter to the desired magnitude for testing (several kV). However, the pulse shape is distorted by parasitic effects in the transformer. The equivalent circuit suggested by the IEEE 390-1987 standard is presented in Figure B.2. This circuit contains the most important parasitic capacitances (C_{11}, C_{12}, and C_{22}), as well as the leakage inductances (L_{11} and L_{22}).

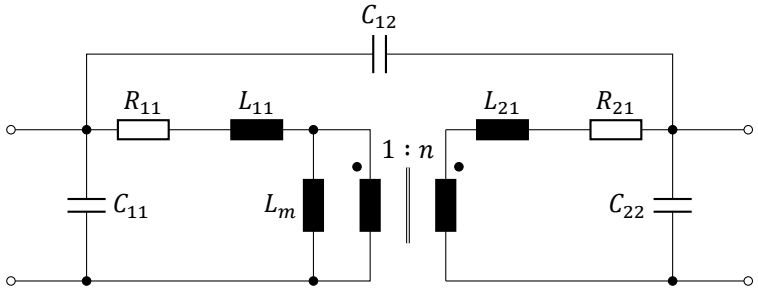


Figure B.2: Equivalent circuit of a pulse transformer (adapted from IEEE 390-1987 [84]).

There are several conflicting requirements for the design of a pulse transformer:

1. The magnetising inductance L_m should be large enough to limit the flux swing ΔB to reasonable levels (i.e., to limit core losses and prevent saturation of the magnetic core) for the worst-case pulse profile. Limiting the output voltage droop is a secondary reason to make L_m large.

2. The turns ratio $n = {}^{N_2}/_{N_1}$ should be large enough to achieve the desired output voltage.

3. The leakage inductances and parasitic capacitances should be as small as possible to prevent distortion of the pulse shape. Most importantly, the voltage rise time should remain representative.

The dynamic behaviour of the pulse transformer driving a capacitive load gives rise to third or fourth-order equations, such as the PQR equation[1] (B.1) derived in [63].

$$\frac{u_o(s)}{u_i(s)} = \frac{nPQ}{s^3 + s^2R + sP + PQ} \tag{B.1a}$$

$$P = \frac{1}{L_\sigma C_\sigma} \qquad Q = \frac{1}{R_d(C_d + C_{DUT})} \qquad R = Q + \frac{1}{R_d C_\sigma} \tag{B.1b}$$

where P, Q, and R represent the transformer parasitics, damping filter response, and their coupling. Such equations are not amenable to calculations by hand but may be used to evaluate the transient behaviour using software packages such as MATLAB. If the parasitic capacitance C_σ is very small, it may be neglected to obtain a second-order equation (B.2).

$$\frac{u_o(s)}{u_i(s)} = \frac{n\omega_0^2}{s^2 + 2\zeta\omega_0 s + \omega_0^2} \tag{B.2a}$$

$$\omega_0 = \frac{1}{\sqrt{L_\sigma(C_d + C_{DUT})}} \qquad \zeta = \frac{R_d}{2}\sqrt{\frac{C_d + C_{DUT}}{L_\sigma}} \tag{B.2b}$$

In Appendix E.2, several observations are made, which will be useful in the following design procedure.

B.1.1. Parameter Extraction from COMSOL

The parameters of the transformers can be extracted from a COMSOL simulation to predict the output pulse waveforms and verify that they meet the requirements. The parameters of interest are the magnetising inductance L_m, leakage inductances L_{11}, L_{21}, and the parasitic capacitances.

(a) Open-circuit test. (b) Short-circuit test.

Figure B.3: Primary-referred equivalent circuits for transformer inductance extraction.

Inductances The inductances can be extracted by open-circuiting (L_m) or short-circuiting (L'_σ, referred to primary) the secondary side of the transformer and measuring the inductance (Figure B.3). In COMSOL, the magnetic field energy can be integrated over the simulation domain.

$$L_m \approx \frac{2}{I_p^2}\iiint_\Omega w_{m,av}\,d\Omega \qquad \text{if } I_s = 0 \tag{B.3}$$

$$L'_\sigma \approx \frac{2}{I_p^2}\iiint_\Omega w_{m,av}\,d\Omega \qquad L''_\sigma = n^2 L'_\sigma \qquad \text{if } U_s = 0 \tag{B.4}$$

where I_p is the primary current, $w_{m,av}$ is the average magnetic energy density (expressed in W/m^3), and Ω is the simulation domain. This approximation is valid only if the leakage is much smaller than the magnetising inductance and the coupling factor k is close to 1.

[1] The original derivation is wrong and the correct result, derived in Appendix E.2, is presented here.

Capacitances Similarly, the capacitances can be obtained by integrating the electric field energy over the domain.

$$C \approx \frac{2}{U^2} \iiint_{\Omega} w_{e,av} d\Omega \tag{B.5}$$

The voltage should be assigned as a linear distribution on the HV winding because this significantly alters the capacitance. In literature, it is found that the capacitance between two winding layers with a linear voltage distribution is 1/3 of C_0, the capacitance when a uniform voltage is applied [85].

$$W_e = \frac{C_0}{2h} \int_0^h U^2(z) dz = \frac{1}{3} \frac{C_0 U^2}{2} = \frac{1}{2} C_{eq} U^2 \implies C_{eq} = \frac{1}{3} C_0 \tag{B.6}$$

where h is the height of the windings and $U(z) = \frac{U}{h} z$.

B.1.2. Parameter Extraction from Measurements

The winding inductances and resistances can be measured as a function of frequency using an LCR meter. The magnetising inductance is measured when the secondary is open-circuited (Figure B.3a), and the primary-referred leakage inductance when it is short-circuited (Figure B.3b).

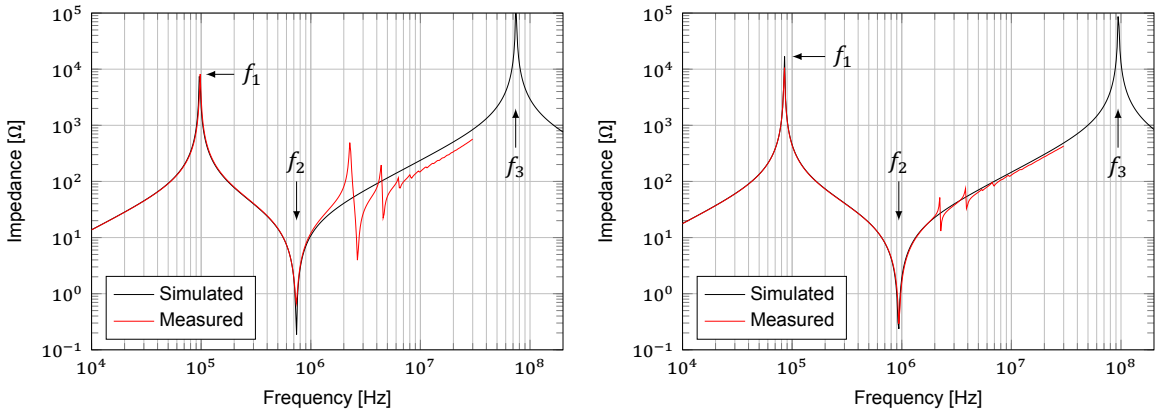
The capacitances cannot be measured with the LCR meter. For C_{12}, measuring this way would yield the geometrical capacitance C_0 instead of C_{eq}. Instead, the primary impedance is measured with a VNA. The resonance frequencies in this spectrum (Figure B.4) can be referred to combinations of components in the equivalent circuit [86].

$$f_1 = \frac{1}{2\pi\sqrt{L_m C'_{22}}} \tag{B.7}$$

$$f_2 = \frac{1}{2\pi\sqrt{L'_\sigma C'_{22}}} \tag{B.8}$$

$$f_3 = \frac{1}{2\pi\sqrt{L'_\sigma C'_{12}}} \tag{B.9}$$

The primary-referred capacitances can be transformed to the equivalent circuit in Figure B.2 using conservation of electrostatic energy, as described in Appendix E.3.



(a) Transformer PT1 (b) Transformer PT2

Figure B.4: Primary impedance spectrum measured with a Bode 100 VNA.

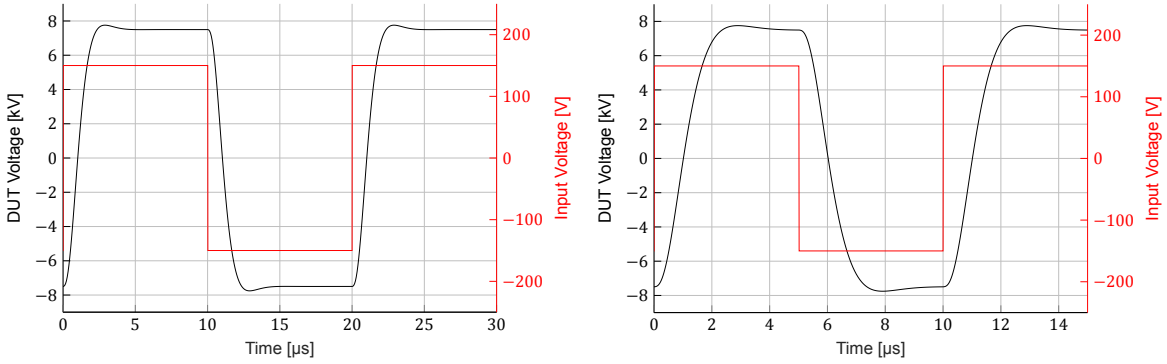
B.1.3. Transformer Parameters

The parameters of the two existing pulse transformers are extracted using the procedure presented above and summarised in Table B.1. The response of the transformer is simulated for the desired testing frequencies to ensure that the pulse is not unacceptably distorted. Ideally, the rise time of the output voltage should be the same as that encountered during regular operation (i.e., in the range 10 to 100 ns).

Table B.1: Pulse transformer parameters.

Param.	PT1	PT2	Note
L_m	217 µH	280 µH	Magnetising inductance
L''_σ	7.3 mH	5.7 mH	Leakage referred to secondary
C_{12}	2.9 pF	3.1 pF	Inter-winding capacitance
C_{22}	2.1 pF	2.0 pF	Secondary winding capacitance
R_{11}	15 mΩ	17 mΩ	Primary winding resistance (DC)
R_{21}	13.8 Ω	44.6 Ω	Secondary winding resistance (DC)

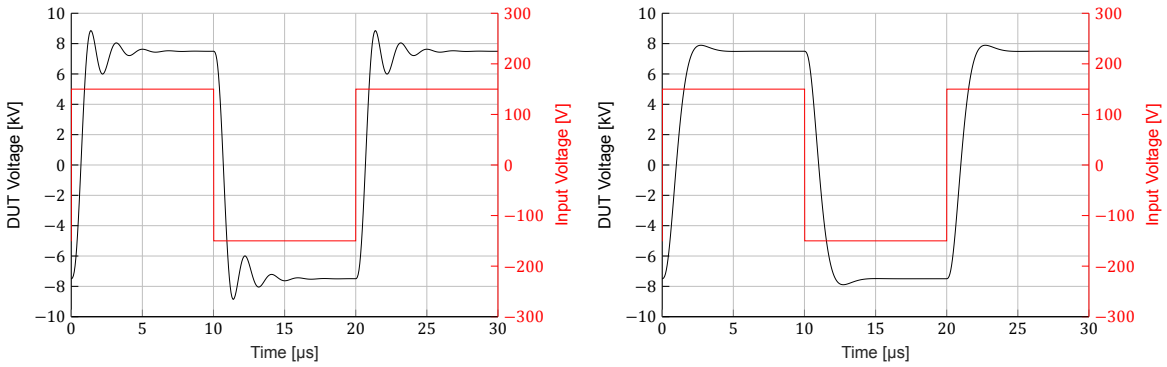
The rise and fall times take up a significant portion of the waveform at increased frequencies. The simulated waveforms shown in Figure B.5 correspond to the worst case DUT load ($C_{DUT} = 68$ pF) with a ±7.5 kV square wave voltage. In this case, a rise time of 1.3 µs is achievable, corresponding to a slew rate of at most 10 V/ns.



(a) At 50 kHz (b) At 100 kHz

Figure B.5: Simulation of pulse transformer output ($C_{DUT} = 68$ pF, $R_d = 15$ kΩ).

With smaller capacitive loads (e.g., $C_{DUT} = 15$ pF), the achievable rise time decreases slightly, but the parasitics of the transformer cause much more oscillation, even with increased damping (see Figure B.6). In this case, a variable capacitance could be added parallel to the DUT to reduce the overshoot at the cost of increasing the rise time again.



(a) Without damping capacitor: $R_d = 45$ kΩ, $C_d = 0$ pF. (b) With damping capacitor: $R_d = 15$ kΩ, $C_d = 50$ pF.

Figure B.6: Simulation of pulse transformer output ($C_{DUT} = 15$ pF, $f = 50$ kHz).

B.1.4. Breakdown Transients

Because the test setup will be used to perform many breakdown tests, it must survive the transients generated by such a breakdown event. While the transformer is the first to receive such transients, the effect on the other components (most importantly, the inverter) should be addressed.

First, the sample represented by C_{DUT} is expected to break down frequently. However, this is not harmful to the other components because of the large damping resistor R_d in series with the sample, which limits the short-circuit current to levels which can be endured for several switching cycles. Second, flashover may occur inside the pulse transformer, which is the leading cause of damage to the power electronics in the previous works. In this case, the damping resistor does not limit the current, and the full short-circuit current may flow for a short time. Mathew [63] reported four failure modes (Table B.2) which can result in damage to the low-voltage system.

Table B.2: Failure modes and mitigations.

Failure Mode		Mitigation
I	Core to LV discharges	Grounding the core; insulation between core and LV winding
II	HV to core discharges	Sufficient clearance; insulation between core and HV winding
III	HV to LV discharges	Sufficient clearance; insulation between HV and LV winding
IV	Core to core discharges	Sufficient conductive contact between the core segments

Additional insulation may be added between the windings and core using (i) HV insulated wire, (ii) Kapton tape, (iii) placing the transformer inside a pressurised gas tank, or (iv) placing the transformer in oil. The latter option will be explored since the analysis of the PQR equation showed that no significant increase in rise time is expected, even if the parasitic capacitance is increased slightly.

B.1.5. Transformer Design Improvements

The transformer design presented above is dimensioned to not saturate under a 10 kHz 200 V bipolar square wave (i.e., generating a ±10 kV output). As a result, the required number of secondary turns is relatively large ($N_p : N_s = 4 : 200$), leading to significant leakage inductance. For the current research, different ratings are required (summarised in Table B.3), resulting in a more favourable transformer design.

Table B.3: Pulse transformer requirements.

Parameter		Value	Note
Primary voltage	U_p	±400 V	Limited by DC supply
Secondary voltage	U_s	±8 kV	
Voltage overshoot	ΔU_s	≤5 %	
Frequency	f_s	25 to 100 kHz	Pulse duration: 10 to 40 µs
Rise time	t_r	≤500 ns	5 % at 100 kHz

Dimensioning The flux density swing ΔB is calculated from the volt-seconds $U_p \cdot t_{on}$ applied to the magnetising inductance. Because a DC offset is not allowed, the duty cycle must be 50 %, yielding the expression in (B.10), where N_p is the number of primary turns and A is the magnetic core area.

$$\Delta B = \frac{U_p t_{on}}{N_p A} = \frac{U_p}{2 N_p A f_s} \tag{B.10}$$

To ensure that the core does not saturate, a condition $\Delta B \leq 2B_{max}$ should be imposed, where B_{max} is the maximum allowable flux density. Usually, B_{max} is chosen slightly below the worst-case saturation level. The minimum number of turns to impose this condition is calculated using (B.11).

$$N_p \geq \frac{U_p}{4 B_{max} A f_s} \tag{B.11}$$

Two cores are available for this transformer design: (i) UU core based on N87 MnZn ferrite, and (ii) AMCC1000 core based on MetGlas 2605SA1 amorphous iron. The properties of these materials are summarised in Table B.4.

Table B.4: Magnetic core material properties.

Property	N87 MnZn	MetGlas 2605SA1
B_{sat}	0.5 T	1.56 T
H_c	20 A/m	15 A/m
μ_r	2200	≥10 000
ρ	10 Ω m	1.3 µΩ m

The transformer is not expected to run very hot, so no derating of the saturation flux level is required. Hence, for the ferrite core $B_{max} = 400$ mT and for the amorphous core $B_{max} = 1.0$ T. The increased B_{sat} of the amorphous core allows for a reduction in the number of turns. However, because a cut core is used, the effective $\mu_r \approx 1500$ is more in the range of ferrite materials. There is a minimum number of turns to keep the magnetising inductance at an acceptable level.

Leakage Inductance Minimisation To reduce the rise and fall times to the desired level, the leakage inductance of the transformer must be reduced. The parasitic inter- and intra-winding capacitances could also be reduced, but these have a much smaller effect than the inductance. Reducing the leakage inductance can be achieved by:

- Reducing the number of turns N, since the leakage inductance scales with N^2. However, a minimum number is required to prevent saturation of the transformer core. If the magnetising inductance is too low, it may lead to droop of the output voltage.
- Reducing the turns ratio n, since L_{11} referred to the secondary side scales with n^2.
- Reducing the volume enclosed between the primary and secondary winding (e.g., by reducing the distance between them). Most of the leakage energy is contained in this volume. However, bringing the windings closer together increases C_{12}.
- Making the windings the same height. This is not always possible because the electric field between the primary and secondary will increase, resulting in a higher risk of breakdown.

For example, a bifilar winding results in very low leakage. However, because this is a high-voltage application, a certain level of insulation is required between the primary and secondary windings. This insulation can be realised using an insulating medium or by keeping sufficient distance between the windings. In the following sections, insulation using air and transformer oil is investigated. Oil is a much better insulating medium than air. However, it is also challenging to work with and would significantly increase the parasitic capacitance of the transformer (by a factor $\varepsilon_r \approx 2.4$).

B.1.6. New Transformer Design

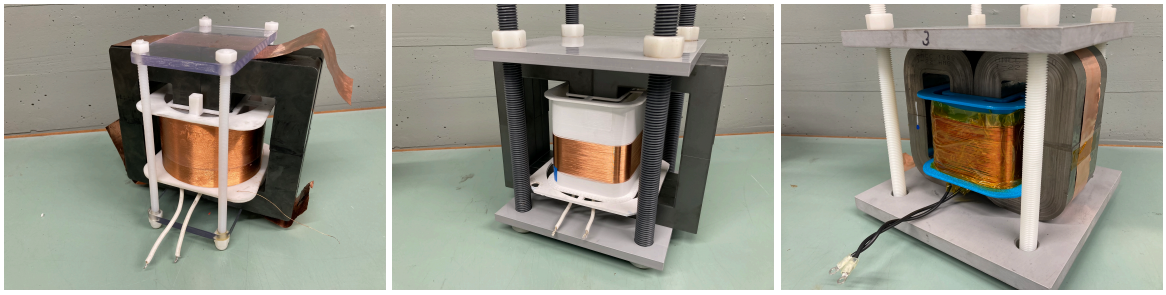
Besides flashover between the primary and secondary winding, flashover may occur between the secondary and the (grounded) core. Because of potential field enhancement at the top of the HV winding, it is preferable to keep the HV winding in the middle of the core window. With this much distance, the primary height can be increased to 100 %. The increased distance also reduces the interwinding capacitance (C_{12}).

Three new designs are made and simulated to evaluate the performance of different winding and core configurations. Lowering the turns ratio brings a considerable improvement since the leakage scales with n^2. Amorphous cores (AMCC1000) are necessary to prevent saturation with the corresponding increased primary voltage. The new designs are compared against the previous designs by Mathew and Kaparapu in Table B.5. Observe that the rise time is approximately proportional to the square root of the leakage inductance, as expected based on the theoretical equations (B.1) and (B.2).

Table B.5: Simulated rise times for transformer configurations (C_{DUT} = 68 pF and ζ = 0.9).

	Core	Turns	U_p	$L_{\sigma 2}$	t_r	Note
PT1	4× UU 93/152/30 (N87)	4 : 200	230 V	6.5 mH	1815 ns	[63]
PT2	8× UU 126/182/20 (N87)	4 : 200	200 V	5.3 mH	1380 ns	[65]
	8× UU 126/182/20 (N87)	2 : 100	200 V	1.3 mH	675 ns	
PT3	2× AMCC1000	3 : 60	400 V	340 µH	345 ns	
	4× AMCC1000	2 : 40	400 V	220 µH	250 ns	

Realization Pulse transformer 3 (PT3) was realised using a 3D-printed bobbin to hold the secondary winding. The primary consists of 3 turns of 6.5 cm high foil winding. The secondary comprises 60 turns of 1 mm enamelled copper wire, distributed over approx. 6.5 cm of the bobbin.



(a) Transformer PT1 [63] (b) Transformer PT2 [65] (c) Transformer PT3

Figure B.7: Photographs of the realised pulse transformers.

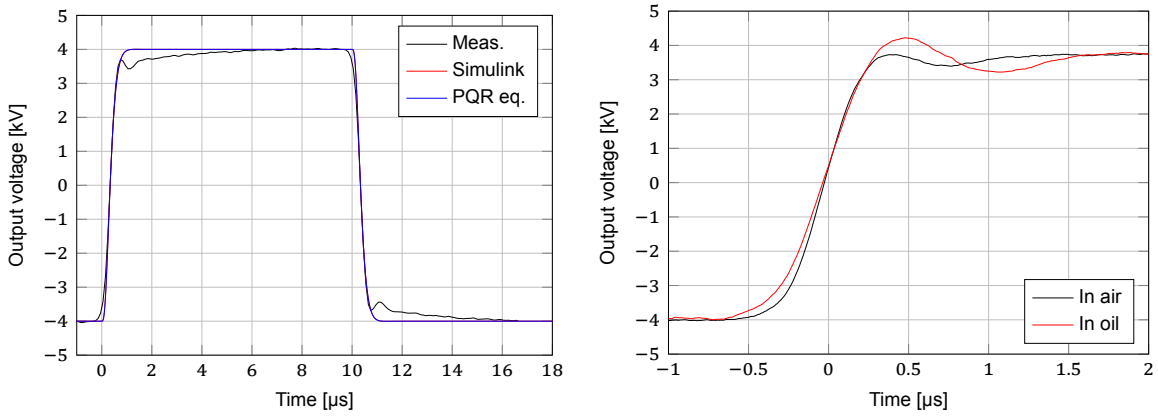
Parameter Extraction The extracted transformer parameters are presented in Table B.6. The measured parameters match well with those obtained by simulation and analytical calculation. The leakage inductance is significantly larger than predicted because the primary winding leads were not considered in the COMSOL model (approx. 20 cm accounting for the increase of $\ell\mu_0 n^2 \approx 100$ µH).

Table B.6: Parameters extracted from PT3.

Parameter	Modelled	Measured
L_m	185 µH	200 µH
$L_{\sigma 2}$	340 µH	440 µH
C_{12}	5.1 pF	5.8 pF
C_{22}	1.4 pF	1.7 pF
R_{11}	5.5 mΩ	8.4 mΩ
R_{21}	0.56 Ω	0.6 Ω

Pulse Waveforms The transformer is supplied with a ±200 V bipolar square wave on the primary winding. The resulting output voltage is measured and compared against the simulated pulse response in Figure B.8a for $f_s = 50$ kHz, $C_{DUT} = 68\,\mathrm{pF}$ and $R_d = 4.6\,\mathrm{k\Omega}$. The predicted rise time (460 ns) matches well with the measured 480 ns. However, the measured pulse shape exhibits some undershoot, which was not predicted by the PQR equation or Simulink model. This deviation is because the input waveform is not perfectly square: it has some low-frequency oscillation on the DC link.

High-Voltage Withstand Test Because a flashover inside the transformer could destroy the low-voltage power electronics, a 50 Hz withstand test is performed to evaluate the maximum voltage to which the transformer can be used. The secondary winding is replaced by copper tape. This is only partially representative since the secondary winding should have a linear voltage distribution, but it



(a) Comparison of pulse response simulations and measurements with $f_s = 50\,\mathrm{kHz}$, $C_{DUT} = 68\,\mathrm{pF}$ and $R_d = 4.6\,\mathrm{k\Omega}$.

(b) Pulse response comparison with and without transformer oil.

Figure B.8: Output voltage waveforms of PT3 with ±200 V square-wave primary voltage.

indicates the worst case. For diagnostics, the CoroCAM was used to measure partial discharge activity optically. The measured partial discharge inception voltages (PDIV) and flashover voltages are recorded in Table B.7.

Table B.7: Results of high-voltage withstand test.

	Test voltage	PDIV U_i	Flashover U_f	Location
PT1	50 Hz AC	10 kV_{rms}	11 kV_{rms}	HV to core
PT2	50 Hz AC	9 kV_{rms}	16 kV_{rms}	HV to core
PT3	50 Hz AC	11 kV_{rms}	14 kV_{rms}	HV to core
	50 kHz sq. wave	7.5 kV_p	–	

For PT3, the PDIV at 50 kHz was measured to be around 7.5 kV_{pk} on the HV winding. The PDIV is reduced by more than 50 % under high-frequency square wave excitation. This is similar to Agarwal et al., who show that the PDIV is decreased by 30 % in the frequency range 10 to 50 kHz compared to 50 Hz [56].

Thermal Performance The ferrite transformers (PT1, PT2) have a core loss of several tens of watts. Given the large size of the transformer, this power can be dissipated effectively to the environment with a negligible temperature rise. On the other hand, the amorphous transformer (PT3) heats up significantly, as shown in Figure B.9.

As expected, most of the temperature rise is concentrated around the cut. Two potential explanations are (i) the high conductivity of the area around the cut, and (ii) the orthogonal flux due to misalignment between the core halves. An improved cooling solution is required to perform insulation tests for an extended time. Short-term tests do not cause a noticeable increase in core temperature because of the large thermal mass of the transformer.

B.1.7. Submersion in Oil

The transformer is completely submerged in transformer oil for two reasons: First, the measurements presented in the previous section give little confidence in reaching the desired output voltage (±8 kV) without flashover occurring. Second, the oil provides better cooling than air and acts as a thermal buffer. The PQR equation analysis predicts this will lead to a slight reduction in rise time, verified through the measurements in Table B.8. However, the damping must be increased to achieve an acceptable overshoot. The pulse response is shown in Figure B.8b.

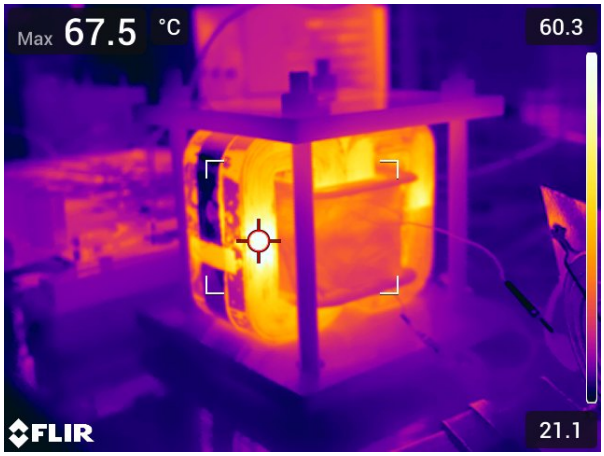


Figure B.9: Thermal image of pulse transformer 3 using an amorphous cut core at f_s = 50 kHz, U_p = 200 V, and U_{DUT} = 4 kV_{pk}. Estimated core losses P_c = 280 W. The region around the cut is approx. 30 °C hotter than the rest of the core.

Table B.8: Rise time and overshoot of PT3 ($C_{DUT} = 68\,pF$).

	In air	In oil	In oil
R_d	4.6 kΩ	4.6 kΩ	5.1 kΩ
Rise time	480 ns	420 ns	520 ns
Overshoot	0.5 %	12.7 %	4.8 %

B.2. DC Voltage Source

In the previous works [63, 65], a variac and full-bridge rectifier were used to generate a variable DC bus voltage, which was then fed to the inverter. As a result of this choice, very large filter capacitors were necessary to reduce the 100 Hz ripple. Additionally, the output voltage cannot be regulated well, especially when ramps on the order of 500 V/s have to be generated.

For this setup, therefore, a programmable DC voltage source is used. Ramps or constant voltages can be generated either on the front panel or remotely via a GPIB/RS232 port. This particular source is limited to 400 V and 25 A.

B.3. Inverter

The inverter is implemented using a full-bridge configuration. It converts the DC bus voltage into pulses with a variable frequency (25 to 100 kHz) and duty cycle. Three-level waveforms may also be obtained using the phase shift between the legs. The entire low-voltage system utilises a split bus arrangement, meaning that the DC bus is symmetric around earth with $\pm U_{dc}/2$.

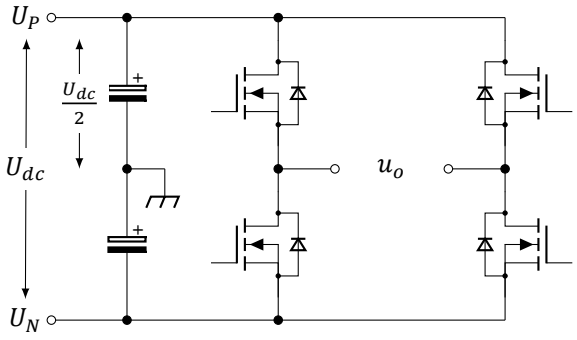


Figure B.10: Full-bridge inverter schematic.

C

Resonant Test Setup

The resonant setup for high-frequency sinusoidal voltage used in this research was built at the TU Delft. The earlier design was documented by Patil [87]. The setup is further developed to make it suitable for the tests described in this thesis. The usable frequency range is extended, and a PD measurement system is added. The setup schematic is repeated in Figure C.1.

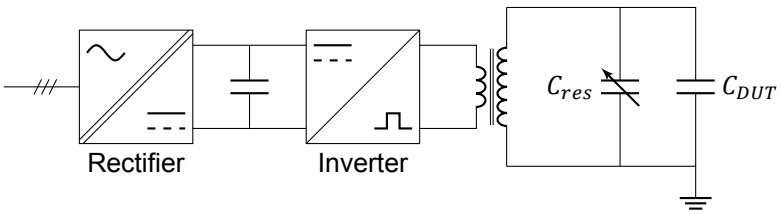
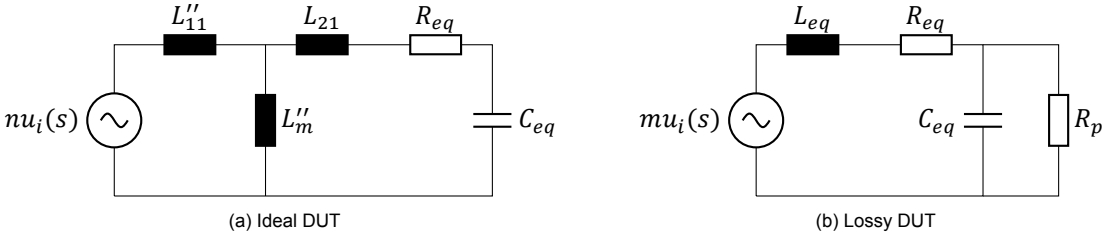


Figure C.1: Schematic test setup for sinusoidal voltage (repeated Figure 3.6).

The design of three transformers for 25, 50, and 100 kHz (named RT1, RT2, and RT3, respectively) is described in detail. Further variations necessary to obtain the desired resonance frequency with samples E and F follow the same design procedure.

C.1. Analysis

Replacing the transformer with its equivalent circuit and assuming an ideal (lossless) capacitive load, the circuit in Figure C.2a is obtained. The conditions for resonance can be derived from this circuit.



(a) Ideal DUT (b) Lossy DUT

Figure C.2: Equivalent circuit of resonant setup.

The parameters are defined as $L_{eq} = L_{21} + L''_m \parallel L''_{11}$, $C_{eq} = C_{DUT} + C_{res} + C_\sigma$, and $R_{eq} = R''_{11} + R_{21}$. Parameter m accounts for the gain reduction due to the voltage drop over the primary leakage inductance. The response u_o of the test setup due to an excitation u_i can be modelled using the second-order transfer function (C.1).

$$\frac{u_o(s)}{u_i(s)} = \frac{m\omega_0^2}{s^2 + 2\zeta\omega_0 + \omega_0^2} \tag{C.1}$$

where

$$\omega_0 = \frac{1}{\sqrt{L_{eq}C_{eq}}} \qquad \text{and} \qquad \zeta = \frac{R_{eq}}{2\omega_0 L_{eq}} = \frac{R_{eq}}{2}\sqrt{\frac{C_{eq}}{L_{eq}}} \tag{C.2}$$

The resonance frequency ω_r and ideal resonant gain G^* can be derived from these.

$$\omega_r = \omega_0\sqrt{1-\zeta^2} = \sqrt{\omega_0^2 - \frac{R_{eq}^2}{2L_{eq}^2}} \qquad G^* = \left|\frac{m}{\zeta^2 + 2j\zeta\sqrt{1-\zeta^2}}\right| \approx \frac{m}{2\zeta} \tag{C.3}$$

Lossy DUT In reality, the DUT is not perfectly capacitive, and an additional loss component must be considered. The origin of this loss can be dielectric loss ($\tan\delta$), partial discharges, or conductivity of the dielectric. The loss is modelled with an additional resistance R_p in parallel with the DUT capacitance (see Figure C.2b).

$$\frac{u_o(s)}{u_i(s)} = \frac{m\omega_0^2}{s^2 + s\left(\frac{R_{eq}}{L_{eq}} + \frac{1}{R_p C_{eq}}\right) + \omega_0^2\left(\frac{R_{eq}}{R_p} + 1\right)} \tag{C.4}$$

With increasing loss (i.e., decreasing R_p), the damping of the circuit is increased. The resonance frequency will also shift significantly for very low values of R_p (on the order of R_{eq}).

In the most general case, R_p will be a function of frequency, voltage, temperature, and other environmental influences. To accurately predict the output voltage of the test system, it is critical that R_p can be modelled to represent the relevant phenomena.

Dielectric Loss The dielectric loss of the sample is a function of frequency (and sometimes temperature) and can be represented by the parallel resistor R_p. Using the definition of $\tan\delta$, the equivalent R_p is given by (C.5).

$$R_p(\omega) = \frac{1}{\omega C_{eq}\tan\delta(\omega)} \tag{C.5}$$

C.2. Resonant Transformer

The resonant transformer must be adequately designed to achieve resonance at the desired frequency and generate a high output voltage. Although f_r is adjustable in a particular range by using C_{res}, the inductance L_{eq} (dominated by $L_{\sigma 2}$) must be in the correct order of magnitude. Similarly, excessive AC resistance will lead to damping and hence reduced output voltage.

In the following sections, analytical methods will be presented to calculate the parasitics of the transformer, which will aid in making a proper design. Of course, it is also possible to perform these calculations numerically, as shown in Appendix B.

C.2.1. Leakage Inductance Estimation

To obtain the desired resonance frequency, it is critical to design the leakage inductance of the transformer properly. Therefore, the leakage inductance must be estimated analytically or numerically (e.g., using COMSOL). For concentric windings, the leakage inductance can be estimated quite accurately using (C.6), as suggested by Lambert et al. [88].

$$L_{\sigma 2} = \mu_0 N_2^2\left[\frac{\ell_{m1}d_1}{3h_1} + \frac{\ell_{m2}d_2}{3h_2} + \frac{\ell_{mg}d_g}{h_g}\right] \tag{C.6}$$

where d_1, d_2 are the thicknesses of the windings, d_g is the dimension of the gap, h_1, h_2 are the heights of the windings, $h_g = (h_1 + h_2)/2$ is the effective gap height, and ℓ_{m1}, ℓ_{m2}, and ℓ_{mg} are the mean lengths of the windings and the gap. Fringing effects at the ends of the windings can be accounted for using an effective (reduced) winding height using the Rogowski factor (C.7).

$$K_R = 1 - (d_1 + d_2 + d_g)\frac{1 - \exp\left(-\frac{\pi h}{d_1+d_2+d_g}\right)}{\pi h} \tag{C.7}$$

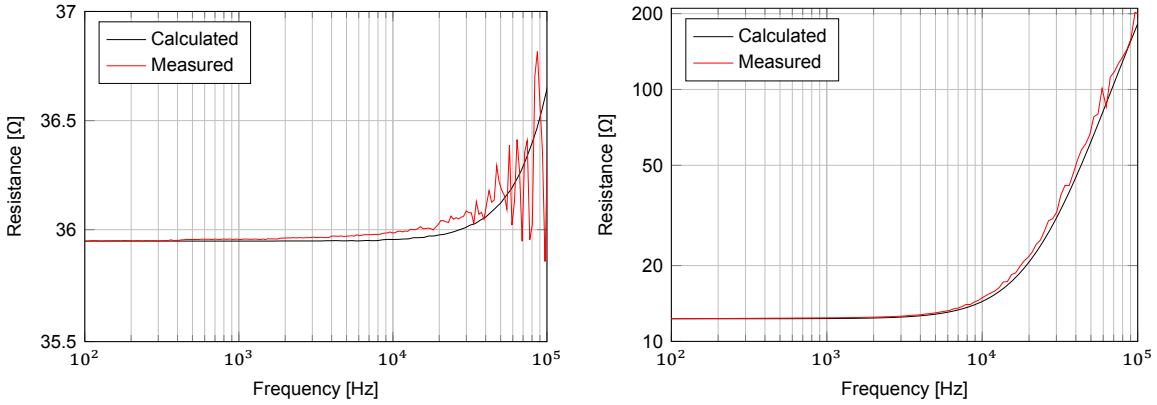
Placing the windings on different legs (e.g., of a UU or UI core) drastically increases the leakage inductance, as shown experimentally by Mathew [63]. No good analytical models are available for this configuration.

C.2.2. AC Resistance Estimation

Since the desired operating frequencies are in the range of 25 to 100 kHz, the skin and proximity effect should be taken into account to determine the gain of the system. The AC resistance can be estimated using the procedure presented by Biela [89, pp. 235-240].

$$R_{AC}(f) = 2R_{DC}\left[F_R(f) + G_R(f)\frac{N^2}{M^2}\frac{4M^2-1}{12b_F^2}\right] \tag{C.8}$$

where $F_R(f)$ and $G_R(f)$ represent the skin and proximity effect, N/M is the number of turns per layer, M is the number of layers, and b_F is the winding height. The DC resistance R_{DC} is calculated from the winding geometry.



(a) Winding with $N = 300$, $M = 1$, and $d = 0.2$ mm.

(b) Winding with $N = 600$, $M \approx 15$ and $d = 0.5$ mm.

Figure C.3: AC resistance calculation and measurement (with Bode 100 VNA).

The AC resistance of RT1 (multi-layer winding) and RT2 (single-layer winding) are calculated using the equation above and compared to the measurement in Figure C.3. While measuring with an impedance analyser or VNA, it is important to keep the winding away from any magnetic materials since these may influence the magnetic field and hence the R_{AC}.

C.2.3. Parasitic Capacitance Estimation

The transformer's leakage inductance and parasitic capacitance determine its self-resonance frequency, and it cannot be used to generate frequencies higher than this. However, considering the need for sufficient insulation and distance between the windings, for most practical winding configurations, the parasitic capacitance will be much less than the DUT capacitance. Therefore, accurately estimating the parasitic capacitances is not that interesting.

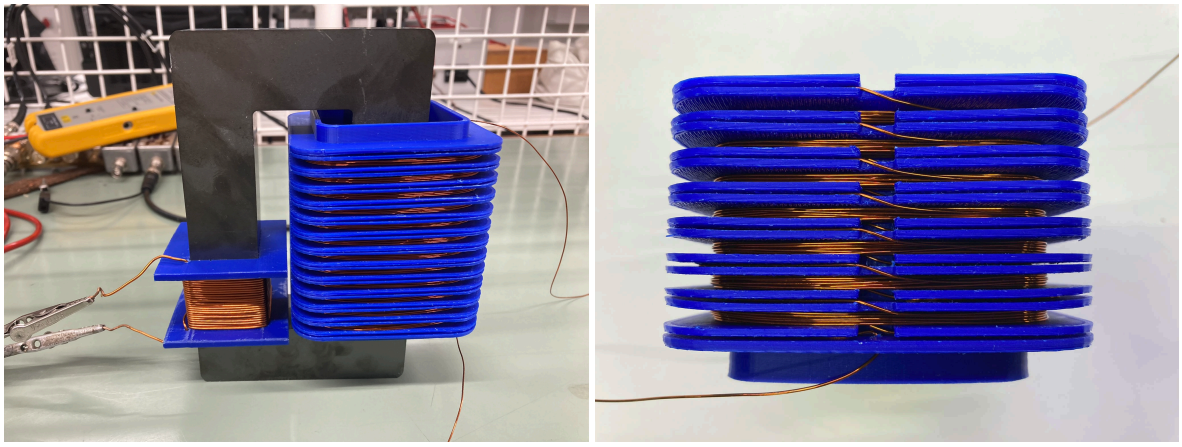
The parasitic capacitance comprises two dominant components: the secondary intra-winding capacitance C_{22} and the inter-winding capacitance C_{12}. As noted before, because of the distance between the windings, C_{12} will be small (on the order of several pF). The capacitance C_{22} depends on the secondary winding configuration but reduces with an increasing number of turns. It can be further limited by separating the windings into several segments with some distance between them (see, e.g., Figure C.4).

C.2.4. Secondary Winding Design

Apart from obtaining the desired component values, several high-voltage aspects must also be considered. Like before, flashover may occur between the high- and low-voltage windings and the magnetic core.

The primary and secondary windings are already wound on separate legs to achieve a high leakage inductance and low parasitic capacitance. Therefore, the two remaining dangers are (i) flashover

between the HV winding and the core, and (ii) flashover between turns of the HV winding. The bobbin design employed in the designed resonant transformers (see Figure C.4) aims to reduce both risks.



(a) Photograph of RT1.

(b) Detailed view of the secondary bobbin.

Figure C.4: Photographs showing the split winding configuration and bobbin designs.

C.2.5. Measurement

In this section, several measurements are presented that show the design procedure and functionality of the resonant transformer. The transformer parameters are extracted using VNA measurements, and the output voltage of the circuit is measured under various conditions.

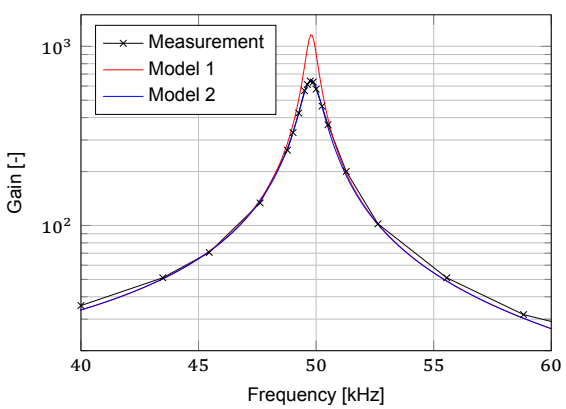
Parameter Extraction The equivalent circuit parameters of the designed transformers are extracted according to the procedure presented in Section B.1.6. The winding resistances are measured at the transformer's operating frequency.

Table C.1: Extracted transformer parameters

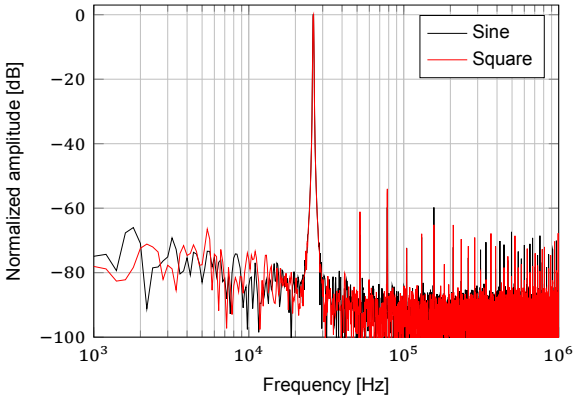
	RT1 (25 kHz)		RT2 (50 kHz)		RT3 (100 kHz)	
	Calc.	Meas.	Calc.	Meas.	Calc.	Meas.
L_m	4.4 mH	3.3 mH	4.1 mH	3.7 mH	4.4 mH	3.8 mH
$L_{\sigma 2}$		133.8 mH		31.0 mH		16.6 mH
C_{12}		1.9 pF		1.4 pF		
C_{22}		3.9 pF		3.4 pF		
R_{11}	0.14 Ω	0.11 Ω	0.18 Ω	0.16 Ω	0.27 Ω	0.27 Ω
R_{21}	25.3 Ω	27.3 Ω	36.1 Ω	36.2 Ω	25.0 Ω	24.9 Ω

Transfer Function and Output Spectrum The response of the transformers is measured by exciting the primary with a small square wave voltage and measuring the peak output voltage of the transformer. The gain is calculated from the output voltage and the fundamental component of the input voltage. The measured resonance peak is compared to the models presented in the previous section in Figure C.5a. Observe that the resonant gain is only predicted correctly when the sample's dielectric loss is considered.

One of the main drawbacks of ferrite-based resonant transformers cited in the literature is the nonlinearity of the magnetic core, which may introduce harmonics in the output spectrum. If the transformer is operated far below saturation (current designs operate below 10 mT, while $B_{sat} \approx 400$ mT), this is not the case. The frequency spectrum of the output voltage of RT1 is measured for sinusoidal and square-wave primary excitation to demonstrate this (Figure C.5b). For both, the total harmonic distortion is around 0.2 %.



(a) Transfer function of RT2 (C_{DUT} = 90 pF, $\tan\delta = 300 \times 10^{-4}$ @ 50 kHz and an additional C_{res} = 200 pF with no dielectric loss).



(b) Frequency spectrum of RT1 output voltage.

Figure C.5: Measurements demonstrating the proper functioning of the resonant circuit.

Effect of Lossy Capacitors The resonant capacitor should be sufficiently stable over temperature, frequency, and voltage to ensure good output voltage stability. In Figure C.6, three measurements are shown, which use a variable air capacitor with and without an additional external ceramic capacitor C_{ext}. When a ceramic capacitor is included, the output voltage drifts due to varying losses inside this additional capacitor.

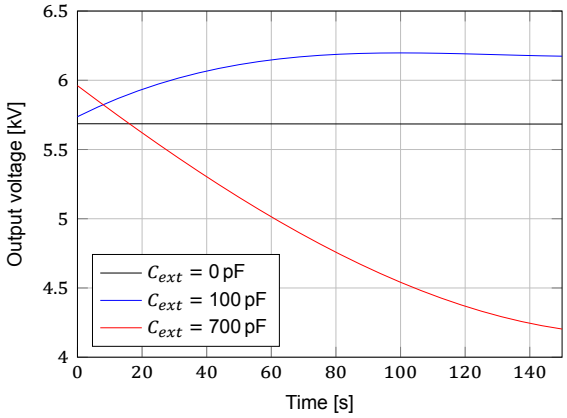


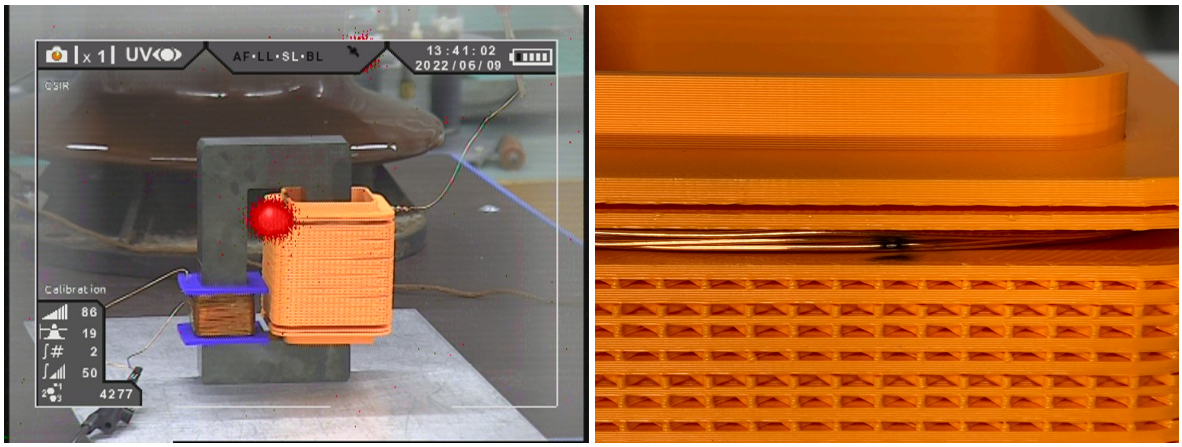
Figure C.6: Output voltage drift due to lossy ceramic capacitors in the resonant circuit.

High-Voltage Withstand Test To ensure that no flashover occurs from the high-voltage to the low-voltage side, similar precautions are taken as in Appendix B. The magnetic core is grounded, and the secondary winding design should prevent partial discharges at low voltage. The PDIV and flashover voltage are measured to verify that the transformer can reach the desired output voltage.

Table C.2: Discharge Inception and Flashover Voltages

	Test frequency	PDIV U_i	Flashover U_f	Location
RT1	50 Hz	11 kV_{rms}	17 kV_{rms}	HV to core
	25 kHz	6 kV_{pk}	–	
RT1 (oil)	50 Hz	–	>40 kV_{rms}	
	25 kHz	19 kV_{pk}	–	

Photographs of the partial discharge activity and flashover location are shown in Figure C.7. Flashover occurred at 17 kV_{rms} from the top of the high-voltage winding to the inside of the core window.



(a) CoroCAM photograph showing discharges at the top of the high-voltage winding at 15 kV_{rms}, 50 Hz

(b) Flashover from the high-voltage winding to the inside of the core window.

Figure C.7: Photographs of the withstand test results.

Submerging the transformer in oil increases the flashover voltage beyond the 40 kV_{rms} that can be generated and measured. This is not strictly necessary for the tests in this thesis but demonstrates the wide range of applications in which the designed resonant transformer can be used. Under oil at high frequency, discharges start at roughly 15 kV_{pk} (or about 1.2 kV per segment). Since the segments are wound randomly, these discharges are hypothesised to occur between neighbouring turns.

C.3. PD Measurement

PD measurement can be directly integrated with the resonant setup since a coupling capacitor can be added in parallel to the DUT without any decrease in performance. Doing this in the pulse setup would be challenging since the load capacitance significantly affects the achievable rise time and overshoot.

The measurement system is shown schematically in Figure C.8. To eliminate the interference caused by the switching and auxiliary circuits of the inverter, a function generator and linear amplifier were used to provide the low-voltage excitation u_i.

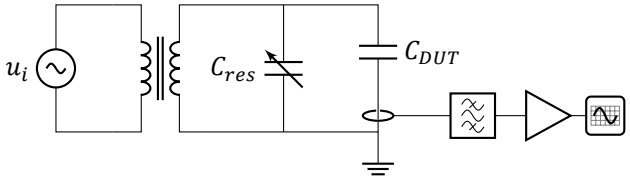


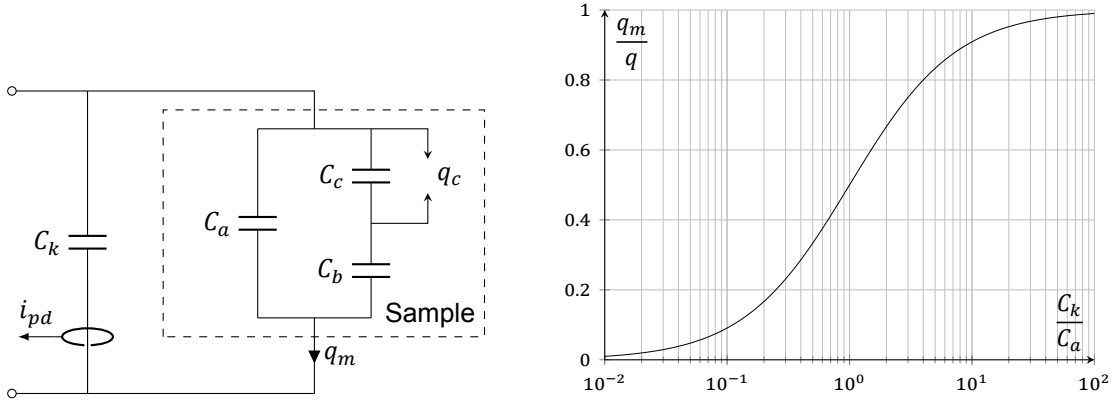
Figure C.8: Resonant setup with PD measurement.

C.3.1. Coupling Capacitor

Using the simple abc-model shown in Figure C.9a, it can be calculated that the measured charge q_m (i.e., the charge flowing through the measuring device, also called “apparent” charge) depends on the capacitor ratio c_k/c_a. q is the charge that would be displaced internally if no C_k is present.

$$\frac{q_m}{q} = \frac{C_k}{C_a + C_k} = \frac{c_k/c_a}{1 + c_k/c_a} \tag{C.9}$$

For 50 Hz PD tests, C_k is usually chosen such that $C_k \gg C_a$ to obtain a high PD signal amplitude. While this is also true for high-frequency PD tests, other factors must be taken into account: increasing the load capacitance results in (i) higher resonant current, (ii) reduced resonance frequency, and (iii) increased losses in the coupling capacitor [90]. The latter can lead to an unstable output voltage of the resonant setup since the losses and capacitance are typically temperature-dependent.



(a) abc-model (b) Measured charge vs capacitor ratio [55].

Figure C.9: Role of the coupling capacitor in PD measurements.

Therefore, a trade-off must be made between the signal-to-noise ratio and the effect of C_k on the performance of the test setup. The measured charge is shown as a function of the capacitor ratio C_k/C_a in Figure C.9b.

C.3.2. PD Current Measurement

The discharge current can be measured using a measuring impedance (a combination of a current sensing resistance and filtering elements) or a high-frequency current transformer (HFCT). These current sensing elements may be placed in series with the coupling capacitor or the sample. The PD magnitude can be calculated by integrating the measured current over time.

$$q_m = \int i_{pd}(t)dt \tag{C.10}$$

This thesis uses an HFCT consisting of an N30 ferrite core with five secondary turns (as described by Mor et al. [91]). This HFCT has a bandwidth of 35 kHz–60 MHz. The transformer should be terminated into 50 Ω, either in an oscilloscope, burden resistor, or amplifier with 50 Ω input impedance.

C.3.3. Post-Processing

The current pulses measured with the HFCT are filtered with a 1.5 to 90 MHz band-pass filter. The low-frequency cutoff needs to be relatively high to reject the capacitive current (up to 100 kHz) that results from the HF sinusoidal excitation. A 30.5 dB amplifier increases the range of detectable discharges. The amplified current pulses are recorded with a PicoScope and a ramp voltage for synchronisation (modification of the system in [91]). The pulses are post-processed in the PDflex software.

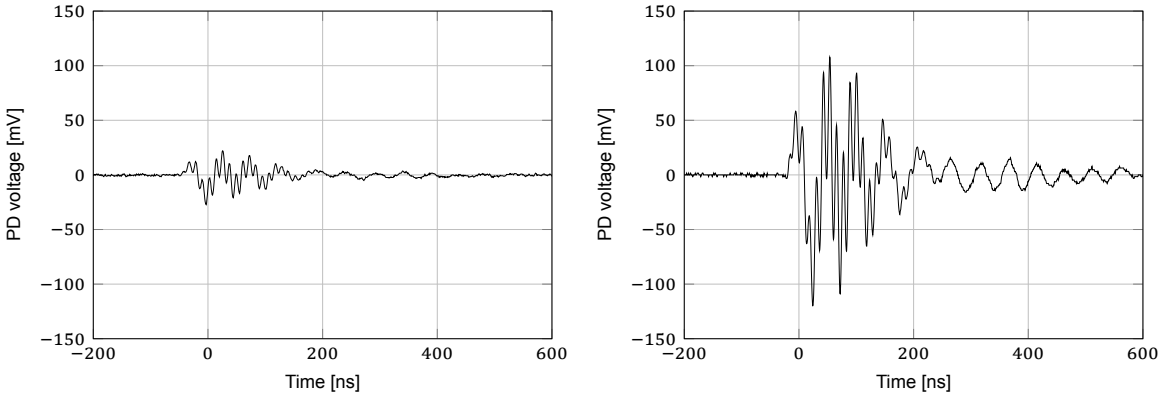
C.3.4. PD Measurements

In this section, several examples of PD measurements are shown. These results show that the setup can properly detect PD at high frequency but highlight several drawbacks.

Calibrator Figure C.10 shows the response of the detection circuit to calibration pulses of 50 and 200 pC. Even though a unipolar calibration pulse is applied, the response measured on the oscilloscope shows significant oscillation because of the inductance in the circuit and the band-pass filter.

Negative Corona Negative corona in the Trichel pulse regime is also often used for calibration because of its well-defined characteristics. At 50 Hz, the Trichel pulses have a constant amplitude (apparent charge) which depends on the needle geometry. The repetition rate depends on the applied voltage, typically of the form

$$f(U) = k(U - U_0)^2 \quad \text{or} \quad f(U) = kU(U - U_0) \quad \text{for} \quad U > U_0, \tag{C.11}$$

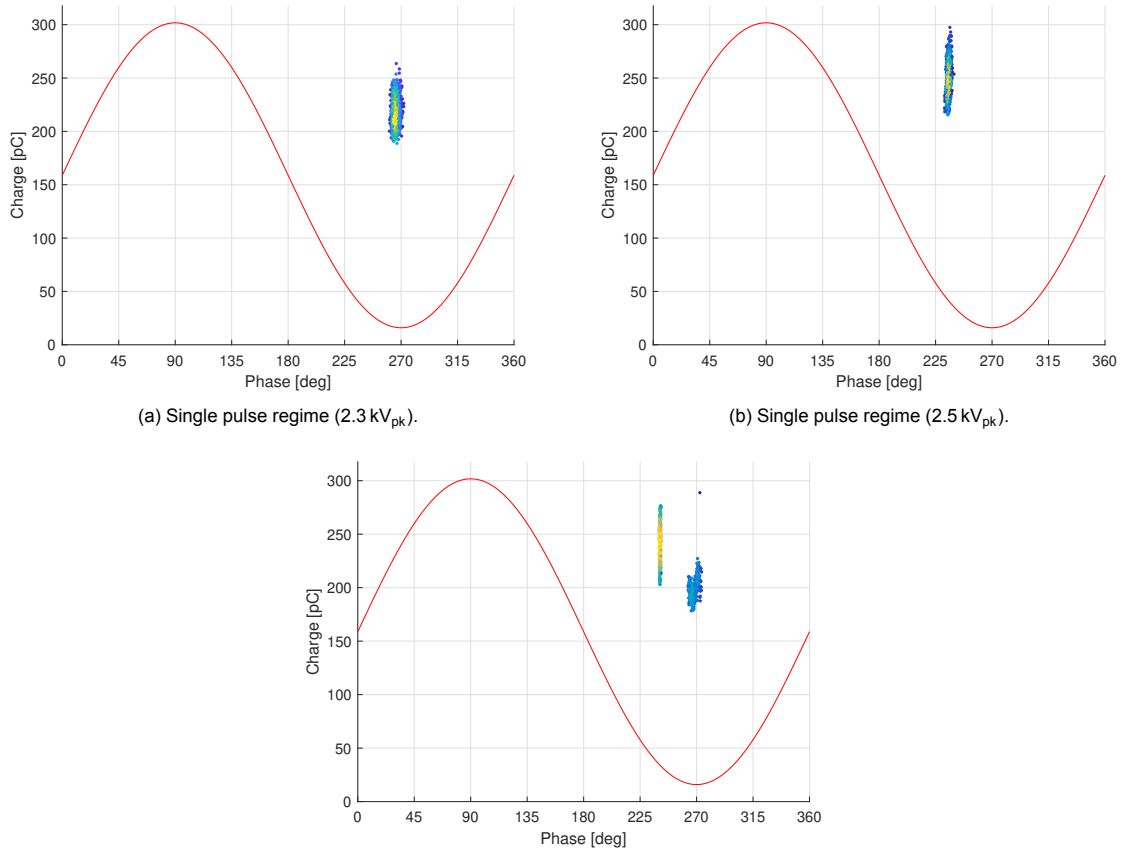


(a) 50 pC calibration pulse.

(b) 200 pC calibration pulse.

Figure C.10: Calibrator pulses measured with the PicoScope.

where k is a constant, which depends on the geometry, and U_0 is the inception voltage. The negative corona was measured at 30 kHz using a needle-plane setup. Due to the high-frequency voltage, the individual pulses can be distinguished.



(a) Single pulse regime (2.3 kV_{pk}).

(b) Single pulse regime (2.5 kV_{pk}).

(c) Double pulse regime (2.8 kV_{pk}).

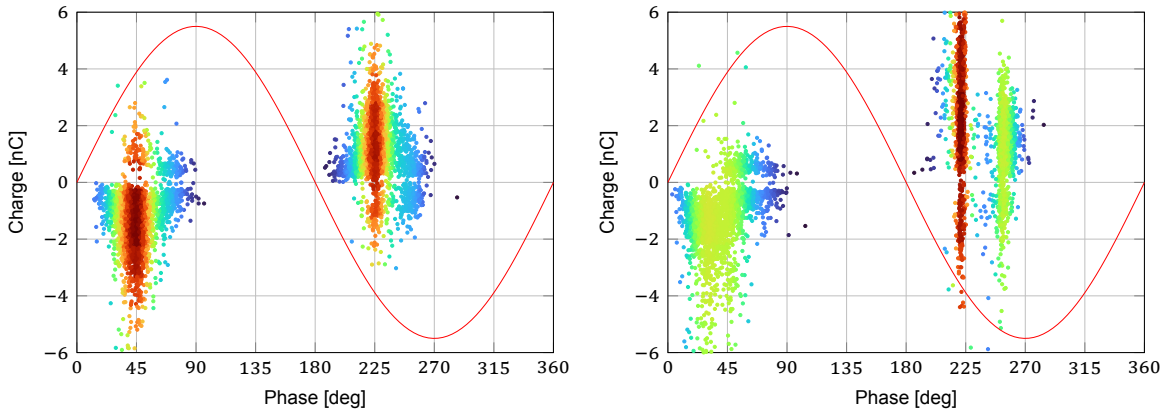
Figure C.11: Corona Trichel pulses recorded with a 30 kHz sinusoidal voltage.

At the PDIV, the pulse occurs precisely in the middle of the negative half-cycle. As the voltage increases, the pulse moves to the left, where the voltage equals the PDIV, and becomes more concentrated. More pulses occur when the space charge dissipates fast enough, i.e., when the repetition rate increases as in (C.11). Although these findings hold little importance for the current research, they may

give detailed information about the formation of Trichel pulses and their relation to the space charge around the needle.

Surface Discharges It was found that the presence of surface discharges on epoxy caused a drastic drop in resonant gain [87]. This may be explained by considering the model presented in Section C.1, where the losses due to surface discharges result in a drastically lowered R_p. The output voltage stagnates at the surface PDIV because any additional power provided by increasing the input voltage is spent sustaining the surface discharges. This makes the resonant setup unsuitable for testing in applications where surface discharges are expected. However, in the case of corona or (relatively small) internal discharges, there is no noticeable effect on the resonant gain and output voltage.

The phase resolved patterns of surface discharges on epoxy (samples taken from Patil [87]) at two voltages slightly above the PDIV are shown in Figure C.12. These show clearly that discharges are very concentrated (around the inception phase) at high frequency.



(a) At 1.6 kV_{pk} (b) At 1.8 kV_{pk}

Figure C.12: Surface discharges on neat epoxy at 30 kHz. Color indicates number PD events per cycle (red: high).

D

Partial Discharge Analysis

In this chapter, the partial discharge patterns recorded for various PCB samples and voltage levels are analysed in detail. The progression of the pattern (and its related quantities, e.g., the maximum PD magnitude over time) can give some insight into the processes occurring at the partial discharge site and hence the mechanism behind the corresponding degradation.

D.1. Statistical Operators

Statistical operators have been used to describe and classify partial discharges for a long time [55, 92, 93]. Two distributions are defined, which capture the primary quantities of a phase-resolved pattern.

1. The mean pulse height distribution $H_{qn}(\phi)$ represents the average amplitude in each phase bin.
2. The pulse count distribution $H_n(\phi)$ represents the number of discharges in each phase bin.

These distributions are typically evaluated separately for the positive and negative voltage half-cycle. In the following paragraphs, several operators are defined which operate on the four resulting distributions $H_{qn}^{+}(\phi)$, $H_{qn}^{-}(\phi)$, $H_{n}^{+}(\phi)$, $H_{n}^{-}(\phi)$.

Skewness and Kurtosis The skewness $\mathrm{Sk}[X]$ and (excess) kurtosis $\mathrm{Ku}[X]$ of a distribution correspond to its third and fourth moment, respectively. The skewness indicates the asymmetry, and kurtosis the “peakedness” compared to the normal distribution.

$$\mathrm{Sk}[X] = \sum \frac{(x_i - \mu)^3 p_i}{\sigma^3} \tag{D.1}$$

$$\mathrm{Ku}[X] = \sum \frac{(x_i - \mu)^4 p_i}{\sigma^4} - 3 \tag{D.2}$$

Correlation The similarity between the positive and negative half-cycle is captured in the charge asymmetry Q and cross-correlation cc. Combining these gives the modified cross-correlation mcc. This quantity can help distinguish, e.g., between dielectric- and electrode-bounded cavities.

$$Q = \frac{Q_s^- / N_q^-}{Q_s^+ / N_q^+} \tag{D.3}$$

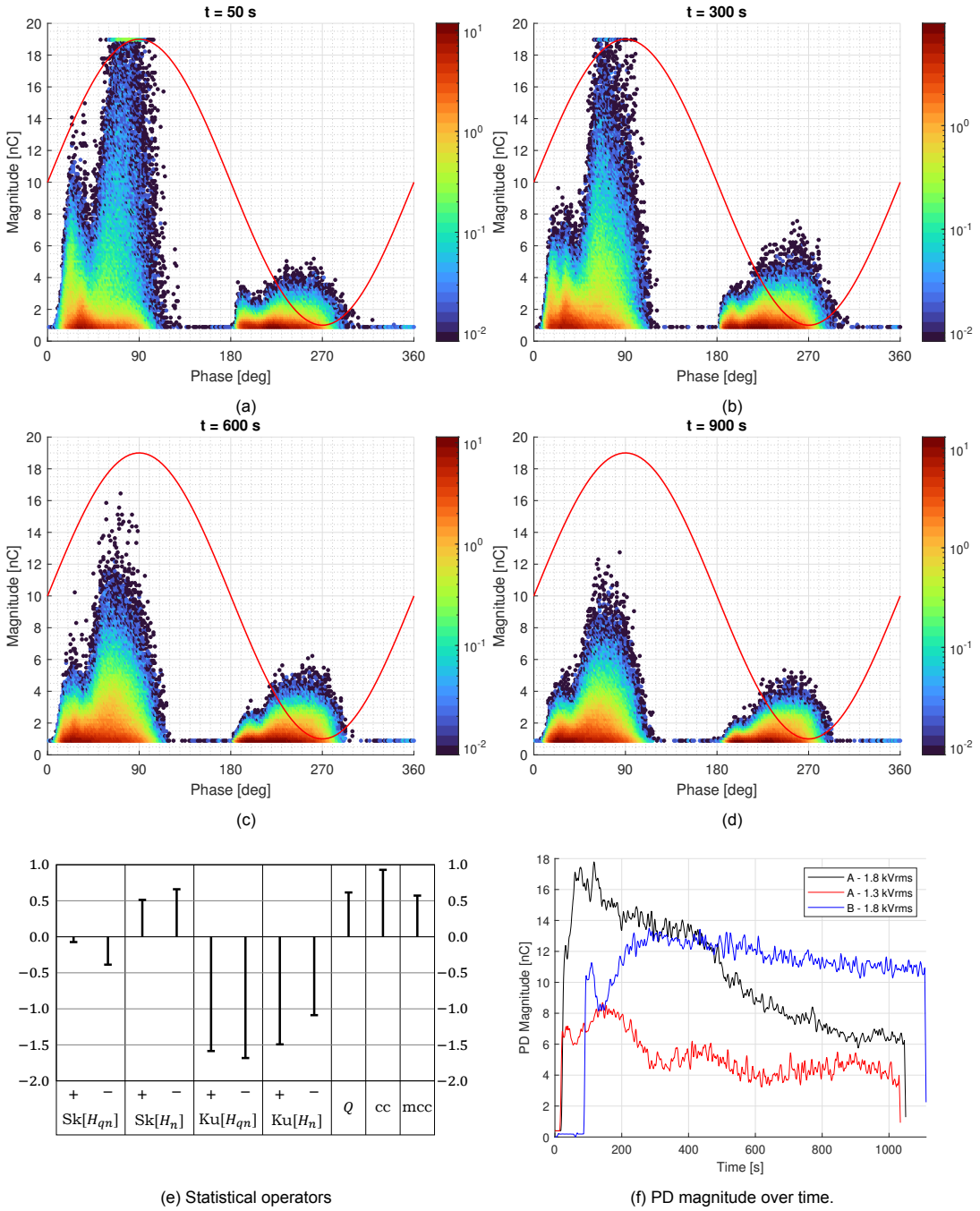
$$\mathrm{cc} = \frac{\sum x_i y_i - \frac{1}{n} \sum x_i \sum y_i}{n \sqrt{\mathrm{Var}[X]\,\mathrm{Var}[Y]}} \tag{D.4}$$

$$\mathrm{mcc} = Q \cdot \mathrm{cc} \tag{D.5}$$

Classification Partial discharge patterns can be classified by comparing the features extracted using the operators to reference measurements such as those presented in [92]. The features are summarised in a graph like Figure D.1e for easy visual inspection. The variation of the operators over time, especially $\mathrm{Sk}[H_{qn}(\phi)]$, gives additional insight into the discharge mechanism.

D.2. Surface Discharges in Air

Surface discharges are recorded on sample A at 1.8 kV_{rms} (i.e., 20 % above the PDIV). Figure D.1 presents four patterns at different test times. Tests are run for approx. 1000 s and full breakdown does not occur.



(e) Statistical operators

(f) PD magnitude over time.

Figure D.1: PRPD of surface discharges on Sample A at 1.8 kV_{rms}.

As expected, the PD is localised in the first and third quadrants (0° to 90° and 180° to 270°). Due to the electrode configuration (a small HV electrode and large ground plane), the patterns are highly asymmetrical towards the positive half-cycle. Positive streamers tend to be more prominent on the positive half-cycle, while negative streamers or smaller Townsend discharges occur on the negative half-cycle. Over time, the PD magnitude of the positive peak decreases significantly. This is usually attributed to the accumulation of space charge around the electrode, which affects the onset and development of

subsequent discharges [94, 95].

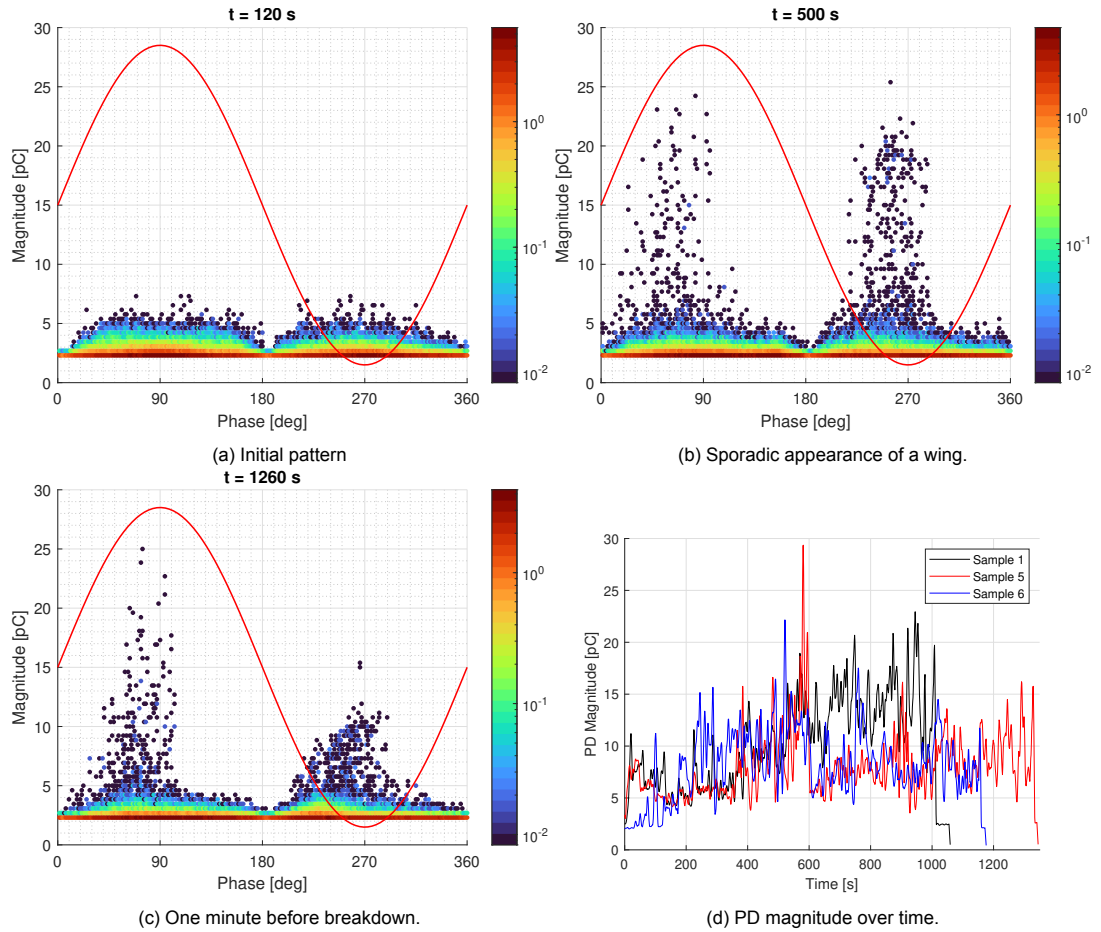
When the applied voltage is lower (closer to the PDIV), the magnitude of the discharges is much smaller, and the decrease over time is smaller (see Figure D.1f). Space charges may also explain this phenomenon, as the amount of charge deposited on the surface by the smaller discharges is less; hence the change in magnitude is not as drastic as when the voltage is higher.

D.3. Tests Under Oil

Next, PD measurements are performed under oil to eliminate the surface discharges described in the previous section. Under these conditions, the internal discharges in the dielectric should become visible (their magnitude being much less than the surface PD). Because the magnitude is typically much below 10 pC, it is difficult to determine an inception and extinction voltage. The discharges disappear into the noise floor (1 to 2 pC) when the voltage drops below approx. 2 kV_{rms}.

D.3.1. Sample A1

Measurements were performed on samples of type A (50 µm dielectric and $d = 10$ mm). The recorded PD activity was usually of low magnitude but extremely unstable, with a lot of variation in time and sometimes between samples. The most common pattern is shown in Figure D.2. It consists of two roughly symmetrical "humps" centered between 0° to 180° and 180° to 360°. In most cases, the magnitude increases over time but fluctuates due to irregular discharges above the humps, as shown in Figure D.2d.



(a) Initial pattern

(b) Sporadic appearance of a wing.

(c) One minute before breakdown.

(d) PD magnitude over time.

Figure D.2: PRPD of Sample A1 at 4.4 kV_{rms}.

The phase distribution of the pattern is unusual since internal discharges are usually concentrated between 150° to 270° and 330° to 90°. These discharges are likely floating particle/electrode discharges, which are typically symmetrical, as described above. The statistical operators in Figure D.3

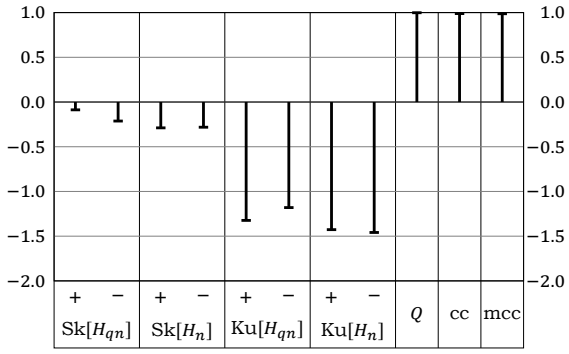


Figure D.3: Statistical analysis of Sample A1 (4.4 kV_{rms}).

support this conclusion. Considering the PCB sample construction, many floating electrodes are present since each PCB consists of an electrode grid with only one electrode energised at one time. Since this pattern obscures the other information which may be obtained from the analysis, samples are cut out of the PCB before testing.

D.3.2. Sample A2

The PRPD for a single electrode of sample A is presented in Figure D.4. In the first 1000 s, the pattern irregularly flares up with increasing magnitude, potentially indicating treeing discharges [96]. After 1000 s, the erratic discharges die down, and a cavity discharge pattern remains with a slowly decreasing magnitude. The statistical operators in Figure D.5 indicate that the discharges are cavity discharges.

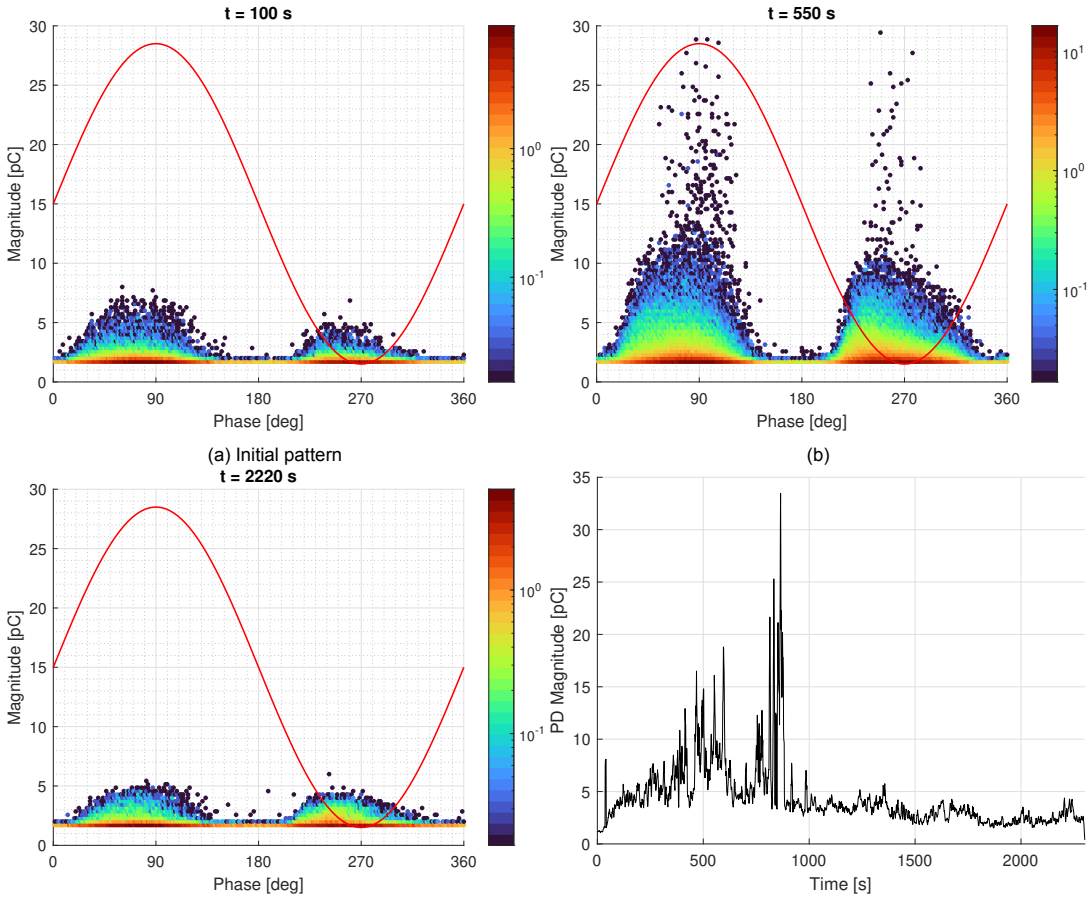
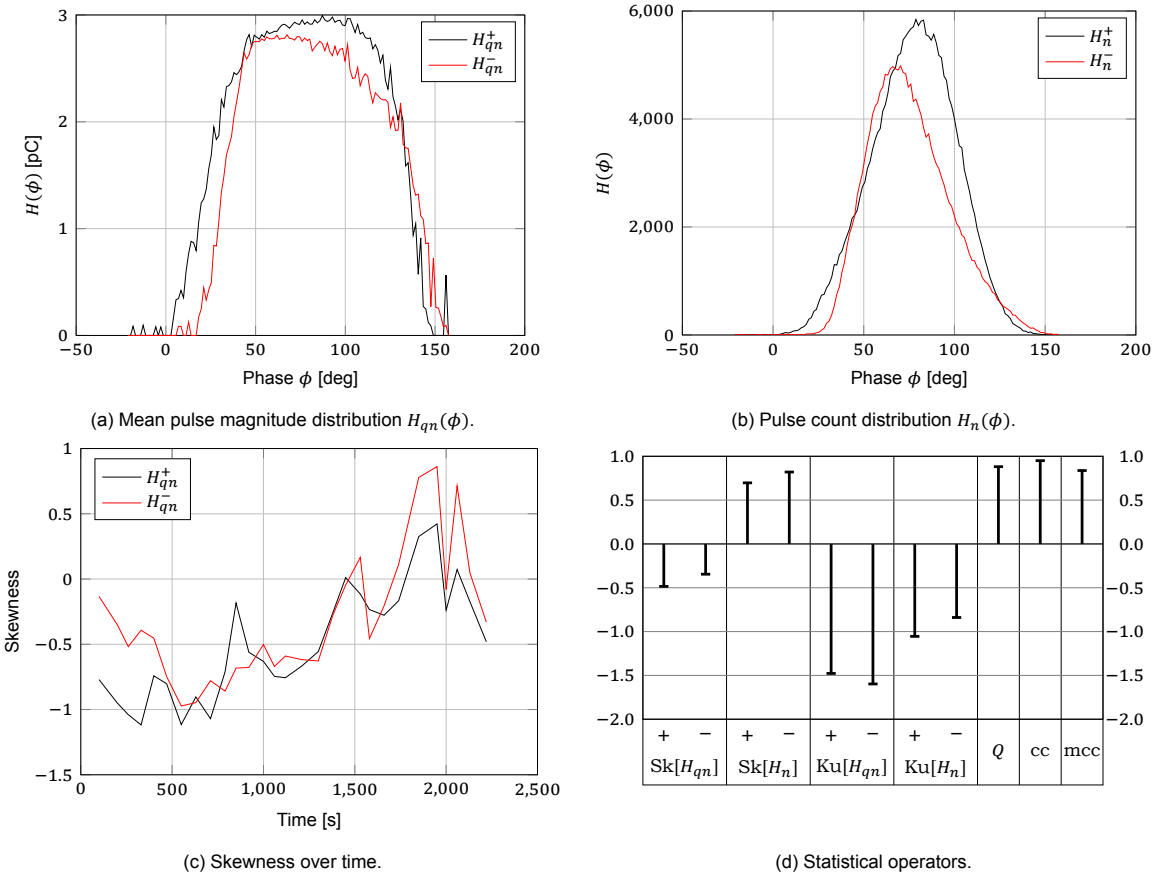


Figure D.4: PRPD of Sample A2 at 3.7 kV_{rms}.

The negative $\mathrm{Sk}[H_{qn}^{\pm}]$ indicates that the cavities are relatively narrow, while the high correlation between $H_{qn}^{\pm}$ shows that the cavity is not bounded by an electrode. The charge asymmetry Q is close to one, which is uncommon for treeing discharges. However, considering the PRPD, skewness, and PD magnitude over time, low levels of treeing are possible.



(a) Mean pulse magnitude distribution $H_{qn}(\phi)$.

(b) Pulse count distribution $H_n(\phi)$.

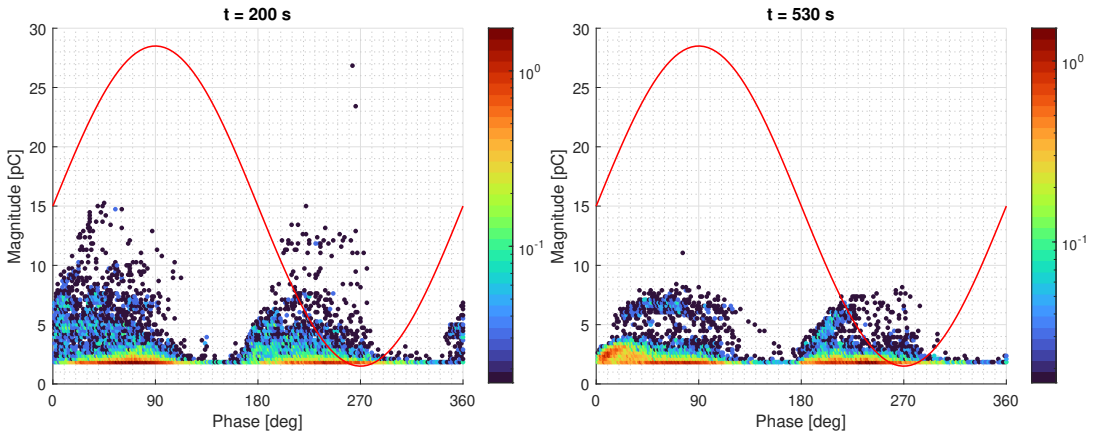
(c) Skewness over time.

(d) Statistical operators.

Figure D.5: Statistical analysis of Sample A2.

D.3.3. Sample B

Sample B with 150 µm dielectric) shows similar patterns and behaviour over time as sample A. The

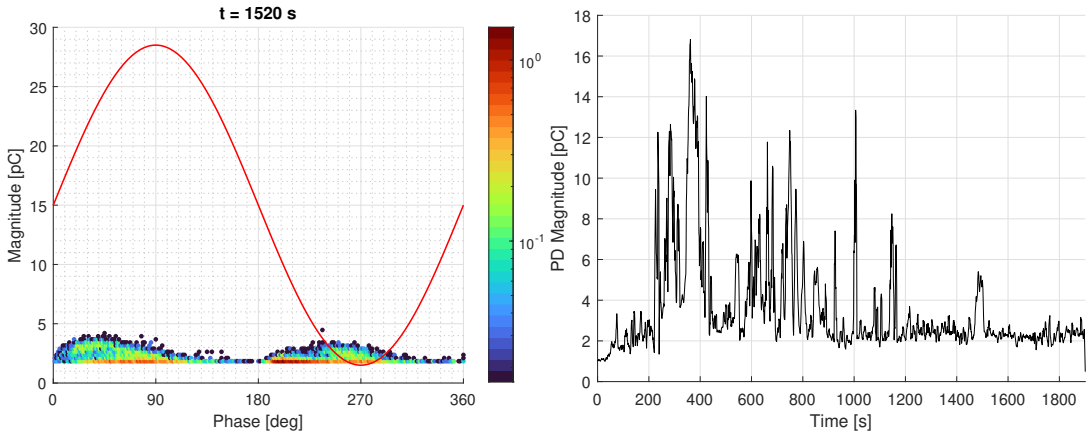


(a) Initial pattern

(b)

Figure D.6: PRPD of Sample B at 5.2 $\mathrm{kV_{rms}}$.

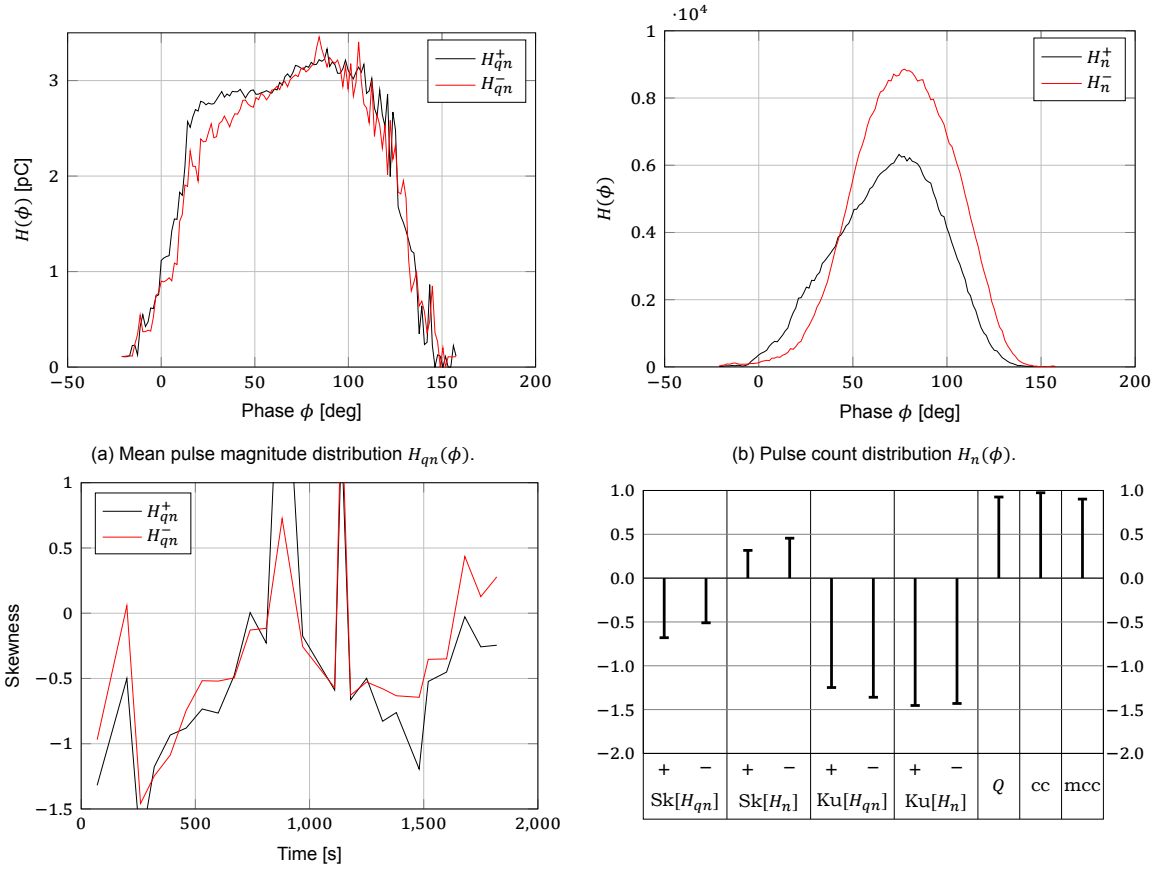
pattern is relatively small, with the irregular appearance of larger clouds of PD activity. After 1200 s, the irregular discharges die down, and a nearly constant cavity discharge pattern remains.



(c) (d) PD magnitude over time.

Figure D.6 (*Continued.*): PRPD of Sample B at 5.2 kV_{rms}.

The statistical analysis again supports this conclusion. The mostly negative skewness over time again indicates narrow cavities or low levels of treeing.



(a) Mean pulse magnitude distribution $H_{qn}(\phi)$.

(b) Pulse count distribution $H_n(\phi)$.

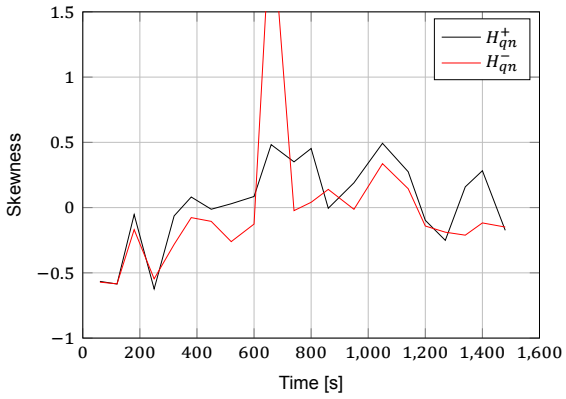
(c) Skewness over time.

(d) Statistical operators.

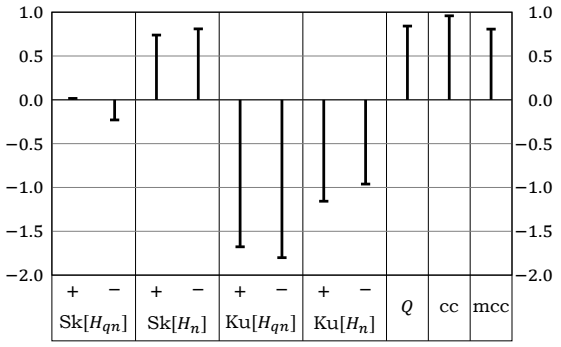
Figure D.7: Statistical analysis of Sample B (5.2 kV_{rms}).

D.3.4. Sample E

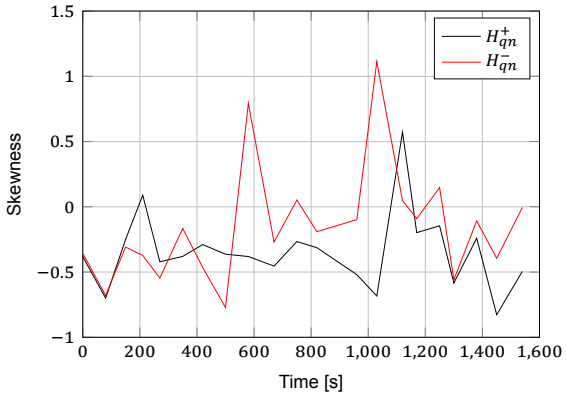
PRPD patterns for sample E are presented in Section 4.4.2, showing a typical pattern for cavity discharges with small electrical treeing. The statistical analysis leads to a similar conclusion. The skewness of $H_{qn}^{\pm}(\phi)$ is consistently below 0 at 4.3 kV_{rms}, indicating electrical treeing with certainty. At the lower test voltage (3.4 kV_{rms}), it fluctuates around zero. This could be because the treeing discharges are unstable or because there are no treeing discharges yet: this fluctuation skewness is characteristic of discharges in narrow cavities.



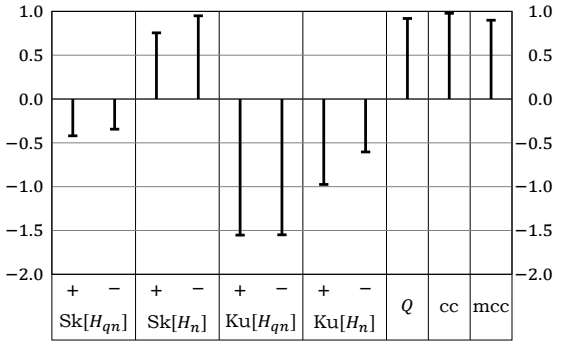
(a) Skewness over time (3.4 kV_{rms}).



(b) Statistical operators (3.4 kV_{rms}).



(c) Skewness over time (4.3 kV_{rms}).



(d) Statistical operators (4.3 kV_{rms}).

Figure D.8: Statistical analysis of Sample E at two test voltages.

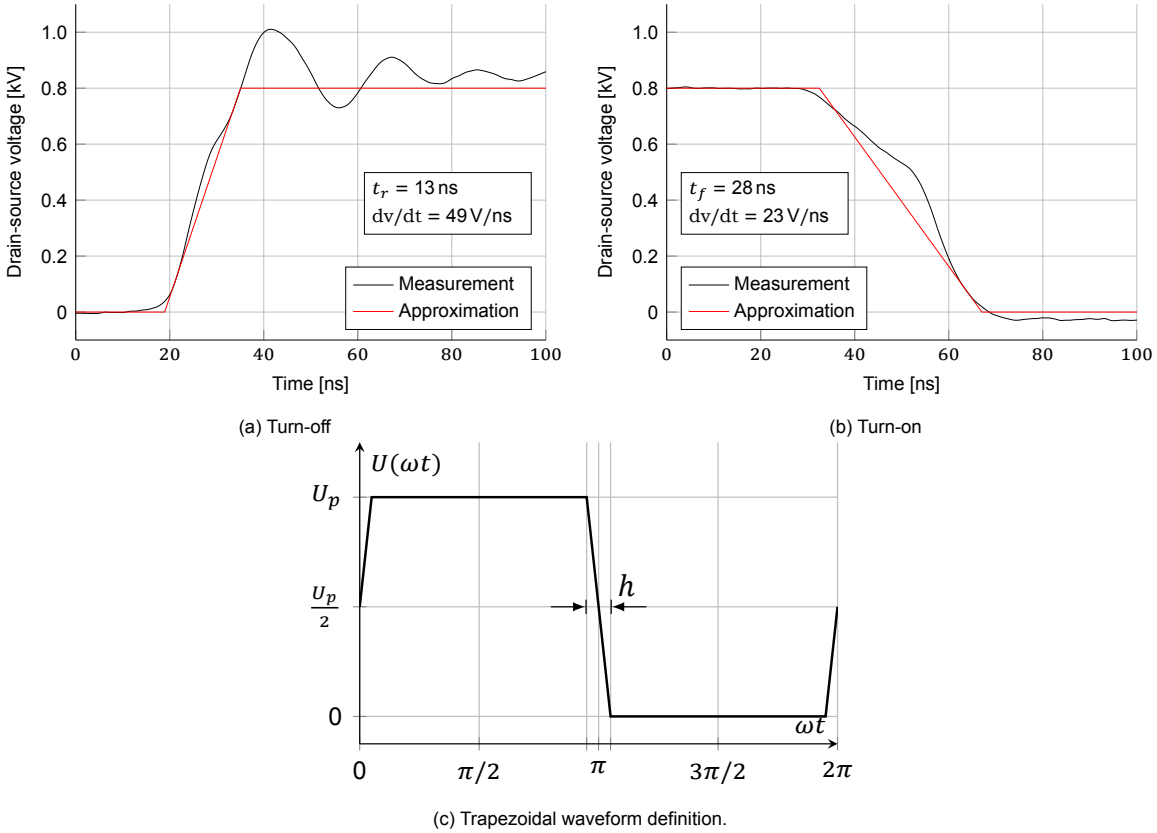
E

Derivations

E.1. Fourier Analysis of Trapezoidal Waveform

The switching waveforms in most power electronic converters can be reasonably approximated using a trapezoidal pulse waveform such as that shown in Figure E.1. The defining features of this waveform are the period T, the rise time t_r, and the amplitude U_p.

Overshoot, oscillation, and non-linearities in the flanks are neglected in this approximation, while they can add additional high-frequency components to the spectrum in a real application. Figure E.1 also shows that the rise and fall times may differ significantly. This difference is usually neglected, and the shortest time is chosen for harmonic calculations.



(a) Turn-off

(b) Turn-on

(c) Trapezoidal waveform definition.

Figure E.1: Power-electronic switching waveforms with trapezoidal approximation.

The Fourier coefficients of a periodic waveform $y(\omega t)$ with a frequency of $\omega = 2\pi f$ are given by

integration over a 2π period of ωt. In the case of (E.1), the interval $[-\pi, \pi]$ was chosen.

$$a_0 = \frac{1}{2\pi}\int_{-\pi}^{\pi} y(\omega t)d(\omega t) \tag{E.1a}$$

$$a_n = \frac{1}{\pi}\int_{-\pi}^{\pi} y(\omega t)\sin(n\omega t)d(\omega t) \qquad n = 1, 2, 3, \ldots \tag{E.1b}$$

$$b_n = \frac{1}{\pi}\int_{-\pi}^{\pi} y(\omega t)\cos(n\omega t)d(\omega t) \qquad n = 1, 2, 3, \ldots \tag{E.1c}$$

Taking the waveform $U(\omega t)$ as defined in Figure E.1c, the Fourier coefficients can be calculated using the definition above. For convenience, $h = {}^{2\pi t_r}/_{T} = 2\pi f t_r$ is defined as the rise time in radians. Because the waveform is even ($U(\omega t) = U(-\omega t)$), $a_n = 0$ for $n \geq 1$.

$$a_n = \frac{U_p}{2} \qquad n = 0 \tag{E.2a}$$

$$= 0 \qquad n \geq 1 \tag{E.2b}$$

$$b_n = \frac{4U_p}{\pi n^2}\frac{2}{h}\left[\cos\left(\frac{n\pi}{2} - \frac{nh}{2}\right) - \cos\left(\frac{n\pi}{2}\right)\right] \qquad n = 1, 3, 5, \ldots \tag{E.2c}$$

$$= 0 \qquad n = 2, 4, 6, \ldots \tag{E.2d}$$

Observe that the amplitudes of the harmonics are dependent on h, which encodes the rise time of the waveform. Therefore, it can be concluded that the dominant factor in the ageing of insulation (related to the harmonics) is the *rise time* and not the slew rate. It is well-known that the harmonics of a trapezoidal waveform decrease with 20 dB/dec above the knee point $f = \frac{1}{\pi t_r}$, and 40 dB/dec below the knee point.

Three spectra of trapezoidal waveforms with realistic parameters are presented in Figure E.2 up to the 1000th harmonic. The first spectrum represents a high-power IGBT switching 1.5 kV at 1.5 kHz and 1.5 µs (corresponding to a slew rate 1 kV/µs). The last two spectra are representative of fast Si or SiC MOSFETs switching 800 V at 30 kHz.

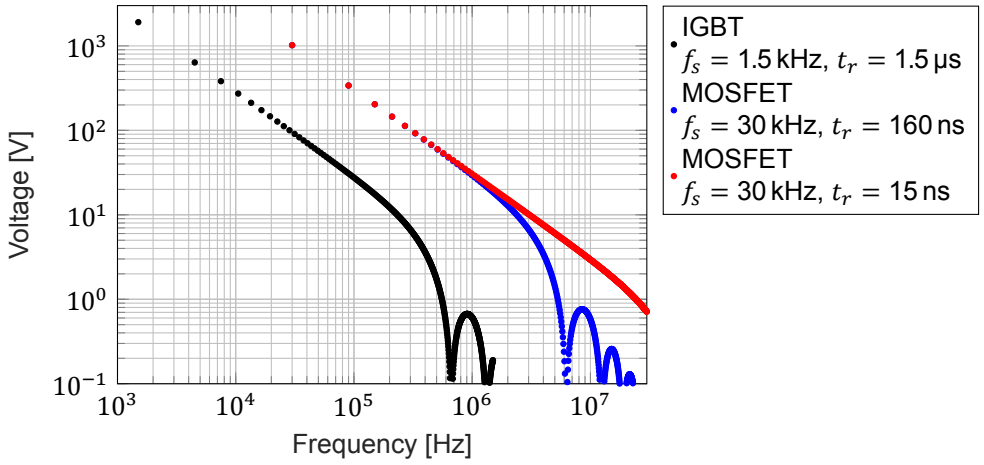


Figure E.2: Frequency spectrum of a trapezoidal waveform with varying h.

High switching frequencies and low rise time lead to increased harmonic content, which may lead to accelerated ageing of insulation materials. The switching frequency is the dominant factor, while rise time has a smaller influence on the harmonic content.

E.2. PQR Equation

Mathew [63] presents a Laplace domain equation for the step response of a simplified pulse transformer driving a capacitive load. This equation encodes the transformer parasitics P, damping filter "quality" Q, and their coupling R. However, a mistake is made in the original derivation, yielding the wrong result. An improved derivation is presented here.

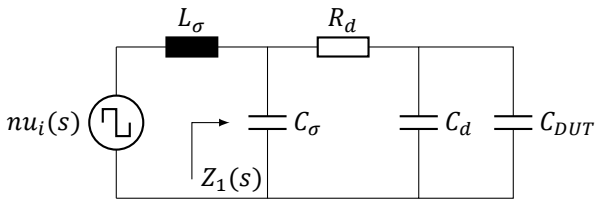


Figure E.3: Pulse transformer driving a capacitive load.

Derivation Consider the equivalent circuit presented in Figure E.3 obtained by referring the complete circuit to the secondary side of the transformer. The transfer function from the source $u_i(s)$ to the voltage across the DUT $u_o(s)$ is given by

$$u_o(s) = \frac{Z_1(s)}{sL_\sigma + Z_1(s)} \frac{1}{sR_dC_{eq} + 1} nu_i(s) \tag{E.3}$$

where $C_{eq} = C_d + C_{DUT}$ and $Z_1(s) = Z_{C_\sigma} \parallel (R_d + Z_{C_{eq}})$, as indicated in Figure E.3. Through some algebraic manipulation, this can be rewritten as a third-order equation in terms of P, Q, and R.

$$\frac{u_o(s)}{u_i(s)} = n \frac{\frac{1}{L_\sigma C_\sigma}\frac{1}{R_dC_{eq}}}{s^3 + s^2\frac{1}{R_d}\left(\frac{1}{C_\sigma} + \frac{1}{C_{eq}}\right) + s\frac{1}{L_\sigma C_\sigma} + \frac{1}{L_\sigma C_\sigma}\frac{1}{R_dC_{eq}}} \tag{E.4}$$

$$= \frac{nPQ}{s^3 + s^2R + sP + PQ} \tag{E.5}$$

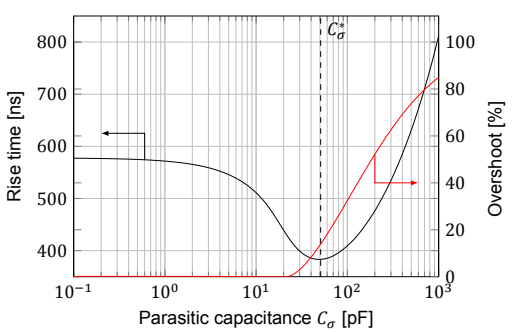
where

$$P = \frac{1}{L_\sigma C_\sigma} \qquad Q = \frac{1}{R_dC_{eq}} \qquad R = \frac{1}{R_d}\left(\frac{1}{C_\sigma} + \frac{1}{C_{eq}}\right) = Q + \frac{1}{R_dC_\sigma} \tag{E.6}$$

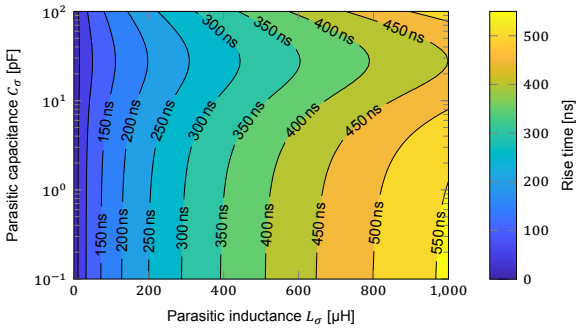
Step Response The step response can be calculated simply by substituting a step for $u_i(s)$. For example, assuming a step amplitude of U_p, the response is given by

$$u_o(s) = \frac{U_p}{s} \frac{nPQ}{s^3 + s^2R + sP + PQ} \tag{E.7}$$

The rise time of the PQR model is plotted versus the transformer parasitics L_σ and C_σ in Figure E.4. As expected, the rise time is approximately proportional to $\sqrt{L_\sigma}$. Unexpectedly, a small amount of parasitic capacitance (in the range of 25 to 50 % of C_{eq}) can actually reduce the rise time slightly. However, this is accompanied by an increased overshoot for the same R_d.



(a) Rise time and overshoot vs C_σ for L_σ = 440 µH, C_{eq} = 90 pF, and R_d = 4 kΩ.



(b) Rise time vs parasitic components (with C_{DUT} = 68 pF and $\zeta = 1/\sqrt{2}$).

Figure E.4: PQR model rise time versus parasitic components.

If $C_\sigma = 0$, the equivalent circuit is a damped series RLC circuit, and the rise time is determined by its natural frequency. When introducing C_σ, two critical parameters to consider are (i) the characteristic

impedance of the transformer circuit, and (ii) the natural frequency of the transformer compared to that of the load. When C_σ is small compared to C_{eq}, the natural frequency of the transformer is much larger than that of the damping filter. The reduced characteristic impedance of the transformer allows for faster charging of C_{eq} and hence a shorter rise time. When C_σ increases further, the natural frequency of the transformer becomes similar to or smaller than that of the filter, resulting in an increasing rise time. The transformer parasitics then dominate the rise time.

Under conditions different from those described in this thesis, such as excess damping or operation with very large or small capacitive loads, the described relations may change. No analytical equation has yet been found relating the rise time to C_σ in a form that is amenable to analysis.

Relation to Original Equation The original equation derived in [63] does have some significance. It describes the voltage at the high-voltage secondary winding terminal instead of the output voltage. The rise time on this node is much shorter due to the lack of the big damping resistor R_d; consequently, the overshoot is larger. Studying this equation may also yield interesting results since it shows the peak voltage that may occur on the HV winding.

$$\frac{u_o(s)}{u_i(s)} = \frac{nP(s+Q)}{s^3 + s^2R + sP + PQ} \tag{E.8}$$

E.3. Transformer Capacitances

In the transformer analysis, three equivalent circuits are used. The circuit shown in Figure B.2 serves as the basis. The following paragraphs show how to transform the capacitances between the different representations.

Primary-referred Equivalent Circuit A primary-referred circuit is used to determine the transformer parameters. The capacitances are transformed using the conservation of electrostatic energy, as discussed by Candolfi et al. [86].

$$C_{11}U_1^2 + C_{12}(U_1 - U_2)^2 + C_{22}U_2^2 = C'_{11}U_1^2 + C'_{12}\left(U_1 - \frac{1}{n}U_2\right)^2 + C'_{22}\left(\frac{1}{n}U_2\right)^2$$

$$(C_{11} + C_{12})\,U_1^2 + (C_{22} + C_{12})\,U_2^2 - 2C_{12}U_1U_2 = \left(C'_{11} + C'_{12}\right)U_1^2 + \frac{1}{n^2}\left(C'_{22} + C'_{12}\right)U_2^2 - \frac{2}{n}C'_{12}U_1U_2$$

Equating the terms yields three equations to refer the primary quantities (obtained by measurement) to the standard equivalent circuit.

$$C_{11} = C'_{11} + \frac{n-1}{n}C'_{12} \tag{E.9}$$

$$C_{22} = \frac{1}{n^2}C'_{22} + \frac{1-n}{n^2}C'_{12} \tag{E.10}$$

$$C_{12} = \frac{1}{n}C'_{12} \tag{E.11}$$

Secondary-referred Equivalent Circuit Similarly, the capacitances can be referred to the secondary side for use with the equivalent circuit in Figure E.3.

$$C_{11}U_1^2 + C_{12}(U_1 - U_2)^2 + C_{22}U_2^2 = C''_{11}(nU_1)^2 + C''_{12}\left(nU_1 - U_2\right)^2 + C''_{22}U_2^2$$

$$(C_{11} + C_{12})\,U_1^2 + (C_{22} + C_{12})\,U_2^2 - 2C_{12}U_1U_2 = n^2\left(C''_{11} + C''_{12}\right)U_1^2 + \left(C''_{22} + C''_{12}\right)U_2^2 - 2nC''_{12}U_1U_2$$

The following equations refer the transformer parameters to the secondary side for simulation or calculation using the PQR equation.

$$C''_{11} = \frac{1}{n^2}C_{11} + \frac{1-n}{n^2}C_{12} \tag{E.12}$$

$$C''_{22} = C_{22} + \frac{n-1}{n}C_{12} \tag{E.13}$$

$$C''_{12} = \frac{1}{n}C_{12} \tag{E.14}$$

It has been shown that C_{11} has a negligible influence on the pulse response [65]. Therefore, the parasitic capacitance of the transformer C_σ can be taken as (E.15).

$$C_\sigma = C''_{22} + C''_{12} = C_{22} + C_{12} \tag{E.15}$$

E.4. Confidence Intervals for MLE

Confidence intervals indicate the interval containing the quantity of interest at a certain confidence level (usually denoted $100(1-\alpha)\,\%$). Several types of confidence intervals exist, with different coverage probabilities. The following is derived from Meeker et al. [58].

E.4.1. CI Based on Profile Likelihood

In maximum likelihood estimation, the profile likelihood is obtained by evaluating the likelihood function while keeping all parameters except one constant.

$$R(\theta_1) = \max_{\theta_2,\ldots,\theta_n} \left[\frac{L(\theta_1,\ldots,\theta_n)}{L(\hat{\theta}_1,\ldots,\hat{\theta}_n)}\right] \tag{E.16}$$

The confidence interval with confidence level α for parameter θ is then defined as the set of θ such that

$$-2\log[R(\theta)] \leq \chi^2_{(1-\alpha;1)} \implies R(\theta) \geq \exp\left[-\frac{1}{2}\chi^2_{(1-\alpha;1)}\right] \tag{E.17}$$

E.4.2. Wald Confidence Interval

Very often, an approximate interval is sufficient. Under the assumption that the normalized quantity μ is distributed according to a normal distribution $Z_{\hat{\mu}} \sim N(0,1)$, the Wald confidence interval is

$$[\mu_+, \mu_-] = \hat{\mu} \pm z_{(1-\alpha/2)} \cdot \mathrm{se}_{\hat{\mu}} \tag{E.18}$$

where z_p is the p-th quantile of the standard normal distribution and $\mathrm{se}_{\hat{\mu}}$ is the standard error of $\hat{\mu}$. The standard error is calculated from the likelihood function through the variance-covariance matrix. Consider a likelihood function with two parameters μ and σ, the covariance matrix is

$$\Sigma_{\hat{\mu},\hat{\sigma}} = \begin{bmatrix} \mathrm{Var}[\hat{\mu}] & \mathrm{Cov}[\hat{\mu},\hat{\sigma}] \\ \mathrm{Cov}[\hat{\mu},\hat{\sigma}] & \mathrm{Var}[\hat{\sigma}] \end{bmatrix} = \begin{bmatrix} -\frac{\partial^2 \mathcal{L}(\mu,\sigma)}{\partial \mu^2} & -\frac{\partial^2 \mathcal{L}(\mu,\sigma)}{\partial \mu \partial \sigma} \\ -\frac{\partial^2 \mathcal{L}(\mu,\sigma)}{\partial \mu \partial \sigma} & -\frac{\partial^2 \mathcal{L}(\mu,\sigma)}{\partial \sigma^2} \end{bmatrix}^{-1} \tag{E.19}$$

evaluated in $\mu = \hat{\mu}$ and $\sigma = \hat{\sigma}$. This concept can be extended to any number of parameters. The covariance matrix can usually be obtained from the MLE tool or by applying finite differences in the neighbourhood of the estimated parameters.

E.4.3. Wald CI for Logarithmic Quantities

For quantities expressed on a logarithmic scale, such as the scale parameter σ, it is more useful to assume a distribution like $Z_{\log(\hat{\sigma})} \sim N(0,1)$. The Wald confidence interval is then

$$[\sigma_+, \sigma_-] = \left[\sigma \cdot w, \frac{\hat{\sigma}}{w}\right] \qquad w = \exp\left[z_{(1-\alpha/2)} \cdot \mathrm{se}_{\hat{\sigma}}\right] \tag{E.20}$$

E.4.4. Confidence Bands

It is desirable to indicate the confidence bands to visualise the uncertainty in the predicted lifetime curves. A confidence band $\hat{f}(x) \pm w(x)$ around the point estimate $\hat{f}(x)$ with coverage probability $1-\alpha$ satisfies (E.21) for all values of x.

$$\mathrm{P}\left[\hat{f}(x) - w(x) \leq f(x) \leq \hat{f}(x) + w(x)\right] = 1 - \alpha \tag{E.21}$$

The function $w(x)$ can be generated using the information obtained from the fitting procedure. For example, non-simultaneous bounds are given by

$$w(x) = t\sqrt{\mathrm{MSE} + J_\theta(x)\Sigma_{\hat{\theta}}J_\theta^T(x)}, \tag{E.22}$$

where MSE is the mean squared error, $J_\theta(x)$ is the Jacobian of $f(\theta; x)$ with respect to θ, and $\Sigma_{\hat{\theta}}$ is the covariance matrix resulting from the MLE procedure. The parameter t is calculated using

$$t = F_\nu^{-1}(1 - \alpha/2), \tag{E.23}$$

where F_ν^{-1} is the inverse Student-t distribution, ν is the number of degrees of freedom, and α is the confidence level.

E.5. Volume Effect for Weibull Distribution

The relation for the volume effect can be derived by assuming that the breakdown of an insulation sample with volume n can be split into n independent events for samples with unit volume. The reliability (i.e., the non-breakdown probability) of the enlarged sample becomes

$$1 - P_n = \prod_{i=1}^{n}(1 - P_i) \implies F_n(x) = 1 - (1 - F_1(x))^n. \tag{E.24}$$

Combining this with the definition of the Weibull CDF, a relation between η_1, β_1 and η_n, β_n can be derived which relates the measured parameters (subscript 1) to a volume which is n times larger (subscript n).

$$\begin{aligned} F_n(x) &= 1 - \left(\exp\left[-\left(\frac{x}{\eta_1}\right)^{\beta_1}\right]\right)^n \\ &= 1 - \exp\left[-n\left(\frac{x}{\eta_1}\right)^{\beta_1}\right] \\ &= 1 - \exp\left[-\left(\frac{x}{\eta_1/n^{1/\beta_1}}\right)^{\beta_1}\right] \end{aligned}$$

After enlarging the sample, the breakdown voltages (scale parameter η_n) follow a Weibull distribution with modified parameters

$$\eta_n = \eta_1 \cdot n^{-1/\beta_1}, \tag{E.25}$$

$$\beta_n = \beta_1. \tag{E.26}$$

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