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Three-terminal electric transport measurements on gold nano-particles combined with *ex situ* TEM inspection

B Gao, E A Osorio, K Babaei Gaven and H S J van der Zant

Kavli Institute of Nanoscience, Delft University of Technology, Lorentzweg 1, 2628 CJ Delft, The Netherlands

E-mail: h.s.j.vanderzant@tudelft.nl

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Abstract

We have fabricated nanometer-spaced electrodes on electron-transparent silicon nitride membranes. A thin Cr/Au layer is evaporated on the backside of the membrane which serves as a gate electrode. Using these devices, we have performed three-terminal electron transport measurements on gold nano-particles at liquid helium temperature. Coulomb Blockade features have been observed and the capacitance to the gate has been extracted. After transport measurements, the Cr/Au back gate is removed and the devices are inspected with a transmission-electron microscope (TEM). TEM inspection reveals the presence of a few nano-particles in the nanogap, which is in agreement with the transport measurements. In addition, the nano-particle size as observed by TEM coincides with the one estimated from the gate capacitance value.

(Some figures in this article are in colour only in the electronic version)

1. Introduction

In the search for new quantum effects and novel building blocks for integrated circuits, the electronic transport properties of nano-objects such as nano-particles and molecules have been widely explored over the past few decades [1–3]. The typical size of these objects is less than 10 nm; a scale that is unreachable using conventional lithography methods. New nano-fabrication techniques have been developed to make electrical contacts to these nano-objects, such as electromigration [4], mechanical break junctions [5, 6], electroplating [7], nano-particle break junctions [8] and the shadow evaporation technique [9]. Moreover, since nanometer-sized objects are usually beyond the resolution capability of most scanning-electron microscopes (SEM), the lack of information about the exact sample topology and structure can result in an ambiguity when interpreting the transport data. For example, electromigration of metal nanowires is a frequently employed technique to make closely spaced electrodes with a gap of a few nanometers. Such electrodes are indispensable to electrically address objects in the sub-10 nm scale. However, it has been reported that metal particles formed during electromigration may be left in the gap, giving spurious signatures of Coulomb Blockade (CB) and Kondo physics, which are not related to the objects deposited onto the device [10–13]. A completely different system, in which difficulties in the understanding of transport data may occur, is a fullerene peapod; in this case it is not clear if the irregular structure of Coulomb diamonds is due to the encapsulated fullerene molecules or to defects or impurities in the nanotube [14].

High-resolution transmission-electron microscopy (HRTEM) is a powerful tool to inspect objects on the nanometer scale. A combination of transport measurements with TEM inspection will help to lift ambiguities in data interpretation. However, transport measurements on the nanometer scale are often performed using devices made on non-electron-transparent substrates, which do not allow TEM inspection. Only a few attempts have been made to develop electron-transparent substrates and perform two-terminal transport measurements using devices made on these substrates [15, 16]. In this paper, we demonstrate a technique which makes three-terminal transport measurements compatible with *ex situ* TEM inspection. We use an electron-transparent Si_3N_4 membrane as the substrate and nanogaps are formed on the membrane

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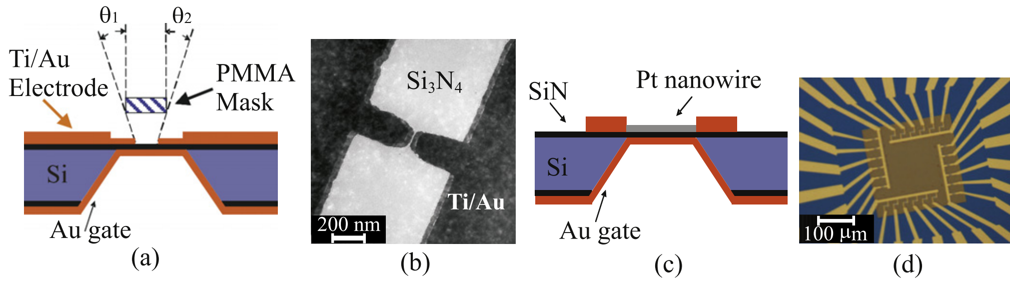

Figure 1. (a) Schematic view of device type I made by angle evaporation using a PMMA mask. θ_1 and θ_2 are the corresponding evaporation angles. (b) TEM image of device type I. The brighter area is the transparent Si_3N_4 substrate and the darker area is the Ti/Au electrodes. The Cr/Au back gate has been removed. (c) Schematic view of device type II. The Pt nanowire lies on the silicon nitride membrane. On the backside of the membrane, a Cr/Au layer serves as the back gate. (d) Top-view of device type II under a microscope. The inner square is the free standing Si_3N_4 membrane with 24 Pt wires with contact pads evaporated on top.

using electromigration or angle evaporation. A Cr/Au layer is deposited on the backside of the membrane, serving as the back gate. With these devices, we have performed three-terminal electron transport measurements on gold nano-particles. At cryogenic temperatures, CB features are observed. After transport measurements, the Cr/Au back gate is removed and TEM inspection is carried out on these samples. TEM inspection reveals the presence of a few nano-particles, in agreement with transport measurements. In addition, the nano-particle size as observed by TEM coincides with the one estimated from the gate capacitance values.

2. Sample preparation

We start with the deposition of 100 nm thick Si_3N_4 layers on both sides of a silicon (100) double side polished wafer using low-pressure CVD (LPCVD) [17]. A two-step etching process is employed to make the free standing Si_3N_4 membrane. At first a 500 nm thick PMMA layer is spin-coated on the sample surface. The sample is then baked on a hot plate at 175 °C for 1 h. Standard E-beam lithography (EBL) is used to define the PMMA etching mask. The exposed Si_3N_4 layer is removed by an anisotropic low-pressure reactive ion etching process (LHZ 400 system using: CHF_3/O_2, gas flow 50/2.5 sccm, chamber pressure 8 μbar and forward power 50 W). The remaining Si_3N_4 layer forms the etching mask for the next wet etching step, which is performed in a 30% (mass concentration) KOH solution at 85 °C at a speed of about 1.5 μm min^{-1}. The KOH solution attacks the silicon and produces the characteristic anisotropic V shaped etch profile. The resulting free standing Si_3N_4 membrane is about 200 × 200 μm^2 in size, which is strong enough to survive the following wet chemical processing. After the membrane is made, a Cr/Au (3/97 nm) layer is evaporated on the back side of the membrane; this is used as the back gate.

Two fabrication methods are used to define nanometer-spaced electrodes (figure 1). The first one is angle evaporation. We perform an oblique evaporation through a lift-off mask (MAA/PMMA double layer), similar to the method developed by Dolan [18]. Electrodes are made of Au with a Ti sticking layer. The thinnest part of the electrode is 17 nm thick, which consists of 3 nm Ti with 14 nm Au on top.

The second method to make a nanogap is electromigration of Pt bridges, which together with Au leads and bonding pads are patterned on the front side of the membrane using standard E-beam lithography. The length, width and thickness of the Pt wires are 300 nm, 200 nm and 14 nm, respectively. Before electromigration the typical device resistance is around 200 Ω. Electromigration is performed with feed-back control.

To deposit gold particles into the nanogap, we use a similar method as described by Ralph *et al* [19]. A thin gold film is evaporated on the sample; gold nano-particles are formed due to surface atom diffusion. This method yields gold particles with a diameter ranging from 5 to 15 nm. After particle deposition, current–voltage characteristics (I–V) as a function of gate voltage are recorded at cryogenic temperatures.

3. Three-terminal transport measurements

We have measured in total 142 devices; 76 of them are devices in which nanogaps are made by angle evaporation. For the remaining 66 devices, nanogaps are formed by electromigration. After metal deposition, Coulomb blockade features are observed in 39 out of these 142 devices. Most of them show the irregular structures of Coulomb diamonds, indicating that the device contains multiple islands in the transport channel. Clear signatures of single-island behavior have not been observed. In a few cases, quasi-periodic Coulomb diamonds were observed, reminiscent of transport through a few dots. We will discuss two samples in detail; one fabricated by angle evaporation (sample 1) and one by electromigration (sample 2).

The nanogap of sample 1 was fabricated using angle evaporation and its low-bias resistance was larger than 10 GΩ. After gold deposition, the resistance dropped to 100 kΩ, suggesting that electron tunneling takes places through one or a few metal nano-particles located in the gap. The sample was then cooled to cryogenic temperature to perform transport measurements. Figure 2(a) (bottom panel) shows the color plot of the differential conductance ($\mathrm{d}I/\mathrm{d}V$) as a function of gate (V_g) and source–drain voltage (V_{sd}). The data was acquired with V_{sd} swept from −20 to 20 mV and V_g from −5 to 25 V. The brighter regions symbolize high conductance and darker regions signify blockade of the current due to Coulomb interaction. A quasi-periodic structure of Coulomb diamonds

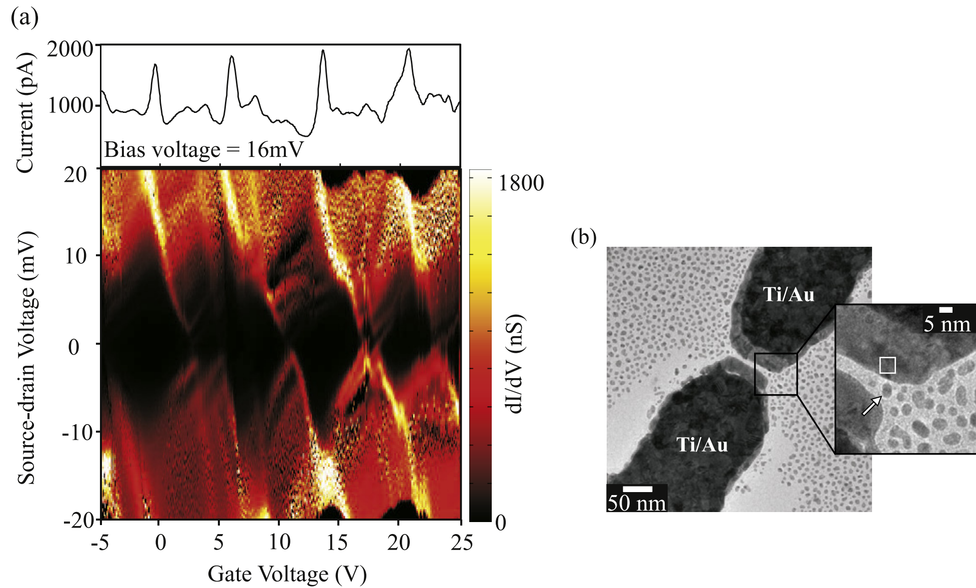

Figure 2. (a) Bottom: color-scale plot of the differential conductance as a function of source–drain and gate voltage. Top: a single gate trace taken at $V_{sd} = 16$ meV, showing the current modulation as a function of the gate voltage. (b) Corresponding TEM image of sample 1. Inset: zoom-in of the gap area, in which the white square is a reference area of 35 nm^2. The white arrow denotes the particle that likely contributes the most to the transport.

is visible in the plot. One trace of the current modulation as a function of the applied gate voltage is plotted in figure 2(a) (top panel). The four peaks correspond to the four bright diamond edges in the dI/dV plot. The gate capacitance can be calculated from the spacing in V_g between these peaks. For this sample, the average spacing ΔV_g is about 7.5 V, from which we estimate the gate capacitance $C_g = e/\Delta V_g$ to be 0.02 aF. Assuming that the particle has a flat form and $C_g = \varepsilon_r \varepsilon_0 A/d$, with A the surface area of the particle, $d = 100$ nm the thickness of Si_3N_4 dielectric layer and ε_r is the dielectric constant of Si_3N_4 ($\approx$7.5); the 0.02 aF value indicates that a particle with a surface area $A \approx 35$ nm^2 dominates the transport of sample 1.

Electromigration of the Pt nanowire of sample 2 was performed at room temperature. After electromigration, the low-bias device resistance was about 20 MΩ. Upon cooling the sample to cryogenic temperature, no signature of CB or the Kondo effect was found, indicating a clean gap. The sample was then warmed up again to room temperature. Because of the stability of the Pt contacts, the device resistance remains almost the same [20]. It was loaded into an evaporator, and a 2 nm thick gold film was evaporated on top. After evaporation, the low-bias device resistance dropped to 100 KΩ. Subsequently the sample was cooled to cryogenic temperature and current–voltage (I–V) curves were measured as a function of gate voltage.

Figure 3(a) shows dI/dV as a function of gate (V_g) and source–drain voltage (V_{sd}). The data was acquired with V_{sd} swept from −50 to 50 mV and V_g from 0 to 30 V. For clarity, only part of the stability diagram is shown in the figure; the diagram for the whole gate voltage range shows the same behavior. The non-closed Coulomb diamonds indicate that transport occurs through islands in series. In addition, diamond edges with more than two different slopes also indicate the presence of islands in parallel [21]. These two observations point at a complicated geometry of particles in the gap. Nevertheless, a regular pattern is still present in the conductance map of figure 3(a), as indicated by the yellow dot lines. These lines denote a set of equally spaced parallel diamond edges which are probably related with tunneling events through the same transport barriers. From the line spacing ($\Delta V_g \approx 0.5$ V), we deduce a gate capacitance of about 0.32 aF. This gate capacitance is fifteen times larger than the one found for sample 1. Using the same assumption as described for sample 1, we expect a fifteen times larger particle to be present in the gap of sample 2: surface area $A \approx 500$ nm^2.

4. TEM inspection

To confirm the sample topology that we deduced from the differential conductance map, TEM inspection has been carried out. The sample was first warmed up to room temperature. In order to perform TEM inspection, the Cr/Au back gate beneath the Si_3N_4 membrane was removed. First a PMMA (4% in Anisole) solution was drop cast onto the sample top surface and the sample was baked at 70 °C for 5 min. Gold particles and the nanogap were therefore protected in the subsequent processing steps. Before dipping the sample into the Au and Cr etchants, ozone cleaning was employed to remove organic contaminations on the back gate electrode to facilitate a homogeneous Au/Cr etching. We used a mixture of I_2:KI:H_2O (1:4:40) as the gold etchant. The Cr etchant used is the commercially available CR-10 from MERCK KGAA. The sample was dipped into the gold and Cr etchant successively; each for 30 s. Afterwards it was rinsed in DI water and 2-propanol. The protective PMMA layer was finally removed using acetone.

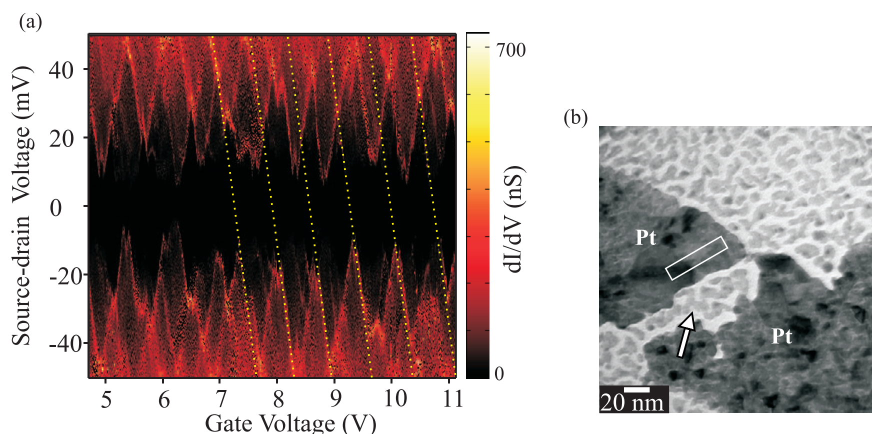

Figure 3. (a) Color-scale plot of the differential conductance as a function of source–drain and gate voltage of sample 2. (b) Corresponding TEM image. Dark regions denote Pt electrodes. The white rectangle indicates an area of 500 nm^2. The white arrow points at a cluster of particles that most likely dominates the transport.

TEM inspection has been performed with a TECNAI G2 microscope from FEI. Figure 2(b) shows the TEM image of sample 1. The inset in the figure is a zoom-in of the gap area, within which a few small particles can be identified. The one indicated by the white arrow is probably the dominant one in the transport channel, whose area is about 35 nm^2, as seen from the comparison with the nearby 35 nm^2 white reference square. The observation is in good agreement with the sample topology deduced from I–V measurements, which also indicated a dominant single transport channel through a particle with a size of about 35 nm^2.

Figure 3(b) shows the topology of sample 2. A cluster of particles can be identified in the gap, as indicated by the white arrow in the image. The particle size is larger than sample 1. The transport channel is composed of particles in series and in parallel, which agrees with the conclusion drawn from the dI/dV map. From the image we can also see particles linked to each other, forming a bigger particle whose size is comparable with the white reference rectangular (10×50 nm^2). This may explain the large gate capacitance determined from the dominant periodicity in the dI/dV map.

5. Conclusion

We have developed a technique which allows the combination of low-temperature three-terminal transport measurements with *ex situ* TEM inspection. Measurements on gold nanoparticles have demonstrated that the sample topology deduced from dI/dV plots agrees with the one that is observed by TEM. We envision that this technique can be used to reduce the ambiguity of data interpretation by providing more information about sample topology and structure. Future work will be extended to combined three-terminal measurements with *in situ* TEM inspection.

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