MSc thesis in Electrical Engineering

A High Input Impedance Readout Integrated Circuit based on Continuous-Time Sigma-Delta Modulator with FIR DAC Feedback

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Abstract

This thesis focuses on the design of a high input impedance sensor readout system based on a continuous-time sigma-delta modulator with finite-impulse-response digital-to-analog converter feedback.

Both the system-level and circuit-level design techniques of this system are investigated. The concept and design methods of finite-impulse-response digital-to-analog converters are introduced. The first integrator with source degeneration resistors and an input Gm-boosting cell is designed to achieve high input impedance and linearity. Both simulation and post-layout simulation results confirm the expected effective number of bits of 15 bits in the readout performance. The design is fabricated in a standard 180nm CMOS technology.

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Acronyms

1 Introduction

The heart rate extraction system proposed in [1], which is based on the infrared thermometry of the ear, reduces motion artifacts while improving user comfort, maintaining signal quality and reducing power consumption. A thermopile is used to convert the detected infrared light signal into an output voltage, where the infrared light signal demonstrates the blood vessel temperature, which in turn gives the heart rate data. This thesis presents the design and realization of a readout integrated circuit (ROIC) for thermopiles which achieves improved precision. The primary areas of concern are design methodologies at the system level and design techniques at the circuit level.

The targeted sensing application and the rationale behind constructing a readout circuit for the sensor are described in Section 1.1 of this chapter. Section 1.2 presents energy-efficient ROICs with a direct current-feedback instrumentation amplifier (DCFIA) architecture. Next, the fundamental concepts of sigma-delta modulators (SDMs) are clarified in Section 1.3. The existing CTSDM structures with high input impedance are introduced and compared in Section 1.4. Finally, Section 1.5 details how this work is organized.

1.1 Motivation

The intrinsic detection circuitry of the sensor is shown in Fig. 1.1. Multiple improvements are required in the circuitry design. The resolution is limited by the noise level of the readout circuit at frequencies below $5Hz$. Detecting the sensor signal and executing a subsequent analysis requires an ROIC with a lower noise level. Because the output voltage of the sensor is at the millivolt level, signal conditioning is necessary to amplify the signal to a reasonable level. Since the signal conditioning also has to read the output voltage without significant loading of the sensor, a high input impedance is required for this stage. To eliminate the effects of input voltage variations, a high common-mode rejection ratio (CMRR) is also expected.

Instrumentation amplifiers (IAs) are widely used to read out small output voltage [2]. After being amplified, the analog signal is injected into a high-resolution analog-to-digital converter

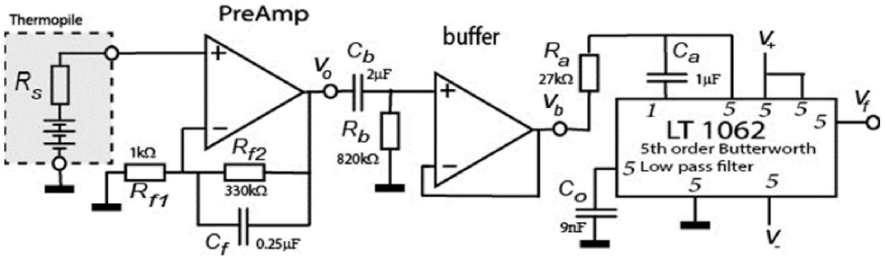

Figure 1.1: Readout amplifier circuit used in [1]

(ADC) in order to facilitate the subsequent digital processing. The signal conditioning and ADC marked in red in Fig. 1.2 comprise the ROIC for a heart rate extraction sensor.

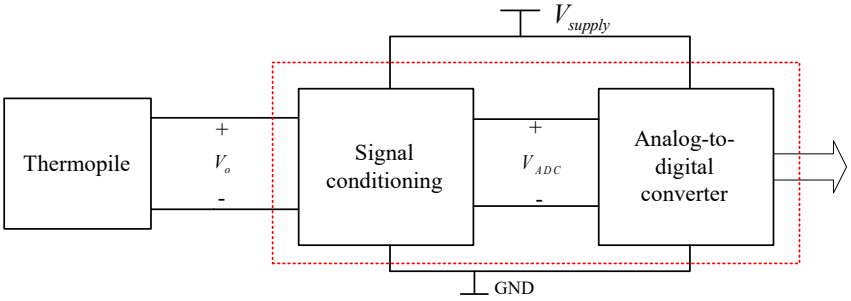

Figure 1.2: Readout system for a heart rate extraction sensor.

IAs provide a high CMRR, high gain, and high input impedance in conventional ROICs, which are crucial requirements for a readout system. As the first stage of the system, the IA essentially defines the input referred noise (IRN) and energy efficiency of the entire system. The topology of IAs is therefore worth considering.

The input stage of a well-designed amplifier is primarily responsible for determining its noise. In a traditional three-opamp IA, as shown in Fig. 1.3, the two input stages marked in red are in parallel connection. The total noise is doubled at the input [3], making the energy efficiency of the classic IA is insufficient. With a common-mode (CM) level constrained by the output voltage, a three-opamp IA is employed when the supply voltage of the sensor is relatively small, which places a limitation on the sensor's sensitivity [4].

The term "current feedback" stems from the fact that in Fig. 1.4 [5], V_{in} and V_{fb} are first converted into currents by G_{m1} and G_{m2}. Then a subtraction is made at the virtual ground of the G_{m3} input. The CFIA features two input stages doubling the input noise similar to the

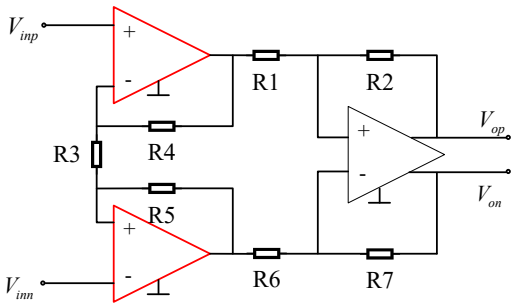

Figure 1.3: Three-opamp IA

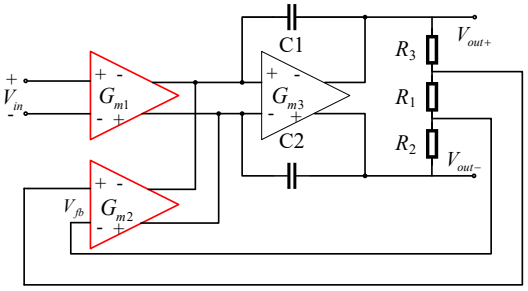

Figure 1.4: Current feedback IA

classic IA. If G_{m1} and G_{m2} are identical, the closed-loop gain of this IA can be expressed as:

$$A_{c,cf} = \frac{R_1 + R_2 + R_3}{R_1}.$$

The popular current-feedback instrumentation amplifier (CFIA) structure has benefits over the classic three-opamp topology. One of the attributes of the CFIA compared to the three-opamp IA is its capability to sense the differential input with a CM range covering either of the supply rails [3]. With the isolation of input and feedback transconductances, the input impedance and CMRR are both higher than that of the classic IA [2]. In order to attain high energy efficiency, μV-level offset can be eliminated by dynamic element matching (DEM) such as chopping [6].

Although gain error and drifts caused by mismatch between G_{m1} and G_{m2} are indeed drawbacks of the CFIA, the gain accuracy can be enhanced with DEM and digitally assisted gain error-correction [4][5]. The CFIA structure is chosen because the benefits outnumber the drawbacks.

1.2 Current-Feedback Readout Systems

A readout system for heart rate extraction needs to detect a small differential voltage superimposed on a large common-mode voltage. A high input impedance, high CMRR, high linearity, and low IRN are especially aimed at this system. These criteria are briefly outlined, after which the ROIC architecture based on these criteria is established in this section.

Input Impedance

Precision sensors with inherent resistance convert infrared light signals into electric signals. If the input impedance of the ROIC is small, excess signal attenuation will be caused by the

resistive division. In order to achieve high resolution, the input impedance of the ROIC should be large enough to eliminate this attenuation.

Common-Mode Rejection Ratio

As previously noted, the small differential output of a heart rate extraction sensor is carried on a large CM voltage. A large CMRR is therefore needed to reduce errors produced by this CM voltage.

Input-Referred Noise

Since the ROIC is designed to detect the output of the thermopile sensor, the input-referred noise (IRN) should be low enough to meet the demand for resolution. In the desired ROIC, low power dissipation is also required as applications are battery-operated and issues are brought on by the self-heating of sensors. The trade-off between power consumption and noise level allows the increase in the energy efficiency of the ROIC so as to reduce the IRN while retaining a power budget.

Linearity

The ROIC should be more linear than the sensor itself in order to accurately process its output signal [7]. Some circuit techniques are employed to reduce the non-linearities, but at a cost. Increasing circuit complexity brings challenges to circuit design and may introduce excess noise. Therefore, a trade-off between linearity and energy efficiency is worth considering during the design.

ROICs can be roughly divided into two categories: conventional ROICs consisting of an IA and an ADC, as shown in Fig. 1.5, and direct ROICs without an IA as shown in Fig. 1.6. In the place of the IA in conventional ROICs, the input stage of the ADC in direct ROICs satisfies the requirements for the input stage.

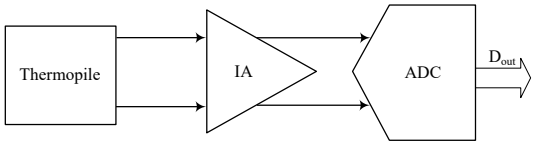

Figure 1.5: Conventional ROIC

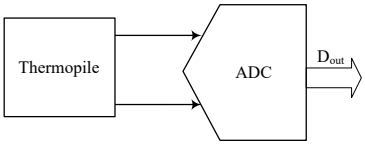

Figure 1.6: Direct ROIC

Compared with conventional ROICs, direct ROIC topologies, as shown in Fig. 1.6, incorporate the IA and ADC reducing complexity. In Fig. 1.7, G_{m1} and G_{m2} are the input and feedback transconductances, respectively. Similar to conventional CFIAs, the CFIA-like ROIC also features a high input impedance and high CMRR. A low pass filter (LPF) is used to suppress

out-of-band noise [8]. It is evident that this topology occupies less space than conventional ones.

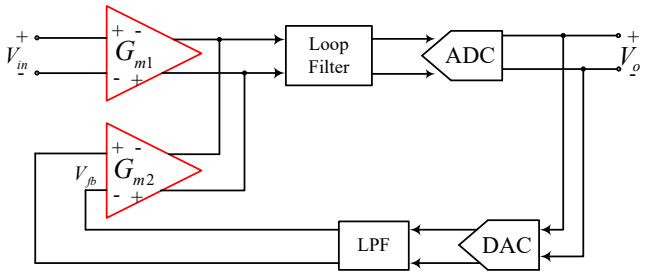

Figure 1.7: CFIA-like ROIC

1.3 Sigma-Delta Modulators

Nyquist-rate ADCs are one type of data converters that can reconstruct the input with a sampling frequency larger than twice the bandwidth (BW), according to Nyquist's criterion. However, the linearity and precision are limited by the mismatch between components in circuit implementation. The other kind of data converter is oversampled converters which can achieve high resolution (more than 12 bits) with a relatively high speed without the influence of component mismatch. This section provides an overview of the fundamentals of oversampled converters.

First-Order or Second-Order Sigma-Delta Modulator

To begin with, a first-order SDM allows for better modulation of inband quantization noise by employing a multibit quantizer, which in turn reduces the quantization noise over all frequencies. In addition, a quantizer with small inband quantization noise can also be employed to raise the signal to quantization noise ratio (SQNR). A first-order SDM converts analog signals into digital signals while modulating quantization noise out of band, so it can be regarded as a quantizer. On the other hand, a second-order SDM is constructed by substituting the first-order SDM for the quantizer in another first-order SDM. With a higher-order SDM, quantization noise is better modulated through the steeper noise shaping. Still, the resolution of an SDM cannot be increased by blindly raising the order of it, because high-order SDMs involve a more complex circuit design, are less stable, and consume more power. A second-order SDM is therefore sufficient to realize the target resolution in this design.

Discrete-Time or Continuous-Time Sigma-Delta Modulator

Where the signal is sampled determines how the discrete-time (DT) and continuous-time (CT) SDM differ from one another. In a DTSDM, the input signal is first sampled and then injected into the first integrator, as demonstrated in Fig. 1.8(a). Errors generated by sampling can not be removed by a loop filter, so a pre-anti-aliasing filter is required. The sampling in a CTSDM, however, takes place before the quantizer, as depicted in Fig. 1.8(b). Because errors caused by sampling will be filtered by the modulator, the CTSDM is inherently anti-aliasing so no extra filtering is necessary.

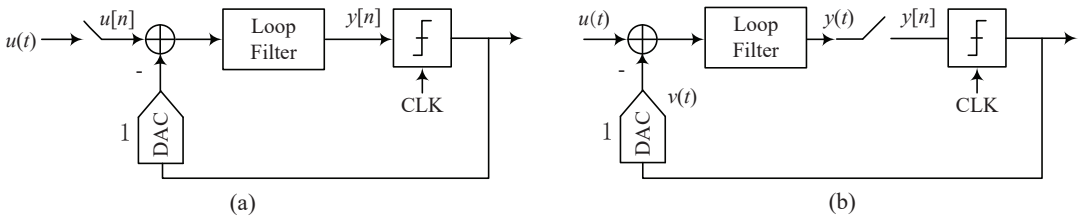

Figure 1.8: Simplified architecture of (a) DT SDM and (b) CT SDM.

As for the circuit implementation of these two types of modulators, switched-capacitor integrators are commonly used in DTSDMs [9]. Coefficients in modulators are decided by the values of the capacitors, which are robust over time and temperature. This structure is also less sensitive to parasitic capacitance. The switch implementation, however, can be problematic if the supply voltage drops to the threshold voltage of the transistors [10]. As a result, extra circuits are needed to maintain proper functioning of the switches, which makes circuit design more challenging. The settling time of the opamp also places a restriction on the sampling frequency of DTSDMs.

In CTSDMs, circuits can be realized in an active-RC or Gm-C technique [11]. The coefficients are less reliable than those of DTSDMs in this regard because they are determined by the values of the resistors and capacitors. Another disadvantage of CTSDMs is that they are inherently more susceptible to clock jitter[9]. Nonetheless with some techniques to reduce the step size of DAC feedback waveform, such as multi-bit quantization, the sensitivity to clock jitter can be reduced. One of the advantages of CTSDMs is that they are easier to drive since their input impedance is resistive. The sampling frequency is limited only by the speed of the quantizer and feedback DAC, thus CTSDMs can have higher sampling frequencies with minimal power dissipation.

In order to realize the resolution and lower power consumption target, a CTSDM is chosen for the design.

Working Principle of the DAC

In a CTSDM, the feedback DAC converts the output of quantizer sequences into a waveform which is nearly identical to the input signal (except for noises). The regulation of a DAC generating a feedback waveform from the digital output code produced by the quantizer can be abstracted into a pulse shape $p(t)$. Mathematically, the essence of the DAC can be regarded as the convolution of the digital code and pulse shape. The feedback waveform $v(t)$ injected into the input can be expressed as:

$$v(t) = \sum_n v[n]p(t - nT_s), \tag{1.1}$$

where $v[n]$ denotes the output sequence of the quantizer, and T_s denotes the sampling period. A commonly used feedback DAC is the non-return-to-zero (NRZ) DAC, whose pulse shape can be expressed as:

$$p(t) = \begin{cases} 1, & 0 < t < T_s \\ 0, & t > T_s \end{cases} \tag{1.2}$$

1.4 Continuous-Time Sigma-Delta Modulator with High Input Impedance

The specifications of ROICs designed in conventional CFIA and DCFIA topologies are illustrated in Table 1.1. With separate optimization of the input stages, conventional ROICs [12] can achieve better energy efficiency than some direct ROICs [13]. Direct CFIA-like ROICs[13][14] typically occupy a smaller area but other specifications such as IRN still need optimization.

Since the DCFIA with CTSDM topology has been determined for this design, the application of [13] and [14] to this architecture will be analyzed in the following.

As previously stated, a high input impedance is the most important requirement for a high precision ROIC. A feasible option to achieve this is applying Gm-C input. In a conventional Gm-C integrator, the input current is only produced by the transconductance, whose value is highly reliant on input voltage:

$$I_{in} = g_m V_{in}$$
$$g_m = \mu_n C_{ox} \frac{W}{L} V_{ov},$$

where V_{ov} denotes the overdrive voltage which is related to V_{in}. More non-linearities are introduced with a larger input range. Although the linearity can be improved, high excess

Table 1.1: State-of-Art of ROICs

	[12]	[13]	[14]	[8]
Architecture	CFIA+DTSDM[1]	DCFIA+CTSDM[2]	DCFIA+CTSDM	CFIA+CTSDM
Year	2011	2012	2020	2011
Input Stage	PMOS	PMOS	PMOS	NMOS
Technology	0.7um	0.7um	110nm	0.7um
Area(mm^2)	6	3	0.078	3.3
Supply Voltage(V)	5	5	1	5
Supply Current(mA)	0.27	0.24	0.0065	0.4
$\pm$Input Range(mV)	40	40	150	50
DC CMRR(dB)	140	120	76	>120
CM Input Range(V)	0-2.5	0-2.5	–	–
INL(ppm)	5	15	–	–
Offset(uV)	48	1	–	32
Input Noise Density($nV/\sqrt{Hz}$)	16.2	20	95	200
NEF[3]	10.4	12	9.3	15.4

[1] DTSDM stands for discrete-time sigma delta modulator.

[2] CTSDM stands for continuous-time sigma delta modulator.

[3] The noise efficiency factor NEF $= V_{irn}\sqrt{2I_{tot}/(\pi \cdot V_t \cdot 4kT \cdot BW)}$ is always used to evaluate the energy efficiency of IAs [15], where V_{irn} denotes the input-referred noise voltage, I_{tot} denotes the total amplifier supply current, V_t denotes the thermal voltage, and the BW denotes bandwidth.

noise will be concomitant, leading to poor energy efficiency[11]. Therefore, the conventional Gm-C integrator is relegated to high speed and low dynamic range applications.

A CTSDM with the complementary high-pass and low-pass paths proposed in [8] is the foundation of [13]. With a replica transconductance Gm_{fb} on the feedback path, the current flowing in the forward path loop in [8] is the difference between the current generated by input transconductance Gm_{in} and Gm_{fb}, which should guarantee better linearity. However, with delay on V_{fb}, the linearity will still be limited. Residual quantization noise will also be injected into the input and introduce errors. The design in [13] keeps the replica Gm_{fb} on the feedback path and uses an inner loop to compensate for the delay. A high CMRR of $120dB$ can be achieved but the linearity of this structure is then limited by the mismatch between the Gm-cells. What's more, the power consumption of this structure is $1200\mu W$ which is not appealing either.

Another method to maintain the high input impedance and high linearity at the same time is the Gm-C based CTDSM with the feedback-assisted Gm linearization introduced in [14]. The signal current produced by source degeneration and the feedback current generated by an RDAC is subtracted so that the input swing is reduced and the correlation between the input swing and the input voltage is abolished. With a Gm-boosting component, the effective G_m is:

$$G_{m,eff} = \frac{g_{m1}A(s)}{1 + g_{m1}A(s)R_s} \approx \frac{1}{R_s}, \tag{1.3}$$

where g_{m1} denotes the transconductance of the input transistor, $A(s)$ denotes the gain of the Gm-boosting component, and R_s denotes the value of the source degeneration resistor. Because g_{m1} is largely enhanced by $A(s)$, $G_{m,eff}$ can be considered as being determined by R_s. With these techniques, the linearity of this structure is increased. The virtual ground provided by the amplifier also contributes to minimized quantization noise leakage. Based on the Gm-C, the input impedance is guaranteed but the input range is limited.

Generally, a Gm-C based DCFIA ROIC like [14] maintains the high input impedance and small area occupation without an additional low pass filter. However, a voltage-controlled oscillator is employed which increases the complexity of the architecture and circuit design. That aside, it can serve as a starting point to simplify the configuration for a high-precision ROIC.

1.5 Organization of the Thesis

This dissertation describes the design procedures and implementation of a Gm-C based DCFIA ROIC in CTSDM architecture. Starting with [14], a different configuration is proposed to

realize a high precision ROIC with a simpler architecture.

Further system level designs are illustrated in Chapter 2. Choices of the modulator topology and circuit architecture are explored and explained. System-level techniques are proposed based on high input impedance and aimed at high precision.

In Chapter 3, the principles and challenges in building a CTSDM with a feedback FIR DAC are clarified. Previous design methods are briefly explained and new design methods are proposed. Numerical simulation results are presented and compared to demonstrate the superiority of the proposed design methods.

The circuit-level implementation of the proposed ROIC, which combines the current-feedback instrumentation amplifier with a continuous-time sigma-delta modulator, is delivered in Chapter 4. The layout design in a 0.18um TSMC technology along with post-layout simulation results are presented and analyzed.

Finally, conclusions are made in Chapter 5 and future work is described.

2 System-Level Design

In this chapter, the topology of a CTSDM and subsequent choices of architecture related to circuit design are analysed and clarified. The system-level design of the proposed CTSDM is demonstrated.

2.1 Choices of Topology

In order to maintain high performance with an ROIC, the designed SDM should meet the requirements listed in Table 2.1. A second-order CTSDM can be employed to satisfy the specifications with the merits mentioned in Section 1.3. For a second-order SDM, a reasonable sampling frequency can be obtained according to the effective number of bits (ENOB) and BW. With an ENOB of 15 bits, the signal to distortion and noise ratio (SNDR) can be calculated as: $SNDR = 6.02 \times ENOB + 1.76 \approx 92dB$. Without consideration of noise and distortion, the SQNR should be approximately 10dB larger than the SNDR, so it is aimed to be larger than 102dB. With a single-bit (two-level) quantizer, the theoretical oversample ratio (OSR) obtained can reach approximately 2^8 according to Fig. 2.1 [9] . Given a bandwidth $f_b = 2.5kHz$, the sampling frequency f_s can be

$$f_s = 2 * OSR * f_b = 1.28MHz.$$

Table 2.1: Target Specifications of the SDM

Target	Parameters
ENOB	15 bits
Bandwidth	$2.5kHz$

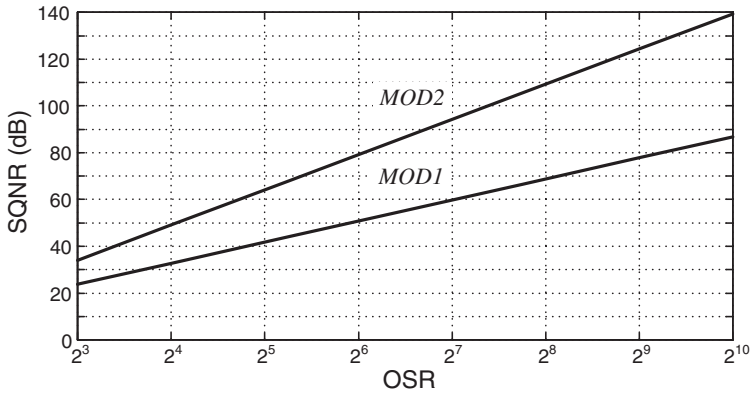

Figure 2.1: Theoretical SQNR versus OSR for MOD1 and MOD2 with a two-level quantizer (MOD1 denotes a first-order SDM; MOD2 denotes a second-order SDM.)

Loop-Filter Topology

After obtaining the target specifications, we start to select the topology of the CTSDM design. A cascade of integrators with a feedforward (CIFF) structure is chosen, where the output of the first integrator is forwarded to the output of the second integrator. A major advantage of this structure is that the output of the first stage has virtually no signal at the input frequency so the gain of the first stage in the signal band can be large. This high gain can effectively suppress any noise and non-linearity caused by the rest of the loop. Without signals at the input frequency, the output swing of the first integrator, which is also the input swing of the second integrator, is reduced in turn relaxing the requirements for the input range of the second-stage integrator. The feedforward path gains these advantages at the cost of introducing extra zeros to the signal transfer function (STF). Therefore, the STF will peak at a high frequency. The advantages of this structure outweigh the disadvantages, so the architecture of the SDM is chosen, as illustrated in Fig. 2.2 [16]. Since the DAC used here has a pulse shape of 1 (when $0 < t < T_s$) as defined in Eq. (1.2), it is an NRZ DAC.

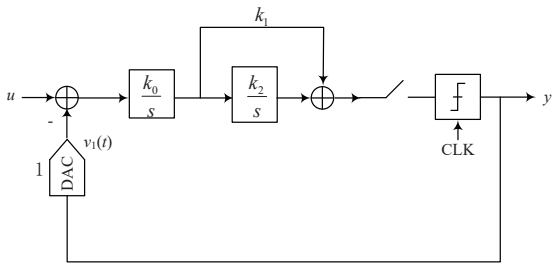

Figure 2.2: Prototype CIFF modulator

Quantization and Feedback DAC

Generally, increasing the order of noise shaping or the OSR contributes to better resolution. However, a high-order modulator involves design complexity and a sampling rate that is too high dramatically increases power dissipation. In order to obtain a high resolution without increasing the order or OSR, multi-bit quantization is used.

A major advantage of multi-bit quantization is that the quantization has a smaller step size, which leads to less quantization noise and a better SQNR. A reduced step size also results in a smaller signal swing in the loop filter, hence the circuit can operate at a lower slew rate. Because noise caused by clock jitter is proportional to voltage levels in the feedback DAC, the modulator using multi-bit quantization with a reduced step size is less sensitive to clock jitter.

Multi-bit quantization, however, can be problematic. With more comparators and multi-bit feedback DACs, the circuit complexity rises and more power is required. Mismatch between the feedback DACs also introduces nonlinearity into the system, which degrades the performance of the modulator.

Single-bit quantization with one comparator significantly simplifies the circuit design. Moreover, the single-bit feedback DAC is also inherently linear. The limitation of it is that with a two-level feedback voltage, the DAC is sensitive to clock jitter and requires better linearity of the forward-path loop.

An elegant way to realize high resolution, to withstand clock jitter noise, and to maintain linearity in a CTSDM simultaneously is to use a finite impulse response (FIR) feedback DAC with a single-bit quantizer. A FIR DAC with a transfer function of $F(z)$ is used in Fig. 2.3.

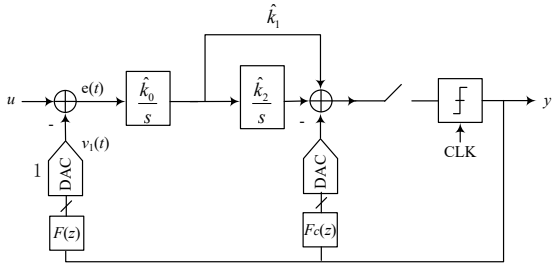

Figure 2.3: FIR CTSDM based on the prototype

A semi-digital realization of a FIR DAC is shown in Fig. 2.4. With an N-tap FIR DAC, the two-level output sequence at different moments is multiplied by a coefficient a_n ($n = 1, ..., N$). To simplify the layout design, all taps of the FIR filter are identical. Also the DC gain of $F(z)$

should be 1 in order to ensure a unity in-band STF. Thus, the transfer function of the FIR filter can be expressed as:

$$F(z) = \frac{1}{N}\left(1 + z^{-1} + \cdots + z^{-(N-1)}\right), \tag{2.1}$$

where N denotes the number of taps. Before being injected into the input signal, the output of the single-bit quantizer is first filtered by the FIR filter. Therefore, the two-level quantized output is changed into an N-level waveform and the step sizes are reduced by N times. With a reduced step size, the FIR feedback benefits from all the merits of multi-bit quantization. A single-bit feedback DAC and single comparator also make it inherently linear as in a single-bit quantizer.

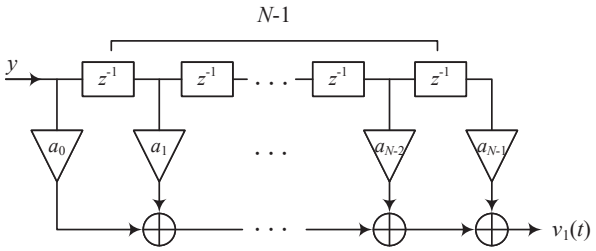

Figure 2.4: Semi-digital realization of FIR filter

With the use of a FIR DAC, delays are introduced to the modulator. Signal attenuation in the high-frequency components will also appear due to the characteristics of the sinc filter. Revising the coefficients, more specifically increasing the feedforward coefficient k_1, contributes to reducing this attenuation although the reduction is limited and not accurate. A compensation feedback FIR DAC is therefore needed to accurately compensate for this attenuation and stabilize the loop. The working principle of a compensation FIR DAC is similar to that of the main FIR DAC as shown in Fig. 2.4. The transfer function of the compensation FIR DAC is:

$$F_c(z) = a_0 + a_1 z^{-1} + \cdots + a_{N-1} z^{-(N-1)}, \tag{2.2}$$

and the values of the coefficients will be obtained in Chapter 3.

The feedback point chosen for the compensation FIR DAC is the output of the second integrator, as shown in Fig. 2.3 according to the circuit architecture, which will be explained further in Section 2.2.

Comparisons between SDMs with NRZ DAC and FIR DAC

Table 2.2 shows the comparisons between the SDM with an NRZ DAC and a FIR DAC. They achieve the same specifications and share the same loop filters, so the propagation delay and

sampling frequency are equal for these two structures. With a reduced step size inversely proportional to the tap number N, the linearity required for the loop filter is relaxed and the sensitivity of the SDM to clock jitter diminishes. Idle tones generated with the small DC input are likewise smaller in architecture with the FIR DAC due to reduced discrepancies between the input and quantization output. The errors in the forward-path loop are also reduced with better filtering of quantization noise. The price paid for these advantages is that the STF peak of the structure with the FIR DAC is higher than that with the NRZ DAC due to the modified value of the coefficient. With additional circuits designed for the taps, the FIR DAC may occupy more area than NRZ DAC. As for power dissipation, the FIR DAC introduces an extra circuit but relaxes the requirements on the integrators, so the total power consumed by these two architectures cannot be decided before the transistor-level circuit simulation.

Table 2.2: Comparisons between SDMs with an NRZ DAC and a FIR DAC

	SDM with NRZ DAC	SDM with FIR DAC
Propagation delay	similar	
Power dissipation	undetermined	
Area	undetermined	
Sampling frequency	same	
STF peak	lower	higher
Step size in feedback waveform	2	2/N
Requirement for linearity of loop filter	more	less
Sensitivity to clock jitter	high	low
Normalized error in forward-path loop	1	less than 1
Idle tones	larger	smaller

2.2 System-Level Architecture Choices of CTSDM

Since the topology ultimately chosen for the CTSDM includes a FIR DAC feedback, as shown in Fig. 2.3, the architecture choices should be made based on this. According to the comparisons described in Section 2.1, one of the aspects where an SDM with a FIR DAC is inferior to that with an NRZ DAC is in the total area. Because a FIR DAC with N taps will occupy N times the area of an NRZ DAC, small-sized FIR DACs are required. The construction of main FIR DACs depends on the first-stage integrator, while the structure of compensation FIR DACs, mentioned in Section 2.1, is closely related to the second-stage integrator.

2.2.1 Second Integrator

Since the design of the second integrator requires less effort compared with that of the first stage integrator, which determines the input impedance and noise level of the system, the structure choices of the compensation FIR DACs and second integrator are first considered.

Active-RC integrators and switch capacitor (SC)-based integrators are both classic structures for the second stage in a CTSDM. If an active-RC integrator is used, the compensation FIR DACs should be resistive, as shown in Fig. 2.5. In addition to the virtual ground of the operational transconductance amplifier (OTA), these resistors form the coefficients of the compensated FIR DACs together with the integrating capacitor. The coefficients can be calculated as

$$a_i = \frac{1}{R_{fir,i} C_2 f_s},$$

where a_i denotes the i-th coefficient of the compensation FIR DACs, $R_{fir,i}$ denotes the value of the i-th FIR resistor, C_2 is the value of the integrating capacitor, and f_s is the sampling frequency. In SC-based integrators, however, capacitive compensation FIR DACs are added to form the coefficients with the integrating capacitors as:

$$a_i = \frac{C_{fir,i}}{C_2},$$

where $C_{fir,i}$ denotes the value of the i-th FIR capacitor.

Both configurations work for the desired integrator and feedback DAC with their own strengths. An active-RC integrator is a simple CT integrator without extra clocks or any KT/C noise generated by this sampling on the capacitor, like that in an SC-based integrator. In this design, however, the KT/C noise referred to the input will be largely suppressed due to the high gain of the first integrator. Thus, the use of an SC-based integrator will not increase the IRN either.

As previously established, area occupation is an important criterion for this design. The use of resistors in an active-RC integrator and resistive FIR DACs will lead to occupy a large area in the layout design. Nevertheless, sampling capacitors in an SC-based integrator and capacitive FIR DACs take up a smaller area.

Because the accuracy of FIR DAC coefficients is of vital importance to fully restore the noise shaping, as is the case with an NRZ DAC, mismatch between compensation FIR DACs needs to be avoided. The Process, Voltage, Temperature (PVT) variations of resistive FIR DACs values are much larger than capacitive FIR DACs values. Therefore capacitive FIR DACs are preferred for accuracy.

With smaller area occupation and less mismatch, an SC-based integrator with corresponding capacitive FIR DACs is preferred as they prevent an increase in the IRN.

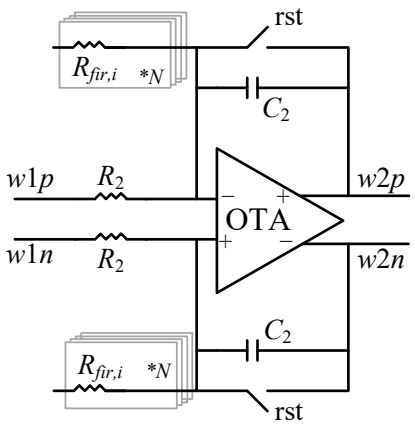

Figure 2.5: Active-RC integrator with resistive FIR DACs

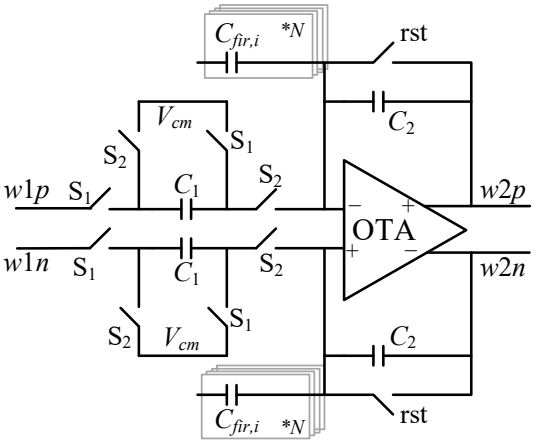

Figure 2.6: SC-based integrator with capacitive FIR DACs

Apart from the feedback point right before the quantizer, as shown in Fig. 2.6, the compensation FIR DACs could be added before the second integrator, as displayed in Fig. 2.7. The feedback capacitive FIR DACs still design coefficients with the integrating capacitors in an SC-based integrator but switches are needed to form the switch capacitor structures, as shown in Fig. 2.8. Mismatch between switches will introduce extra error. More switches also increase both the area occupation and wiring difficulties in layout design. Therefore, the compensation FIR DACs are added at the output of the second integrator and realized with capacitors directly connected to the virtual ground of the OTA.

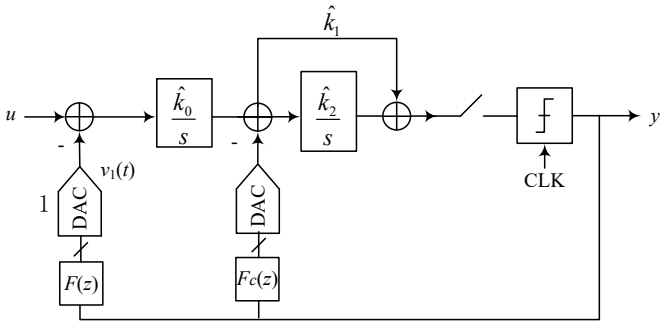

Figure 2.7: Another method to place a compensation FIR DAC

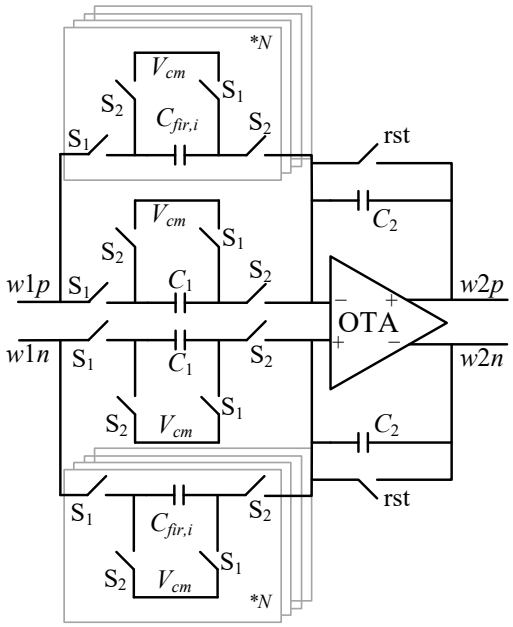

Figure 2.8: Feedback point at the output of the first integrator

2.2.2 First Integrator

Active-RC integrators are commonly used to realize integrated CT filters. They are largely insensitive to stray capacitances because equivalent capacitances neither at the virtual ground nor at the output of the opamp will affect integration. Providing an opamp with high gain and bandwidth enables this filter to achieve high performance [11]. Nevertheless, with a small input impedance, it will also bring about a large attenuation on the detected voltage signal. Assuming the voltage detected by the thermopile is V_s marked red in Fig. 2.9, the negative input of the active-RC integrator is:

$$V_0 = \frac{R_0}{R_s + R_0} V_s,$$

where R_s denotes the sensor resistance, and R_0 denotes the input resistance of an active-RC integrator. The input differential voltage of the integrator is $V_0 - 0 = V_0$. The input differential voltage is approximately V_s without a large signal attenuation only when the input impedance R_0 far outweighs R_s. Noises generated by R_0 will be large and directly referred to the input in an active-RC integrator, which leads to an excessively large IRN.

As mentioned in Section 1.4, the ROIC system in [14], which has high input impedance, can be used as a starting point for the first integrator implemented in the proposed CTSDM. Due to the integrators' open loop design, the Gm-C filters can operate at high speeds. To

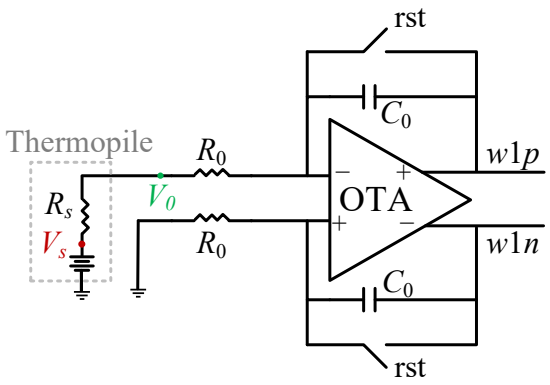

Figure 2.9: Thermopile with an active-RC integrator

achieve a given dynamic range, the power efficiency will be poor due to the superior linearity accompanied by significant excess noise [11]. Because parasitic capacitance exists in parallel with the integrating capacitors, Gm-C filters are susceptible to stray capacitance. Under these conditions, Gm-C integrators are used in applications requiring a low dynamic range, which corresponds with the targeted application for this design.

A CTSDM consisting of a Gm-C input, SC-based second integrator, and an N-tap FIR DAC along with its timing diagram is illustrated in Fig. 2.10. The output bitstream Dout of a single-bit quantizer controls the waveforms on feedback DACs after being processed by a D flip flop (DFF) chain, whose structure and design techniques will be explained in detail in Chapter 4. RDACs are firstly considered to be the main FIR DACs according to the design in [14] due to their simplicity. The feedback currents are decided by both the feedback point voltages V_{sp} and V_{sn} and the reference voltages V_{refp} and V_{refn}. Although the voltage at the feedback point can be designed to be stable, slight jitters in voltage will still bring about inaccurate feedback currents. IDACs providing stable currents are therefore used here.

Nonoverlapping clocks SCLK and QCLK define the integrator sampling and integration phases, respectively. This is necessary to avoid logic confusion. During the SCLK phase, integrator input is sampled and only signals on the feedforward path are integrated on C_2. Both charges on the sampling capacitors C_1 and feedforward capacitors C_3 are integrated during the integration phase, QCLK.

With a determined SC-based integrator as the second stage, however, a Gm-C input is not suitable for this situation. The sampling capacitors C_1 of the second stage are connected in parallel with the integrating capacitor C_{in} of the Gm-C input during the sampling phase. The integrating currents of the first stage will leak into C_1 and degrade the quantization noise modulation of the SDM.

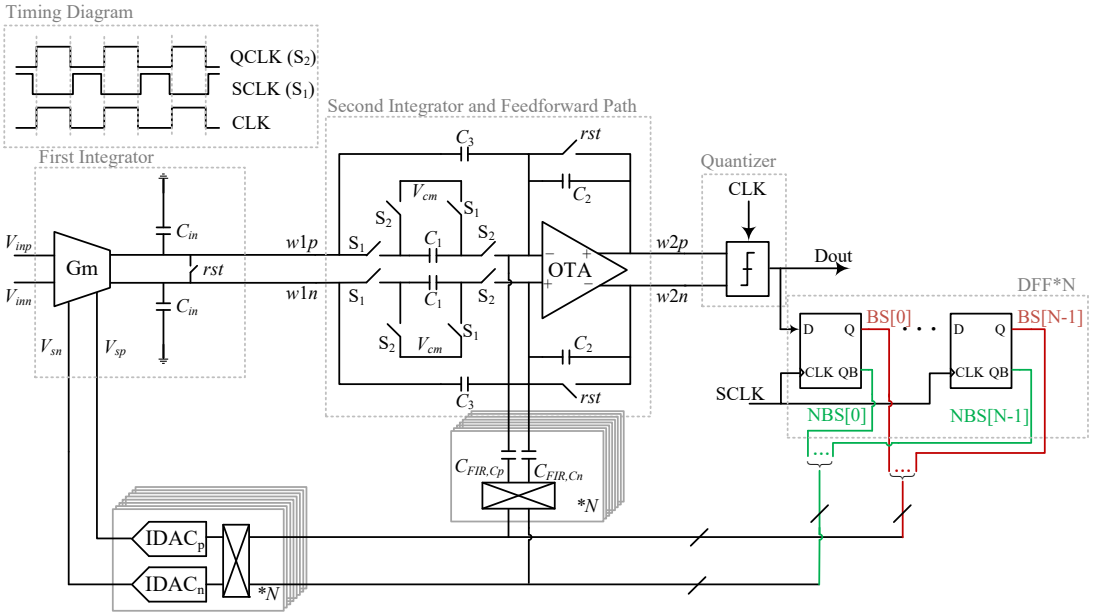

Figure 2.10: Prototype CTSDM with Gm-C input and FIR DAC

A Gm-OTA-C technique can be used to reduce the stray sensitivity compared with a Gm-C input. The OTA can be seen as a buffer which provides isolation to prevent current leakage during the sampling phase. It inherits the dynamic range problems of the Gm-C structure since the transconductance controls its noise and linearity [11]. Since a Gm-OTA-C integrator has an extra stage, it always consumes more power than a Gm-C integrator while covering the same dynamic range. Considering the accuracy of capacitive compensation FIR DACs and the complexity of the circuit design, a Gm-OTA-C structure is ultimately chosen as the first integrator. The final system level architecture is presented in Fig. 2.11.

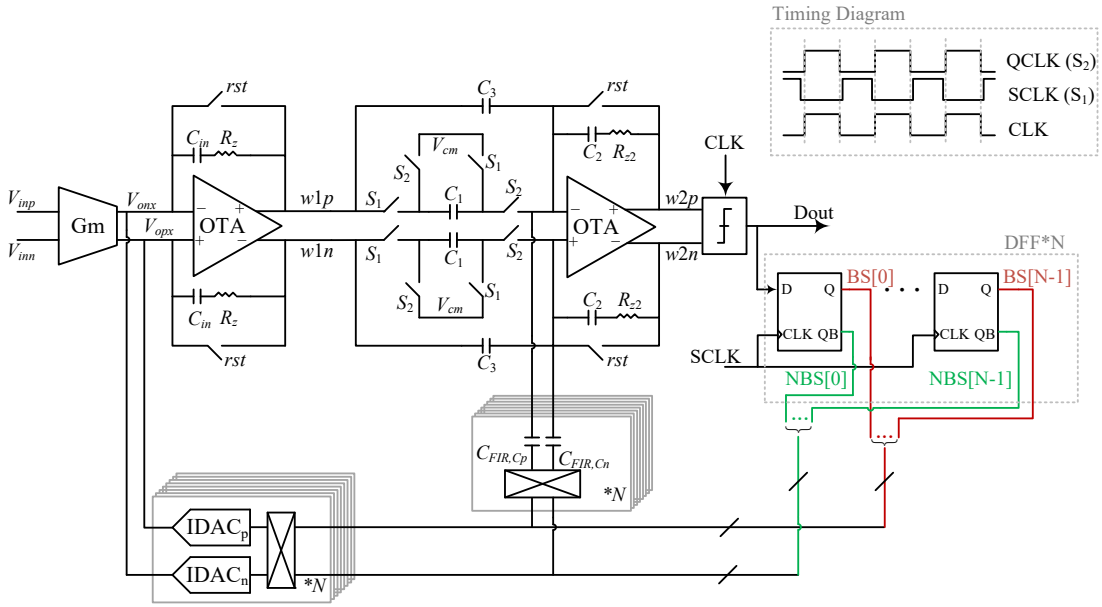

Figure 2.11: Determined CTSDM with a FIR DAC

3 Continuous-Time Sigma-Delta Modulator with a FIR DAC

Now that the system-level architecture of the proposed CTSDM has been decided, the design of FIR DACs is analyzed in this chapter. The design methods for a FIR DAC, choice of tap number and simulation results of the proposed CTSDM with a FIR DAC feedback are presented below.

A criterion for judging the design of a CTSDM with a FIR DAC is whether it can achieve the same specifications as the prototype with an NRZ DAC. In order to obtain the same Fast Fourier transform (FFT) and SNR, they need to have the same noise transfer function (NTF). The model and simulation results of the NRZ DAC are therefore needed as a reference for designing the coefficients of the FIR DAC.

Although the concept of the FIR DAC is not new, the realization of the compensation FIR DAC is still a fertile research field. The core idea behind deriving the expression of $F_c(z)$ is that the main FIR DAC and compensation FIR DAC can be used to realize a fully restored NTF. The NTF can be expressed as:

$$NTF = \frac{1}{1 + H(z)}, \tag{3.1}$$

where $H(z)$ denotes the total loop gain. The total loop gain is equivalent to the NTF, as long as $H(z)$ remains the same as that with an NRZ DAC, the NTF is restored.

The method in [16] uses step-response-invariant transformation to obtain revised forward-path coefficients ($\hat{k}_0$, $\hat{k}_2$) and the feedforward coefficient $\hat{k}_1$. The coefficients of compensation FIR DACs are calculated through mathematical deduction based on the loop gain equation. Instead of considering the loop gain in all frequency bands, [16] mainly focuses on low frequencies and highlighting fitting problems in this architecture. The methods in [17] and [18] both utilize impulse-invariant transformation (`c2d` function) for discretization. The FIR DACs' coefficients are determined by equating the undesired terms in [17], which requires a complex calculation process.

A simplified mathematical method and two image fitting methods without calculation are therefore proposed in Sections 3.1 and 3.2.

3.1 Design Methods: Least Squares Method

The modulator shown in Fig. 2.2 is the prototype structure. Although it is a continuous-time modulator, the input signal is converted to discrete time after being sampled by the quantizer. Therefore, the loop gain from y to the input of the quantizer, which is $k_0k_1/s + k_0k_2/s^2$ in the s-domain, can be discretized into the z-domain though a zero-order holder (ZOH) method; the relationship between the s-domain and the z-domain is shown in Table 3.1. In the z-domain, the total loop gain is given by:

$$k_0k_1H_1(z) + k_0k_2H_2(z) = \frac{1}{NTF} - 1. \tag{3.2}$$

Table 3.1: Discrete-Time Transfer Function for Each Path

Path	DT Transfer Function
$\frac{1}{s}$	$\frac{z^{-1}}{1-z^{-1}}$
$\frac{1}{s^2}$	$\frac{z^{-1}+z^{-2}}{2\left(1-z^{-1}\right)^2}$

Similarly, the total loop gain can be expressed in the z-domain for the modulator with the FIR DAC in Fig. 2.3. According to the core idea mentioned above, the equation can be formulated as:

$$k_0k_1H_1(z) + k_0k_2H_2(z) = \hat{k}_0\hat{k}_1F(z)H_1(z) + F_c(z) + \hat{k}_0\hat{k}_2F(z)H_2(z), \tag{3.3}$$

where the loop gains of both modulators are equated, and $\hat{k}_0$, $\hat{k}_1$, $\hat{k}_2$ denote the revised values of k_1, k_2, and k_3, respectively. Because it is expected that the NTF is exactly restored, (3.3) is established for the entire frequency band. Since the implementation of a compensation FIR DAC is similar to that of the main FIR DAC, the expression of $F_c(z)$ is similar to $F(z)$ except for the different weights between taps. For the convenience of readers, we provide the expression of $F_c(z)$ in (2.2) again:

$$F_c(z) = a_0 + a_1z^{-1} + a_2z^{-2} + \cdots + a_{N-1}z^{-(N-1)}, \tag{3.4}$$

where N denotes the number of taps in the FIR DAC, and a_i denotes the coefficient or weight on the $i-1$th tap ($i = 0, \cdots, N-1$). According to Table 3.1, (3.3) can be represented in detail

as:

$$\begin{aligned} k_0k_1\frac{z^{-1}}{1-z^{-1}}+k_0k_2\frac{z^{-1}+z^{-2}}{2(1-z^{-1})^2} =&\hat{k}_0\hat{k}_1\frac{1-z^{-N}}{N\left(1-z^{-1}\right)}\frac{z^{-1}}{1-z^{-1}} \\ &+F_c\left(z\right) \\ &+\hat{k}_0\hat{k}_2\frac{1-z^{-N}}{N\left(1-z^{-1}\right)}\frac{z^{-1}+z^{-2}}{2(1-z^{-1})^2}. \end{aligned} \tag{3.5}$$

To simplify the equation, all denominators are adjusted to $\left(1-z^{-1}\right)^3$. The numerators of the expressions can be given as:

$$N_{left}(z)=k_0k_1z^{-1}\left(1-z^{-1}\right)^2+\frac{k_0k_2}{2}\left(z^{-1}+z^{-2}\right)\left(1-z^{-1}\right), \tag{3.6}$$

$$\begin{aligned} N_{right}(z) =&\frac{\hat{k}_0\hat{k}_1}{N}\left(1-z^{-N}\right)z^{-1}\left(1-z^{-1}\right) \\ &+\left(a_0+a_1z^{-1}+\cdots+a_{N-1}z^{-(N-1)}\right)\left(1-z^{-1}\right)^3 \\ &+\frac{\hat{k}_0\hat{k}_2}{2N}\left(1-z^{-N}\right)\left(z^{-1}+z^{-2}\right), \end{aligned} \tag{3.7}$$

where $N_{left}(z)$ and $N_{right}(z)$ denote the total numerators of the adjusted equation on the left and right side. Using an undetermined coefficient method, the coefficients of the terms with corresponding orders on the left and right sides are equated. Linear equations can be derived by:

$$Ax=b, \tag{3.8}$$

where $A\in\mathbb{R}^{(N+3)\times(N+2)}$; $x=[\hat{k}_1',\hat{k}_2',a_0',\cdots,a_{N-1}']^\top\in\mathbb{R}^{(N+2)}$, where $\hat{k}_1'=\hat{k}_0\hat{k}_1$, $\hat{k}_2'=\hat{k}_0\hat{k}_2$, and $a'_i=\hat{k}_2a_i$, $i=0,\cdots,N-1$; $b\in\mathbb{R}^{(N+3)}$. Usually, b is in the image of matrix A so we can solve x precisely. Even though b is not just in the image space of A, we can derive the least-squares solution of x through the Moore-Penrose inverse of A.

Considering the choice of coefficients in real modulators, $\hat{k}_0$ and $\hat{k}_2$ can remain the same as k_0 and k_2 because they are both coefficients on a forward-path loop and contribute little to the compensation. With a known $\hat{k}_0$, $\hat{k}_1$ is proportional to $\hat{k}_1'$. $\hat{k}_1'$ can be regulated separately to reduce spikes on the output swing of the first integrator. Given the smooth edge of the swing, the stability of the system and the effectiveness of the feedforward path are ensured. Therefore, to improve the system of linear equations, $\hat{k}_1'$ is seen as a constant which can be adjusted according to the output swing of the first integrator. At this time, the dimension of the matrix and column vector changes: $A\in\mathbb{R}^{(N+3)\times(N+1)}$, $x=[\hat{k}_2',a_0',\cdots,a_{N-1}']^\top\in\mathbb{R}^{(N+1)}$. Again, using a similar method, we can determine accurate value for the coefficients a_i of $F_c(z)$.

3.2 Design Methods: Image Fitting

Although a simpler mathematical method is proposed in Section 3.1, formula derivation and matrix establishment differ from one architecture to another. A general approach using image fitting is thus proposed in this section. The principles of this approach and applications in the proposed CTSDMs are presented.

3.2.1 Implementation of Image Fitting

As clarified above, the designed CTSDM with a FIR DAC should exactly restore the NTF of its counterpart with an NRZ DAC. The principle behind image fitting is to make the impulse responses of loop filters with an NRZ DAC and FIR DAC equivalent, which is a necessary condition to exactly restore the NTF.

The NTF of a CTSDM is the transfer function from the output of the modulator through the feedback DAC and forward-path loop filters to the input of the quantizer. In the designed CTSDM, this path is shown in Fig. 3.1 for the prototype with an NRZ DAC, while Fig. 3.2 presents it in the SDM with a FIR DAC. An impulse is applied to the inputs of both the NRZ DAC and FIR DAC. Because the impulse function contains all frequencies, the impulse response defines the response of this system for all frequencies.

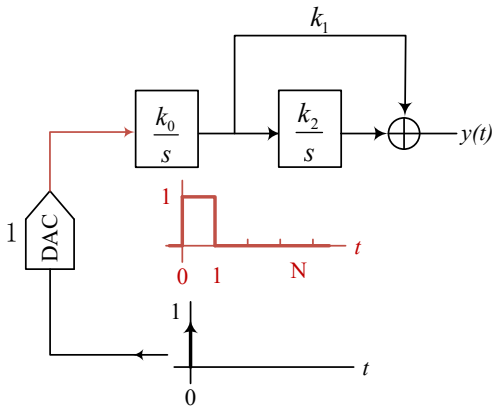

Figure 3.1: Determining the pulse response of the loop filter with an NRZ DAC

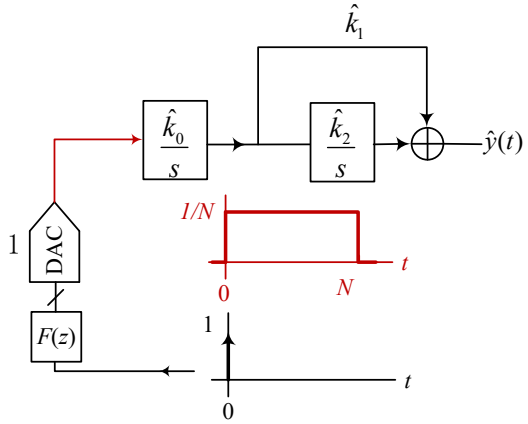

Figure 3.2: Determining the pulse response of the loop filter with a FIR DAC

After being convoluted by the pulse shape of the NRZ DAC, the DAC feedback waveform marked in red in Fig. 3.1 becomes a pulse shape of 1 second wide with a height of 1. $y(t)$ is

the time domain response of the NTF at the input of the pulse shape, which can be expressed as:

$$y(t) = \begin{cases} k_0 k_1 t + \frac{1}{2} k_0 k_2 t^2 & 0 \le t \le 1 \\ k_0 k_1 + k_2 k_0 t - \frac{1}{2} k_0 k_2 & t > 1 \end{cases} \tag{3.9}$$

Given the same input impulse, the feedback waveform of an FIR DAC with N taps marked in red in Fig. 3.2 is a pulse shape N wide with a height of $\frac{1}{N}$. Its impulse response $\hat{y}(t)$ can be expressed as:

$$\hat{y}(t) = \begin{cases} \frac{\hat{k}_0 \hat{k}_2}{2N} t^2 + \frac{\hat{k}_0 \hat{k}_1}{N} t & 0 \le t \le N \\ \hat{k}_0 \hat{k}_2 t - \frac{\hat{k}_0 \hat{k}_2 N}{2} + \hat{k}_0 \hat{k}_1 & t > N \end{cases} \tag{3.10}$$

Since the input impulse is the same, when $t > N$, $y(t) = \hat{y}(t)$, i.e.,

$$k_0 k_1 + k_2 k_0 t - \frac{1}{2} k_0 k_2 = \hat{k}_0 \hat{k}_2 t - \frac{\hat{k}_0 \hat{k}_2 N}{2} + \hat{k}_0 \hat{k}_1 \tag{3.11}$$

is a necessary condition for exactly the same NTF in a prototype with an NRZ DAC and its counterpart with a FIR DAC. Therefore the classic set of loop-filter coefficients $k_0 = k_2 = 1$ and $k_1 = 2$ is chosen. As mentioned above, the values of the revised coefficients can be chosen as $\hat{k}_0 = k_0 = 1$ and $\hat{k}_2 = k_2 = 1$. Through (3.11), we can obtain $\hat{k}_1 = \frac{N+3}{2}$.

With the chosen k_0, k_1, k_2 and revised coefficients, the impulse response of both loops can be derived from (3.9) and (3.10):

$$y(t) = \begin{cases} \frac{1}{2} t^2 + 2t & 0 \le t \le 1 \\ t + 1.5 & t > 1 \end{cases} \tag{3.12}$$

$$\hat{y}(t) = \begin{cases} \frac{1}{2N} t^2 + \frac{N+3}{2N} t & 0 \le t \le N \\ t + 1.5 & t > N \end{cases} \tag{3.13}$$

It is evident from (3.12) and (3.13) that the impulse responses of the two loops are the same when $t > N$ or $t = 0$. When $0 < t \le N$, however, it is impossible for $y(t)$ and $\hat{y}$ to be equal. That is to say, purely tuning $\hat{k}_0$, $\hat{k}_1$, and $\hat{k}_2$ is not enough to exactly restore the NTF. An extra compensation FIR DAC is therefore needed. Specifically, when the compensation FIR DAC is placed right before the quantizer, the coefficients of the compensation FIR DAC in (3.4) are exactly the difference between $\hat{y}(t)$ and $y(t)$ when $t \le N$, i.e.,

$$[a_0,\ a_1,\ \ldots,\ a_{N-1}] = [y(1) - \hat{y}(1),\ y(2) - \hat{y}(2),\ \ldots,\ y(N) - \hat{y}(N)]. \tag{3.14}$$

Assuming the tap number is $N = 8$, the calculated result of the coefficients of the compensation FIR DAC is

$$[a_0,\ a_1,\ a_2,\ a_3,\ a_4,\ a_5,\ a_6,\ a_7] = [1.75, 1.875, 1.875, 1.75, 1.5, 1.125, 0.625, 0].$$

For the ease of explanation and comparisons, the subsequent derivations and methods both use $N = 8$ as a prerequisite.

3.2.2 Fitting Models in Simulink

The implementation method of image fitting can be applied in Simulink models to reduce manual calculation. The fitting models built in Simulink for the forward-path loop filter with an NRZ DAC and an 8-tap FIR DAC with $k_0 = k_2 = 1$ and $k_1 = 2$ are presented in Figs. 3.3 and 3.4, respectively. y in Figs. 3.3 and y_fir in Fig. 3.4 are the impulse responses.

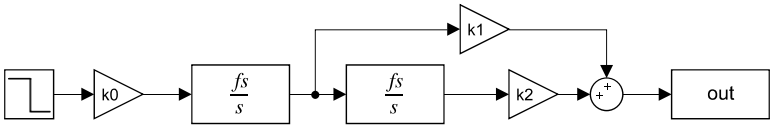

Figure 3.3: Fitting model of a forward-path loop filter with an NRZ DAC

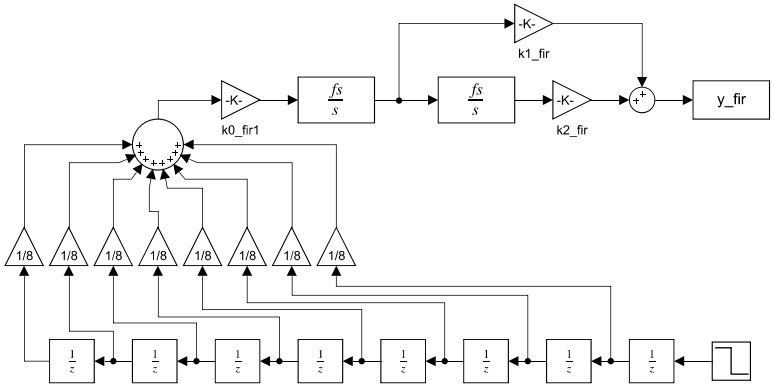

Figure 3.4: Fitting model of a forward-path loop filter with a FIR DAC

k0_r, k1_r, and k2_r denote the $\hat{k}_0$, $\hat{k}_1$, and $\hat{k}_2$ in Fig. 3.2. $\hat{k}_0$ and $\hat{k}_2$ can be kept the same as k_0 and k_2 as mentioned above. $\hat{k}_1$ can be chosen according to the fitting image in Fig. 3.5 to make the impulse responses y and y_fir coincide when $t > N$. When $\hat{k}_1 = 5.5$, y is equivalent to y_fir after the 9th sample, although the impulse responses are not the same for the first 8 samples in Fig. 3.5. In particular, the first sample corresponds to $t = 0$, the second sample corresponds to $t = 1$, and so on. A compensation FIR DAC is therefore needed to compensate

for the difference between y and y_fir. The coefficients of this compensation FIR DAC are the values of y - y_fir at each sample. The coefficients obtained in this Simulink fitting model are identical to those calculated in Section 3.2.1.

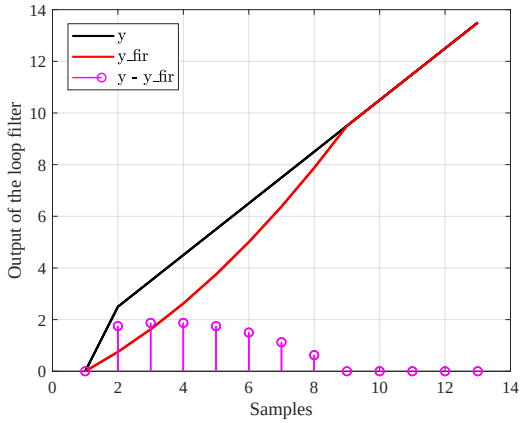

Figure 3.5: Subtraction of two impulse responses

3.2.3 Fitting Models in Cadence

Fitting models can also be built in Cadence with the support of ideal models. Similar to methods in Section 3.2.1 and 3.2.2, an impulse is given to the inputs of both an NRZ DAC and a FIR DAC. The impulse responses out and out_fir are plotted and the difference is displayed in Fig. 3.6.

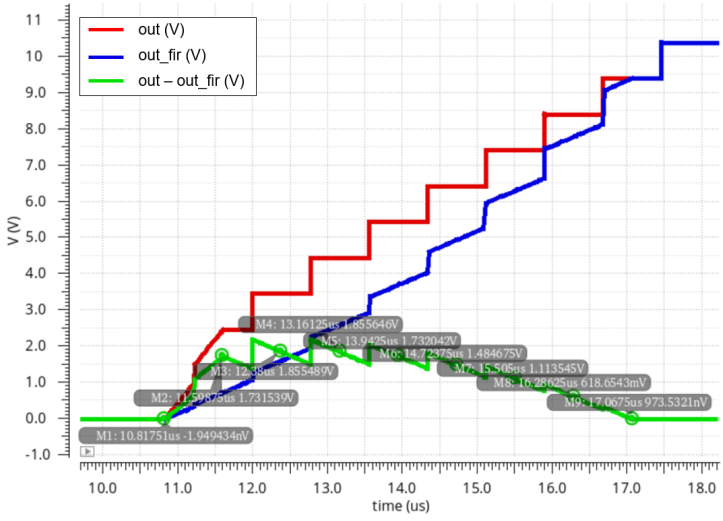

Figure 3.6: Fitting results in Cadence

The impulse responses are not given by the same straight lines as found in Fig. 3.5 but by lines with steps caused by the DT second integrator. When the second integrator is in the sampling phase, the integrating capacitors are charging while the impulse response remains the same. The impulse response jumps at the beginning of the integrating phase. In the loop filter with the NRZ DAC, the impulse given to the input of the first integrator lasts for only one clock sampling phase. The width of the impulse given to the loop filter with the FIR DAC is 8 sampling clocks, so the jumps in out_fir are superimposed on a linear result due to first-order integration.

$\hat{k}_0$ and $\hat{k}_2$ are still kept the same as k_0 and k_2. $\hat{k}_1$ is also chosen according to the fitting result in Fig. 3.5 to make the impulse responses out and out_fir match when $t > 8$. In this fitting model, $\hat{k}_1$ is still 5.5. The coefficients of the compensation FIR DAC obtained with the fitting models in Cadence are approximately

$$[a_0,\ a_1,\ a_2,\ a_3,\ a_4,\ a_5,\ a_6,\ a_7] = [1.75, 1.85, 1.85, 1.75, 1.5, 1.1, 0.625, 0],$$

which are mostly identical to those achieved with the calculation and models in Simulink.

3.3 Choice of Number of Taps in the FIR DAC

Because a longer FIR DAC contributes to better filtering of quantization noise, a preliminary conclusion is made that increasing the tap number N could reduce the magnitude of the error signal $e(t)$ in Fig. 2.3. The z-domain expression of the error signal is:

$$\begin{aligned} E(z) &= u(z) - F(z)y(z) \\ &= u(z) - F(z)\left[NTF(z)Q(z) + STF(z)u(z)\right] \\ &= -F(z)NTF(z)Q(z) + \left(1 - F(z)STF(z)\right)u(z), \end{aligned} \tag{3.15}$$

where quantization noise (shaped and filtered) and the input component both influence the error signal. With an increased N, shaped and filtered quantization noise contributes to a smaller peak magnitude of $e(t)$. However, $1 - F(z)STF(z)$ increases with a larger N, which means that the $e(t)$ will not decrease infinitely with an increase in N. Too many taps also involve more IDACs and capacitive compensation FIR DACs, leading to more power consumption. A trade-off between $e(t)$ and the tap number is, therefore, needed.

Fig. 3.7 shows that the simulation results of peak magnitude of $e(t)$ decrease with an increasing tap number N. Considering $e(t)$, power consumption, and area occupation, a tap number of $N = 8$ is chosen for this design. The final architecture of the CTSDM with 8-tap FIR DACs is shown in Fig. 2.11. Note that a DFF chain is formed by 8 DFFs to provide the control signals $BS[0:7]$ and $NBS[0:7]$ for both main and compensation FIR DACs.

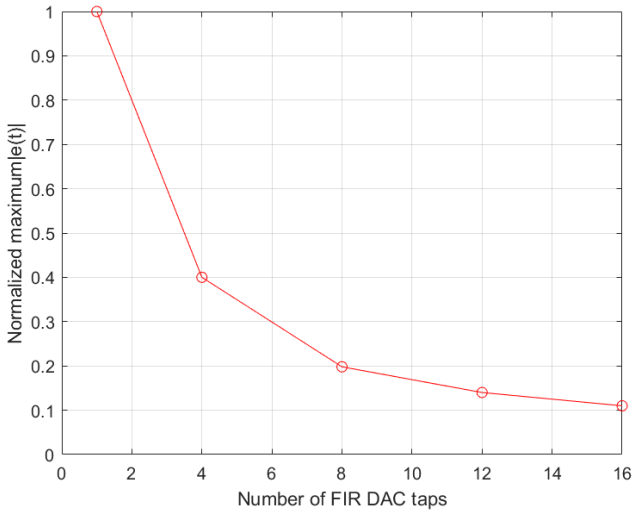

Figure 3.7: Peak magnitude of the error signal exciting the input integrator versus the number of taps in the main FIR DAC

3.4 Choice of Methods and Simulation Results

3.4.1 Simulation results

Although the revised coefficients of the forward-path loop are the same in all three methods, the coefficients of the compensation FIR DAC obtained in these methods are not identical. The coefficients obtained through calculation and fitting models in Simulink are exactly the same, whereas those achieved through fitting models in Cadence differ slightly.

In order to verify whether these two sets of coefficients will affect the main circuit performance, the coefficients are used to build two second-order CIFF CTSDMs, but with different compensation FIR DACs using ideal models in Cadence. An FFT of the prototype with an NRZ DAC is also performed as a reference for that with a FIR DAC. A well-designed CTSDM with a FIR DAC should have the same FFT result as that with an NRZ DAC.

Given a $113Hz$ sinusoid with an amplitude of 0.6, the FFT results of the modulators built using ideal modules with an NRZ DAC and FIR DAC with coefficients obtained from different methods are presented in Fig. 3.8. Considering the targeted sensing application, f_b can be chosen as $400Hz$. Since the simulated SQNR is 129.5dB, which is larger than 102dB, it meets the requirement for ENOB. We can conclude from the simulation results that as long as the change in the coefficients of the compensation FIR DAC is smaller than 1%, it will not affect

the performance of the modulator. The FFT results of the CTSDM with a FIR DAC is equal to that with an NRZ DAC, so the FIR DACs are well designed.

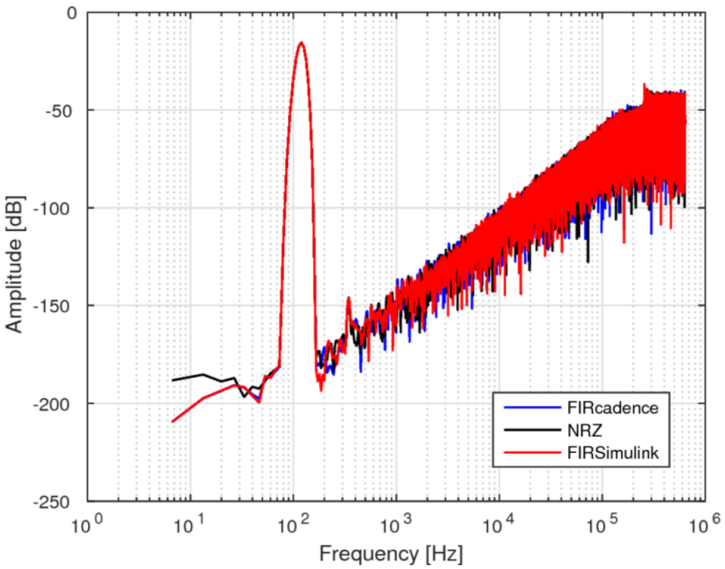

Figure 3.8: FFT results of modulators with an NRZ DAC and FIR DAC

3.4.2 Comparisons between Different Methods

In [16], the method to derive the function of $F_c(z)$ shares the idea with the proposed method of equating the total loop gain of both modulators with the NRZ DAC and FIR DAC. Instead of considering the loop gain in all frequency bands, [16] mainly focuses on low frequencies and it will bring about both a move in the FFT result and a degraded SNR. The method put forward in Section 3.1 solves this problem and achieves a targeted FFT result. Another advantage of the proposed mathematical method is the simplified calculation process because complex matrix calculations can be done with tools. Also, the choice of feedforward coefficient is more adjustable to cater to the requirements of circuit design. The limitation of this method is that sometimes the least-squares solution is not accurate enough to restore the NTF exactly.

Three image fitting methods are proposed in Section 3.2 to compensate for this problem. All three methods can achieve proper coefficients for a compensation FIR DAC. The results of calculation and fitting models in Simulink are identical to each other. Using fitting models avoids mistakes that may appear in manual calculations. The fitting model built in Simulink is also easier than that in Cadence. Only blocks presenting CT or DT integrators are needed, while specific circuit structures are not illustrated.

Although the image fitting in Cadence should be used after the system-level design of a prototype CTSDM with an NRZ DAC is finished, fitting models in Cadence are ultimately chosen for this design. Because the fitting is carried out between the models built in real circuit structures with ideal modules, the coefficients obtained will most closely resemble those of real circuits. Another advantage of this method is that coefficients can first be fitted again by replacing the ideal modules with real circuits and then revised after the circuit level design is finished.

4 Circuit Implementation

As discussed in Chapters 2 and 3, a CTSDM with Gm-OTA-C input is the chosen architecture to realize a high input impedance for the input stage. The linearity and noise analysis of this stage are worth considering since they are determined by the transconductor. Feedback IDACs are also designed to provide stable feedback currents.

In this chapter, the implementation of the proposed high input impedance CIFF CTSDM with FIR DAC feedback is described, and design techniques are investigated. The layout design and post-layout simulation results are also demonstrated.

4.1 Circuit Designs

4.1.1 Input Integrator

Figure 4.1 shows the schematic of the proposed Gm-OTA-C integrator, which is composed of a two-stage amplifier and integrating capacitors. The input stage determines the input impedance and noise level of the whole system, so the circuit design will be discussed to highlight these key characteristics.

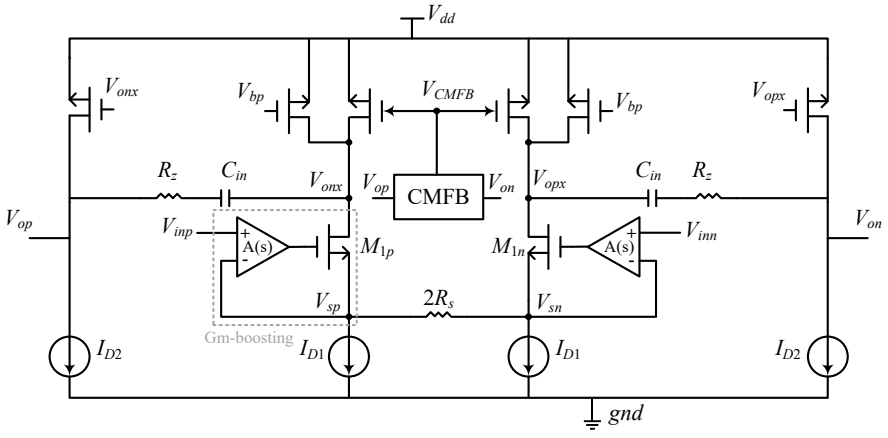

Figure 4.1: High input impedance Gm-OTA-C first integrator

Gm Cell with Input Gm-boosting

The first-stage amplifier of the first integrator is a Gm cell with resistive source degeneration and input Gm-boosting. These techniques, based on [14], provide a high input impedance and high linearity for the whole system.

Resistive source degeneration is the simplest linearization method to solve the problems caused by the variations in the transconductance of the input transistors at the input level. Taking the common-source stage with resistive degeneration in Fig. 4.2 as an example, the effective transconductance of the stage is:

$$G_m = \frac{g_{m0}}{1 + g_{m0} R_s}. \tag{4.1}$$

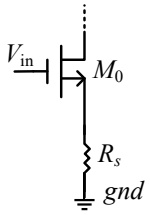

Figure 4.2: Common-source stage with resistive degeneration

If the $g_{m0}R_s$ is much larger than 1, Eq. (4.1) can be simplified to $G_m = 1/R_s$, which is relatively constant. The voltage gain of this stage, $Av = G_m R_{out}$, is therefore independent of the input level with a stable transconductance. Given the determined current flowing through M_0, the source degeneration resistance also increases the input range by $1 + g_{m0}R_s$. The signal current generated by the effective transconductance is $I_{out} = G_m V_{in}$, which decreases with the increase in R_s. R_s is related to the saturation current flowing through M_0, which further affects the power consumption. Meanwhile, R_s is an important input-referred noise source. Thus, the use of resistive degeneration, R_s, is a trade-off between linearity, noise, power dissipation, and gain [19].

A larger R_s results into higher linearity at the cost of poor noise performance and more area occupation. In order to further optimize the linearity without increasing the input-referred noise dramatically, Gm-boosting cells are added to the input pairs $M_{1p,n}$ as shown in Fig. 4.1. The Gm-boosting cells are high-gain amplifiers with a voltage gain of $A(s)$. The differential input is connected to the positive inputs of both Gm-boosting cells. Their negative inputs are connected to the drains of the input pairs V_{sp} and V_{sn} and form negative feedback loops. The output of the Gm-boosting cells are connected to the gate of the input pairs. Assuming a slight change ΔV in V_{inp}, the negative input of the Gm-boosting cell V_{sp} will not change immediately. The input connected to the gate of M_{1p} will increase by $A(s)\Delta V$ and lead to the

same increase in V_{gs}. In order to keep the current I_{D1} flowing through M_{1p}, V_{gs} will decrease by an increased V_{sp}. In other words, the drain voltages of the input pairs will duplicate the change in differential input. Therefore, a Gm-boosting cell and an input transistor function as a transistor with an increased transconductance, $g_{m1}A(s)$. The total effective transconductance of the first integrator can be modified as:

$$G_{m,eff} = \frac{g_{m1}A(s)}{1 + g_{m1}A(s)R_s} \approx \frac{1}{R_s}. \tag{4.2}$$

With a g_{m1} enhanced by $A(s)$, $G_{m,eff}$ is decided by a relatively small R_s. This structure achieves high linearity while ensuring low noise introduced by source degeneration.

As for the design of the Gm-boosting cell, several essential metrics need consideration: 1) ***Gain*** In order to guarantee that $g_{m1}A(s)R_s$ is much larger than 1, a folded cascode OTA is chosen to achieve a high-gain amplifier, as shown in Fig. 4.3; 2) ***Speed*** The amplifier response should be fast enough to allow V_{sp} and V_{sn} to follow the input signal; 3) ***Stability*** The Gm-boosting cell should ensure the stability of the negative feedback loop. Since the Gm-boosting cell forms a negative feedback loop at the input, the voltage gain and stability response of it in the feedback loop is simulated instead of a single OTA. The feedback loop is broken by an Iprobe to perform the stability (stb) analysis, which is shown in Fig. 4.4. With an $A(s)$ larger than $80dB$, $g_{m1}A(s)R_s$ is guaranteed to be much larger than 1, which helps good linearity to be achieved. The negative feedback loop is also stable with a 59° phase margin. In transient simulation, the voltage at the negative input of the Gm-boosting cell V_{sp} changes with the input signal, as shown in Fig. 4.5, which means the OTA is fast enough for V_{sp} and V_{sn} to follow the input signal.

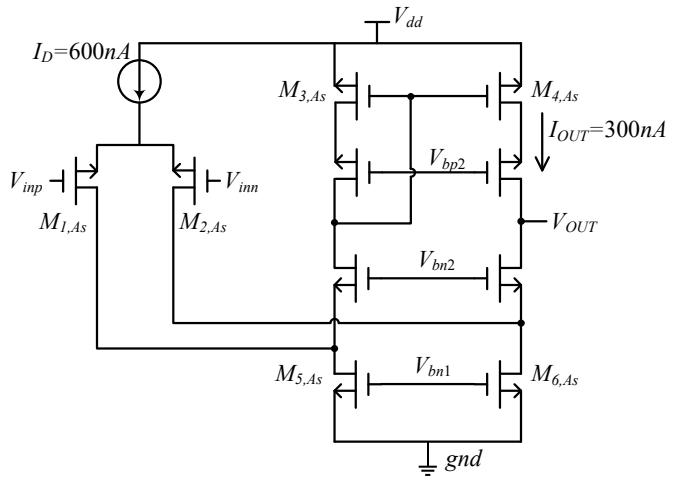

Figure 4.3: Circuit diagram of the amplifier used for Gm-boosting

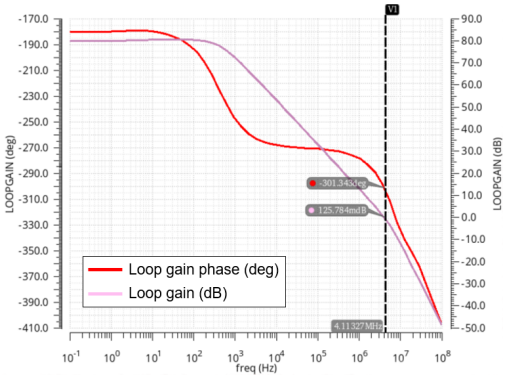

Figure 4.4: Frequency response of the feedback loop

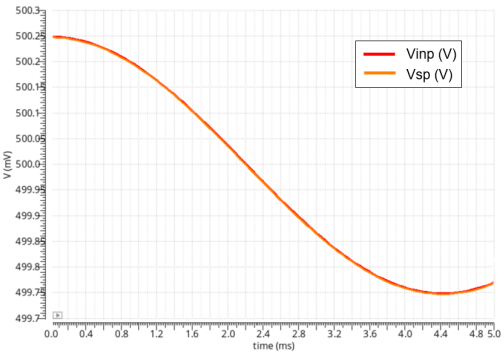

Figure 4.5: V_{sp} changes with V_{inp}

The bulks of the input PMOS transistors $M_{1,As}$ and $M_{2,As}$ are connected directly to their sources to reduce body effect, in turn reducing the threshold voltage (Vth) and improving the input common-mode range. They also improve the linearity and CMRR performance[14]. The gain-bandwidth product (GBW) can be calculated as $GBW = \frac{g_m}{2\pi C_L}$ which should be large enough to ensure that V_{sp} and V_{sn} follow the input signal. The GBW is only affected by the transconductance of the input transistors and the load capacitances, which are the capacitances equivalent to the gates of M_{1p} and M_{1n} in Fig. 4.1. With M_{1p} and M_{1n} having been decided and the input PMOS working in the weak inversion region, the input current is simulated and determined to be $300nA$. Within the signal BW of $400Hz$, it is simple to maintain the voltage gain above $80dB$. The cascode currents flowing through $M_{3,As}$ and $M_{4,As}$ are therefore allowed to be $300nA$ so as to reduce power consumption.

Common-Mode Feedback Circuit

In Fig. 4.1, V_{op} and V_{on} are the differential output of the Gm-OTA-C integrator. A CMFB circuit is used to maintain the output CM voltage of the fully differential opamp at a constant level so that the output swing can achieve maximum symmetry. Existing types of CMFB circuits are the resistor averaging circuit (R-C), switched-capacitor averaging circuit, and differential difference amplifier (DDA) [20]. Because SC CMFB circuits are sensitive to clock jitter noise, they are not suitable for use in oversampling systems. Resistor averaging CMFBs and R-C CMFBs are first considered for this opamp due to their uncomplicated circuit design. Large resistors help achieve high CM detection accuracy but occupy too much area. The DDA CMFB in Fig. 4.6 is therefore chosen for this opamp which occupies a smaller area. Differential input pairs are used to sense and compare the output voltages of the first stage with the reference voltage V_{biascm}. Proportional currents generated according to the detected voltages mirror the main amplifier through V_{CMFB} and, in turn, modulate the values of V_{on} and V_{op}. Since a Gm-

OTA-C integrator cannot handle a wide signal range, DDA CMFB with a limited linear signal range for the main amplifier can be chosen for this design.

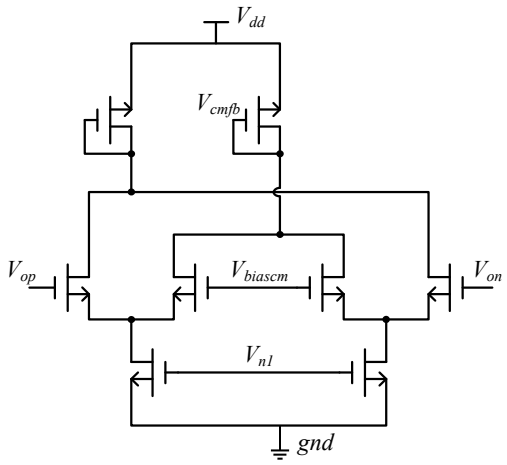

Figure 4.6: Schematic of the DDA CMFB circuit

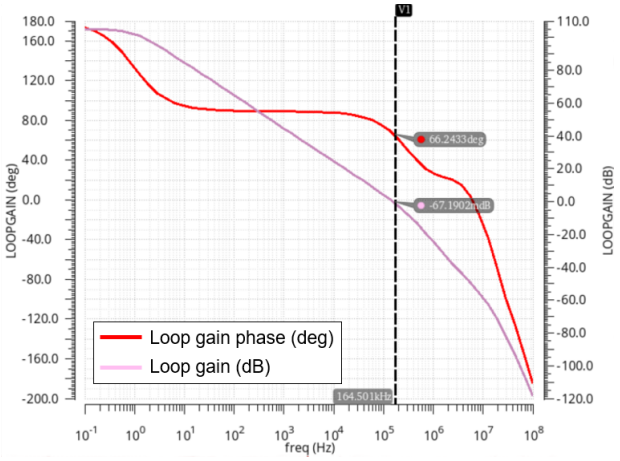

Figure 4.7: Frequency response of the CM loop

The two differential input pairs in the CMFB circuits use *nmosnvt2v* to detect the output and compare them with the reference voltage. These NMOS transistors are native transistors with a nearly zero Vth, which guarantees enough headroom for other transistors work correctly. The output voltage of the CMFB circuit V_{cmfb} only controls some of the transistors used for upper tail current sources in the main amplifier, as shown in Fig. 4.1. The CMFB circuit saves currents by controlling only some of the transistors instead of all of them. With more transistors controlled by the CMFB circuit, the CM loop gain will increase but the stability

margin decreases. The ratio of the number of transistors controlled by the CMFB and by biasing is determined to be 4:2. Figure 4.7 shows the frequency response of the CM loop, which achieves a DC gain of $102dB$ with a phase margin of 66°.

OTA Design

A second-stage OTA is designed in the first integrator to isolate the integrating capacitors C_{in} and the sampling capacitors of the second integrator. A common-source amplifier is connected to the outputs of the first-stage opamp which gives the differential outputs of the first integrator. Because V_{sp} and V_{sn} need to follow the changes in the input signal, V_{onx} and V_{opx} have to reserve a sufficient margin for them to change. With an input common-mode voltage of $500mV$ and input range larger than $50mV$, $V_{sp}(V_{sn})$ will reach a value larger than $550mV$. The common-mode voltage at virtual ground is finally designed to be $V_{cm,vg} = 850mV$ according to simulation results. It is realized by regulating the number of multipliers of the transistors working as tail-current sources for the second stage. Since the supply voltage is $V_{dd} = 1.5V$, PMOS transistors are used as the input of the second stage to provide enough headroom for the tail-current sources.

Two capacitors with a value of C_{in} are connected between the output of the first stage and the output of the second stage, which is also the feedback path of the Gm-OTA-C integrator. They serve as both integrating capacitors and Miller compensation capacitors. The value of C_{in} is determined by $k_0 = 1$, $f_s = 1.28MHz$, and $R_s = 50k\Omega$, which is related to input-referred noise and is chosen based on the value in [14]:

$$C_{in} = \frac{k_0}{f_s R_s} = \frac{1}{1.28M \times 50k} = 15.625pF.$$

Miller compensation capacitors move the dominant pole to low frequencies and move non-dominant poles to high frequencies to achieve pole separation at the cost of introducing a right-half plane zero. In the feedback path of the Gm-OTA-C integrator, an additional resistor is connected in series with the integrating capacitor to eliminate the right-half plane zero. The transfer function of the whole integrator is:

$$H(s) = \frac{V_{op} - V_{on}}{V_{inp} - V_{inn}} = \frac{2G_{m,eff}A_1}{sC_{in}(A_1 + 1)} + \frac{2G_{m,eff}(A_1 R_z - R_{o2})}{A_1 + 1}, \tag{4.3}$$

where A_1 and R_{o2} denote the voltage gain and the on-resistance of the second stage amplifier, separately. The theoretic value of the compensation resistor is:

$$R_z = \frac{R_{o2}}{A_1} \approx 6k\Omega$$

After adjusting the resistance value according to the actual simulation results, $R_z = 11k\Omega$ is finally used to cancel the right-half plane zero. The frequency response of the first integrator is

shown in Fig. 4.8. The phase shift is 90° at a sampling frequency of $1.28MHz$, so the integrator will be stable and operate well in the CTSDM [21]. Specifically, extra zeros introduce upturn in both the phase and gain images. Since the upturn appears at a frequency larger than $10MHz$, it will have no influence on the CTSDM working at $1.28MHz$.

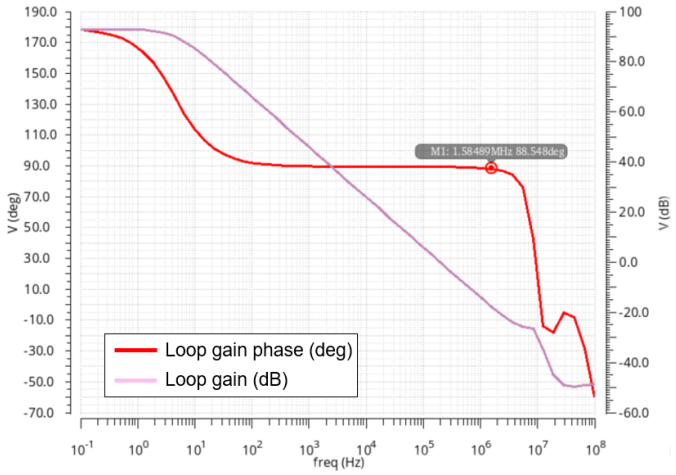

Figure 4.8: Frequency response of the first integrator

Noise Analysis

Being the first stage, the first integrator defines the noise level of the whole ROIC. Each noise source and what it contributes is analyzed in this section. An equivalent half circuit of the Gm-OTA-C for noise calculation is shown in Fig. 4.9.

$$\begin{aligned} v_{n,tot}^2 = v_{n,A(s)}^2 &+ \frac{v_{n,M1}^2}{A_v^2} \\ &+ \frac{i_{n,Rs}^2 R_{out}^2 + v_{1/f,M2}^2 + i_{n,M2}^2 R_{out}^2 + v_{1/f,M3}^2 + i_{n,M3}^2 R_{out}^2}{A_v^2} \\ &+ \frac{v_{1/f,M4}^2 + i_{n,M4}^2 R_{out2}^2 + v_{1/f,M5}^2 + i_{n,M5}^2 R_{out2}^2}{A_v^2 A_{v2}^2}, \end{aligned} \tag{4.4}$$

where A_v denotes the voltage gain of the first-stage amplifier of the Gm-OTA-C.

1) M_1, M_4, and M_5: Since the thermal noise and $1/f$ noise of M_1 are suppressed by A_v^2, the input-referred noise of M_1 is negligible. Similarly, the thermal noise and $1/f$ noise of M_4 and M_5 are suppressed by both A_v^2 and A_{v2}^2 so the noise generated by them can be ignored.

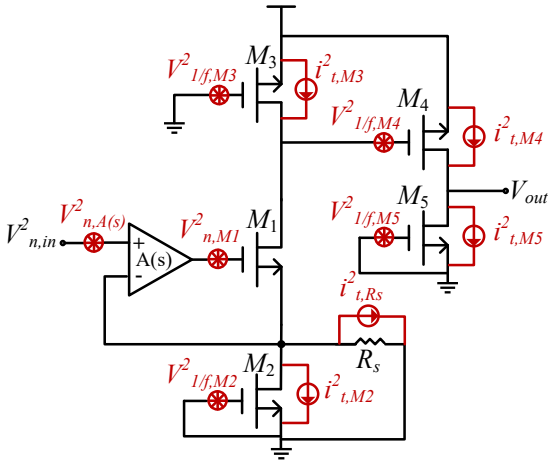

Figure 4.9: Equivalent half circuit of the input stage for noise calculation

2) M_2 and M_3: The input-referred thermal noise and $1/f$ noise of the current sources M_2 and M_3 can be expressed as:

$$v^2_{n,th,cs} = \frac{4kT\gamma\,(g_{m2}+g_{m3})}{G^2_{m,eff}} = \frac{4kT\gamma R_s\,(g_{m2}+g_{m3})}{G_{m,eff}} \tag{4.5}$$

$$v^2_{n,1/f,cs} = \frac{Kg^2_{m2}}{fC_{ox}(LW)_2 G^2_{m,eff}} + \frac{Kg^2_{m3}}{fC_{ox}(LW)_3 G^2_{m,eff}} \tag{4.6}$$

The ratio $g_{m2,3}/G_{m,eff}$ should be minimal enough to limit the noise contribution from the current sources. M_2 and M_3 should operate in strong inversion so they have a large width and small transconductance.

3) R_s: For the noise of degeneration resistor R_s, the input-referred noise is calculated to be $2.88\mu V_{rms}$.

4) $A(s)$: Since the noise of the Gm-boosting cell is directly referred to the input, it is the dominant noise source. To reduce the $1/f$ noise contribution, the cascode currents of $A(s)$ are raised to $300nA$ from $100nA$ so as to increase the size of cascode transistors. Current sources in the Gm-boosting cell ($M_{3,As-6,As}$) also have a large size and small transconductance and work in strong inversion, so that both the thermal noise and flicker noise of each are minimized. The simulated results of the noise contributions of these noise sources are shown in Fig. 4.10. The total input-referred noise of the first stage is simulated to be $32.5\mu V_{rms}$ integrated over $2.5kHz$ signal BW.

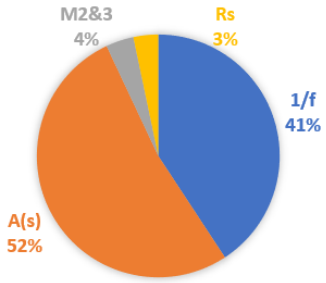

Figure 4.10: Simulated noise contribution of each noise source

4.1.2 Second Integrator

As mentioned above, the second stage of the CTSDM employs an SC-based integrator. High gain and high input impedance are required for the opamp used in this integrator, so the common folded-cascode amplifier shown in Fig. 4.11 is chosen. Both the input current and the cascode current are set at $300nA$ to reduce power dissipation while maintaining the high gain and stability. The folded-cascode amplifier also needs CMFB to reduce output asymmetry due to the fully differential structure. The same DDA CMFB cell as applied to the first integrator is utilized, but the proportion of the number of transistors controlled by the CMFB and by the bias is changed to 2:4 to stabilize the CM loop.

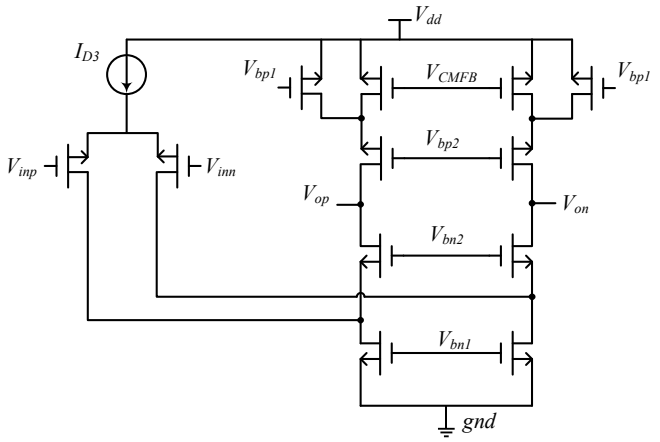

Figure 4.11: Schematic of the opamp used in the second integrator

As shown in Fig. 2.11, resistors with a value of R_{z2} are connected in series with the integrating capacitors. They are used to remove the right-half plane zero point to increase the phase margin of the integrator. Since the SC integrator is a discrete-time integrator, PSS and PAC simulations are run to obtain the AC performance of the second integrator. Fig. 4.12 shows

the frequency response of the second integrator. With a phase shift of nearly 90° at a sampling frequency of $1.28MHz$, the integrator will also work well in the CTSDM.

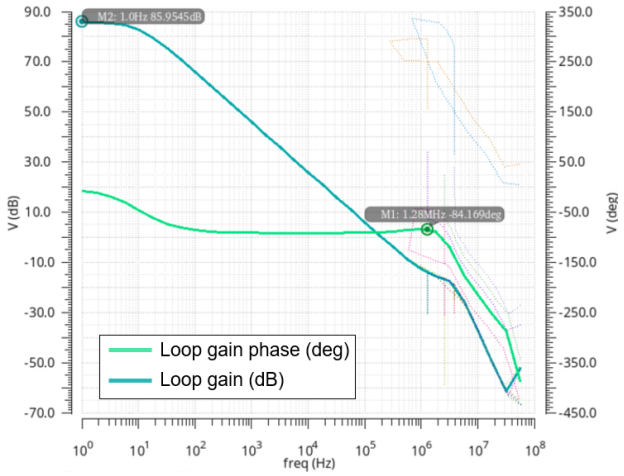

Figure 4.12: Frequency response of the second integrator

4.1.3 IDACs

As shown Fig. 2.11, main FIR DACs are connected to the virtual ground V_{onx} and V_{opx} of the Gm-OTA-C. The currents flowing through the first stage will be analyzed in detail to clarify the working principle of the IDACs.

The 8-tap main FIR DACs are controlled by the output of the DFF chain $BS[0:7]$ and $NBS[0:7]$. Since $BS[n]$ and $NBS[n]$ are outputs of the positive and negative output of the nth DFF respectively, their waveforms are completely inverted. When $BS[n] = 1$, the nth IDAC will inject a stable current I_{idac} into the feedback point V_{onx}. Conversely, the current will be drawn from V_{onx}. For $BS[0:7] = 1$, Fig. 4.13 shows the current directions around V_{onx} and V_{sp}. According to Kirchhoff Circuit Laws, the currents flowing through V_{onx} and V_{sp} can be expressed as:

$$I_{idac} + I_{D1} = I_{cin} + I_{M0},$$
$$I_{M0} = I_{Rs} + I_{D1},$$

where I_{cin} is the integrating current, I_{D1} and I_{idac} are stable currents, I_{M0} is larger than 0 because the current flows from source to drain, and I_{Rs} is determined by the node voltages around the resistor:

$$I_{Rs} = \frac{V_{sp} - V_{sn}}{2R_s}.$$

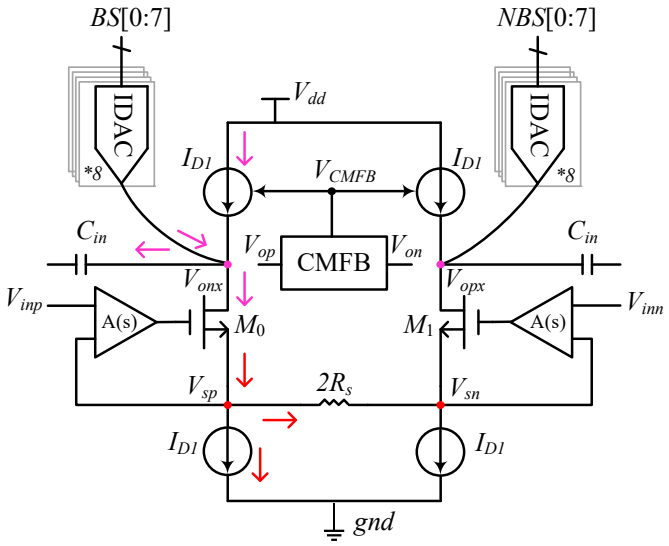

Figure 4.13: First stage of the CTSDM with integrating capacitors and feedback IDACs

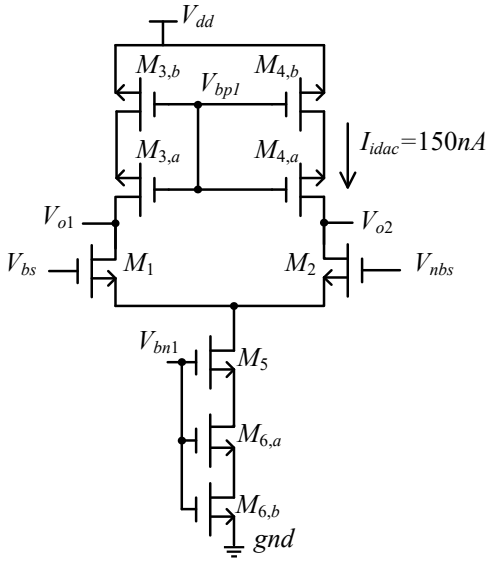

Figure 4.14: The schematic of IDAC circuit

The IDAC circuit is designed as shown in Fig. 4.14 to provide stable feedback currents. $M_{3,ab}$, $M_{4,ab}$, and $M_{6,ab}$ all comprise two transistors connected in series to increase the total length of the effective transistor. Increased length helps reduce the transconductance of these transistors and makes them work in the strong inversion region, which is the working region for transistors serving as current sources. M_5 is the cascode transistor used to copy currents from

the biasing circuit more accurately and further ensures the accuracy of I_{idac}. To this end, a $nmosnvt2v$ transistor with a small Vth is chosen for M_5 to save enough headroom for the other transistors. M_1 and M_2 are MOS switches controlled by $V_{bs}[n]$ and $V_{nbs}[n]$. When $BS[n] = 1($ $V_{bs}[n] = 1.5V)$, and $NBS[n] = 1($ $V_{nbs}[n] = 0V)$, M_1 is switched on and M_2 is switched off. $I_{idac} = 150nA$ is copied by $M_{3,ab}$ but no currents flow through M_2. Currents copied by $M_{4,ab}$ will flow out through V_{o2} and be injected into the feedback point. Since the total current copied by M_5 and $M_{6,ab}$ is $300nA$, extra currents will flow into the IDAC through V_{o1} and be drawn out from the feedback point. Figure 4.15 shows the currents, I_o1 and I_o2, flowing out of V_{o1} and V_{o2} for a given square-wave signal to BS and its inverse phase to NBS. The output currents prove I_{idac} to be $150nA$.

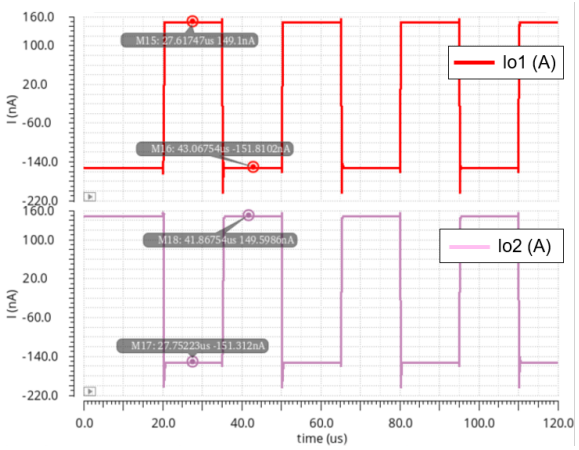

Figure 4.15: Currents provided by the IDAC

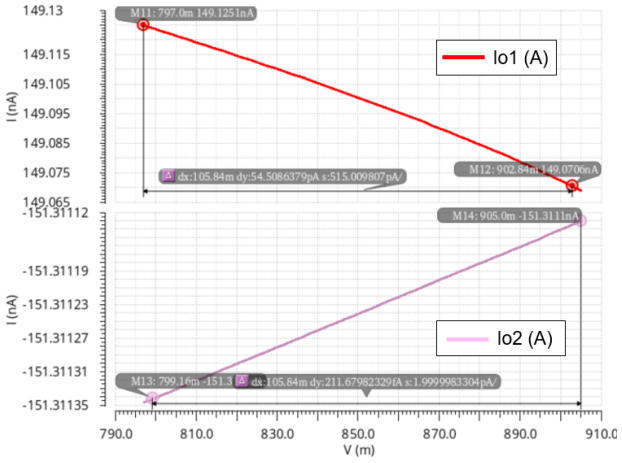

Figure 4.16: Current change with the variations in node volatge

As for the feedback point, V_{o1} and V_{o2} are connected to the virtual ground of the first integrator while the voltages at the virtual ground float around the $V_{cm,vg} = 850mV$. In order to determine whether the current of the IDAC will change with the variations in $V_{onx,opx}$, IDAC currents are plotted in Fig. 4.16 as sweeping the V_{o1} across the range from $795mV$ to $905mV$, which is the variation range of the virtual ground voltage. With a variation smaller than $520pA$, the output current of 150nA of the designed IDAC can be seen as stable.

4.1.4 DFF chain

The output waveforms of real DFFs have a rise-fall asymmetry which causes Inter Symbol Interference (ISI) that is manifested as additional second-order distortions (HD_2) introduced in FFT results. An ISI tuning DFF chain is designed to reduce HD_2 as shown in Fig. 4.17. The inputs of the DFFs take turns to be $BS[n]$ and $NBS[n]$ to average the asymmetry. Extra buffers are also connected to the outputs of the DFFs to provide the same load capacitance. This structure effectively reduces the rise-fall asymmetry of the output waveform.

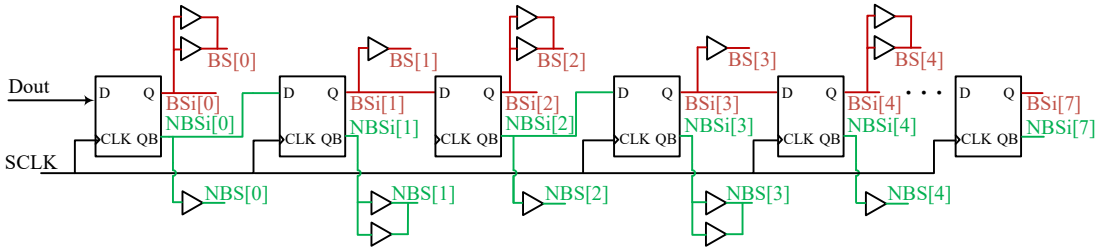

Figure 4.17: ISI tuning DFF chain

4.1.5 Comparator

This design reuses the dynamic comparator without a pre-amplifier, as designed in [22] and shown in Fig. 4.18. When $CLK = 0$, the comparator is in reset mode. By charging the capacitance at the output node, $M_{9,10}$ pull both outputs to V_{dd} while $M_{3,4,7,8}$ are turned off and $M_{5,6}$ start to conduct currents. When $CLK = 1$, $M_{3,4}$ immediately conduct and output nodes $V_{op,on}$ start to be discharged. If the left branch's total current is larger than the right branch's, V_{on} is discharged to 0 V first, M_6 is turned off, and M_8 begins to conduct currents, pulling V_{op} to V_{dd}.

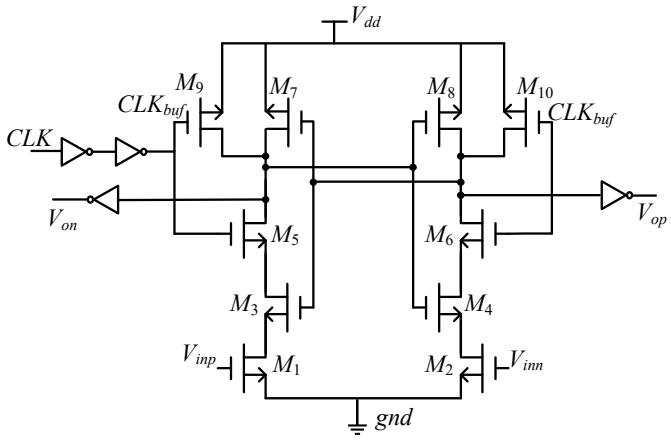

Figure 4.18: Schematic of the dynamic comparator

4.1.6 Power Consumption

Figure 4.19 shows the power breakdown of the whole system. The total power consumption is 35.7μW and the first integrator dominates the power consumption due to a second-stage amplifier.

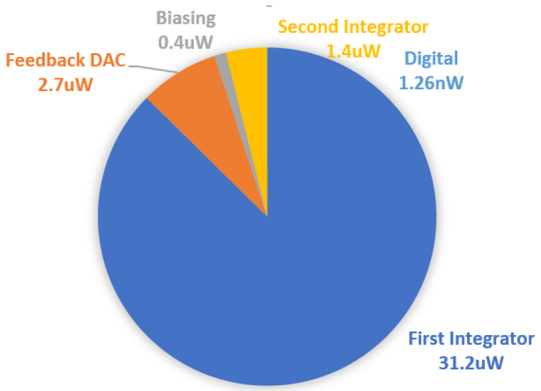

Figure 4.19: Power breakdown

4.1.7 Simulation Results

Now that the circuit-level architecture of the proposed CTSDM has been designed, FFT results of the CTSDM with real circuits are simulated. Figure 4.20 shows that the second-order distortion is effectively suppressed by the DFF chain with ISI tuning compared with that without

ISI tuning. Since the simulated SQNR of the designed CTSDM is $112dB$, which is larger than $102dB$, it meets the requirement for ENOB.

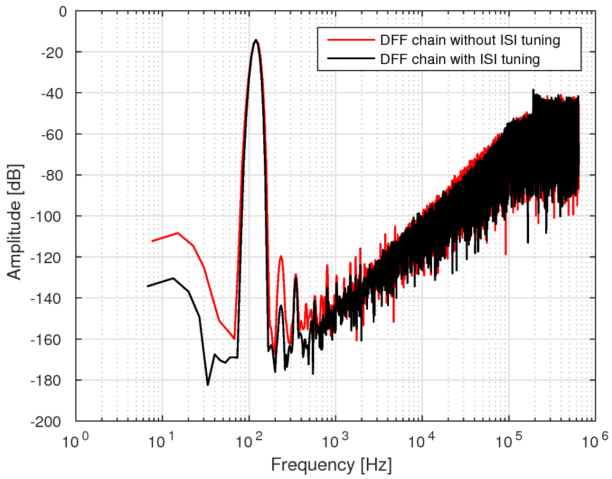

Figure 4.20: Simulation results of the CTSDM

4.2 Layout Design and Post-Layout Simulation

This design is implemented in a $0.18\mu m$ CMOS technology. In order to reduce the mismatch between capacitors, the capacitors of the same value connected to the corresponding positions in the fully differential system are placed symmetrically. Figure 4.21 shows the symmetrically placed compensation FIR DACs fed back to the positive and negative virtual ground of the second integrator. The integrating capacitors with a value of C_{in} in the first integrator is

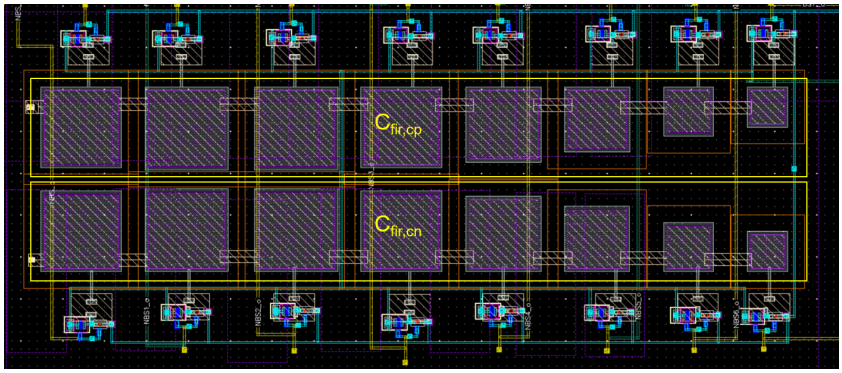

Figure 4.21: Layout of the compensation FIR DAC

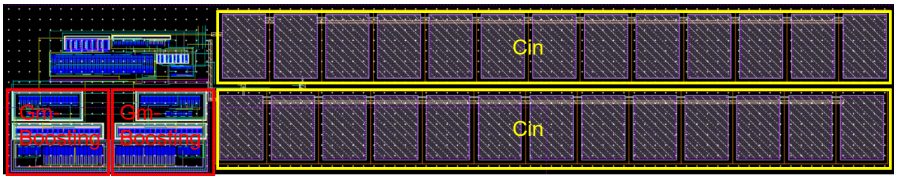

Figure 4.22: Layout of the first integrator

another example of the symmetrically placed capacitors shown in Fig. 4.22. The two Gm-boosting cells at the input are also placed symmetrically to reduce mismatch. One drawback of the capacitors is that they occupy a large area compared to that occupied by the transistors. It is acceptable, however, because the capacitors are placed at higher levels in the layout layers which allows other components, for example resistors, to be placed on the capacitors and effectively use the occupied area.

Except for the capacitors, the mismatch between the transistors used for the input pairs and the current sources brings about a large offset. A cross-coupled layout technique is used for differential pairs to prevent mismatch. Figure 4.23 shows the layout design of the Gm-boosting cell with the cross-coupled layout technique. As far as the PMOS and NMOS current sources and PMOS input pairs, corresponding transistors on differential branches are arranged alternately in either a "ABBA" or "AABB" sequence. We also use dummy devices to reduce mismatch. The voltages of the drain, source, bulk, and gate of the dummy devices are connected together, and sizes of the dummy devices are the same as the matching transistors. The currents generated by the IDACs need to be very stable to ensure the accuracy of the feedback waveform, so mismatch of the IDAC also needs to be avoided. Figure 4.24 shows the use of the cross-coupled layout technique in the layout of the IDACs.

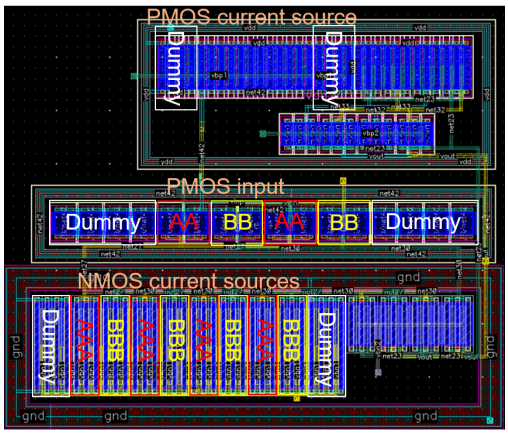

Figure 4.23: Layout of Gm-boosting cell

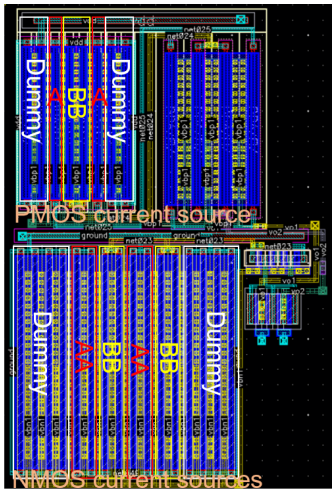

Figure 4.24: Layout of the IDAC

Figure 4.25 shows the layout design of the whole design. All the yellow framed area indicate the location of the ROIC circuits while the red framed area is the decoupling capacitors which filter supply noise. Separate power lines are used for the analog and digital supplies to provide isolation and avoid coupling between the digital and analog circuits.

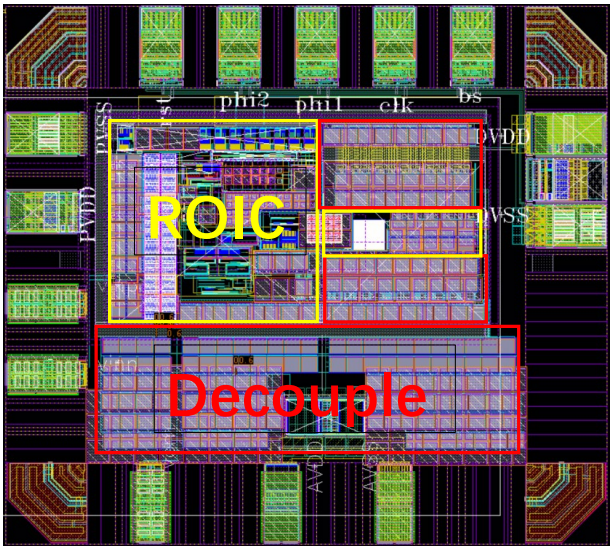

Figure 4.25: Layout of the whole design

Figure 4.26 shows the post-layout simulation results with and without noise in the circuit layout. Distortions appear in the FFT result of the post-layout simulation whithout noise. Since the noise floor of the CTSDM is higher than that of the distortions, they are negligible.

The SNR calculated according to the post-layout simulation result is obviously smaller than $92dB$, which is the targeted value, due to the large DC offset. The offset at low frequencies is introduced by the layout itself. Although the capacitors are placed symmetrically and the cross-coupled layout technique and dummies are used, there maybe mismatch in the layout design causing it to be a sub-optimal solution. Regardless, considering the complexity of the layout design and matching, this layout design is acceptable because the offset at low frequencies will not affect the applications of the system. Therefore, the designed ROIC can be used as the readout circuit of the targeted heart rate extraction sensor.

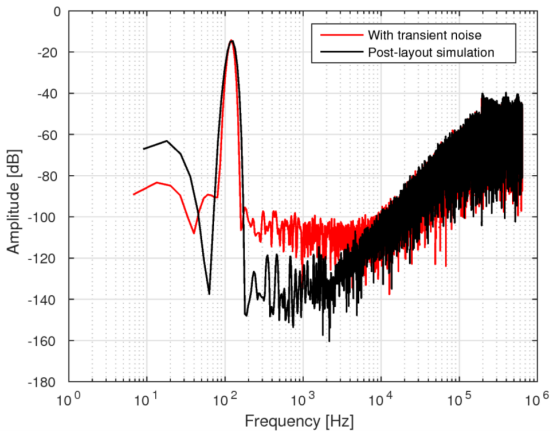

Figure 4.26: Post-layout simulation results of the CTSDM

Table 4.1: Performance Summary and Comparison

	This work		LT1028[1]		Low power amplifier[2]	
	ST150[3]	ZTP135[4]	ST150	ZTP135	ST150	ZTP135
Total RMS noise $[\mu V]$ $(\Delta f = 5Hz)$	34.6	29.8	147	96	30	24
Power consumption $[\mu W]$	35.7		74000		360	
Area $[mm^2]$	0.6545		> 31		> 1.4	

[1] The readout systems used in [1] is based on a LT1028 [23].

[2] The readout systems is based on low power CMOS amplifier [24]. In [1], it is a potential improvement for the readout system in the future.

[3] ST150 [25] is a sensor used for detector in [1].

[4] ZTP135 [26] is the other sensor served for detector in [1].

Table 4.1 shows the performance summary and comparison with the ROICs applied to the heart rate extraction sensor [1]. One of the improvements of the proposed ROIC is the lower IRN, which helps realize a higher resolution. The proposed CTSDM together with the ST150

and ZTP135 sensor achieves low input-referred noise of 34.6μV and 28.9μV at frequencies below 5Hz, respectively. The IRN in this work is enormously reduced compared with the circuitry based on LT1028 while is slightly larger than the readout systems based on a low power CMOS amplifier [24]. It is acceptable, however, because the power consumption and area occupation of this work are far less than that of these two systems. This work significantly lowers the energy consumption to 57.15μW. Meanwhile, the area occupied is reduced by at least ten times. In summary, this work has presented the design of a high input impedance ROIC with low input-referred noise, small power consumption, and small area occupation.

5 Conclusion

In this thesis, the theory and implementation of a high input impedance CTSDM-based readout system for thermopile sensors has been presented. The use of DCFIA structure reduces power consumption and circuit complexity. A second-order CIFF CTSDM with FIR DAC feedback is chosen to meet the desired ENOB and BW. The proposed design offers a simple architecture to achieve a high accuracy CTSDM and is a better solution with reduced IRN, lower power dissipation, and smaller area occupation for the sensor readout system compared with [1].

There are two main contributions and innovations of this work: 1) A CTSDM with FIR DAC feedback is realized. In particular, the systematic methodology for FIR DAC feedback design is proposed. 2) A Gm-OTA-C integrator with Gm-boosting input stages is designed and implemented to realize a high input impedance. Apart from the high input impedance, it also helps increase the linearity of the ROIC.

The CTSDM-based ROIC is implemented in a $0.18\mu m$ technology. The post-layout simulation results show that the designed circuit meets the requirements for the targeted application. As for future work, the PCB design of the chip and the measurement results post tape-out will be performed.

An aspect of this system worth improving is the total power dissipation. Since the choice of the first integrator is a second-stage amplifier, the current flowing through the second stage is kept large enough to maintain stability, which results in large power consumption. A more compact structure could be considered to reduce power consumption while ensuring the operation of the CTSDM in the future.

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