A 0.5e$^-_{rms}$ Temporal Noise CMOS Image Sensor With Gm-Cell-Based Pixel and Period-Controlled Variable Conversion Gain

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A 0.5e^-_{rms} Temporal Noise CMOS Image Sensor With Gm-Cell-Based Pixel and Period-Controlled Variable Conversion Gain

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***Abstract*— A deep subelectron temporal noise CMOS image sensor (CIS) with a Gm-cell based pixel and a correlated-double charge-domain sampling technique has been developed for photon-starved imaging applications. With the proposed technique, the CIS, which is implemented in a standard 0.18-μm CIS process, features pixel-level amplification and achieves an input-referred noise of 0.5 e^-_{rms} with a correlated double sampling period of 5 μs and a row read-out time of 10 μs. The proposed structure also realizes a variable conversion gain (CG) with a period-controlled method. This enables the read-out path CG and the noise-equivalent number of electrons to be programmable according to the application without any change in hardware. The experiments show that the measured CG can be tuned from 50 μV/e- to 1.6 mV/e- with a charging period from 100 ns to 4 μs. The measured characteristics of the prototype CIS are in a good agreement with expectations, demonstrating the effectiveness of the proposed techniques.**

***Index Terms*— Charge-domain sampling, CMOS image sensor, conversion gain (CG), low noise, low pass, period controlled, pixel-level amplification, sinc-type filter, subelectron.**

I. Introduction

THE increasing demand in photon-starved imaging system, especially in the application of medical and diverse scientific imaging, requires the development of high-sensitivity CMOS image sensors (CIS). The advantages of such a CIS solution over alternative imaging techniques include its power-efficient, cost-effective, and capability of supporting higher spatial resolution. However, the read-out noise originating from the signal path of a CIS plays a significant role in the total imaging systematic error budget, and thus often limits their ultimate detection performance.

To address this shortcoming, along with recent advances in the CIS process, a variety of approaches [1]–[14] have been proposed to reduce the input-referred noise of CIS. One solution based on implementing a high-gain column-level amplifier [2], [3] has widely been used in low-light level CIS attribute to its effectiveness of temporal noise reduction. Another trend in recent works [6]–[11] is to minimize the capacitance of the floating diffusion node in the pixel. In view of the high conversion gain (CG), these image sensors exhibit a very impressive photon-counting capability in respect of the noise performance. Nevertheless, the use of a fixed high-gain amplification, either in the voltage domain or the charge domain, inevitably leads to degradation of the dynamic range (DR). Given the fact that the signal-to-noise ratio at high light levels is adequate without high-gain amplification, an efficient technique to embed a tunable CG along the read-out path is essential for the implementation of low-noise CMOS image sensor with high DR.

In this paper, a Gm-cell-based pixel targeted for a deep subelectron temporal noise CIS is presented [15]. Implemented in a standard 0.18-μm CIS technology, the proposed pixel structure adopts in-pixel amplification method [1] to reduce its input-referred noise. To overcome the tradeoff between high DR, which benefits from low gain, and low input-referred noise, which benefits from high gain, a pixel-level variable-gain has been realized in a period-controlled manner. As such, the read-out path CG can be programmed according to the specific application of the CIS without any reconstruction of the hardware. In addition, the proposed pixel architecture allows the realization of pixel-level amplification without any in-pixel capacitors or resistors, enabling a relatively pixel compact layout with a pitch of 11 μm. Different from conventional low-noise CIS architectures [2], [3], the Gm-cell-based pixel leverages the use of a column-level high-gain amplifier and correlated multiple sampling (CMS). This simplifies the system and decreases the row read-out time. Measurement results show that the Gm-cell-based pixel effectively realizes a period-controlled CG, which can be tunable from 50 μV/e- to 1.6 mV/e- with a charging period from 100 ns to 4 μs. In addition, an input-referred noise of 0.5 e^-_{rms} is achieved in the measurement within a correlated double sampling (CDS) period of 5 μs and a row read-out time of 10 μs.

The rest of this paper is organized as follows. Section II describes the operating principle of the Gm-cell-based pixel and the periodic filtering model of the charge domain sampling and charge domain CDS. Section III presents the details

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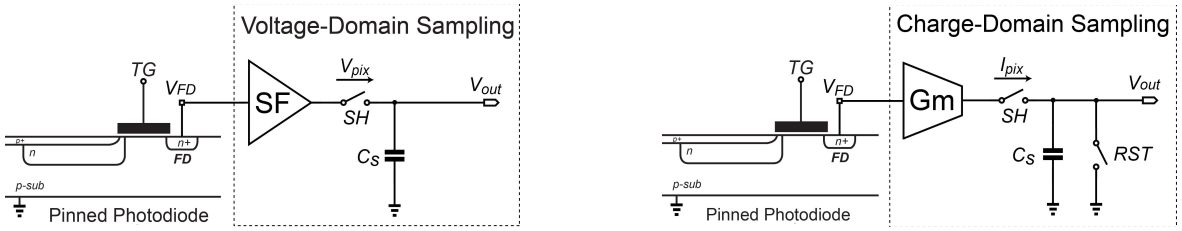

(a) (b)

Fig. 1. Signal read-out mechanism. (a) SF-based pixel with voltage-domain sampling. (b) Gm-cell-based pixel with charge-domain sampling.

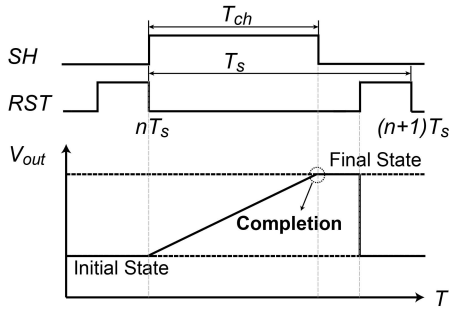

Fig. 2. Basic working principle of Gm-cell-based pixel.

of the circuits and sensor implementation. The characterization results of the fabricated image sensor are presented in Section IV. Conclusions are given in Section V.

II. Operating Principle

In a conventional CIS, a source followers (SFs) [Fig. 1(a)] is used in every pixel for buffering the floating diffusion (FD) node voltage onto the sample-and-hold (S/H) capacitors or column-parallel switched-capacitor amplifiers. Owing to its unity-gain nature, the SF topology inherently restricts the signal amplification at pixel-level. As a consequence, the combination of the pixel-level SF and column-level amplifier has been recognized as the most significant noise contributor along the read-out path. To address this problem, in this paper, we use a trans-conductance (Gm) cell-based pixel [Fig. 1(b)]. In contrast to prior work [26], which employed a trans-conductance cell to convey the pixel voltage to a current-mode output, the proposed pixel integrates the output current of the trans-conductance cell on a column-level S/H capacitor, thus producing a voltage output. This topology, on one hand, offers a pixel-level voltage gain to reduce the input-referred noise, and enables a period-controlled variable gain to achieve an optimal noise/DR tradeoff on the other hand. A dedicated charge-domain CDS technique has been applied to a CIS for the first time to realize this period-controlled method as well as to act as a *sinc*-type low-pass filter to reduce the input-referred noise, which will be discussed in this section.

A. Concept of Gm-Cell-Based Pixel

Fig. 2 shows the operating principle of the Gm-cell-based pixel. The pixel is composed of a pinned-photodiode (PPD) followed by a Gm-cell. Combined with the S/H capacitors, the read-out chain acts as a Gm-C integrator. Unlike the conventional SF-based pixel, which samples the signal with an exponential settling process in voltage domain, the proposed architecture first converts the FD node voltage V_{FD} into a current I_{pix}. Afterward, this current starts charging into the S/H capacitors with capacitance value of C_s within a programmable time window T_{ch}. Upon completion of the charging process (at the end of T_{ch}), the resulting voltage on the S/H capacitors is readout. To ensure that there is no relation between two adjacent sampling operations, the S/H capacitor is discharged by switching on *RST* before the next new sample. This process is often referred to as charge-domain sampling, which is also known as boxcar sampling [16]. Neglecting nonideal effects of the circuit, the time-domain output voltage of the sampler can be written as

$$V_{\mathrm{out}}(t) = \frac{1}{C_s}\cdot q[t] = \frac{1}{C_s}\cdot \int_{nT_s}^{nT_s+T_{ch}} \mathrm{I}_{pix}(t)dt$$
$$= \frac{g_m}{C_s}\cdot \int_{nT_s}^{nT_s+T_{ch}} V_{\mathrm{FD}}(t)dt \quad (1)$$

where g_m is the trans-conductance value of the Gm-cell, C_s is the S/H capacitance, n is an integer, T_{ch} is the charging period, and T_s is the sampling period.

B. Periodic Filtering Model of the Charge-Domain Sampling

The described charging process in (1) behaves as the convolution integral of an input signal and a rectangular window whose height is g_m/C_s and width is T_{ch}. Thus, it forms a continues-time (CT) first-order *sinc*-type low-pass filter prior to sampling at discrete-time (DT) intervals (Fig. 3) [17]. The transfer function of this filter in the s-domain is [18]

$$H(s) = \frac{g_m T_{ch}}{C_s}\cdot\frac{1-e^{-sT_{ch}}}{sT_{ch}} \quad (2)$$

and the ideal magnitude transfer function can be expressed as

$$|H_{WI}(f)| = \frac{g_m T_{ch}}{C_s}\cdot\left|\frac{\sin(\pi f T_{ch})}{\pi f T_{ch}}\right| = \frac{g_m T_{ch}}{C_s}\cdot|\sin c(\pi f T_{ch})|. \quad (3)$$

Fig. 4 shows the curve of $|H_{WI}(f)|$. From the envelope of the curve, the roll-off of the transfer function sidelobe is

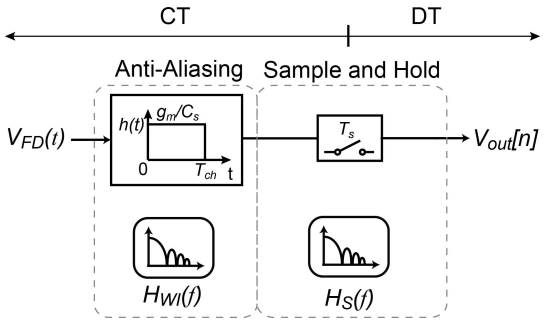

Fig. 3. Block diagram model of charge-domain sampling.

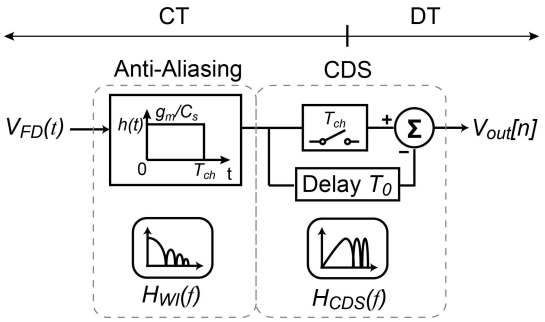

Fig. 5. Block diagram model of charge-domain CDS.

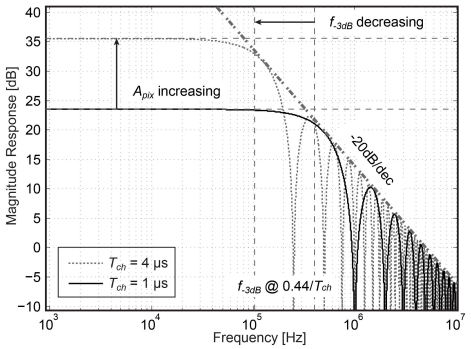

Fig. 4. Transfer function of the charge-sampling *sinc*-type low-pass filter.

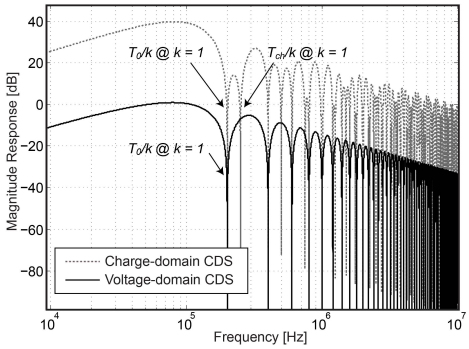

Fig. 6. Transfer function of the charge-domain CDS versus voltage-domain CDS.

found as −20 dB/dec, which is the same as a first-order low-pass filter. In addition, the notches of this *sinc*-type filter land at integer multiples of $kf_{\rm ch}$, where $f_{\rm ch} = 1/T_{ch}$ and k is an integer. Accordingly, the aliasing interference at $kf_{\rm ch}$ is theoretically infinite attenuated by the notches before they are aliased on top of the desired signal. As the notches only appear at discrete frequencies, the suppressed amount of high-frequency components at other frequency ranges is decided by the skirts of sidelobe adjacent to a notch. If the aliasing component appears at an offset frequency Δf from the kth notch $kf_{\rm ch}$, it will be suppressed by [19]

$$A(kf_{ch} + \Delta f) = \frac{\sin(\pi + \pi\,\Delta f T_{ch})}{\pi + \pi\,\Delta f T_{ch}} \approx \frac{\Delta f}{f_{ch}} \tag{4}$$

for $\Delta f \ll f_{\rm ch}$. It can be shown that for a given signal bandwidth and a particular attenuation requirement in the aliasing bands, (4) sets the required charging clock frequency to ensure a sufficiently wide *sinc* notches. Our simulation in MATLAB shows that, with the aid of the *sinc* notch attenuation, the charge-domain sampling reduces more than 20% thermal noise, in comparison with the voltage-domain sampling which features a first-order low-pass transfer function.

The transfer function also shows that the −3 dB bandwidth of the *sinc* filter is around $f_{-3\ \rm dB} \approx 0.44/T_{ch} = 0.44 f_{\rm ch}$ [20]. Meanwhile, the ideal dc voltage gain is found as

$$A_{pix} = \frac{V_{\rm out}}{V_{\rm FD}} = \frac{g_m T_{ch}}{C_s} = g_m \cdot \frac{1}{C_s f_{ch}} \tag{5}$$

where $1/C_s f_{\rm ch}$ can be regarded as the equivalent discrete time output impedance of the Gm-cell. Given the fact that both the gain of the voltage amplification $A_{\rm pix}$ and −3 dB bandwidth $f_{-3\ \rm dB}$ are determined by T_{ch}, a programmable $A_{\rm pix}$ and $f_{-3\ \rm dB}$ can be obtained by tuning the time window T_{ch} without using any other changes at circuit-level implementation. Fig. 4 also shows the charge-domain sampler transfer function with a different T_{ch} applied. Note that increasing T_{ch} not only helps in boosting the dc gain, but also reducing the bandwidth of the charge-domain sampler. This result is used in the operation of the CIS with proposed Gm-cell-based pixel to reduce the input-referred noise, which will be described in Section II-C.

C. Periodic Filtering Model of the Charge-Domain CDS

CDS is a well-known noise reduction technique in CIS. By subtracting the reset level and signal level, which are sampled at $T_{\rm rst}$ and $T_{\rm sig}$, the effectiveness of the CDS noise canceller can be characterized as a DT high-pass filtering operation, as analyzed in [21]. The transfer function of $H_{\rm CDS}(f)$ is given by

$$H_{\rm CDS}(f) = 2\sin(\pi f T_0) \tag{6}$$

where T_0 is the sampling interval between $T_{\rm rst}$ and $T_{\rm sig}$. A behavioral model of the Gm-cell-based pixel with charge-domain CDS is depicted in Fig. 5. As two distinct filtering functions, namely, a CT *sinc* low-pass filter $H_{WI}(f)$ and a DT high-pass filter $H_{\rm CDS}(f)$ are realized simultaneously, the overall transfer function of the charge-domain CDS without zero-order hold effect [22] can be written as

$$\begin{aligned} H_{\rm CD}(f) &= H_{WI}(f) \cdot H_{\rm CDS}(f) \\ &= 2\frac{g_m T_{ch}}{C_s} \sin c(\pi f T_{ch}) \cdot \sin(\pi f T_0). \end{aligned} \tag{7}$$

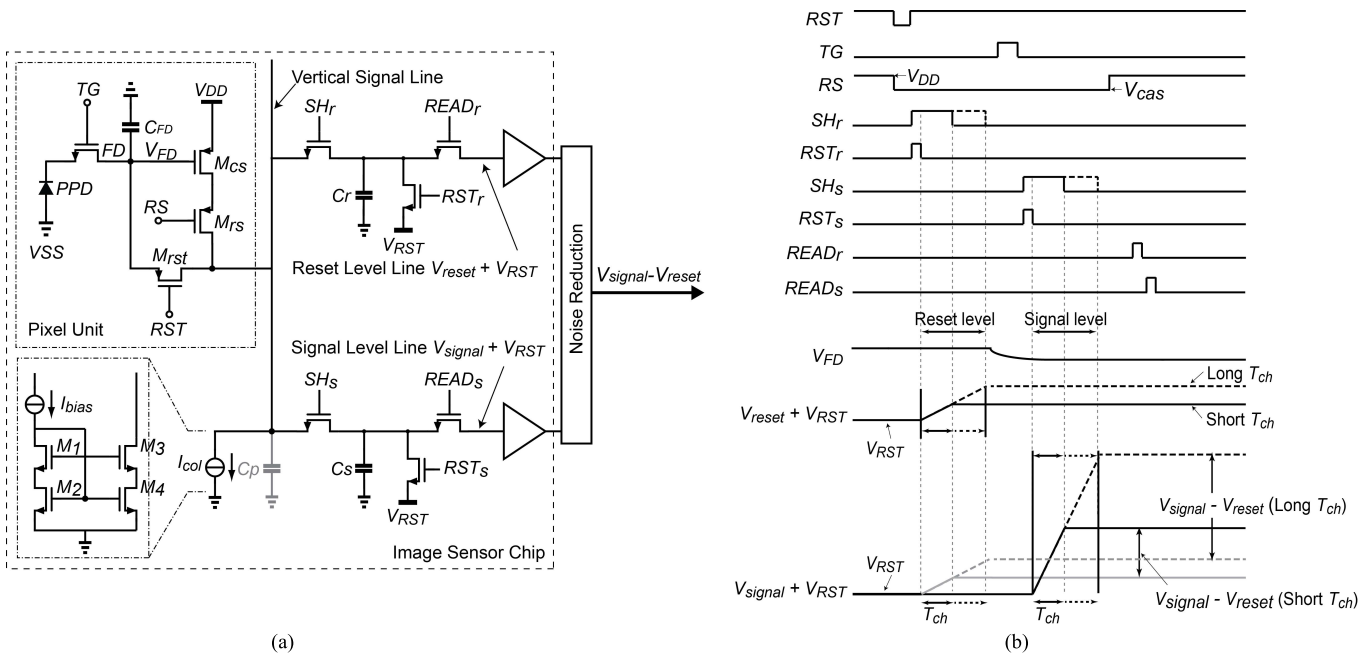

Fig. 7. (a) Schematic and (b) timing diagram of the CMOS image sensor with Gm-cell-based pixels.

Compared to a corresponding voltage-domain CDS transfer function, which has an equal −3 dB bandwidth, the charge-domain CDS introduces two groups of notches. As shown by simulations in Fig. 6, one group of notch frequencies is located at T_{ch}/k, owing to the charge-sampling *sinc*-type filter ($sinc(\pi f T_{ch})$), while the other group is placed at T_0/k, owing to the *sinc* function effect ($sin(\pi f T_0)$) of the CDS operation [22]. The joint effect of $sinc(\pi f T_{ch})$ and $sin(\pi f T_{ch})$ increases the depth of the notches and thus further improves the attenuation in the stopband. As such, compared with the voltage-domain CDS response, the charge-domain CDS provides a greater extent attenuation on high-frequency noise components than the first-order low-pass filtering of the voltage-sampling circuits.

III. Circuit And Sensor Implementation

Fig. 7 shows the implementation details and timing diagram of the proposed Gm-cell-based pixel in a CIS. It consists of a Gm-cell in each pixel and a CDS S/H capacitor bank at column-level. As the choice of the Gm-cell topology is dictated by the fill factor limitation, similar to [1], the proposed architecture adopts a single-ended cascode common-source topology as a pixel-level Gm-cell, where g_m is set by the pMOS transistor $M_{\rm cs}$. A relatively large size of $M_{\rm cs}$ ($W/L = 3/0.5$), needed for providing a sufficient g_m at the pixel-level, also helps to provide a sufficiently high self-biased reset voltage (∼2.3 V) at the FD node during the reset phase. A conceptual pixel layout is shown in Fig. 8.

The sinc-type filter analysis above assumes that the output resistance of the trans-conductor is infinite for the case when the trans-conductor and the capacitor form an integrator. Although such an assumption is not possible, as long as the time constant of the integrator is prominently longer than T_{ch}, the finite output resistance will not affect the performance significantly. Therefore, the Gm-C integrator's time constant τ

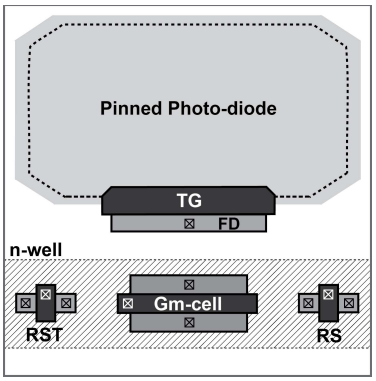

Fig. 8. Conceptual pixel layout of the Gm-cell-based pixel.

should be designed in the following way:

$$\tau = R_{o,Gm} \times (C_{\rm S/H} + C_p) \gg T_{ch}/2\pi \tag{8}$$

where $R_{o,Gm}$ is the output impedance of the Gm-cell, $C_{S/H}$ is the capacitance of the S/H capacitors, and C_p is the parasitic capacitance of the column net. In order to boost $R_{o,Gm}$ as well as mitigate the Miller effect [23], an adequate gate voltage $V_{\rm cas}$ is applied to the row select state of the pixel, allowing M_{rs} to operate as a cascode transistor, rather than to work in the triode region as a switch. Meanwhile, a high-impedance cascode current-source $I_{\rm col}$, which is implemented by long channel transistors M_1 to M_4, is chosen as the load of the common-source stage to define the biasing current. What is more, the capacitor in each column is carefully sized to meet the time constant and gain requirement, while also ensure that the associated kT/C noise is not dominant. In this paper, the values of C_r and C_s are both 2 pF, which in total occupy around 80% of the column area. Compared to other column-level architectures with similar readout gain, bandwidth and process [24], which paid the majority of the column area for additional amplifiers, the S/H capacitors used in this paper do not introduce a significant area overhead.

The uniformity of the CG across the pixel array is determined by the consistency of the T_{ch} pulsewidth, which in turn is affected by the rising/falling transition time of the clock pulse. To minimize the transition time, logic repeaters have been inserted to the clock distribution network. According to our simulations, the maximum clock delay from the clock input pad to the end of the repeater chain is less than 1 ns, while the variation of the T_{ch} pulsewidth is within 55 ps, which has negligible impact on the accuracy of the CG.

For the purpose of maximizing the output swing and improving the linearity performance, the supply voltage of the prototype chip is set to 3.8 V. According to simulations, g_m of M_{cs} is around 30 μS, and $R_{o,Gm}$ is larger than 200 MΩ with a 4-μA bias in each pixel. With $C_r = C_s = 2$ pF, T_{int} can be digitally programmed between 100 ns to 4 μs, resulting in a tuneable pixel-level voltage gain ranging from $\times 1$ to $\times 32$.

During the reset phase of each RS operating sequence, the Gm-cell is configured as a negative feedback scheme by switching on the reset transistor M_{rst}. As such, the Gm-cell is auto-zeroed, and the settled bias voltage of the common-source transistor M_{cs} as well as the reset level of the pixel is stored at the FD node capacitor.

After switching off M_{rst}, the Gm-cell is connected as an open-loop configuration, operating at the "memorized" bias condition stored on the parasitic capacitors of the FD node. With the help of switching on SH_r, a current I_r, which is proportional to the reset level V_r, is first produced by the Gm-cell and charges on the S/H capacitor C_r during a period T_{ch} from the initial state level V_{RST}. Then, at the end of the charge transfer from the PPD to the FD, the corresponding video signal current I_s is generated. Within the same period length T_{ch}, by switching on SH_s, this current is windowed charging into C_s from the same initial level V_{RST}. By performing these double charging processes, the resulting voltage level V_{reset} and V_{signal} are held on C_r and C_s, respectively, and are sequentially readout from the CIS chip via multiplexers and output buffers. An off-chip 16-b analog-to-digital converter (ADC) with an LSB of 30 μV has been implemented on the printed circuit board (PCB) to convert the analog output voltage levels into digital signal. The voltage subtraction of the reset level and the signal level (V_{signal}—V_{reset}) is then performed in the digital domain with the aid of a National Instruments—Vision Acquisition Software. In this way, we realize the CDS in digital domain and obtain the period-controlled amplified video signal V_{signal}–V_{reset} with the charge-domain CDS.

The test sensor with the proposed pixel architecture has been fabricated in a 0.18-μm 1P4M standard CIS process technology. Fig. 9(a) presents a microphotograph of the prototype chip with the main functional blocks highlighted. The test pixels has been divided into six subgroups, each of which includes 20(H) $\times$ 32(V) pixels and features the same pixel pitch of 11 μm. For flexibility, the digital logic, which implements the charging clocks T_{ch} and other operating clocks are realized off-chip.

IV. Experimental Results

The pixel-level CG CG_{tot} associated with the period-controlled function has been measured by using the photon transfer curve measurement technique. Fig. 10 shows the measured CG $CG_{\text{tot}} = CG_{\text{FD}} \times A_{\text{pix}}$ of the fabricated Gm-cell-based pixel, where CG_{FD} is the CG at FD node. To separately investigate the gain factor A_{pix} of the charge-sampling pixel, we also measure the CG_{FD} of an unity-gain pMOS SF-based reference 4T-pixel [24] as a comparison, in which the FD node is laid out with the same area as the proposed pixel. Note that the CG_{FD} of the SF-based pixel is measured as 55 $\mu V/e^-$, which indicates that the nominal value A_{pix} of the charge-sampling pixel is around $\times 30$. The measurement results show that CG_{tot} can be programmable from 50 $\mu V/e^-$ to 1.6 mV/e^- when a charging period from 100 ns to 4 μs applied. Four sample images captured by the test array at 0.5 lux at room temperature are shown in Fig. 9(b) with T_{ch} programmable from 0.5 to 4 μs.

Fig. 11 shows the DR as a function of T_{ch}. The highest DR exceeds 68 dB at T_{ch} = 100 ns, and remains above 60 dB

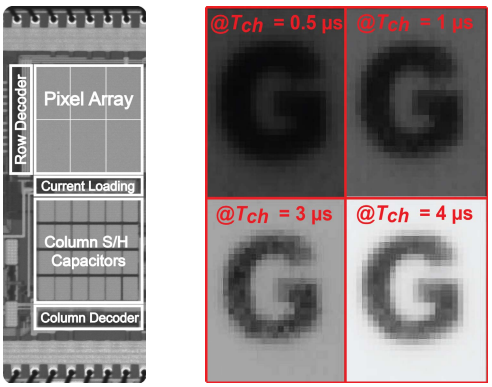

Fig. 9. (a) Microphotograph of the prototype sensor. (b) Sample images of the prototype sensor (T_{ch} = 0.5–4 μs).

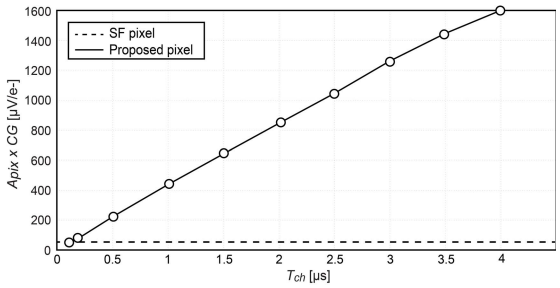

Fig. 10. Measured CG ($CG_{\text{FD}} \times A_{\text{pix}}$) as a function of the charging period T_{ch}.

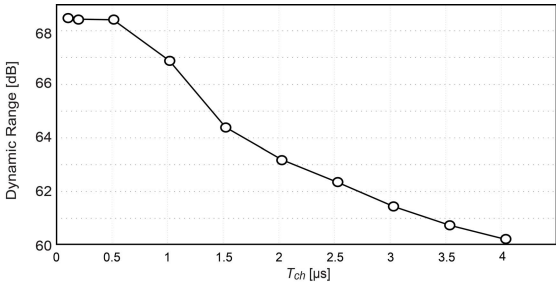

Fig. 11. Measured DR as a function of the charging period T_{ch}.

TABLE I
PERFORMANCE SUMMARY AND COMPARISON WITH PREVIOUS WORKS

	This work	ISSCC'11[1]	ISSCC'12 [2]	JSSC'16 [4]	EDL'15 [8]	VLSI'15 [10]
Noise reduction technique	Charge-domain sampling	Pixel level open loop amplification	Buried channel SF and column level amplification & CMS	Thin oxide pMOS SF and column level amplification	Pump transfer gate with tapered reset gate	LOFIC architecture with column level amplification
Process	180nm CIS	180nm CIS	180nm CIS	180nm CIS	65nm CIS	180nm CIS
Pixel size [μm^2]	11×11	11×11	10×10	6.5×6.5	1.4×1.4	5.5×5.5
Fill factor [%]	50	50	33	40	---	---
Read-out noise [e^-_{rms}]	0.5	0.86	0.7	0.48	0.29	0.5
CG [$\mu V/e^-$]	90~1600	300	45	160	413	240
Row read-out time [μs]	10	15	1600	25	---	143

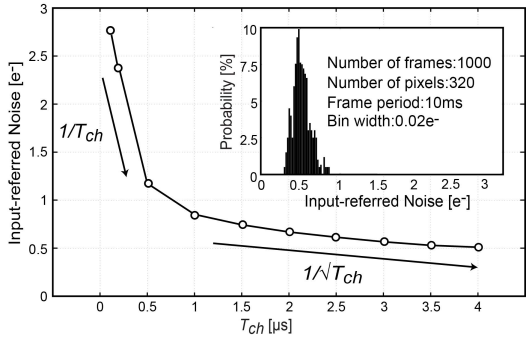

Fig. 12. Measured input-referred noise as a function of the charging period T_{ch}, and noise histogram at $T_{ch} = 4$ μs.

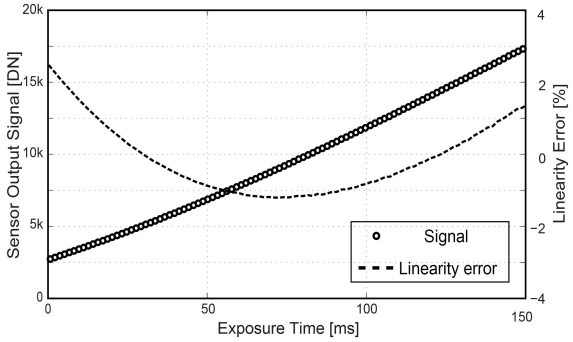

Fig. 14. Measured pixel output as a function of the exposure time.

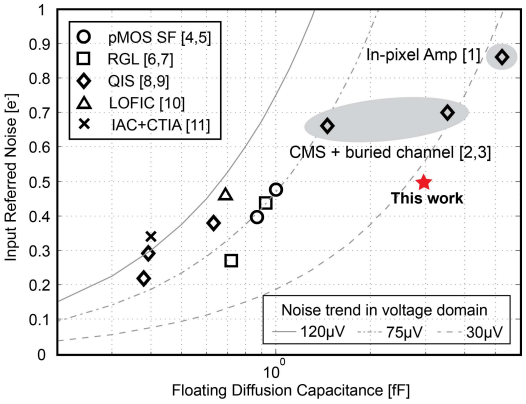

Fig. 13. Comparison of input-referred noise in the electron domain versu. FD capacitance, and noise trend in the voltage domain with reported image sensors [25]. The values are based on the best guess with the known values of CG_{FD} in reported publications.

at $T_{ch} = 4$ μs. In addition to the single exposure DR, the proposed pixel provides a calculated potential DR of 89 dB using typical multiple exposure methods thanks to the embedding of an adjustable-gain function.

Temporal noise characterization has been done in dark and implemented by keeping the transfer gate TG off during the measurement period. The rms temporal noise is first measured by a board-level 16-b ADC and then referred to the electron domain by dividing its corresponding measured CG. Fig. 12 shows the measured input-referred noise of the proposed pixel as a function of T_{ch}. The noise-reduction tendency initially is proportional to $1/T_{ch}$ and later becomes proportional to $1/\sqrt{T_{ch}}$. This result indicates that the Gm-cell-based pixel not only reduces the noise originating from the exceeding circuits connected at the back of the pixel as a result of the signal amplification of the charge-sampling technique, but also suppresses the thermal noise generated by the pixel level circuit as a result of noise-bandwidth reduction. At $T_{ch} = 4$ μs, the pixel achieves an input-referred noise of 0.51 e^-_{rms}. The inset of Fig. 12 shows the corresponding noise histogram. This result isobtained from 320 pixels after performing 1000 readouts with a CDS period of 5 μs and a row read-out time of 10 μs. In addition, when referred the noise back to the input of the signal chain in the voltage domain by dividing its corresponding gain factor A_{pix}, the lowest measured input-referred noise level is found around 27 μV, which is shown and compared with other state-of-the-art low-noise CIS in Fig. 13. Fig. 13 presents that an improvement in figure-of-merit regarding the read-out noise reduction was successfully obtained by using the proposed Gm-cell-based pixel and charge-domain CDS technique.

Fig. 14 shows the measured pixel output signal as a function of the exposure time, as well the corresponding linearity error. The peak linearity error of the proposed pixel architecture is measured as 2.5% with an output voltage range ranging from 0 to 0.5 V. Because of the trans-conductance is V_{FD}-dependence and the Gm-cell is open loop, the g_m variation across the whole array is relatively large compared with an SF-based pixel array. This degrades the pixel output linearity, and decreases the effectiveness of CDS. The latter results in a worse fixed pattern noise (FPN), which is measured as 3.8% at $T_{ch} = 1$ μs. For this sake, digital calibration has to be done after the acquisition

of the raw image from the sensor to improve the linearity and FPN. Besides the common approach of performing digital image processing, a trans-conductance linearization technique, such as source-degeneration [23], can also be applied to each Gm-cell to compensate for the nonlinearity, with the cost of a slightly elevated input referred noise.

Table I summarizes the performance of the proposed Gm-cell-based pixel in comparison with prior work on low-noise CIS. Compared to pixel-level open-loop amplification [1], this paper has the same pixel pitch and process node, while achieving 1.7× lower input-referred noise. Although the pixel pitch is large due to an extra n-well introduced by the pMOS transistors, it can be potentially reduced (e.g., ∼7-μm pixel pitch with a 50% fill factor) with the help of an optimized layout approach [4] and a smaller size pixel transistor. By utilizing the charge-sampling approach, the low noise performance of our prototype is achieved with a 10 μs row read-out time. It is worth noting that this row read-out speed would not degrade significantly even if the pixel array is extended to a larger size, thanks to the adoption of the charge-sampling approach.

V. Conclusion

In this paper, a prototype CIS with Gm-cell-based pixels has been presented. The proposed structure realizes the tunable CG with period-controlled method. This enables the CG and the noise-equivalent number of electrons to be programmable according to the application without any change in hardware. The obtained noise performance is comparable to the state-of-the-art low-noise CIS, while this paper employs a simpler circuit, without suffering from DR limitations, and is fabricated in a low cost, standard CIS process.

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References

[1] C. Lotto, P. Seitz, and T. Baechler, "A sub-electron readout noise CMOS image sensor with pixel-level open-loop voltage amplification," in *IEEE Int. Solid-State Circuits Conf. Dig. Tech. Papers*, Feb. 2011, pp. 402–404.

[2] Y. Chen, Y. Xu, Y. Chae, A. Mierop, X. Wang, and A. Theuwissen, "A 0.7 e^-_{rms} temporal-readout-noise CMOS image sensor for low-light-level imaging," in *IEEE Int. Solid-State Circuits Conf. Dig. Tech. Papers*, Feb. 2012, pp. 384–385.

[3] S.-F. Yeh, K.-Y. Chou, H.-Y. Tu, C. Y.-P. Chao, and F.-L. Hsueh, "A 0.66 e^-_{rms} temporal-readout-noise 3D-stacked CMOS image sensor with conditional correlated multiple sampling (CCMS) technique," in *Proc. Symp. VLSI Circuits*, Jun. 2015, pp. C84–C85.

[4] A. Boukhayma, A. Peizerat, and C. Enz, "A sub-0.5 electron read noise VGA image sensor in a standard CMOS process," *IEEE J. Solid-State Circuits*, vol. 51, no. 9, pp. 2180–2191, Sep. 2016.

[5] A. Boukhayma, A. Peizerat, and C. Enz, "Temporal readout noise analysis and reduction techniques for low-light CMOS image sensors," *IEEE Trans. Electron Devices*, vol. 63, no. 1, pp. 72–78, Jan. 2016.

[6] M.-W. Seo, S. Kawahito, K. Kagawa, and K. Yasutomi, "A 0.27 e^-_{rms} read noise 220-μV/e-conversion gain reset-gate-less CMOS image sensor with 0.11-μm CIS process," *IEEE Electron Device Lett.*, vol. 36, no. 12, pp. 1344–1347, Dec. 2015.

[7] M.-W. Seo, T. Wang, S.-W. Jun, T. Akahori, and S. Kawahito, "A 0.44 e^-_{rms} read-noise 32 fps 0.5 Mpixel high-sensitivity RG-less-pixel CMOS image sensor using bootstrapping reset," in *IEEE Int. Solid-State Circuits Conf. Dig. Tech. Papers*, Feb. 2017, pp. 80–81.

[8] J. Ma and E. R. Fossum, "Quanta image sensor jot with sub 0.3 e^-_{rms} read noise and photon counting capability," *IEEE Electron Device Lett.*, vol. 36, no. 9, pp. 926–928, Sep. 2015.

[9] J. Ma, K. Starkey, A. Rao, K. Odame, and E. Fossum, "Characterization of quanta image sensor pump-gate jots with deep sub-electron read noise," *IEEE J. Electron Devices Soc.*, vol. 3, no. 6, pp. 472–480, Nov. 2015.

[10] S. Wakashima, F. Kusuhara, R. Kuroda, and S. Sugawa, "A linear response single exposure CMOS image sensor with 0.5e^- readout noise and 76 ke^- full well capacity," in *Proc. Symp. VLSI Circuits*, Jun. 2015, pp. C88–C89.

[11] Q. Yao, B. Dierickx, B. Dupont, and G. Ruttens, "CMOS image sensor reaching 0.34 e^-_{RMS} read noise by inversion-accumulation cycling," in *Proc. Int. Image Sens. Workshop*, Vaals, The Netherlands, Jun. 2015, pp. 369–372.

[12] M. Sakakibara *et al.*, "A high-sensitivity CMOS image sensor with gain-adaptive column amplifiers," *IEEE J. Solid-State Circuits*, vol. 40, no. 5, pp. 1147–1156, May 2005.

[13] X. Wang, M. Snoeji, P. Rao, A. Mierop, and A. Theuwissen, "A CMOS image sensor with a buried-channel source follower," in *IEEE Int. Solid-State Circuits Conf. Dig. Tech. Papers*, Feb. 2008, pp. 62–63.

[14] Y. Yamashita *et al.*, "A 300 mm wafer-size CMOS image sensor with in-pixel voltage-gain amplifier and column-level differential readout circuitry," in *IEEE Int. Solid-State Circuits Conf. Dig. Tech. Papers*, Feb. 2011, pp. 408–409.

[15] X. Ge and A. Theuwissen, "e^-_{rms} temporal-noise CMOS image sensor with charge-domain CDS and period-controlled variable conversion-gain," in *Proc. Int. Image Sens. Workshop*, Hiroshima, Japan, Jun. 2017, pp. 290–293.

[16] S. Karvonen, T. A. Riley, S. Kurtti, and J. Kostamovaara, "A quadrature charge-domain sampler with embedded FIR and IIR filtering functions," *IEEE J. Solid-State Circuits*, vol. 41, no. 2, pp. 507–515, Feb. 2006.

[17] M. Tohidian, I. Madadi, and R. B. Staszewski, "Analysis and design of a high-order discrete-time passive IIR low-pass filter," *IEEE J. Solid-State Circuits*, vol. 49, no. 11, pp. 2575–2587, Nov. 2014.

[18] A. Mirzaei, S. Chehrazi, R. Bagheri, and A. A. Abidi, "Analysis of first-order anti-aliasing integration sampler," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 55, no. 10, pp. 2994–3005, Nov. 2008.

[19] J. L. Bohorquez, M. Yip, A. P. Chandrakasan, and J. L. Dawson, "A biomedical sensor interface with a sinc filter and interference cancellation," *IEEE J. Solid-State Circuits*, vol. 46, no. 4, pp. 746–756, Apr. 2011.

[20] S. Karvonen, T. A. D. Riley, and J. Kostamovaara, "A CMOS quadrature charge-domain sampling circuit with 66-dB SFDR up to 100 MHz," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 52, no. 2, pp. 292–304, Feb. 2005.

[21] H. Wey and W. Guggenbuhl, "Noise transfer characteristics of a correlated double sampling circuit," *IEEE Trans. Circuits Syst.*, vol. 29, no. 11, pp. 1028–1030, Oct. 1986.

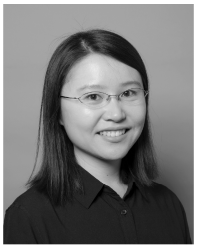
[22] P. Martin-Gonthier and P. Magnan, "CMOS image sensor noise analysis through noise power spectral density including undersampling effect due to readout sequence," *IEEE Trans. Electron Devices*, vol. 61, no. 8, pp. 2834–2842, Aug. 2014.

[23] B. Razavi, *Design of Analog CMOS Integrated Circuits*. New York, NY, USA: McGraw-Hill, 2001, pp. 166–169.

[24] X. Ge and A. Theuwissen, "A CMOS image sensor with nearly unity-gain source follower and optimized column amplifier," in *Proc. IEEE SENSORS*, Oct. 2016, pp. 1–3, doi: 10.1109/ICSENS.2016.7808589.

[25] N. Dutton, "Advanced IC design for ultra-low-noise sensing forum: Noise in single photon counting image sensors," in *Proc. IEEE Int. Solid-State Circuits Conf. Dig. Tech. Papers*, Feb. 2016, pp. 506–509.

[26] R. M. Philipp, D. Orr, V. Gruev, J. V. D. Spiegel, and R. Etienne-Cummings, "Linear current-mode active pixel sensor," *IEEE J. Solid-State Circuits*, vol. 42, no. 11, pp. 2482–2491, Nov. 2007.



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