A Phase-Domain Readout for Thermal-Diffusivity Based Temperature Sensors

by

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Abstract

This thesis describes the implementation of a phase-domain readout system for a thermal-diffusivity (TD) based temperature sensor. Such sensors measure the phase shift of an electro-thermal filter (ETF), which exhibits a near-linear dependency on absolute temperature. The phase shift is measured by a phase-domain delta-sigma modulator (PD-DSM). Although ETFs can be very accurate, their readout circuitry often constrains overall performance. A notable concern is their offset, which is usually much larger than the ETF's output signal and may cause the PD-DSM to clip. In this work, this issue is addressed by a hybrid offset-reduction strategy. The PD-DSM itself is designed to achieve a temperature inaccuracy of 0.04°C.

The design was fabricated using TSMC 180nm CMOS technology. Due to a design error, the PD-DSM did not achieve the targeted accuracy. Nonetheless, the hybrid offset cancellation scheme works as intended, demonstrating efficacy by effectively mitigating residual offset to sub-µV levels across temperature ranges extending up to 180°C.

Acknowledgments

As I began writing this section of my thesis, memories of the past two years came flooding back. I must acknowledge that my journey here in Delft has been filled with learnings and challenges from the very beginning. I could only navigate this path with the immense support and encouragement from those around me. I want to express my gratitude to each one of them for their unwavering presence.

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Lastly, I would like to express my profound gratitude to my mother, father, and brother for believing in me and providing their unconditional love and support. This work is dedicated to my family who have gone above and beyond to support my life overseas.

Kind regards,
Tanmeet Kaur.

Contents

1. Introduction

1.1 Motivation and Objective

Modern systems-on-chip (SoCs), such as microprocessors, often employ billions of transistors switching at GHz frequencies. With so many transistors crammed into a small die area, self-heating becomes a major challenge. To maintain performance and reliability, on-chip thermal management systems are crucial. These systems regulate the power dissipation of SoCs by reducing the clock speeds or shutting off the processors to maintain the die temperature within the safe operating limits.

In multi-core processors, for example, the task-dependent activity of the cores can lead to multiple hotspots, some of which may reach temperatures as high as 100°C [1]. Therefore, thermal management systems are used to detect and minimize their occurrence. To do this, modern SoCs typically employ several temperature sensors (TS), which are located near potential hotspots. To obtain sufficient accuracy, however, such sensors must usually be calibrated and trimmed, which is expensive and time-consuming. Therefore, there is a need for temperature sensors that are sufficiently *accurate without the need for calibration.*

This chapter will briefly introduce the main types of CMOS temperature sensors and the limitations on their accuracy. Section 1.2 discusses BJT-based temperature sensors, while sections 1.3 and 1.4 discuss MOSFET- and resistor-based temperature sensors, respectively. Section 1.5 discusses thermal diffusivity (TD) sensors, which are especially suitable for thermal management because of their low untrimmed inaccuracy, and introduces the readout circuit for TD sensors. Section 1.6 discusses the latest developments in TD sensors, which provides the basis for the formulation of the main goals of this thesis. Section 1.7 discusses the design targets and lastly, the organization of the thesis is presented in Section 1.8.

1.2 BJT-based CMOS Temperature Sensors

In CMOS technology, temperature sensors can be realized in several ways. Of these, the most popular are sensors based on the properties of bipolar-junction transistors (BJTs). These exploit the fact that at a constant collector current I_C, the base-emitter voltage, V_{BE}, of a BJT is a strong function of temperature, expressed as:

$$V_{BE} = \frac{kT}{q}\ln\left(\frac{I_C}{I_S}\right) \tag{1.1}$$

Since the saturation current (I_S) is an exponential function of temperature ($\propto T^4$), V_{BE} decreases almost linearly with temperature and thus exhibits complementary-to-absolute-temperature (CTAT) behavior. However, it is not very accurate, since I_S depends on several process-dependent parameters.

By biasing two BJTs at a well-defined collector current ratio, and subtracting their base-emitter voltages, a voltage that is proportional to absolute temperature (PTAT) is generated:

$$V_{BE1} - V_{BE2} = \Delta V_{BE} = \frac{kT}{q}\ln\left(\frac{I_{C1}}{I_{C2}}\right) \tag{1.2}$$

A temperature-independent voltage called a bandgap reference voltage (V_{REF}) can be made by linearly combining V_{BE} and scaled ΔV_{BE}, as shown in Figure 1.1. A digital representation of absolute temperature can then be obtained by digitizing the ratio between V_{REF} and either the PTAT or CTAT voltages.

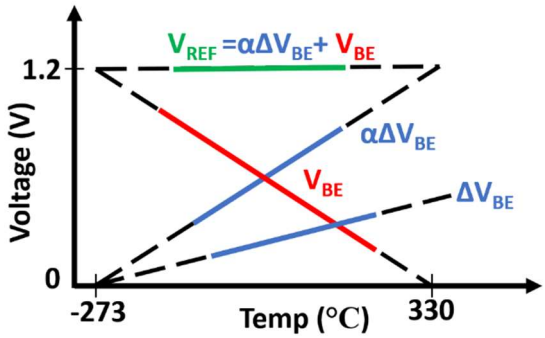


Figure 1.1: PTAT and CTAT Voltages vs Temperature.

The spread in V_{REF} is mainly due to the spread in V_{BE} and typically results in a temperature error of a few °C. Since the spread in V_{BE} is mainly due to the spread in I_S, a 1-pt trim can be used to significantly reduce this error, to less than ±0.1°C (3σ) from -55°C to 125°C [2]. For this reason, BJT-based temperature sensors are widely used.

Due to the exponential increase of I_S with temperature, however, the accuracy of BJT-based temperature sensors degrades at high temperatures. Over the temperature range -55°C to 200°C, the best-reported inaccuracy is ±0.45°C after a 1-pt trim [3]. However, this was implemented in a low-leakage CMOS SOI (Silicon-on-insulator) technology.

1.3 MOSFET-based Temperature Sensors

When biased in weak inversion, MOSFETs also exhibit an exponential relationship between their gate-source voltage (V_{GS}) and the drain current (I_D), as shown in Equation 1.3.

$$I_D = \frac{W}{L}\mu \left(\frac{kT}{q}\right)^2 \exp\left(\frac{V_{GS} - V_{TH}}{nkT/q}\right) \tag{1.3}$$

As a result, in the same way as BJTs, MOSFETs can also be used as temperature sensors [4]. Since V_{TH} is generally lower than V_{BE}, MOSFET-based sensors can be operated at lower supply voltages. However, because of the process spread in both V_{TH} and in the charge mobility μ, MOSFET-based sensors require at least 2-pt trim to achieve the same accuracy as their BJT counterparts [5].

After a 1-pt trim, the best-reported inaccuracy is ±0.4°C (3σ) from -40°C to 125°C [4]. However, MOSFETs exhibit high leakage currents at high temperatures, and thus limited accuracy. For example, the design in [5] only achieves an inaccuracy of ±0.8°C (3σ) from -55°C to 150°C after a 1-pt trim.

1.4 Resistor-based Temperature Sensors

Due to their temperature dependence, resistors in CMOS technology can also be used as on-chip temperature sensing elements. However, since the value of a resistor depends on both its geometry and

its doping concentration, the resulting temperature sensors are not very accurate. The lowest reported inaccuracy is ±0.4°C from -40°C to 180°C after a 1-pt trim [6].

Table 1.1 summarizes the inaccuracy of the state-of-the-art sensors reported in [3], [5], and [6]. Due to process spread, they all need at least a 1-pt trim to achieve reasonable inaccuracy.

Table 1.1: Performance Overview

Sensor type	Technology	Inaccuracy [°C]	Trimming points	Temp. range [°C]
BJT [3]	0.16µm CMOS	0.4	1-pt trim	-55 to 200
MOSFET [5]	0.18µm CMOS	0.8	1-pt trim	-50 to 150
Resistor [6]	0.18µm CMOS	0.4	1-pt trim	-40 to 180

However, trimming is an expensive and time-consuming process; it requires the TS under test to be brought to at least one known temperature, established by an accurate reference TS, after which its output can be corrected, e.g. by setting a digital trim code. An on-chip programmable memory is then required to store these trim codes, which increases fabrication costs.

Another way of sensing temperature is by measuring the thermal diffusivity of silicon [7]. Recent results show that such sensors can achieve better untrimmed accuracy than conventional temperature sensors [10] [14], as well as better accuracy at high temperatures [15].

1.5 TD-based temperature sensors

1.5.1 Working Principle

Thermal diffusivity is an intrinsic property of materials and defines the rate of heat transfer through them. Studies of the thermal diffusivity of silicon, D_{si} (= 0.86 cm^2/s at 27°C) show that it is strongly dependent on temperature [8]. Furthermore, since the silicon used in CMOS technology is very pure, D_{si} is very well-defined. From –55°C to 125°C, the relationship between D_{si} and temperature may be approximated by [9]:

$$D_{si} \propto \frac{1}{T^{1.8}} \tag{1.4}$$

In practice, D_{si} can be determined by measuring the time it takes for heat to diffuse between two designated points on a silicon chip. This is typically done by placing a temperature sensor a short distance, denoted by *s*, away from a heater, as illustrated in Figure 1.2. This arrangement is called an electro-thermal filter (ETF) and it serves as the sensing element of a TD sensor.

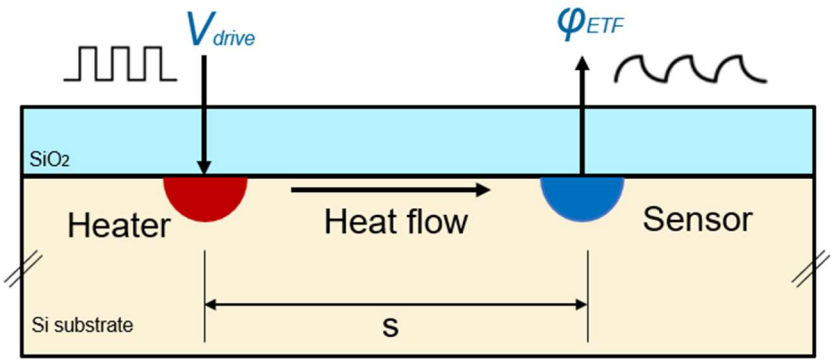


Figure 1.2: ETF with point heater and point sensor.

If the heater is driven by a periodic signal (V_{drive}) with an angular frequency ω, the heat will diffuse through the substrate and cause delayed temperature variations at the position of the sensor. This delay is a measure of D_{si} and manifests itself as a phase shift in the electrical signal received by the sensor.

In Figure 1.2, considering the heater to be a point heat source and the SiO_2 layer to be a perfect insulator, the heat will diffuse outward in a semi-spherical manner. From [22], the thermal impedance $Z_{th}(\omega,s)$, which relates the temperature fluctuations $T(\omega,s)$ around the heater to the power dissipated in the heater $P_{heater}(\omega)$, is given by:

$$\mathrm{Z_{th}}(\omega,s)=\frac{T(\omega,s)}{P_{heater}(\omega)}=\frac{1}{2\pi k_{si}s}\exp\left(-s\sqrt{\frac{\omega}{2D_{si}}}\right)\exp\left(-js\sqrt{\frac{\omega}{2D_{si}}}\right) \tag{1.5}$$

Where s is the distance to the point heat source, $T(\omega,s)$ is the temperature increase at this distance and k_{si} is the thermal conductivity of Silicon. The magnitude and phase of Z_{th} are then:

$$|\mathrm{Z_{th}}(\omega,s)|=\frac{1}{2\pi k_{si}s}\exp\left(-s\sqrt{\frac{\omega}{2D_{si}}}\right) \tag{1.6}$$

$$\varphi(\omega,s)=-s\sqrt{\frac{\omega}{2D_{si}}} \tag{1.7}$$

From Equation 1.6, the magnitude of thermal impedance Z_{th} is a function of k_{si} and D_{si} and decreases as the angular frequency increases, which is analogous to the behavior of an electrical low-pass filter.

If the sensing element has a sensitivity of S_t (mV/K), then the amplitude of the ETF's output is given by:

$$V_{ETF}(\omega,s)=\frac{P_{heater}S_t}{2\pi k_{si}s}\exp\left(-s\sqrt{\frac{\pi f_{drive}}{D_{si}}}\right) \tag{1.8}$$

The phase shift measured at the output of the ETF as a function of D_{si} is expressed as:

$$\varphi_{ETF}=-s\sqrt{\frac{\pi f_{drive}}{D_{si}}}==-s\sqrt{\pi f_{drive}T^{1.8}} \tag{1.9}$$

where f_{drive} is the frequency of the electrical signal driving the heater. From Equation 1.8 and Equation 1.9, we can conclude that to determine D_{Si}, we can either measure the output voltage of an ETF, or its phase shift. However, V_{ETF} depends on heater power (P_{heater}) and ETF sensitivity (S_t), both of which suffer from process spread, while φ_{ETF} only depends on D_{Si}, $f_{drive,}$ and $s,$ which are well-defined parameters. Therefore, it is a better choice to read out the output phase shift of an ETF. Additionally, φ_{ETF} is proportional to $T^{0.9}$, and this near-linear relation makes it convenient to extract temperature information from the ETF output.

1.5.2 ETF Designs

Two main considerations govern the design of an ETF. First, φ_{ETF} is proportional to the distance s, which means that any process spread in s causes additional error and must be minimized. Second, both the heater and the temperature sensor must be embedded in the substrate for maximum heat transfer. Furthermore, the sensor must be low power to avoid introducing additional errors due to its own self-heating.

The heater in an ETF is simply realized as a small on-chip diffusion resistor. The resistor is sized based upon the targeted P_{heater} such that:

$$P_{heater} = \frac{1}{2}\frac{V_{ddH}^2}{R_{heater}} \tag{1.10}$$

Where V_{ddH} is the heater supply voltage and R_{heater} is the resistance of the heater. With P_{heater} = 4.2mW (as in [15]) and V_{ddH} = 1.8V, R_{heater} equals to 385Ω.

Integrated thermocouples are passive sensors and dissipate no power. A thermocouple exploits the Seebeck effect, which stipulates that when two dissimilar conducting materials experience a temperature difference across their terminals, they produce an output voltage proportional to this temperature variation. In CMOS technology, a thermocouple can be made by combining a diffusion resistor with a metal interconnect. The combination of a *p+* -diffusion resistor and *Al* metal interconnect yields a thermocouple with a sensitivity, S_t, of approximately 0.5mV/K [9]. The geometrical accuracy of such thermocouples is defined by lithography, which improves with technology scaling. Therefore, thermopiles, consisting of several *p+/Al* thermocouples (Figure 1.3) are well-suited for use in ETFs.

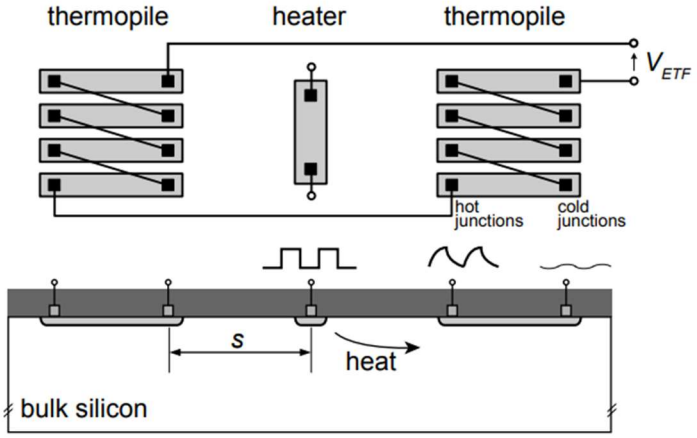


Figure 1.3: Thermopile ETF [17].

The two main considerations for the design of the thermopile are the length of its diffusion resistor arms and the heater/sensor spacing, *s*. Ideally to maximize its output signal (V_{ETF}), the distance between its hot and cold junctions should be maximized. However, this increases the thermopile's resistance and therefore, its noise. To optimize the resulting Signal-to-noise Ratio (SNR), the length of the thermopile is typically made equal to the value of *s* [10].

Lithographic errors will change the heater-sensor spacing. From Equation 1.9, these will cause phase errors, and thus, temperature sensing errors:

$$\frac{\delta\varphi_{ETF}}{\varphi_{ETF}} = \frac{\delta s}{s} = -0.5\frac{\delta D}{D} = 0.9\frac{\delta T}{T} \tag{1.11}$$

The effect of lithographic errors can thus be reduced by increasing the value of *s*. However, from Equations 1.8 and 1.9, if s is increased while φ_{ETF} is kept constant by scaling f_{drive} by a factor $1/s^2$, then V_{ETF} will scale by a factor $\frac{1}{s}$. Since both the thermopile and its readout circuit contribute to noise, a trade-off exists between the SNR and the accuracy of a TD sensor. For the same P_{heater}, decreasing the value of *s* reduces accuracy but increases SNR. In scaled CMOS processes, the use of better lithography should enable the use of smaller ETFs with higher SNR while maintaining sufficient accuracy.

To maximize the SNR of an ETF, various thermopile ETFs have been developed [10] [11]. The best design is the so-called polygon ETF [12], whose top view is shown in Figure 1.4.

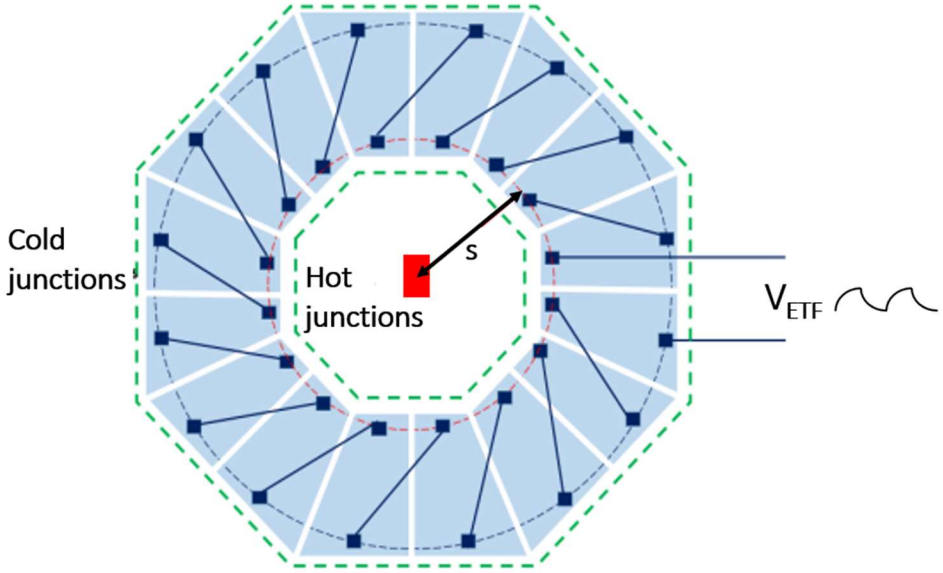


Figure 1.4: Polygon (Octagonal) TP-ETF with 16-arms [23].

The polygon ETF in [12] employs a thermopile made of 16 thermocouples (*p+* diffusion resistor/ metal interconnect) in series. The heater is surrounded by the thermocouples to maximize the transfer of heat from the heater to their hot junctions, and thus maximize the output signal (V_{ETF}).

The layout of a polygon ETF also maximizes the area of the thermocouple arms, which minimizes their resistance and maximizes the ETF's SNR. However, this also maximizes their parasitic junction capacitance, which limits the ETF's electrical bandwidth (BW). Another drawback is that the use of

trapezoidal arms makes the layout difficult and, in many cases, incompatible with the complex design rules of advanced processes.

An ETF with a simpler layout, the so-called ring ETF, replaces the thermopile with ring-shaped thermistors [13]. To get a voltage output, four thermistors are configured as a Wheatstone bridge, as shown in Figure 1.5. The resistors on the bridge diagonals are then heated in anti-phase, resulting in a differential output signal.

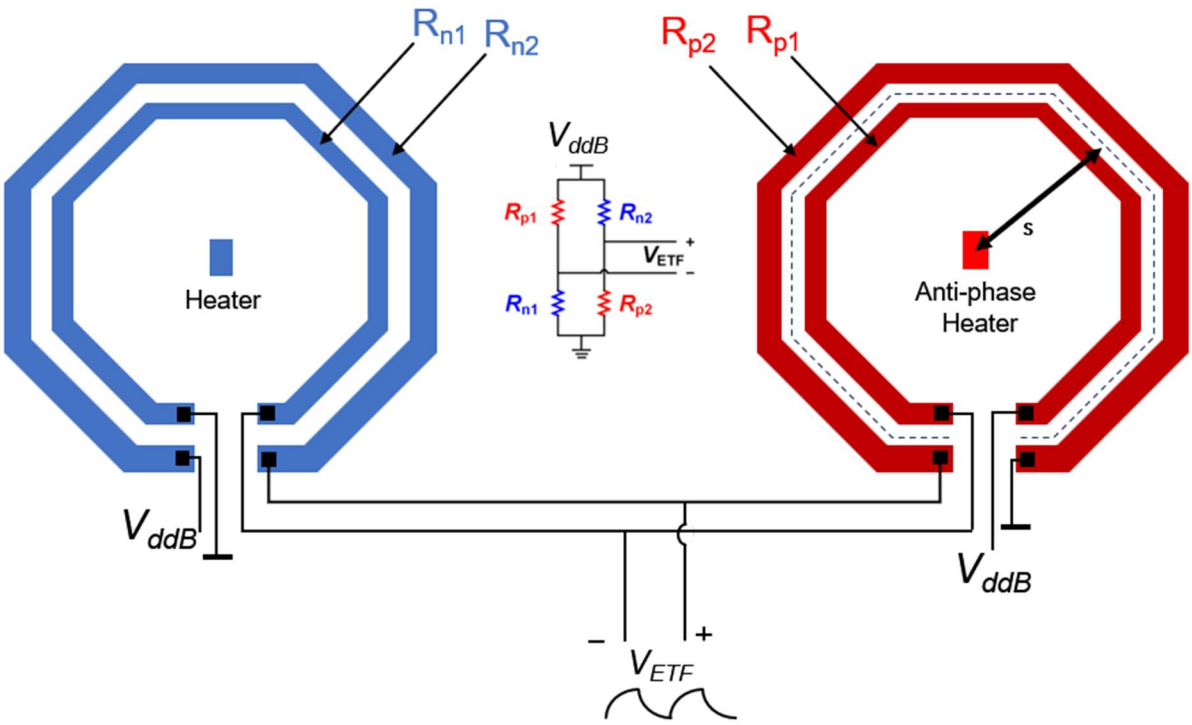


Figure 1.5: Ring ETF [13].

The resistance of a thermistor with a temperature coefficient, $T_{C,}$ can be expressed as:

$$R_{Ring}(T) = R_{Ring,nom} * (1 + \Delta T * T_C) \tag{1.12}$$

Where $R_{Ring,nom}$ is the thermistor's resistance at nominal temperature and ΔT represents small temperature changes.

The amplitude of the output of the Wheatstone bridge is then given by:

$$V_{out,bridge} = \frac{R_{Ring}(T)}{R_{Ring,nom}} * V_{ddB} \tag{1.13}$$

where V_{ddB} is the supply voltage of the Wheatstone bridge. The temperature sensitivity (S_{bridge}) of the $V_{out,bridge}$ can then be derived by taking the partial derivative of Equation 1.13, resulting in:

$$S_{bridge} = \frac{\partial V_{out,bridge}}{\partial T} = V_{ddB} * T_c \tag{1.14}$$

In the target CMOS 180nm technology, silicided diffusion resistors have the largest T_c (0.33%/°C), which results in a bridge sensitivity of 6mV/K, when V_{ddB}=1.8V. This is comparable with the sensitivity of a 16-arms thermopile (8mV/K).

As in thermopile ETFs, the sensing thermistors fully surround the heater, which maximizes their output signal. Moreover, their effective *s* is determined by a complete ring of diffusion, and not by a limited number of (hot) junctions, which should reduce lithography-related errors. However, they require more power since they require two heaters instead of one, and some power is needed to bias the Wheatstone bridge. They also suffer from higher output offset, due to the mismatch between the thermistors.

1.5.3 The Readout Circuit

As shown in Equation 1.9, at a constant driving frequency (f_{drive}), φ_{ETF} has a near-linear relation with temperature ($\propto T^{0.9}$). This can then be digitized by a phase-domain delta-sigma modulator (PD-DSM), as shown in Figure 1.6.

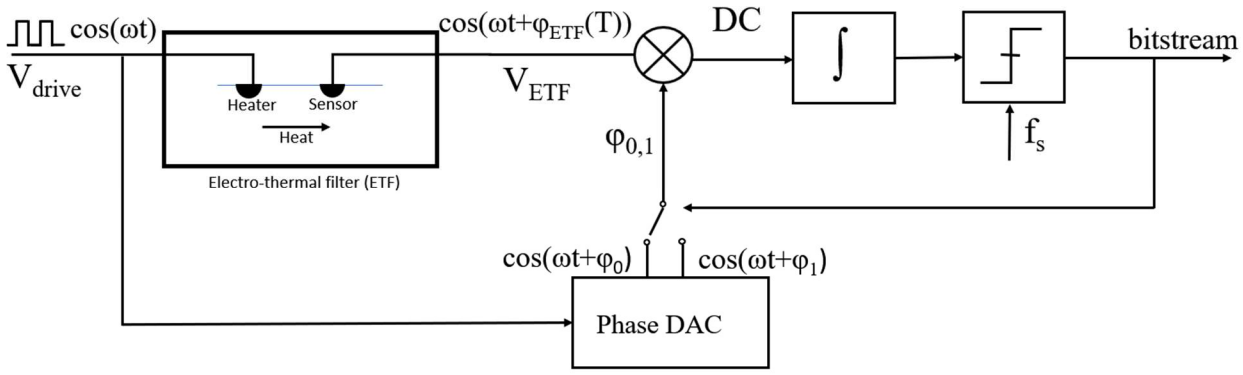


Figure 1.6: Block diagram of a Phase-domain delta-sigma modulator (PD-DSM). [9]

The ETF signal (V_{ETF}) is multiplied by a DAC signal ($\varphi_{0,1}$), which is at the same frequency, but has a phase-shift of either φ_0 or φ_1 depending on the value of the bitstream. This results in two components: a DC component containing the ETF's phase information, proportional to cos ($\varphi_{ETF} - \varphi_{0,1}$), and a high-frequency component. In the case of sinusoidal signals, this can be expressed as:

$$\begin{aligned} A_{ETF} * cos(2\pi f_{drive} t + \varphi_{ETF}) * cos\left(2\pi f_{drive} t + \varphi_{0,1}\right) \\ = \frac{1}{2} * A_{ETF} * cos\left(\varphi_{ETF} - \varphi_{0,1}\right) \\ + \frac{1}{2} * A_{ETF} * cos\left(4\pi f_{drive} t + \varphi_{ETF} + \varphi_{0,1}\right) \end{aligned} \quad (1.15)$$

where A_{ETF} is the amplitude of V_{ETF}. This signal is then applied to an integrator, which filters out the component at twice the frequency. The phase references (φ_0 and φ_1) are chosen such that $cos\ (\varphi_{ETF} - \varphi_0) > 0$ and $cos\ (\varphi_{ETF} - \varphi_1) < 0$, which means that the quantizer will toggle the reference phases such that the average DC current flowing in the integrator is zero, such that:

$$\mu \cos(\varphi_{ETF} - \varphi_1) + (1 - \mu)\, cos(\varphi_{ETF} - \varphi_0) \approx 0 \quad (1.16)$$

Where μ is the bitstream average, with a range between 0 and 1, which represents φ_{ETF} as a weighted average of the reference phases (φ_0 and φ_1):

$$\mu \approx \frac{\cos(\varphi_{ETF} - \varphi_0)}{\cos(\varphi_{ETF} - \varphi_0) - \cos(\varphi_{ETF} - \varphi_1)} \tag{1.17}$$

The resulting μ is thus a non-linear digital representation of φ_{ETF}. However, if $\varphi_{ETF} - \varphi_{0,1}$ is close to 90°, the cosine function is quite linear, leading to a linear relation between μ and φ_{ETF}:

$$\mu \approx \frac{\varphi_{ETF} - (90° + \varphi_0)}{\varphi_1 - \varphi_0} \tag{1.18}$$

In the case of square-wave input and reference signals, which are easier to generate and multiply, similar behavior is obtained. The multiplier demodulates the phase-shifted input signal to DC and any higher-order multiplication products are eliminated by the low pass filter.

1.6 State-of-the-art TD-based Temperature Sensors

To accurately read out an ETF, the phase error of the PD-DSM should be much less than that of the ETF. Since the ETF output is quite small (a few hundred µV peak-to-peak), this requires the use of precision analog circuits. This section reviews the design of previous PD-DSM readouts for TD-based temperature sensors.

In [10], an ETF and a PD-DSM were fabricated in 180nm CMOS bulk technology. This design achieved a state-of-the-art untrimmed inaccuracy of ±0.2°C (3σ) from -55°C to 125°C. The PD-DSM employed a fully differential, 1st order, single-bit architecture, whose single-ended block diagram is shown in Figure 1.7.

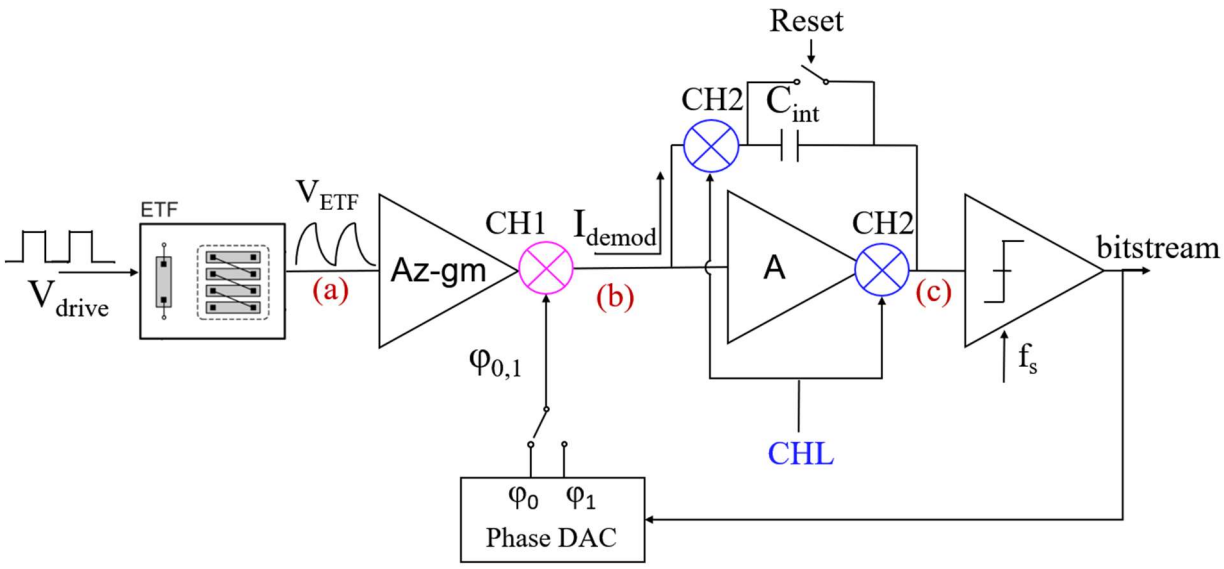


Figure 1.7: System-level architecture of PD-DSM designed in [10].

In this design, the output of the ETF is first converted to a current by a high-bandwidth gm-stage, after which it is demodulated (I_{demod}) and then applied to the DSM's integrator. The gm-stage consists of a gain-boosted folded-cascode operational transconductance amplifier (FC-OTA). The demodulator is implemented by a chopper (CH1) which is located between the source of the cascode transistors and the virtual ground of the gain-boosters [11], as shown in Figure 1.8.

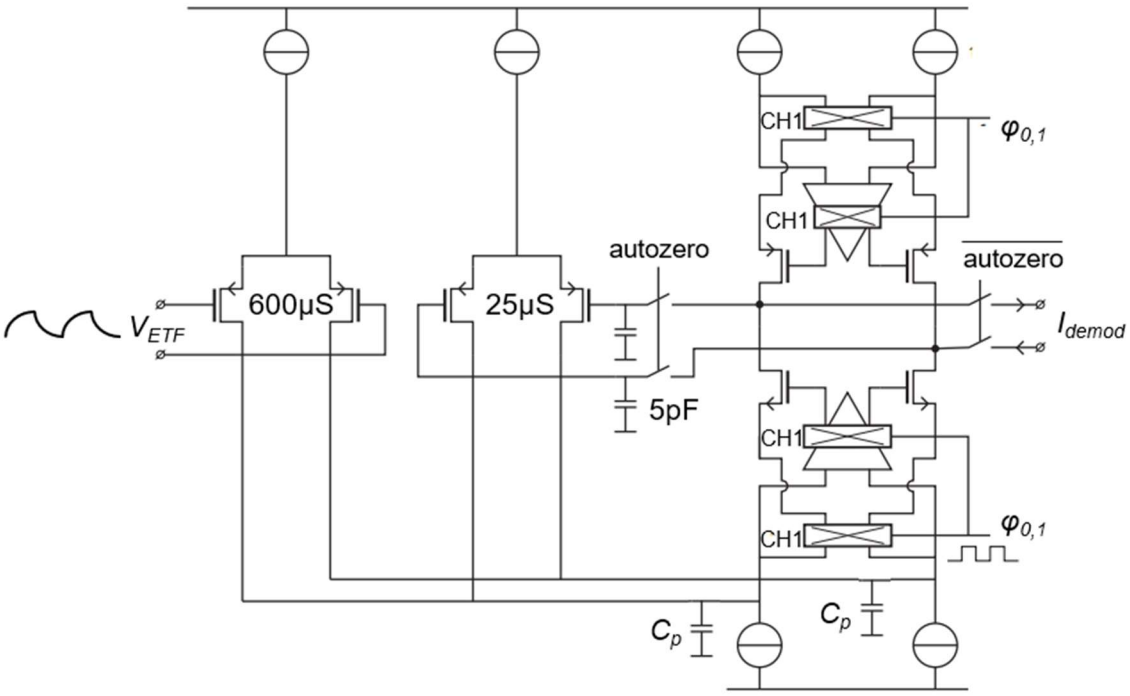


Figure 1.8: FC-OTA used in [10] showing the location of CH1.

Placing CH1 at a virtual ground mitigates the effect of the offset of the cascodes. This would otherwise cause a DC offset current at the OTA output, due to the periodic charging and discharging of the parasitic capacitance (C_P in Figure 1.8) at the folding node of the FC-OTA. The gain-booster establishes a virtual ground at this node, thereby reducing this offset current by its gain [11]. To maintain the correct feedback polarity, the output of the gain-booster amplifier is chopped as well.

Apart from demodulating the AC component of V_{ETF}, CH1 also up-modulates the input DC offset voltage (V_{OS}) from the ETF and the gm-stage. The resulting AC current (I_{offset}= $gm*V_{OS}$) causes a large voltage ripple (V_{ripple}) at the integrator output, which may cause the output of the integrator to clip. This is illustrated in Figure 1.9, where the sub-figures (a), (b), and (c), depict the transient waveforms at the respective nodes in Figure 1.7.

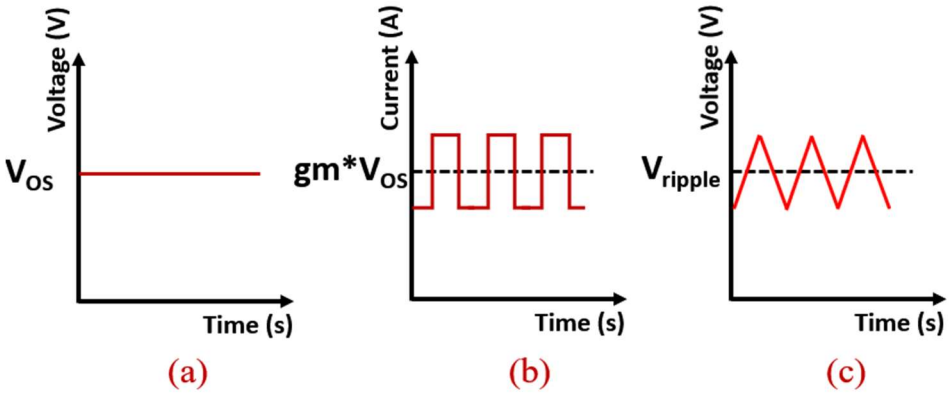


Figure 1.9: Upmodulated DC offset in PD-DSM.

In [10], V_{OS} is reduced by auto-zeroing the gm-stage at the start of every PD-DSM conversion. As shown in Figure 1.8, this is done with the help of an auxiliary trans-conductor, which cancels the differential offset current at the OTA output when the auto-zero switches are closed. As the DC component of V_{ETF} is also a significant source of offset, the ETF is driven at a much higher frequency ($16f_{drive}$) during AZ, which preserves its DC component while suppressing its AC component. As a result, the auto-zero loop compensates for both thermal and device offsets.

Low-frequency choppers (CH2 in Figure 1.7) suppress the offset current associated with the charge injection of the CH1 switches, and any other offset currents. They periodically reverse the polarity of these DC errors and convert them to AC signals, which are then filtered out by the decimation filter of the DSM. The timing diagram of the *CHL* (low-frequency chopping signal) and its effect on the polarity of the heater drive signal V_{drive} is shown in Figure 1.10. The *AZ* and the *Reset* signal are triggered at the start of each *CHL* phase. This results in a residual offset current of less than 7.5 pA.

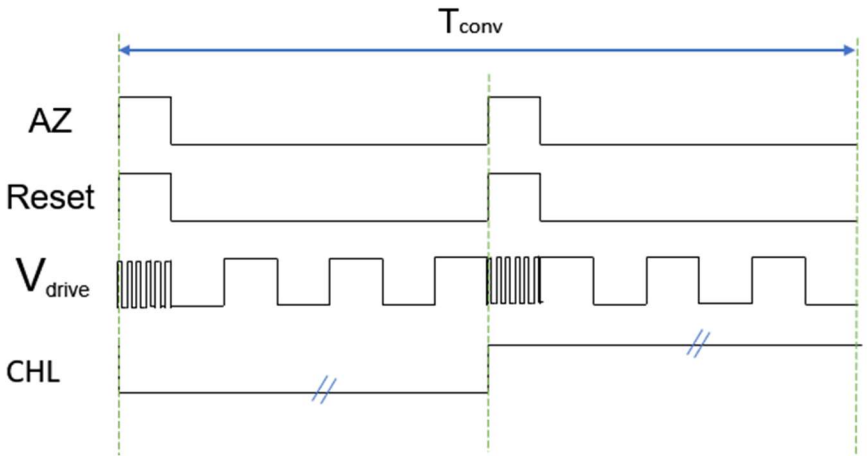


Figure 1.10: System- Level chopping timing diagram.

In [14], a TD sensor based on a polygon ETF (as shown in Figure 1.4) is implemented in 180nm CMOS bulk technology. It is read out by a 2nd order DSM with a switched capacitor (SC) based 2nd stage, as shown in Figure 1.11. The resulting TD sensor achieved an untrimmed inaccuracy of 0.3°C from -55°C to 125°C.

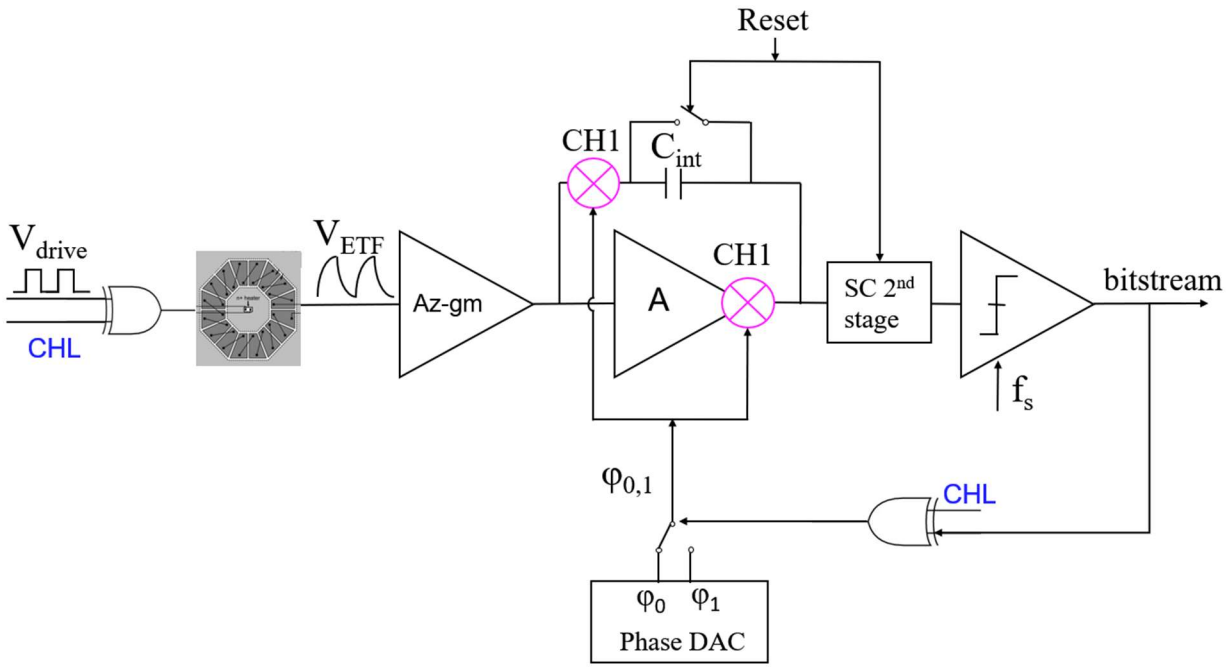


Figure1.11: System-level architecture implemented in [14].

The design in [14] also employs an auto-zeroed gm-stage. Compared to [10], the main architectural difference is in the implementation of the low-frequency choppers (CH2) and the location of the demodulator (CH1). In this design, they are merged and placed in series with the integration capacitor. The low-frequency chopping is then performed by using XOR gates to periodically (CHL=100 Hz) invert the polarity of V_{drive} and $\varphi_{0,1}$.

To extend the operating temperature range of TD-based sensors, a 1st order PD-DSM based on a gm-C integrator is implemented in a 0.5um silicon-on-insulator (SOI) BiCMOS process [15]. Its block diagram is shown in Figure 1.12. The resulting TD sensor achieves an inaccuracy of 0.6°C from -70°C to 225°C.

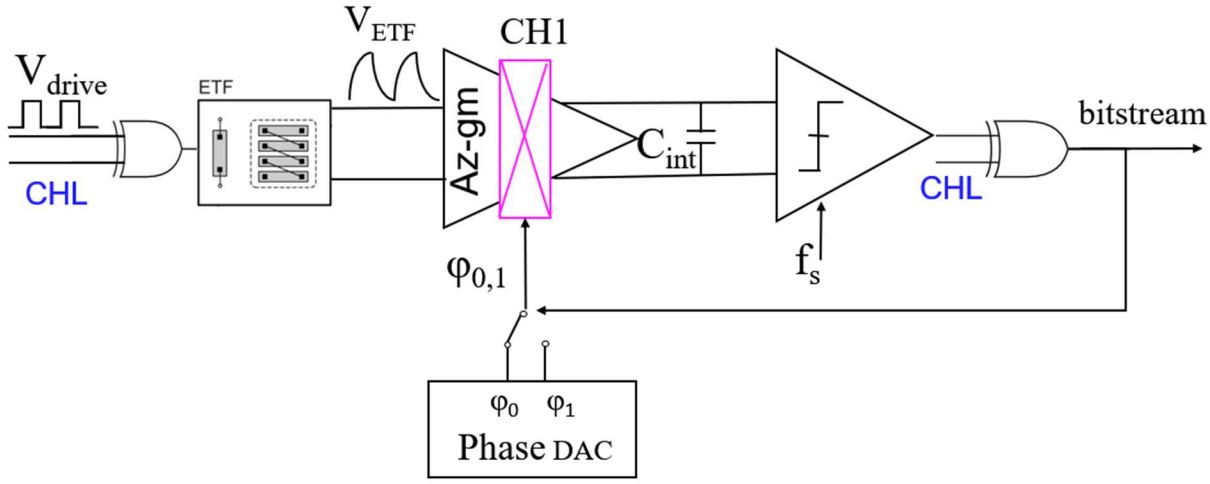


Figure 1.12: System-level architecture of [15].

The use of SOI technology allows the readout circuitry to operate up to high temperatures because all the devices can be fully isolated, which in turn reduces the effect of leakage currents. Furthermore, ETFs realized in SOI technology benefit from the fact that less heater power is lost to the substrate, resulting in a larger output signal and a 7 times better SNR with sub-mW of P_{heater} [15].

As in [10], phase detection is achieved by embedding CH1 in the OTA. Similarly, the OTA is auto-zeroed to suppress its offset. The low-frequency chopping is done using XOR gates.

1.7 Design Target

Table 1.2 summarizes the performance of the TD sensors and readout architectures discussed in the previous section.

Table 1.2: Overview of PD-DSM specifications.

	Casper ISSCC'10 [10]	Casper Sensors'12 [15]	Sining ISSCC'21 [14]	Target
Sensor type	**Thermopile ETF**	**Thermopile ETF**	**Thermopile ETF**	**TP/Ring ETF**
CMOS Technology	0.18um	0.5um SOI BiCMOS	0.18um	0.18um
Area (mm^2)	0.18	1	0.2	0.2
Temp Range (°C)	-55 to 125	-70 to 225	-55 to 125	-55 to 180
(3σ) Inaccuracy (°C)	±0.2	±0.6	±0.3	±0.2
Power (mW)	3	3.5	5.1	5/10
Conversion time (ms)	6250	1000	1000	1000
Resolution (mK)	20	26	15	15

Despite achieving excellent inaccuracy (0.2°C from -55°C to 125°C), the TD-sensor in [10] required a long conversion time (~6s) to achieve commensurate resolution (~20 mK). This was mainly due to the ETF's low SNR. Therefore, in [14], this was improved by using a polygon ETF with five times less R_{TP} and two times more heater power. This achieved 15mK resolution in a 1s conversion time, but worse inaccuracy (0.3°C) over the same temperature range. The operating temperature range of both [10] and [14] is limited by the leakage current of the auto-zeroing switches used in the designs [16]. Using low-leakage SOI technology [15], the temperature range could be extended, but the resulting inaccuracy was only 0.6°C from -70°C to 225°C.

The main goal of this work is to design a readout architecture for TD-based sensors realized in standard CMOS technology, which is capable of operating at temperatures above the military range while achieving an untrimmed inaccuracy of 0.2°C. Furthermore, the proposed readout should also be compatible with ring ETFs, which exhibit significant DC offset.

1.8 Organization of Thesis

The thesis is organized as follows:

- Chapter 2 discusses the system-level design of the proposed readout architecture. The error sources of the ETFs and the readout circuitry are analyzed and their design implications are discussed. Finally, an error budget for achieving the desired accuracy is established.
- Chapter 3 presents the circuit-level implementations of all the sub-blocks in the readout system. Additionally, the scalability of the PD-DSM concerning the ETF structures is discussed.
- Chapter 4 illustrates the measurement setup and the obtained results from the chip, such as phase characteristics, inaccuracy, and resolution. Furthermore, the design errors and their effects on the system performance are documented.
- Chapter 5 concludes the work and proposes future design improvements.

2. System Design

This chapter discusses the system-level design of the TD-based temperature sensor in a TSMC 180nm CMOS technology. Section 2.1 describes the ETFs implemented in this work, while Section 2.2 discusses the system-level specifications of the readout circuit (PD-DSM). In Section 2.3 the main error sources of a TD sensor are discussed. In Section 2.4 the non-idealities of its phase demodulator together with ways to mitigate them are discussed. Section 2.5 introduces some offset cancellation techniques. Lastly, in Section 2.6, the error budgeting based on the discussed errors is summarized.

2.1 ETF Structures

In this work, four different ETF structures are implemented, together with their associated readout circuits. In [10], [14], and [15], thermopile ETFs with *s*= 24 µm were implemented. To enable a direct comparison with this work, a polygon TP-ETF with *s*= 24 µm is implemented (referred to as an S24 ETF). An S24 ring ETF (see Section 1.5.2) is also implemented to compare its performance with that of the S24 TP-ETF. Furthermore, to examine the effect of reducing *s* on accuracy and resolution, half-size ETFs with *s*= 12 µm (referred to as S12 ETFs) are also implemented.

2.2 PD-DSM System-Level Architecture

The readout consists of a fully differential, first-order, single-bit PD-DSM. For simplicity, Figure 2.1 shows a single-ended representation of the proposed architecture. In this section, the system-level design choices are discussed. These are initially based on the requirements of the S24 TP/Ring ETFs and are adjusted later (in Chapter 3) to meet the requirements of the half-size ETFs.

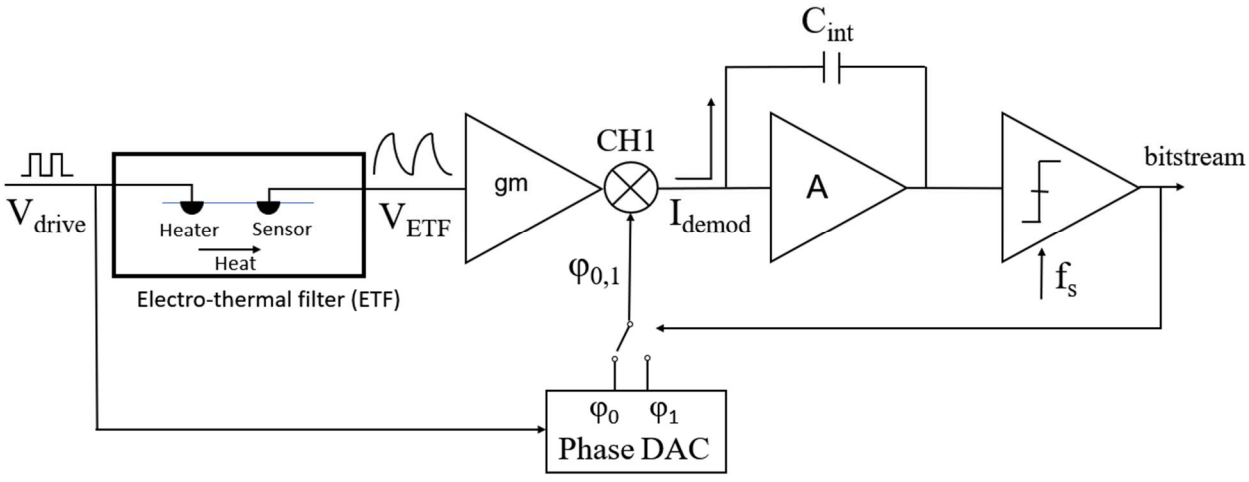


Figure 2.1: Proposed first-order single-bit PD-DSM.

As discussed in section 1.5.2, the main sources of inaccuracy in an ETF are lithographic errors and finite BW. From Equation 1.10, the expected lithographic spread (10% of 180nm) in the targeted 180nm technology, together with the phase sensitivity (4.8°C/°ϕ) of the S24 TP-ETF implemented in [9], translates into an inaccuracy of ±0.2°C. Moreover, simulations show that the ETF exhibits an absolute phase error of 15m°ϕ when driven at f_{drive} = 30kHz (as in [23]), which translates into an absolute

temperature error of 0.072°C. As the spread of phase error related to the finite ETF BW will be even smaller, this error source is neglected compared to the lithographic error.

The PD-DSM readout in this work is designed to ensure that its phase error is less than 20% of the total temperature error, or 0.04°C, which is equivalent to a phase error of less than ±8.3m°ϕ.

For a resolution of 15mK over the targeted -55°C to 180°C operating range, the PD-DSM should achieve a resolution of 14 bits. This should be dominated by thermal noise, and so its quantization noise should be even lower. Assuming that the modulator's output is decimated by a 1st-order sinc filter, then a 1s conversion time (T_{conv}) corresponds to a noise bandwidth of 0.5Hz. At a sampling frequency, $f_s = f_{drive} \approx$ 30kHz, the modulator's OSR is 30,000, which translates into a quantization-noise-limited resolution of ≈ 15 bits. As discussed in Section 1.5.2, if *s* is scaled from 24 µm to 12 µm, then f_s must be increased by 4x to ≈ 120kHz, which increases the OSR by 4x, and the quantization-noise-limited resolution to ≈ 17 bits. Hence, for both S24 and S12 ETFs, a first-order PD-DSM can achieve sufficient SQNR.

In the designed architecture, as in [10], [14], and [15], V_{ETF} is converted into an AC current by a high-bandwidth gm-stage. Its transconductance, *gm*, is set by noise requirements. For the ETF's sensing resistors (R_{ETF}) to be the main source of noise, *1/gm* must be less than R_{ETF}. The resistance of the S24 TP-ETF described in [23] is ≈4kΩ, while the resistance of the S24 ring ETF (R_{Ring}) is ≈950Ω. Therefore, *gm* should be greater than 1mS. In this work, the designed *gm* value is 1.4mS, and a detailed noise analysis is provided in Chapter 3.

The allowable output swing of the integrator dictates the value of C_{int}. From Equation 1.15, when the phase-shifted AC output current of the gm-stage (V_{ETF} * *gm*) is multiplied by a square wave reference signal, the resulting DC current (I_{demod}) is given by [9]:

$$I_{demod} = \frac{4}{\pi^2} V_{ETF} * gm * \cos\left(\varphi_{ETF} - \varphi_{0,1}\right) \tag{2.1}$$

The largest signal current corresponds to the full DAC range and is proportional to $\cos(\varphi_0 - \varphi_1)$. The voltage integrated on C_{int} in one sampling period ($1/f_s$), then has a peak-to-peak swing of:

$$V_{swing,pk-pk} = \frac{8}{\pi^2} V_{ETF.pk-pk} * \cos(\varphi_1 - \varphi_0) * \frac{gm}{C_{int1} f_s} \tag{2.2}$$

With P_{heater} = 4.2mW, the S24 TP-ETF reported in [14] had an output swing $V_{ETF,pk-pk}$ ≈500µV. With phase references 22.5°ϕ and 67.5°ϕ and f_s = 30kHz, choosing C_{int} = 28pF results in a peak-to-peak integrator swing of ≈473mV. This can be readily achieved by a simple and robust folded-cascode OTA operating from a 1.8V supply.

2.3 System Error Sources

2.3.1 Temperature error due to self-heating

In an ETF, the DC component of P_{heater} will cause a temperature gradient in the silicon around the heater [9]. As a result, there will be a DC offset in V_{ETF}, which also needs to be processed by the readout circuit. From Equation 1.5, this temperature offset ($T_{DC,local}$) at a radius *s* is given by [9]:

$$T_{DC,local}(s) = P_{heater} * Z_{th}(s) = P_{heater} \frac{1}{2\pi k_{si} s} \tag{2.3}$$

With P_{heater} = 4.2mW, s = 24µm and k_{Si} = 156 W/m/K at 300K [8], this results in a temperature offset of 0.18°C. This can be corrected by calibration, but then variations in the heater resistance or the supply voltage will cause variations in P_{heater} and temperature spread. A 10% variation in P_{heater} will result in an error of 0.018°C. Since a TP-ETF senses the temperature difference between its *hot* and *cold* junctions, the resulting spread in its output will be smaller than in the case of a ring ETF, which only senses absolute temperature.

There will also be a temperature offset due to the finite thermal impedance of the package. A typical ceramic package has a thermal resistance $R_{package}$ of 50°C/W [9], which will also spread depending on how the package is mounted on the PCB. The associated DC offset is given by:

$$T_{DC,package}(s) = P_{heater} * R_{package} \tag{2.4}$$

A 10% variation in packaging impedance will then result in an additional spread of 0.021°C. The total error due to self-heating is therefore about 0.04°C, which is significant when targeting 0.2°C inaccuracy. It can be reduced by reducing the heater power but at the expense of reducing the output of the ETF.

2.3.2 Phase error due to timing delay

To achieve high accuracy, the phase relationship between the heater drive signal (V_{drive}) and the phase references ($\varphi_{0,1}$) used in the DAC of the PD-DSM must be defined precisely. The phase error associated with a timing delay can be expressed as:

$$\varphi_{err} = delay * f_{drive} * 360° \tag{2.5}$$

Where f_{drive} is the driving frequency of the ETF. This means that for an absolute temperature error of e.g., 0.01°C, which translates into a phase error of 2m°ϕ, the delay must be less than 185 ps. To achieve such small delays, both the heater drive signal and the phase references must be generated on-chip.

2.3.3 Phase error due to the finite BW of ETF and gm-stage

Any phase shift in the signal path between V_{ETF} and the output of the gm-stage (I_{signal}) will also introduce errors since it will be indistinguishable from φ_{ETF}.

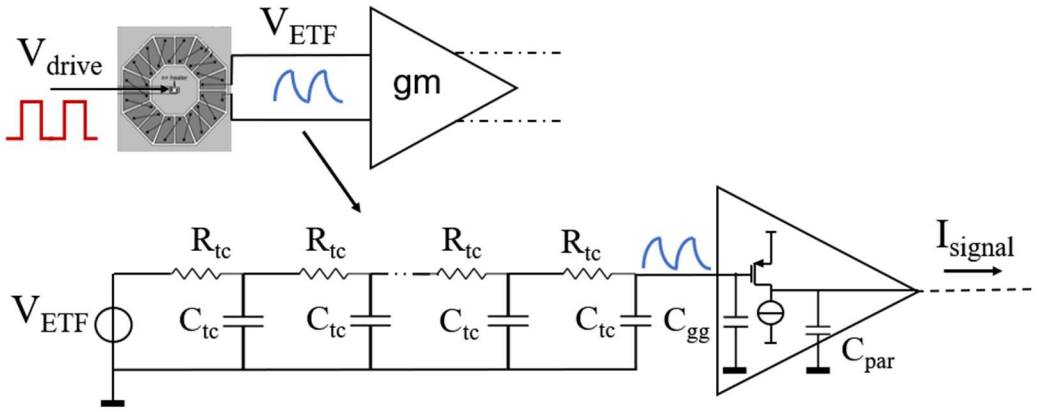


Figure 2.2: Phase offset associated with input and output capacitance (C_{gg} and C_{par}) of gm-stage.

As shown in Figure 2.2, an ETF can be modeled as a distributed RC low-pass filter, where R_{tc} and C_{tc} are the resistance and capacitance of thermocouples [17]. The ETF's total resistance R_{ETF} and the input capacitance (C_{gg}) of the gm-stage also form a low-pass filter, while the finite bandwidth of the gm-stage forms yet another low-pass filter. Therefore, the spread in the input and output parasitic capacitances (C_{gg} and C_{par} in Figure 2.2) of the gm-stage will cause a spread in φ_{ETF}. To reduce this, the associated parasitic poles should be designed to be at a sufficiently high frequency.

The phase error of a 1st-order low-pass filter is given by:

$$\varphi_{err} = -\arctan\left(\frac{f_{drive}}{f_{-3dB}}\right) * \frac{180°}{\pi} \tag{2.6}$$

where f_{-3dB} is its corner frequency. To achieve a temperature error of less than 0.01°C, or 2 m°ϕ at f_{drive} = 30kHz, f_{-3dB} must be greater than 800MHz. For an S24 TP-ETF, R_{ETF} ≈4kΩ, which means that C_{gg} must be around 50fF (ignoring the ETF's own parasitic capacitance). Achieving such a small capacitance puts a strong constraint on the design of the gm-stage. As in [9], to relax this requirement, the input capacitance is designed such that the *spread* on φ_{err} is below the target error levels. Assuming a 5% variation in input parasitic capacitances across PVT, the spread in the phase error must be 2 m°ϕ at f_{drive}. This translates into approximately C_{gg} of 1pF.

2.4 Electrical offset

Figure 2.3 shows a simplified ETF model consisting of an ideal voltage source, the ETF's total resistance, $R_{ETF,}$ and the ETF's parasitic capacitance, C_{ETF}, connected to a gm-stage. Any DC offset added to the output of the demodulator (I_{demod}) will cause an apparent phase error at the output of the PD-DSM.

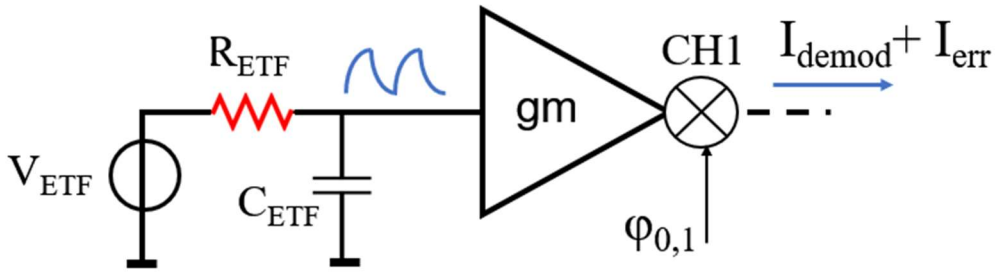


Figure 2.3: Error current contributing to $\varphi_{ETF.}$

Since the integrator in the PD-DSM will average its input current to zero, then:

$$\int_0^{T_{conv}} I_{demod} = \int_0^{T_{conv}} I_{err} \tag{2.7}$$

As shown in [24], the phase error φ_{err} associated with I_{err} can then be expressed as:

$$\sin(\varphi_{err}) = \frac{2I_{err}}{V_{ETF} * gm} \tag{2.8}$$

Then with V_{ETF} =500µV and gm=1.4mS, for an absolute temperature error of 0.01°C, which corresponds to a phase error of 2m°ϕ, the resulting I_{err} must be < 12pA. The following sub-sections discuss two main causes of I_{err}, and discuss ways of mitigating them.

2.4.1 Electrical offset due to the demodulator

As shown in Figure 2.1, the PD-DSM employs a demodulator chopper, which is realized by four switches, as shown in Figure 2.4.

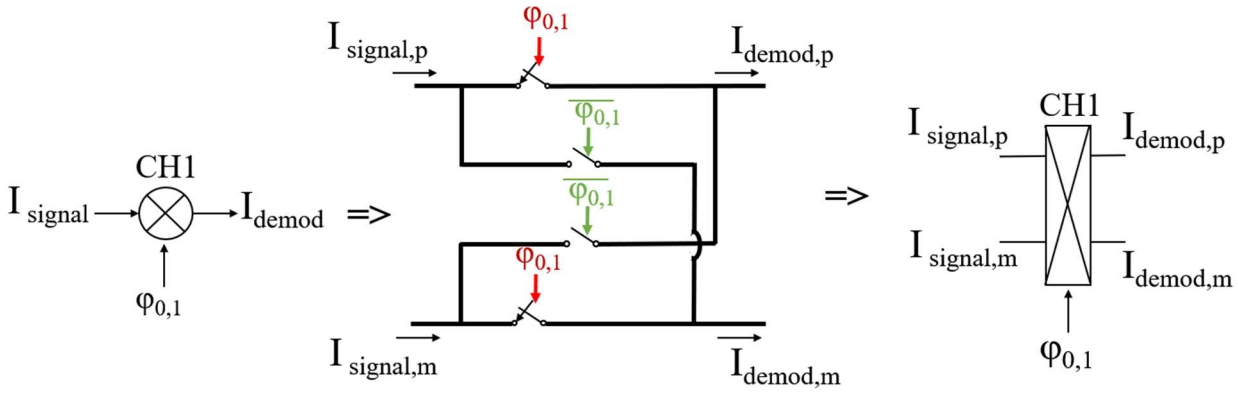


Figure 2.4: Demodulator Chopper.

The charge injection (CI) mismatch of these switches ΔQ_{inj} results in a differential error current in the demodulator's output current I_{demod}. The error current $I_{Cinj,CH1}$ can be expressed as [9]:

$$I_{Cinj,CH1} = 2 * f_{drive} * \Delta Q_{inj} \tag{2.9}$$

Since Q_{inj} scales linearly with switch area, minimum-size switches will have the lowest $I_{Cinj,CH1}$. In the targeted CMOS 180nm technology, a minimum-size switch (W/L = 220nm/180nm), has a total gate capacitance of 0.4fF. The channel charge ($Q_{ch} = WL*C_{ox}*(V_{GS}-V_{TH})$), is then 13 fC, assuming a typical overdrive of V_{GS}-V_{TH} ≈ 300 mV. At f_{drive}=30kHz, the corresponding CI current is 0.78nA. As a result, $I_{Cinj,CH1}$ = 78pA, assuming a 10% charge injection mismatch. This error current is significant compared to the targeted I_{err}, and so it must be suppressed. As will be discussed in Section 2.4.3, this can be done with low-frequency (LF) chopping.

2.4.2 Integrator Offset

The input-referred offset of the integrator OTA ($V_{OS,OTA}$) is another source of DC error current (I_{err}). Due to the finite output resistance of the gm-stage, $R_{out,gm}$, this voltage will generate an error current $I_{OS,OTA}$ in the demodulator's output current I_{demod} as shown in Figure 2.5.

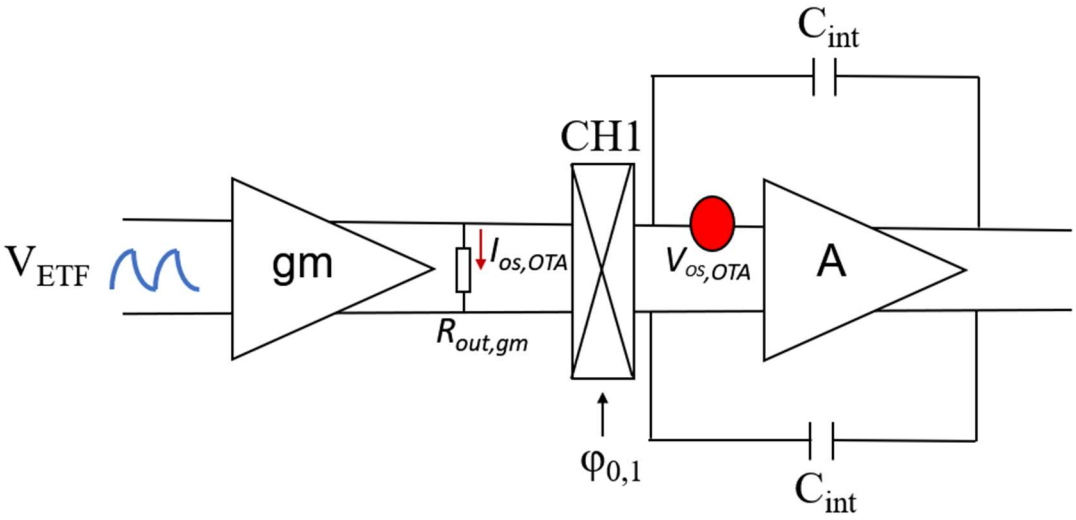


Figure 2.5: Error current due to integrator OTA's voltage offset.

Assuming that the worst-case $V_{OS,OTA}$ is 10mV, then $R_{out,gm}$ should be at the GΩ level to ensure that $I_{OS,OTA}$ is at the pA level. However, this offset current will also be mitigated by low-frequency chopping.

2.4.3 Low-frequency Chopping

As shown in Figure 2.6, low-frequency chopping can be used to suppress the offset current caused by the demodulator's CI mismatch and by the input-referred voltage offset of the integrator OTA [10].

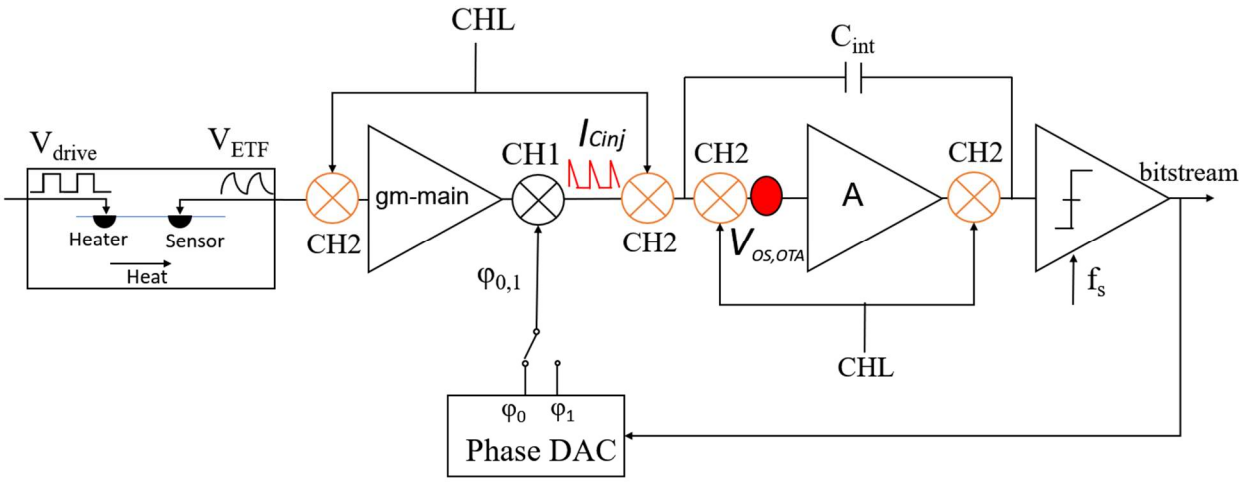


Figure 2.6: Low-frequency choppers (CH2).

The associated low-frequency choppers (CH2) convert the offset current into an AC current that can then be filtered out by the decimation filter of the PD-DSM. The low-frequency choppers are driven at a frequency much lower than f_s. In this work, they are operated at 1 Hz, by switching their polarity after every DSM conversion.

As noted in [10], the LF chopper at the ETF output can be shifted through the ETF and simply implemented by reversing the polarity of V_{drive}. In addition, the two LF choppers at the virtual ground of

the integrator can be combined and shifted into the integrator's feedback path. This simplified placement of the low-frequency choppers is shown in Figure 2.7.

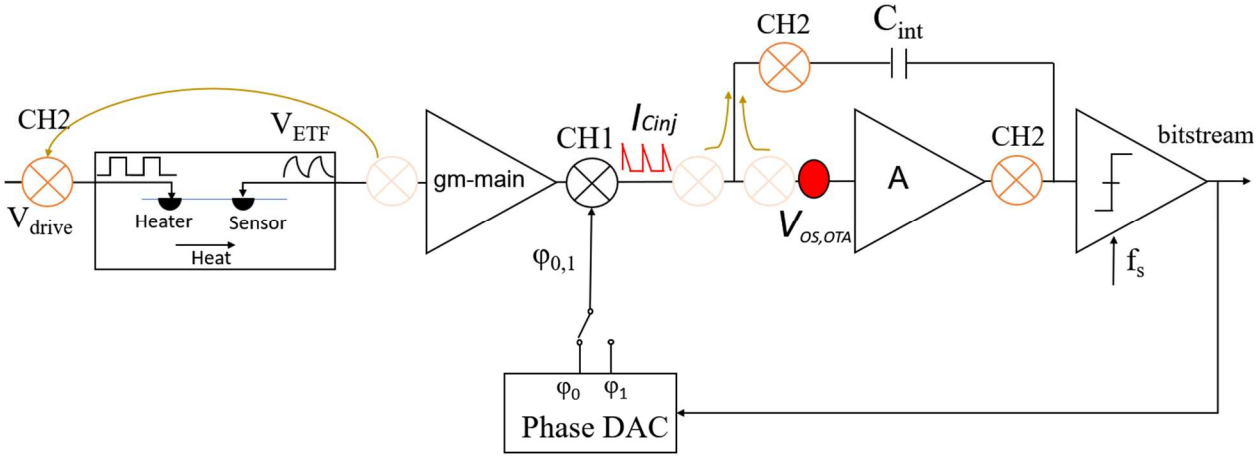


Figure 2.7: Simplified placement of low-frequency choppers.

2.4.4 Demodulator Location

There are three options for the location of the chopper demodulator of the PD-DSM, Figure 2.8 shows these three options, and their characteristics are explained below:

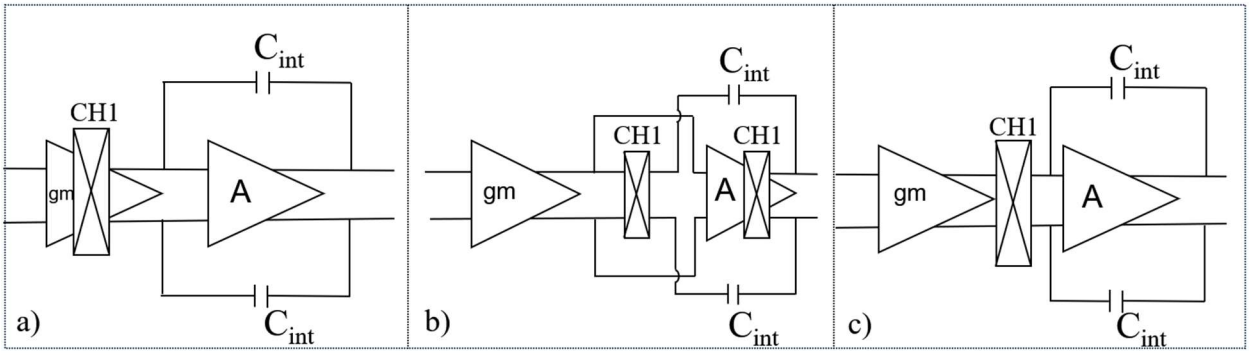


Figure 2.8: Different demodulator chopper (CH1) locations.

a) The first option is to place the choppers inside the gm-stage, i.e., at the sources of the cascode transistors, as in [10] and [15]. However, as discussed in Section 1.6, the charging and discharging of the parasitic capacitance at this node by the DC offset of the cascode transistors result in a DC error current. In [10] this is mitigated by gain-boosting the OTA, which creates a virtual ground at the input of the choppers.

b) Another option is to place the chopper switches in series with the integration capacitors, as was done in [14]. The LF output chopper can then be implemented by simply reversing the polarity of CH1 using XOR gate, as in [14]. However, this means that its own CI current may not be effectively canceled.

c) In this work, the demodulator is placed between the output of the gm-stage and the virtual ground of the integrator. This ensures that the voltage offset of the cascode devices does not contribute to the DC current at the output of the demodulator. The low-frequency chopping is then implemented as shown in Figure 2.7.

2.5 Ripple Reduction Techniques

As explained in Section 1.6, the chopper demodulator also up-modulates the low-frequency noise and DC offset of the ETF ($V_{os,ETF}$) and the gm-stage ($V_{os,gm}$) to harmonics of the chopping frequency. This is illustrated in Figure 2.9(a) and (b).

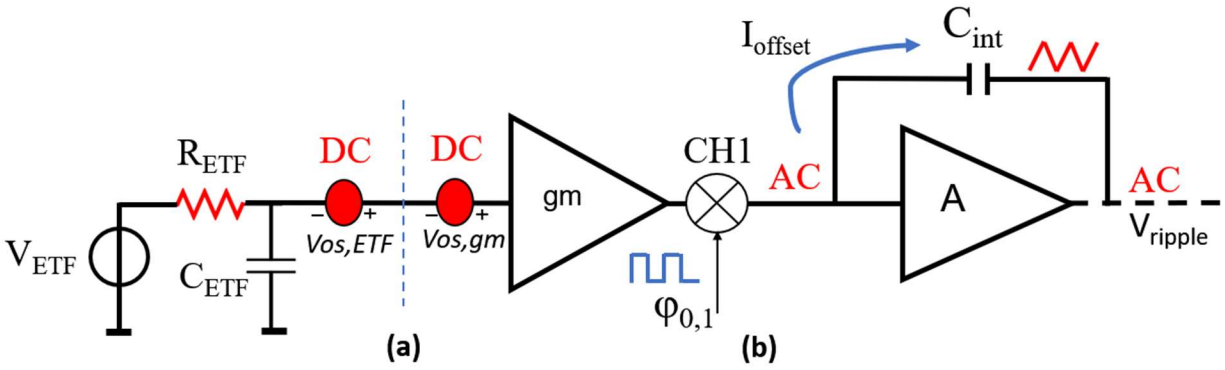


Figure 2.9 (a): Up-modulated DC offset.

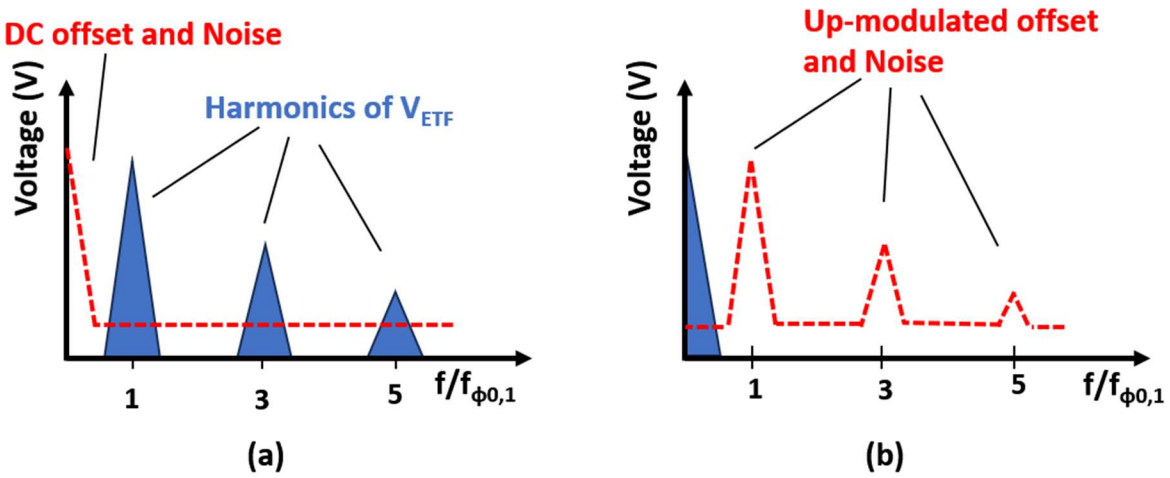


Figure 2.9 (b): Upmodulated DC offset in the frequency domain.

The up-modulated input offset (V_{OS} =$V_{OS,ETF}$ + $V_{OS,gm}$) is a square wave, which is converted into a triangular wave (V_{ripple} in Figure 2.9(a)) at the output of the integrator. The peak-to-peak amplitude of the V_{ripple} is given by [18]:

$$V_{pk-pk,ripple} = \frac{V_{os} * gm}{2C_{int} * f_{\varphi 0,1}} \tag{2.10}$$

As discussed in Section 1.5.2, the mismatch of the various resistors of a ring ETF may also cause significant offset $V_{os,\,ETF}$. Monte Carlo mismatch simulations on an s=24µm ring ETF with minimum width resistors show that $V_{os,\,ETF}$ is 16 mV (3σ).

Assuming that $V_{os,\,ETF}$ dominates the total offset at the OTA's input, then with gm = 1.4mS, C_{int} = 28pF, and f_{drive} = 30kHz, $V_{pk\text{-}pk,\,ripple}$ is 13.33V_{pp}, which will certainly clip the integrator's output. Therefore, it must be reduced.

2.5.1 Reducing Chopper Ripple

One way to reduce V_{OS} is to use auto-zeroing, as was done in [10], [14], and [15]. However, the offset voltage must then be stored on an auto-zeroing capacitor without leaking during the DSM conversion time. Since leakage increases exponentially with temperature, this is not effective at temperatures above 125°C [16].

To avoid the need to store the offset voltage on a capacitor for the whole of the PD-DSM's conversion (≈1s), an offset-cancellation technique that operates during the conversion is a better approach. In this work, a ripple reduction loop (RRL) [18] is used, as shown in Figure 2.10.

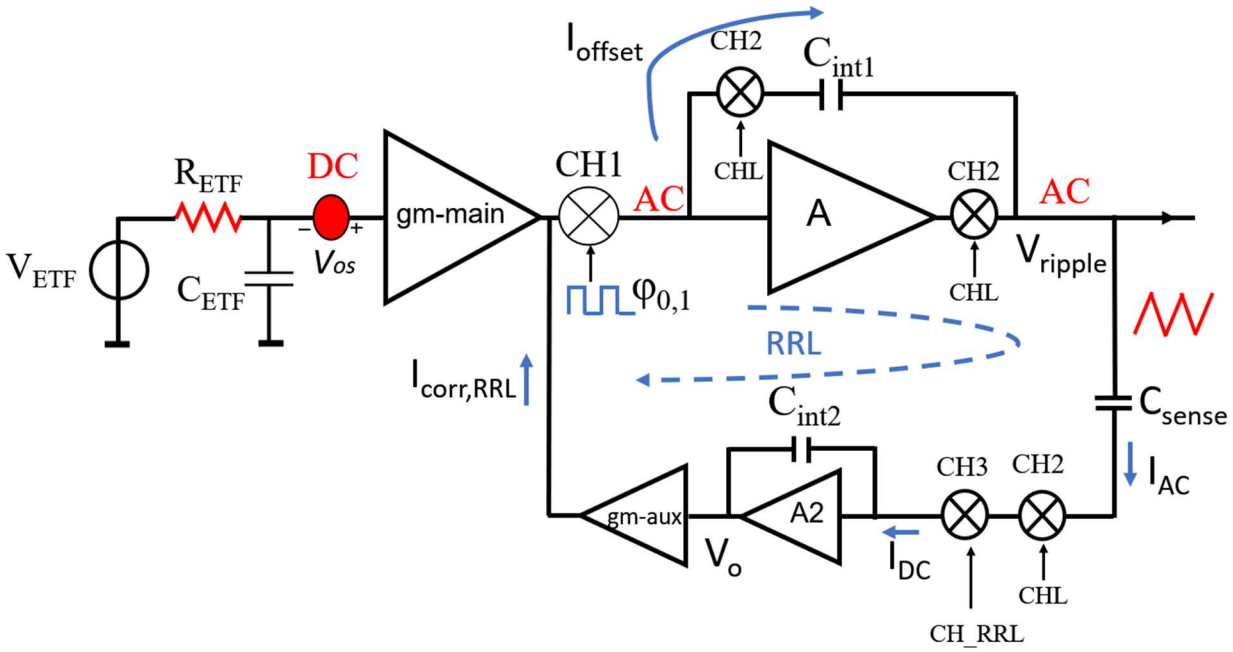


Figure 2.10: Block diagram of PD-DSM with RRL.

The RRL consists of a sense capacitor, C_{sense}, a chopper, CH3, an integrator, A2 with $C_{int2,}$ and a compensation transconductance, gm-aux. The sense capacitor converts the output ripple, V_{ripple} into an AC current I_{AC}, which is proportional to the derivative of V_{ripple}, given by:

$$I_{AC} = C_{sense}\frac{dV_{ripple}}{dt} \tag{2.11}$$

The AC current (I_{AC}) is then demodulated by the chopper CH3, running at frequency f_{CH_RRL}=$f_{drive,}$ and with the same phase-shifted phase-DAC output signal (φ_0, φ_1) as CH1. The resulting DC current (I_{DC}) is

integrated by A2 and C_{int2}, generating a DC compensation voltage V_o that is proportional to the ripple amplitude. This is then fed back via an auxiliary transconductance (gm-aux) to cancel the offset of gm-main. A low-frequency chopper, CH2, is added in the RRL to maintain the correct polarity of the current injected in gm-main during the low-frequency chopping in the signal path (as discussed in Section 2.4.4). Figure 2.11 shows the waveforms in the RRL.

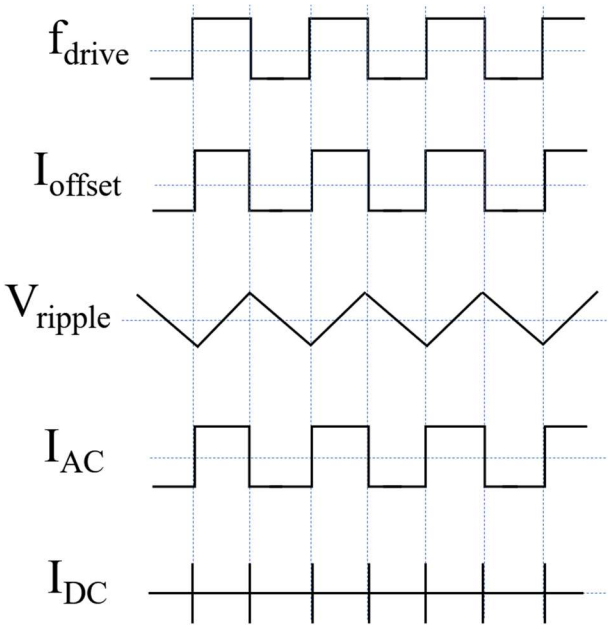


Figure 2.11: Transient waveforms in RRL.

Since both the input offset and the correction current provided by the RRL are DC signals, the offset reduction ratio is determined by the DC Loop gain of the RRL. As derived in [19], the Loop Gain *(L(s))* is given by [19]:

$$L(s) = \frac{C_{sense}}{C_{int}} \frac{Z_{SCsense} A_{2,DC}}{1 + sZ_{SCsense}\left(1 + A_{2,DC}\right)C_{int2}} gm_{aux} \tag{2.12}$$

Here, $Z_{SCsense}$ is the impedance looking into the RRL demodulator (CH3) from the virtual ground of the integrator A2 and is given by:

$$Z_{SCsense} = \frac{1}{f_{CH\_RRL} * C_{sense}} \tag{2.13}$$

The DC Loop gain (L_{DC}) that corresponds to the offset reduction ratio is then given by:

$$L_{DC} = A_{2,DC} Z_{SCsense} \frac{C_{sense}}{C_{int2}} gm_{aux} = \frac{A_{2,DC} * gm_{aux}}{C_{int2} * f_{CH\_RRL}} \tag{2.14}$$

To avoid clipping the DSM, the magnitude of the $V_{pk\text{-}pk,\ ripple}$ must be reduced to a fraction of the signal swing at the output of the integrator. As discussed in Section 2.2, the output signal swing is ≈473mV$_{pp}$. Setting V_{ripple} to 10% of this (≈47mV$_{pp}$) and using Equation 2.10 means that the input referred offset must be less than 56.4µV. Since the combined initial offset of the ETF and the gm can be as large as 16mV, the offset reduction ratio must be > 284.

The RRL also acts like a high pass filter for the DC offset voltage. From [19], its -3db high pass corner frequency is given by:

$$f_{c,HPF} = \frac{C_{sense}}{2\pi * C_{int1}} * \frac{gm_{aux}}{C_{int2}} \quad (2.15)$$

The phase error generated by this high pass corner frequency can then be estimated as:

$$\varphi_{err,HPF} = -arctan\left(\frac{f_{c,HPF}}{f_{drive}}\right) * \frac{180°}{\pi} \quad (2.16)$$

For $\varphi_{err,HPF}$ of less than 2 m°ϕ at f_{drive}=30kHz, $f_{c,\,HPF}$ must be less than 1 Hz.

As discussed in Section 2.2, C_{int1} = 28pF is determined by the integrator output swing. Considering the area, C_{int2} was chosen to be equal to C_{int1}. The freedom to design $f_{c,HPF}$ is then limited to selecting the values of C_{sense} and gm-aux.

However, a trade-off exists between the amplitude of the current entering the RRL, I_{AC}, as given by Equation 2.11, and the size of C_{sense}, because the charge injection current $I_{Cinj,\,CH3}$ generated by the RRL demodulator (CH3) will cause an error current in I_{AC}. To minimize this, C_{sense} must be chosen such that $I_{AC} > I_{Cinj,CH3}$. For a ripple amplitude of 47mV and f_{drive} = 30kHz, choosing C_{sense} = 142fF results in I_{AC} = 200pA, which is 2x more than the CI current $I_{Cinj,CH3}$ created by minimum-size chopper switches (as discussed in Section 2.4.1). Additionally, the low-frequency chopping also helps mitigate error current due to CI as discussed in Section 2.4.3. In turn, for $f_{c,\,HPF}$ = 1Hz, a value of 36 nS is calculated for gm-aux. But from Equation 2.14, the offset correction ratio (L_{DC}) will then only be 136, assuming that $A_{2,DC}$ ~70 dB, which is 2x less than the required ratio.

Another design consideration is the offset correction range, which is limited by the swing of the RRL integrator (A2) and the linear input range of gm-aux. Equation 2.17 relates the differential input voltage of gm-aux (V_O, shown in Figure 2.10) and the offset voltage (V_{OS}).

$$\frac{gm\_main}{gm\_aux} * V_{OS} \approx V_O \quad (2.17)$$

With the calculated values of gm-main =1.4mS, gm-aux =36nS, and assuming that the differential input range of gm-aux is about +/-1V, the maximum V_{OS} that can be corrected by the RRL is +/-51.4μV. This is much smaller than the expected V_{OS} ≈16mV. To correct this, gm-aux must be increased to ≈22μS.

Hence, when deciding on the value of gm-aux, a tradeoff exists between the offset correction range of the RRL and the phase error introduced by the high-pass corner $f_{c,HPF}$. This can be reduced below 1Hz by making gm-aux weaker, but this further reduces the offset correction range. One solution is to first reduce the initial offset, thus relaxing the requirement for a large offset correction range. Therefore, in this work, a hybrid RRL is proposed.

2.5.2 Hybrid RRL

The hybrid RRL operates as follows: at the start of each PD-DSM conversion, an initial offset reduction is performed by digitally trimming the offset of gm-main ① [20]. Then during the conversion, an

extremely slow RRL (for minimum phase error) is used to compensate for any residual offset or drift ②. Figure 2.12 shows the proposed architecture.

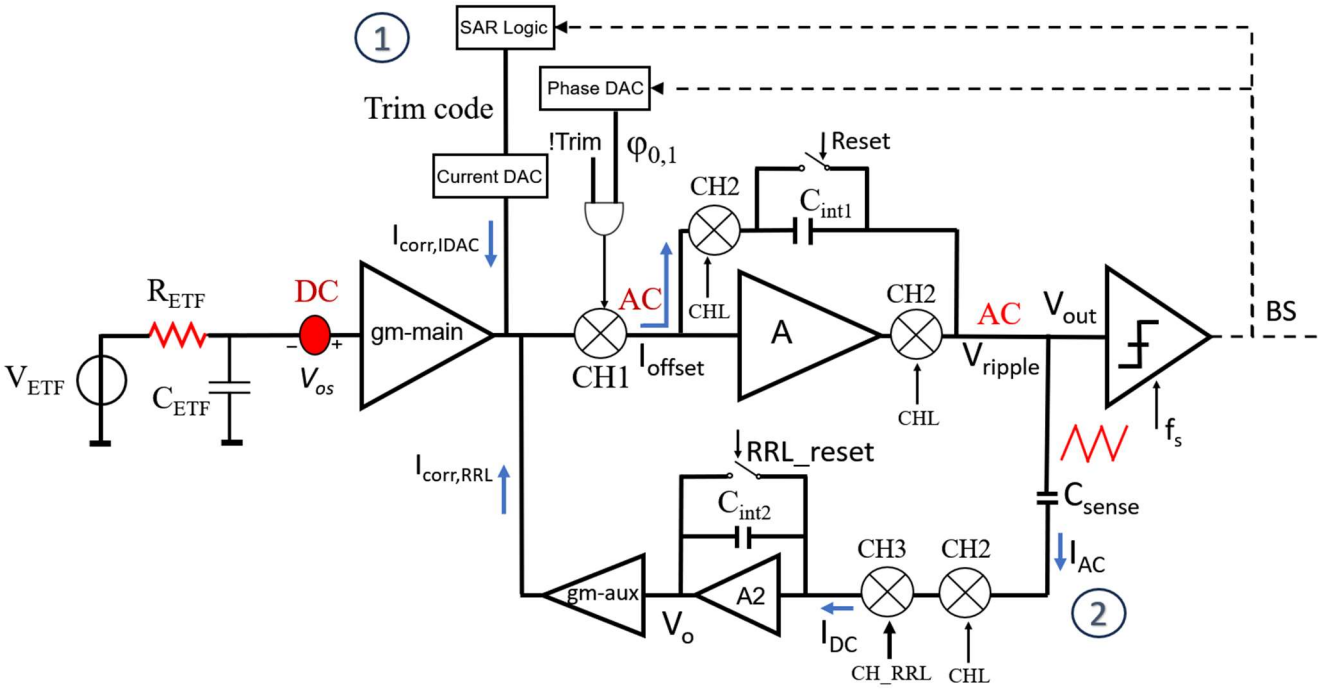


Figure 2.12: Hybrid ripple reduction loop.

In the actual design, a 6-bit SAR trim is implemented with the help of a binary-weighted current steering DAC (IDAC), which injects a correction current into the auxiliary input of gm-main. This reduces the initial offset by 64 times and proportionally relaxes the requirement for a large value of gm-aux.

2.6 Error budgeting

For the lithography error to be the main source of temperature error, the error of the PD-DSM must contribute less than 0.04°C. The following table summarizes the contribution of the various error sources and the consequences for the circuit implementation.

Table 2.1: Error budgeting.

Error Source	Design consideration	Error (3σ, °C)
Phase error due to timing delay	Timing delay < 185ps	± 0.01
Phase error due to finite BW of gm-stage	BW > 800 MHz	<0.01
Phase error in V_{ETF} (RC phase shift)	φ_{err} spread < 2m°ϕ (C_{gg} < 1pF)	<0.01
Phase error due to CI current	Low-frequency chopping	<0.01
Self-heating	Minimum spread in P_{heater}	∝ P_{heater}

3. Circuit Implementation

This Chapter describes the circuit-level implementation of the various sub-blocks of the readout architecture discussed in Chapter 2, as shown in Figure 2.12. The readout is designed in TSMC CMOS 180nm technology, with a power supply (V_{DD}) of 1.8V.

3.1 Trans-conductor (gm-stage)

The output voltage of the ETF (V_{ETF}) is converted to current by a transconductance stage (gm-stage). As discussed before, the thermal noise contribution of the gm-stage should be less than that of the ETF's resistance R_{ETF} (R_{TP} = 4kΩ and R_{Ring} = 950Ω). Assuming the input differential pair of the gm-stage is the main contributor, this requires:

$$v_{n,\,gm}^2 = \frac{8kT\gamma}{g_m} < 4kTR_{ETF} \tag{3.1}$$

Where γ is the excess noise factor and is equal to 2/3 for long-channel transistors, and k is Boltzmann constant = $1.38*10^{-23}$ J/K. With R_{ETF} = 950 Ω, the minimum gm is then 1.4 mS, which makes the noise of the gm-stage equal to that of R_{ETF}.

In the chosen 180nm process, the PMOS transistors have less $1/f$ noise than the NMOS transistors for the same *gm*. Hence a PMOS input differential pair is chosen for the gm-stage. Its $1/f$ noise density is then given by:

$$V_{n,1/f}^2 = \frac{2K}{C_{ox}\,WL} \cdot \frac{1}{f} \tag{3.2}$$

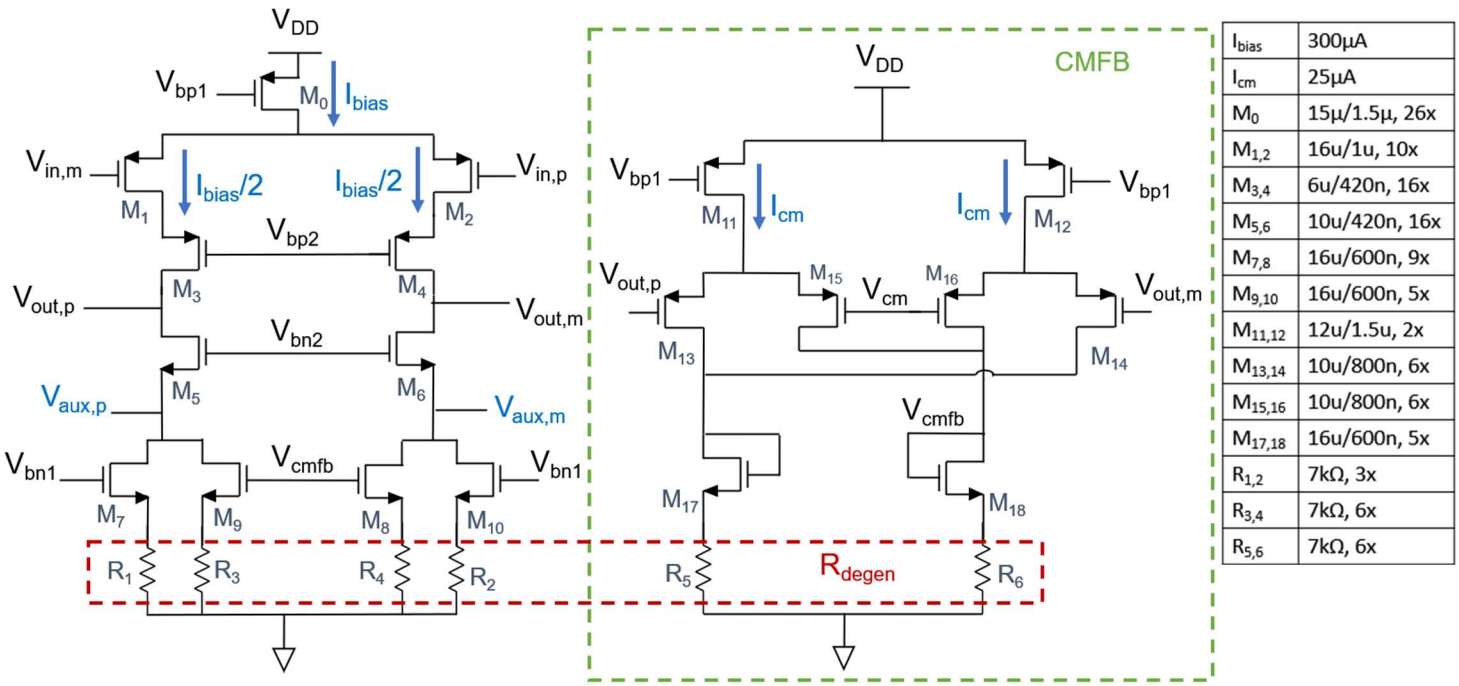
Where K is in the order of $5*10^{-25}$ V^2F and is a process-dependent constant [26].

$$\text{At } f_{drive},\ \overline{V_{n,\frac{1}{f}}^2} < V_{n,R_{ETF}}^2 \tag{3.3}$$

The corner frequency (f_c) must be less than f_{drive} for the thermal noise to dominate. Using Equation 3.2, with C_{ox} = 15 fF/μm^2 and f_c = 28kHz, the minimum required area of each input device is around 160 μm^2. This results in a gate capacitance (C_{gg}) of 1pF, which is small enough (see section 2.3.3).

As discussed in Section 2.3.3, along with the high *gm*, the BW of the gm-stage must be ≈800 MHz, thus the input pair should operate near moderate inversion (gm/I_D=9.5). With *gm*= 1.4mS, this results in a minimum bias current per device of 150 μA.

Since the gm-stage drives the virtual ground of the integrator, a high output swing is not necessary. Thus, as in [15], a telescopic amplifier is preferred because of its low power consumption. A dual differential-pair common-mode feedback (CMFB) is implemented to set the output common-mode voltage close to $V_{DD}/2$. The designed gm-stage and CMFB are shown in Figure 3.1.



I_{bias}	300µA
I_{cm}	25µA
M_0	15µ/1.5µ, 26x
$M_{1,2}$	16u/1u, 10x
$M_{3,4}$	6u/420n, 16x
$M_{5,6}$	10u/420n, 16x
$M_{7,8}$	16u/600n, 9x
$M_{9,10}$	16u/600n, 5x
$M_{11,12}$	12u/1.5u, 2x
$M_{13,14}$	10u/800n, 6x
$M_{15,16}$	10u/800n, 6x
$M_{17,18}$	16u/600n, 5x
$R_{1,2}$	7kΩ, 3x
$R_{3,4}$	7kΩ, 6x
$R_{5,6}$	7kΩ, 6x

Figure 3.1: Telescopic gm-stage with CMFB.

The gm-stage also has auxiliary inputs ($V_{aux,p}$ and $V_{aux,m}$) at the drains of the NMOS current sources to provide the offset correction current from the hybrid RRL. To reduce their noise contribution, degenerated NMOS current sources are used.

The simulated thermal noise density of the gm-stage at room temperature (RT-27°C) is 6.13nV/√Hz, which is 2.2nV/√Hz higher than that of the S24 ring ETFs. This is mainly due to the contribution of the NMOS current sources, which was not taken into account in Equation 3.1. The total input-referred noise of the gm-stage and the S24 ring and TP ETFs is then 7.2nV/√Hz and 10nV/√Hz, respectively. The front end thus increases the noise floors of the ring and TP ETFs by 1.8x and 1.2x, respectively. In [15], a TD sensor with a total input-referred noise of less than 8.1nV/√Hz achieved 10mK in 1s conversion time with an S24 TP-ETF (P_{heater}=4.2mW). Since the target resolution is 15mK, the noise increase by the front end was considered acceptable.

Figure 3.2 shows the noise performance of the gm-stage at room temperature, where the horizontal markers indicate the noise level of ring ETF and TP ETF.

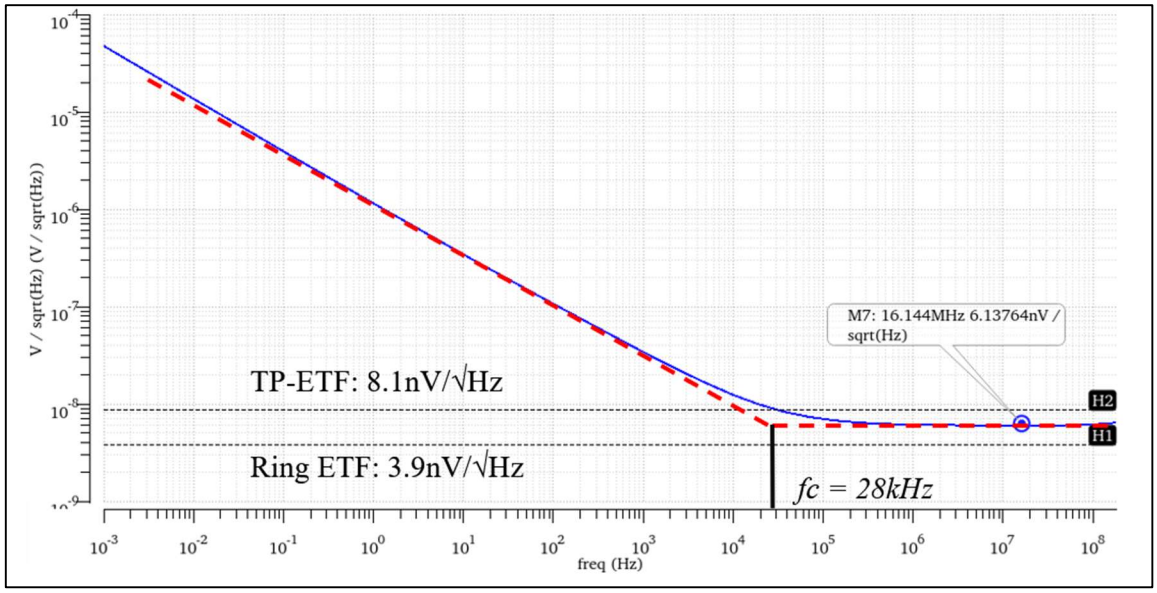


Figure 3.2: gm-main 1/f noise.

To simulate its AC transconductance, the gm-stage was driven by an ideal voltage source with input common-mode voltage of $V_{DD}/2$, while its output was short-circuited to emulate the input of an ideal integrator. Figure 3.3 shows the magnitude and phase response of the output current for a 1V AC input voltage. The achieved gm is more than 1.3 mS across PVT with a BW ≈ 800 MHz. At f_{drive} = 30kHz the absolute phase error is around 3m°ϕ, and the spread is about 0.7m°ϕ, which is very small compared to the targeted phase error (2m°ϕ).

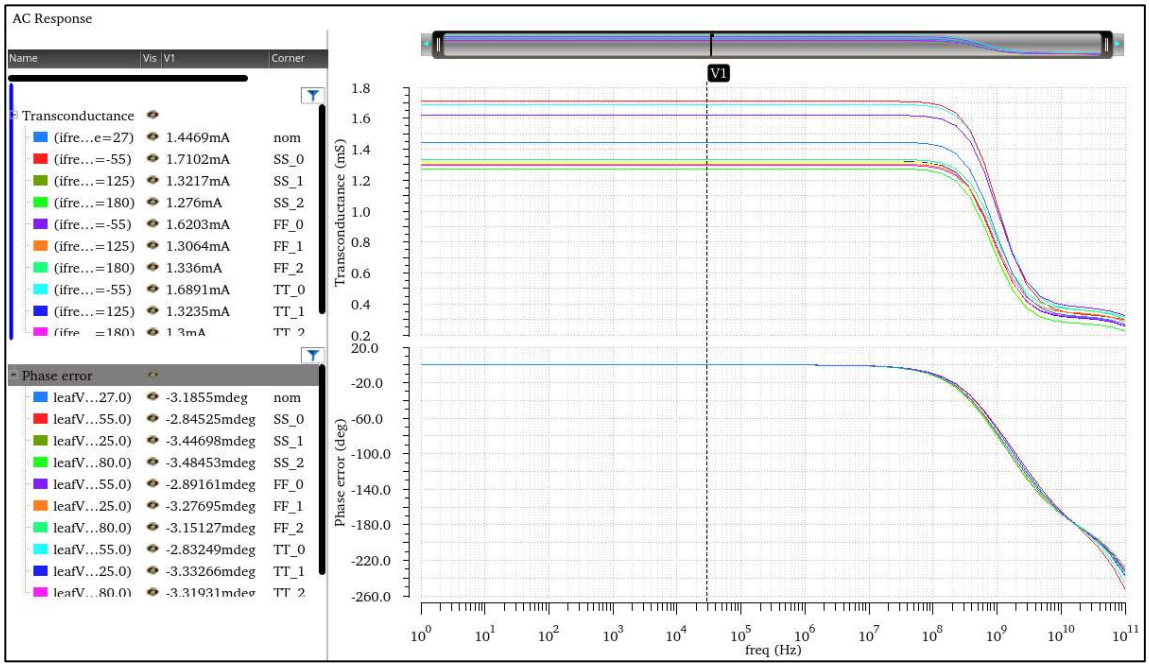


Figure 3.3: V-to-I magnitude and phase response of gm-stage.

As discussed in Section 2.3.3, the BW at the output of the gm-stage is also limited by the RC filter formed by the ETF resistance (R_{ETF}=4kΩ) and the input capacitance (C_{gg}=1pF) of the gm-stage. Figure 3.4 shows the V-to-I transfer function of the gm-stage and the S24 TP-ETF when they are driven by an ideal AC voltage source with a common mode voltage of $V_{DD}/2$.

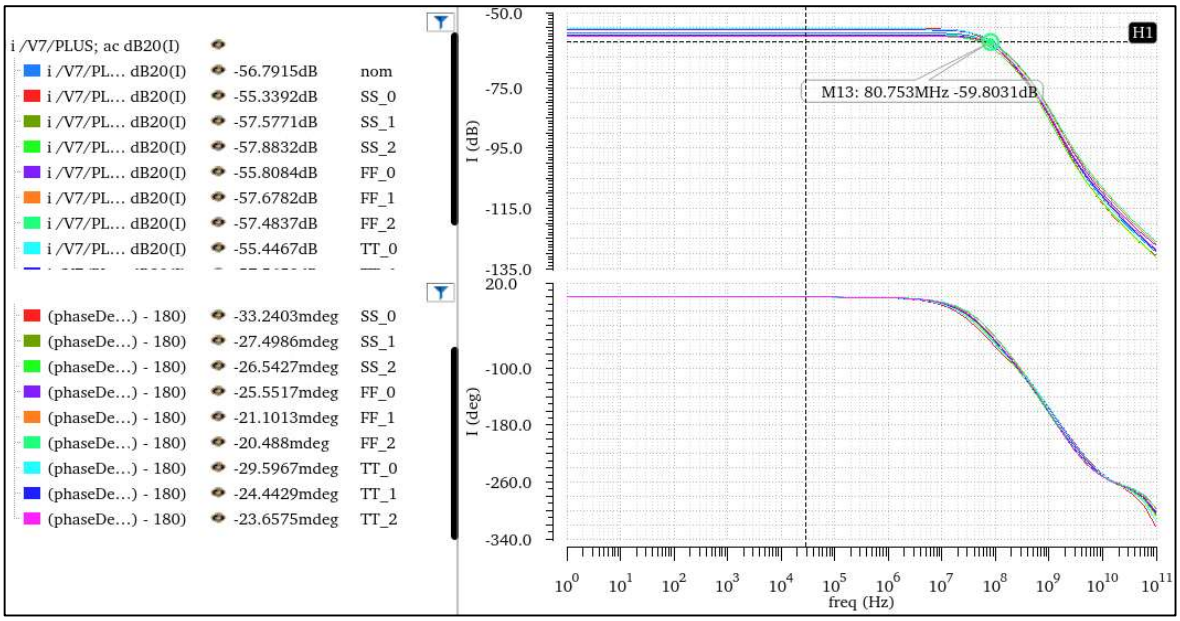


Figure 3.4: V-to-I magnitude and phase response of gm-stage with S24 TP-ETF.

The BW is reduced to 80MHz. The phase error at f_{drive}=30kHz is around 26m°ϕ and spreads by 12m°ϕ over PVT, resulting in a temperature error of 0.06°C. Note that this spread is mostly a function of the spread of the TP resistors, as the simulated spread is less than 1m°ϕ with fixed resistors.

The input-referred offset $V_{os,gm}$ of the gm-stage is calculated by running Monte Carlo mismatch simulations over the temperature range. These give $V_{os,gm}$ = 3mV (3σ).

3.2 Demodulator Chopper

The demodulator chopper is designed using NMOS switches. As discussed in Section 2.4, minimum-size transistors (W/L = 220/180nm) are used to minimize the charge injection current and parasitic capacitance.

The phase references of the phase DAC (φ_0, φ_1) should be chosen to cover the expected range of φ_{ETF}. Taking into account the wide temperature range and the need to readout both S24 and S12 ETFs, four different phase ranges were implemented: 0°- 45°, 22.5°- 67.5°, 45°- 90°, and 67.5° - 112.5°. These were generated on-chip from a master clock running at 16f_s.

3.3 Integrator design

The differential output of the gm-stage is connected to the virtual ground of an active integrator, which consists of a differential OTA and two integration capacitors (C_{int}). The OTA is designed to have high gain and a large output voltage headroom. As discussed in Section 2.2, the designed C_{int} is chosen to be 28pF,

which results in an estimated output swing of 470 mV_{pp}. Furthermore, to reset the PD-DSM at the start of every conversion, an NMOS reset switch is added in parallel to the C_{int} as shown in Figure 3.5.

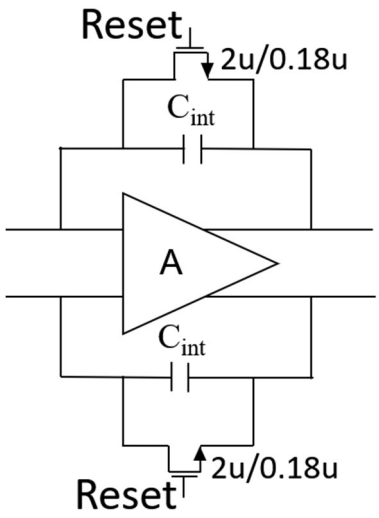
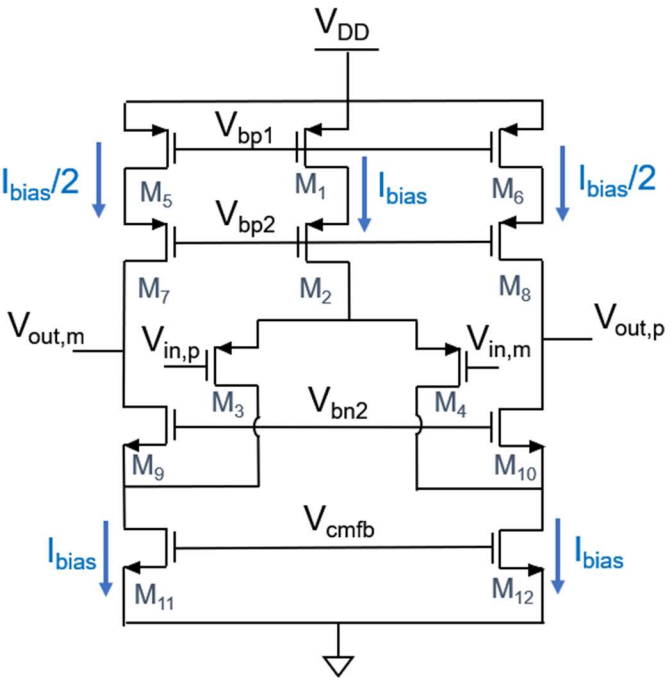


Figure 3.5: OTA with C_{int} and Reset switch.

Given the output swing requirement, the chosen topology for the active integrator is a fully differential folded cascode amplifier. To maximize the DC gain, the input pair was sized to operate in weak inversion ($gm/I_D \approx 19$). The output swing of the OTA was maximized by placing the cascodes in weak inversion and the current sources in moderate to weak inversion, achieving a peak-to-peak voltage swing of 1.4V_{pp}. The small amount of bias current (I_{bias}=10µA) has been chosen such that the OTA's power consumption is negligible when compared to the gm-stage. The designed OTA is shown in Figure 3.6.



I_{bias}	10µA
$M_{1,2}$	5u/2u, 10x
$M_{3,4}$	5u/800n, 5x
$M_{5,6}$	5u/2u, 5x
$M_{7,8}$	5u/420n, 8x
$M_{9,10}$	5u/420n, 2x
$M_{11,12}$	5u/2u, 10x

Figure 3.6: Fully differential folded cascode OTA.

The simulated gain of the OTA is around 80 dB across PVT, which ensures that the total DS loop-filter gain, including the gain from the gm-stage, is more than 120dB. The phase and magnitude response of the OTA are shown in Figure 3.7. The maximum gain-bandwidth (*GBW*) product of the OTA, when loaded by the comparator and the bottom-plate parasitic capacitance of C_{int1},($=C_{load}$) is 109MHz, corresponding to the FF corner at -55°C.

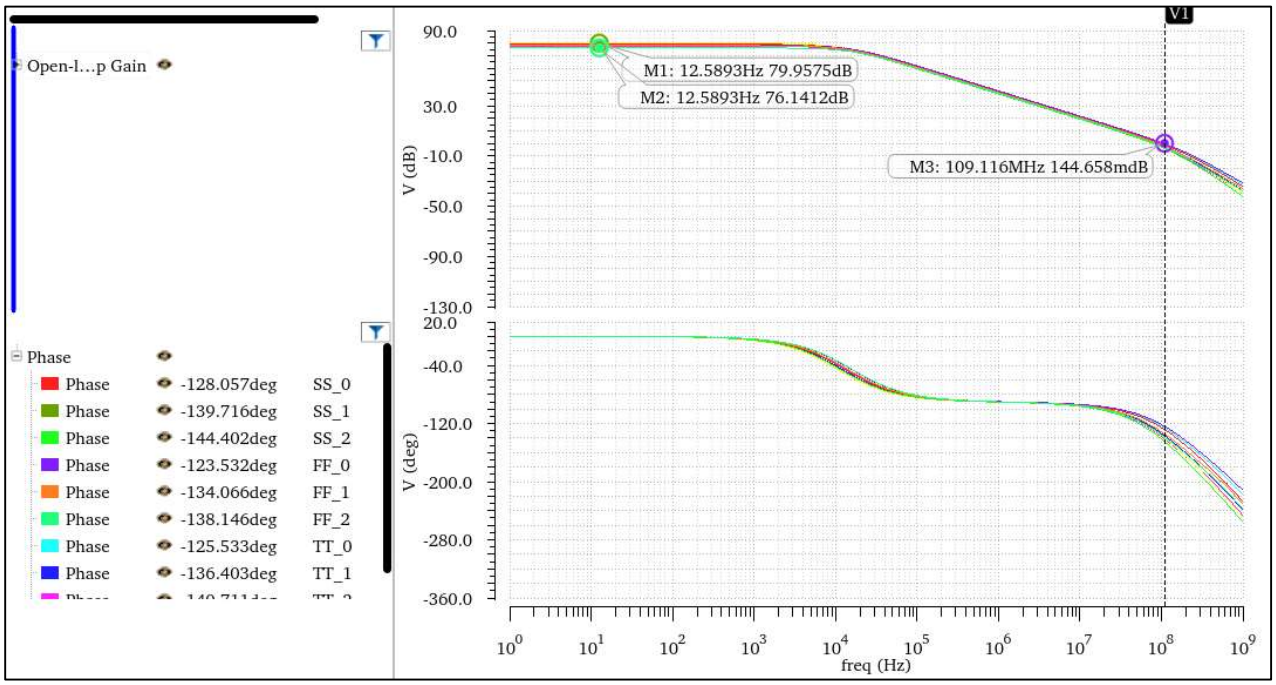


Figure 3.7: Magnitude and phase response of FC-OTA.

To avoid limiting the system's bandwidth, the PD-DSM's integrator must have a low input impedance (Z_{in}) (discussed in Section 2.3.3). The input impedance of a single-stage OTA with a feedback integration capacitor is given by Equation 3.4. The small-signal model used to derive this is shown in Figure 3.8.

$$Z_{in}(s) = \frac{V_{in}}{I_{in}} = \frac{1 + s(C_{int1} + C_{load})r_o}{s^2(C_{int1} + C_{in})(C_{int1} + C_{load})r_o + s[C_{int1}r_o(g_m - sC_{int1}) + C_{in} + C_{int1}]} \quad (3.4)$$

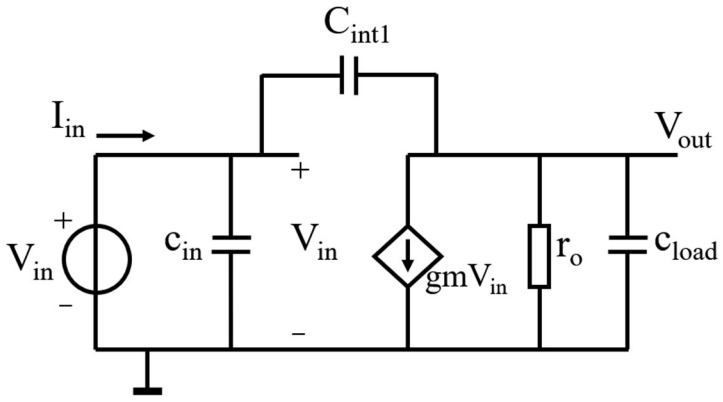


Figure 3.8:Small-signal model of a single-stage integrator to calculate Z_{on}

The input impedance behavior over frequency is illustrated in Figure 3.9. The integrator's input impedance is infinite at DC and is approximately equal to $\frac{1}{gm}$ from low frequencies up until the high-frequency pole approximated by $-\frac{gm}{C_{in}}$.

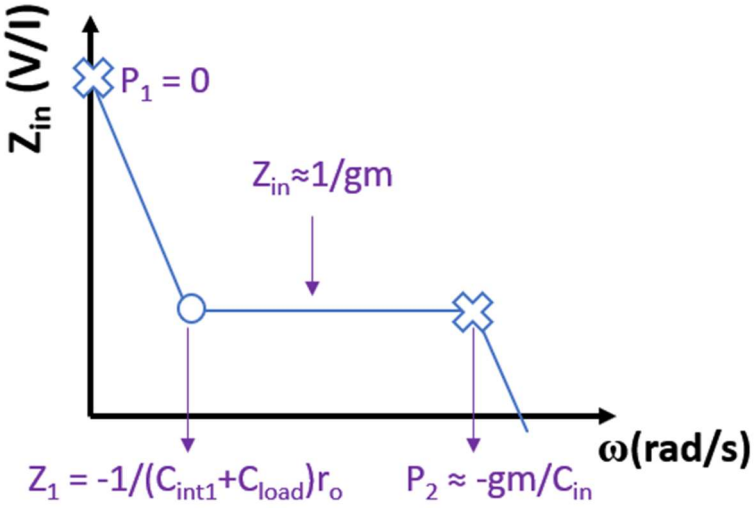


Figure 3.9: Location of poles and zeros for Zin for one-stage integrator.

The gm of the designed OTA is equal to 90 µS, while its output impedance is 110MΩ. Together with the large integration capacitance C_{int1}=28pF this results in Z_{in} ≈ 11KΩ at f_{drive} = 30kHz and a zero at (≈55 Hz). In a PD-DSM, however, the signal current (I_{signal}) is demodulated by the chopper to very low frequencies (≈1 Hz), so it is desirable to push the zero well below these frequencies. Unfortunately, this effect was not considered during the design phase, but should be addressed in an improved design. The detailed implications of this effect are further explained in Section 4.4.

3.4 Ripple Reduction Methods

As discussed in Section 2.5, this work employs a hybrid offset reduction technique, where a SAR trim performs a coarse offset reduction before each DS conversion, followed by a continuous-time ripple reduction loop, which cancels the residual offset voltage during the DS conversion. The single-ended block diagram of the readout (without low-frequency choppers) is shown in Figure 3.10. This section discusses the circuit-level implementation of both techniques.

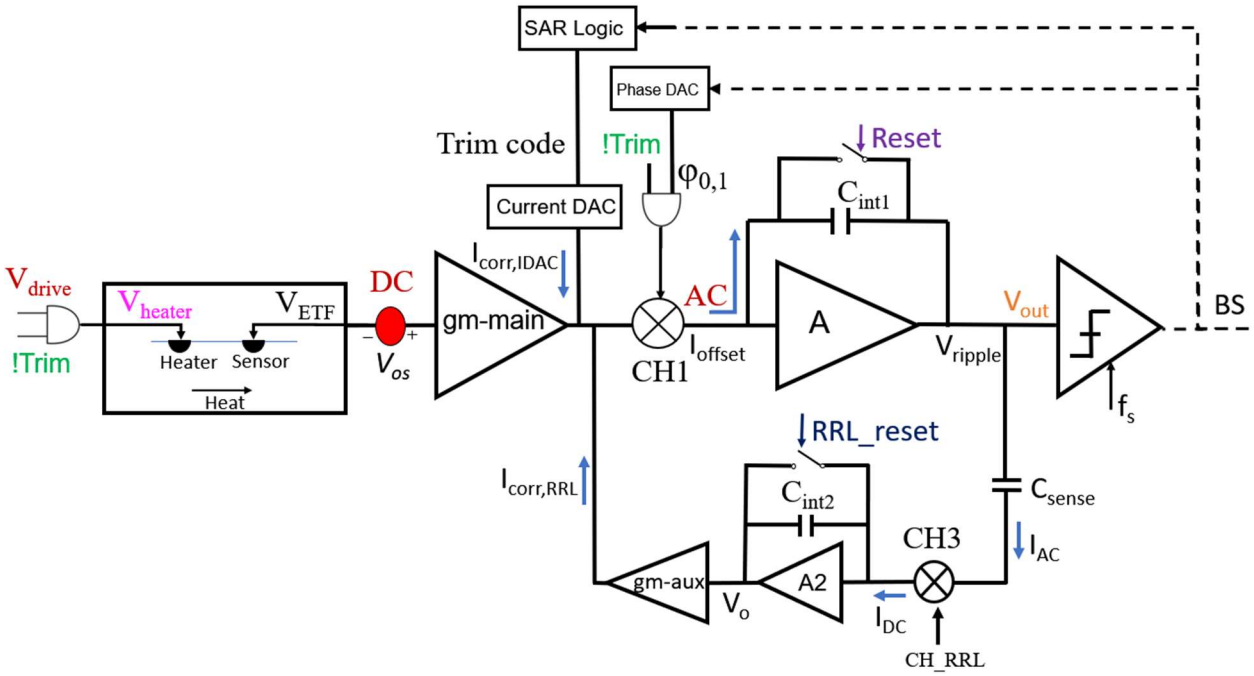


Figure 3.10: Hybrid Ripple reduction loop.

3.4.1 Digitally Assisted SAR Trimming

As shown in Figure 3.10, the digital SAR trim loop, which is the same as that in [20], consists of a comparator, SAR Logic, and a current DAC (IDAC) [20]. Its timing diagram is shown in Figure 3.11.

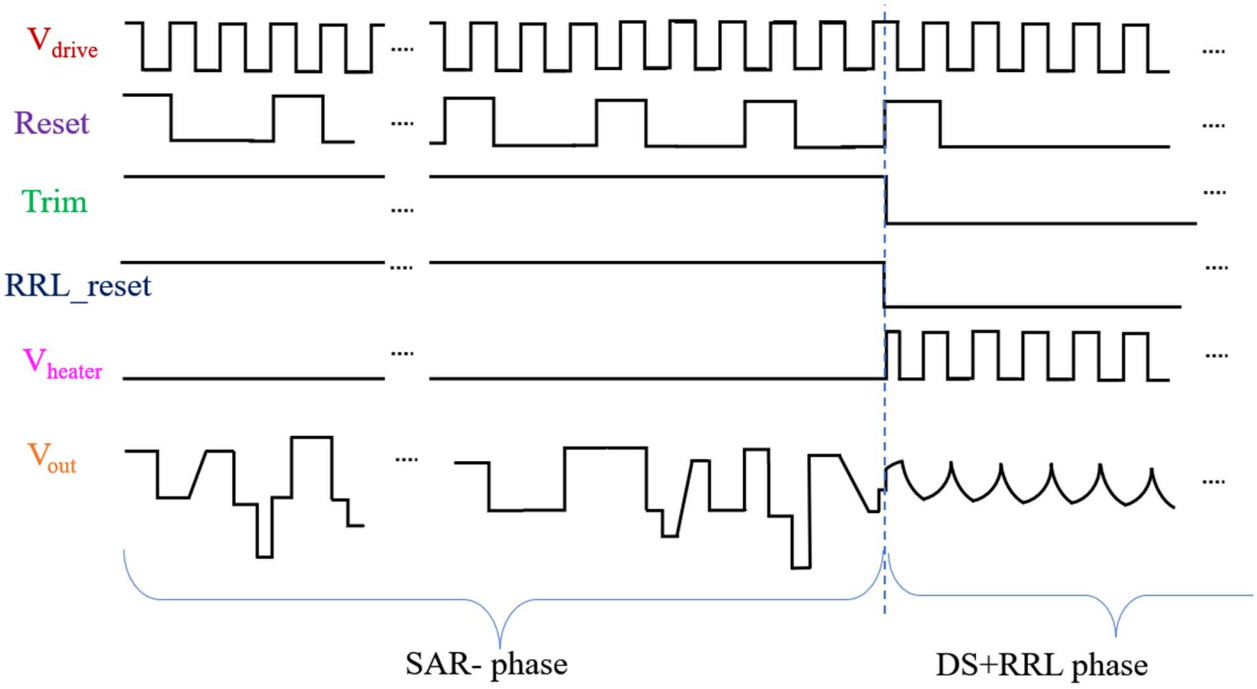
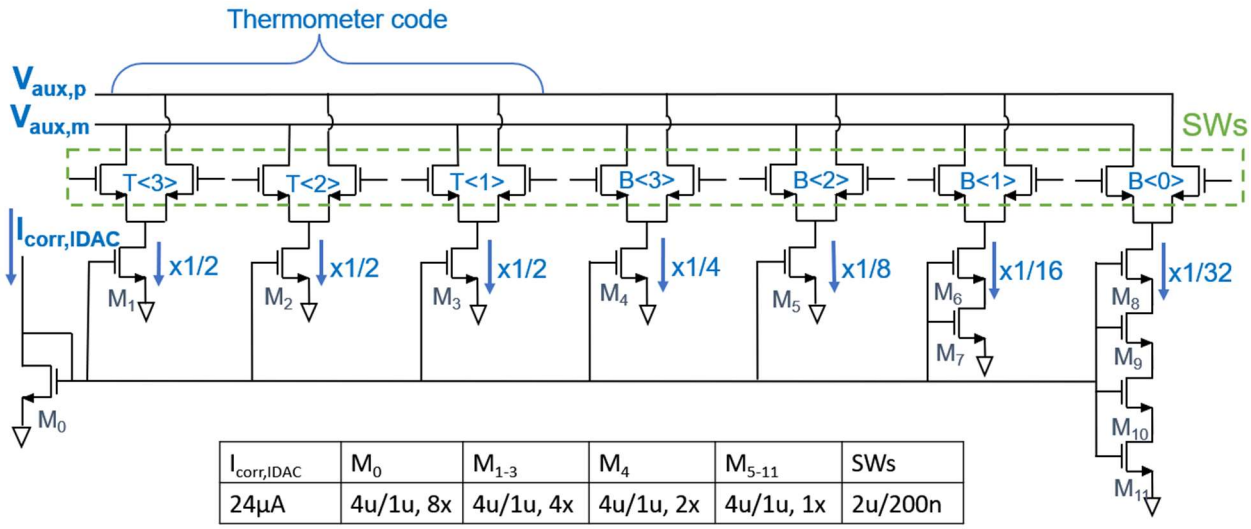


Figure 3.11: Timing Diagram of the proposed offset reduction technique.

At the start of each SAR conversion, the heater of the ETF is turned off (V_{heater}), the DSM is reset (*Reset*), and the demodulating chopper is disabled (*Trim*), the RRL is also turned off by resetting the integrator in the RRL (*RRL_reset*). As in [20], one SAR trim bit is coded in three clock cycles (two clock cycles for SAR conversion and one for Reset, as shown in Figure 3.10). During the conversion, the output current of the gm-main is amplified by the loop filter, which is then fed to the comparator. Based on the comparator output, the polarity of the correction current ($I_{corr,IDAC}$ in Figure 3.10) is decided. After the 6 SAR trim bits are set, the RRL loop is switched ON and the DS conversion is started.

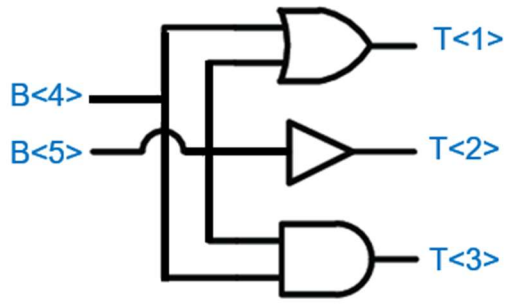
In this work, a 6-bit NMOS current DAC with the polarity switches is designed to compensate for an offset of ±16.5mV, with a maximum correction current ($I_{corr,IDAC}$) of 24 µA. The LSB of the IDAC corresponds to a correction current of ±0.8µA, which corresponds to $V_{OS,LSB}$ of 0.5mV. The implementation of the current DAC is shown in Figure 3.12.



$I_{corr,IDAC}$	M_0	M_{1-3}	M_4	M_{5-11}	SWs
24µA	4u/1u, 8x	4u/1u, 4x	4u/1u, 2x	4u/1u, 1x	2u/200n

Figure 3.12: NMOS current-steering IDAC.

To reduce the total area of the current DAC, the 2 LSBs are implemented using stacked devices. The 2 MSBs (B<4> and B<5>) are implemented using unary devices, which are driven by the binary to thermometer decoder shown in Figure 3.13.



Binary Code		Thermometer Code		
B<5>	B<4>	T<3>	T<2>	T<1>
0	0	0	0	0
0	1	0	0	1
1	0	0	1	1
1	1	1	1	1

Figure 3.13: Binary to thermometer decoder for B<4< and B<5>.

The DAC's differential current is injected into the auxiliary inputs of the gm-stage ($V_{aux,p}$ and $V_{aux,m}$), which are highlighted in Figure 3.1. The SAR-Logic and the control signals were re-used from the work done in [20], and hence are not presented in this document.

Figure 3.14 shows the simulated timing diagram of SAR Logic and the residual ripple after one SAR conversion.

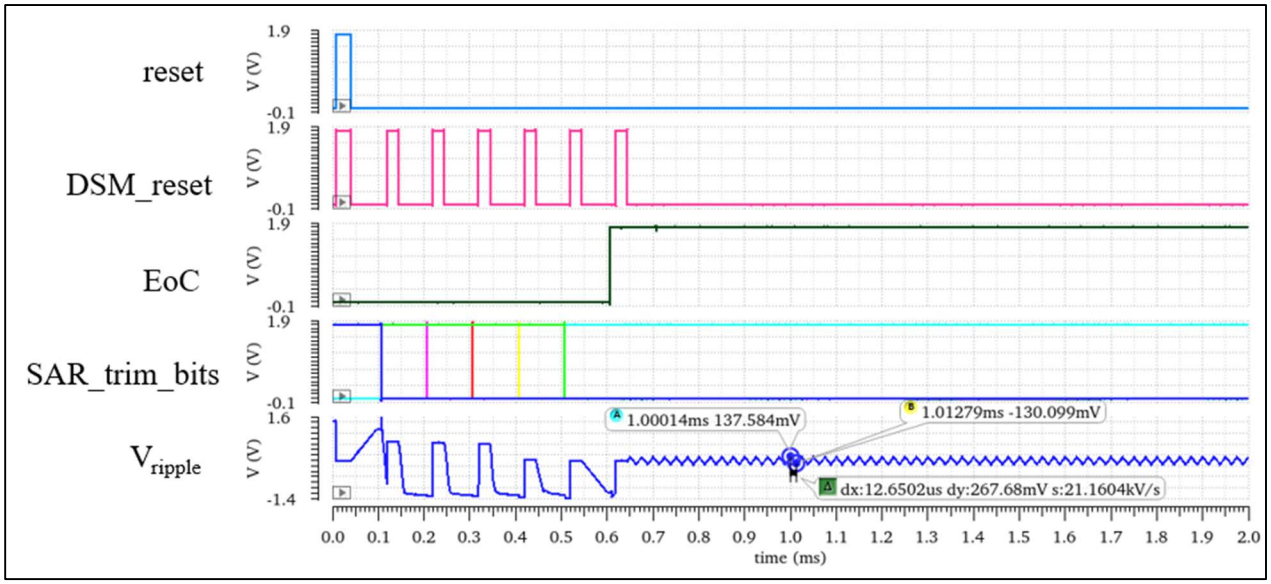
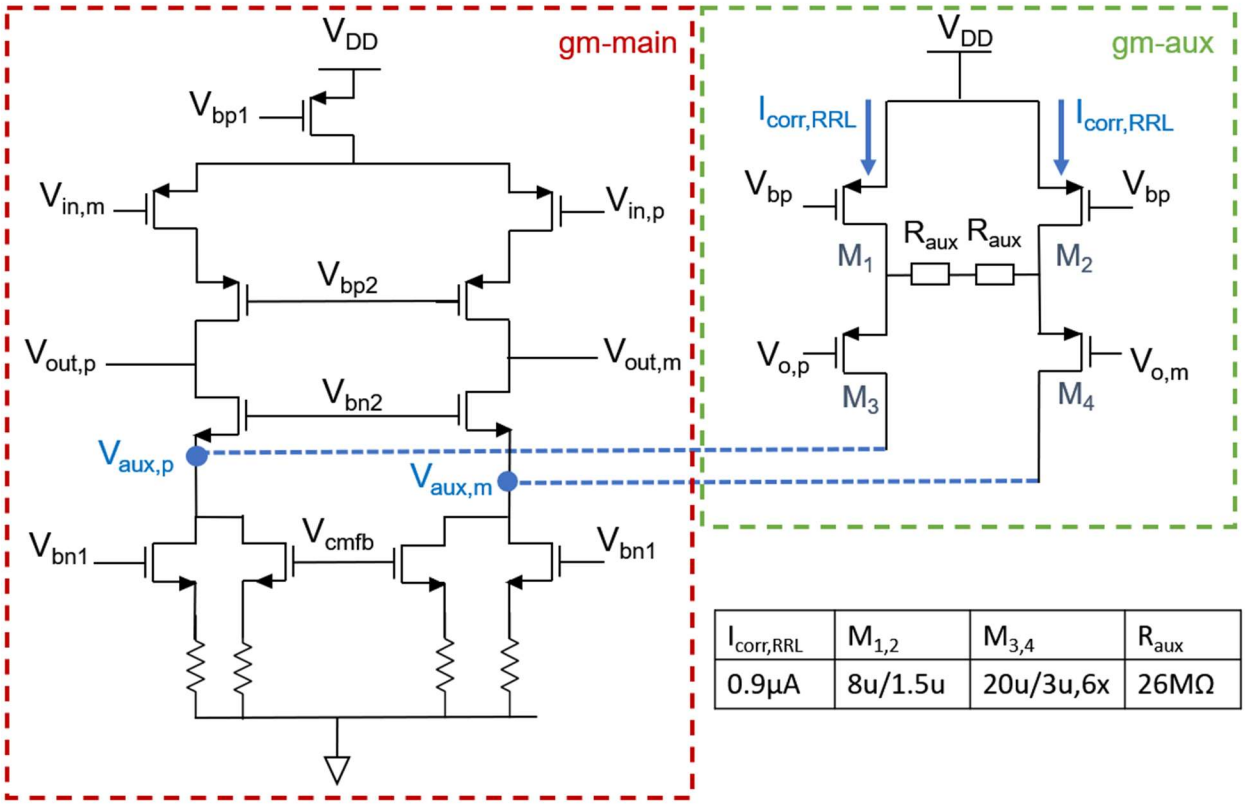


Figure 3.14: Residual offset after SAR trim.

During the SAR conversion, the demodulator is disabled. The end of conversion (*EoC*) signal triggers the RRL ON and starts the DS conversion. Figure 3.14 shows the residual ripple with a peak-to-peak amplitude of 267 mV_{pp}, which corresponds to a residual offset of 0.3 mV (≈ 1/2 LSB). The simulation is done with no input signal and the input V_{OS} was set to zero, which is in the middle of an LSB.

3.4.2 Ripple Reduction Loop

The correction range of the RRL is designed with some margin to compensate for a maximum residual offset of 0.625mV (≈ 2 times 1/2 LSB). Gm-aux is designed such that it can provide a correction current ($I_{corr,RRL}$) of 0.9µA. To make *gm-aux* very small, as discussed in Section 2.5.1, its PMOS input pair is placed in weak inversion and heavily degenerated. Theoretically, the effective gm of the designed structure is $1/R_{aux}$ i.e., 1/26MΩ = 40nS. The implementation of gm-aux is shown in Figure 3.15.



$I_{corr,RRL}$	$M_{1,2}$	$M_{3,4}$	R_{aux}
0.9µA	8u/1.5u	20u/3u,6x	26MΩ

Figure 3.15: Auxiliary transconductance (gm-aux).

The R_{aux} is implemented using p-poly resistors and has the same area as the integration capacitors, which means that they can be stacked in the layout, making the RRL very compact. The integrator (A2) is based on a folded-cascode OTA. To realize a low $f_{c,HPF}$ the value of C_{int2}, as shown in Figure 3.7, was chosen to be equal to C_{int1}, that is, 28pF.

The voltage-to-current (*V-to-I*) transfer function of the system with the RRL was simulated with the testbench shown in Figure 3.16. An ideal differential AC voltage source, with the common-mode voltage of $V_{DD}/2$ is used to drive the gm-stage and the result is obtained by plotting the differential current in the integration capacitors, C_{int1}. The resulting HP corner of the designed RRL is 1.85 Hz, amounting to an RRL time constant of 80ms, as shown in Figure 3.17.

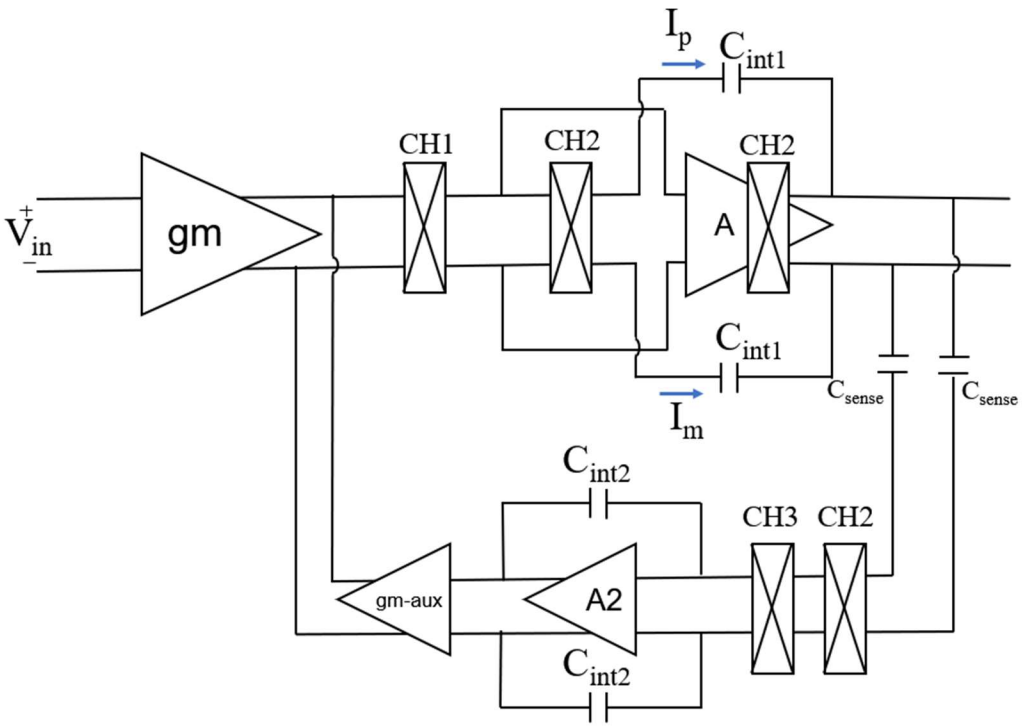


Figure 3.16: Testbench to simulate the V-to-I transfer function.

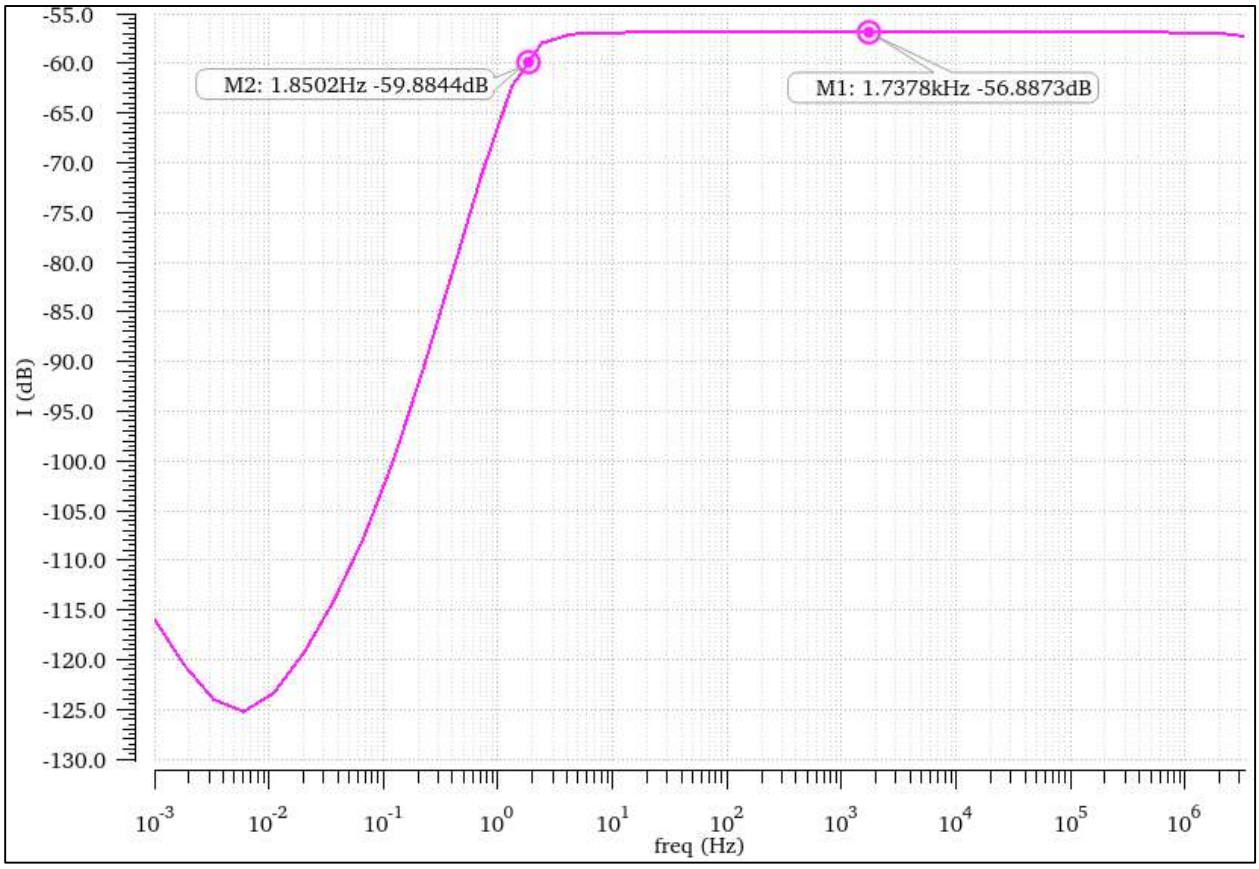


Figure 3.17: High-pass corner with RRL.

For a conversion time of 1s, the settling time of RRL is quite significant (≈12.5% of the conversion time). To reduce this, the sensing capacitance is temporarily increased by adding a 3.5pF capacitor (C_{fast}) in parallel with C_{sense}, as shown in Figure 3.18 (single-ended implementation). This increases the speed of the RRL loop by 26 times and the loop settles in less than 3ms.

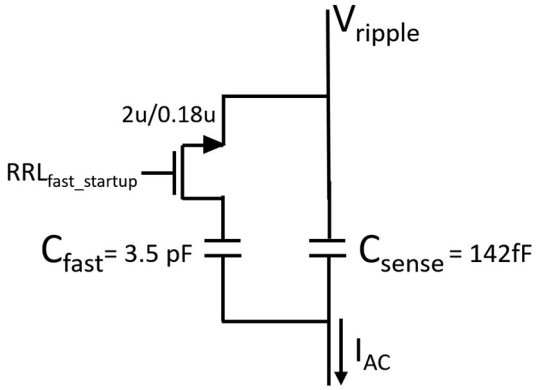


Figure 3.18: RRL fast startup scheme.

Figure 3.19 shows a transient simulation with both the SAR and the fast mode of RRL activated. When the signal *RRL_reset* is high, SAR operation takes place, and with *RRL_reset* low the RRL switches ON. Signal $V_{o,RRL}$ i.e., differential output of the integrator A2, settles after 1 ms, and the ripple is reduced to 0.75mV$_{pp}$, corresponding to a residual offset of 0.8µV when the voltage offset after SAR trim was 0.3mV.

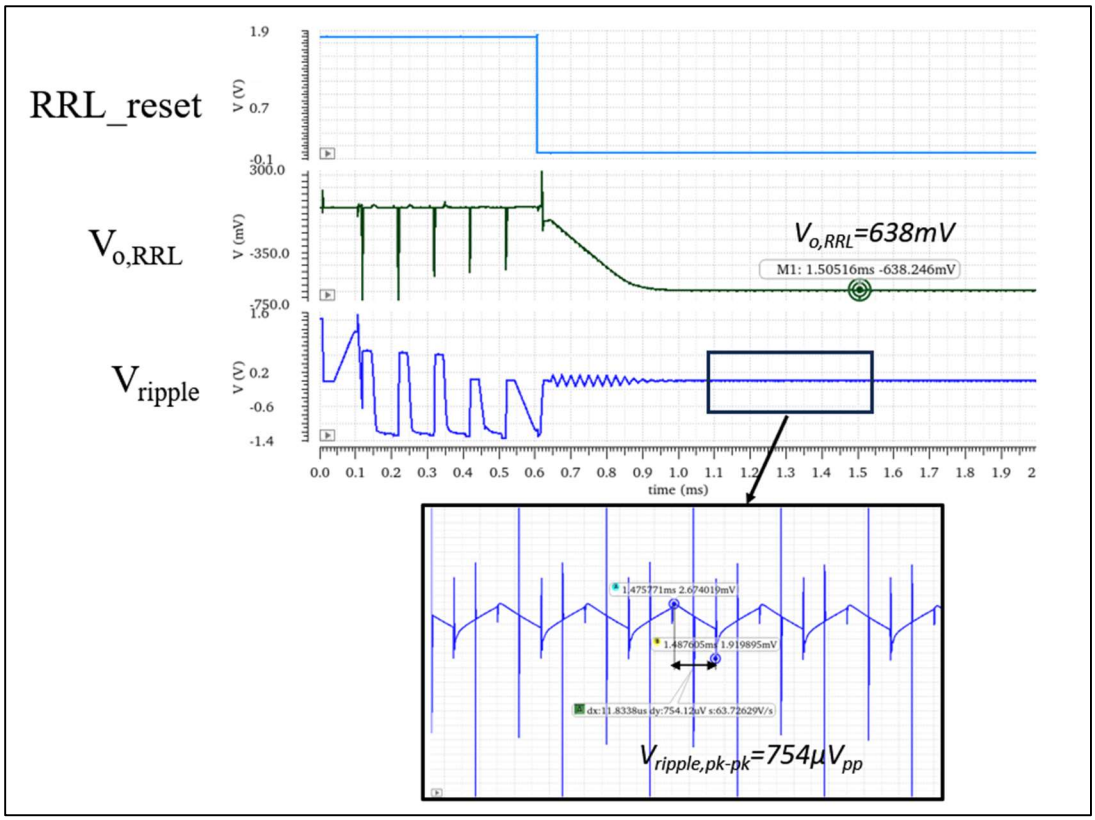


Figure 3.19: Residual offset after SAR trim and RRL compensation.

3.5 PD-DSM scalability

So far the circuit specifications have been derived by considering the requirements of the s=24µm TP and ring ETF. As discussed in Section 2.1, scaled-down versions of the TP and ring ETF with s= 12µm are also implemented. As discussed in Section 1.5.2, if s is reduced while φ_{ETF} is kept constant by scaling f_{drive} by a factor $\left(\frac{1}{s^2}\right)$, then V_{ETF} will scale by a factor $\frac{1}{s}$.

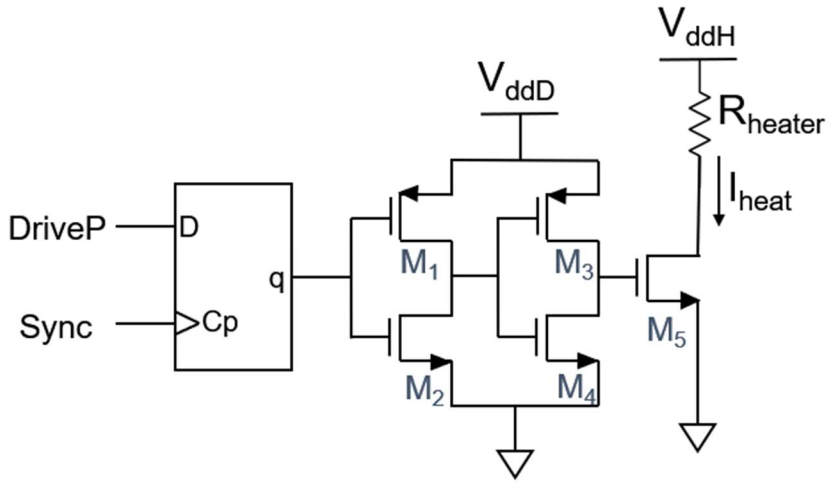
Also, Equation 2.2 shows that $V_{swing,pk\text{-}pk}$ is proportional to V_{ETF} and inversely proportional to f_s. Therefore, for a scaled-down ETF, the voltage swing at the output of the PD-DSM integrator will decrease by $\frac{1}{s}$. To maintain the same integrator output swing, either gm or C_{int1} must be scaled. To avoid modifying the OTA too much, it was chosen to reduce the value of C_{int1} to 14pF.

Furthermore, since scaling down an ETF will reduce its area proportionally, its total parasitic capacitance (C_{ETF}) will scale by $\frac{1}{s^2}$. Therefore, for a similar phase error in V_{ETF} the input capacitance of the gm-stage should be scaled down proportionally. Thus, for the S12 ETFs, the width and length of the differential pair of the gm-stage are halved, which reduces C_{gg} by 4x while keeping gm constant.

3.6 Miscellaneous Circuits

3.6.1 Heater Driver

In this work, an on-chip heater driver is realized by an NMOS switch connected in series with the heater resistor (R_{heater} ≈ 385Ω, discussed in Section 1.5.2). The gate of the NMOS switch is driven by an edge-triggered D-Flip Flop (DFF) and a cascade of two inverters as depicted in Figure 3.20.



V_{ddH}	1.8V
R_{heater}	385Ω
I_{heat}	2.3mA
M_1	5.6u/180n
M_2	2.5u/180n
M_3	5.6u/180n, 2x
M_4	2.5u/180n, 2x
M_5	10u/180n, 5x

Figure 3.20: Heater Driver.

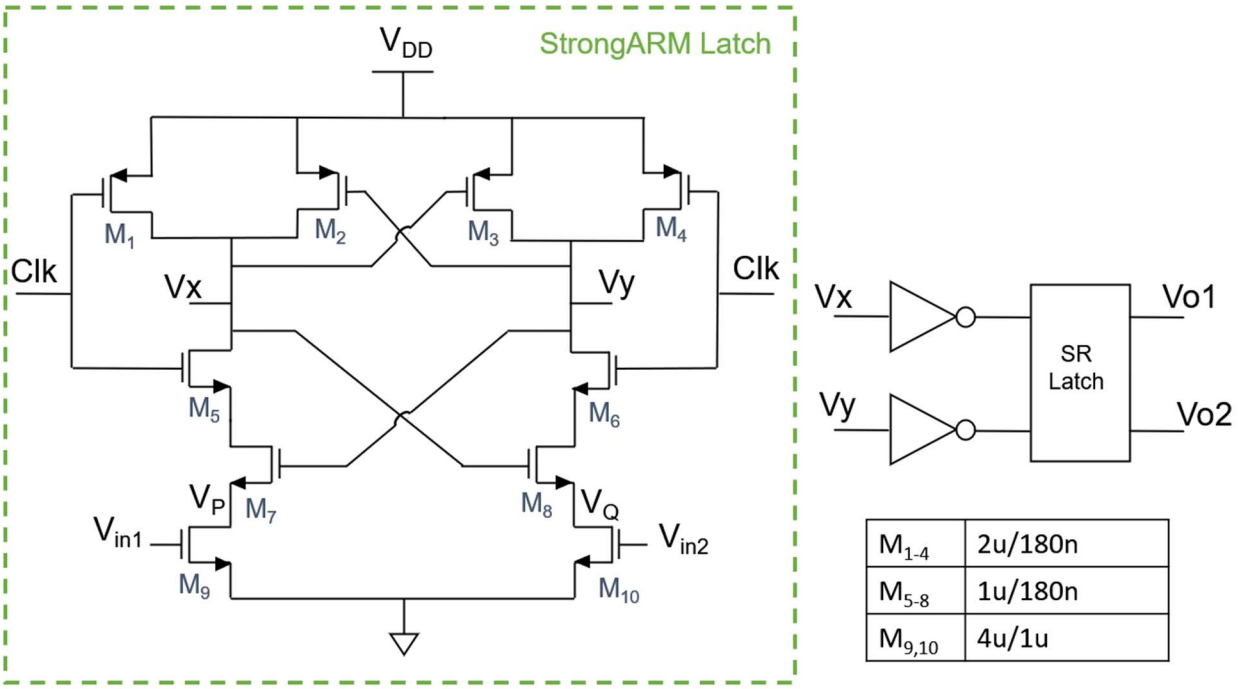
The edge-triggered DFF synchronizes V_{drive} with the reference clock signal. An identical DFF is used to synchronize the output of the phase-DAC. The inverter chain is added to drive the gate of the large NMOS switch more efficiently. The resulting heater driver has a delay of around 260ps from the

synchronization signal, which is mainly due to the DFF. The associated temperature spread is about 1.3m°C error, assuming a 10% spread in this delay.

An additional aspect in the context of the heater driver pertains to the self-heating of the NMOS switch. The designed NMOS switch has an R_{ON} (ON-resistance) of 11 Ω – a value significantly smaller than R_{heater}. To further mitigate the influence of its self-heating, the switch is positioned along one of the symmetry axes within the ETF arrangement for a uniform distribution of the undesired heat generated.

3.6.2 Comparator Design

In the designed PD-DSM architecture, the 1-bit quantizer is implemented with a clocked comparator. The chosen topology for the comparator is the StrongARM Latch shown in Figure 3.21.



M_{1-4}	2u/180n
M_{5-8}	1u/180n
$M_{9,10}$	4u/1u

Figure 3.21: Comparator Design.

The comparator design consists of an input differential pair, two cross-coupled pairs, and two pairs of switches controlled by the *Clk* [21]. Depending on the polarity of *Vin1-Vin2*, a rail-to-rail output is provided at the nodes *Vx* and *Vy*.

When *Clk* is low, the input pair is turned off, the PMOS switches are turned ON and the output nodes *X* and *Y* are pre-charged to V_{DD}. In the next phase, when the *Clk* goes high, the input pair starts drawing differential current proportional to *Vin1-Vin2* and starts discharging the nodes V_P and V_Q. When the V_P and V_Q fall to $V_{DD} - V_{th,n}$ the NMOS cross-coupled transistors switch ON, allowing the discharge of nodes V_X and V_Y. The output voltages V_X and V_Y continue to fall until they reach V_{DD} - $|V_{th,p}|$, such that the PMOS cross-coupled pair switches ON. The positive feedback thus created by the cross-coupled transistors pulls one output back to V_{DD} while forcing the other to discharge to zero.

As for a major part of the conversion V_X and V_Y outputs are invalid, an SR Latch follows the output of the StrongARM Latch. The inverters act as buffers between the two latches and allow the SR Latch to toggle only when either V_X or V_Y falls.

3.6.3 Constant-gm biasing circuit

The biasing currents for the gm-stage and the integrators are generated on-chip using the constant gm biasing circuit as shown in Figure 3.22.

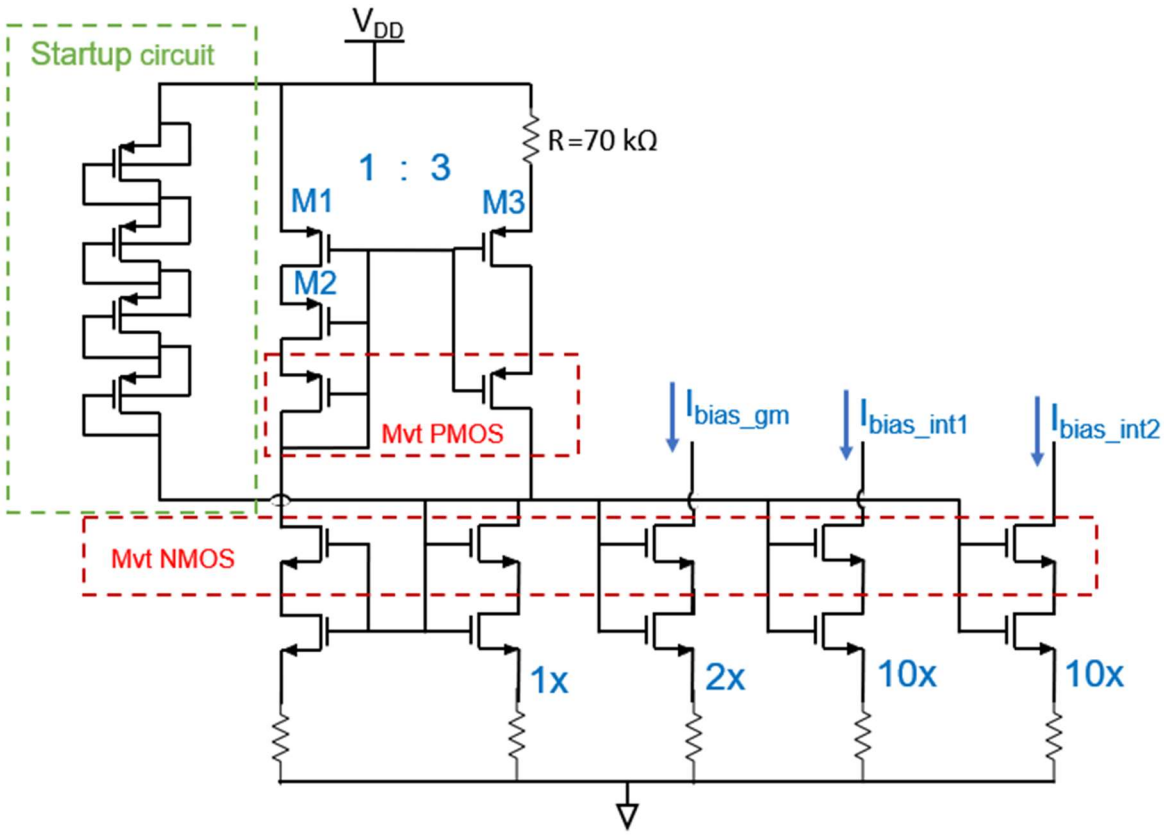


Figure 3.22: Constant gm biasing circuit.

As in [15], a current ratio of 1:3 is used to generate constant-gm equivalent to $\frac{\sqrt{2}}{R}$. This ensures that the current flowing through transistors M_1, M_2, and M_3 is PVT-independent as long as the transistors are in saturation. A silicided p-poly resistor is used for its low-temperature coefficient in the chosen process. The current mirrors are realized with NMOS transistors. To improve the matching of the devices, the NMOS current mirrors are degenerated [25]. Medium-V_{th} devices (Mvt) are used to self-cascode the transistors [15]. A start-up circuit is included to avoid the unwanted state where all transistors are off, which can arise due to the positive feedback around the circuit. The transistors in the start-up circuit are sized to not affect the circuit performance during normal operation.

4. Measurement results

This chapter describes the measurement setup and the results of measurements of 6 test chips fabricated in TSMC 180nm CMOS technology. Each chip has 4 different ETF structures and each has its readout circuit. The die micrograph of the test chip is shown in Figure 4.1, while a zoomed-in image of the S24 TD sensor is shown in Figure 4.2.

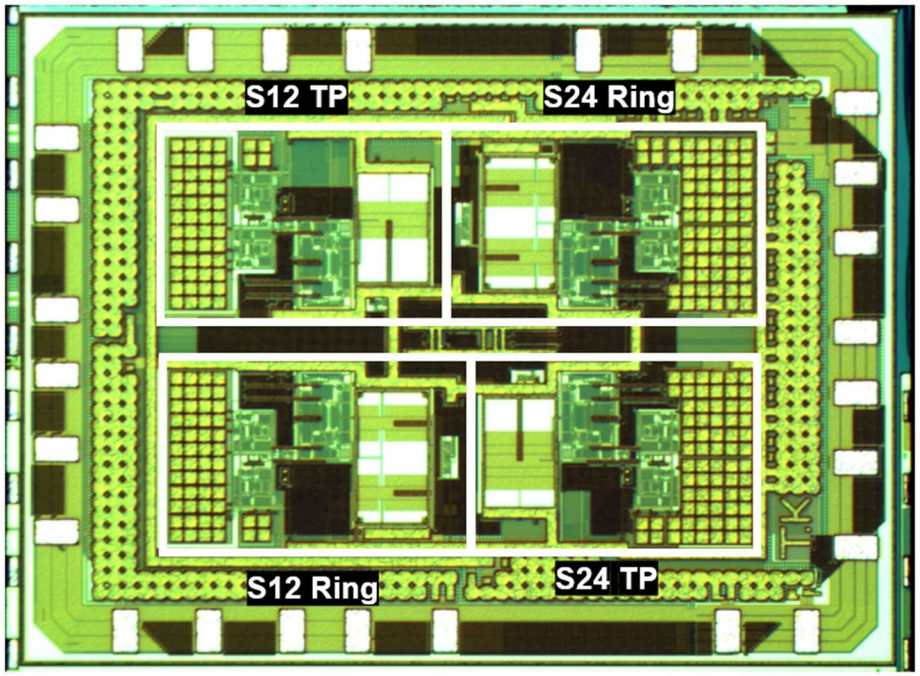


Figure 4.1: Die micrograph.

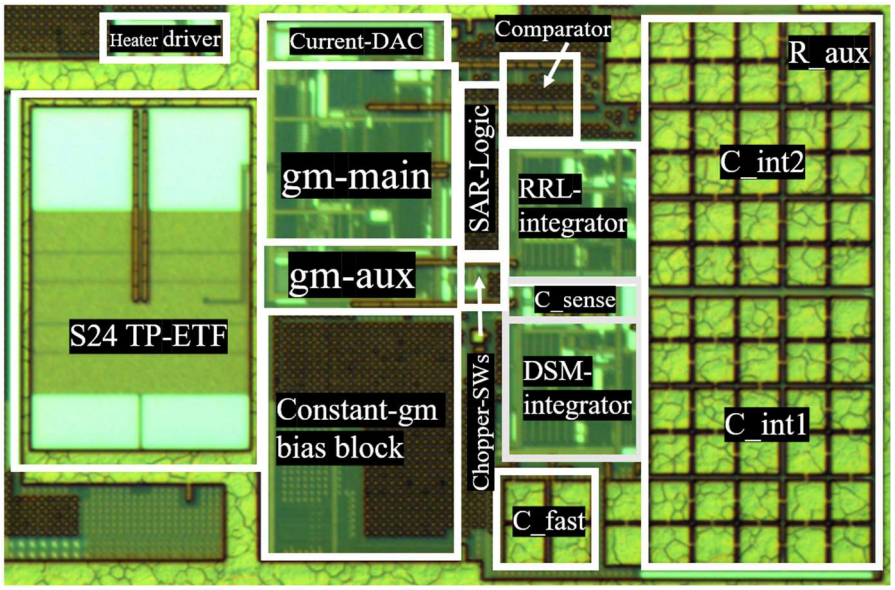


Figure 4.2: Zoomed-in image of S24 TP TD-sensor.

The area of each TD sensor (ETF + readout) is 0.25 mm^2. The ETF structures are not visible since they are shielded by metal layers. The middle of the chip includes the frequency dividers and other digital circuitry, while the rest of the chip is covered by decoupling capacitors.

4.1 Measurement Setup

The block diagram of the measurement setup is shown in Figure 4.3. The test chips were packaged in ceramic 24-pin dual in-line (DIL) packages and were mounted on the PCB using through-hole sockets. The PCB board was designed to test 6 chips at a time. To create a stable and accurate temperature environment for the device under test (DUTs), the PCB was placed in a heavy metal box, which acts like a thermal filter, and a conductive thermal paste was used to create close contact between the chips mounted on the PCB and the metal box. The metal box was placed inside a Vötsch 7004 oven, and the oven temperature was swept from -55°C to 180°C. The temperature inside the metal box was also monitored by a Kelvin-connected Pt-100 sensor, which was calibrated for an error of less than 0.01°C. The Pt-100 sensor was read out by a Keithley 2001A multimeter. A Keysight function generator was used to generate the master clock. The control bits were written to the shift registers on the chip using the FPGA Cyclone V, and the output bitstream was post-processed in a PC. The wires going in/out of the oven were taken through a tightly sealed opening. The PC controlled the power supply, function generator, multimeter, and oven using the LabVIEW application through GPIO ports.

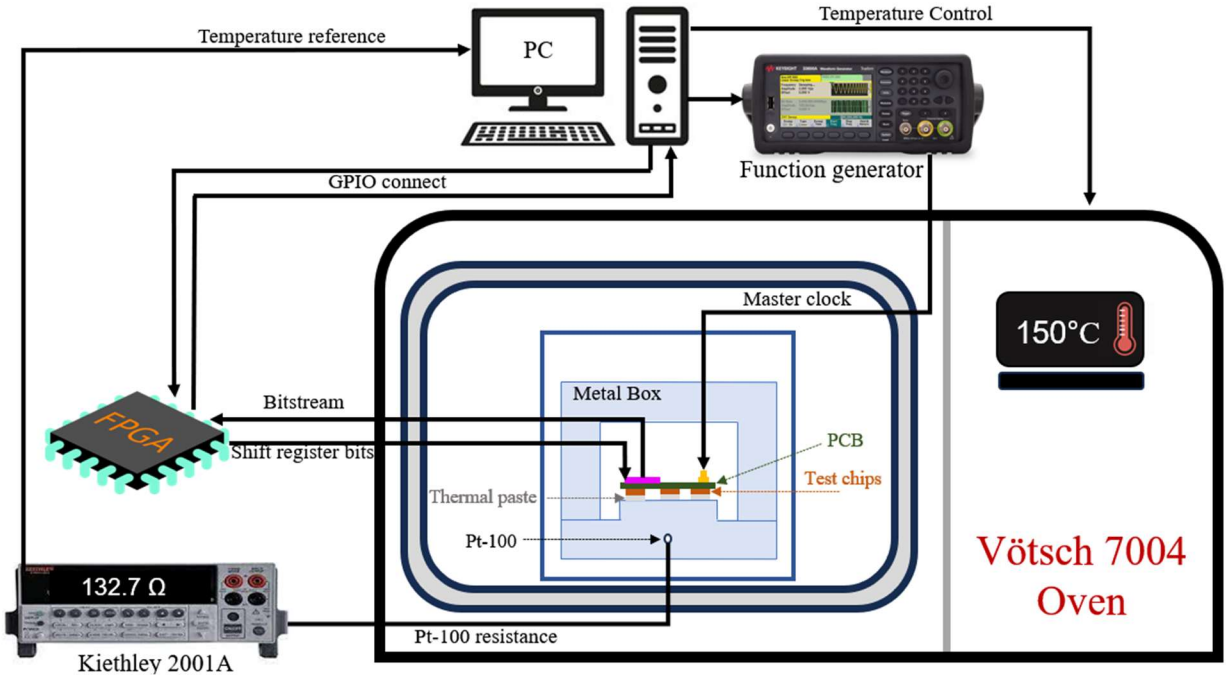


Figure 4.3: Block diagram of measurement Setup.

4.2 SAR trim and RRL

In the design, test pins were placed in the S24 sensor at the differential outputs of both the integrator used in the PD-DSM (*A* and C_{int1}) and the integrator used in the RRL (*A2* and C_{int2}). As a first check, these signals were observed at room temperature (27°C) to verify the operation of the hybrid RRL. Figure 4.4

shows the output of the PD-DSM's integrator when both the SAR trimming and RRL are switched off. The output is clipping due to the upmodulated input offset.

Figure 4.4: PD-DSM's Integrator output w/o SAR trim, w/o RRL.

Figure 4.5 shows the timing of the control signals when SAR trimming is switched on. It shows that after the reset signal has a falling edge, the polarity of the 6 trim bits is observed at the output. The bitstream of the DSM is generated when all trim bits have been loaded.

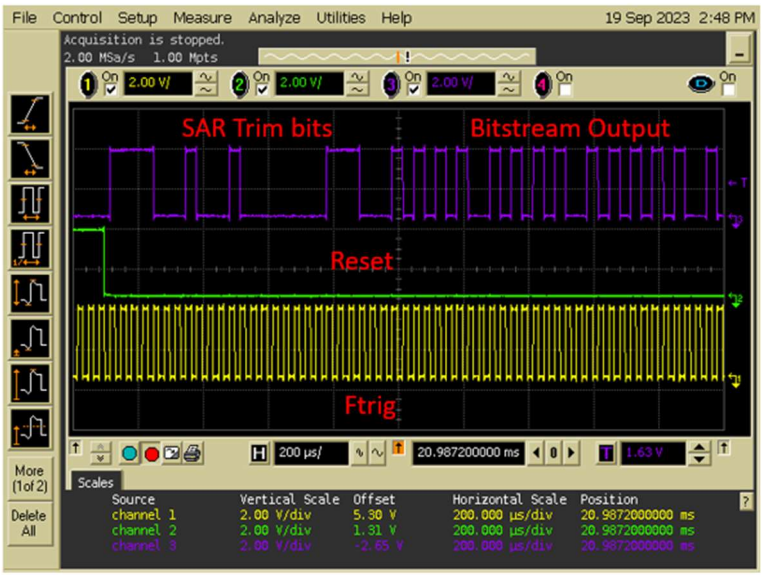


Figure 4.5: Timing Waveforms.

Figure 4.6 shows the integrator's output waveform in the DSM after the SAR trim. It can be observed that the offset has been reduced significantly, but still, there is an additional ripple riding over the integrator's output due to the residual offset. With the measured P_{heater} = 3.6mW, the peak-to-peak swing ($V_{swing,pk\text{-}pk}$) is about 250mV, which is slightly less than that predicted in Section 2.2.

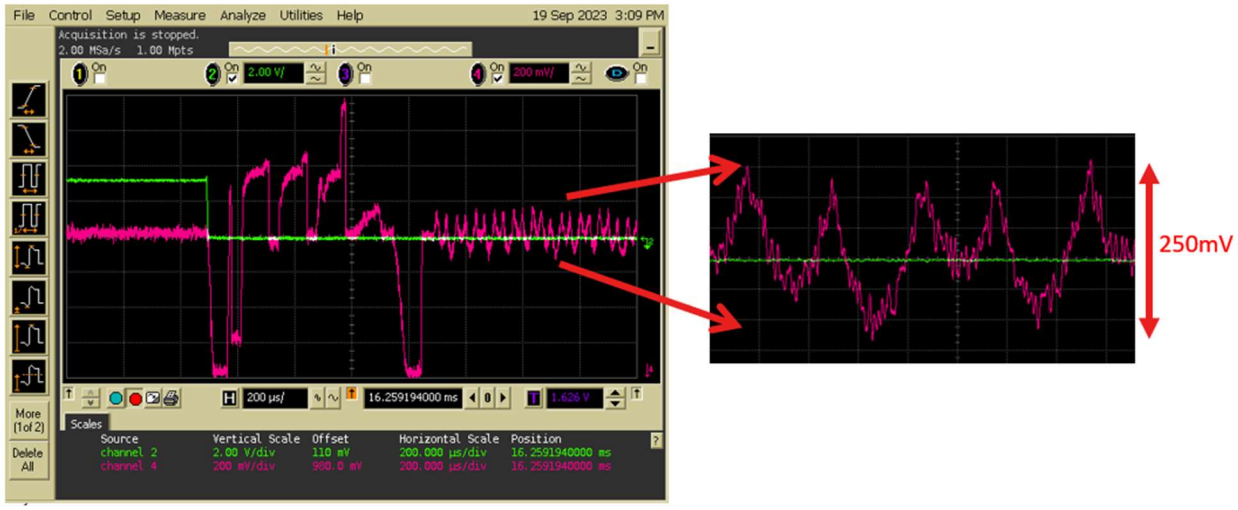


Figure 4.6: PD-DSM Integrator output with SAR trim and RRL Off.

Figure 4.7 shows the auto-generated SAR trim codes for the S24/12 ring ETF (left) and S24/12 TP-ETF (right) of the 6 test chips at room temperature - 27°C.

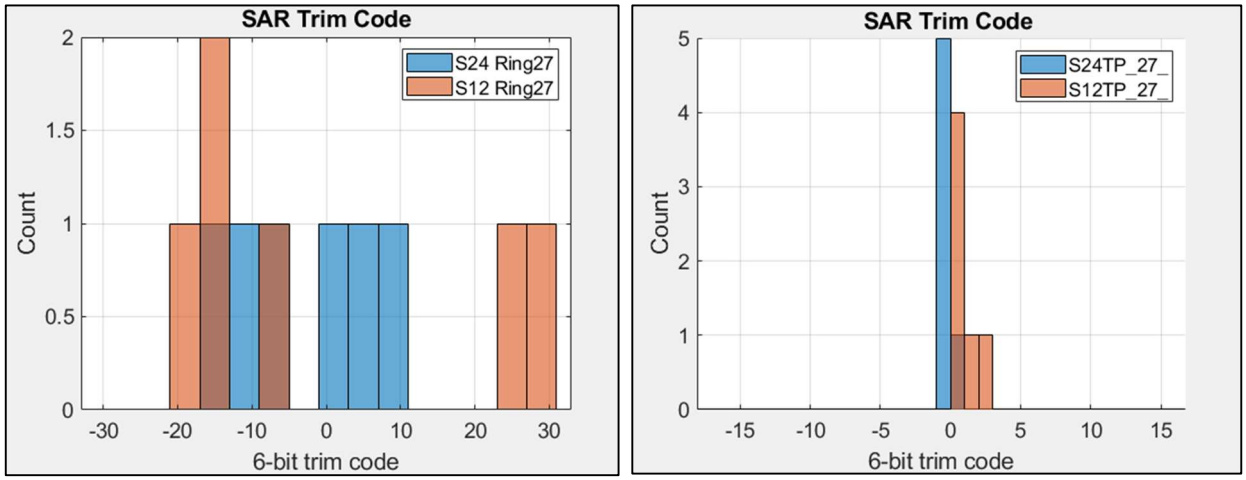


Figure 4.7: SAR Trim codes of 6 samples at RT.

It can be seen that the S12 ring ETF exhibits the most offset, with a worst-case trim code of [011110], which corresponds to around 15mV of input V_{OS}. This is close to the limit of the SAR trim and may cause clipping at high temperatures.

Figure 4.8 shows the integrator's output waveform after SAR trim and the RRL, it is observed that the ripple has significantly reduced.

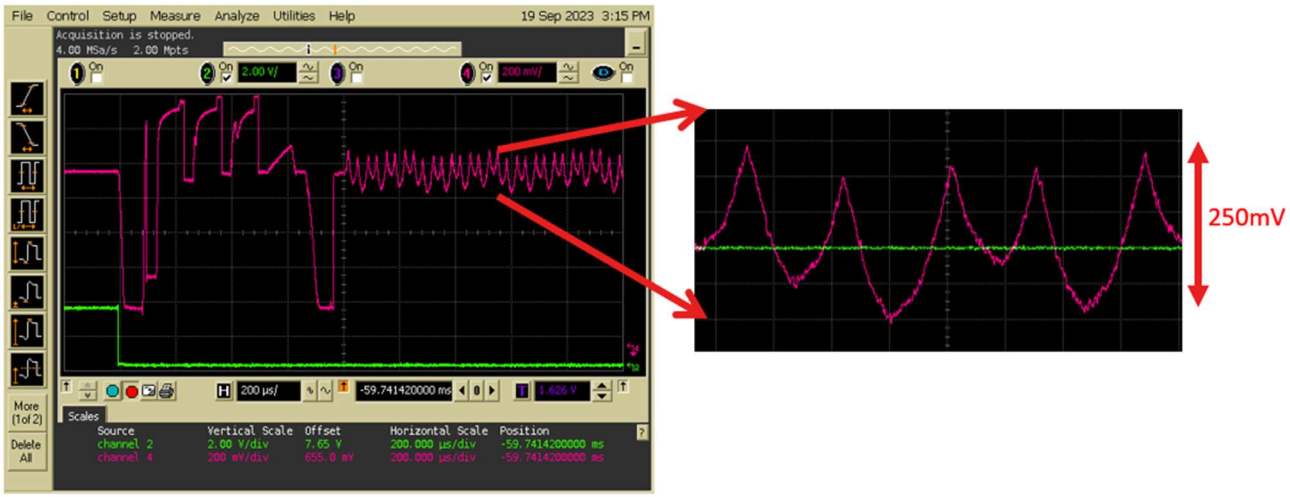


Figure 4.8: PD-DSM's Integrator output after SAR trim and RRL.

As the output test probe pins were only placed in the S24 TP readout, it wasn't possible to determine the output swing of the other ETFs. However, these waveforms validate the designed hybrid offset reduction technique in PD-DSMs.

4.3 RRL settling time constant

Next, the settling behavior of RRL was measured. As described in Section 3.4.2, the RRL can be operated in two modes. In the fast mode, a 3.6pF capacitance is added in parallel to the ripple sensing capacitor C_{sense} = 142fF. This should increase the settling speed of the RRL by 26.4x. This is confirmed by the measurement results shown in Figure 4.9, which show that the ratio of the settling times in fast and slow modes is ≈27 (= 5.4ms / 0.2ms).

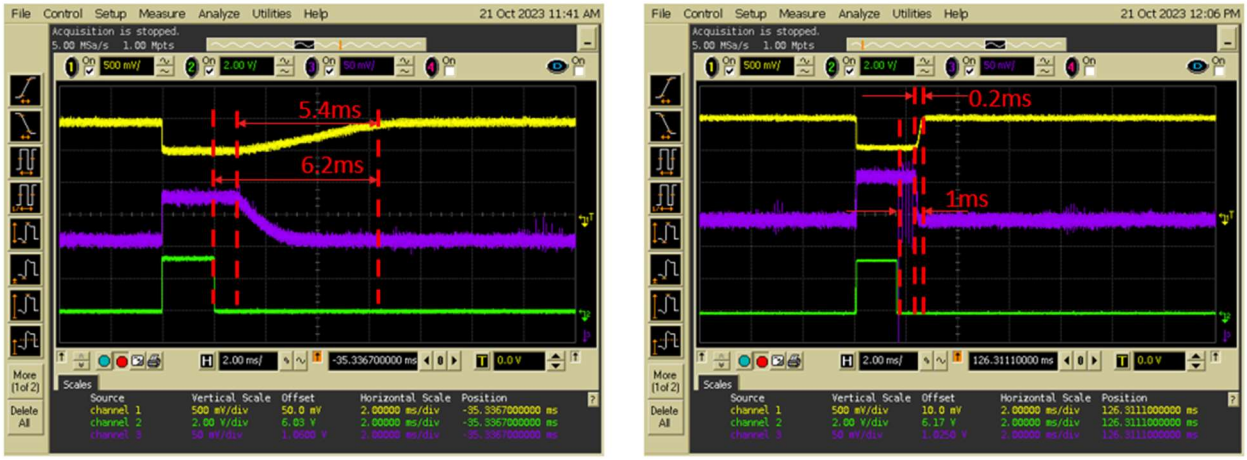


Figure 4.9: RRL Settling behavior (a) Slow mode (b) Fast mode.

However, in slow mode, the measured settling time is 15 times faster than expected. This was confirmed in simulations, which showed that the settling time depends on the value of the input offset voltage (V_{OS}), as shown in Figure 4.10.

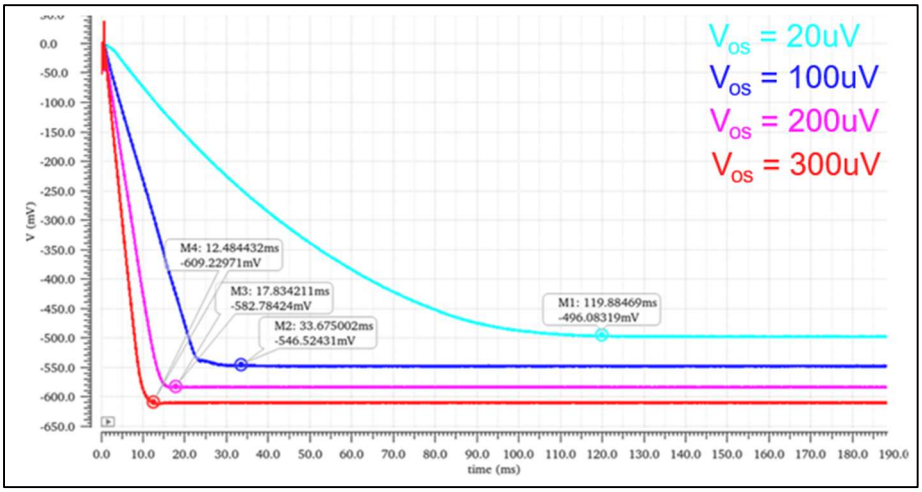


Figure 4.10: Transient settling of RRL with different input V_{os}.

The reason for this behavior was tracked down to the limited offset correction range of the RRL. From Equation 2.17, the ratio between gm-main(=1.4mS) to gm-aux(=40nS) is 36000, which limits V_{os} to 57µV before bringing gm-aux out of its linear region (+/-1V). However, the worst-case error after the SAR conversion is 0.5*LSB = 300µV.

4.4 Bandwidth limitation

During measurements, it was observed that the TD sensor's phase error was larger than expected. AC simulations of the transconductance linking the differential input voltage of gm-main to the differential current flowing into the DSM's integration capacitor were made. As shown in Figure 4.11, the resulting BW is only around 13 MHz, and the associated phase error at f_{drive} = 30kHz is around 74m°ϕ. This BW is much lower than the targeted 800MHz.

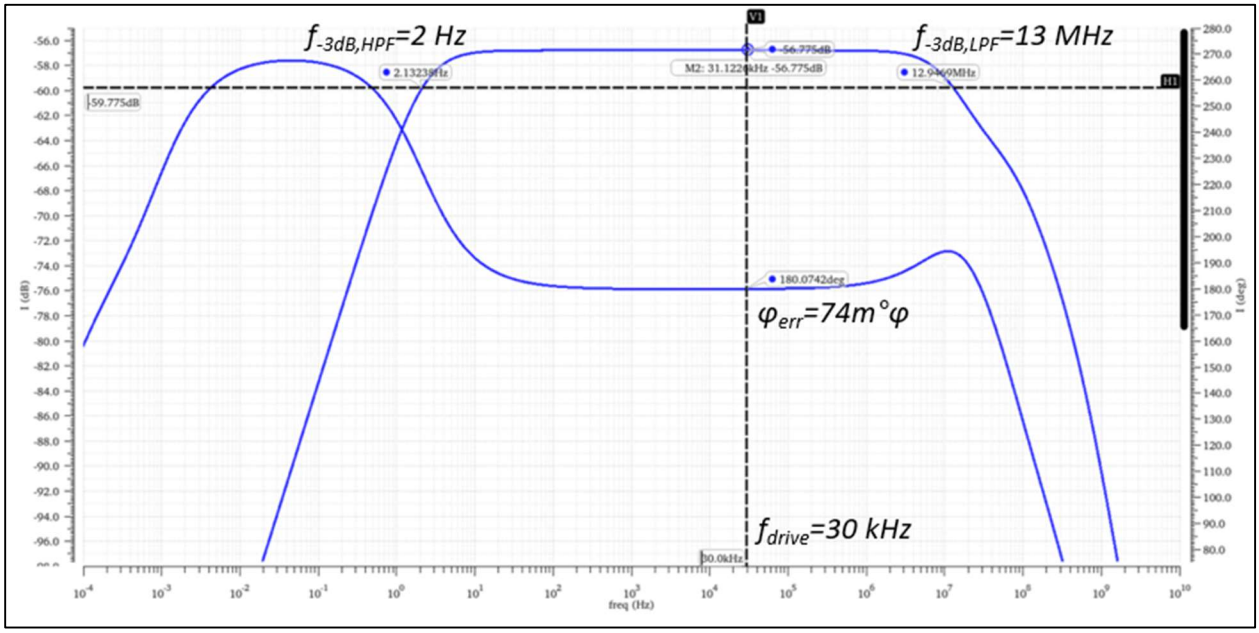


Figure 4.11: Voltage-to-current transfer function of the system.

One reason for this could be that the input impedance of the DSM's integrator (Z_{in}) (Section 3.3), and the R_{on} of the switches used in the demodulator chopper (CH1) (Figure 4.12) are too large compared to the output impedance of the gm-stage.

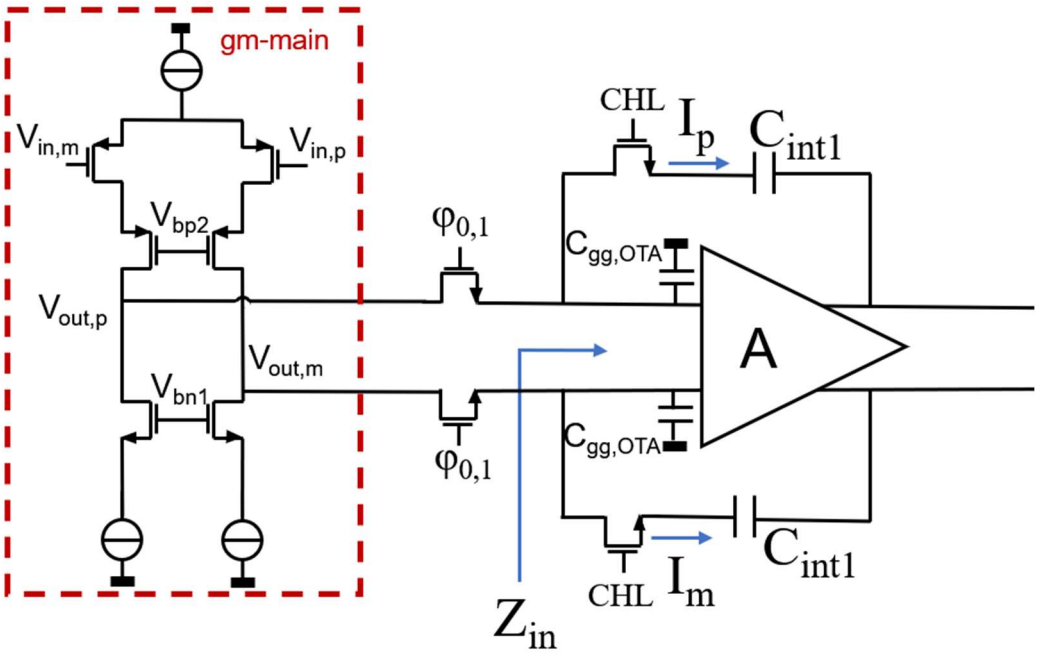


Figure 4.12: Block diagram showing Chopper switches and input impedance of PD-DSM's integrator

The demodulator choppers were implemented with minimum-sized NMOS transistors to reduce their charge injection. The resulting on-resistance (R_{on} ≈5.8kΩ) is then significant compared to the input impedance of the integrator (Z_{in}≈11kΩ at 30kHz). Furthermore, the output impedance $R_{out,gm}$ of the gm-stage is only 5.7MΩ, and so the current divider it forms with R_{on} + Z_{in} may cause more phase error. Ways to mitigate these issues are discussed in Section 5.1.2.

4.5 Phase Characteristics

4.5.1 Phase vs f_{drive}

Even though there were a few issues with the test-chip, some important measurements were done to characterize the designed ETFs. First, the proportionality of φ_{ETF} with $\sqrt{f_{drive}}$ was evaluated. This was done by sweeping f_{drive} and keeping the temperature constant. The measurements were done with and without the use of the RRL. The ambient temperature of 27°C was maintained during the measurements. Figures 4.13 and 4.14 show the phase outputs of the S24 and S12 TP-ETFs with and without RRL. It is observed that the S24 TP results are in good agreement with the theoretically calculated phase vs f_{drive} relation (the dotted line), whereas a deviation from the phase and f_{drive} relation is observed in S12 TP.

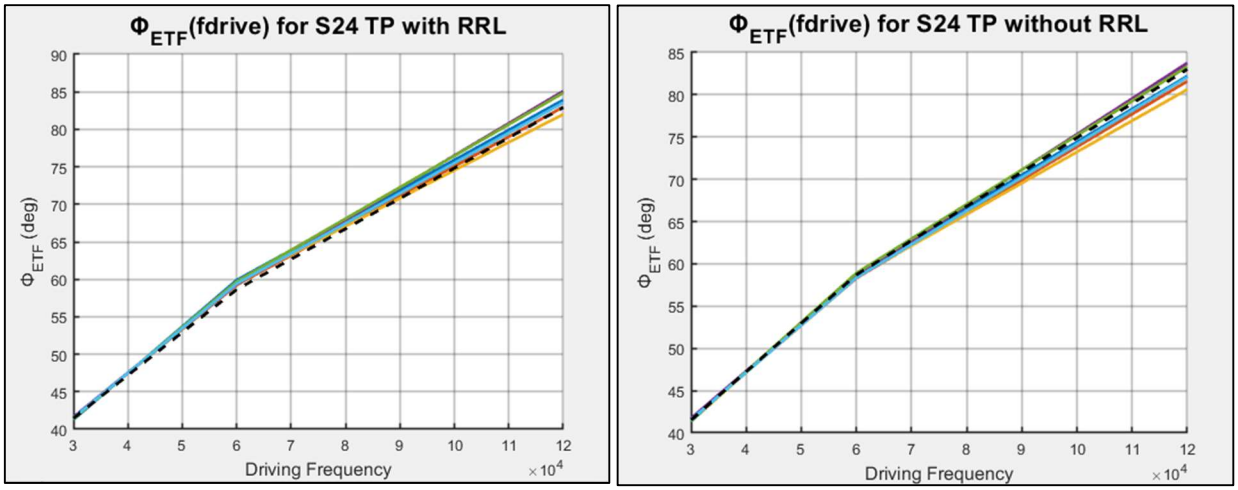


Figure 4.13: Phase vs frequency behavior at constant temperature for S=24um TP-ETF

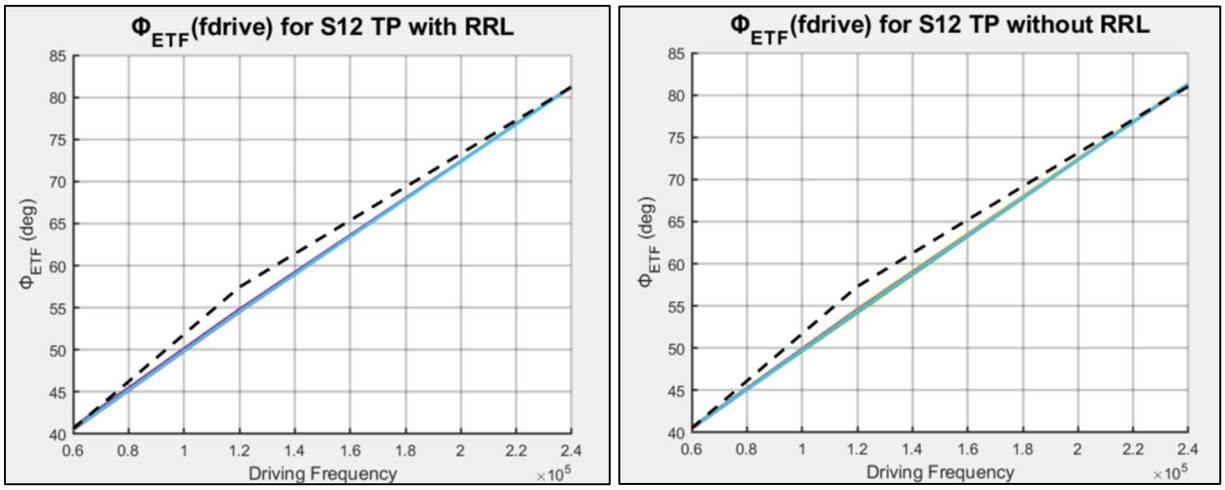


Figure 4.14: Phase vs frequency behavior at constant temperature for S=12um TP-ETF.

When the difference between the phase output obtained with and without RRL is plotted, it is much less for the S12 TP ETFs than for the S24 TP ETFs. This can be attributed to smaller V_{ripple}, due to higher driving frequency and hence less introduced phase error, as shown in Figure 4.15. However, the spread in the error is higher for the S12 TP ETFs than for the S24 TP ETFs.

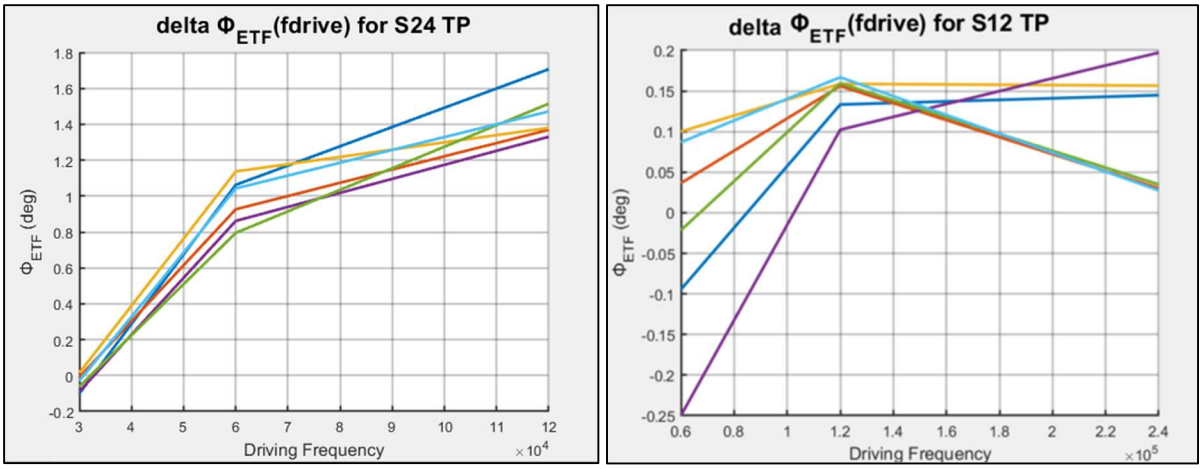


Figure 4.15: Delta phase output for TP-ETF, with and without RRL.

Similar measurements were performed for S24 and S12 ring ETFs and are shown in Figure 4.16-4.18.

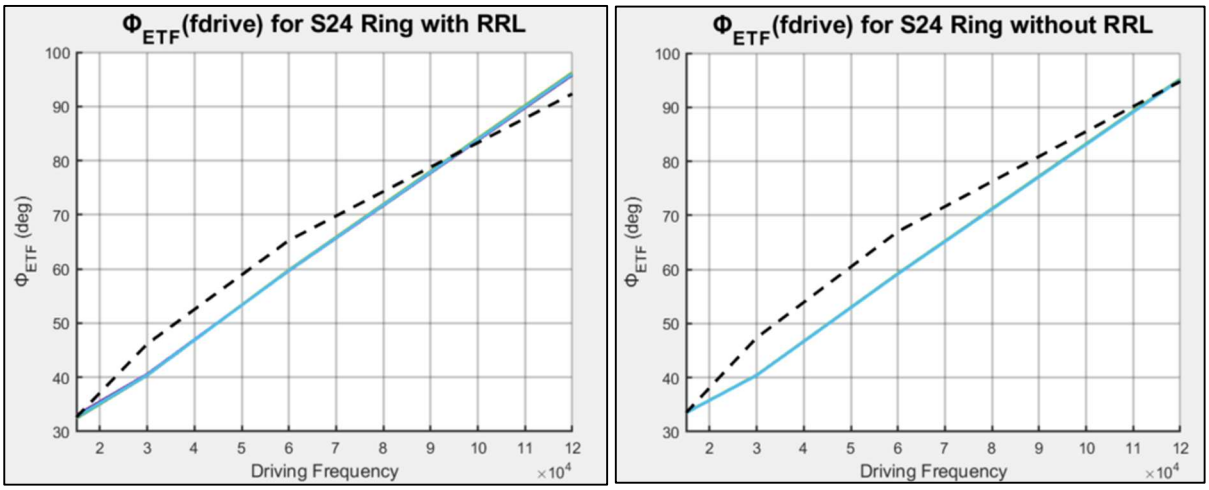


Figure 4.16: Phase vs frequency behavior at constant temperature for S=24um ring ETF

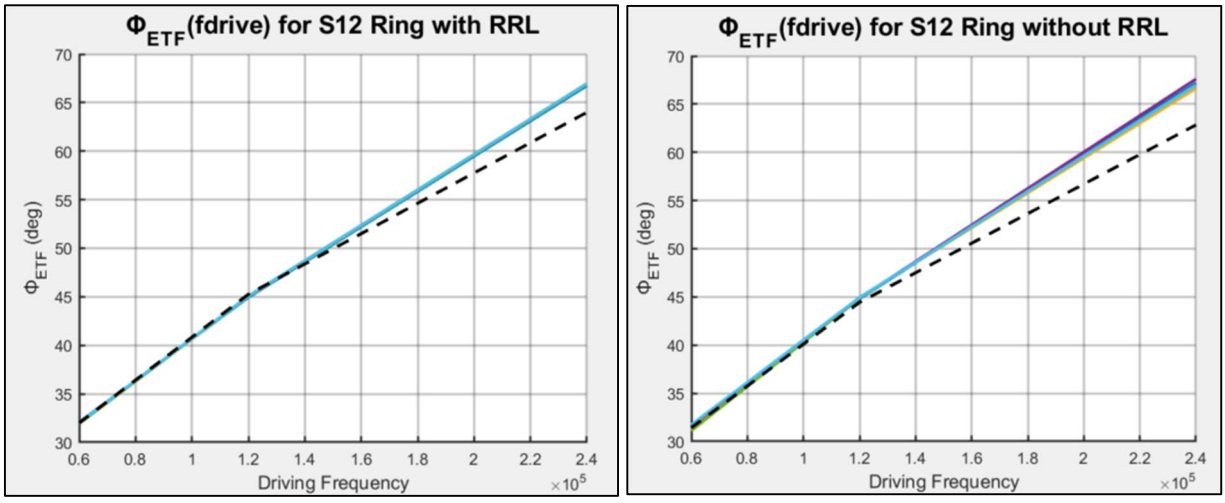


Figure 4.17: Phase vs frequency behavior at constant temperature for S=12um ring ETF.

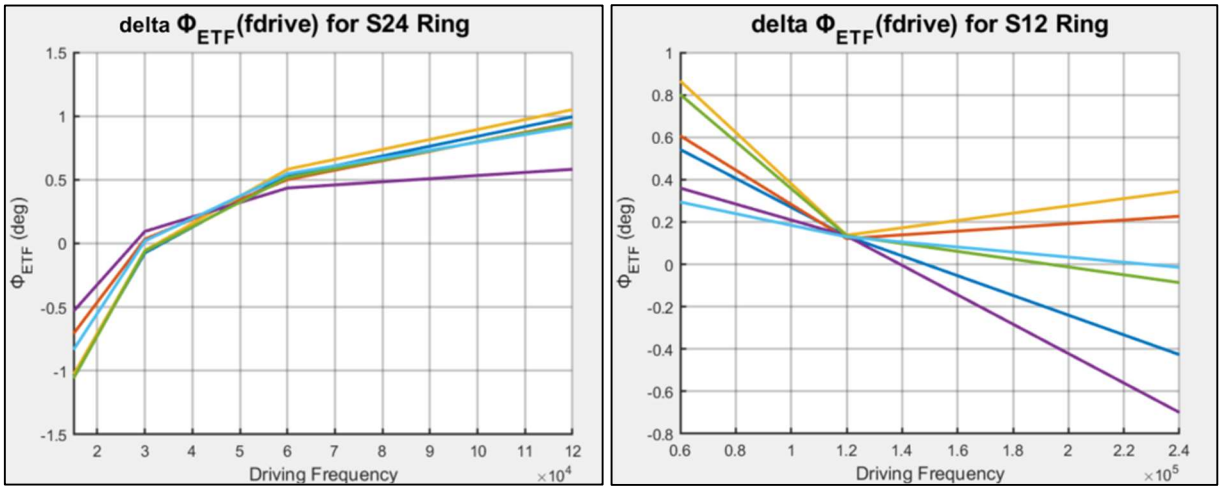


Figure 4.18: Delta phase output for ring ETF, with and without RRL.

These measurements were also crucial in finding the optimum driving frequency and the phase DAC range of the designed ETFs.

4.5.2 Phase vs temperature

The driving frequency and phase DAC range used for different ETFs that covered the entire range of temperature and gave the best results are shown in Table 4.1.

Table 4.1: f_{drive} and DAC range for different ETFs.

ETF	f_{drive}	DAC range
S24 TP	28.75kHz	[22.5°- 67.5°]
S12 TP	115kHz	[22.5°- 67.5°]
S24 ring	43.75kHz	[45°- 90°]
S12 ring	175kHz	[45°- 90°]

Figures 4.19 and 4.20 show the phase vs temperature plots of the designed ETF structures. The measurements show a near-linear relationship of the phase output of the ETFs with the temperature which aligns with the theoretical analysis. The driving frequency and the DAC range were chosen such that the ETFs can cover the temperature range of -55°C to 180°C. However, one sample of S24TP/ring ETFs and S12 TP/ring ETFs could not operate at the extreme temperature of 180°C. The reason for the clipping was suspected to be the DAC phase range overload.

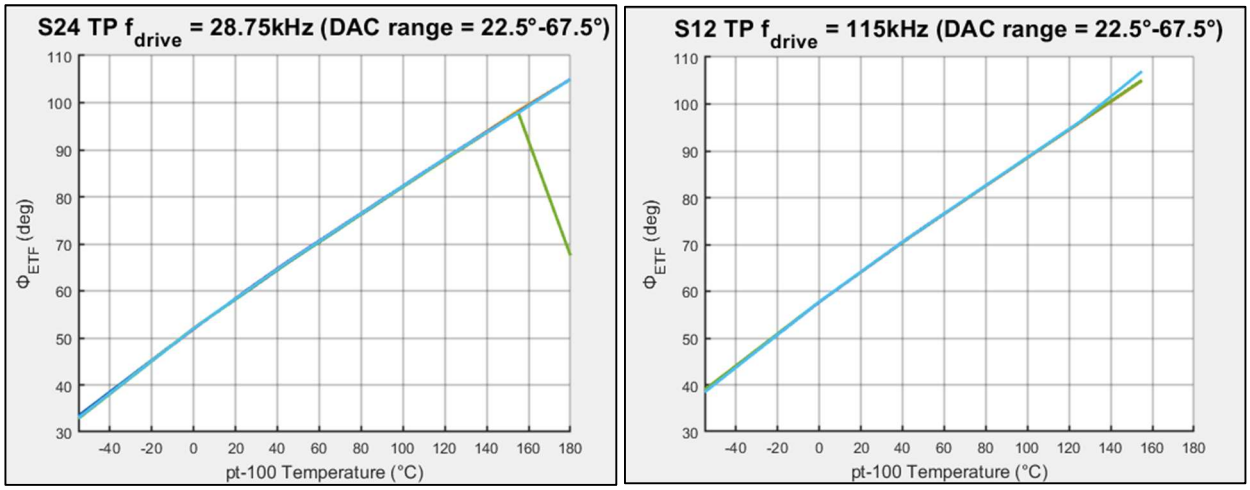


Figure 4.19: Master Curve for TP-ETF.

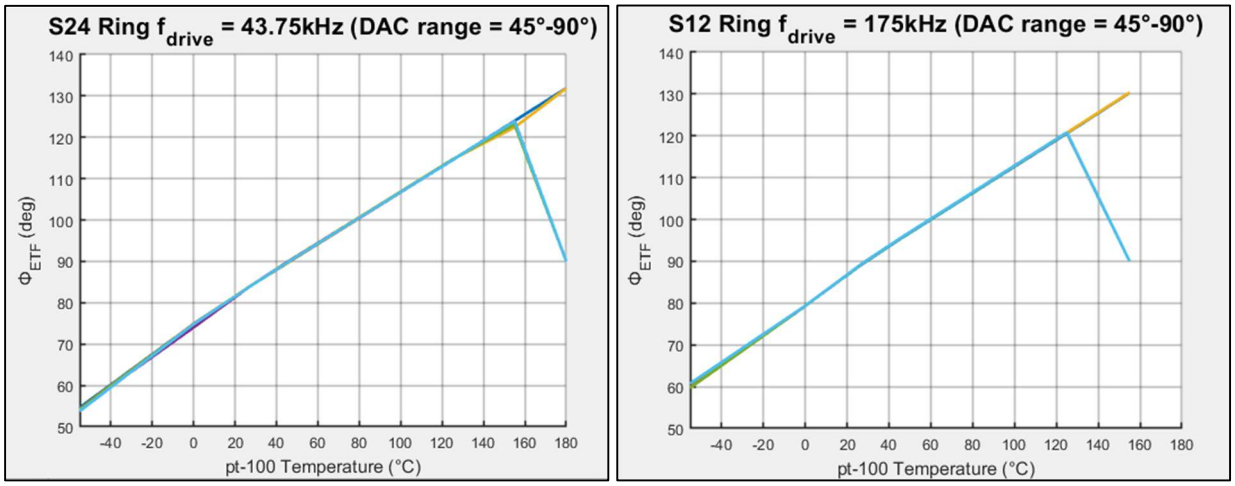


Figure 4.20: Master Curve for ring ETF.

The measured sensitivities (°ϕ/°C) of various ETFs, based upon the obtained Master curves for temperatures -55°C to 125°C are listed in Table 4.2.

Table 4.2: Sensitivities of different ETFs

ETF	Sensitivity (°ϕ/°C)
S24 TP	0.3
S24 ring	0.34
S12 TP	0.32
S12 ring	0.33

The measured sensitivity numbers are slightly higher than the ones measured in [15]. The S24 ETF implemented in [15] had a sensitivity of 0.21°ϕ/°C.

4.6 Inaccuracy

Figures 4.21-4.24, show untrimmed inaccuracy plots of the designed ETFs with and without RRL. Since the output of the modulator clipped in some samples, the inaccuracy is only plotted from -55°C to 125°C. Even though the desired inaccuracy of less than 0.2°C was not achieved, the following graphs show that the 3σ spread of the designed ETFs reduces when the RRL is enabled especially for S12 ETFs driven at high frequency.

The high inaccuracy numbers are attributed to the additional phase error introduced by the readout architecture due to the reasons discussed in Section 4.3 and Section 4.4. The phase output of the ETFs is smaller for lower temperatures and the phase error introduced by the readout is quite large for temperatures below 0°C. Hence higher inaccuracy is observed at low temperatures.

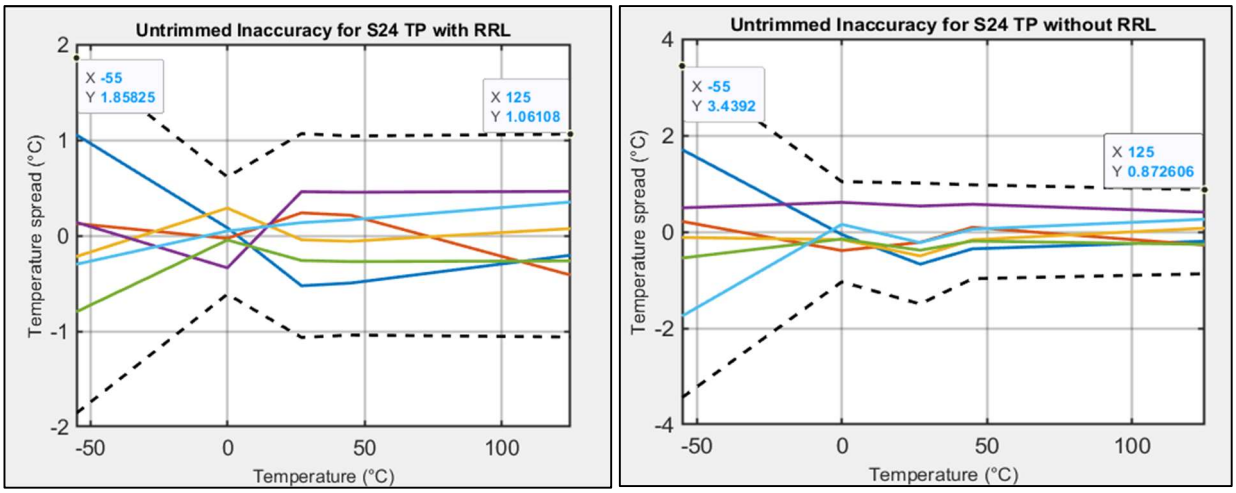


Figure 4.21: Untrimmed Accuracy of S24 TP-ETF.

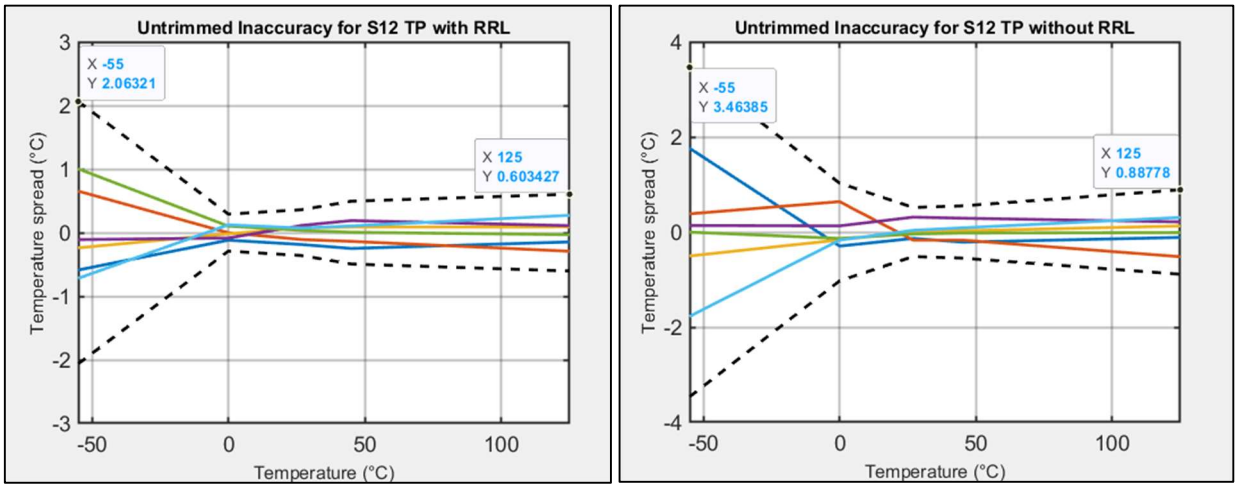


Figure 4.22: Untrimmed inaccuracy of S12 TP-ETF.

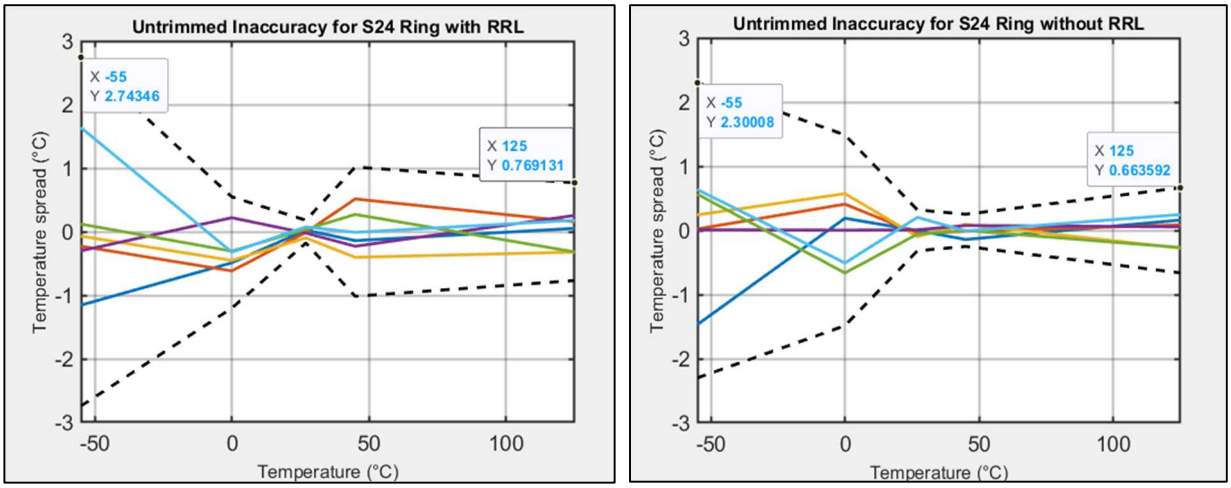


Figure 4.23: Untrimmed inaccuracy of S24 ring ETF.

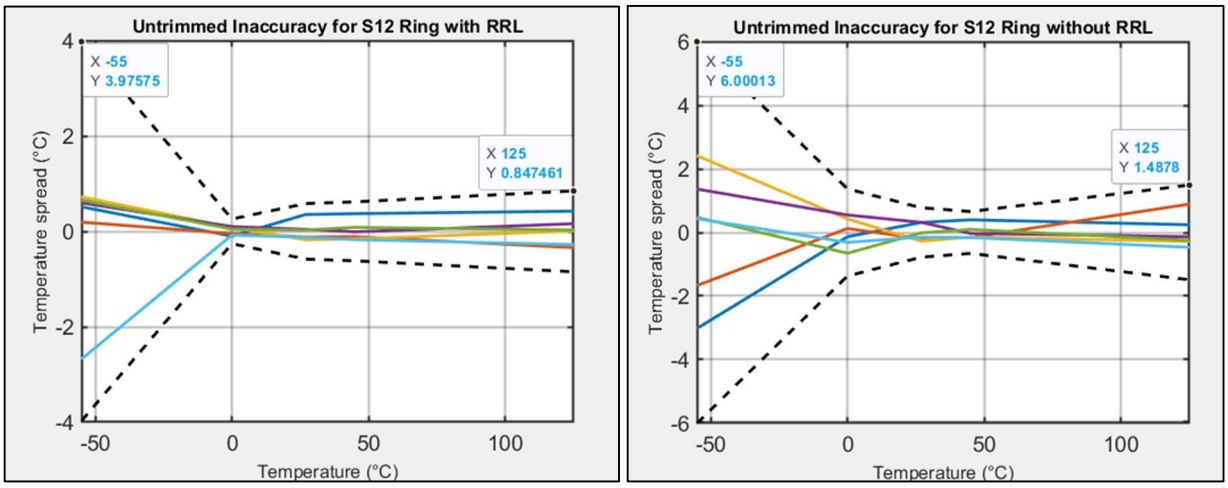


Figure 4.24: Untrimmed inaccuracy of S12 ring ETF.

The measured results are not consistent enough to draw any strong conclusions about the inaccuracy of the ETFs. However, a pattern is seen with the results of S24 and S12 ETFs. When driven at high driving frequency, the spread in the inaccuracy of S12 ETFs improves with the RRL ON, whereas the opposite is observed for S24 ETFs. This is again because the S12 ETFs are driven at 4 times higher frequency than the S24 ETFs, the peak-to-peak amplitude of the ripple is reduced, hence resulting in less error introduced by the RRL.

4.7 Bitstream Spectra

Figures 4.25 show the FFTs of the bitstream output of S24 TP and S24 ring ETF at -55°C, 180°C and room temperature. The ring ETFs show around 10 dB lower noise floor when compared with the TP-ETFs.

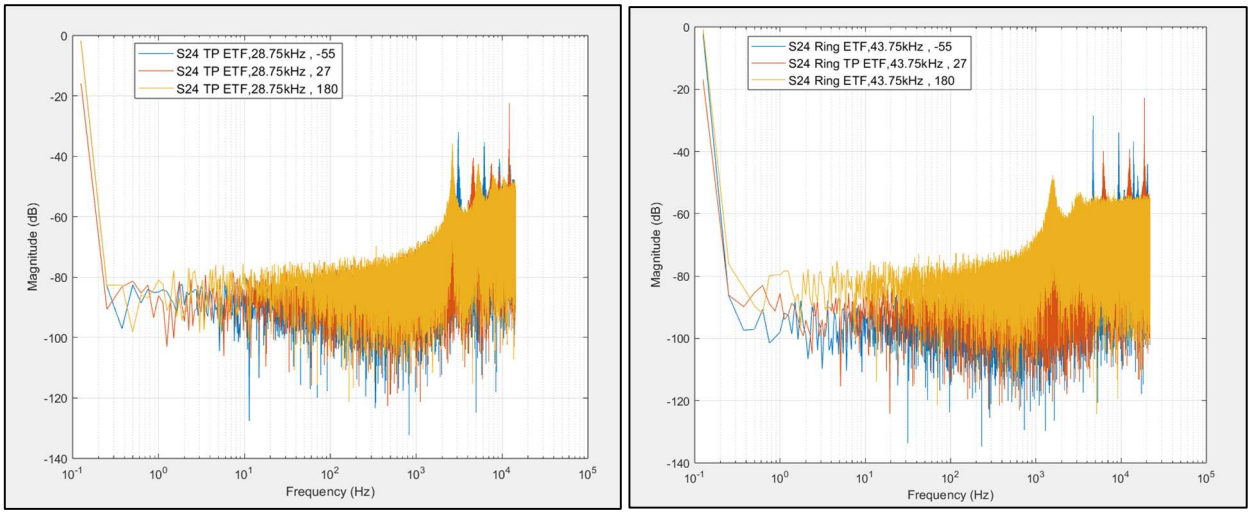


Figure 4.25: Bitstream spectra of S24 TP and ring ETF for different temperatures.

As shown earlier, the output of S12 ETF clipped at 180°C, therefore in Figures 4.26 and Figure 4.27 the FFTs of all the ETF structures are plotted for the highest temperature of 155°C.

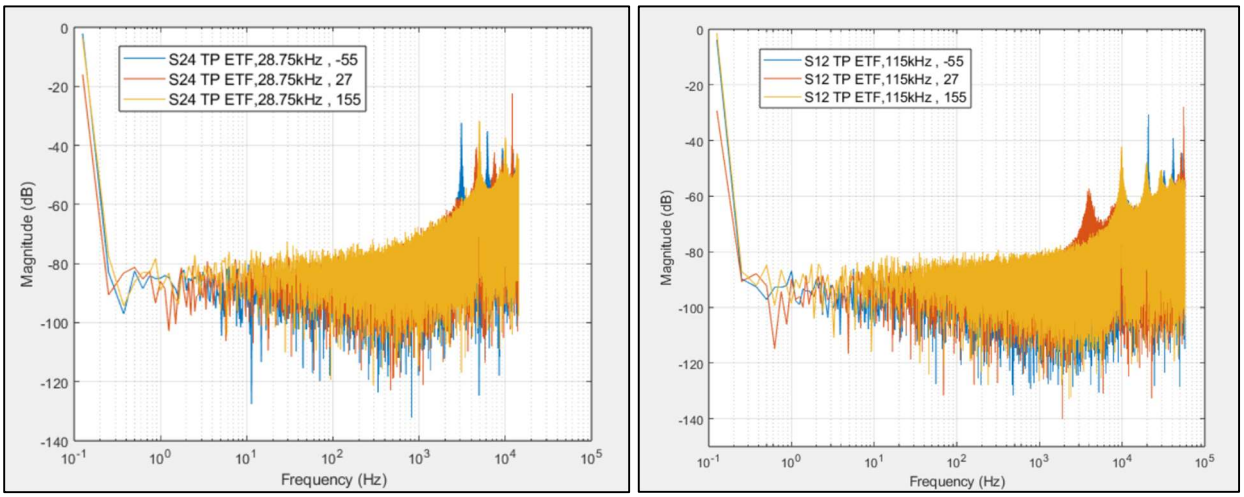


Figure 4.26: Bitstream spectra of S24 and S12 TP-ETF for different temperatures.

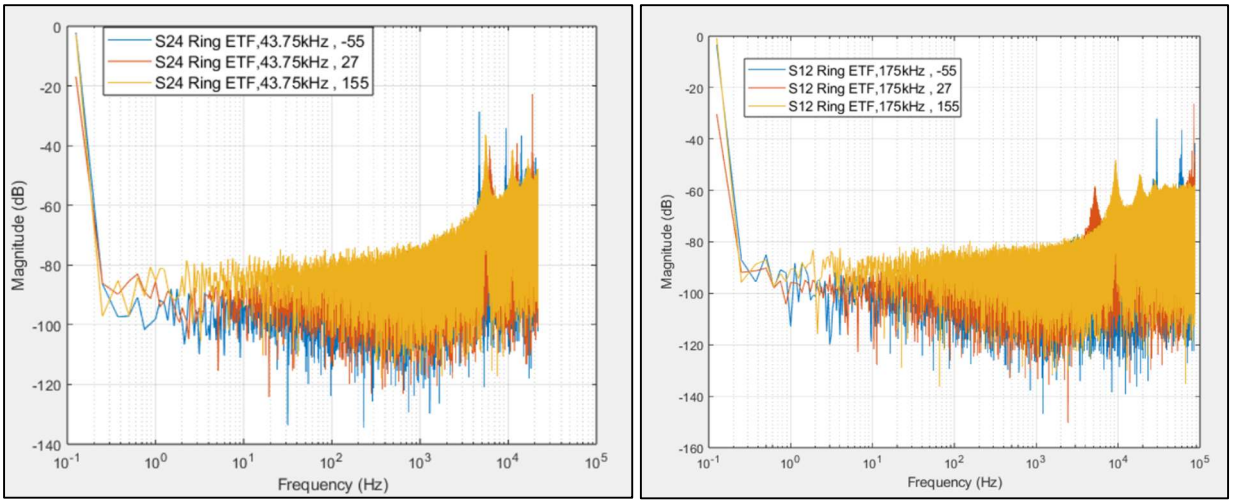


Figure 4.27: Bitstream spectra of S24 and S12 ring ETF for different temperatures.

4.8 Resolution

The resolution of TD sensors is heavily limited by the thermal noise of the ETF and the readout system. To measure the resolution of the various ETFs at room temperature, the bitstream output of the readout is decimated by a sinc2 filter and converted to temperature using the estimated sensitivity of TP and ring ETFs as listed in Table 4.2. The measured resolution of various ETFs is plotted in Figure 4.28.

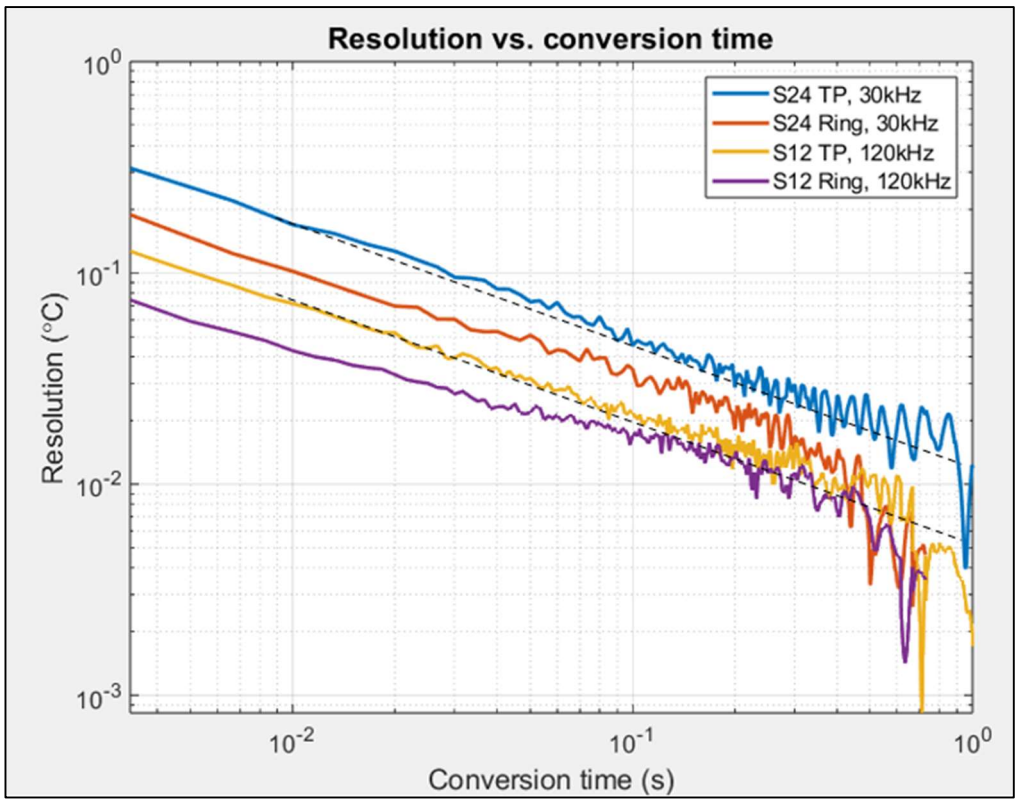


Figure 4.28: Resolution vs conversion time.

Table 4.3 gives a comparison table of achieved resolution for different ETFs for T_{conv} = 1s.

Table 4.3: Resolution of different ETFs

ETF	Resolution (mK)
S24 TP	25
S24 ring	16
S12 TP	11
S12 ring	8

5. Conclusion and Future Work

This thesis describes a phase-domain delta-sigma modulator (PD-DSM) for the readout of thermal-diffusivity based temperature sensors. To achieve high accuracy, any phase errors introduced in the signal path must be minimized. An additional challenge is to reduce the offset at the input of the readout circuit, which, after chopper phase detection, is converted to a large voltage ripple at the output of the modulator's loop filter. The main novelty of this work lies in the implementation of a hybrid ripple reduction loop, which operates robustly up to high temperatures and reduces the offset to sub-µV levels. The loop consists of a 6-bit current DAC, which removes most of the offset at the start of a conversion, while a continuous-time ripple reduction during the DSM conversion removes the remaining offset and drift. Even though the resulting sensor did not achieve high accuracy, the causes for this inaccuracy have been identified, thus paving the way for a successful redesign.

5.1 Future Work

5.1.1 Better linearity of gm-aux

As previously discussed in Section 4.3, it was observed that the settling behavior of the RRL is highly dependent on the magnitude of the residual offset voltage, resulting in a higher spread in the phase error of the DSM. Therefore, the design of the RRL imposes a challenge in keeping the high-pass corner of the transfer function below 2 Hz. Continuing the discussion in Section 4.3, the limitation lies in the limited linear range of the designed gm-aux. The linear range of the gm-aux is constrained by the output swing of the integrator in the RRL and the supply rails. Additionally, the gm-aux designed in the RRL has a very low transconductance to achieve the low high-pass corner, but at the same time it increases the ratio between gm-main and gm-aux, given as:

$$\frac{gm\_main}{gm\_aux} * V_{OS} \approx V_O$$

Hence, the potential way to mitigate this issue is to reduce the offset correction range of the RRL, this can be achieved by higher resolution SAR trimming. If the rest of the design is kept the same, at least an 8-bit SAR trimming is required to reduce the initial offset by $1/2^8$, reducing the residual offset to 62µV instead of 300µV.

5.1.2 Increased bandwidth

As discussed in Section 4.4, the observed bandwidth of the system was reduced significantly by the design of the integrator and the chopper switches. Therefore, to mitigate this effect some design changes are recommended.

Figure 5.1 shows the simplified test benches used to debug the low-pass characteristic of the transconductance AC response.

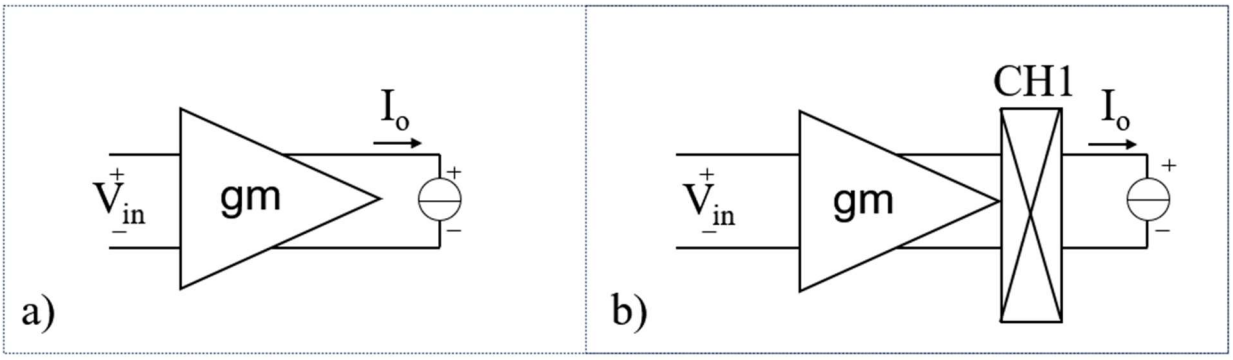


Figure 5.1: Transconductance AC Response Testbench, gm-stage driving a) an ideal virtual ground; b) an ideal virtual ground with demodulator.

Figure 5.2 shows the simulated low-pass -3dB point in three cases:

1. Green curve: corresponds to Figure 5.2 a), with the gm-stage driving an ideal virtual ground.
2. Blue curve: corresponds to Figure 5.2 b), with the gm-stage driving an ideal virtual ground with the demodulator at the output.
3. Pink curve: also corresponds to Figure 5.2 b) with increased demodulator switches size (W= 16 times W_{min}).

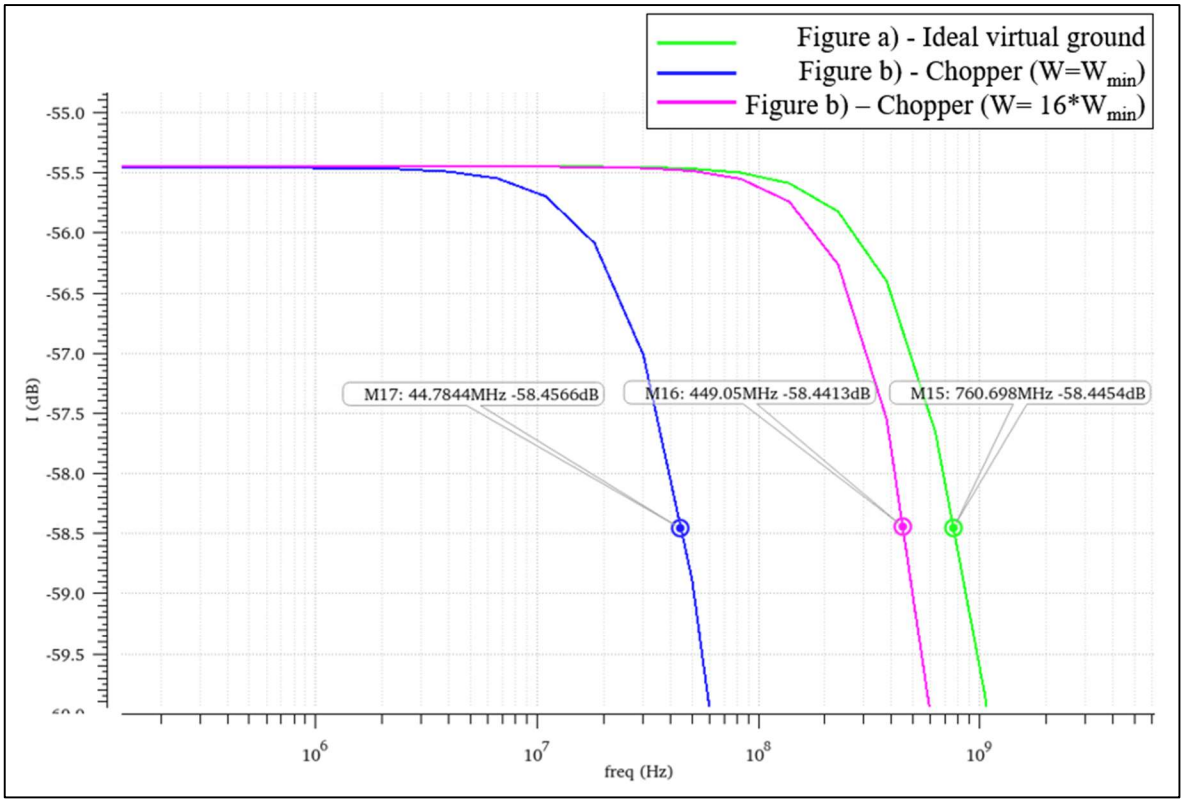


Figure 5.2: V-to-I transfer showing -3dB Bandwidth of the gm-stage corresponding to the test benches shown in Figure 5.1.

The above results indicate that the switch sizes used in the demodulator are limiting the -3dB bandwidth of the transconductance AC response. It is recommended to use at least 3.5um width switches, which reduces the R_{ON} to 362Ω.

The input impedance of the integrator is also limiting the -3dB bandwidth. It is desirable to keep the integrator operating at low power. Therefore, a possible solution that realizes a lower input impedance at a low bias current is to use a two-stage amplifier, as in [15]. The input impedance of a two-stage OTA with a feedback integration capacitor and miller compensation (C_M) is given by Equation 5.1. The simplified small-signal model used to derive this is shown in Figure 5.3.

$$Z_{in}(s) = \frac{s^2 C_M r_{o1} r_{o2}(C_{load} + C_{int1}) + s[r_{o2}(C_{load} + C_{int1} + C_M) + C_M r_{o1}(1 + gm_2 r_{o2})] + 1)}{s^3 C_{int1} C_{load} C_M r_{o1} r_{o2} + s^2\left[C_{int1} C_M r_{o1}\left(1 + r_{o2}(gm_1 + gm_2)\right)\right] + sC_{int1} gm_1 r_{o1} gm_2 r_{o2}} \tag{5.1}$$

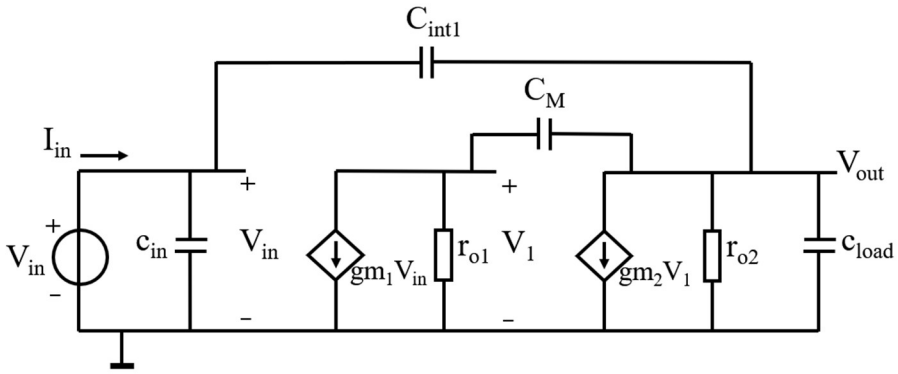


Figure 5.3: Small-signal model of two-stage integrator.

The input impedance behavior over frequency is shown in Figure 5.4. In comparison to the one-stage integrator (Section 3.3), the two-stage implementation has an additional pole and zero. The low frequency zero location and Z_{in} value are much lower. Z_{in} can be approximated at lower frequencies as $\approx \frac{1}{gm_1 r_{o1} gm_2} + \frac{1}{GBW\ C_{int1}}$. It is important to design P_2 and P_3 as close as possible to each other and at high frequency to avoid the input impedance peaking effect affecting the system's low-pass corner frequency ($f_{-3dB,LPF}$).

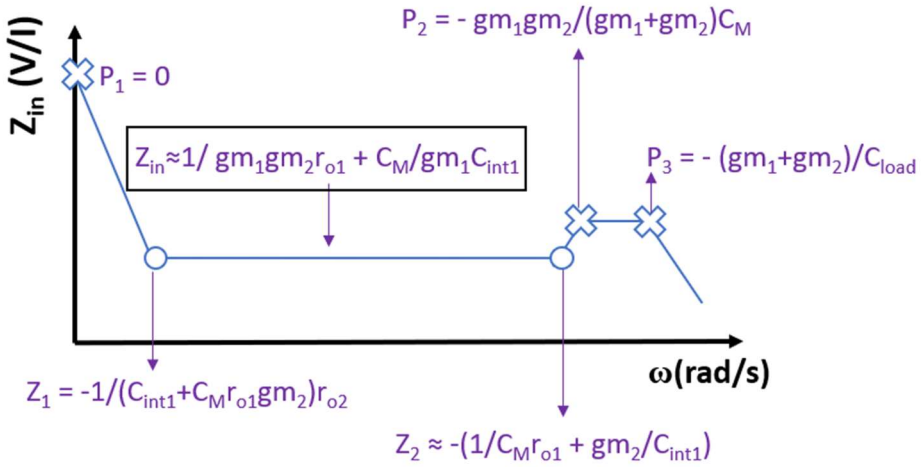


Figure 5.4: Location of poles and zeros for Zin for two-stage integrator.

To test this hypothesis, a two-stage Miller-compensated amplifier was designed. Its first stage is a FC-OTA, while its second stage is a NMOS-based common source (CS) stage as shown in Figure 5.5.

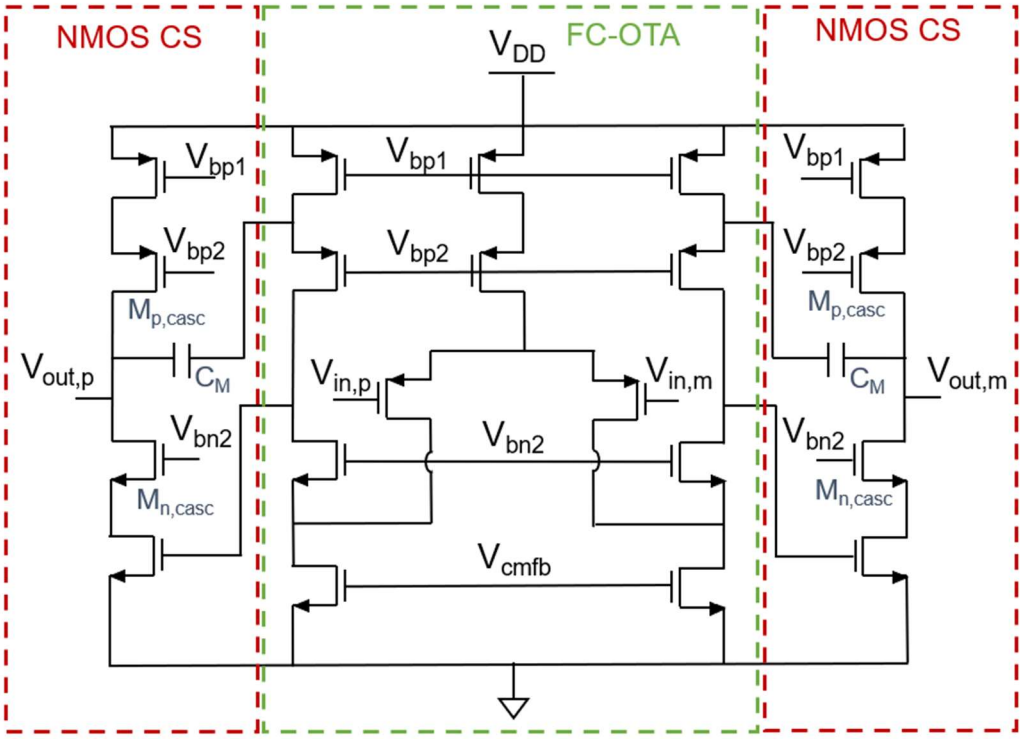


Figure 5.5: Two-stage OTA

The OTA is designed for a *GBW* of 30 MHz with C_M of 1pF. Cascode compensation [27] was chosen to maximize *GBW*. The current used in the FC-OTA + the NMOS CS second stage amounts to around 160uA, required for pushing poles P_2 and P_3 to much higher frequency and to stabilize the OTA.

Figure 5.6 shows the simulated input impedance of 1-stage OTA and 2-stage OTA with and without cascodes ($M_{n,casc}$ and $M_{p,casc}$).

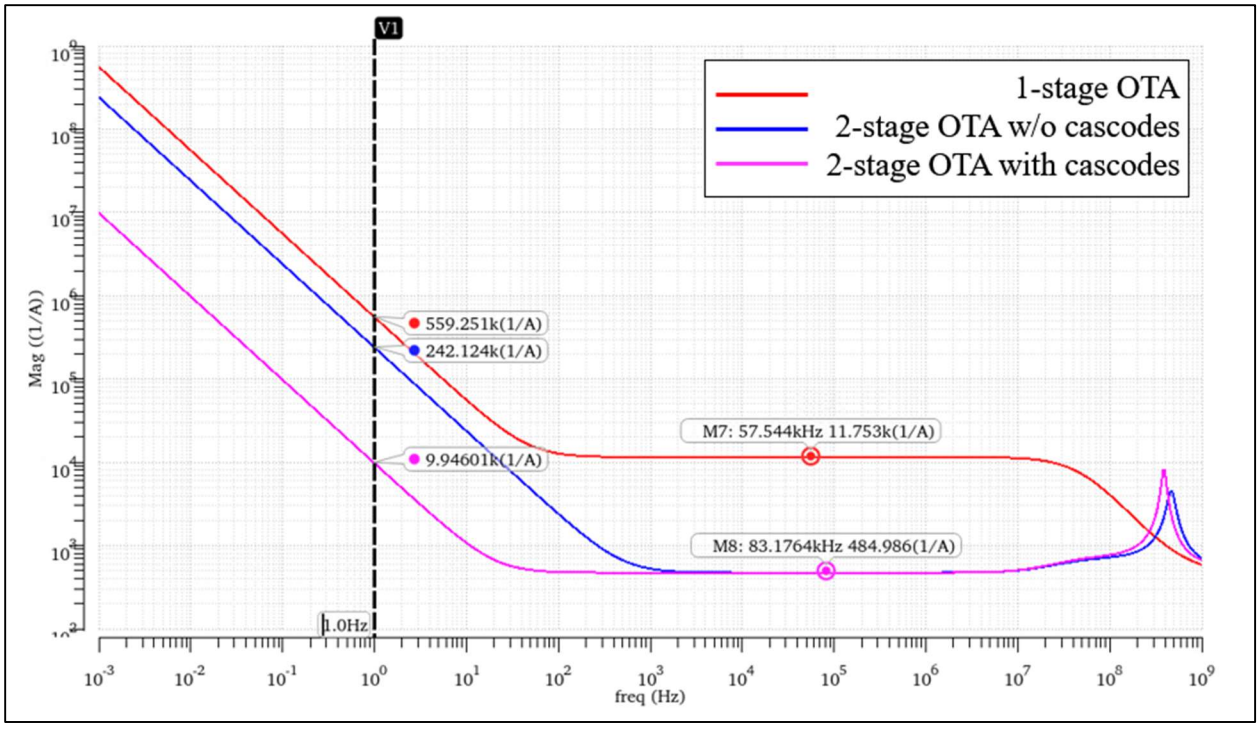


Figure 5.6: Input impedance of 1-stage, 2-stage integrator with and without cascodes.

It is observed that the input impedance (in the flat region) of the two-stage integrator is much smaller than that of a one-stage integrator. The first zero (Z_1) shifts to higher frequencies for the two-stage integrator because of the lowered output impedance ($r_{o1,2} \propto 1/I_{bias}$) due to increased power consumption. This can be mitigated by cascoding the common-source amplifier and the current source ($M_{n,casc}$ and $M_{p,casc}$) used in the second stage, obtaining the pink curve.

Figure 5.7 shows the testbench that was used to plot the low-pass BW of the system. It includes the gm-stage (*gm*), the choppers (CH1 & CH2), and the integrator (A).

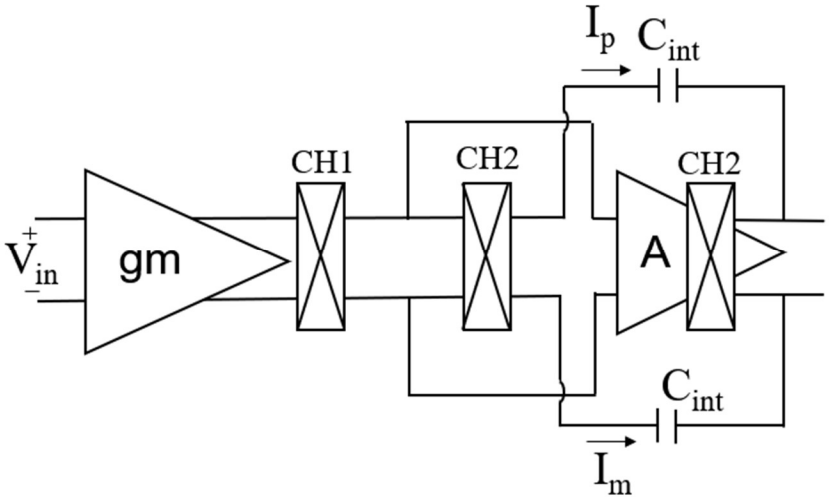


Figure 5.7: AC transfer testbench.

Figure 5.8 shows the voltage-to-current transfer of the system with one-stage (red curve) and the proposed two-stage (blue curve) integrator, with 16x larger switch size. The proposed improvements effectively increase the $f_{-3dB,LPF}$ 21 times, reducing the phase error from 111m°φ to 6m°φ at f_{drive}. The peaking in the blue curve is suspected to be caused by the peaking in the input impedance, as can be seen in Figure 5.6.

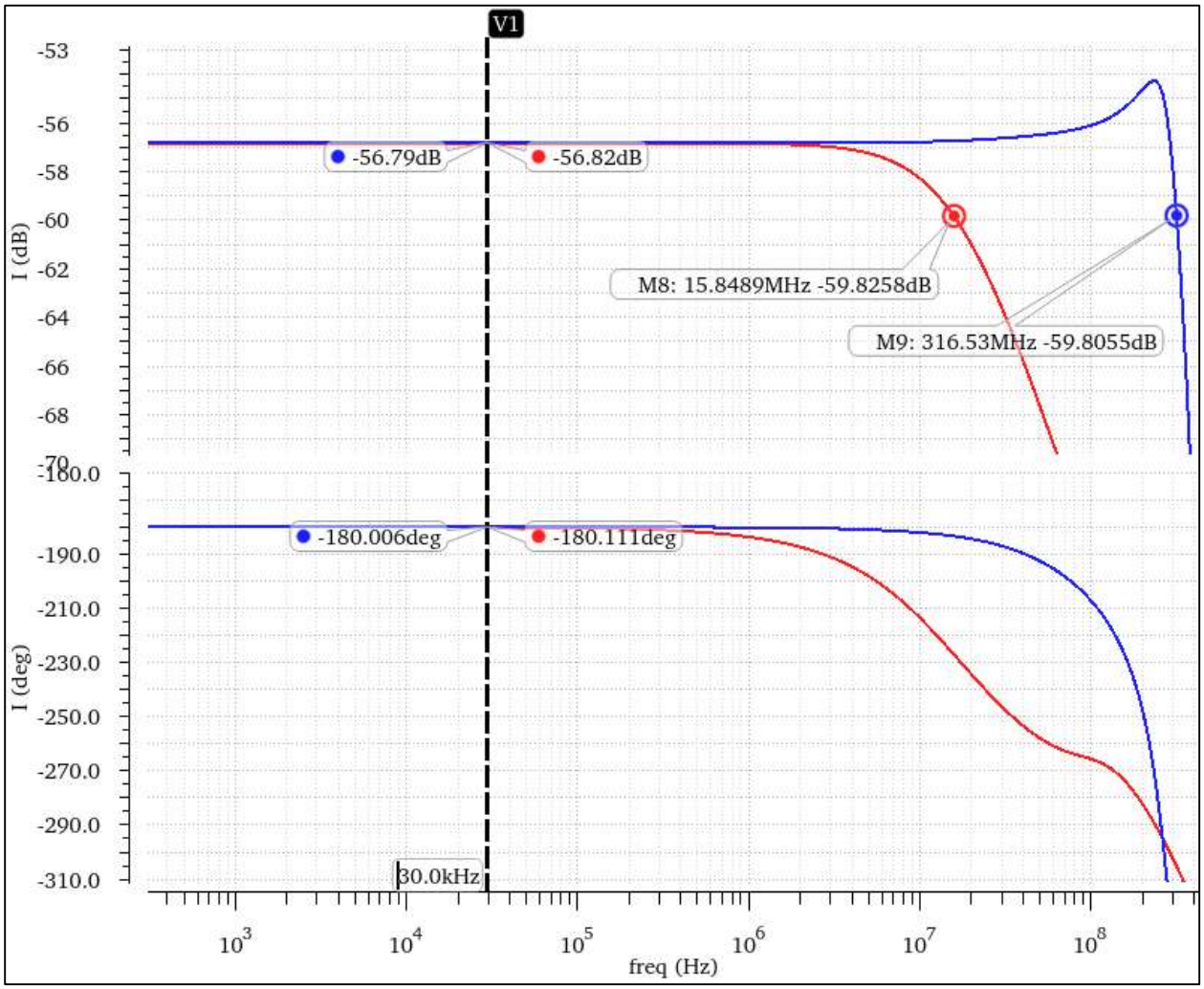


Figure 5.8: V-to-I transfer showing -3dB Bandwidth with original 1-stage (red curve) and proposed 2-stage OTA (blue curve).

5.1.3 Self-heating

As already mentioned in Section 2.3.1, with high P_{heater}, the effect of spread in self-heating can cause a significant temperature error. In this work, each heater dissipates about 3.6 mW. With two TP-ETFs and two ring ETFs, there are 6 heaters on the chip. Table 5.1 presents the power breakdown of the chip.

Table 5.1: Power breakdown

Block	Notation	Supply voltage	Supply current	Power consumption
Analog+Digital	VddA + VddD	1.8V	2.4mA	4.32mW
Bridge bias	VddB	1.8V	1.8mA	3.24mW
Heater	VddH	1.8V	2mA * 6 Heaters	3.6mW * 6 Heaters
I/O supply	VddPST	3.3V	7.2mA	23.76mW

From Table 5.2, the total power consumption of TP-ETF is 7.92mW (=4.32mW+3.6mW), and for ring ETF it is 14.76mW(=4.32mW+3.6mW*2). Due to a design error, all 6 heaters were ON all the time during the measurements. Resulting in the total power burnt in the chip being 25.92mW during TP-ETFs measurements and 29.16mW during ring ETFs measurements. The high power burnt in the chip is suspected to be another cause of the poor inaccuracy of the designed temperature sensor. From Equation 2.3 and Equation 2.4, with a 5% spread in the total power, the estimated $T_{self\text{-}heating}$ is calculated to be 0.07°C.

To observe the effect of self-heating 10 iterations of temperature measurements were performed for S24 TP and ring sensors on 6 samples. The time difference between each iteration is 8 seconds. The result of the measurements is shown in Figures 5.9 and 5.10.

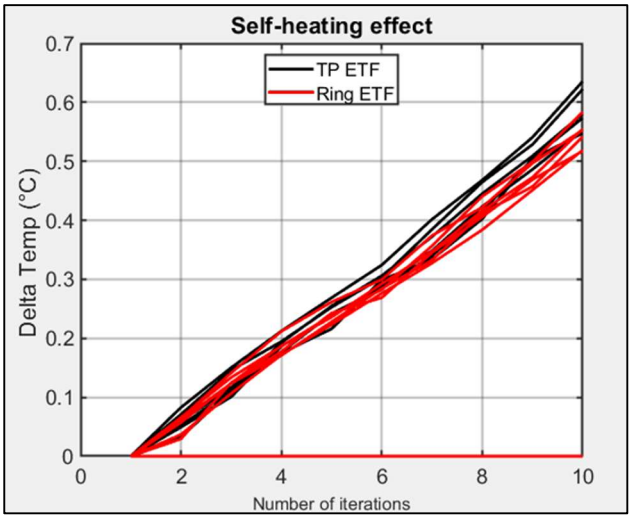


Figure 5.9: Self-heating effect with chips placed outside the oven.

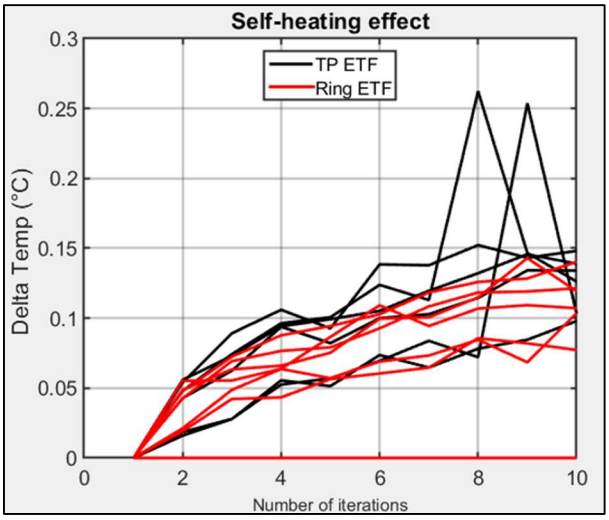


Figure 5.10: Self-heating effect with chips placed inside the oven (controlled temperature).

Figure 5.9 depicts the temperature difference of the test chips versus the number of measurement iterations. This measurement was taken by keeping the chips at room temperature under an uncontrolled temperature environment. Figure 5.10 shows the same measurement when the chips are placed inside the Oven with a controlled temperature environment. For two samples, glitches occur in temperature measurement for the 8^{th} and 9^{th} iterations, despite that, the measurements show a 3σ spread of $T_{self\text{-}heating}$ to be around 0.1°C.

A simple fix in the design, by enabling only the heater of the sensor under test, the error due to the self-heating can be reduced to 0.01°C.

5.2 Conclusions

Despite some design issues, the tape-out validates the functionality of the hybrid offset correction scheme in PD-DSM. All the potential bugs have been identified, and some design modifications are proposed in this work. Theoretically, the inaccuracy of the TD-based sensors must be only limited by the intrinsic electrical BW of the ETF and lithography errors. The proposed design modifications along with the hybrid offset cancellation scheme make it feasible to achieve an untrimmed inaccuracy of 0.2°C or less in temperature range beyond the military range.

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