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Low Temperature Wafer Bonding Based on Copper Nanoparticle Sintering for 3D Interconnect Fabrication

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by

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Contents

Selected List of Abbreviations

AFM	Atomic force microscopy
AP-PAB	Atmospheric pressure-plasma activated bonding
Ar-FAB	Argon fast atom beam
ASH	Average surface height
BCB	Benzocyclobutene
BHF	Buffered hydrofluoric acid
CBKR	Cross-Bridge Kelvin Resistor
CMOS	Complementary metal–oxide–semiconductor
CMP	Chemical-mechanical polishing/planarization
CTE	Coefficient of thermal expansion
DBD	Dielectric barrier discharge
DC	Direct current
DI	Deionized
DRIE	Deep reactive-ion etching
ECD	Electrochemical deposition
FIB	Focused ion beam
HAR	High aspect ratio
HF	High frequency
HMDS	Hexamethyldisilazane
IC	Integrated circuit
IPA	Isopropyl alcohol
ITO	Indium tin oxide
IR	Infrared
LFPD	Local focal plane deviation
LPCVD	Low pressure chemical vapor deposition
LP-PAB	Low pressure-plasma activated bonding
LTV	Local thickness variation
MBE	Molecular beam epitaxy
MEMS	Microelectromechanical systems
MOSFET	Metal–oxide–semiconductor field-effect transistor
NEMS	Nanoelectromechanical systems
NMP	N-methylpyrrolidone
PCB	Printed circuit board
PDMS	Polydimethylsiloxane
PECVD	Plasma-enhanced chemical vapor deposition
PAB	Plasma-activated bonding
PEB	Post-exposure bake
PVD	Physical vapor deposition
RC	Resistor-capacitor
RCA	Radio Corporation of America
RF	Radio frequency
RIE	Reactive ion etching
RMS	Root mean square
SAB	Surface activated bonding
SAC	Tin(Sn)-Silver(Ag)-Copper(Cu)
SAED	Selected area electron diffraction
SEM	Scanning electron microscope
SOG	Silicon on glass
SOI	Silicon on insulator

SOS	Silicon on sapphire
SPAB	Sequential plasma activated bonding
TEM	Transmission electron microscopy
TEOS	Tetraethyl orthosilicate
TGA	Thermal gravimetric analysis
TMAH	Tetramethylammonium hydroxide
TSV	Through-silicon via
TTV	Total thickness variation
UHV	Ultra high vacuum
UV	Ultraviolet
VLSI	Very large scale integration
XRD	X-ray diffraction

List of Figures

List of Tables

1 Introduction

1.1 Motivation

Three-dimensional (3D) integration is a promising technology for reducing power consumption and increasing the signal processing speed of semiconductor devices. The primary drivers for the introduction of 3D integration are the form factor, performance and high volume low cost production. The **form factor** improvements include the reduction of the system dimensions such as volume, weight and footprint. The **performance** is enhanced by the increase in integration density and by the decrease in interconnect length which result in improved transmission speed and lower power consumption. The current research work [1] aims to contribute to these improvements by demonstrating a low temperature wafer bonding technique based on nanocopper sintering for 3D integration applications. Furthermore, the combination of different optimized base technologies such as microelectromechanical systems (MEMS) and complementary metal-oxide-semiconductor (CMOS) can significantly decrease manufacturing costs compared to monolithic integration, leading to **high volume low cost production** [2, 3, 4].

Recently, the advantages of 3D integration have been demonstrated by numerous bonding technologies such as metal-to-metal bonding, oxide-to-oxide bonding and polymer bonding [5]. Metallic contacts realized by wafer and die level bonding find many applications in the integration of MEMS and CMOS devices [6, 7]. High temperature bonding techniques such as direct bonding exhibit excellent bond strength values, but are severely limited by the thermal budget of the application. Existing metal-metal bonding techniques also require a relatively high processing temperatures [8]. Problems associated with high temperature bonding include thermal stress generation, especially for dissimilar materials used in hybrid bonding, and defect generation which degrades the reliability of the devices on the bonded wafers [9]. Therefore, considerable interest is shown in novel processes and materials that achieve a reduction in temperature for wafer bonding techniques for 3D integration.

Copper (Cu) has generated growing interest in the area of very large scale integration (VLSI) interconnection technology as the dominant candidate for the conducting material. The reduced cost of copper compared to those of silver or gold make it a preferable economic alternative as an interconnect material [10]. Its main advantages over aluminum are high electrical conductivity and high electromigration resistance [11, 12]. These characteristics are becoming of vital importance for improving the performance of electronic devices by reducing the resistor-capacitor (RC) delay as the size of VLSI circuits decreases [13, 14] in accordance with Moore's law.

Nano-structured metals are being investigated intensively as an alternative solution for such semiconductor interconnection challenges [15]. Metallic pastes based on nanoparticles offer the distinct advantage of sintering at temperatures significantly lower than the bulk metal melting temperature [16]. The reduction of sintering point with decreasing particle size is attributed to the increased surface area of nanoparticles which provides higher surface energy and reactivity [17].

Nanocopper metallic paste combines the aforementioned advantages by offering a low-temperature processing material compatible with modern IC metallization techniques based on Cu. Furthermore, its lithographical patterning demonstrated in this paper recommends its use in wafer stacking for 3D integration. For these reasons we have investigated and developed a low temperature wafer bonding technique based on metallic nanoparticle sintering.

1.2 Objectives

The current research work on wafer bonding was conducted using a **nanocopper material** trademarked as CuantumFuse® and developed by Dr. Zinn from Lockheed Martin [18]. Due to the novel nature of the nanocopper paste, there was limited information available regarding the nanocopper structure and properties. Since the current work was the first attempt to utilize this nanocopper material for wafer bonding, difficult processing challenges needed to be overcome. Futhermore, novel patterning techniques such as lithographically defined screen printing of nanocopper paste were developed. Therefore, an **exploratory research** approach was adopted by focusing on obtaining preliminary results of wafer bonding and nanocopper interconnect patterning process technologies rather than performing an in-depth study of the underlying physical phenomena. A list of the project objectives is presented below.

- Perform a literature review to determine the current state-of-the-art wafer bonding techniques and quantify the associated challenges relevant for the current work such as achieving metallic bonding at low temperatures.
- Develop a low temperature wafer bonding method and interconnect patterning technique based on nanocopper sintering.
- Characterize, quantify and optimize the quality of the newly developed wafer bonding and interconnect patterning techniques by performing mechanical and electrical measurements on the fabricated devices.

The types of experiments performed within the current research work are illustrated schematically in Fig. 1. A detailed explanation of the thesis structure is provided in section 1.3.

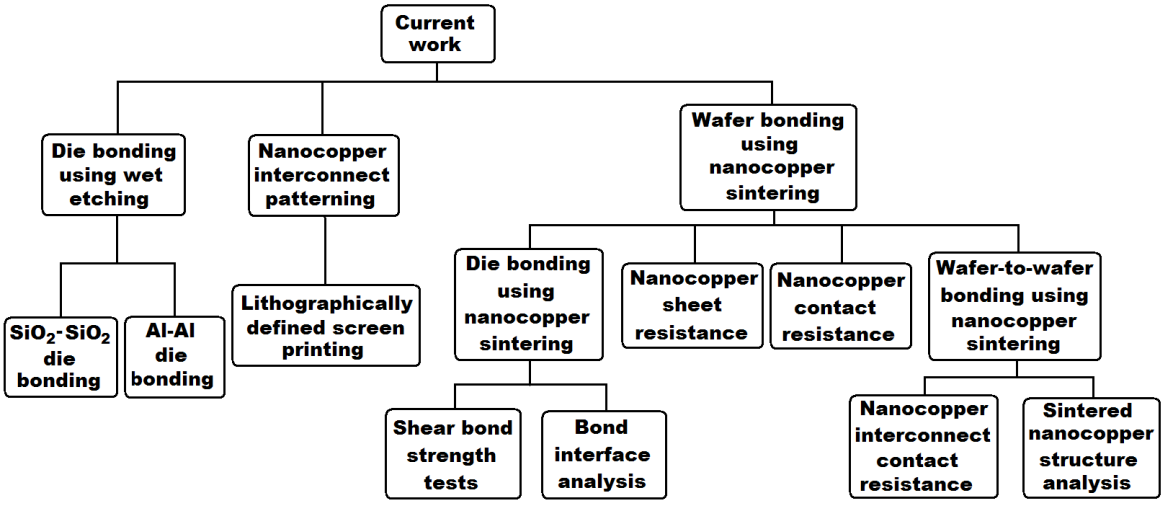

Figure 1: Schematical illustration of the experimental work conducted within the current research project.

1.3 Organisation of the Thesis

The current thesis is organized into 7 chapters. Chapter 1 offers a brief overview of the current research work and presents the project objectives, report structure and the relevant 3D integration challenges . The introductory section 1.1 provides the motivation for the current work by matching the current requirements in 3D integration with advantages offered by the proposed wafer bonding technique based on nanocopper sintering. The chapter continues with a description of the objectives in section 1.2 and is concluded by a brief outline of the thesis report given in section 1.3.

Chapter 2 provides the theoretical background based on a literature review of state-of-the art wafer bonding techniques, surface interactions, wafer specifications and bond characterization methods. The first section 2.1 focuses on identifying challenges associated with low temperature wafer bonding techniques applicable to the current research work. The surface preparation and wafer parameters relevant for this project are presented in section 2.2. Section 2.3 offers a brief explanation of the theory behind the characterization methods utilized to measure the mechanical and electrical parameters of the interconnect structures fabricated using nanocopper sintering.

Chapter 3 presents the first experiment on die bonding based on surface activation using wet etching. The first section 3.1 describes the sample preparation and mechanical characterization based on die shear tests of silicon dioxide dies bonded using hydrofluoric acid (HF) etching. Section 3.2 gives an insight into the sample fabrication and characterization procedure based on bond strength and electrical measurements of dies bonded using partial etching of aluminum. The conclusions 3.3 provides an overview and evaluation of the obtained results and discusses possible improvements for future work.

Chapter 4 describes the development, fabrication and characterization of the nanocopper interconnect patterning using lithographically defined screen printing. Section 4.1 contains an explanation of the sample fabrication procedure. The screen printing process is presented in section 4.2 with focus on the challenges encountered and the solutions found to optimize the nanocopper screen printing process quality. The photoresist lift-off process employed to pattern the screen printed nanocopper is described in section 4.3. The measurements and results are presented and analyzed in section 4.4. The concluding section 4.5 offers a summary of the results, provides explanations for the observed effects and gives an outlook for future improvements and applications.

Chapter 5 describes the main experiment of this research project focused on the development of a wafer bonding technique for metallic 3D interconnect fabrication using nanocopper sintering. The investigation of fused nanocopper sheet resistance is presented in section 5.1. It includes the sample fabrication procedure, the description of the nanocopper fusing process parameters and finally the sheet resistance measurements with conclusions and explanations based on the obtained results. Section 5.2 describes the nanocopper-to-bulk Cu contact resistance experiment. After the sample fabrication procedure is explained, the details of the nanocopper fusing process are given, followed by the description of the contact resistance measurements. The fabrication procedure details are presented and possible optimizations of the technique utilized are discussed. The results are presented and analyzed, followed by explanations of the observed phenomena and conclusions. Section 5.3 describes the in-situ nanocopper fusing measurements. The sample fabrication of the nanocopper structures on a PCB are described along with the experimental setup and fusing parameters. The results are presented and conclusions are drawn based on the result analysis and observed nanocopper fusing effects. The transmission electron microscope (TEM) analysis of the nanocopper material is presented in section 5.4. Important results regarding the nanocopper particle structure are gathered and analyzed. The mass loss ratio variation with temperature is investigated using thermal gravimetric analysis (TGA) in section 5.5. The nanocopper fusing temperature point is estimated based on the TGA results. Section 5.6 describes the die-to-die bonding experiment using nanocopper sintering.

After explaining the sample fabrication procedure, the die bonding parameters are given, followed by the qualitative measurements of the contact resistance. Scanning electron microscope (SEM) imaging of ion-milled cavities is employed to analyze the structure of the sintered nanocopper-bulk Cu interface. The porosity and changes in the nanocopper layer after the sintering process are measured. Die shear tests are utilized for evaluating the bond strength of dies bonded using nanocopper. The results are summarized and valuable conclusions are drawn based on the results analyzed. Section 5.7 describes the final experiment on wafer-to-wafer bonding using nanocopper sintering. The important data and conclusions gathered from the previous experiments are employed to optimize the wafer bonding process. After describing the sample preparation procedure, the bonding process is explained. Further sample processing details are given including top wafer removal for access to the test structure for electrical measurements. The contact resistance measurements are described and the results are discussed with explanations found for the observed effects. The sintered nanocopper structure and bond interfaces are analyzed based on SEM imaging. Using these results, modifications to the nanocopper internal structure during the sintering process are correlated with the mechanical and electrical properties of the fabricated interconnects. Finally, the results from the entire chapter are summarized and conclusions are established based on the observed effects. Possible improvements for optimizing the nanocopper interconnect fabrication and bonding process are provided.

Chapter 6 gives a brief outline of the current thesis starting from the theoretical background and ending with recommendations for future work. The most important results obtained from the experiments conducted on interconnect fabrication and wafer bonding using nanocopper sintering are presented. The effects observed during the fabrication and characterization steps are summarized and explained, with focus on process optimization. Possible improvements to the developed nanocopper patterning and wafer bonding techniques are discussed by giving an outlook for future research work.

The appendix chapter 7 provides extra theoretical background information on wafer bonding techniques, surface preparation procedures and wafer parameters.

2 Theoretical Background

2.1 Wafer-to-wafer bonding

Wafer bonding is a key packaging technology for 3D integration by which two semiconductor wafers are joined. Currently, wafer bonding finds many applications in the micro- and optoelectronics industries. Among these, the most prominent uses are substrate fabrication for modern integrated circuits (IC) such as Silicon on insulator (SOI), Silicon on glass (SOG) and Silicon on sapphire (SOS), 3D stacking of processsed layers and encapsulation of MEMS and nanoelectromechanical (NEMS) systems.

Wafer bonding techniques can be classified into **(a)** methods without an intermediate layer such as fusion and anodic bonding and **(b)** methods with intermediate layers such as adhesive bonding based on polymers as is illustrated schematically in Fig. 2. Generally, each method has its advantages and drawbacks. Direct or fusion bonding typically requires special wafer surface conditions and preparations. The utilization of an intermediate layer overcomes this challenge at the expense of issues with instability, bond strength and the hermetic seal of the bond interface. Further differentiation can be made based on the processing temperature. The use of high temperature annealing can result in high bond strength as is the case for fusion bonding. However, this severely restricts the application range. Therefore, there is a significant interest in researching techniques for reducing the processing temperature in wafer bonding.

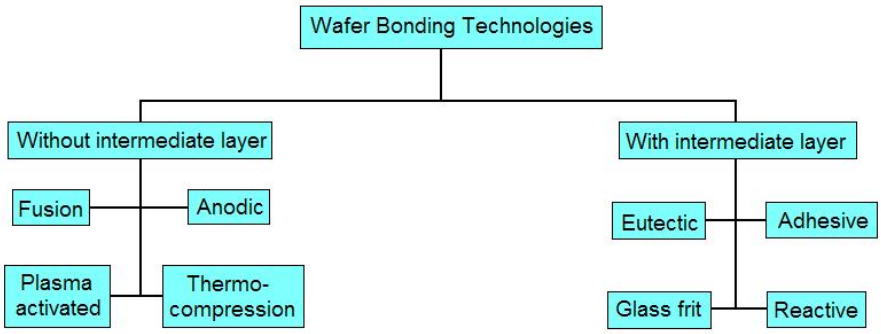

Figure 2: Wafer bonding classification

The thermocompression and eutectic bonding techniques are of particular importance for the current developed method based on nanocopper sintering. The diffusion of metal atoms examined within subsection 2.1.1 is relevant for gaining valuable insight into metallic bonding applicable to the current method. Furthermore, the metal-metal interface formation during eutectic bonding in subsection 2.1.2 offers important information for the nanocopper-bulk Cu bonding developed in the current work. Therefore, the current chapter focuses on the 2 aforementioned wafer bonding methods, with fusion bonding, adhesive bonding and the other techniques being presented in the appendix chapter 7.

2.1.1 Thermocompression Bonding

Thermocompression bonding is a technique based on the diffusion of metals using heat and pressure to achieve wafer bonding. It is also referred to as diffusion bonding, thermocompression welding, solid-state welding or pressure joining. The most commonly used metals are gold, copper and aluminum

(Al) due to their high diffusion rates and ductile properties [19]. The diffusion process of metal atoms is based on lattice vibration [8] and is classified into:

- Surface diffusion
- Grain boundary diffusion
- Bulk diffusion

Surface diffusion, also named atomic diffusion, is the process describing the movement of atoms from surface to surface in order to free energy. The diffusion rate is influenced by the bonding conditions, mostly by the process temperature and applied pressure. Surface diffusion is the most rapid diffusion process, although grain boundary and bulk diffusion also play important roles [20]. The grain boundary diffusion is based on the free migration of metal atoms in free atomic lattice locations. This process occurs in polycrystalline layers and is based on the movements of atoms along the boundaries of atomic lattice mismatches and grains. Bulk diffusion is based on the movement of atoms within the lattice by exchanging locations with vacancies. The bulk diffusion rate increases exponentially with temperature and starts to play a significant role above half of the melting point of the material [8].

Surface topography variations must be reduced as much as possible in order to provide an intimate contact between the two metallic surfaces. A CMP process is employed to bring the surface roughness value below 1 nm root mean square (RMS) [9]. Organic contaminants can be removed by UV-ozone exposure [21], wet etching or ion bombardment [9]. Plasma treatment of the metal surface can be used to increase the diffusion rates and improve the bonding quality [8].

Typical metal deposition techniques include sputtering, evaporation and electroplating. The slow deposition rate of sputtering and evaporation limits the thickness of the metal layer to a few micrometers. For thicker layers, electroplating is the method of choice. However, electroplating usually results in layers with higher amounts of impurities and increased surface roughness. Diffusion barrier layers consisting of silicon nitride or dioxide are used. Additional layers for protection against diffusion and enhacing adhesion are deposited using titanium (Ti), nickel (Ni), titanium nitride (TiN) or tantalum (Ta) [22].

During the bonding process, the two wafers are brought into contact and a high force is applied, acting to reduce the warp and bow in the wafer. The pressure needs to be sufficient to produce plastic deformation of the non-uniformitites in the metal layer. Furthermore, the uniformity of the applied force is essential to ensure that the two metal surfaces are brought within atomic contact. Also, by increasing the uniformity of the applied force, the applied pressure can be lowered, which reduces the risk of damaging the structures on the wafer surface. When applying a higher pressure, the processing temperature can be reduced, which allows for some flexibily in the bonding conditions [22]. In order to avoid oxidation of the metal layer, the bonding process is performed under an inert atmosphere such as nitrogen or under vacuum. Gases which prevent oxidation like formic acid vapor or which reduce the metal oxides such as forming gas (hydrogen and nitrogen mixture) are used inside the bonding chamber. The inert gases also prevent the rise of thermal gradients across the wafers by improving heat conduction. CTE mismatch control is crucial for proper aligning right before bonding. A Cu-Cu connection realized using thermocompression bonding is shown in Fig. 3.

Typical conditions used for thermocompression bonding are 400-450 ℃ for Al-Al, 260-450 ℃ for Au-Au and 380-450 ℃ for Cu-Cu at bonding pressures in the range of 30-120 MPa. [22] Lowering the process temperature has attracted significant interest recently and room temperature bonding using surface activated bonding (SAB) has been reported by Taniyama et al. [9]. This technique enables the bonding of Si-Si/Au-Au/Cu-Cu wafers using a low-energy ion beam to provide surface activation followed by bonding under vacuum. An argon fast atom beam (Ar-FAB) is used for etching the metal

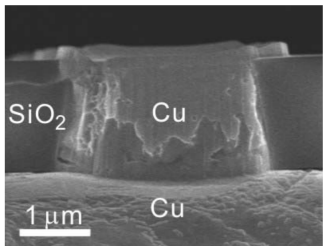

Figure 3: SEM image of a Cu interconnect bonded by thermocompression to a Cu pad showing a high quality Cu-Cu bond interface [23].

surface and remove surface contaminants and any metal oxides. A force in the range of 100-1000 kgf is applied to the wafer pair under a pressure of 10^{-5} Pa. Succesful bonding is achieved, with bond strength values extracted from tensile tests of 16 MPa for Si-Si and 12.4 MPa in the case of Au-Au [9].

Cu-Cu bonding using SAB at room tempearature has been reported by Kim et al. [24]. Using an ultra high vacuum (UHV) environment and a low energy (40-100 eV) Ar ion bombardment, Cu-Cu wafers were successfuly bonded at room temperature. A bond strength in excess of 6.47 MPa was measured using tensile tests. Atomic force microscopy (AFM) meausurements revealed that the surface roughness was kept below 2 nm RMS. No increase in surface roughness was observed after surface activation using ion beam etching. The bond interface was inspected using transmission electron microscopy (TEM), showing a good atomic contact, without any visible voids, as illustrated in Fig. 4.

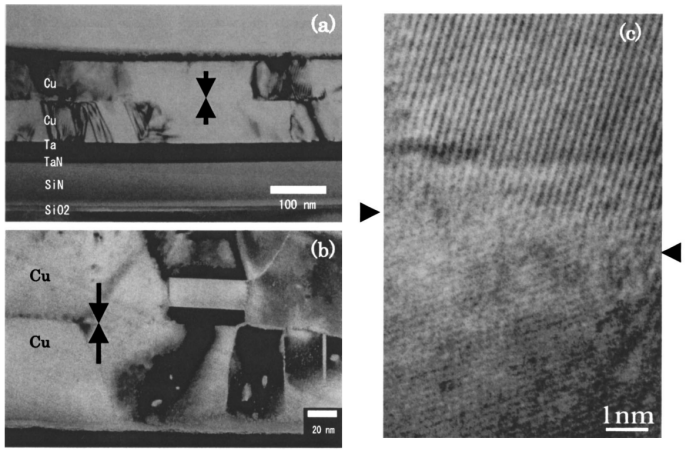

Figure 4: TEM image of bonded Cu-Cu interface: (a) low magnification, (b) high-resolution and (c) magnified high resolution showing bonded lattice structure at the interface [24].

Surface preparation is crucial for successful thermocompression bonding. Atomic contact between the two metallic surfaces is required for the diffusion process to occur. Furthermore, impurities and oxidation can significantly disturb the bonding process by reducing the diffusion rates. Oxidation is a particularly challenging issue for Cu-Cu bonding. Consequently, the removal of oxide layer and impurities as well as preventing re-oxidation are needed. Aluminum and copper oxides can be removed by wet or dry etching. A solution of hydrochloric acid (HCl) is commonly used to remove copper oxides before bonding [25]. Formic acid (CH_2O_2) vapor cleaning is a dry etching process which can also be

used during the bonding process to prevent re-oxidation of the copper surface. The cuprous oxide (Cu_2O) reduction mechanism by formic acid is presented in Eq. 1 [26].

$$Cu_2O + CH_2O_2(g) \rightarrow 2Cu + H_2O(g) + CO_2(g) \quad (1)$$

Dry etching avoids immersion in fluids, reducing the etching of underlying passivation and dieletric layers [8]. This is very important, as even traces of oxygen can result in copper oxidation at temperatures above 200 ℃. The effect of formic acid vapor cleaning is illustrated in Fig. 5. Copper oxidation is avoided even under thermal cycling to 400 ℃ for 20 min when formic acid treatment is used. This shows that Cu-Cu surface diffusion can be significantly improved using surface treatments such as formic acid vapour.

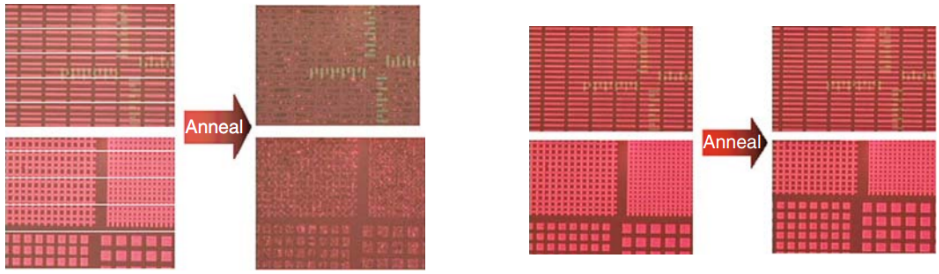

Figure 5: Cu films annealed at 400 ℃ in vaccum: **(a)** unpassivated and **(b)** cleaned and passivated with formic acid vapour [8].

Thermocompression Cu-Cu bonding is currently used together with CMOS processes for the fabrication of vertical ICs and MEMS devices, gyroscopes and pressure sensors [21]. Companies such as IBM and Intel have adopted this technique to reduce interconnect length in 3D ICs for processor-on-processor and memory-on-processor chips using Cu bonding together with Through-Silicon Via (TSV) technology. Currently, the most popular method in industry is thermocompression at temperatures in the range on 300-400 ℃ due to its simplicity and lower costs [8].

2.1.2 Eutectic Bonding

Eutectic bonding decribes a wafer bonding technique based on eutectic metals. Such materials posses the distinct property of passing from a solid to a liquid state at a particular temperature and composition without going through a two-phase equilibrium. These specific temperature and composition values constitute the eutectic point of the alloy. The main advantage of this technique is that the eutectic temperature of the metal allloy is much lower than the melting temperature of one or both of the constituent metals in their pure state.

The metal mixture known as the eutectic alloy can be deposited by dual source evaporation, electroplating or sputtering. Alternatively, the alloy can be produced through diffusion reactions of pure metals followed by melting the eutectic mixture [20]. Other advantages of eutectic bonding include relatively low processing temperatures, hermetically sealed packages, high bond strength, good reliability and low resultant stress in the bonded wafer pair. Control of important parameters such as applied pressure, bonding pressure and time are essential for successful eutectic bonding [27].

Eutectic bonding based on Au-Si alloy has attracted considerable interest in applications such as the fabrication of pressure sensors and fluidics. It offers the advantages of high bond strength and

low processing temperature [27]. The variation of melting temperature with alloy composition and temperature for Au-Si is illustrated by the phase diagram in Fig. 6. The eutectic temperature of Au-Si is only 363 ℃, much lower than the melting points of Au (1064 ℃) and Si (1414 ℃). This eutectic point recquires an alloy composition of 19 at.% Si and 81 at.% Au [28]. At this concentration, the alloy will be in a liquid state while the temperature is above the eutectic value (363 ℃). When the temperature is reduced or the concentration ratio decreases below the liquid line, the composition will solidify. While the Au and Si layers are in atomic contact, the atomic diffusion is increasing with temperature. This diffusion leads to the formation of an Au-Si alloy at the bond interface. As the composition of this mixture reaches the Au and Si concentrations corresponding to the eutectic point, the alloy passes from a solid to a liquid phase, which accelerates the diffusion process [29].

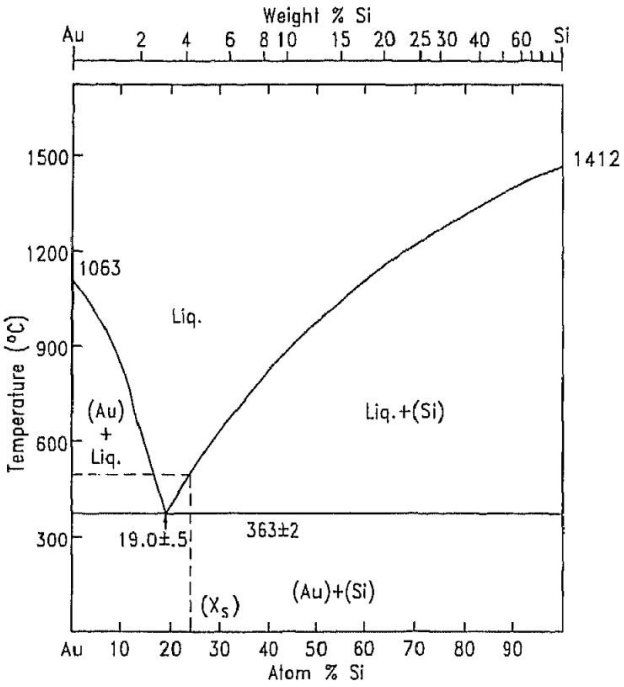

Figure 6: Au-Si phase diagram [28].

As the wafers cool down below the Au-Si eutectic temperature, the resulting solidification causes epitaxial growth in both the gold and silicon layers on the substrate wafer. This leads to the formation of silicon islands in a polysilicon gold layer, as illustrated in Fig. 7 [30]. Below the eutectic point, gold diffuses into silicon and not vice versa, causing the formation of gold silicide ($SiAu_3$). Thus, annealing should be done at a temperature above the eutectic point in order to prevent gold contamination by diffusion into the silicon substrate and degrade the performance of the active devices [30].

The use of Au-Si material is widespread in die-level bonding due to its advantages such as low eutectic temperature [31]. However, there are several challenges with obtaining reproducible practical results [30, 32]. The reliability of the bond obtained through Au-Si eutectic bonding is limited by the oxide present on the processes silicon wafer. The relatively poor wettability of gold on silicon oxide leads to adhesion problems. Several methods to circumvent this challenge have been developed. During die-to-wafer bonding, the silicon die can be rubbed in order to break the oxide layer. However, this can lead to the destruction of delicate microstructures for micromachined wafers. Removal of the silicon oxide before bonding can be done by wet etching in an HF-solution, but a thin native oxide

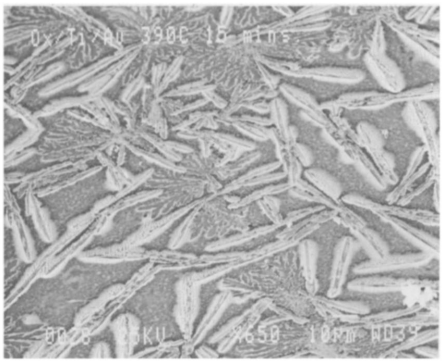

Figure 7: Structure of AuSi eutectic material after heating up to 390 ℃. [30]

layer will be formed again when the wafer is exposed to air. Therefore, an argon sputter clean under vacuum followed by an in situ gold sputter deposition are needed to obtain sufficiently high gold to silicon adhesion strength. This improved adhesion comes at the cost of expensive equipment and more complex processing steps [28]. This method is generally used in advanced die-bonding processes and is presented schematically in Fig. 8 [33]. Once the back side of the wafer is treated to remove the oxide and cleaned using sputtering, the gold layer is deposited by in sity sputerring. During heating to eutectic temperature, an alloy of Au-Si is produced. This is followed by an Au-coating of the package substrate with a die-attachement Au-plated preformed placed on top. The presence of the Au-Si alloy at the interface between the gold coating and silicon die back side ensures the formation of a good quality eutectic die bonding. Several reliability challenges remain, such as bond cracking caused by CTE mismatch, which are the focus of research in this field [33].

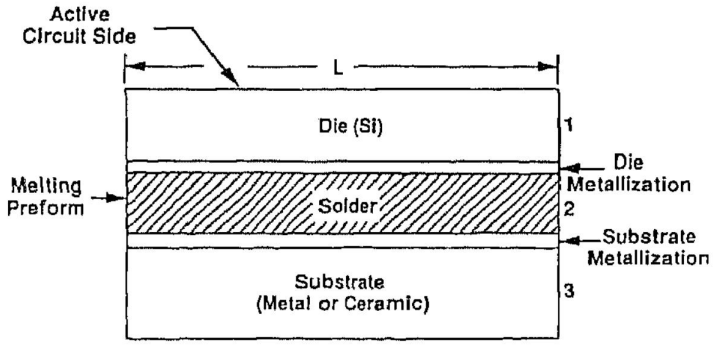

Figure 8: Structure used for die bonding. [33]

Another method consists of depositing a thin intermediate metal film which provides good adhesion to silicon oxide, followed by gold deposition on top of the intermediate layer. Candidate metals for the intermediate layer are titanium (Ti) and chromium (Cr) used in a $Si/SiO_2/Ti/Au$ stack or a $Si/SiO_2/Cr/Au$ stack [28]. Aluminium is used extensively as an interconnect material and has a good adhesion to silicon oxide. However, the silicides formed at the interface between Au and Al are known to be brittle and poorly conducting. Therefore, aluminium is not used for intermediate metal layer. Furthermore, Ti and Cr act as diffusion barriers, making them ideal for the intermediate material. Successful eutectic bonding using the Au-Ti-Si system has been reported by R.F. Wolffenbuttel [33]. These results come at the cost of a higher process temperature (520 ℃ compared to 363 ℃ for Au-Si), which is necessary to achieve a uniform and reliable bond. Additionally, silicide grain formation in the gold layer was observed, with $TiSi_2/CrSi_2$ grains replacing the silicon grains in eutectic AuSi bonding.

Table 1: Eutectic alloys commonly used in wafer level bonding [34, 35, 36].

Eutectic Alloy	Eutectic Temperature [℃]	Eutectic Composition [wt%]
Cu-Sn	231	5/95
Au-Sn	280	80/20
Au-In	156	0.6/99.4
Au-Ge	361	28/72
Au-Si	363	97.1/2.9
Al-Ge	419	49/51

The low solubility of Si in Ti/Cr prevents the diffusion on Si through the Ti/Cr layer and reaching the Au layer to form an eutectic AuSi composition. The process is further hindered by the silicidation of the Ti/Cr layer. During the silicidation process, the diffusion of silicon into titanium causes the oxide to break, resulting in oxygen atoms present at the interface. This is different from the clean silicon lattice in the case of pure Au-Si bonding. The relatively high temperature (520 ℃) causes the diffusion of silicon atoms from the substrate. This leads to dangling bond formation, allowing for the diffusion of oxygen atoms in the silicon substrate. The excess oxygen atoms migrate through the lattice, making the surface unsuitable for the formation of silicon columns through epitaxial growth [33].

Bonding in a nitrogen ambient helps to reduce the oxidation of silicon atoms diffusing through the gold layer, resulting in better bond quality. The high temperature (520 ℃) is needed for silicidation to occur, which is believed to be required in order to reach the Au-Si eutectic composition. The eutectic bonding is therefore initiated by the silicidation breaking the oxide layer, as described previously. However, more research is needed to provide conclusive evidence for this theory [33].

Eutectic bonding can be achieved by depositing the metal alloys as compound layers on different wafers, which are then aligned and brought into contact. By heating the wafers above the eutectic temperature, the metal alloy melts and re-solidifies during the subsequent cooling step, providing a bond interface. This method offers the advantage of faster processing and avoidance of the diffusion step. Alternatively, pure metals can be deposited separately on the wafers, followed by bonding under applied pressure and heating. When the eutectic temperature is reached, the two metals mix via diffusion to produce a solid solution interface. The limited solid solubility causes grain boundary reaction to play a significant part in this process, affecting the quality of the bonding process. Once the metal mixture via diffusion occurs, the wafers are heated above the eutectic point followed by re-solidification during the cooling step. Selecting the eutectic alloy type depends on the intended application and is often determined by the processing temperature and material compatability. The most commonly employed metals are gold, copper and aluminium, as proven by their extensive use in modern semiconductor processes [34]. Their alloys used for eutectic wafer bonding are listed in Table 1.

2.2 Surface Preparation and Prerequisites for Direct Wafer Bonding

Direct wafer bonding relies on contacting the two substrates at room temperature as the first step to achieve a reliable bond. In the absence of an applied electrical field or an adhesive intermediate layer, the adhesion between the wafers is determined by surface interactions occuring and the interface. Therefore, understanding the nature of these forces and interactions is the key to achieving a reliable bonding process. Furthermore, factors such as wafer flatness and surface roughness play important roles in determining the quality of the contact between the substrates. Finally, surface preparation such as the removal of particle contamination is essential to ensure a high quality bond is achieved [37].

A detailed explanation of surface interactions and the forces governing them is provided in the appendix section 7.6.

2.2.1 Wafer specifications

Wafer parameters such as flatness, thickness variation and surface roughness play important roles during the wafer bonding process. The success of the bonding procedure relies on the atomic contact between the two wafer sufaces. Therefore, a proper understanding and control of these wafer parameters are crucial for achieving reliable wafer-to-wafer bonds.

The flatness of semiconductor wafers can greatly influence the bonding process. One important flatness specification is the total thickness variation (TTV), defined as the difference between the minimum and maximum wafer thickness values, as illustrated in Fig. 9 [38].

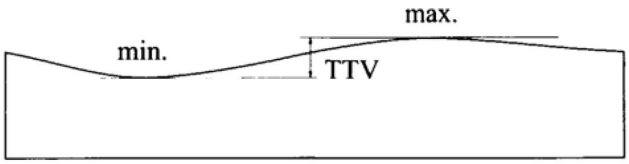

Figure 9: Wafer total thickness variation (TTV) [38].

The warp is measured as the sum of the maximum deivations (positive and negative) from the best fit plane on an unclamped wafer. The bow is defined as the distance from the unclamped wafer surface to the best fit plane at the wafer's center, as illustrated in Fig. 10 [38]. The warp and bow values are independent of the TTV. External force needs to be applied during the bonding process to prevent air from being trapped in gaps at the interface caused by large bow and warp values.

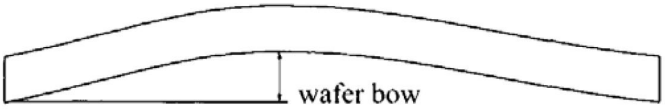

Figure 10: Schematic of wafer bow [38].

In contrast to the TTV and warp, which are defined on the global scale, other parameters are relevant over local areas. The local focal plane deviation (LFPD) is defined as the maximum distance between the unclampled wafer surface and the best fit plane for a specified area. The local thickness variation (LTV) is measured as the difference between the minimum and maximum thickness values for an unclamped wafer. All these wafer specifications contribute to the quality of the bonding process. For example, large TTV values can result in the formation of gaps at the bond interface, causing unbonded areas proportional to the values of thickness variations [38, 39].

For an interface gap of height h and lateral extension R between two standard silicon wafers with a thickness t_w and a specific interfce energy γ of 100 mJ/m^2, the influence of these parameters on whether the gap can be closed or not is depicted in Fig. 11 [39].

In practice, successful bonding at room temperature can be achieved as long as the wafer TTV value is kept within the 1-3 µm range. Bow and warpage tolerances are higher, with values up to 25 µm posing no significant obstacles for wafer bonding.

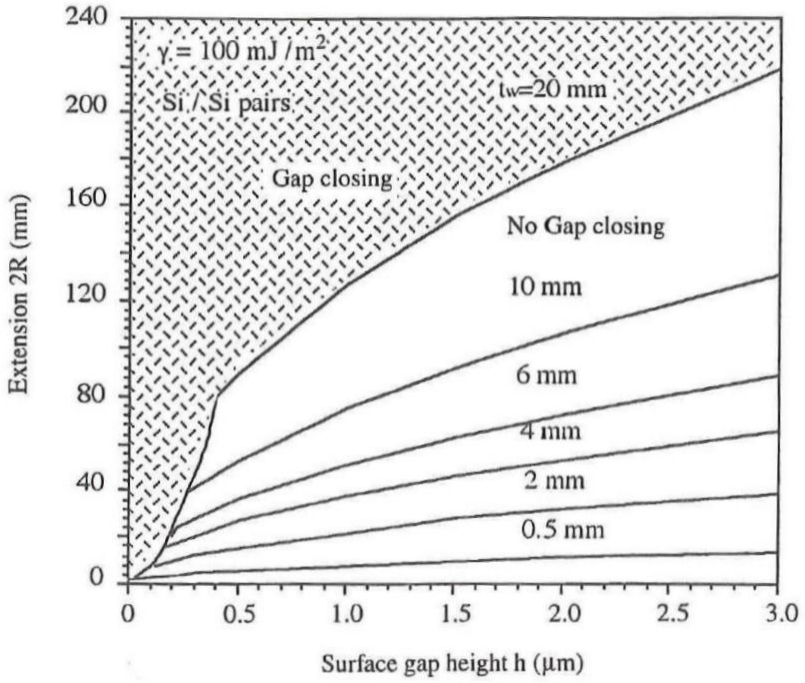

Figure 11: Influence of gap height h and lateral extensions R on silicon wafer interface gaps. The shaded area indicates gaps which can be closed [39].

Surface roughness is another limiting factor for wafer bonding quality. Roughness is defined as a local microscopic parameter characterizing the deviation from the average surface level over very small areas. It is typically indicated by the root mean square (RMS) value. As the roughness increaes, the contact area between the two wafers decreases. Above a certain roughness value, no bonding can be achieved, due to large gaps caused by surface asperities. Therefore, obtaining a smooth wafer surface is crucial for the success of the bonding process. Using modern CMP processes, the RMS surface roughness of silicon wafers can be kept below 1 nm [40].

2.2.2 Cleaning procedures

Contaminations can severely affect the quality of the wafer bonding process. Therefore, a careful cleaning procedure has to be employed to ensure that surfaces are virtually free of contaminants before bonding.

Factors contributing to contamination during wafer bonding can be classified into: particle contamination, organic contamination and ionic contamination. Particles hinder the bonding process by acting as spacers between the two surfaces. Thus, they inhibit the interaction between the opposing surface species present on the two wafers. For standard 4-inch silicon wafers, a 1 µm particle can debond an area of several cm^2[41]. Therefore, the removal of particles is of the utmost importance to ensure that a successful bond is obtained. Performing the bonding procedure in a controlled cleanroom environment greatly helps to reduce particle contamination.

Organic contaminants generally do not affect the surface roughness because they are only present as a very thin film or even single molecules on the wafer surface. Therefore, such contaminants are unable to act as spacers and do not result in significant unbonded areas at room temperature. However, they can result in adhesion problems since the organic film adheres poorly to the wafer substrate. Furthermore, during high temperature annealing, such contaminants can cause nucleation of interface bubbles, which lead to large unbonded areas. Metallic ion contaminants do not affect the bonding interface at room temperature or during annealing. However, difussion of metals such as Cu, Fe or Au during the annealing step can be harmful to the electronic properties of semiconductor devices [41].

Surface cleaning is very important to achieve a successful wafer bonding. The commonly used wafer cleaning techniques in the semiconductor industry are hydrogen-peroxide-based "RCA" wet cleaning steps. This procedure consists of sequentially using two chemical solutions known as RCA1 (or Standard Clean-1) and RCA2 (or Standard Clean-2). The organic contaminant which are insoluble in water can attach to the wafer surface, rendering it hydrophobic, which prevents the removal of metal contaminants. Thus, the organic contaminants are removed first during the RCA1 step. The RCA1 is a 1:1:5 volumetric solution of NH_4OH, H_2O_2 and H_2O heated at 75-85 ℃. The organic contaminants are removed by dissolving in NH_4OH and by the oxidizing action of H_2O_2. Some metals such as Cu, Ag and Ni can also be removed by the RCA1 solution. The particles are attached to the surface by the action of adhesive forces such as van der Waals forces and capillary forces. In order to enhance the removal of insoluble particles, megasonic acoustic cleaning can be employed together with the RCA1 solution [40].

After a thorough rinse in deionized (DI) water up to 18 MΩ×cm, the wafers are dried. The thin native oxide formed during drying, which can act as a contaminant trap for metallic ions, is removed in a 1:50 solution of HF and H_2O at 25 ℃. Heavy metal and alkali contaminants such as Al, Fe, Mg, Cu and Au are removed using the RCA2 solution, which is a 1:1:6 volumetric mixture of HCl, H_2O_2 and H_2O heated at 75-85 ℃. The reaction forms soluble alkali and metal salts, preventing redeposition. A final rinse step followed by Marangoni drying ensures a clean surface free of native oxide [40].

One disadvantage of the RCA1 step is the microroughening of the substrate surface. The RMS roughness can increase from 1 Å up to 5 Å after the RCA1 due to the chemical etching of the native oxide by the NH_4OH. This effect can be significantly reduced by decreasing the NH_4OH mixing ratio from 1 to 0.05. This comes at the price of greatly reduced efficiency of particle removal. A relatively good compromise between the microroughening effect and particle removal efficiency is to use a NH_4OH mixing ratio of 0.25. Alternative cleaning solutions are based on sulfuric and hydrofluoric acids. These solutions eliminate the surface roughening issue. However, their use is relatively hazardous due to the concentrated sulphuric acid. Such techniques are common in applications where native oxide removal is crucial such as replacement of epitaxial growth [40].

After native oxide removal in HCl, some fluorine and hydrogen atoms can remain present on the wafer surface, even after annealing at high temperatures. The presence of these atoms can lead to the formation of electron traps and defects at the bonding interface. This is especially important for interfaces related to active device areas with a need for long carrier lifetimes. The removal of such foreign species from the surface can be accomplished using excited or ionized hydrogen. By exposing the wafer to 1:1 Ar:H_2 plasma, native oxide and hydrocarbons on the wafer surface are removed and the silicon surface becomes fully terminated by hydrogen atoms, rendering it hydrophobic. The wafer is next trensferred to a Si molecular beam epitaxy (MBE) chamber under UHV, where it is heated to 600 ℃ to desorb the hydrogen from the surface. The thermal desorption treatment results in a clean hydrophilic silicon surface ready for bonding. The bonding process is preferably performed in situ, immediately after the desorption treatment in order to avoid native oxide growth by exposing the wafer to air. Alternatively, the native oxide can be removed using thermal treatment at 850 ℃ in

UHV [40].

2.3 Wafer Bonding Characterization Methods

2.3.1 Optical transmission

A common issue in wafer bonding is the formation of interface voids. Therefore, a careful inspection procedure of the bonding interface is required. Optical transmission is a widely used inspection method for analyzing interface such interface voids. In order to minimize the absorption of radiation by the wafer substrate, the wavelength λ of the selected light source must satisfy the criterion expressed by Eq. 2, where h is the Plank constant, c is the speed of light in vacuum and E_g is the bandgap energy of the substrate material [39].

$$\lambda > \frac{hc}{E_g} \tag{2}$$

The wavelength is therefore a function of the wafer substrate material. In the case of transparent wafer materials such as glass and quartz, visible light can be employed for optical transmission. However, in the case of silicon and silicon dioxide wafer, infrared (IR) light has the appropriate wavelength to enable the inspection of interface voids. A schematic of the system configuration for the IR inspection of bonded silicon wafers is depicted in Fig. 12 [39].

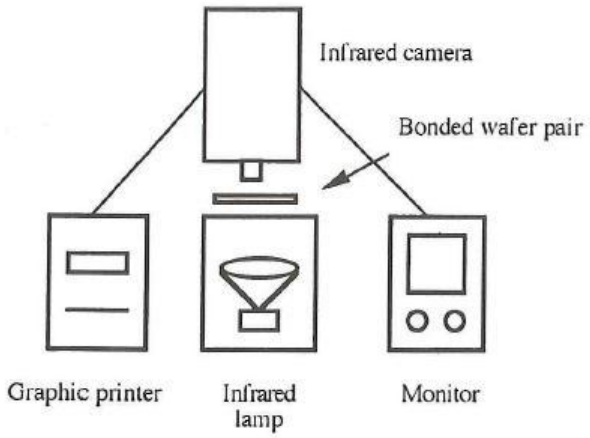

Figure 12: IR imaging system configuration for measuring interface voids in Si/Si and SiO_2/SiO_2 bonded wafer pairs [39].

The bonded wafer pair is positioned above the IR light source. The transmitted radiation is measured by the IR camera located above the wafer pair. By modifying the distance between the camera and the wafer pair, the interface is brought into focus and the data is analyzed and recorded using imaging software [39].

When particles are trapped at the bonding interfaces, the resulting interface voids or bubbles can be observed using IR light transmission from the interference fringes formed. The height of the interface bubble is given as a function of the IR radiation wavelength λ and the number of fringes N, according to Eq. 3.

$$H = N\frac{\lambda}{2} \tag{3}$$

The minimum detectable bubble size is half of one fringe. Therefore, the smallest bubble height which can be measured is 0.275 µm using an IR radiation wavelength of 1.1 µm. The minimum observable lateral size defines the system resolution and is dependent on the resolution of the IR camera. Typically, interface bubbles with diameters of 1 mm or larger can be observed, with smaller structures requiring the use of IR microscopes [39]. An IR image of two silicon wafers showing interface voids with interference fringes is presented in Fig. 12.

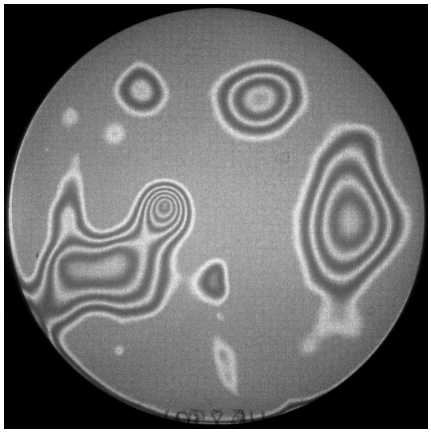

Figure 13: IR image of interface voids the at oxide-oxide bonding interface of two 100 mm silicon wafers.

Optical transmission based on IR light is an inexpensive, non-destructive and fast method to inspect interface voids of bonded silicon wafers in real time. However, its limited resolution in the lateral dimension can prove to be a drawback for some applications. Furthermore, metals are not transparent to IR radiation, which makes this technique not entirely suitable for wafers with large areas covered by metallic films [39].

2.3.2 Bond strength measurement using die shear test

Shear tests are a widely used technique to measure the bond strength of die-to-die or die-to-wafer bonded structures is represented by shear tests. A typical die shear test setup is presented in Fig. 14 [1].

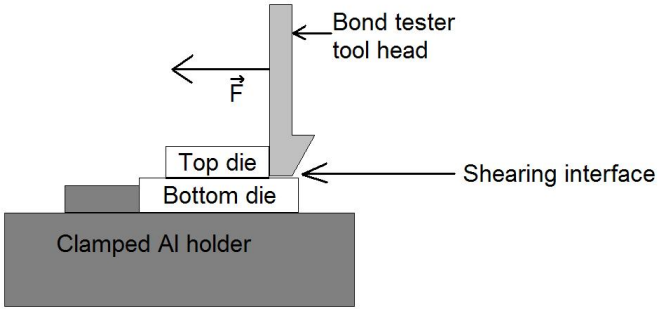

Figure 14: Schematic of die shear testing setup. [1]

The bonded dies are placed on a clamped metal holder and the top die is contacted by the toolhead of the bond tester machine. A load cell records the load displacement curve generated by the force

applied by the toolhead to the top die. According to the Mil-Std-883 industry standard, [42] the top die must be subjected to a stress parallel to the plane of the die attach substrate, represented in this case by the bottom die. In the case of a die attach material present at the die-die interface, this action causes a shear stress between: (1) the top die-die attach material interface and (2) the substrate - die attach material interface. Once the maximum shear force is reached, the top die detached from the substrate. The shear bond strength is given by the shear stress τ expressed in Eq. 4, where F_{shear} is the maximum shear force and A is the contact area between the top die and the substrate [43].

$$\tau = \frac{F_{shear}}{A} \tag{4}$$

Several important aspects need to be controlled carefully to ensure a reliable shear test is conducted properly. The toolhead needs to make contact with the full length of the die edge in order to apply the shear force uniformly. It should be possible to rotate the substrate holder in order to align the toolhead to the die edge. Also, the toolhead must be perpendicular to the die attach plane. Once the initial contact occurs between the toolhead and die, the position of the former must not change vertically. This is to ensure that the toolhead does not contact the substrate or the die attach material. After shearing, the mode of separation can be classified as: [42]

1. The die is sheared due to bulk failure with silicon material remaining attached to it;
2. The die is separated from the die attach material;
3. Both the die and die attach material are separated from the substrate.

2.3.3 Electrical Characterization

2.3.3.1 Sheet resistance of metallic layers is measured using van der Pauw structures such as the one illustrated in Fig. 15.

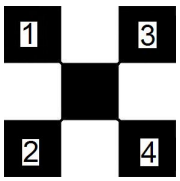

Figure 15: Typical van der Pauw structure for sheet resistance measurements.

The technique relies on the use of a virtually two-dimensional strucure with a thickness value much smaller than the length and width of the sample. A 4-terminal sensing method is employed by placing an ohmic contact on each of the four pads. A current I_{12} is forced between contacts 1 and 2, while a potential difference V_{34} is sensed over contacts 3 and 4. The sheet resistance is calculated using a correction factor according to the van der Pauw formula described in Eq. 5 [44].

$$R_S = \frac{V_{34}}{I_{12}} \frac{\pi}{ln(2)} \tag{5}$$

Several conditions must be met for a reliable measurement of van der Pauw structures. The metallic layer must be homogeneous, isotropic, without any isolated holes. Also, the layer must be flat and have a uniform thickness. Furthermore, the contacts must be positioned at the sample edege and the contact area needs to be an order of magnitude smaller than the total sample area. Although the measurement of asymmetrical stuctures is possible, a symmetrical sample is preferable to reduce calculation errors [45].

The resistivity ρ of a metallic layer of thickness t can be calculated according to Eq. 6.

$$\rho = R_S \cdot t \tag{6}$$

2.3.3.2 Contact resistance is an important parameter for wafer-to-wafer metallic interconnects fabricated using wafer bonding. A widely used structure employed for the measurent of contact resistance is the Cross Bridge Kelvin Resistor (CBKR), illustrated schematically in Fig. 16 [46].

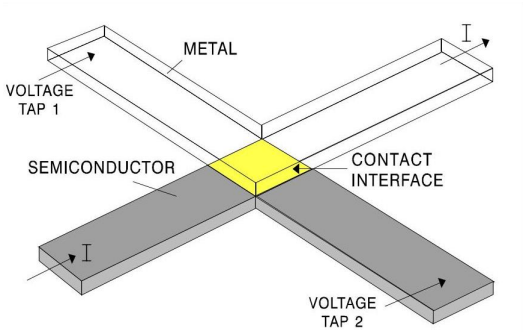

Figure 16: A schematic of a Cross Bridge Kelvin Resistor (CBKR), showing contact area in yellow. [46]

A 4-terminal sensing technique is used by forcing current I from the bottom layer (semiconductor or metal) through the contact area and into the top metal layer. The potential difference V is recorded using voltage taps placed on each conductive layer. The contact resistance R_C is calculated using Ohm's law as expressed in Eq. 7.

$$R_C = \frac{V}{I} \tag{7}$$

The specific contact resistance ρ_c is calculated according to Eq. 8, where A is the contact area between the two layers.

$$\rho_c = R_C \cdot A \tag{8}$$

In order to correct for parasitic resistances, error correction curves are used to obtain the true value of the specific contact resistance. However, the accurate measurement of very low ρ_c values ($< 10^{-7}\ \Omega \cdot \mathrm{cm}^2$) remains challenging [46].

3 Wet Etch Assisted Die Bonding

Surface activation by wet etching was investigated for die-to-die bonding of silicon chips. Starting from HF-assisted oxide-to-oxide bonding, metal-to-metal contacts were fabricated at room temperature using wet etching of Al-terminated dies. The bond strength was evaluated by die shear tests and analyzed as a function of etchant concentration. The realization of electrically conductive Al-Al contacts was demonstrated.

3.1 HF-assisted SiO_2-SiO_2 Die Bonding

3.1.1 Sample preparation

The starting material for this experiment consisted of single side polished monocrystalline 100 mm Si wafers with a 0.2-0.4 nm RMS roughness and a thickness of 525 ± 15 µm. A 300 nm thick silicon dioxide layer was grown using thermal oxidation. The wafers were diced into dies of various sizes from 2 mm × 2 mm to 10 mm × 10 mm. A cleaning step using isopropyl alcohol (IPA) followed by rinsing with DI water was employed to remove contaminants from the die surface. The large 10 mm × 10 mm dies were used as substrates onto which the smaller dies were bonded.

3.1.2 Bonding procedure

The bonding procedure consisted of manually applying a small droplet of HF solution on the substrate followed immediately by placing the top die and applying a small pressure to bring the two dies into full contact. The pressure was maintained for approximately 30 seconds until all the excess HF solution evaporated. The samples were left at room temperature for at least 24 hours for the reaction at the bonding interface to be complete before attempting to test the bond strength. The two SiO_2 layers are partially dissolved by the HF solution resulting in the formation of a thin interlayer at their interface. After the reaction is completed, the resolidification at the interface forms the interlayer, which provides the actual bond strength. A bonded pair of chips fabricated is such manner is presented in Fig. 17.

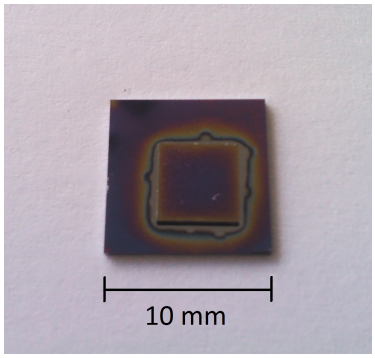

Figure 17: A 5 mm SiO_2 die bonded using HF to a 10 mm SiO_2 substrate die. SiO_2 etching by HF cause thickness variations, leading to light interference which causes colour differences around the top die.

3.1.3 Die shear test results

A substrate holder was fabricated from an Al block with a 450 µm thick stainless steel sheet section attached to it, as illustrated in Fig. 18.

During the shear test, the substrate was kept fixed by the sheet section, while the top die was able to glide over it. This is made possible by the lower thickness of the sheet section (450 µm) compared

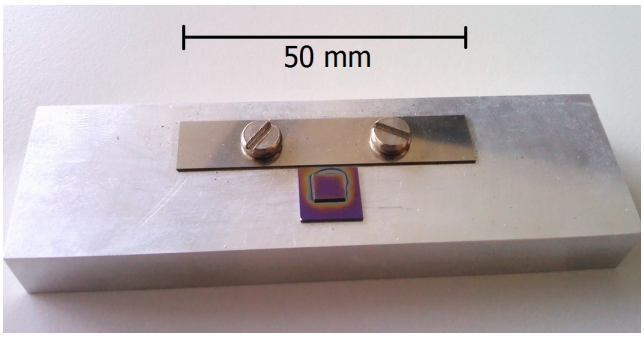

Figure 18: Die holder fabricated out of an Al block with stainless steel sheet section attached with two screws. Two SiO_2-SiO_2 bonded dies are positioned ready for die shear test.

to that of the substrate (525 µm). The bond strength was calculated based on the maximum recorded shear force according to Eq. 4. The results as function of the HF concentration are illustrated in Fig. 19 [1].

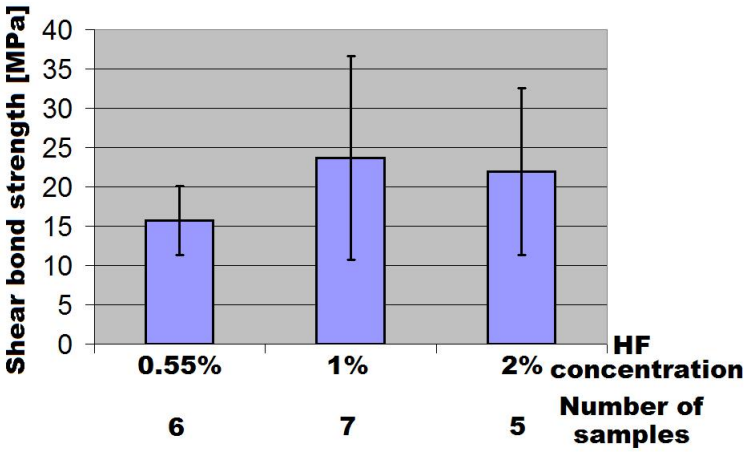

Figure 19: Influence of HF concentration on bonding strength according to shear tests on SiO_2-SiO_2 bonded dies with a contact area of 4 mm^2 [1]. Error bars indicate standard deviation.

The increase in bond strength from 15.71 MPa for 0.55% HF to 23.76 MPa for 1% HF can be attributed to the increase in HF etch rate of SiO_2 from 2 nm/min to 5 nm/min, respectively. [7] No further increase in bond strength is observed above 1% HF, as this concentration value is sufficient to form the necessary interlayer at the bonding interface. Concentration values above 10% can actually result in virtually zero bond strength due to the complete removal of SiO_2 layers by the strong acid solution.

Top dies of various sizes were used during the experiment. The bond strength values obtained for different die sizes are not influenced by the contact area, which indicated that the shear tests is a reliable indicator of the bond quality. For example, bond strength values of 15.71 MPa and 14.54 MPa were obtained for die sizes of 2 mm × 2 mm and 5 mm × 5 mm, respectively. The highest bond strengh values achieved using HF-assisted bonding of SiO_2-SiO_2 dies at room temperature were in the 20-25 MPa range, which are higher than those reported in the literature for bonding using eutectic alloys or polymers [6].

3.2 PES-assisted Al-Al Die Bonding

3.2.1 Sample preparation

The same type of Si wafers were used as starting material for this experiment. After growing a 300 nm layer of SiO_2 by thermal oxidation, sputtering by PVD was employed to deposit a 400 nm thick Al layer. After dicing, die samples of various sizes from 2 mm × 2 mm to 10mm × 10 mm were obtained.

A separate batch of wafers was sujected to patterning of the Al layer using standard photolithography, dry etching of exposed Al and cleaning steps. Dicing was used to obtain patterned 5 mm × 5 mm Al samples which were later bonded to 10 mm × 10 mm die substrates fully covered with Al. In order to measure the electrical contact resistance, the bulk Si material and oxide layer using deep reactive ion etching (DRIE).

3.2.2 Bonding procedure

An Al-etchant mixture of phosphoric acid- acetic acid - nitric acid 77:19:4 (vol. %) Selectipur® PES solution was used to bond Al-Al dies. A small droplet of diluted PES solution was placed on the 10 mm × 10 mm substrate die, followed immediately by placing the top die and applying pressure. After a 30 second drying time, the bonded chips were stored at room temperature for at least 24 hours before bond strength tests.

3.2.3 Die shear test results

Maximum shear force values measured using die shear tests were utilized to calculate the bond strength of both patterned and unppatterned Al-Al bonded dies. The results are depicted in Fig. 20 as function of the PES concentration [1].

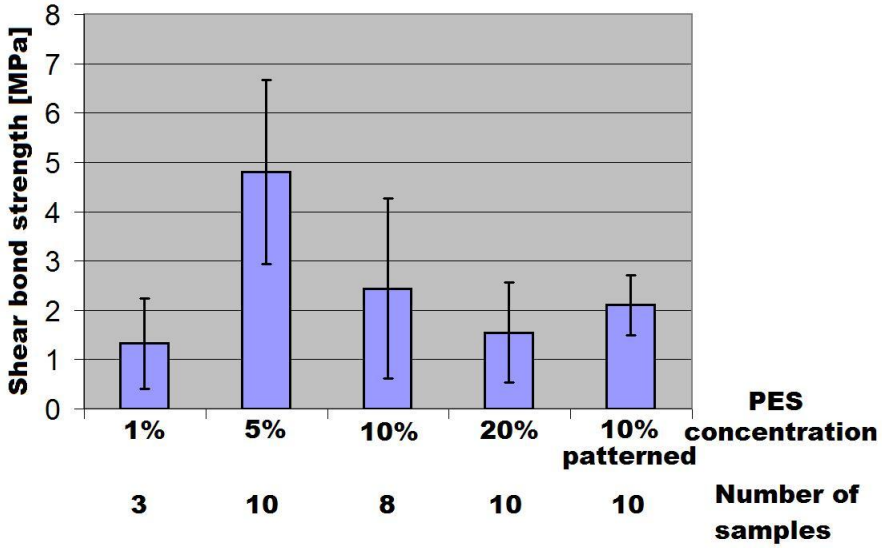

Figure 20: Influence of PES concentration on bonding strength according to shear tests on Al-Al bonded dies with a contact area of 4 mm^2 [1]. Error bars indicate standard deviation.

The bond strength increases with PES concentration, reaches a peak of 4.72 MPa at 5% PES and then decreases for higher concentration values. This is explained by the influence of the PES etchant

on the Al-Al interface. A certain amount of PES acid mixture is recquired to partially etch the two Al surfaces and form an interlayer by resolidification. However, at higher etchant concentrations, the interlayer increases in thickness and becomes more non-uniform, which results in lower bond strength, as confirmed by similar results reported in the literature [7]. The relatively large standard deviation values suggest that further improvements are needed such as automated die placement and better control of the applied pressure which would increase the reproducibility of the bonding conditions.

The bond strength measured using patterned Al dies is similar to that of unpatterned dies for the same HF concentration. Given that the Al area of the patterned dies is significantly lower than the total area, the results indicate a possible increase in bond quality for patterned dies. The patterned structure of the top die results in a 400 nm separation between the SiO_2 layer of the top die and the Al layer on the bottom die. This separation is believed to help with the evaporation of the etch by-products, which would otherwise remain trapped at the bond interface. As it can be seen from Fig. 21, such by-products are present between the Al structures, but do not influence the bond quality. Therefore, the interlayer created by partial etching at the Al-Al interface results in higher bond strength.

3.2.4 Electrical measurements

A proper electrical contact measurement was not possible due to the lack of patterned structures on the bottom die, which could allow for the realization of CBKR structures. A picture showing the Al-Al contacts is presented in Fig. 21. No alignment was possible during the bonding process. However, a qualitative assessment of the electrical connection was performed. The top and bottom Al layers were contacted with probe needles and a current was forced through the vertical contacts, while the potential difference was measured and recorded. The resistance measured was in the range of tens of mΩ, which indicated the successful fabrication of a conducting Al-Al contact.

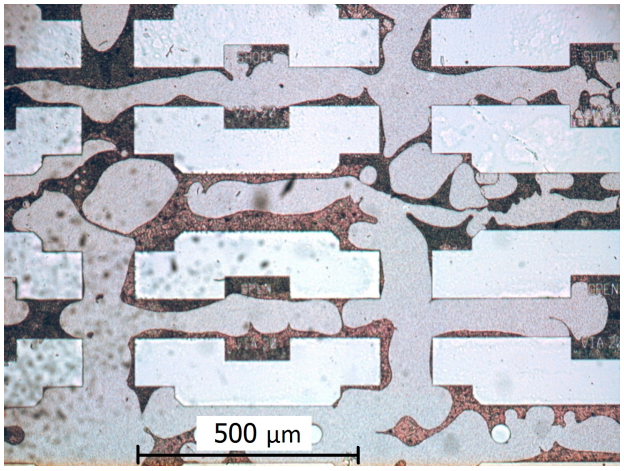

Figure 21: Al-Al contacts after top chip removal by DRIE. Bright areas: Al layer from the top chip; darker grey areas: Al layer on the bottom die; irregular dark shapes: etching by-products from the PES-Al chemical reaction.

3.3 Conclusions

The die bonding experiment based on wet etching was successful in demonstrating a room temperature technique for die-to-die attach using both oxide-to-oxide and Al-Al metallic bonding.

The first part of the experiment focused on oxide-oxide bonding using HF for surface activation. The values obtained for the shear bond strength as function of HF concentration were collected and analyzed. The highest shear bond strength values achieved were in the 20-25 MPa range using 1% HF, comparable to results reported in the literature for eutectic alloy and polymer bonding [47, 48, 49].

The **contribution of the current work to the research effort** is the fabrication of electrically conductive Al-Al interconnects through die bonding at room temperature using a **novel surface activation technique by wet etching**. The variation of shear bond strength with PES concentration was investigated. The highest shear bond strength value obtained was 4.72 MPa for a 5% PES concentration. The variation of bond strength with PES concentration was explained based on the intralayer thickness dependence on the Al etch rate at the bond interface. Pattened Al dies were also successfully bonded using PES to Al-coated die substrates using 10% PES solution with a measured shear bond strength of 2.18 MPa. The Al-Al contact resistance was measured after top die bulk silicon removal using DRIE. In the absence of proper CBKR structures, no quantitative results were possible. However, the resistance values measured were in the range of tens of mV, indicating the presence of an electrically conducting Al-Al ohmic contact.

The die-to-die bonding experiment based on surface activation by wet etching provided valuable information regarding the room temperature fabrication of die-to-die interconnects. The shear bond strength and electrical measurements have shown promising results for die bonding at room temperature. The realization of Al-Al interconnects is especially important for 3D integration applications. However, further research effort is required in order to optimize the die bonding process. Recommendations for future work include automatic die pick & place and control of the applied pressure in order to increase the reproducibility of die bonding conditions.

4 Nanocopper Interconnect Patterning using Photolithography

Screen printing is a widely used technology for printed electronics and metallization of solar cells. The technique relies on the pattern transfer from the stencil to the substrate. A squeegee terminated with a fill blade is moved across the stencil while a certain degree of pressure is applied to force the ink/paste into the stencil openings. The stencil is removed mechanically, leaving the patterned paste deposited on the substrate.

The resolution of this method is largely limited by the stencil dimensions and paste composition. The thickness is usually in the range of tens of microns, with lower values not being able to ensure the mechanical integrity of the stencil. Stencils are commonly fabricated out of stainless steel and have openings in the range of hundreds of microns. Capillary forces acting on the paste during the stencil removal result in paste particles remaining attached to the stencil sidewalls, which leads to patterning issues. Decreasing the size of the stencil openings appears to aggravate such problems. Furthermore, the resolution is limited by the paste particle size, which can be 40 µm or more for solders.

The following section presents an approach for fabricating metallic interconnects with a critical dimension in the 1-5 µm range using lithographically defined photoresist as stencil for screen printing. The nanocopper paste used with sub-micron particle size was screen printed on silicon wafers using developed photoresist for pattern transfer. After the resist lift-off process, copper metallic interconnects were left on the wafer substrate. The process was optimized by a careful control of the screen printing conditions and lift-off parameters.

4.1 Sample Fabrication Procedure

Standard 100 mm single side polished monocrystalline silicon wafers with 525 µm thickness were used as the starting material for this experiment. A 300 nm silicon nitride (Si_3N_4)layer used as copper diffusion barrier was deposited using low-stress low pressure chemical vapor deposition (LPCVD). AZ Nlof 2000 series negative resist was deposited using spin coating. After a soft bake step at 95 ℃, the resist was exposed using an ASML PAS 5500/80 I-Line stepper. A 115 ℃ subsequent bake step was employed to cross-link the negative resist, followed by development using MF322 solution.

A separate batch of wafers was prepared using sputtering by PVD to deposit a 300 nm Cu layer. This was done to improve the adhesion, as the nanocopper paste was found to adhere better to bulk Cu than to Si_3N_4. The wafers were coated with positive resist, exposed and developed to fabricate a mask for etching the bulk Cu layer. An aqueous solution of $Na_2S_2O_8$ and H_2SO_4 was employed to etch the exposed Cu areas. Removal of the developed photoresist was performed using NMP heated to 70 ℃. After rinsing with DI water and spin drying, the wafers were covered with negative resist and patterned using the procedure described in the previous paragraph.

The same technique was repeated using positive instead of negative resist, obtaining the same results. Acetone was found to remove the nanocopper material. Therefore, NMP was used for the lift-off process of the positive resist, resulting in clearly defined patterning of the nanocopper structures.

4.2 Screen Printing Process

The patterned photoresist layer used as stencil for screen printing is illustrated schematically in Fig. 22 (a).

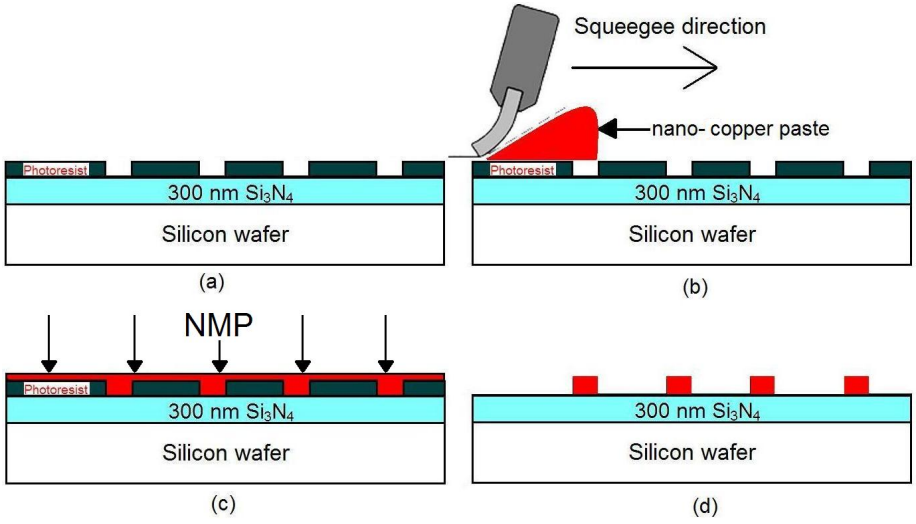

Figure 22: Sample fabrication using screen printing: **(a)** developed resist acting as stencil; **(b)** nano-copper paste screen printing; **(c)** resist lift-off using NMP; **(d)** nano-copper interconnects after cleaning steps.

The nanocopper paste utilized was developed by Dr. Zinn from Lockheed Martin [18] and is trademarked as CuantumFuse®. A small quantity of the nanocopper paste was dispensed using a syringe on the silicon wafer. A squeegee fill blade from KOENEN Technologies with a 65° hardness was used to screen print the copper paste on the substrate, as indicated schematically in Fig. 22 (b). The edge of the squeegee fill blade needs to be as straight as possible in order to obtain an uniform nanocopper paste layer on the substrate wafer during screen printing. Therefore, a squeegee holder was fabricated by inserting the squeegee fill blade between two stainless steel plates with a thickness of 5 mm. The plates were secured using two screws, which were tightened while keeping the two steel plates parallel. This ensured that the fill blade was kept fixed and its edge was maintained straight during the screen printing process. The squeegee holder setup is illustrated in Fig. 23.

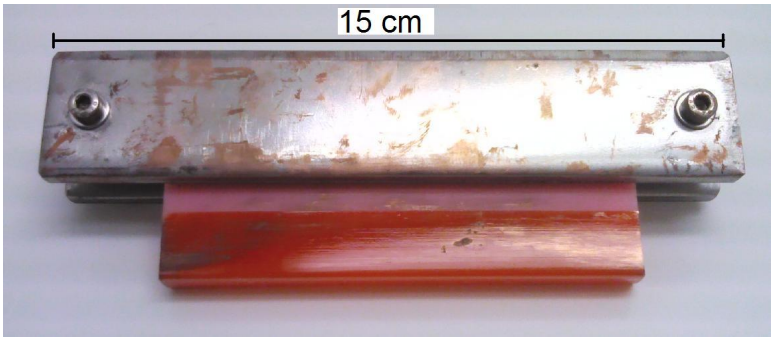

Figure 23: Squeegee holder setup.

The applied pressure and the angle of inclination of the blade with respect to the wafer surface were varied to optimize the uniformity of the nanocopper paste layer. When the edge of the squeegee blade reaches the a contact opening in the resist mask, elastic deformation caused by the applied pressure warps the blade. The part of the blade over the contact opening is not supported by the resist layer and is thus free to deform, bringing its edge below the resist layer level. As the squeegee fill blade moves across the wafer, it drives a certain amount of copper paste in front of it. When the

squeegee reaches the falling edge of a contact opening, the blade edge sinks below the resist layer level, leaving a depression in the copper paste profile. As the squeegee blade arrives at the rising edge of the contact opening, a part of the copper paste driven in front of the blade becomes trapped against the resist sidewall, forming a bulge in the nanocopper layer. These effects are illustrated schematically in Fig .24.

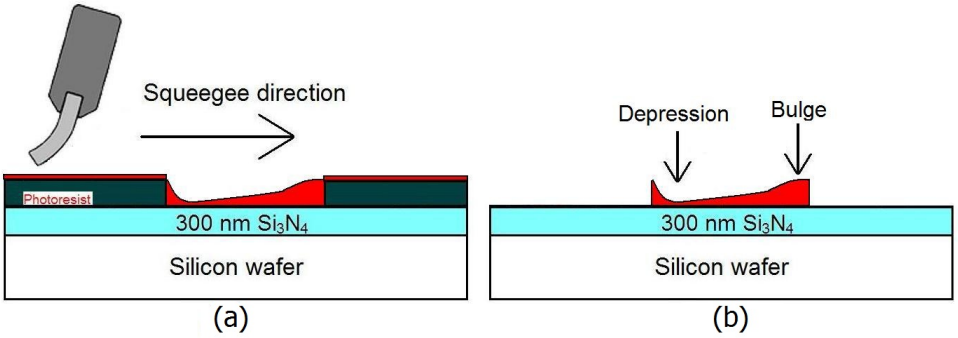

Figure 24: Surface profile effects along squeegee direction during screen printing: **(a)** squeegee blade movement; **(b)** depression and bulge left in the copper layer after resist removal.

The bulge and depression effects were investigated using optical microscope imaging and the results are presented in Fig. 25. When applying high pressure to the squeegee, the depression caused in the copper layer was so pronounced that the nanocopper paste was completely removed over local areas, exposing the Si_3N_4 layer underneath. The maxima in the surface topography corresponding to the bulge effect are also visible in Fig. 25 (b). By lowering the applied pressure, significant improvements were obtained, with no visible depression and bulge effects being observed, as can be seen from Fig. 25 (a). The lowest height non-uniformities in the deposited copper paste were obtained using an angle of inclination between the blade surface and wafer planes of approximately 20°. Higher inclination values resulted in very thin nanocopper paste layers and damage to the photoresist mask layer.

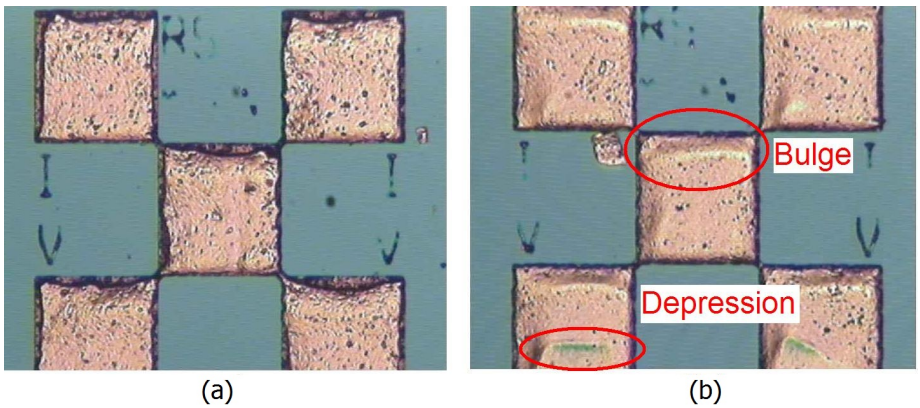

Figure 25: Bulge and depression effects during screen printing using: **(a)** low pressure; **(b)** high pressure.

Elastic deformation of the blade perpendicular to the direction of squeegee movement results in a warped blade edge profile, as depicted in Fig. 26 (a). As the nanocopper paste is pressed and driven forward by the squeegee, it acquires the surface profile of the blade edge, with a minimum thickness

(or depression) present in the center of the contact opening and increasing thickness values toward the photoresist sidewalls, as indicated in Fig. 26 (b).

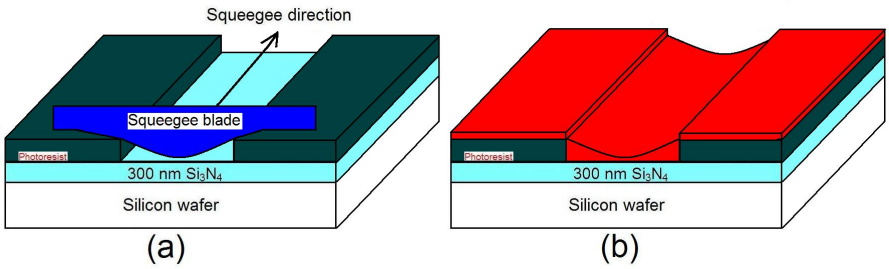

Figure 26: Surface profile effects perpendicular to squeegee direction during screen printing: **(a)** squeegee blade movement; **(b)** depression formed in the nanocopper paste layer in the center of the contact opening.

Optical microscope images shown in Fig. 27 illustrate the effect of the warped blade edge on the thickness profile of the nanocopper layer. By applying a high pressure to the squeegee, its blade edge is severely warped, leaving a very thin copper paste layer, with exposed Si_3N_4 along the center of the contact openings corresponding to the thickness depressions explained previously, as can be seen in Fig. 27 (b). By applying lower pressure to the squeegee, the depression effect was significantly reduced, as can be seen from Fig. 27 (a). However, lowering the pressure too much can result in incomplete filling of the contact openings with nanocopper, as insufficient pressure is applied to the paste to reach all the resist openings. Therefore, a compromise between the depression level in the nanocopper paste layer thickness and the filling of the resist contact openings was reached through a careful control of the applied pressure.

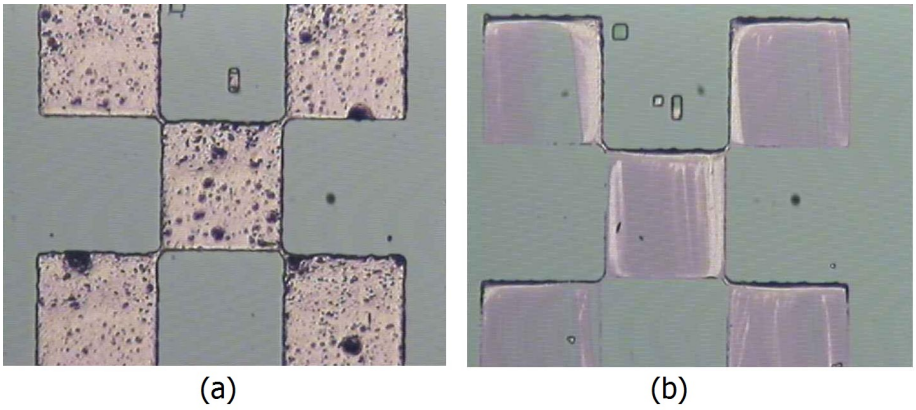

Figure 27: Depression effect during screen printing using: **(a)** low pressure; **(b)** high pressure.

The viscosity of the nanocopper paste also plays a role in the screen printing process. Using a lower paste viscosity resulted in more pronounced bulge and depression effects, as the fill blade is able to imprint its warped profile better on the less viscous paste. Furthermore, nanocopper paste with higher viscosity can dry within a few seconds after being dispensed on the wafer surface and can result in higher thickness of the nanocopper layer.

4.3 Lift-off Process

The nanocopper layer is dried on a hot plate at 50 ℃ for 5 minutes, followed by the photoresist lift-off process using NMP. The wafers were placed in an ultrasonic bath in N-Methyl-2-pyrrolidone (NMP) at room temperature. The ultrasonic agitation was able to permit the infiltration of NMP through the nanocopper paste and reach the photoresist and dissolve it. The lift-off process is depicted schematically in Fig. 22 (c). The exposure times to ultrasonic agitation and to NMP were varied in order to obtain clearly defined nanocopper structures, as presented in Fig. 22 (d).

After the screen printing process, nanocopper paste is attached to the resist sidewalls of the contact openings. Once the paste is dried, it forms a solid continuous layer covering the entire wafer, including the photoresist areas. During lift-off, the underlying resist layer is dissolved and removed along with the nanocopper paste covering it. Ideally, a sharp transition corresponding to the resist sidewalls will occur between the areas with removed resist and the ones with nanocopper paste. However, due to the brittleness of the dried nanocopper layer, excessive exposure to ultrasonic agitation can result in nanocopper removal from the edges of patterned structures corresponding to the dark areas in Fig. 28 (a).

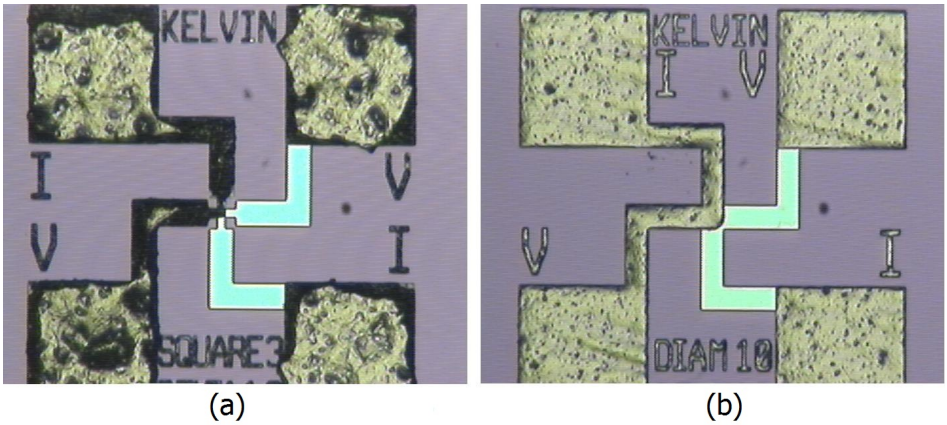

Figure 28: Influence of ultrasonic agitation during resist lift-off with NMP using: **(a)** 2 min ultrasonic exposure; **(b)** 1 min ultrasonic exposure.

In order to correct for the abovementioned edge effect, the ultrasonic agitation time was reduced from 2 min to 1 min, which resulted in significant improvements, specifically the clear patterning definition of the structure edges without any visible dark areas, as can be seen from Fig. 28.

4.4 Measurements and Results

4.4.1 Nanocopper layer height and surface profile

A Dektak 150 surface profiler was used to measure the height of the nanocopper structures after development using NMP. The developed resist height was also measured using the same equipment. Furthermore, the average surface roughness was measured by scanning the nanocopper structures.

A height profile of a 80 µm sized nanocopper structure is presented in Fig. 29. The resist thickness used was 1.5 µm thick and the profile shows the nanocopper height after resist removal in NMP. This result confirms the depression and bulge effects discussed previously. As can be seen from Fig. 29,

Table 2: Resist and nanocopper parameters measured with Dektak surface profiler.

Resist ASH [µm]	Nanocopper ASH [µm]	Nanocopper roughness [nm RMS]
1.52	1.15	146
2.03	1.73	237
3.08	2.64	284

in the 40-70 µm range on the x-axis, the height reaches a minimum of 500 nm corresponding to the depression point. The bulge is evident in the 85-105 µm range on the x-axis, confirming the direction of squeegee movement from left to right during the screen printing process. The **average surface height (ASH)** of the nanocopper layer is 812 nm, which is significantly lower than the resist thickness of 1.5 µm. The difference can be explained by the volume reduction of the paste as it dries through solvent evaporation and by the depression effect resulting from the squeegee blade deformation.

Figure 29: Height profile of nanocopper structure after NMP lift-off process.

Resist nominal thicknesses in the range of 1.5-3 µm were used for the screen printing process. The thickness values were measured using the Dektak surface profiler along with the height and average surface roughness of the nanocopper layer. The results are presented in Table 2.

The average height of the nanocopper layer is approximately 20% lower than that of the resist layer, with the difference originating from nanocopper paste volume reduction through drying and the depression effect caused by fill blade deformation. The average surface roughness increases with layer thickness, reaching approximately 300 nm RMS for the 3 µm layer.

4.4.2 Patterning resolution

In order to study the patterning limits of the nanocopper screen printing technique, resolution test structures were prepared using 1.5 µm negative resist as mask. The screen print and lift-off process conditions were optimized for obtaining clearly defined structures and the results are illustrated in Fig. 30.

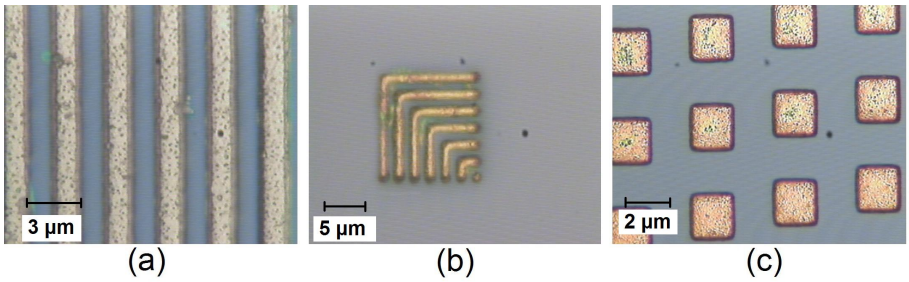

Figure 30: Patterned nanocopper structures: (a) lines with a pitch of 3 µm; (b) corner lines with a pitch of 2 µm; (c) squares with a pitch of 4 µm.

Successful nanocopper structure patterning was achieved down to 1 µm dimensions. The limiting factor for the experiment was the lithography resolution along with the minimum resist thickness of 1.5 µm. Therefore, based on these results, it can be concluded that the patterning of interconnects with smaller critical dimension would be possible using a higher resolution lithographic processes.

4.5 Conclusions

A novel interconnect patterning technique was developed based on lithographically defined screen printing of nanocopper. Screen printing issues such as the bulge and depression effects were studied and corrected by optimizing the squeegee pressure control. The nanocopper sidewall patterning problem during lift-off was addressed by optimizing the ultrasonic agitation parameters. A **high patterning resolution up to 1-5 µm** was achieved using a negative photoresist mask 1.5 µm thick. Based on these results, **sub-micron patterning of nanocopper interconnects** is expected to be possible by using higher resolution lithographic equipment. Although further optimization of the screen printing and lift-off processes is required, the novel nanocopper technique developed shows promising results for 3D integration applications.

5 Wafer Bonding Based on Nanocopper Sintering

The wafer bonding experimental work based on nanocopper sintering is presented in the current chapter 5. Several nanocopper parameters such as sheet and contact resistance, copper nanoparticle dimension, nanocopper paste composition and fusing profile are investigated. Die-to-die bonding is employed as a preliminary test for evaluating the shear bond strength and copper nanoparticle fusing at the bond interface. The obtained results are utilized for optimizing the bonding process and are applied to the wafer-to-wafer bonding process for 3D nanocopper interconnect fabrication.

Please note that sintering represents a transition process from small particles to larger structures achieved through atomic difussion enhanced by applying heat and external pressure. In the current work, the term **"nanocopper sintering"** is employed to denote a process in which external pressure is applied to the nanocopper material. The term **"nanocopper fusing"** refers to the transition from nanoparticles to larger entities based solely on heating the nanocopper paste and without applying external pressure.

An overview of the current chapter was give in the introductory section 1.3.

The nanocopper sheet resistance characterization is described in section 5.1. The sample fabrication procedure of van der Pauw sheet resistance test structures is described and the fusing parameters are presented. The sheet resistance measurements are presented and analyzed, followed by explanations of the results and conclusions. The investigation of nanocopper-to-bulk copper contact resistance is presented in section 5.2. After the test structure fabrication is described, the nanocopper fusing parameters are give, focusing on copper oxidation prevention. The contact resistance measurement procesure is explained, together with a schematic illustration of current flow. The contact resistance results are presented and discussed. The effects of fusing temperature and copper oxide-reducing agents on the contact resistance value are described, followed by conclusions.

Chapter 5.3 discusses the in-situ measurement of nanocopper resistance as function of fusing temperature. After the fabrication of the nanocopper sample on a PCB substrate is described, the fusing profile parameters are explained. The results are presented and discussed, with an explanation of the observed resistance variation being provided. Section 5.4 provides valuable information regarding the nanocopper material composition such as copper nanoparticle dimension, particle conglomeration and copper nanoparticle encapsulation by organic surfactants based on transmission electron microscope (TEM) analysis. Further investigation of the nanocopper paste composition and fusing profile is presented in section 5.5 based on thermal gravimetric analysis (TGA). The mass loss rate is recorded as function of temperature, enabling the identification of different solvents and other organic components of the nanocopper paste based on their boiling temperatures. Furthermore, the nanocopper fusing point was determined based on the TGA results.

The die-to-die bonding experiment is presented in section 5.5. The sample fabrication procedure is explained and the die bonding process using nanocopper sintering is explained. The bond interface is investigated using SEM imaging of a cross-section obtained using ion-milling. The nanocopper porosity is estimated based on the SEM images. Die shear tests are utilized to study the influence of sintering temperature and copper oxide removal agents on the shear bond strength. The observed effects are discussed and explained, followed by conclusions. The wafer-to-wafer bonding experiment is presented in section 5.7. The sample fabrication procedure is described in detail, including a schematic illustration of the processing steps. Infrared imaging is employed to check the alignment of the bonded nanocopper structures. The contact resistance measurement procedure is described and the results are presented. The specific contact resistance is calculated and is plotted as function of the nanocopper sintering temperature. The internal structure of the sintered nanocopper at the bond interface is investigated using SEM imaging. Valuable data regarding the nanocopper porosity reduction and

formation of large copper structures during the sintering process. The chapter is concluded by a summary of the results obtained and effects observed during the experimental work presented.

5.1 Nanocopper Sheet Resistance Characterization

In order to investigate the possibility of wafer bonding based on nanocopper sintering, a preliminary analysis of the fused nanocopper properties is required. One important parameter for this novel nanoparticle metallic paste is its sheet resistance dependence on processing conditions, with fusing specifications being particularly relevant. Therefore, the measurement of nanocopper sheet resistance was investigated in the current section by fabricating and measuring standard van der Pauw structures.

5.1.1 Sample fabrication procedure

The starting materials for this experiment were 100 mm single side polished silicon wafers, 525 µm thick with an average surface roughness of 0.2-0.4 nm RMS. In order to protect against copper diffusion, a 300 nm Si_3N_4 barrier layer was deposited on the wafers using low stress LPCVD. A 300 nm Cu layer was sputtered on the wafers using PVD. Positive Shipley SPR 3012 photoresist with a 1.4 µm thickness was deposited on the wafers using spin coating. After a soft bake step at 95 °C, the mask pattern containing the van der Pauw test structures was exposed in the resist layer using an ASML PAS 5500/80 I-Line stepper. A post-exposure bake (PEB) step at 115 ℃ was performed to reduce the effect of standing waves produced in the resist layer during exposure. The exposed photoresist areas were removed during development. The final result was a patterned resist layer, which was used as mask for the nanocopper paste screen printing process. An example of a fabricated nanocopper van der Pauw structure for sheet resistance meaurements is presented in Fig. 31.

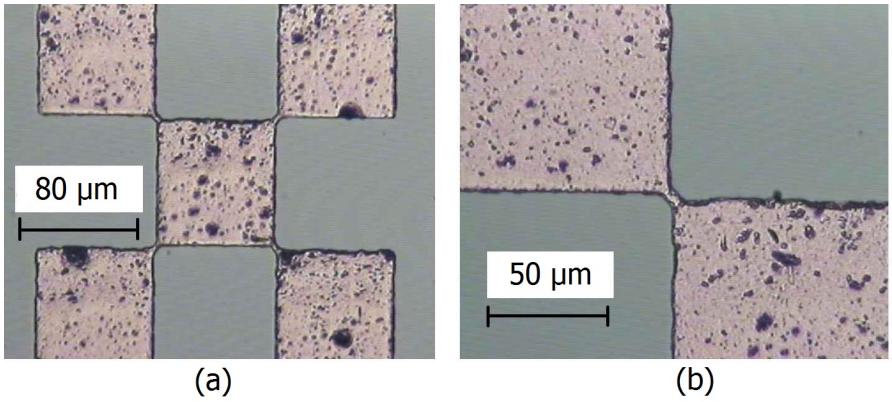

Figure 31: Sheet resistance structure: **(a)** van der Pauw structure; **(b)** detail showing 5 µm wide voltage tap line.

The technique used resulted in clearly defined structures down to 5 µm lines, as can be seen from Fig. 31 (b).

5.1.2 Nanocopper fusing process

The nanocopper paste was fused inside a Hereaus vacuum oven. Control of the oxygen content was crucial for obtaining relevant results. As the copper paste contains nanoparticles, the total area exposed to the surrounding environment is substantially larger than the area occupied by the nanocopper

structures on the wafer. This large area resuls in a high reactivity of the nanocopper paste with oxygen. Therefore, even trace amounts of oxygen present in the fusing ambient atmosphere can result in oxidation of the nanocopper structures, which degrades their electrical performance.

In order to minimize oxidation, the oven chamber was pumped down to 1 mbar and purged with nitrogen several times before the fusing process was started. The vacuum chamber pressure was kept at 1 bar and a continuous flow of nitrogen gas was used to prevent oxygen leakage from the outside environment.

The wafers were placed inside the vacuum chamber and, after nitrogen purging, the temperature was ramped up from 20 ℃ to the fusing temperature in 12 min. A ramp up rate of 15 ℃/min was selected in order to prevent bubble formation in the nanocopper layer at higher temperature increase rates. The wafers were kept at a constant fusing temperature ranging from 180 ℃ to 240 ℃ for 60 min, followed by cooling down to room temperature inside the oven for 2-3 hours.

5.1.3 Sheet resistance measurements

The sheet resistance measurements were performed on nanocopper van der Pauw structures by forcing a current and measuring the potential difference using 4-terminal sensing, as described in subsection 2.3.3.1. The voltage-current charateristics were recorded using 33 data points per measurement. A least square fitting of a linear function to the data points was performed and the correction factor for van der Pauw structures was used to calculate the sheet resistance value according to Eq. 5. The voltage offset and correlation coefficient of the curve fitted to the data points were measured and recorded. Values of the correlation coefficient below 0.995 indicate unreliable measurements caused by poor ohmic contact or damaged structures and the corresponding data were not included in the measurement analysis. The difference between data points with high and low correlation factors is illustrated in Fig. 32.

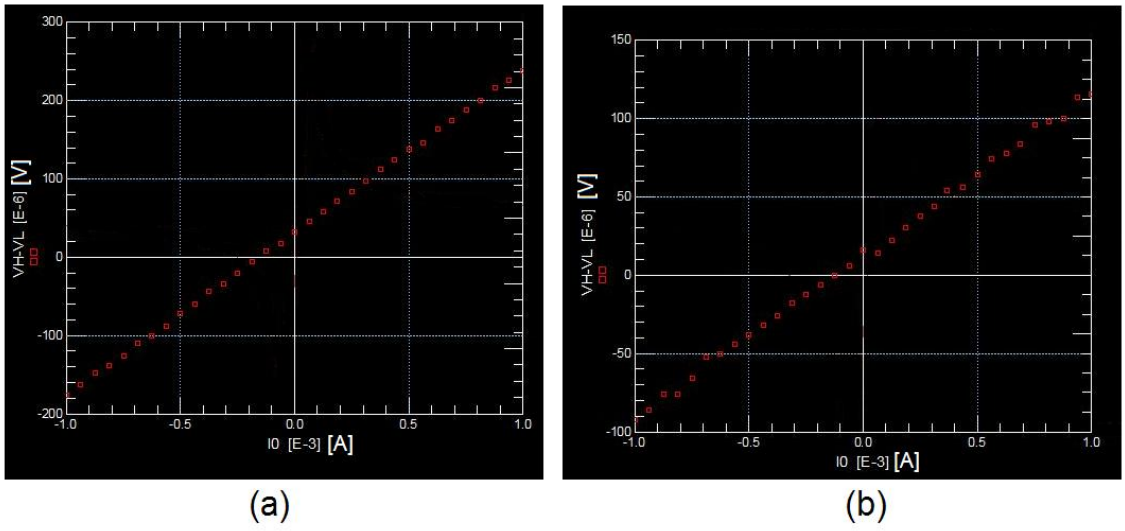

Figure 32: Voltage-current plots of measured nanocopper van der Pauw structures with curve correlation coefficients: **(a)** 0.999; **(b)** 0.995.

The average surface height of the nanocopper layer was measured using a Dektak surface profiler and used as the nanocopper thickness. The nanocopper resistivity was calculated as described in sub-

section 2.3.3 using the measured nanocopper sheet resistance and thickness values. Resist thicknesses of 1.5 µm, 2 µm and 3 µm were used for nancopper structure patterning for each of the four fusing temperatures (180 ℃, 200 ℃, 220 ℃ and 240 ℃). One wafer was used for each thickness-temperature combination and the resistivity results are based on the mean value of 15 sheet resistance measurements on each wafer.

5.1.4 Results and conclusions

The values obtained for the nanocopper resistivity as a function of fusing temperature are presented in Fig. 33 using the data from 4 wafers with nanocopper structures fused at a different temperature.

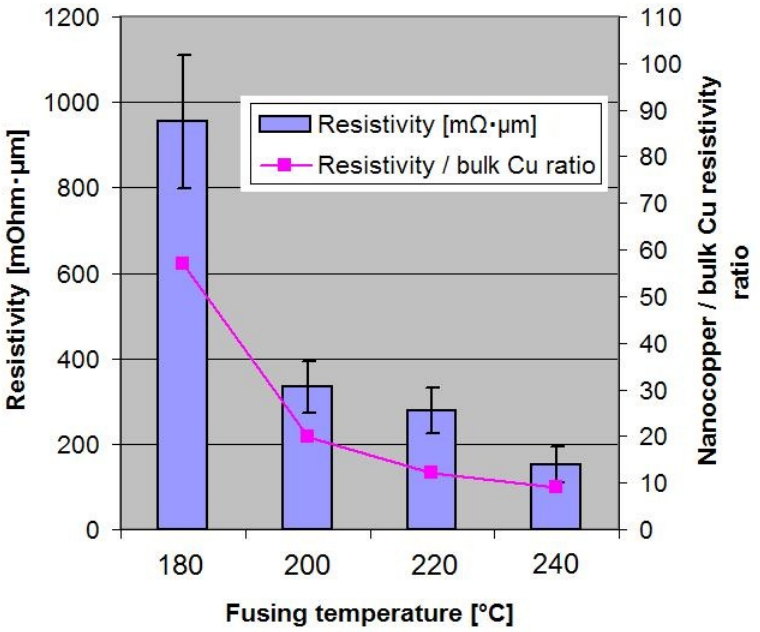

Figure 33: Influence of fusing temperature on nanocopper resistivity. Error bars indicate standard deviation on a sample size of 15 data points.

The nanocopper resistivity decreases with fusing temperature due to the increased surface energy and interaction of the nanocopper atoms at higher temperature [50]. The rate of resistivity decrease is lower at temperatures above 200 ℃, indicating that the nanoparticles have fused and no significant resistivity decrease is expected above 250 ℃. The lowest nanocopper resistivity value obtained was 151.7 mΩ · µm for the sample fused at 240 ℃. This value is approximately 9 times higher than the theoretical one for bulk copper (16.78 mΩ · µm [11]).

The difference in resistivity can be attributed to the stucture of the fused nanocopper material such as the relatively high porosity. Furthermore, the evaporation of solvents during the fusing process might cause voids to form in the nanocopper, resulting in a porous layer structure. The porosity and impurities or remaining solvents in the fused material contribute to the increased resistivity of the fused nanocopper with respect to that of bulk copper. The porosity of a nanocopper sample fused at 250 ℃ was estimated at 43% using image processing software on the SEM image of the nanocopper layer cross-section shown in Fig. 34.

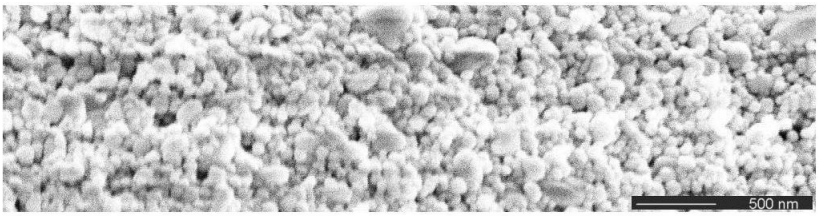

Figure 34: SEM image showing a cross-section of nanocopper material fused at 250 ℃ without any applied pressure and having a porosity of 43%.

5.2 Nanocopper-to-bulk Copper Contact Resistance Characterization

An important parameter for the electrical performance of wafer bonded metallic interconnects is the contact resistance. Therefore, a characterization of the nanocopper-to-bulk copper contact resistance was performed. The contact resistance value provides valuable information regarding the quality of the bond at the interface between the nanocopper and bulk copper materials. Cross-bridge Kelvin resistor structures were fabricated on silicon wafer substrates and measured in order to study the effects of fusing temperature variation and copper oxide reduction agents on the contact resistance.

5.2.1 Sample fabrication procedure

The starting materials for this experiment were 100 mm single side polished silicon wafers with the same parameters as in the previous section. A 300 nm Si_3N_4 barrier layer was deposited on the wafers using low stress LPCVD to protect against copper diffusion into the silicon. PVD was employed to sputter a 300 nm Cu layer on the wafer substrates. CBKR structures for measuring contact resistance were patterned in a positive photoresist layer using the same procedure as in the previous section. The developed photoresist was used as an etching mask for the bulk copper layer.

The exposed copper areas were etched using an aqueous solution of $Na_2S_2O_8$ and H_2SO_4. The developed resist was removed in NMP at 70 ℃, followed by wafer rinsing in acetone, IPA and DI water and spin-drying. The masking layer for the screen printing process was fabricated by coating the wafers with AZ Nlof 2000 negative photoresist, followed by exposing it with UV light, cross-linking and developing it using the procedure in subsection 4.1.

The bulk copper oxide was a limiting factor for obtaining low contact resistance values. Therefore, the efficiency of several copper oxide reducing agents was investigated. Separate wafers with bulk copper areas were exposed to aqueous solutions of formic acid, acetic acid and Cu etchant ($Na_2S_2O_8$ + H_2SO_4) for 30 seconds, followed by rinsing in DI water, drying and immediate screen-printing to minimize the growth of a new native oxide layer on the copper surface. A wafer without any copper oxide reduction treatment was used as reference. The different surface treatments are presented in the list below.

- Sample 1: 30 second etch in 85% formic acid at room temperature.
- Sample 2: 30 second etch in 50% acetic acid at room temperature.
- Sample 3: 30 second etch using 1.2% $Na_2S_2O_8$ + H_2SO_4 solution.
- Sample 4: reference wafer without copper oxide removal treatment.

The nanocopper paste was screen printed and the resist lift-off process was performed as described in sections 4.2 and 4.3. In addition to CBKR structures, daisy chains of bulk copper to nanocopper

contact structures were fabricated. Examples of such structures are illustrated in Fig. 35.

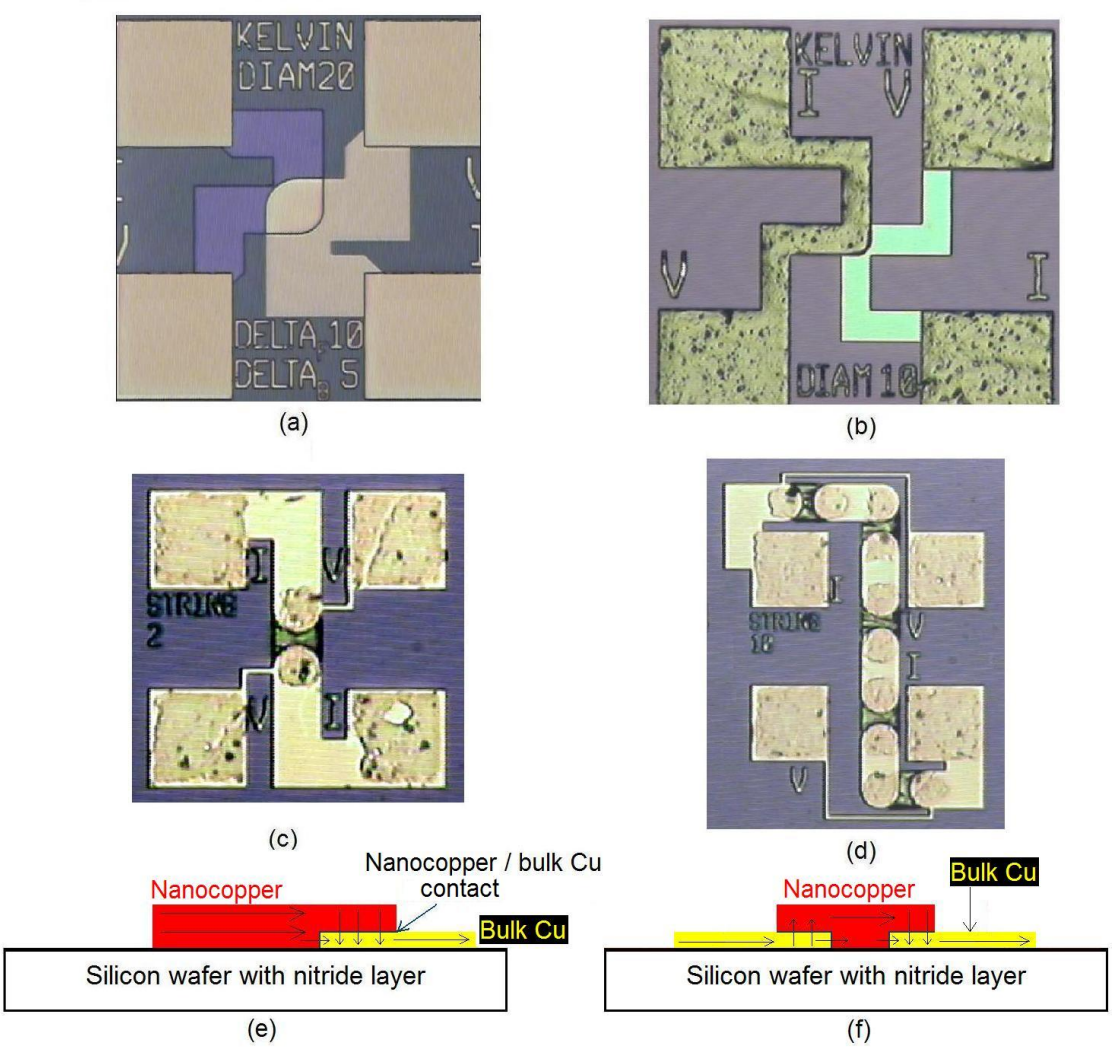

Figure 35: Contact resistance test structures: **(a)** CBKR structure before screen printing; **(b)** CBKR structure after nanocopper patterning; **(c)** daisy chain of 2 nanocopper contacts; **(d)** daisy chain of 10 nanocopper contacts; (e) current flow direction indicated by arrows in schematical cross-section of CBKR structure; (f) current flow direction indicated by arrows in schematical cross-section of daisy structure containing 2 contacts.

During the contact resistance measurements, the electrical current flows through the nanocopper, travelling through the nanocopper/bulk Cu and finally through the bulk Cu, as indicated in Fig. 35 (e). In the case of daisy structures the current flows through each nanocopper/bulk Cu interface as is indicated in Fig. 35 (f). A small amount of current will flow through the vertical interface corresponding to the bulk Cu sidewall. However, due to the reduced thickness (300 nm) of this sidewall compared to the structure dimensions in the range of 2-80 µm, most of the electrical current flows through the horizontal interface. Therefore, the lateral current flow is considered to be negligible. Challenges with the screen printing process due to height differences between the nitride and bulk Cu resulted in patterning issues in the case of daisy chain structures. Therefore, strings of more than

10 contacts could not be patterned with sufficient accuracy to fabricate structures which could be measured properly.

5.2.2 Nanocopper fusing process

The nanocopper sheet resistance structures were placed in side a Hereaus vacuum oven for the fusing process. A nitrogen purge was performed to minimize oxygen content as described in subsection 5.1.2. The temperature ramp up rate used was 15 ℃/min and the fusing temperatures investigated were in the 180-240 ℃ range. The samples were exposed to the fusing temperatures for 60 min, followed by a subsequent cooling to room temperature for approximately 3 hours.

5.2.3 Contact resistance measurements

The CBKR structures were measured using the 4-terminal sensing technique described in subsection 2.3.3. The extracted data was analyzed using Matlab software and a plot of the voltage-current (V-I) characteristic from a CBKR nanocopper struture is presented in Fig. 36. The sample was fused at 220 ℃ and a least squares fitting of a linear function to the data points resulted in a correlation coefficient of 0.9996, indicating a reliable ohmic contact.

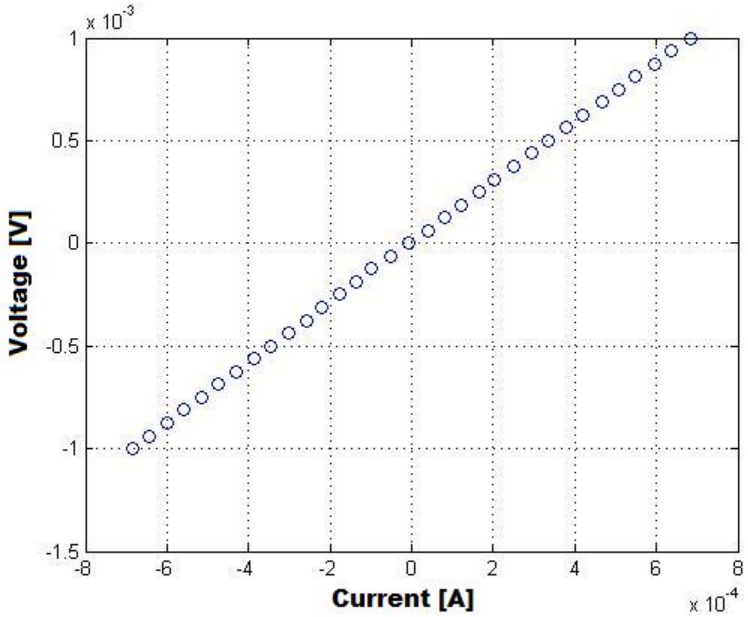

Figure 36: V-I data points of CBKR structure with a 20 µm × 20 µm contact area.

5.2.4 Results and conclusions

CBKR structures with various contact areas ranging from 1.4 µm × 1.4 µm to 30 µm × 30 µm were measured. The obtained contact resistance values decrease with increasing area, as expected, due to the larger area available for current flow. This dependence is illustrated in Fig. 38 (b). The line fitting approximates the reciprocal function *1/x*. This confirms the expectation for a contant specific contact resistance, independent of the contact area value. The specific contact resistance is calculated by multiplying the contact resistance with the contact area, according to Eq. 8 in subsection 2.3.3. The

variation of the specific contact resistance with fusing temperature for samples without any surface treatment is illustrated in Fig. 37 (a).

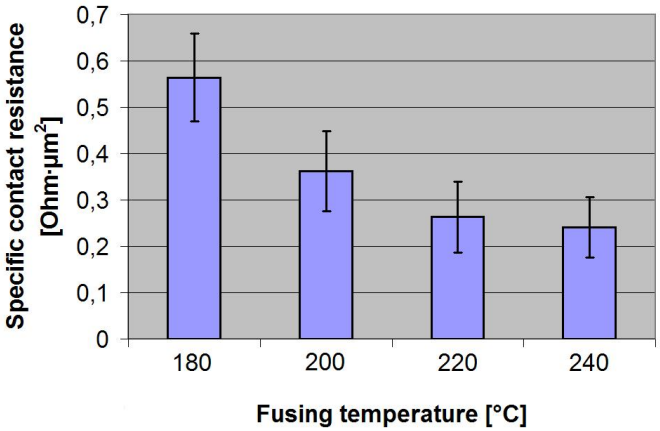

Figure 37: Specific contact resistance variation with fusing temperature. Error bars indicate standard deviation.

As expected, there is a decrease in specific contact resistance with fusing temperature. At higher temperatures, the surface nanocopper atoms have higher energy, making them more likely to form metallic bonds with nearby Cu atoms and fuse together. During this fusing process, the nanocopper atoms close to the bulk Cu/nanocopper interface will form bonds with the bulk Cu atoms. Any voids at the interface will increase the specific contact resistance by obstructing the electron flow. At higher temperatures, the nanocopper atoms reactivity increases, leading to better nanocopper fusing close to the interface. The rate of the decrease in specific contact resistance is lower at higher temperatures, which indicates that the fusing process has stabilized. Therefore, no significant change in specific contact reistance is expected at temperatures above 240 ℃.

The results for specific contact resistance as function of difference oxide reducing agents are illustrated in Fig. 38.

The use of acetic acid resulted in poor adhesion of nanocopper on the wafer substrate, causing patterning issues. Therefore, no structures were available for measurements on the sample treated with acetic acid. The samples treated with formic acid resulted in the lowest specific contact resistance value of 0.227 $\Omega \cdot \mu m^2$. This result is only 50% higher than the specific contact resistance value of bulk Cu samples bonded at 400 ℃ reported in the literature [25]. Therefore, specific contact resistance values only 50% higher were obtained at temperatures almost 200 ℃ lower. The samples treated with formic acid showed a 25.6% reduction in specific contact resistance compared to the reference sample, which can be explained by the enhanced nanocopper fusing to the bulk Cu layer in the absence or signicant reduction of copper oxides. A specific contact resistance value 29.5% higher than for the reference case was observed in the case of the sample treated with Cu etch solution. The extra contact resistance can be attributed to the partial etch of the deposited nanocopper by any Cu etchant residues on the surface. However, further investigation is required for a better understanding of this effect.

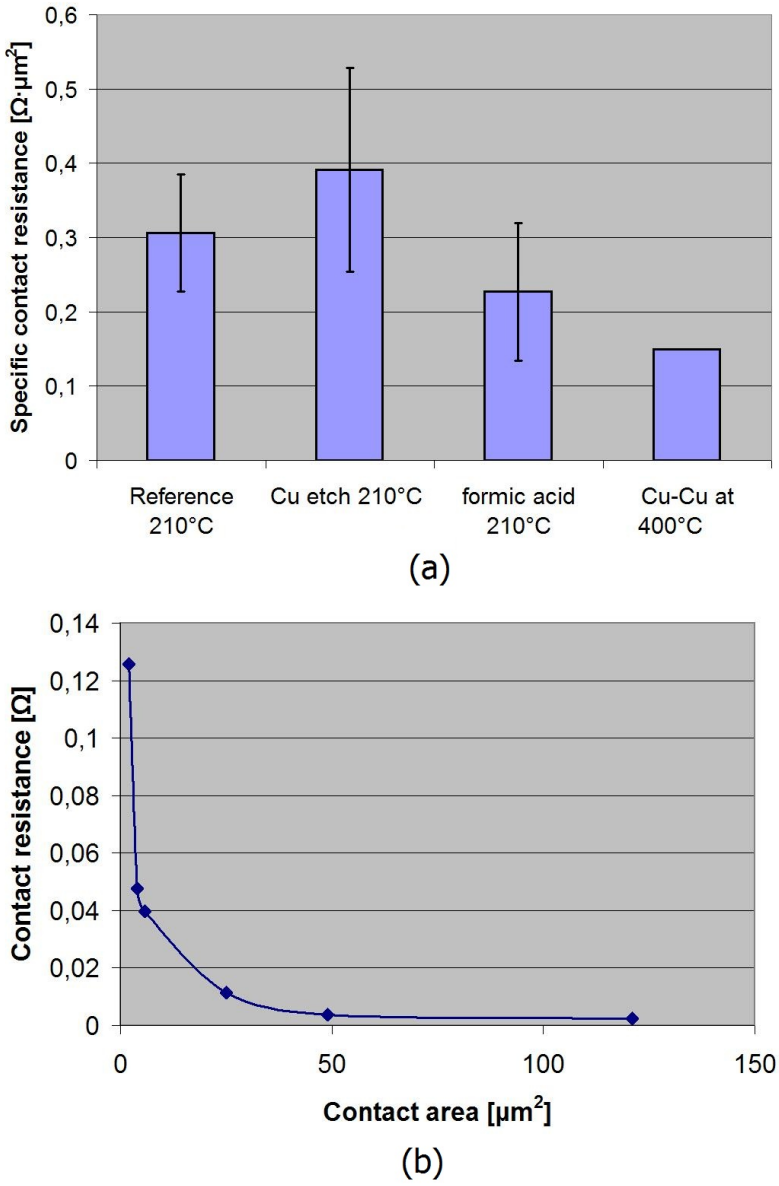

Figure 38: **(a)** Influence of oxide removal agents on specific contact resistance. Error bars indicate standard deviation; **(b)** Contact resistance variation of CBKR structures with contact area.

5.3 In-situ Nanocopper Fusing Measurement

The in-situ measurement of nanocopper resistance during fusing was performed. Nanocopper paste was applied between metallic contacts on a PCB. The sample was connected to I-V measurement equipment. A thermocouple was employed for an accurate reading of the fusing temperature. The sample was placed inside a vacuum oven and the temperature ramp-up rate was controlled based on the thermocouple readings. The resistance and temperature data were recorded and analyzed to produce the nanocopper fusing profile.

5.3.1 Sample fabrication procedure

A PCB with Al structures was used as substrate for screen printing a small quantity of nanocopper material between two Al lines. The obtained nanocopper structure dimensions were 2 µm × 10 µm and the layer thickness, measured with the Dektak profiler, was 3 µm. Copper cables were soldered to the Al pads on the PCB and connected to measuring equipment outside the oven. Two cables were soldered using SAC lead-free solder to each Al pad, one for supplying current and another for voltage sensing. A thermocouple placed inside the oven was used to record the fusing temperature.

5.3.2 Results and conclusions

The temperature and resistance values were recorded using data acquisition software and processed using Matlab. The temperature and resistance results are presented as function of recorded time in Fig. 39. As can be seen from the plots, during the first 35 min, the temperature increased from 50 to 200 ℃ corresponds to a decrease in resistance by 3 orders of magnitude. During the constant temperature step from 35 to 145 min, there was no significant change in resistance. However, the fusing process was not complete. The increase in temperature from 200 ℃ to 350 ℃ during time period 145 to 190 min causes a drastic decrease in resistance. Based on these data, the nanocopper fusing point corresponds to a temperature in the range of 220-260 ℃. The relatively constant resistance at higher temperature followed by a sharp resistance drop in response to the rise in temperature gives a clear indication of the critical fusing point at approximately 240 ℃. No further resistance decrease is observed at higher temperatures. Furthermore, the nanoparticle fusing is irreversible, as no significant increase in resistance is observed during the cooling down phase corresponding to the time period 190 min to 280 min.

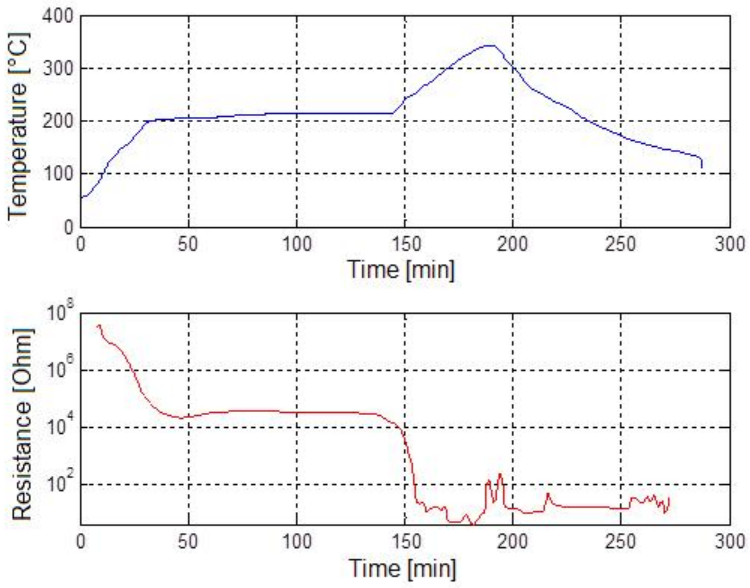

Figure 39: Nanocopper fusing profile showing temperature and resistance as function of recorded time.

The lowest resistance measured was in the 1-10 Ω range. Since no proper sheet resistance structures were fabricated, no reliable results regarding the quantitive nanocopper resistance were produced. However, the experiment has provided valuable information regarding the nanocopper fusing point,

measured at approximately 240 ℃.

5.4 TEM Analysis of Nanocopper Material

A TEM inspection was performed on unfused nanocopper material to analyze the nanoparticle properties. The images obtained from the TEM inspection are presented in Fig. 40.

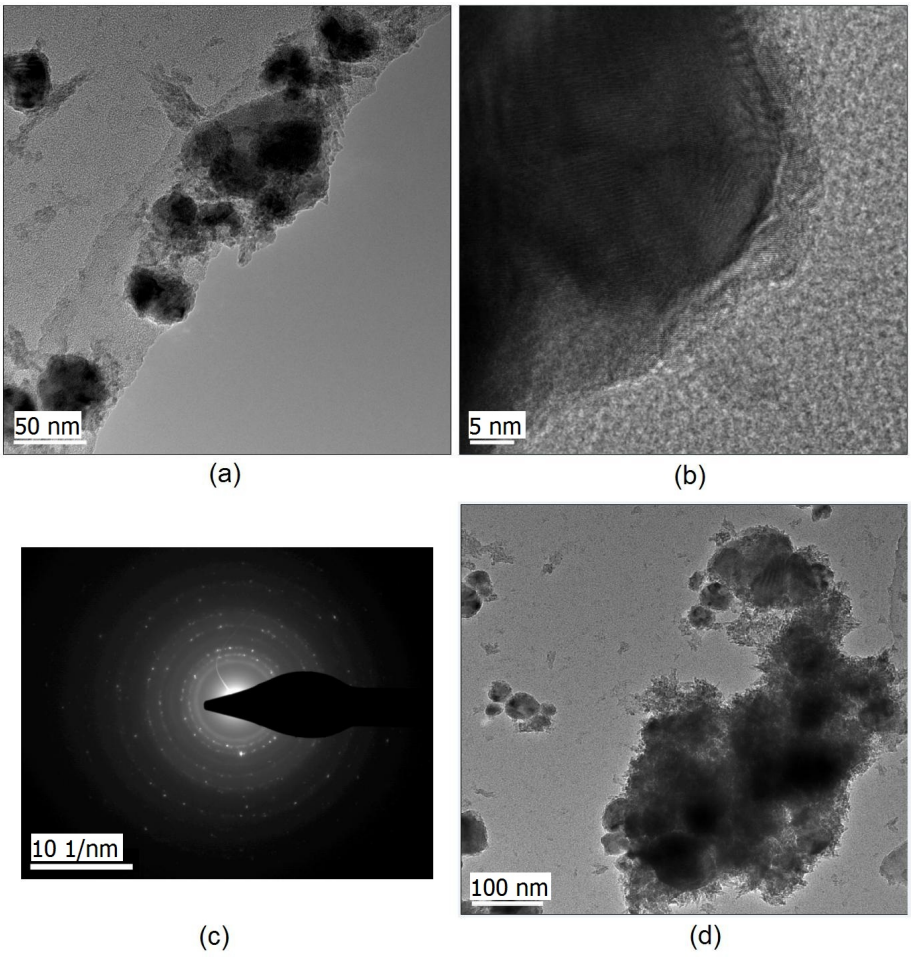

Figure 40: TEM images of unfused nanocopper: **(a)** nanocopper particles (dark areas); **(b)** nanocopper crystal lattice lines; **(c)** SAED pattern of nanocopper paste; **(d)** copper nanoparticles surrounded by solvents and surfactants.

The crystalline copper cores of the nanoparticles in the copper paste material are encapsulated in an organic shell acting as an oxidation barrier. The organic shell protects the copper cores from exposure to oxygen in air. An organic coating with surfactant molecules located on the surface of the organic shell prevents the agglomeration of the nanoparticles into larger entities [18]. The small size of the copper particles results in large surface areas, rendering the nanoparticles thermodynamically unstable. The amorphous structure of the organic shell leads to an activated high energy state, which increases the reactivity of the nanoparticles [51]. This is in contrast with the stable, low energy state of the nanoparticle copper core with a crystalline structure. The highly reactive nature of the organic coating is enhanced during the sintering process by the applied heat and pressure, increasing the surface energy states of the nanoparticles [51].

Under the applied pressure, the organic shell is compressed and deformed. Furthermore, the organic materials evaporate due to the increasing temperature during the sintering process, exposing the copper cores underneath and allowing them to interact with each other. The natural tendency of the electrons from atoms located on the copper core surfaces is to reach the lowest available energy state, which is the low energy level of bulk copper. This is achieved by forming metallic copper-copper bonds between the surface atoms of neighbouring nanoparticle cores brought into contact by the applied pressure and organic shell removal through evaporation. However, further research is required for a better understanding of copper-copper bond formation during the sintering process. The final result is an electrically conductive nanocopper material with strong metallic bonds between sintered copper structures separated by voids left by the evaporated solvents and other organic materials. The challenge is to increase the uniformity of the sintered nanocopper by minimizing the porosity caused by such voids and therefore increase the electrical conductivity by forming longer conductive paths along sintered nanocopper structures.

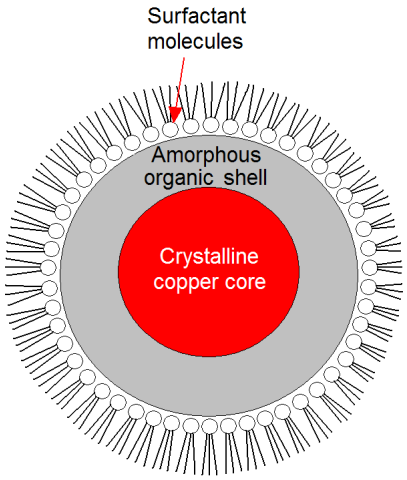

Figure 41: Schematic illustration of copper nanoparticle structure.

The TEM images show the copper nanoparticles as dark areas surrounded by lighter shades of grey representing the organic shell coating and surfactants. The dimensions of the encapsulating organic shell and surfactants is estimated to be in the range of 2-5 nm based on the TEM images in Fig. 40 (b). The solvent used to control the nanocopper paste viscosity can also be observed located between the nanoparticles in Fig. 40 (a).

Based on TEM inspection, the nanoparticles size is below 50 nm, with most particle dimensions being in the range of 10-30 nm. The high resolution image presented in Fig. 40 (b) shows the lines originating from planes in the atomic lattice, confirming the presence of copper atoms in a face-centered cubic crystal system.

A selective area electron diffraction (SAED) analysis, which is similar to X-ray diffraction (XRD), was performed on the nanocopper material. SAED utilizes the wave-like behaviour of electrons to generate diffraction patterns indicating the crystallographic structure of the sample material. The measured nanocopper diffraction pattern is presented in Fig. 40. The visible rings indicated the presence of crystalline copper in the paste material. Each ring corresponds to the electron diffraction in a crystalline plane. Due to the polycrystalline structure of the nanocopper, all the crystal orientations were visible simultaneously, resulting in the presence of multiple concentric rings in Fig. 40 (c). The ring structure illustrated in Fig. 40 (c) indicated the presence of crystalline copper in the nanocopper

material, confirming the expectation of crystalline structure of the copper nanoparticles.

The TEM analysis provided valuable results regarding the nanocopper material composition. The copper nanoparticle size was found to be in the range of 10-30 nm and the presence of oxide-preventing organic shell and surfactants was confirmed by the TEM imaging. Furthermore, the presence of crystalline copper cores inside the nanoparticles was confirmed both by the SAED analysis and the TEM images of copper crystal lattice lines. Additionally, based on the TEM analysis and the information on the nanoparticle structure provided by the nanocopper manufacturer [18], the applied pressure is expected to have a significant influence on the resistance of the nanocopper material. More specifically, increasing the applied pressure is believed to enhance the interaction and metallic bond formation between the copper cores, resulting in longer conductive paths and thus lower resistivity and contact resistance of the sintered nanocopper material.

5.5 TGA Analysis of Nanocopper Material

A thermogravimetric analysis (TGA) was performed on the nanocopper material used for the screen printing and bonding experiments in order to study the temperature dependence of the copper paste constituents. During the fusing process, the non-metallic componenents of the nanocopper paste such as solvents and organic surfactants will evaporate and be removed. Depending on the temperature the nanocopper is exposed to, an amount of non-metallic components such as water and organic solvents will be evaporated. By measuring the mass loss as a function of increasing temperature, valuable information can be extracted regarding the sintering process of the nanocopper material.

During the TGA analysis, the nanocopper sample was placed inside an oxygen free chamber containing nitrogen at atmospheric pressure. The lack of oxygen prevented the oxidation of the copper nanoparticles. The sample was heated at a constant rate of 10 ℃/min. The mass loss was recorded and is presented in Fig. 42 as a function of temperature.

There is a sharp drop in mass loss in the 25-125 ℃ range indicated by region I. This is believed to correspond to the evaporation of solvents in the nanocopper paste. Such solvents include water and other volatile adhesives like long chain organic alcohols [51]. The sample mass decreases from 100% to 85%. The mass loss will result in voids contributing to porosity of the nanocopper layer. The rate of mass loss decreases substantially and is almost constant within the 125-175 ℃ range in region II, which indicated no important change in the material composition through evaporation. The mass loss rate becomes higher from 175 ℃ to 220 ℃ in region III, which is attibuted to the evaporation of the organic surfactants coating the copper nanoparticles, based on the information provided by the nanocopper manufacturer [51].

The mass ratio drops to 81.5% at 220 ℃. After this point, the mass loss rate decreases significantly. Its non-zero value from 220 ℃ to 350 ℃ in region IV indicates that residues in the nanocopper material require higher temperatures to evaporate and be removed. These higher boiling materials are responsible for increasing the flow rate of the nanocopper paste and extending the time before the paste dries when applied on the substrate [51]. The mass ratio measured at 350 ℃ was 79%. No significant change is observed above 350 ℃ in region V. The final mass ratio at 550 ℃ was measured to be 78%. The 1% mass loss in region V is attributed to materials with high boiling points which are added to the paste to make its texture smoother in order to facilitate the paste dispensing process, as indicated by the nanocopper manufacturer Alfred Zinn [51]. The 20% mass loss around 250 ℃ is expected to lead to similar porosity values after nanocopper fusing as the solvents evaporate, leaving voids in the nanocopper material. Higher porosity values are possible due to bubble formation in the case of high temperature ramp-up rate during the nanocopper fusing process.

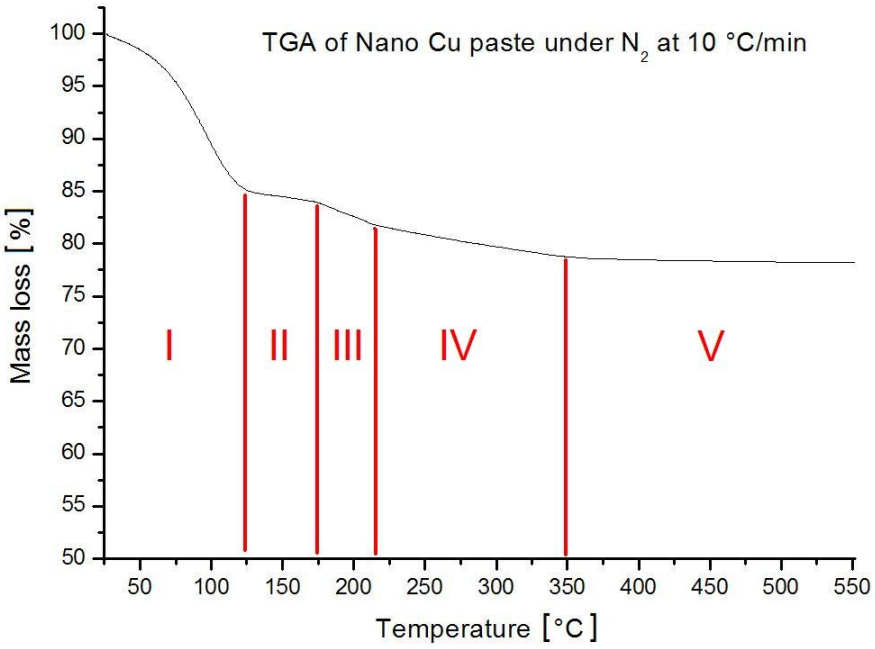

Figure 42: Nanocopper paste mass loss as function of temperature based on TGA analysis. Regions labeled I to V indicate different mass loss processes. The temperature ramp up rate was 10 °C/min.

Based on the recorded mass loss, several valuable conclusions can be inferred. A temperature above 125 ℃ was required in order to remove the solvents in the nanocopper material. **The organics coating the nanoparticles must also be evaporated in order for the sintering process to occur. This requires a temperature above 220 ℃.** After this point, the nanoparticle sintering process can occur once their surfactant coating has been removed. This result confirms the sharp resistance drop at 220 ℃ observed during the in-situ nanocopper fusing profile measurement. Increasing the temperature further above 220 ℃ increases the mass loss only marginally. The difference in mass loss between 220 ℃ and 550 ℃ is only 3.5%. This comes at the expense of a very large increase in the sintering temperature. Since the objective of the project was to develop a low temperature bonding process, a nanocopper sintering temperature in the range of 200-250 ℃ was selected based on the aforementioned results.

5.6 Die-to-die Bonding using Nanocopper Sintering

A die-to-die bonding experiment was conducted in order to study the bond characteristics of Cu-Cu bonding using nanocopper sintering. The prepared die samples were bonded under various conditions and the use of copper oxide-reducing agents was investigated. The bond strength and electrical contact resistance were recorded. The results were analyzed and utilized as a starting point for wafer-to-wafer bonding based on nanocopper sintering.

5.6.1 Sample fabrication procedure

The starting materials for this experiment were 100 mm single side polished silicon wafers. A metal stack of 0.75 µm Al, 100 nm Ti and 300 nm Cu was deposited on the substrate wafer using sputtering. The titanium layer was used as a copper diffusion barrier and to improve the adhesion of copper to the substrate. Finally, the wafer was diced using a saw blade into samples ranging from 2 mm × 2 mm to 10 mm × 10 mm to produce the dies needed for the bonding process.

The dies were cleaned with IPA, followed by rinsing in DI water to obtain a clean copper surface for nanocopper deposition. A separate batch of dies was placed in a 85% formic acid solution for 30 seconds in order to remove the copper oxide. After rinsing in DI water and drying, the dies were moved immediately to a pick & place machine for die attach using nanocopper.

A separate batch of die substrates was prepared by dicing to a depth of 30 µm into the silicon substrate to remove the metal stack, including the copper layer. This resulted in electrically insulating tracks 0.8 mm wide, which delimited the die into 4 distinct areas covered with the copper layer, as can be seen from Fig. 44. This separation was performed in order to fabricate distinct electrically conducting paths for measuring the contact resistance along the top die, substrate and nanocopper at the die attach interface.

A manual MECH-EL 772 pick & place machine was used to attach the top die to the substrate with nanocopper material. A small quantity of nanocopper was dispensed from a syringe needle with an inner diameter of 0.51 mm onto the substrate die followed immediately by placing the top die and applying a small amount of pressure. The applied pressure causes some nanocopper material to flow from the bond line to the outside environment. This excess material, known as the die attach fillet, formed an irregular layer on the substrate die along the top die sidewall, as can be seen from Fig. 43. The presence of the fillet indicated the formation of a macroscopic void-free uniform nanocopper layer between the top die and substrate during the die-attach process.

5.6.2 Die bonding process

The bonding was performed using an AML-AWB-04 aligner wafer bonder machine. The 2.5 mm top dies attached with nanocopper to the 6 mm substrate dies were placed between two 100 mm silicon wafers inside the wafer bonder. The bonding chamber was pumped down to a UHV pressure of 1.6 × 10^{-4} mbar. A bonding pressure of 10 MPa was applied to the dies. The samples were heated with a temperature ramp up rate of 20 ℃/min. Three different sintering temperatures were investigated: 200 ℃, 250 ℃ and 300 ℃. The dies were exposed to the sintering temperature for 30 min under UHV, followed by an annealing step at the same temperature using nitrogen at 1 bar for 30 min, while the applied pressure was maintained at 10 MPa. Finally, the chamber was cooled down to room temperature by venting it with nitrogen and the samples were removed and measured.

The bonding conditions for the bond strength and contact resistance tests are presented in Table 3.

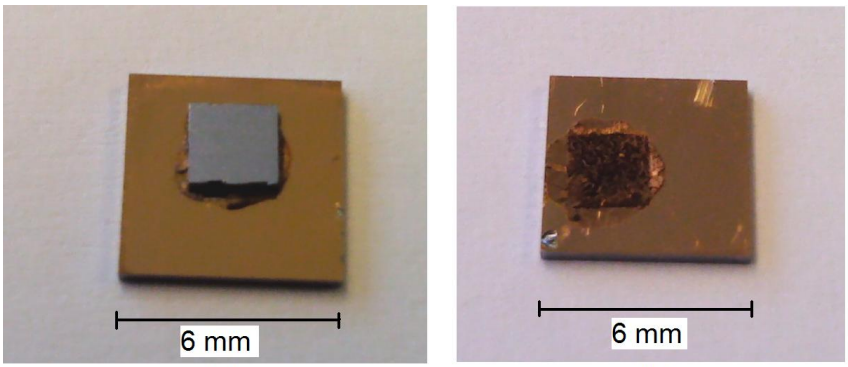

Figure 43: Bonded dies using nanocopper: **(a)** before shear test with visible nanocopper fillet; **(b)** after shear test with nanocopper visible at bond interface.

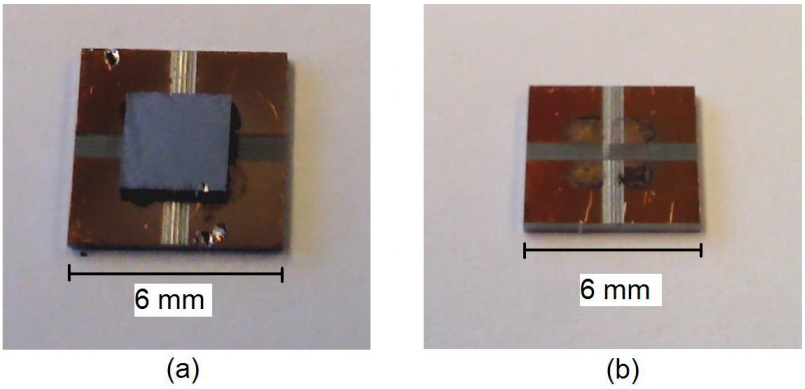

Figure 44: Bonded dies used for contact resistance measurements: **(a)** before shear test; **(b)** after shear test.

5.6.3 Contact resistance measurements

The bonded samples were measured by contacting the copper layer on the die substrate with probe needles. Only 2 of the 4 available insulated areas on the die substrate were contacted at any given moment, as illustrated in Fig. 45 (a). The current *I0* was forced through the copper layer on the die substrate. The current path is illustrated in Fig. 45 (b). The voltage drop was measured with contact probes and the values *V1* and *V2* along the current path indicated in Fig. 45 were measured and recorded. The measured resistance was calculated as the ratio between the measured potential difference *(V1 - V2)* and the forced current *I0*. Due to the lack of proper Kelvin structures, additional resistance values were measured. Thus, in addition to the bulk copper-nanocopper-bulk copper contact resistance, the bulk copper resistance on both the top and substrate dies along the current path were included in the measurement.

Table 3: Bonding parameters for die-to-die bonding tests.

Die size	Test type	Bonding pressure [MPa]	Bonding temperature [°C]
2.5 mm × 2.5 mm	Bond strength	10	200-300
3 mm × 3 mm	Contact resistance	10	200-300

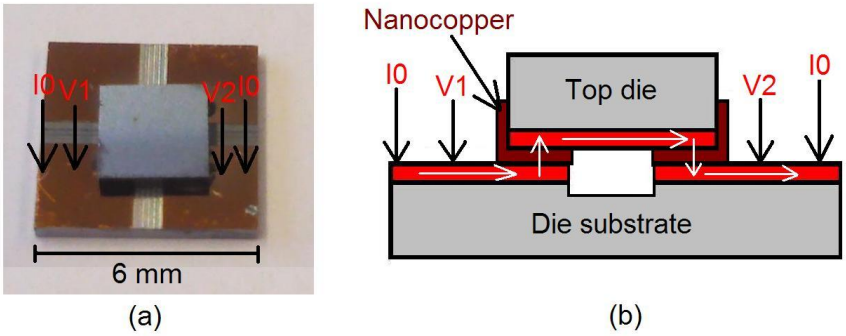

Figure 45: Bonded dies used for contact resistance measurements: **(a)** contact probe needle positions; **(b)** schematical cross-section with white arrows indicating electrical current direction.

A total of 10 die samples bonded with nanocopper at each of the 3 sintering temperatures were measured. The average value and standard deviations were calculated and the results are presented in Fig. 46.

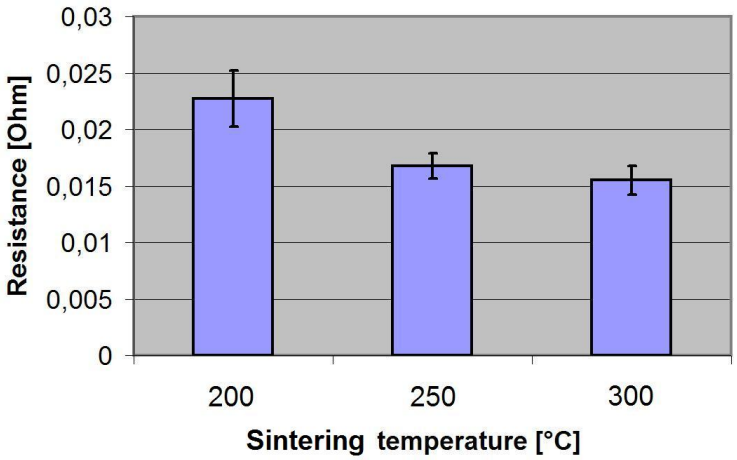

Figure 46: Contact resistance versus sintering temperature measurements for 3 mm dies bonded with nanocopper to 6 mm die substrates. Error bars indicate standard deviation on a sample size of 10 bonded dies.

As can be seen from Fig. 46 the resistance values decrease with increasing sintering temperature. This confirms the expectation that at higher temperatures the sintering process results in a lower resistance due to the higher surface energy of copper nanoparticles, which lead to the formation of fewer voids in the nanocopper material and at the bulk copper-nanocopper interface. Additionally, the organic shells of the nanoparticles evaporate at approximately 220 °C, enhancing the interaction and metallic bond formation between the copper cores and lowering the resistance. This is confirmed by the larger drop in resistance from 200 °C to 250 °C than from 250 °C to 300 °C in Fig. 46. In order to confirm this, a SEM analysis of the sintered nanocopper cross-section obtained using ion milling was performed, as described is subsection 5.6.4. Furthermore, the resistance drop is lower at higher temperatures. Based on the previous TGA analysis, this is attributed to the lower mass loss rate

above 250 ℃. This confirms the lack of a significant resistance improvement (lower value) at temperatures above 250 ℃. The lowest average resistance value obtained was 15.5 mΩ at 300 ℃. The lack of Kelvin structures makes this value not comparable to previous contact reistance measurements in subsection 5.2.3. Therefore, the results obtained should only be regarded as qualitative measurements giving an indication of the resistance as a function of fusing temperature. For quantitive values of the bulk copper-nanocopper contact resistance, please refer to the contact resistance subsection 5.2.3.

5.6.4 FIB and SEM analysis of nanocopper material and interfaces

A focused ion beam (FIB) was used to mill a cavity in the fused nanocopper layer from a 3 mm top die detached after the die shear test. The die sample was sintered at 250 ℃ for 30 min followed by 30 min anealling time under an applied pressure of 10 MPa. The experiment resulted in the fabrication of clean cavity sidewalls utilized for in-situ SEM analysis to obtain high resolution images of the bulk copper nanocopper interfaces and the structure of the sintered nanocopper paste.

The FIB milling of the cavity was performed using gallium ions. The ion beam milling resulted in the formation of a 5 µm × 15 µm cavity. The FIB milling removed approximately 15 µm of material in the following order starting from the sample surface:

- A sintered nanocopper layer approximately 350 nm thick.
- A 300 nm bulk copper layer obtained through sputtering.
- A 100 nm titanium layer as copper diffusion barrier.
- A 750 nm aluminium layer.
- 10-15 µm of the silicon substrate.

The SEM images obtained are presented in Fig. 47.

As can be seen from Fig. 47, the nanocopper particles have fused and formed connections to the bulk copper layer. The voids formed in the nanocopper material by the evaporated solvents are clearly visible in Fig. 47 (b-d) as dark areas. The copper nanoparticles accumulate and form clusters which fuse together to form continuous, void-free structures with dimensions up to 200 nm, as can be seen from Fig. 47 (c,d). Such structures with uniform density are expected to have excellent electrical characteristics, with conductivity close to that of bulk copper. However, the presence of voids at the boundaries of such structures is a limiting factor for the sintered nanocopper conductivity.

Furtheremore, the presence of voids at the nancocopper - bulk Cu interface is expected to result in a decrease of the shear bond strength. Only the nanoparticles which formed bonds to the copper atoms in the bulk Cu layer on the dies during the sintering process can contribute to the die bond strength. An estimation of the actual contact area was performed based on the SEM images in Fig. 47 of the interface cross-section fabricated using FIB milling. The dark areas present at the nanocopper-bulk Cu interface correspond to such interface voids, while the bright continuous areas across the interface correspond to bonds formed between the fused copper nanoparticles and bulk Cu atoms. The effective contact area was measured as the ratio between these continuous areas across the interface and the total interface area, with the obtained values being in the 50-60 % range.

The dark areas in Fig. 47 (b-d) caused by nanocopper voids were used to calculate the material porosity. Image processing software was employed to calculate the porosity value as the ratio between the void area and the total area of the nanocopper cross-section. The porosity values measured were in the 25-30% range. An example of such an image used to measure a porosity value of 26% is presented

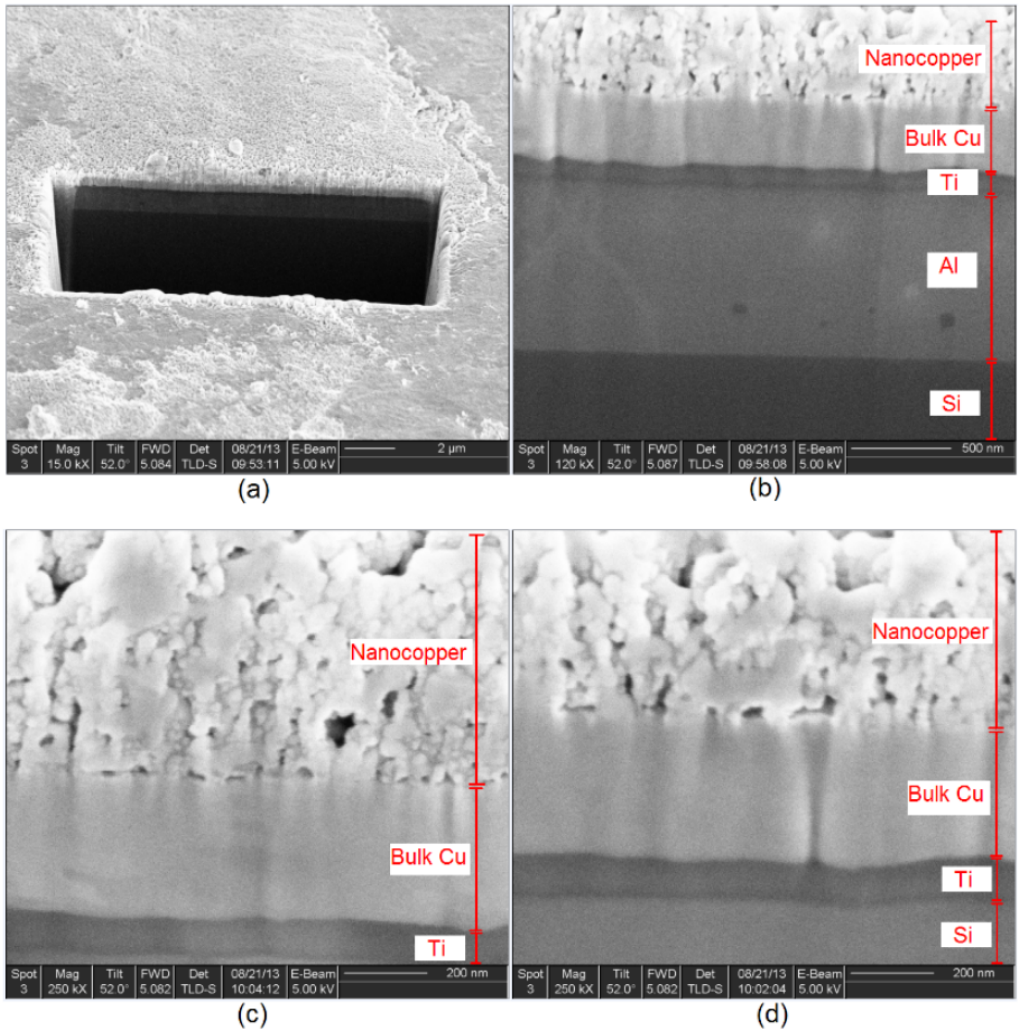

Figure 47: SEM images showing: **(a)** 5 µm × 15 µm cavity fabricated using FIB; **(b)** cross-section of metal stack (from top to bottom): sintered nanocopper, bulk Cu, Ti, Al, Si substrate; **(c)** bulk Cu-nanocopper interface; **(d)** sintered nanocopper structure; vertical lines in bulk Cu layer are SEM imaging artifacts casued by voids in the nanocopper layer.

in Fig. 48 (a). The sample was sintered at 250 ℃ while a pressure of 10 MPa was applied to it. An SEM image of a nanocopper sample fused at the same temperature of 250 ℃, but without applying external pressure is presented in Fig. 48 (b) for comparison. The latter sample was fabricated for the sheet resistance measurement experiment described in section 5.1.

As can be seen from Fig. 48, there is a significant difference in the fused nanocopper layer structure between the two samples. Applying an external pressure of 10 MPa resulted in a much lower porosity of 26% compared to 43% when no pressure was applied during the fusing process. Another sample of unfused nanocopper is presented in Fig. 48 (c) for comparison. The lack of FIB milling for the unfused sample made the porosity calculation challenging. A sidewall of a Kelvin structure present on the substrate was used for SEM inspection of the unfused nanocopper internal structure. This resulted in a non-uniform side wall used for the porosity measurements. Nevertheless, using the same method for porosity calculation, a much higher value of 61% was obtained for the unfused sample.

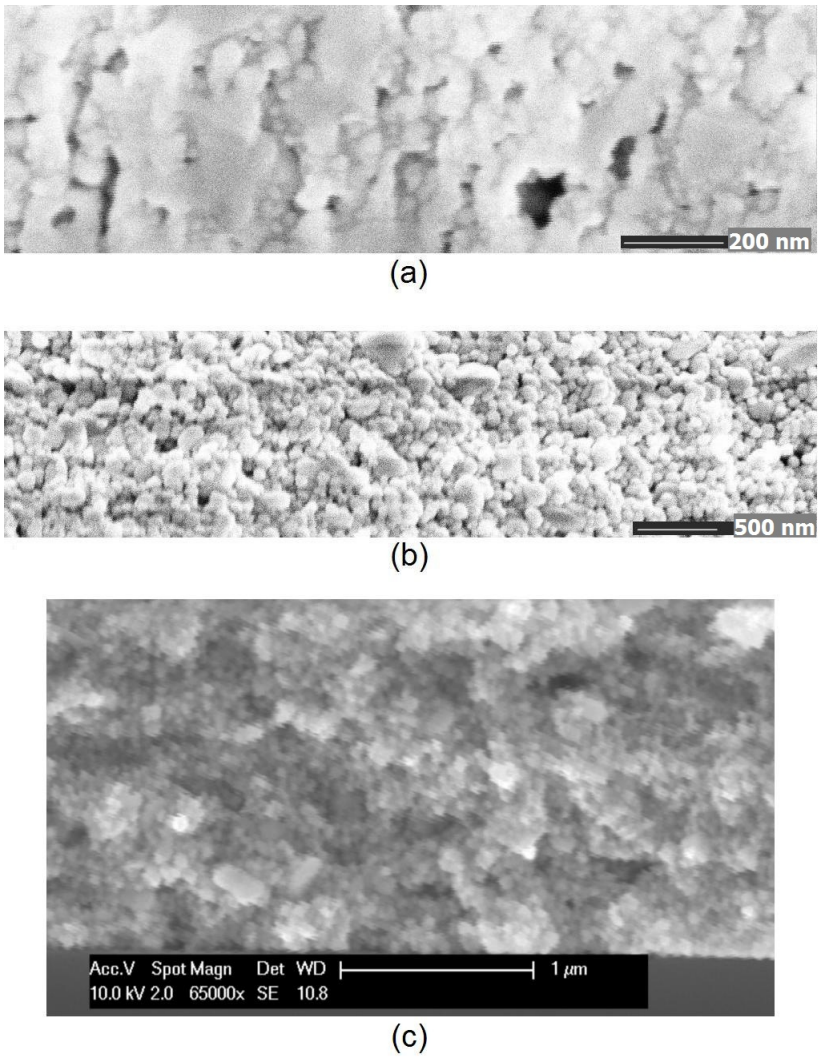

Figure 48: SEM images showing cross-sections of: **(a)** sintered nanocopper at 250 ℃ and 10 MPa applied pressure with 26% porosity; **(b)** fused nanocopper paste at 250 ℃ without any applied pressure with 43% porosity; **(c)** unfused nanocopper sample with a porosity of 61%.

The average particle size increased slightly by fusing the nanocopper at 250 ℃, as can be seen from Fig. 48 (b, c). However, applying an exernal pressure of 10 MPa drastically improved the sintering process, resulting in large 200 nm nanocopper structures.

5.6.5 Bond strength measurements

The bond strength of 2.5 mm × 2.5 mm dies bonded using nanocopper sintering to 6 mm × 6 mm substrate dies was measured using die shear tests. The procedure for die shear test measurements was explained in subsection 2.3.2. An example of a load-displacement curve obtained during the die shear tests is presented in Fig. 49.

As can be seen from Fig. 49, during an initial 1700 ms when the die shear tool head is travelling

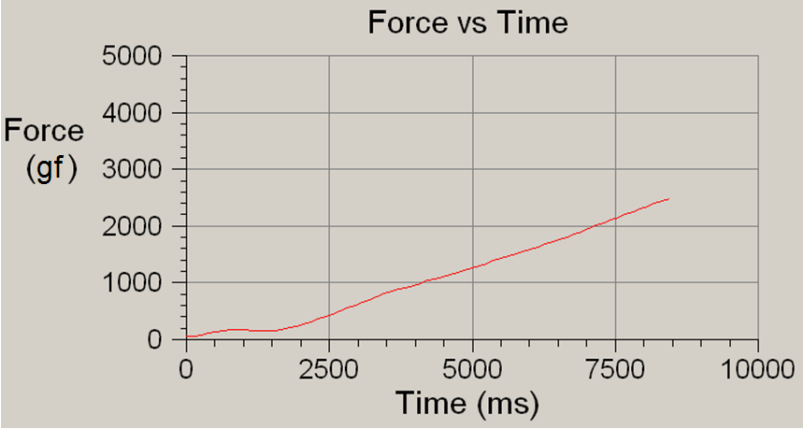

Figure 49: Load-displacement curve from die shear test measurements of 2.5 mm × 2.5 mm dies bonded using nanocopper sintering at 200℃. Die shear occurs at 2500 gram-force (gf).

toward the top die without contacting it, the force was constant and close to 0 N. When contact was made between the top die and the tool head at approximately 1700 ms, the measured applied force started to increase linearly with time. When the maximum shear force was reached, the top die detached from the substrate, at which point the force is no longer recorded because it decreases below the minimum threshold of 50 gf (gram-force). The maximum shear force is recorded by the machine and is used to calculate the shear bond strength according to Eq. 4.

The shear bond strength values of 2 mm × 2 mm dies bonded at temperatures of 200 ℃, 250 ℃ and 300 ℃ while applying an external force of 10 MPa were calculated. The obtained values for surface treatment with formic acid compared to reference samples cleaned only with IPA are presented in Fig. 50.

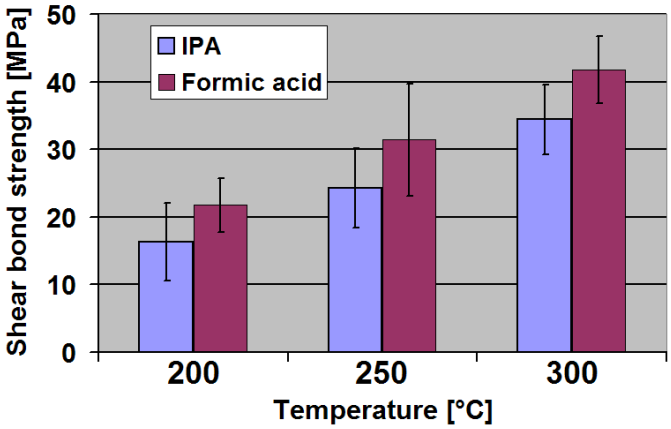

Figure 50: Bond strength as function of sintering temperature and surface treatment. Error bars indicate standard deviation on as sample size of 10 bonded dies.

As can be seen from Fig. 50, the shear bond strength increases with sintering temperature. This can be attributed to the enhanced fusing process of copper nanoparticles at higher temperatures, which resulted in the formation of fewer voids at the nanocopper-bulk Cu interface as well as in the

sintered nanocopper material. Therefore, a denser nanocopper material with a lower porosity and larger fused copper structures is able to withstand a larger shear force.

The samples treated with formic acid to remove the copper oxide showed a higher shear bond strength compared to reference dies cleaned only with IPA and bonded with nanocopper sintered under the same conditions. The lack of copper oxide on the die surfaces is expected to increase the adhesion of the sintered nanocopper to the die surfaces. During the nanocopper fusing process, bonds between the Cu atoms in the nanoparticles and the atoms in the bulk Cu layer on the die surfaces can form if enough surface energy is present and the atoms are in close proximity. However, a thin native copper oxide layer acts as a barrier preventing the realization of such atomic bonds. Therefore, the removal of copper oxide by the formic acid is able to improve the shear bond strength. However, a very thin native copper oxide will form during the bulk Cu exposure to air after formic acid treatment. This was unavoidable, as no setup for die attach in an oxygen-free atmosphere was available. The presence of native copper oxide on all dies explains the minor difference between the samples treated with formic acid and the reference dies. The dies treated with formic acid showed a 18-25% larger shear bond strength than the reference samples fused at the same temperature. The highest bond strength value obtained was 41.74 MPa for dies sintered at 300 ℃ after formic acid treatment.

5.6.6 Results and conclusions

The die-to-die bonding experiment was successful in providing valuable results regarding the mechanical and electrical properties of copper to copper bonding based on nanoparticle sintering. A detailed explanation of the die sample preparation for bonding including die attach was provided. The die bonding process was presented with focus on parameters relevant for optimizing the copper nanoparticle sintering such as sintering temperature and copper oxide reducing agents.

Resistance measurements were performed on dies bonded with sintered nanocopper. The qualitative results confirmed the expectation of increasing conductivity at higher temperature. This effected was attributted to the reduction in voids at the nanocopper-bulk Cu interface and to the enhanced nanoparticle fusing at higher temperatures.

The bond strength of bonded dies was evaluated based on die shear tests. A surface treatment with formic acid for removing copper oxide was investigated. The copper oxide reducing agent was successful in increasing the shear bond strength by providing a cleaner Cu surface for the nanocopper atoms to bond to. However, the formation of a thin copper native oxide during re-exposure to air was a limiting factor for the bond strenght. The highest measured shear bond strength value was 41.74 MPa, which is comparable values obtained using anodic bonding [52], eutectic bonding [47], solder-based bonding [6] and polymer bonding [48, 49] reported in the literature. A comparison between the shear bond strength values obtained using nanocopper sintering and selected values reported in the literature is presented in Fig. 51. However, the use of different die sizes and test conditions makes such comparison challenging. Therefore, further research is required for confirming the obtained die shear bond strength results.

Furthermore, silicon bulk failure of the top die was observed for very high forces above 25 kgf during the die shear process. This indicated a reliable connection with a very strong bond strength formed between the dies using the sintered nanocopper die-attach method.

Higher bond strength values are expected to be possible by reducing the interface voids at the nanocopper-bulk copper bond line. These voids effectively reduce the contact area between the sintered nanocopper and the bulk copper on the dies. Therefore, the actual contact area is lower than the die area used to calculate the shear bond strength values. An estimate of the real contact area

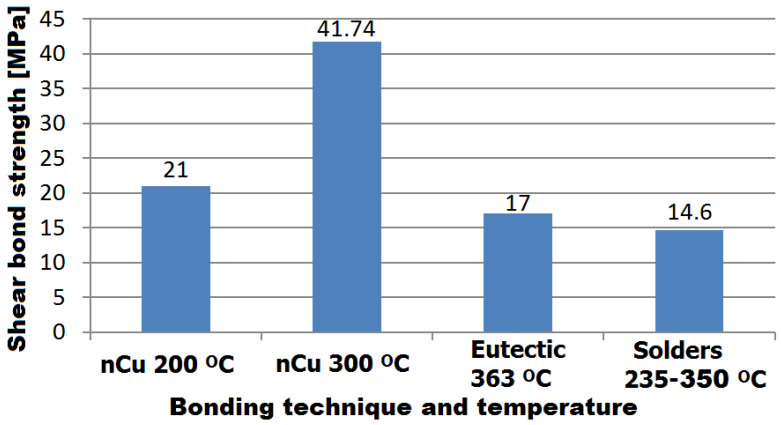

Figure 51: Shear bond strength values obtained using nanocopper (nCu) sintering compared to other bonding techniques [6, 47, 48, 49, 52, 53].

between the nanocopper and bulk copper on the die substrate was made based on visual inspection of the SEM images obtained from the FIB cross-section. Approximately 40-50% of the bond interface area was found to correspond to such voids. The porosity of the sintered nanocopper layer is expected to further decrease the shear bond strength by providing crack propagation paths along the boundaries of the voids in the nanocopper material. Therefore, considering the reduced effective contact area of the nanocopper-bulk copper interface, bond strength values comparable to that of silicon fusion bonding are expected to be obtained by future improvements to the nanocopper sintering process.

5.7 Wafer-to-wafer Bonding Experiment

The objective of the wafer-to-wafer bonding experiment was to develop and characterize 3D interconnect nanocopper vias fabricated between two wafer substrates using nanocopper sintering. CBKR structures for measuring nanocopper-to-bulk copper contact resistances are fabricated by patterning the bulk Cu top and bottom layers on the separate corresponding wafers, followed by nanocopper deposition and wafer bonding using nanoparticle sintering. The bulk silicon of the top wafer is removed by ething in a KOH solution, exposing the copper CBKR strucures for electrical contact measurements. The previous results and developed processes such as the sintering temperature of nanoparticles based on TGA analysis and in-situ measurements, the lithographically defined screen-printing of nanocopper and nanocopper-to-bulk copper interface SEM analysis are utilized to develop and optimize the wafer-to-wafer bonding process.

5.7.1 Sample fabrication procedure

The starting materials for this experiment consisted of 100 ± 0.2 mm double side polished monocrystalline p-type silicon wafers doped with boron with a resistivity of 2-5 $\Omega \cdot$cm and a (100) crystal orientation. The wafers used had a thickness of 525 ± 15 µm and a 0.2-0.4 nm RMS roughness on both polished sides.

The wafer front side was spin-coated with Shipley SPR3012 positive photoresist 1.4 µm thick using an EVG 120 coater/developer machine. A hexamethyldisilazane (HMDS) surface treatment was used to improve the adhesion of phororesist to the substrate. A soft photoresist bake at 95 ℃ for 90 seconds was performed to remove residual solvent. A subsequent exposure at an energy density of 150 mJ/cm^2 using an ASML PAS 5500/80 I-Line stepper was employed to transfer the alignment marks from the patterned chromium structures on the photomask to the photoresist on the wafer substrate. Both stepper marks for aligning future layers and AML bonder marks used to align wafes during the bonding process were exposed. A post-exposure bake (PEB) step at 115 ℃ for 90 seconds was performed to reduce the effect of standing waves produced in the resist layer during exposure. The exposed photoresist areas were removed during the development step using an MF322 aqueous solution of tetramethylammonium hydroxide (TMAH). A hard bake step at 100 ℃ for 90 seconds was utilized to further solidify the fabricate photoresist mask layer, increasing its durability for the subsequent processing steps. A quartz pen was used to manually label the wafers by inscribing their number in the developed photoresist layer next to the wafer primary flat. A schematic illustration of the fabricated photoresist mask for etching the alignment marks is presented in Fig. 52 (a). Optical microscope inspection of the developed photoresist layer confirmed that no resist residues were present in the exposed areas.

The **dry etching of the alignment marks** was performed using an Trikon Omega 201 machine. The wafers were etched using fluorine containing plasma under a vacuum pressure of 60 mTorr using an incident RF (radio frequency) power of 500 W. The total etching time for each wafer was 55 seconds, resulting in 120 nm deep alignment marks in the silicon substrate. The plasma-hardened photoresist was removed using oxygen plasma under vacuum in a Tepla resist stripper. An endpoint detection system was employed to calculate the processing time, followed by a 2 minute overetch. Organic residues were removed by wafer immersion from 10 min nitric acid (99% HNO_3), followed by rinsing in DI water. Metal contaminants were removed by immersing the wafers for 10 minutes in 65% nitric acid at 110 ℃ for 10 minutes, followed by rinsing in DI water up to resistiviy value of 5 M$\Omega \cdot$cm. Finally, the wafers were dried using a Semitool Avenger Basic 8-2 spin rinser dryer. A schematic illustration of the fabricated alignment marks in the silicon substrate is presented in Fig. 52 (b). The extensive cleaning steps described were performed to prevent furnace contamination during the subsequent silicon nitride deposition.

The **deposition of silicon nitride** was performed using a Tempress horizontal furnace. A gaseous mixture of dichlorosilane (SiH_2Cl_2) and ammonia (NH_3) was used during the low-stress LPCVD process at 850 ℃ for 43 minutes to obtain a 300 nm thick layer of silicon nitride on the wafer substrates. A low-stress deposition process was selected to prevent excessive bow of the wafers. The wafer flatness variation casued by the increased bow would have otherwise adversely affected the uniformity of the screen-printed nanocopper layer. A Leitz MVP-SP ellipsometry machine was utilized to measure the silicon nitride thickness with results being in the 300±5 nm range. The fabricated wafers with the silicon nitride layer on both sides are depicted schematically in Fig. 52 (c). The silicon nitride was used as part of the diffusion barrier against copper diffusion and as a stop layer for KOH etching of the top silicon wafer.

At this point, the substrates were separated into top and bottom wafers depending on their position during the bonding process. The top wafers were coated with 1.4 µm photoresist, exposed and developed using the same lithographic procedure described before. The exposed strucures were round-shaped **contact openings** with a diameter of 100 µm. During exposure, the structures were aligned to the marks previously etched in the silicon substrate.The developed photoresist mask is illustrated schematically in Fig. 52 (d).

The exposed silicon nitride was removed using a Alcatel GIR 300 F RIE (Reactive Ion Etching) etcher. A gaseous mixture of tetrafluoromethane (CF_4), sulfur hexafluoride (SF_6) and oxygen was employed to dry etch the silicon nitride completely from the back side of the top wafers. This was performed in orded to **expose the bulk silicon for the subsequent KOH etch.** The exposed silicon nitride areas in the photoresist contact openings on the substrate front side were partially etched, leaving a thin layer of approximately 10-20 nm of silicon nitride on the substrate as a stop layer for the KOH etch of bulk silicon. The etching process results in openings in the nitride layer for accessing the metal structures. **These 100 µm round structures were used later to contact the metal layers for resistance measurements after the bulk silicon of the top wafers was removed during KOH etching.** The etch time was carefully controlled based on the etch rate and previous measurements of the etched silicon nitride depth. The photoresist was later removed using oxygen plasma in a Tepla machine, followed by cleaning in nitric acid as previously described. Measurements of the unexposed/etched silicon nitride step height using a Veeco Dektak surface profiler machine were performed in order to accurately control the etch times. This was crucial in order to obtain a silicon nitride layer as thin as possible for the subsequent KOH etching. The silicon nitride layer needed to be thick enough to act as a stop layer for the silicon etch using KOH, but thin enough for easy removal to measure the contact resistance. Therefore, a 10-20 nm thickness range was selected, based on a compromise between mechanical robustness and ease of access to metal structures for electrical measurements. A schematical illustration of the etched contact openings in the silicon nitride layer is presented in Fig. 52 (e). No silicon nitride etching was performed on the bottom wafers.

Physical vapour deposition (PVD) was employed to **sputter a metal stacks of Ti, TiN and Cu** on the front side of both top and bottom wafers. After cleaning step using nitric acid and drying, the wafers were loaded in a Trikon Sigma sputtering machine. A 10 nm Ti layer followed immediately by a 40 nm TiN layer deposition under vacuum at 350 ℃ was performed. The immediate deposition of TiN under vacuum conditions ensured no native Ti oxide was formed during exposure to air to give rise to additional resistance of the metal stack. A subsequent deposition of a 500 nm Cu layer was performed at 25 ℃, resulting in a conformal layer of Cu/TiN/Ti layer on the top silicon wafers, as is presented schematically in Fig. 52 (f). The same metal sputtering procedure was performed on the bottom wafers.

The front side of both top and bottom wafers was coated with a 1.4 µm positive photoresist layer, followed by exposure and development. The patterned photoresist layer was used as a mask for wet

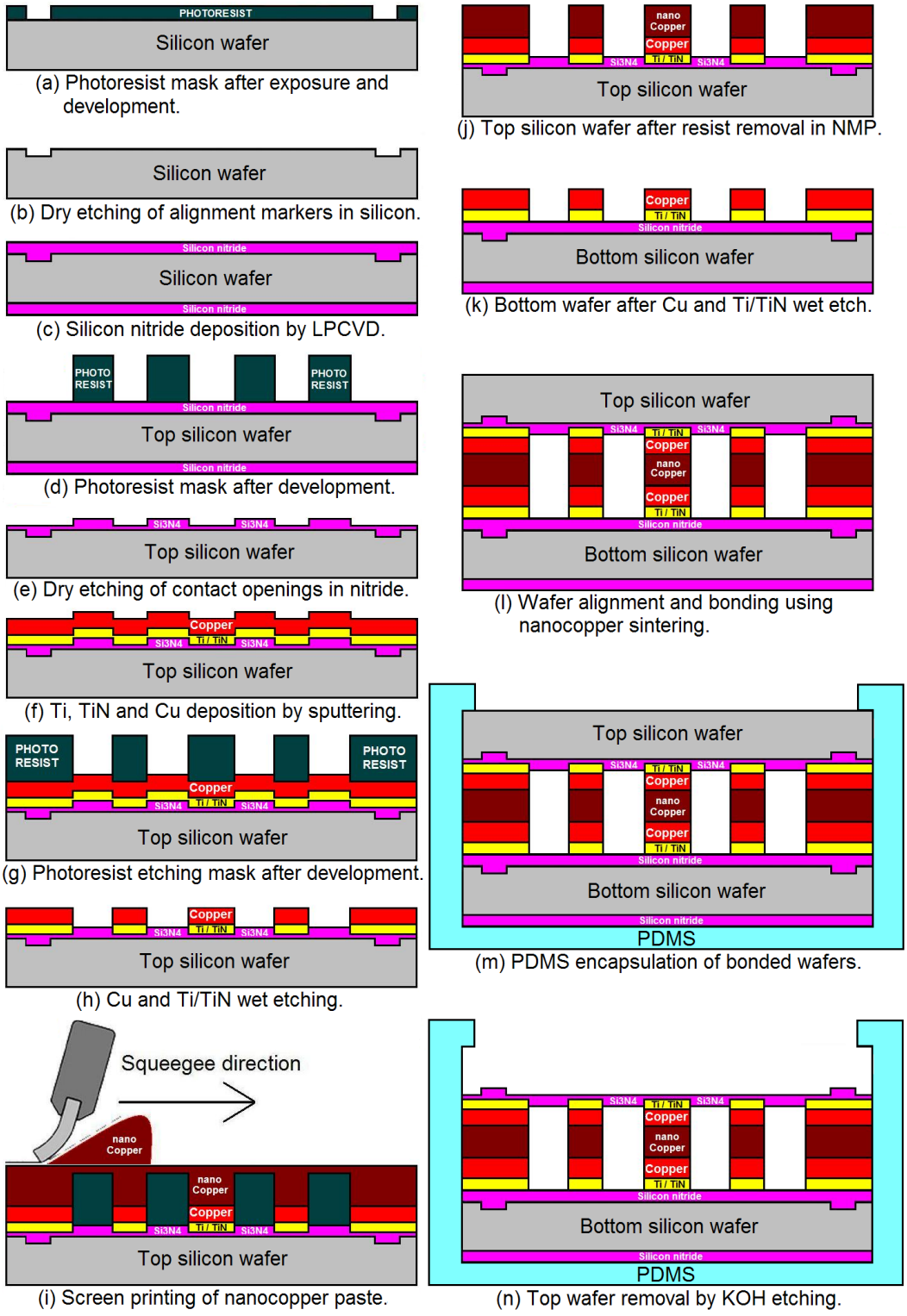

Figure 52: Fabrication sequence of wafers bonded with sintered nanocopper.

etching the Cu/TiN/Ti layers and is presented in Fig. 52 (g). The previously etched marks in the silicon layers were used to align the newly exposed structures to the contact openings in the nitride layer in the case of the top wafers. Furthermore, all the structures etched on the top wafers were **mirrored horizontally** to ensure the correct overlap with the ones on the bottom wafer during the subsequent bonding process. Additional 2 mm × 2 mm structures around the AML marks were exposed on both the top and bottom wafers. These structures were necessary to enable infrared wafer alignment in the bonder, as the infrared radiation cannot be transmitted through the Cu/Ti/TiN layers. The exposed metal areas were subsequently removed by wet etching, enabling IR inspection of AML marks used to align the wafers during the bonding process.

Using the developed photoresist mask, the **Cu layer was removed from the exposed areas by wet etching**. The wafers were immersed in an aqueous solution of sodium persulfate ($Na_2S_2O_8$) and sulphuric acid (H_2SO_4). The solution was kept at room temperature and stirred constantly to ensure an uniform etch rate across the wafer surface. A flash point corresponding to the exposure of the TiN layer after all the exposed Cu was etched was observed after 7.5 min. An overetch time of 1 min was used to remove any residual Cu on the wafers. After a subsequent rinse in DI water, the **wafers were immersed in a Ti/TiN etching aqueous solution** of ammonium hydroxide (NH_4OH) and hydrogen peroxide (H_2O_2). The exposure of the underlying silicon nitride layer corresponding to the flash point was observed as a change in colour after 4 minutes. An overetch time of 1 min was used to remove any residual Ti/TiN on the wafers. After rinsing in DI water for 10 minutes, the wafers were spin-dried. A careful inspection using an optical microsope revealed correct patterning of the metal layers without any significant underetch beneath the photoresist mask. A photoresist removal step was performed by immersing the wafers in an NMP solution at 70 ℃. The wafers were rinsed with IPA, ethanol and DI water and spin-dried. An optical microscope inspection confirmed that no photoresist residues were present on the wafer surfaces. A schematical illustration of the patterned metal layers after wet etching is presented in Fig. 52 (h).

The top wafers were coated with positive photoresist 2 µm thick. The photoresist was exposed using an energy density of 250 mJ/cm^2 by aligning to the marks etched in the silicon substrate, followed by development. The fabricated patterned photoresist layer acted as the **mask for screen-printing the nanocopper paste.** A 10 second immersion in the Cu etchant solution of $Na_2S_2O_8$ and H_2SO_4, followed by rinsing in DI water and spin-drying was performed to remove the copper oxide from the surface in preparation for the nanocopper deposition. The **screen printing process** was performed by dispensing a small quantity of nancopper paste on the wafer edge and spreading it manually across the wafer using the squeegee fill blade. The inclination angle between the squeegee blade and wafer plane was approximately 20°. The screen printing process was repeated several times in several directions across the wafer surface to obtain a uniform nanocopper paste layer. A moderate pressure was applied to the manual squeegee blade to prevent the depression and bulge effects explained in section 4.2. The screen-printed nanocopper layer is illustrated schematically in Fig. 52 (i).

The nanocopper paste was dried by placing the wafers on a hot plate at 50 ℃ for 5 minutes. The **photoresist lift-off process** was performed by immersing the wafers in NMP at room temperature under ultrasonic agitation for 1 minute, followed by further NMP immersion without ultrasonic agitation for 1 minute. The reduced exposure time to ultrasonic agitation was selected to prevent the damage to the nanocopper structure edges described in section 4.3. After rinsing with DI water and spin-drying, the wafers were subjected to optical microscope inspection which revealed no significant photoresist residues or unwanted nanocopper present outside the patterned structures. A schematic illustration of the patterned nanocopper layer is presented in Fig. 52 (j).

The patterned nanocopper structures consisted of round vias with 3 different diameters: 20 µm, 50 µm and 100 µm. The nanocopper vias were aligned to the 100 µm contact openings previously

etched in the silicon nitride layer. Examples of such nanocopper vias on bulk Cu are illustrated by the images obtained using a Leitz optical microscope presented in Fig. 53. The lift-off process resulted in clear patterning of the nanocopper vias with sharp edges, as can be seen from Fig. 53.

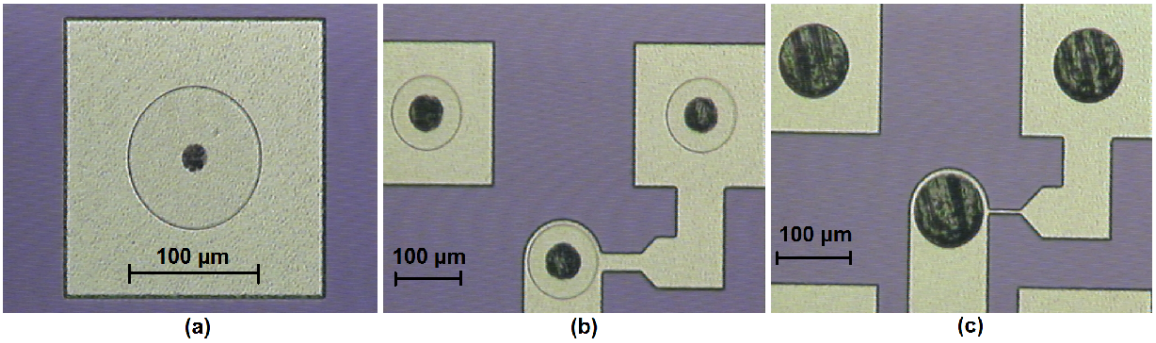

Figure 53: Nanocopper via structures (dark) on bulk Cu (bright) deposited on silicon nitride (magenta): **(a)** 20 µm via; **(b)** 50 µm vias and **(c)** 100 µm via.

Nanocopper was not deposited on the bottom wafer substrates. Before the bonding process, the bottom wafers were immersed in the Cu etchant solution for 10 minutes to remove the copper oxides and provide a clean copper surface for the nanocopper sintering process. A schematic illustration of the bottom wafers ready for bonding is presented in Fig. 52 (k).

The top wafers with the screen-printed nanocopper paste structures were transported after the lift-off process directly to the bonding chamber. The waiting time between the lift-off process and bonding using sintering was kept as low as possible in order to minimize the hardening and possible oxidation of the copper paste before the bonding process starts. The wafers were loaded in an AML-AWB-04 aligner wafer bonder machine and the bonding chamber was pumped down to a high vacuum pressure of 1.6×10^{-4} mbar. The top and bottom wafers were aligned using infrared (IR) radiation generated by IR bulbs located under the bottom wafer. The IR radiation is transmitted through the bulk silicon and silicon nitride layers and the AML mark images are captured by IR cameras. The AML marks are 100 µm × 100 µm cross-shaped structures located on the left and right sides of the wafer. The top and bottom wafers were brought within 0.1-0.2 mm of each other in order to have the AML marks from both wafers within focus. Careful alignment of the marks was performed, followed by applying approximately 500 N of force to contact the wafers. The AML marks on the top wafer are slightly larger, enabling the positioning of the bottom marks within within them to an accuracy of 2-5 µm. The accurate wafer alignment was important in order to fabricate the CBKR structures with a correct overlap of their corresponding top and bottom layers. The IR images of the marks before and after contact are presented in Fig. 54. No visible misalignment was observed when the two wafers were contacted.

After achieving wafer contact, the applied force was increased and maintained at 7500 N, while the temperature was increased to 250 ℃ using a ramp up rate of 15 ℃/min. The wafers were maintained at 250 ℃ under an applied force of 7500 N for 30 min for the nanocopper sintering process to develop. A subsequent annealing step under the same temperature and applied force conditions was performed using nitrogen at 1 bar. The nitrogen was used to provide an inert atmosphere during annealing. Finally, the wafers were cooled down to room temperature using nitrogen venting for approximately 1 hour. The bonded wafer pair is illustrated schematically in Fig. 52 (l). An IR imaging setup described in subsection 2.3.1 was used to inspect the alignment of the bonded wafers. As can be seen from the IR images in Fig. 55, there is no visible misalignment between the top and bottom wafers. Therefore,

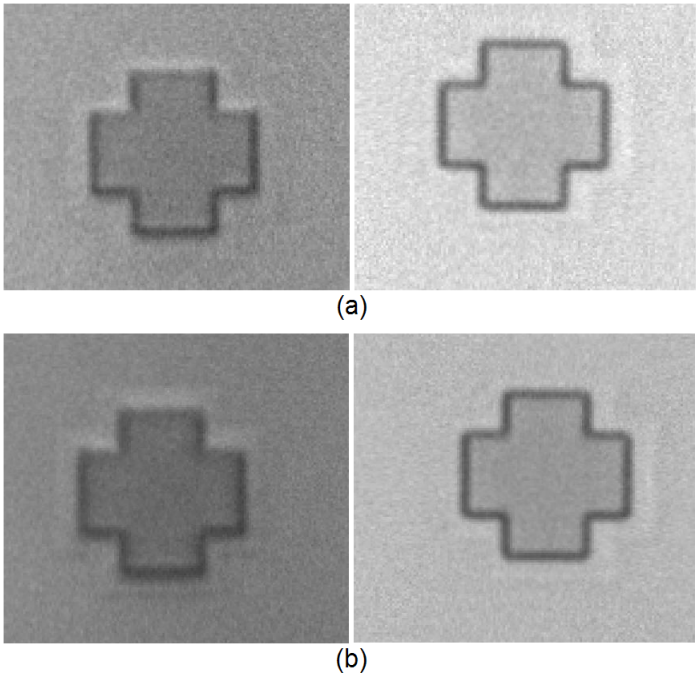

Figure 54: IR images of left and right AML marks: **(a)** before wafer contact; **(b)** after wafer contact. Dark crosses: bottom AML marks; surrounding brighter edges: top AML marks.

the successfully aligned bonded wafers were used for contact resistance measurements after top wafer removal by KOH etching.

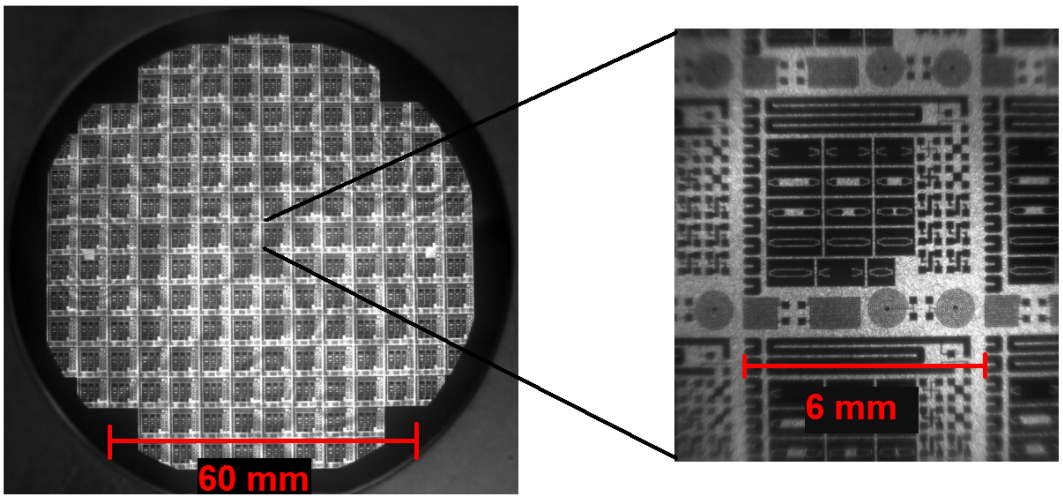

Figure 55: IR images of bonded wafers using sintered nanocopper. CBKR structures are visible in the magnified image on the right. Dark areas: metal layers opaque to IR radiation; Bright areas: bulk silicon and silicon nitride.

The bonded wafers were encapsulated in a polydimethylsiloxane (PDMS) material in order to protect the wafer edges against KOH infiltration to the bond interface. A 30 ml quantity of SYLGARD

184 silicone elastomer was mixed with 3 ml of SYLGARD 184 curing agent for 1 minute until a homogeneous viscous material was obtained. The mixture was poured over the bonded wafers placed in a plastic container. After a uniform layer of PDMS encapsulating the bonded wafer pair was formed, setup was placed in a Heraeus vacuum oven for curing. The PDMS was kept at 65 ℃ for 2 hours at atmospheric pressure in order to cure it. After cooling down to room temperature, the wafers were removed and the PDMS layer on the top wafer was cut and partially removed manually, as illustrated schematically in Fig. 52 (m). A 5 mm wide band of PDMS was left around the wafer edge to protect agains KOH infiltration to the bond interface.

In order to remove the top wafer, the bonded wafer pair encapsulated in PDMS was placed in a KOH solution with the back side of the top wafer exposed to the silicon-etching solution. A 30% KOH solution heated to 80 ℃ was utilized to etch the top wafer. The solution temperature was carefully monitored and an etch time of 6 hours and 7 minutes was calculated for the removal of the 525 µm of bulk silicon. The measured etch time was 6 hours and 15 minutes. The time difference is attributed to extra etch time for the native silicon oxide and any variations in temperature and KOH concentration. The final bonded wafer structure is illustrated schematically in Fig. 52 (n). Before the entire bulk silicon was etched, the contact openings for the largest structures were visible as dark areas against the characteristic grey color of silicon, as can be seen from Fig. 56 (a). After a subsequent 10 minute etch, all the bulk silicon was removed, exposing the metal contacts and silicon nitride layer, as can be seen from Fig. 56 (b).

Unfortunately, some KOH solution was able to infiltrate under the PDMS band around the wafer edge, as can be seen from Fig. 56. This can be explained by the KOH etching of the native silicon oxide layer present on the wafer surface before PDMS encapsulation. The etch reaction by-products include hydrogen gas. The gas trapped between the PDMS layer and substrate expanded and exerted pressure on the PDMS layer causing it to delaminate. Therefore, the KOH was able to infiltrate under the PDMS layer due to this delamination effect. One possible future improvement to this process is to deposit a silicon oxide layer on the back side of the top wafer and pattern a 5 mm silicon oxide band around the wafer edge by wet etching in buffered hydrofluoric acid (BHF). The silicon etch would be performed using TMAH, which does not etch silicon dioxide as KOH does. After PDMS encapsulation, a PDMS band narrower than 5 mm would be left to protect the wafer interface. Therefore, as no reaction between the TMAH and silicon dioxide takes place, no delamination of the PDMS layer should occur. Although a limited amount of KOH infiltration was present, the fabricated structures were not severely affected by it and contact resistance measurements were possible.

5.7.2 Contact resistance measurements

Standard CBKR structures were fabricated to measure the contact resistance of Cu-nanocopper-Cu interconnects between the bonded wafers. An example of a CBKR structure after top wafer removal by KOH along with a schematical cross-section illustrating the metallic layer configuration are presented in Fig. 57. The metal layers (Ti/TiN/Cu) present on the top wafer are visible in yellow-green color due to the light interference effects of a very thin (10-20 nm) Si_3N_4 layer covering the entire wafer. The presence of this layer along with KOH infiltration and any etch reaction by-products on the surface result in characteristic interference rings, as can be seen from Fig. 57 (a). The thicker Si_3N_4 regions covering the metal layer present on the bottom layer, as shown in Fig. 57 (b) have a specific purple color, which is visible in the areas marked by “Bottom” in Fig. 57 (a). The round 100 µm contact openings corresponing to the screen-printed nanocopper structures are also visible in Fig. 57 (a), along with contact probe needle positioned for measurements. The thin 10-20 nm silicon nitride layer above the contact openings was removed in the case of most structures due to the mechanical stresses occured during the KOH etch and the subsequent rinse in DI water and dry steps. Any silicon nitride remnants were removed by a careful scratch with the probe needle tips during

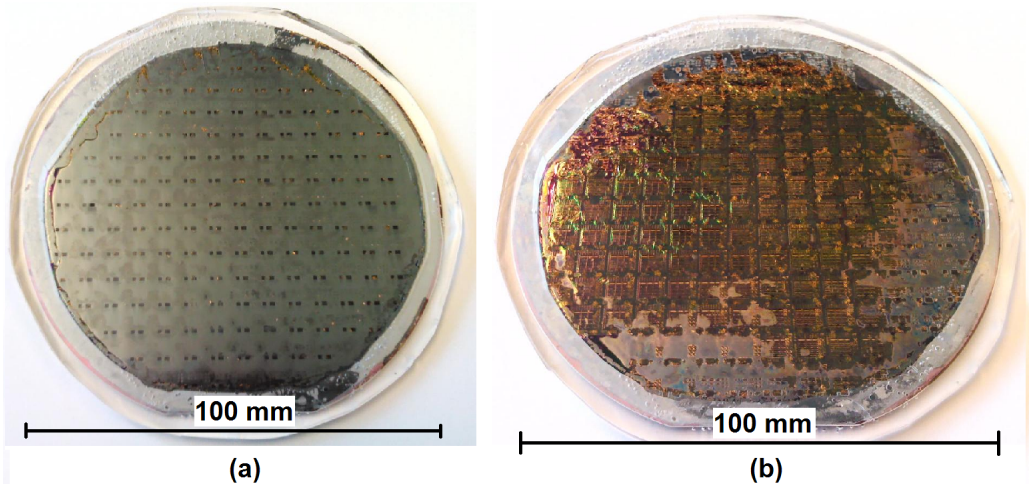

Figure 56: **(a)** Bonded wafer pair after partial KOH etch of top wafer; **(b)** Via openings in the top silicon wafer are visible.

contact resistance measurements.

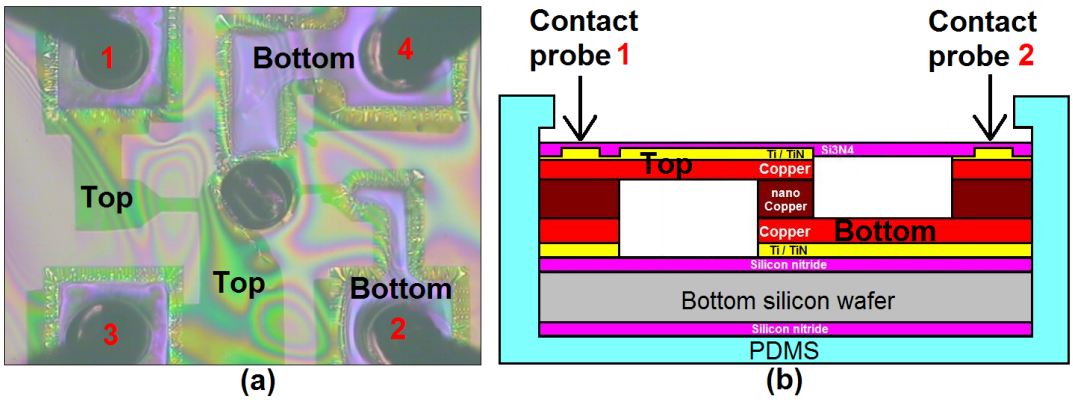

Figure 57: CBKR structure after top wafer etch in KOH: **(a)** "Top" indicates the metal layer covered by thin (10-20 nm) Si_3N_4 from top wafer. "Bottom" indicates the metal layer covered by thick (300 nm) Si_3N_4 on bottom wafer. Contact probe needles are visible. **(b)** Schematical cross-section of CBKR structure with corresponding probe contacts.

A current of 10 mA was forced between contacts 3 and 4, shown in Fig. 57. The current flowed from contact point 3 through the top metal layer and reached the Cu-nanocopper-Cu interconnect in the center of the CBKR structure. The voltage drop over the interconnect structure was measured between the top and bottom metal layers by contact probes 1 and 2 respectively. The recorded voltage potential difference was later used to determine the interconnect contact resistance. Finally, the current flowed from the interconnect structure to contact point 4, which corresponds to ground potential, completing the electrical circuit. Although the current flowed through an additional nanocopper interconnect structure between the bottom and top metal layers, as illustrated in Fig. 57 (b), the extra resistance did not affect the measurement. **The intrinsic advantage of the CBKR structure is a virtual 0 current flow between voltage sensing terminals 1 and 2.** Therefore, a zero current

flow through the bottom Cu/Ti/TiN layer and nanocopper interconnect generated zero additional resistance during the measurement. Furthermore, any asymmetries between CBKR structure components or contact resistances originating from the probe needles did not influence the measurement due to the same reason. The aforementioned effect makes the CBKR structure measurement by 4-terminal sensing an elegant method for accurately evaluating contact resistances.

CBKR structures containing nanocopper interconnects with diameters of 20 µm, 50 µm and 100 µm were measured on two separate wafer pairs bonded at 225 ℃ and 250 ℃. During each measurent, a current of 10 mA was forced between contacts 3 and 4 illustrated in Fig. 57 (a) and the voltage drop over the nanocopper interconnect was measured between contacts 1 and 2 respectively. A least square fitting of a linear function was employed to generate a correlation coefficient based on the 33 data points recorded from each measurement. The correlation coefficient values above 0.995 were assumed to correspond to reliable measurements which showed consistent results during multiple consecutive measurements of the same structure. The difference between a relatively low (0.995) and high (0.9992) correlation coefficient value is illustrated by the corresponding I-V data points in Fig. 58.

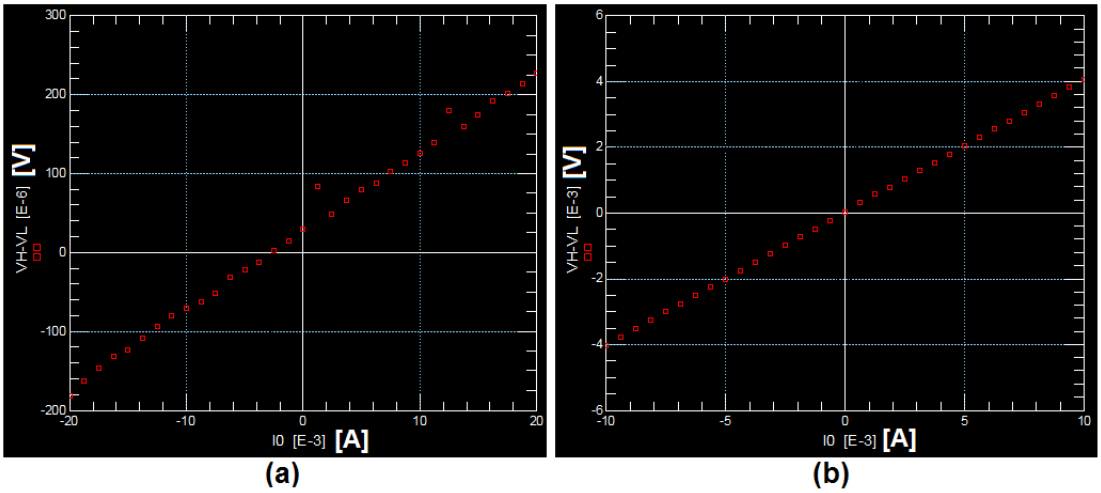

Figure 58: I-V data points from nanocopper via contact measurements with correlation coefficient values of: **(a)** 0.9946; **(b)** 0.9992.

The stray data points in Fig. 58 (a) correspond to electrical contact irregularities occuring during the measurement. Their origin includes variations in poor electrical contact between terminals 3 and 4 used for current forcing. The electrical breakthrough to the metal layer by partial burn-out of the thin silicon nitride layer is believed to contribute to these resistance measurement distortions.

The measured contact resistances for different nanocopper via diameters were averaged and the standard deviation was calculated using measurements from 10 samples per each via dimension and sintering temperature combination. The results are presented in Fig. 59 (a). As expected, the contact resistance is a strong function of the nanocopper via diameter. The larger nanocopper structure dimension offers a larger area for the electrical current to flow through, minimizing the contac resistance. Furthermore, the contact resistance was found to decrease at higher a sintering temperature. This can be explained by the enhanced fusing process of copper nanoparticles at higher temperature. The increased surface energy results in higher reactivity of nanoparticles, leading to a higher chance of forming Cu-Cu bonds between the nanocopper atoms and the ones in the bulk Cu layer. By providing a larger effective contact area between the fused nanocopper structures and the Cu layers on

the wafer surfaces, the enhanced sintering process at higher temperatures was able to minimize the contact resistance, as can be seen from Fig. 59. The average contact resistance was found to be 16.7% lower for the wafers bonded at 250 ℃ than at 225 ℃.

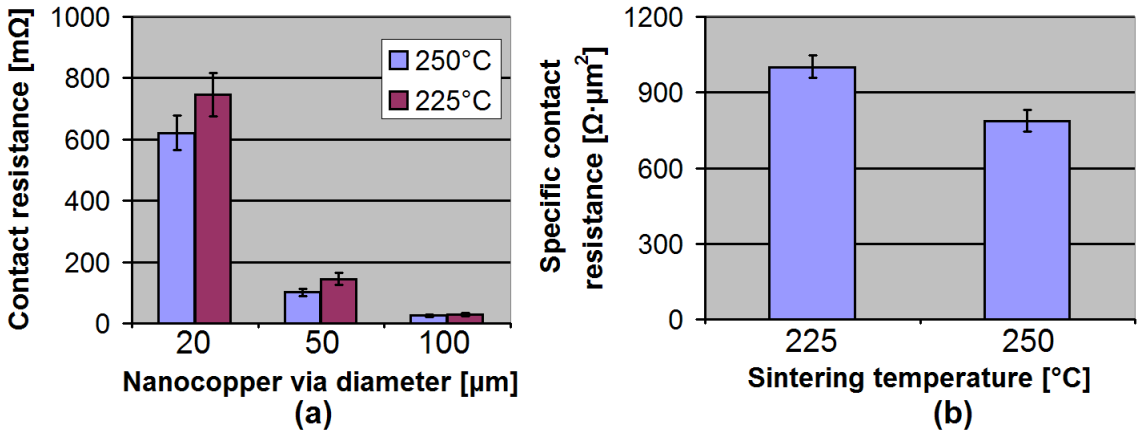

Figure 59: **(a)** Contact resistance as function of nanocopper via diameter for different sintering temperatures; **(b)** Specific contact resistance as function of nanocopper sintering temperature. Error bars indicate standard deviation.

The geometrical correction factor for CBKR structures reported in the literature [54] was not used for the calculation of contact resistances during this experiment. Its use was considered unnecessary and thus avoided in order to simplify calculations and also due to uncertainties related to nanocopper material deformation during bonding and CBKR structure damage during top wafer KOH etch.

The specific contact resistance was calculated by multiplying the contact resistance with the nanocopper via area. This value provided an indication of contact resistance independent of the nanocopper structure area. Using the specific contact resistance enabled a more reliable correlation between the sintering conditions and contact resistance. The calculated average values for the specific contact resistance as function of sintering temperature are presented in Fig. 59 (b). As expected, the specific contact resistance decreases with temperature due to the enhanced copper nanoparticle sintering process at higher temperatures described previously.

The specific contact resistance values obtained using wafer bonding were significantly higher than the ones measured on nanocopper screen-printed on bulk Cu CBKR structures in subsection 5.2.4. There are several factors contributing to this difference. In the case of CBKR structures fabricated using wafer bonding, two nanocopper-to-bulk Cu interfaces contributed to the contact resistance, through resistances *R1* and *R2*. Furthermore, the nanocopper via intrinsic resistance *R(nCu)* was added to the measured value. The schematic illustration of the aforementioned 3 resistances in series is presented in Fig. 60. Therefore, the measured contact resistance R_C is the sum of the intrinsic nanocopper resistance *R(nCu)* and the interface contact resistances R_{C1} and R_{C2}, as indicated by Eq. 9.

$$R_C = R_{C1} + R(nCu) + R_{C2} \tag{9}$$

The patterning technique employed resulted in clearly defined structures down to 5 µm lines, as can be seen from Fig. 31 (b).

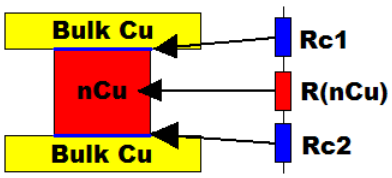

Figure 60: Schematic illustration of the nanocopper intrinsic resistance **R(nCu)** and nanocopper-to-bulk Cu interface contact resistances **Rc1 and Rc2**.

Furthermore and most importantly, the wafers were bonded after the nanocopper paste was dried at 50 ℃ before the photoresist lift-off process in NMP. The dried nanocopper layer resulted in a poor nanocopper-bulk Cu bond interface during the sintering process. A viscous nanocopper paste was able to flow across the wafer when external pressure was applied to it during the screen-printing process, forming a uniform layer on the substrate. This brought a large number of copper nanoparticles in close proximity to bulk Cu atoms to which they subsequently formed strong bonds during the sintering process. However, by drying, the nanocopper paste loses its viscous properties. The dry nanocopper surface had a high roughness and a rigid structure. Therefore, when this surface was pressed against the bulk Cu structure during the wafer bonding process, it was unable to flow and attach to the bulk Cu surfaces as was the case for the wet nanocopper paste. Therefore, the dried nanocopper material was not able to form strong bonds with the atoms in the bulk Cu layer during the sintering process, resulting in a lower number of conducting paths and therefore increased contact resistance.

Another important factor was the introduction of significant stresses to the bond interface during the wafer bonding process which caused damage to the CBKR structures and nanocopper-bulk Cu interfaces. By applying a high external force of 7600 N to the bonded wafers, severe mechanical stress was exerted on the CBKR due to height differences between different structures at the bond interface. The high roughness of the dried nanocopper layer added to this effect. This mechanical stress lead to crack formation in the silicon bulk close to the bond interface. Such cracks, visible in Fig. 61 (b) later constituted infiltration paths for the KOH solution during wet etching of the bulk silicon from the top wafer.

The removal of the top wafer by KOH etching further aggravated the issue. The metal layers from the top wafer were exposed for electrical measurements, resulting in fragile structures vulnerable to delamination. Thermal stresses during removal from the 80 ℃ silicon etch solution and KOH infiltration at the bond interface resulted in delamination effects observed between the two metal layers of the CBKR structures. Furthermore, mechanical stresses caused by probe contacts during 4-terminal sensing measurements correlated with fragile top metal layer structures resulted in damage to the nanocopper vias and nanocopper-bulk Cu interfaces. The end result of these effects was a significantly higher specific contact resistance in the case of CBKR fabricated by wafer bonding.

5.7.3 Nanocopper structure and interface characterization

In order to inspect the nanocopper structure and bond interfaces after the sintering process, a pair of bonded wafers was diced using a 80 µm saw blade. The obtained 2 mm wide sample was placed inside a Philips SEM XL-50 machine for cross-section measurements of the bond interface.

Although FIB milling is able to produce a much cleaner cross-section, the high wafer thickness (525 µm) made the FIB technique impractical for this experiment. The dicing procedure resulted in limited damage to the sample cross-section, but its effects did not prevent the inference of valuable

conclusions from the SEM image inspection and measurements.

An SEM image of the cross-section giving an overview of the bonded wafers and the bond interface is presented in Fig. 61. The two separate wafers along with their bond interface are visible in Fig. 61 (a). The image of the bond interface in Fig. 61 (b) revealed important information regarding the wafer bonding process effect on the bulk silicon. Large cracks in the bulk silicon are visible in a 25 µm range from the bond interface in the top wafer. Their origin is believed to be mechanical stress caused by height differences between different layers at the bond interface, as was explained previously. Futhermore, a delamination can be observed at the nanocopper-top wafer interface. This can be explained by the poor adhesion and lack of bond formation between the dry nanocopper material and bulk Cu surface, as was described previously.

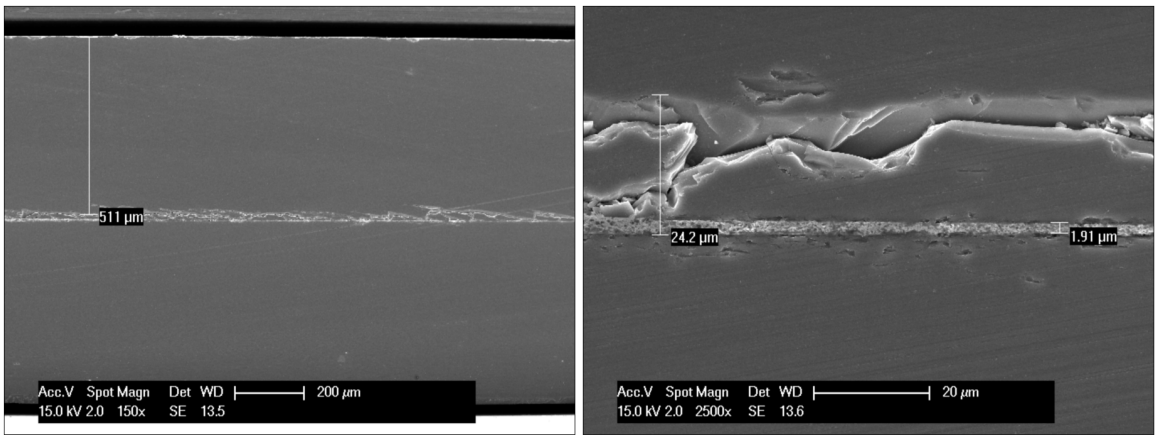

Figure 61: SEM cross-section images of: **(a)** bonded wafer pair overview; **(b)** bond interface with sintered nanocopper and bulk silicon voids and cracks.

The sintered nanocopper layer height was measured to be in the 1.5-2.5 µm range. SEM images of the sintered nanocopper particles are presented in Fig. 62. A significant change in the nanocopper structure was observed compared to the unfused nanocopper illustrated in Fig. 63. The nanocopper sintering process resulted in the formation of large copper structures up to 1 µm in size, as can be observed from the measurements in Fig. 62 (a).

The nanoparticle sintering process was able to transform the small unfused nanoparticles with dimensions in the 50-100 nm range, as can be seen from Fig. 63 (b) into 1 µm structures. The large sintered nanocopper structures are expected to have electrical conductivity values close to that of bulk Cu. The voids present between their bondaries are an important limiting factor for the conductivity of the nanocopper interconnects. Therefore, lowering the amount of voids in the nanocopper and obtaining larger sintered nanocopper structure dimensions was a worthwhile goal for the current project.

An estimate of the nanocopper material porosity was made using ImageJ image processing software. Using the same upper and lower grayscale thresholds for both images, the porosity was calculated as the ratio between the dark areas corresponding to voids and the total cross-section area. The values obtained for unfused and sintered nanocopper material were 62% and 28%, respectively, as can be observed from Fig. 64. The significant porosity reduction was correlated with a densification of the nanocopper layer during the sintering process. This effect, together with the formation of large fused nanocopper structures from 750 nm to 1 µm resulted in long-range conductive paths leading to a

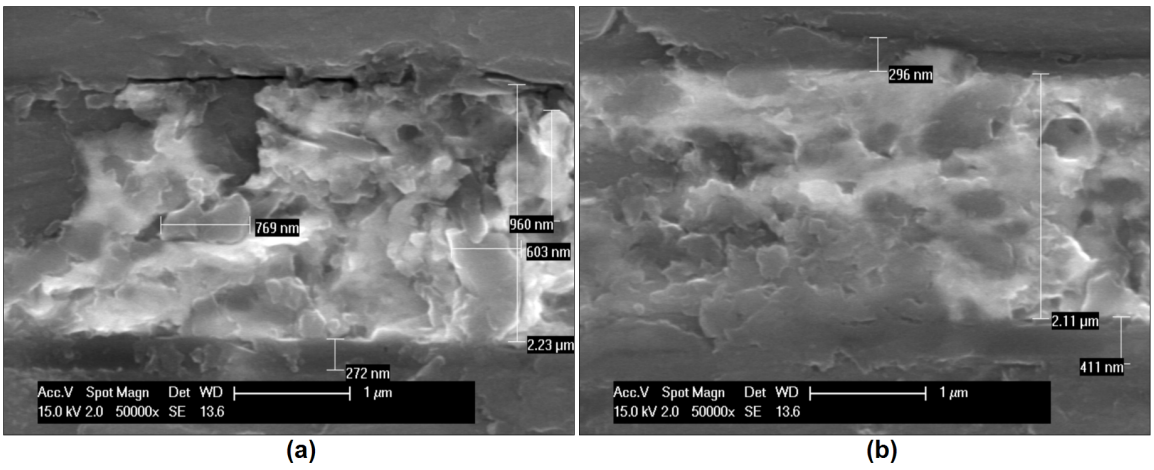

Figure 62: SEM cross-section images of copper nanoparticles sintered at 250 ℃: **(a)** delamination visible at interface with top wafer; **(b)** measured heights of metal stacks on top and bottom wafers.

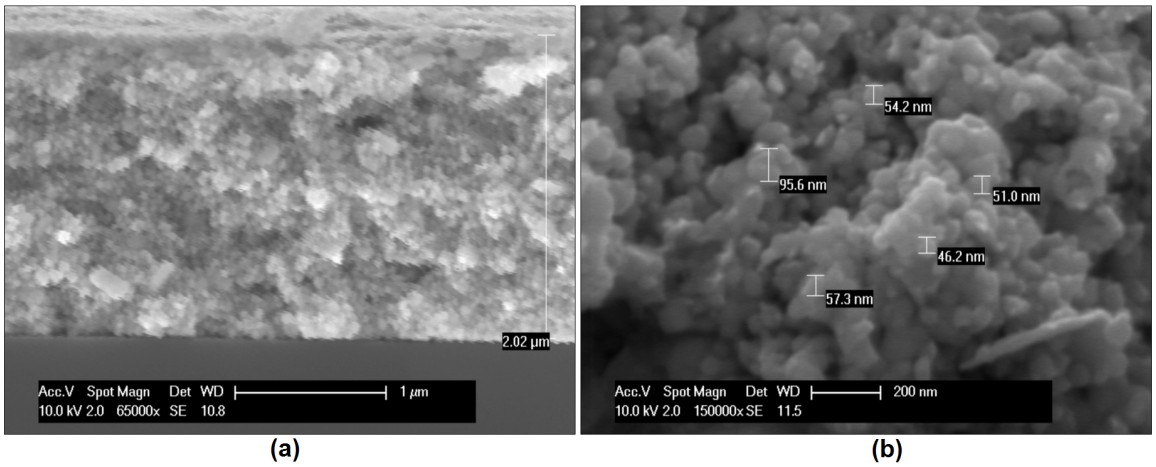

Figure 63: SEM image of unfused nanocopper structure: **(a)** overview; **(b)** high magnification image with measured nanoparticle dimensions.

substantial decrease in sheet resistance. This was confirmed by electrical sheet and contact resistance measurement values in the MΩ range for the unfused nanocopper. After the sintering process, the resistance reduced drastically, as confirmed by the measurement results of the sintered nanocopper material. Furthermore, the formation of continuous copper structures across the nanocopper-bulk Cu interface visible in Fig. 62 resulted in a reduction of contact resistance by increasing the contact area between the nanocopper and bulk Cu layers.

5.8 Conclusions

The wafer bonding experiment based on nanocopper sintering was successful in the development, fabrication and test of the nanocopper interconnect vias for 3D integration applications.

Using the lithographically defined screen printing method desctibed in chapter 4, van der Pauw

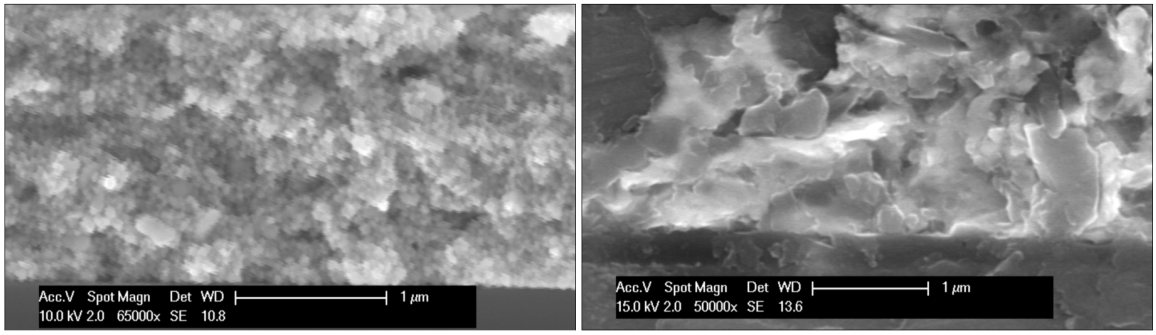

Figure 64: SEM images used for porosity measurements: **(a)** 62% porosity for unfused nanocopper; **(b)** 28% porosity for sintered nanocopper.

nanocopper structures were fabricated in order to measure sheet resistance. The sample fabrication procedure and the nanocopper fusing parameters were explained in detail with focus on minimizing the copper oxidation. The variation of nanocopper resistivity with temperature was measured and explained. The lowest nanocopper resitivity value obtained was 9 times higher than the theoretical value for bulk Cu. The resistivity value measured after fusing the nanocopper at 200 ℃ was approximately 6 times lower than the value reported in the literature for nanocopper thin films fused at a similar temperature [55], showing promising results for high conductivity 3D copper interconnect fabrication.

The realization of CBKR structures for the nanocopper-to-bulk copper contact resistance experiment was explained along with the fusing profile conditions. The 4-terminal measurements of CBKR structures were documented. The lowest value for the specific contact resistance of 0.227 $\Omega \cdot \mu m^2$ was obtained at a fusing temperature of 240 ℃. This resistance is comparable with the 0.15 $\Omega \cdot \mu m^2$ value reported in the literature for Cu-Cu thermocompresion bonding at 400 ℃ after soaking in HCL to remove the copper native oxide [25]. Therefore, a significant fusing process temperature reduction of 200 ℃ was achieved while obtaining comparable contact resistance values.

In order to study the fusing profile of the nanocopper material, an in-situ experiment focused on measuring resistance variation with temperature was conducted. The sample fabrication procedure was explained along with the fusing conditions. The measurement results provided valuable information regarding the fusing point of the copper nanoparticles. A sharp resistance drop was measured corresponding to the nanocopper fusing point at 240 ℃. The prolonged exposure to lower fusing temperatures did not affect the resistance, confirming the above-mentioned fusing point. Furthermore, the fusing process was found to be irreversible, with no significant increase in resistance after the sample was cooled down to room temperature.

A TEM analysis of the unfused nanocopper material was conducted in order to investigate its nanoparticle structure. The TEM images of the nanocopper material revealed valuable information regarding the nanoparticle dimensions and the organic surfactants. The unfused copper nanoparticle size distribution was found to be in the 10-30 nm range with the organic surfactants acting as an effective barrier against particle conglomeration before the evaporation of organics during the sintering process at 240 ℃. The SAED pattern in Fig. 40 (c) confirmed the crystalline structure of the copper nanoparticles.

A TGA analysis of the nanocopper material was conducted in order to further analyze the nanoparticle fusing point. The nanocopper mass loss rate was recorded as function of temperature. The evap-

oration of different solvents and organic surfactants in the nanocopper material was correlated with their boiling temperatures and the mass loss profile was separated into distinct temperature regimes accordingly. The nanocopper fusing range of 200-250 ℃ was selected as a trade-off between mass loss rate and low temperature processing objective.

The die-to-die bonding experiment was conducted in order to study the bond strength and electrical characteristics of dies bonded using sintered nanocopper in preparation for the wafer bonding experiment based on a similar technique. The die fabrication method was explained in detail and the die attach using a pick & place machine was described. The die bonding parameters were documented. The contact resistance of bulk Cu-nanocopper-bulk Cu was measured as function of fusing temperature. Although no quantitative values were measured due to the lack of CBKR structure, the decrease of contact resistance with fusing temperature was confirmed.

The sintered nanocopper structure was investigated along with the nanocopper-bulk Cu bond interface using FIB milling and SEM analysis. A cavity was fabricated in the substrate die covered by the sintered nanocopper layer using FIB milling. The cavity sidewall was used to obtain cross-section SEM images of the sintered nanoparticle structure and bond interface. The SEM measurements provided valuable information regarding the fused copper structures and the nanocopper-bulk Cu interaction at the bond interface. Large fused nanocopper structures up to 200 nm were measured and continuos copper structure were visible across the bond interfaces, indicating the formation of metallic bonds between the nanocopper and bulk Cu atoms. These high-strength bonds were expected to provide reliable connections, as was confirmed by the shear bond strength tests. Furthermore, these measurements were used to obtain estimations of the effective nanocopper-bulk Cu contact area. Finally, the porosity of the sintered nanocopper layer was measured using image processing software. Significant changes in nanocopper porosity were measured for different states such as unfused, fused without pressure and sintered nanocopper using 10 MPa of external pressure. Sintering under applied pressure produced the lowest porosity value of 26%.

Die shear tests were performed on 2.5 mm square dies bonded with nanocopper to a silicon substrate covered with a sputtered bulk Cu layer in order to measure their bond strength. The effect of sintering temperature and surface treatment with formic acid for copper oxide removal were investigated. The copper oxide reducing agent treatment produced shear bond strength values 18-28% larger than for samples treated only with IPA at the same sintering temperatures. The difference can be explained by the enhanced fusing of copper nanoparticles with atoms in the bulk Cu layer when the copper oxide is removed. The higher shear bond strength values measured for larger sintering temperatures was attributed to the increased interaction of nanoparticles at high temperatures, which resulted in the formation of large copper structures and increased effective Cu-Cu contact area at the interface, as confirmed by the SEM analysis of the FIB milled sample. The highest shear bond strength obtained by nanocopper sintering at 300 ℃ was 41.74 MPa, which was substantially higher than values reported in the literature for solder bonding, eutectic and anodic bonding. This value showed promising results for high-strength die bonding based on nanocopper sintering.

The wafer-to-wafer bonding experiment based on nanocopper sintering was successful in demonstrating the fabrication of patterned nanocopper interconnects for 3D applications. The valuable information gathered during the lithographically defined nanocopper structures, nanocopper sheet and contact resistances, fusing profile and die bonding experiments previously presented was used during the wafer-to-wafer bonding experiment.

The wafer sample fabrication procedure was explained in detail, including the nanocopper screen printing and top wafer removal by KOH etching to access the CBKR structures for electrical measurements. The wafer bonding process was described and the IR inspection of bonded structures

confirmed their correct alignment. The contact resistance measurement of CBKR structures exposed after KOH silicon etching was described. The measurement results based on reliable ohmic contacts with CBKR probe contact pads were used to calculate the specific contact resistance of the fabricated nanocopper via interconnects. The obtained values were higher than the ones previously obtained by screen-printing the nanocopper on bulk Cu structures. The increase in contact resistance was explained by the poor interaction of dry nanocopper material with the bulk Cu layer during the sintering process. Additional factors included the double nanocopper-bulk Cu interface, the additional nanocopper via intrinsic resistance and the damage sustained by the CBKR structures during the bonding process and KOH bulk silicon etch. Despite the higher resistance values, the realization of electrically condcutive nanocopper wafer-to-wafer interconnects within the 200-250 ℃ range has shown very promising results for the low temperature fabrication of 3D copper interconnects.

The sintered nanocopper structure and nanocopper-bulk Cu interface were inspected using SEM imaging of cross-sections obtained using dicing. Significant cracks in the bulk silicon layer of the top wafer close to the bond interface were observed. The origin of the silicon cracks was explained based on the mechanical stresses associated with height differences between different structures at the bond interface. The delamination between the nanocopper layer and top wafer surface confirmed the poor adhesion and fusing between the dried nanocopper and bulk Cu layers. The formation of large Cu structures up to 1 µm by copper nanoparticle fusing was confirmed from the SEM images. The change in nanocopper porosity was measured using ImageJ image processing software on the SEM cross-section images. The sintering process resulted in porosity reduction from 62% for unfused nanocopper to 28% for nanocopper sintered at 250 ℃. Furthermore, a significant increase in nanocopper structure dimensions was observed, from 50-100 nm for unfused copper nanoparticles to 1 µm for sintered nanocopper structures. This effect together with the porosity decrease were correlated with the measured reduction in nanocopper sheet resistance and nanocopper interconnect contact resistance.

In conclusion, the wafer bonding experiment demonstrated the successful development and fabrication of wafer-to-wafer nanocopper interconnects for 3D integration applications. The sheet and contact resistance results for fused nanocopper showed very promising results for lowering the processing temperature up to 200 ℃, while obtaining comparable resistance values. Furthermore, the very high shear bond strength values obtained from dies bonded with sintered nanocopper are superior to many other bonding techniques using solders, eutectic or polymer bonding. The SEM analysis of the sintered nanocopper structure revealed the formation of large copper structures up to 1 µm through the nanoparticle sintering process. The bonding of dry nanocopper paste was found to result in poor adhesion and fusing between the nanocopper and bulk Cu layers. Despite the KOH infiltration and damage to the CBKR structures leading to large contact resistance values, the successsful fabrication at 225 ℃ of electrically conductive nanocopper wafer-to-wafer interconnects was demonstrated. Therefore, although further research effort is required to optimize the nanocopper sintering process, the wafer bonding parameters and to find a less destructive etching method for electrical measurement access, the wafer bonding technique based on nanocopper sintering shows promising results for the fabrication of low temperature copper 3D interconnects.

6 General Conclusions and Outlook

The low thermal budget imposed on 3D integration applications due to the damage sustained by active devices on wafers during high temperature processing is a major challenge for the fabrication of vertical metallic interconnects through wafer bonding. In this thesis, the design, fabrication and characterization of a low temperature (<250 ℃) technique for interconnect patterning and wafer bonding have been demonstrated. The melting point depression of copper nanoparticles is the main advantage of using nanocopper for bonding wafers at a low temperature. A novel technique developed within this research project is the lithographically defined screen printing procedure employed to fabricate metallic interconnects by patterning the nanocopper layer. The limited information on the properties of the newly developed nanocopper material, novel screen printing technique with a low maturity and limited project time frame have made this research work a considerably challenging endeavour. In order to achieve this, an exploratory research approach was utilized for the current project. Therefore, the focus was placed on obtaining preliminary results for future optimization of interconnect patterning and wafer bonding processes based on nanocoppper sintering rather than on an extensive analysis of the physical phenomena involved. Nevertheless, the project objectives were achieved and valuable results were obtained and analyzed, with the major achievements being summarized below within this chapter.

- The **fabrication of electrically conductive Al-Al interconnects using wet etching** was demonstrated in section 3.2. The possibility of achieving die-to-die bonding at room temperature shows promising results for fabrication of vertical metallic interconnects for temperature-sensitive 3D integration applications. However, substantial additional research is required for process optimization.

- The successful **fabrication of metallic interconnects through nanocopper patterning down to dimensions of 1-5 µm** was achieved and presented in chapter 4. A novel copper patterning approach based on lithographically defined screen printing of nanocopper was proposed and demonstrated. Patterning challenges were identified and solutions were found to correct for the observed undesired effects. The implemented process alterations resulted in significant optimizations of the nanocopper structure patterning quality. Future improvements including the downscale of patterning resolution to values below 1 µm are expected to be possible based on the obtained results.

- **Low nanocopper-to-bulk Cu specific contact resistaces were obtained**, as shown in section 5.2. The lowest obtained value was 0.227 $\Omega \cdot \mu m^2$ for fusing at 210 ℃, which is comparable to the values reported in the literature for Cu-Cu bonding at 400 ℃. Therefore, a significant decrease in processing temperature of 200 ℃ was achieved. Several copper oxide reducing agents were investigated and formic acid was selected based on its measured ability to result in a 25.6% reduction in specific contact resistance compared to the reference sample. Although further investigation is required for an in-depth understand of the underlying effects, the nanocopper-to bulk Cu contact resistance measurements show promising results for further process optimizations.

- **Very high shear bond strength values** were obtained using die-to-die bonding based on nanocopper sintering, as was presented in subsection 5.6.5. The highest bond strength obtained was 41.74 MPa by sintering the nanocopper at 300 ℃ under a pressure of 10 MPa after copper oxide removal by formic acid. This value is significanlty higher than that reported in the literature for solder, eutectic, anodic and polymer bonding [6]. Furthermore, the bond strength

value measured on dies bonded with nanocopper sintered at 200 ℃, is above 20 MPa, which is higher than reported values for eutectic (<17 MPa) and solder bonding (<14.6 MPa) performed at higher temperatures in the 235-363 ℃ range [47**?**].

- The successful fabrication of vertical interconnects through **wafer bonding of nanocopper structures below 250 ℃ was demonstrated**. The nanocopper fusing point was found to be in the 200-250 ℃ range, based on the TGA analysis and in-situ fusing experiment measurements. The formation of large copper structures up to 1 µm and the development of a continuous copper layer across the bond interface through copper nanoparticle fusing process were observed and analyzed using SEM imaging of ion milled cavities. Furthermore, a direct relation between the sintering parameters and nanocopper structure was observed. Applying external pressure and exposure to fusing temperature results in significantly reduced porosity and larger size of the fused copper nanoparticles. The measured specific contact resistance of the sintered nanocopper interconnects was significantly higher than expected. The extra resistance was attributed to the poor fusing of dry nanocopper to bulk Cu, the damage to CBKR structures during bonding, KOH infiltration and mechanical damage during electrical measurements. Despite these effects, the fabrication of electrically conductive nanocopper interconnect through wafer bonding below 250 ℃ shows very promising results for low temperature 3D integration applications. However, further research is required for better understanding of the underlying phenomena and process optimization.

Recommendations for Future Work

- **Automatic die pick & place and better control of the applied pressure during die attach** for the wet etch die bond experiment are expected to result in more reproducible results. Furthermore, the fabrication of CBKR structures using accurate die alignment would enable the correct measurement of Al-Al contact resistance. The technique could be extended to Cu-Cu bonding using Cu etching acid solutions and the influence of copper oxide reduction agents on contact resistance can be investigated. Self-alignment of dies based on surface tension generated using alternating hydrophobic Si/hydrophilic Cu or Al pads can be considered for future work.

- **Automatic screen printing equipment** can be utilized to obtain more reproducible parameters and results. The pressure and squeegee inclination angle can be controlled thus more accurately. The use of an automatic screen printing machine would also provide the opportunity to investigate the scientific challenges of expanding the nanocopper screen printing approach to large scale industrial applications.

- **Sub-micron nanocopper patterning** can be attempted using thinner resist layers and more advanced photolithographic equipment capable of higher resolution. The aforementioned elements are considered to be the limiting factors for achieving nanocopper interconnect patterning on a sub-micron scale, based on the screen-printing experimental results. The intrinsic nature of the developed screen-printing method puts a lower limit on the dimensions of the openings in the photoresist mask, which need to be several times larger than that of the nanoparticles in order to facilitate the correct filling with nanocopper of the openings and thus ensure the realization of clearly defined structure patterning. Due to the small coppper nanoparticle dimensions in the 10-30 nm range, successful patterning of the nanocopper paste is expected to be possible down to a critical dimension of approximately 100 nm. However, further improvements to the squeegee blade are required to

- **Wafer bonding should be performed before the nanocopper paste begins to dry**. The dry nanocopper layer is not able to fuse to the bulk Cu, resulting in delamination between

the two layers. In order to prevent this, a new nanocopper formulation should be used which would dry after a minimum time of 10 minutes, instead of a few seconds, as is the case for the nanocopper used in the current work. One possibility to achieve this is to develop a nanocopper paste based solely on solvents which evaporate in the 80-150 ℃ range. Furthermore, the nanocopper should be able to withstand the photoresist lift-off process without drying or being removed by the NMP solution, which constitutes a challenging research endeavour.

- **Better control of fusing conditions** is required in order to prevent nanocopper oxidation. Therefore, an oven with oxygen concentration control below 10 ppm is needed. Copper oxide reducing gases such as forming gas (95% N_2 + 5% H_2) or formic acid vapour can be utilized to study the influence of oxidation prevention on the fused nanocopper contact and sheet resistances. A programmable temperature ramp-up rate would also enable an extensive investigation of the fusing temperature profile effect on the mechanical and electrical properties of the nanocopper interconnects.

- **The influence of applied pressure and temperature on the fused nanocopper stucture size and layer porosity** needs to be further investigated. Based on the SEM images of fused nanocopper cross-sections, the applied pressure significantly increases the fused nanocopper structure size and lowers the porosity value. However, cracks in the bulk silicon have been observed when a force of 7600 N was applied. Therefore, an in-depth analysis of these parameters is required to find the optimal pressure and temperature conditions which result in the lowest nanocopper porosity and minimal damage to the nanocopper interconnect structures and silicon substrates.

- **Bonding of screen-printed nanocopper structures on wafers with Cu through-silicon vias (TSV)** should be investigated. Although the fabrication of Cu TSV presents additional challenges, this technique avoids the damage inflicted to the nanocopper structures by the top wafer bulk silicon removal. Therefore, the proposed method offers a more realistic 3D integration application which enables electrical measurements without damaging the fabricated wafer stack.

- **The reliability** of the wafer bond based on nanocopper sintering needs to be **characterized through thermal shock, humidity and mechanical shock tests**. The hermetic sealing ability of the nanocopper material is of particular importance for die bonding applications and requires further investigation. Furthermore, the influence of nanocopper porosity combined with exposure to reliability tests on the die shear bond strength should be studied. The aforementioned tests are required to provide further insight into nanocopper bond degradation effects and possible process optimizations.

7 Appendix

7.1 Appendix A: Fusion Bonding

Fusion bonding generally refers to the joining of two mirror-polished semiconductor wafers. This technique makes use of the principle that such materials form a weak bond at room temperature when brought into contact. No external force is needed, although some pressure is usually applied to correct for deviations in wafer flatness. Special wafer treatment is required to ensure that the surface roughness is low enough and the particle contamination is kept to a minimum. These measures are crucial to increase the contact area between the two wafers and to avoid interface voids. The weak bond formed is caused by physical forces such as van der Waal interactions, electrostatic forces and capillary forces [37]. Although the bond is strong enough to enable safe handling of the bonded pair, further processing is used to improve it. A high temperature annealing step in an inert gas such as nitrogen is required to increase the bond strength substantially by converting the physical forces into chemical bonds. The type of bonds depends on the wafer surface chemistry. Hydrophilic bonding is based on bonds formed between wafers covered with silicone dioxide (SiO_2), while hydrophobic bonding occurs between two Si wafers without any native oxide layer. Fusion bonding offers the important advantage of a very high bond strength, but has rather stringent surface flatness and roughness requirements as well as a high thermal budget.

7.2 Appendix B: Plasma Activated Bonding

Plasma activated bonding is an alternative hydrophilic bonding technique which allows for lower processing temperatures by means of surface activation. The lower annealing temperatures below 400 ℃ enable the use of materials with higher mismatch in coefficients of thermal expansion (CTE). A plasma treatment before bringing the wafers into contact increases the surface energy which depends on the plasma conditions and the materials to be bonded [56]. This surface activation results in higher bond strength, enhanced by an increase in the number of silanol (Si-OH) groups, larger viscous flow of the surface layer, higher diffusivity of water and gases trapped at the wafer interface and by the removal of contaminating particles [57]. Generally, plasma activated bonding is classified based on the process pressure into:

- Atmospheric Pressure-Plasma Activated Bonding (AP-PAB)
- Low Pressure-Plasma Activated Bonding (LP-PAB)

The AP-PAB method eliminates the need of a low pressure environment and vacuum generation. An alternating voltage between two electrodes is used to ignite the plasma gas. The gas mixture used during surface activation is correlated to the annealing temperature and to the materials used. For Si wafers, synthetic air (80 vol.% N_2 + 20 vol.% O_2) and oxygen are generally used, while Ar/H_2 is used for glass and $LiTaO_3$ materials. After surface activation with the plasma gas, the wafers are pre-bonded at room temperature, followed by a low temperature annealing step up to ℃. Very low roughness and flatness values are required to achieve good quality bonding. Therefore, an additional chemical-mechanical planarization (CMP) step is employed when using glass wafers [58].

The dielectric barrier discharge (DBD) method uses a dielectric material such as glass placed on the electrodes to prevent electrical sparks. A grounded carrier acts as the wafer carrier, while an indium tin oxide (ITO) coated glass is used as the second electrode. The plasma discharge is powered by a corona generator operating at a frequency of 28.5 Hz [58].

The LP-PAB technique requires a vacuum environment, additional process gases and a high frequency (HF) electrical field generated between two electrodes. The surface activation is achieved by ion bombardment of the exposed surface and chemical reactions caused by radicals. The most used operating frequency is 13.56 MHz. During the positive voltage, the electrons are free to move toward the

HF electrode. The work function prevents the electrons from leaving the electrode during the positive half wave of the applied voltage, leading to a negative bias voltage of up to 1000 V. The massive ions cannot follow the HF field and move to the negatively charged electrode on which the wafer is located. The ions striking the surface combined with the action of the radicals results in surface activation [58].

The reactive ion etching (RIE) method, commonly used for dry etching is adapted for surface activation use by reducing the HF power. The wafer carrier electrode is attached to the HF generator. The negative charge accumulated on the wafer surface attract the posivie ions in the plasma environment leading to plasma ignition in the reactor. The most used process gases are nitrogen and oxygen. A high bond strength is achieved after annealing at 250 ℃. The surface activation step results in more than twice the bond strength of non-activated wafers annealed at the same temperature. Another LP-PAB method based on remote plasma uses a separate side chamber for plasma generation. The input process gases travel through this chamber containing the remote plasma source and are injected into the main process chamber where the reaction takes place. The surface activation is based mostly on neutral radicals reacting with the wafer surface. The ion bombardment is much less pronounced, which means the wafer surface is less prone to damage. Another advantage is the longer plasma exposure times than for the RIE method, which makes this technique more flexible. Sequential plasma activated bonding (SPAB) consists of two steps. First, a RIE plasma is used to activate the wafer surface. In a separate chamber, radicals are generated using a microwave source and an ion trapping plate. Then, the wafer is exposed to the chemical reaction of the radicals. Thus, the treatment of the wafer surface changes from RIE to chemical plasma activation [59].

7.3 Appendix C: Anodic Bonding

Anodic bonding is mainly used to bond glass wafers to silicon or metal. The most common types of glass used are Schott 8330 and Pyrex 7740, as they are sodium borosilicate glasses and have a CTE close to that of silicon, which reduces the stress accumulated in the bonded wafer pair. A powerful electrostatic field is generated which causes mobile sodium ions in the glass wafer to move toward the bond interface. This is obtained by applying a high DC voltage in the range of 500-1000 V between the two wafers to be bonded at temperatures between 250-400 ℃ [60]. The mobility of positive ions increases with temperature. As the mobile sodium ions (Na^+) diffuse, they travel toward the electrode and a negatively-charged region with oxygen ions (O^{2-}) is generated in the glass wafer close to the interface. No mobile ions diffuse from the silicon wafer, leading to the formation of a positively charged region in the silicon wafer [61]. The two charged depletion regions attract each other, resulting in a strong electrostatic field which pulls the two wafers close together within atomic contact [62]. The process is illustrated in Fig. 65.

The very high electrical field intensity comes as a result of the high voltage drop over depletion region at the bond interface, which is in the range of a few micrometers. Under the influence of this strong electrical field, the oxygen ions drift to the bond interface and travel to the silicon wafer where they react with the silicon, forming silicone dioxide (SiO_2). The covalent bonds formed through the electrochemical reaction generate a strong bond strength between the glass and silicon wafers. Some pressure is applied to create a good contact between the wafers and to provide a good electrical conduction across the two wafers. Typical processing conditions are 200-500 ℃ for 10-20 min at a DC voltage of 500-1000 V. The bonding time increases when voltage and temperature are reduced [63]. The siloxane (Si-O-Si) layer formed between the bond surfaces ensures that an irreversible connection is created between the bonded wafers. Alternatively, if wafers with a SiO_2 layer are used, the bonding process is based on the diffusion of H^+ and OH^- ions instead of Na^+ and O^{2-} [61].

Anodic bonding is less sensitive to surface topography variations than fusion bonding and can provide relatively high bond strengths in the range of 10-20 MPa. Through the use of an intermediate glass layer deposited by sputtering, spin-on or vapour deposition, two silicon wafers can also be joined

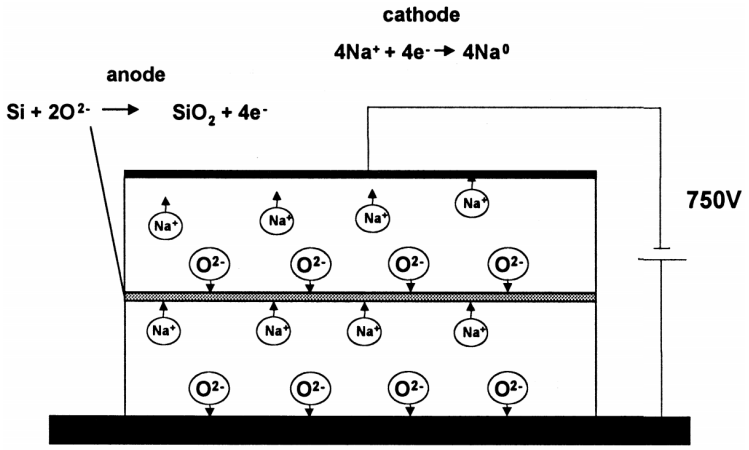

Figure 65: Anodic bonding mechanism [62].

using anodic bonding. Typical thicknesses of such layers range from tens of nanometers to a few micrometers. Solutions based on silica sol and organic silicon containing comppunds like tetraethyl orthosilicate (TEOS) are mixed with sodium salts. Silica films containing sodium oxide are obtained after thermal treatment, which can be used for anodic bonding similarly to glass wafers. [64] Recently, glass-to-glass anodic bonding has attracted interest for applications such as all-glass sealed channels with integrated metal electrodes. [62] Processing temperatures below 400 °C are possible with anodic bonding, which are crucial for compatiblity with conventional IC processes. However, the fabrication of metal-to-metal interconnects is not possible with anodic bonding, since this wafer bonding technique requires thin films or glass materials containing alkali ions.

7.4 Appendix D: Adhesive Bonding

Adhesive bonding, also known as glue bonding, uses an intermediate layer to provide a connection between two different substrates. The adhesives can be organic or inorganic, with the polymer Benzocyclobute (BCB) and SU-8 photoresist being the most widely used materials. Adhesive bonding can be performed within a large temperature range from room temperature to 1000 °C. Since there is no direct contact between the two wafers, this method can be applied to using various substrate materials such as silicon, glass or metals. One disadvantage of adhesive bonding is the widening of small structures during the patterning process, which does not allow for precise dimension control of the intermediate layer. Furthermore, water and gas molecules have a higher permeability when using organic intermediate layer, which leads to issues with hermetic encapsulation. The out-gassed products which can cause corrosion problems along with thermal instability are further limiting factors for the quality of the adhesive bonding process [65].

BCB and SU-8 have recently received great interest due to their light definable property and ability to produce high aspect ratio (HAR) microstructures such as micro channels and nuzzles. Their application in wafer bonding relies on the polymerization reaction of organic macromolecules. The organic molecules known as monomers form long polymer chains during the polymerization step. The high temperature annealing process provides the necessary energy for the polymerization reaction. After a subsequent cross-link reaction, a solid layer of polymer is obtained, which provides the actual bond layer between the substrates [65].

The adhesive layer can be deposited by spray-on, screen printing, embossing, dispensing or spin-on. The layer thickness will be a factor of the rotational speed of the tool and the material viscosity, similar to the coating process of photoresist in standard lithographic processes. The substrate surface is first cleaned, followed by the application of the intermediate layer. The substrates then contract, which is followed by the hardening of the adhesive layer. Various processes can be employed for the hardening of the adhesives such as applying pressure, exposure to UV light or using thermal cycles. Low temperature bonding is possible by using polymers capable of forming connections between substrates by polymerizing at temperatures below 200 ℃. This allows for the integration of electronics, micro-structures and electrodes on a single wafer [66].
SU-8 is one of the most widely used intermediate layers in adhesive bonding. It is a negative photoresist sensitive to UV-light consisting of 3 components: epoxy resin, gamma butyrolactone and triaryl sulfonium salt. Its polymerization reaction occurs at 100 ℃ and the material is stable up to 150 ℃. It offers many advantages such as excelent mechanical, electrical and fluidic properties, high chemical resistance, high thermal stability and high cross-linking density. Layer thicknesses in the range from 1 µm to 500 µm can be obtained by varying its viscosity using solvents, with thicker layers up to 1 mm being possible using multilayer coating. During UV-light exposure, lewis acid is released by the photoinitiator triaylium-sulfonium. The lewis acid acts as a catalyst for the polymerization reaction. During the post exposure bake (PEB) step, the activation of the molecule connections occurs. In order to obtain a proper bond quality, good control of process conditions such as the surface wettability and topography is required [67]. A cross-section of two silicon wafers bonded using SU-8 is shown in Fig. 66 [66].

Pressure in the range of 1.5-4.5 bar is applied to ensure that the intermediate layer is in contact with both substrates. This is required to provide a good quality bond without interface voids. Successful adhesive bonding results based on SU-8 have been reported with bond strength values within the 18-25 MPa range based on shear test measurements [67].

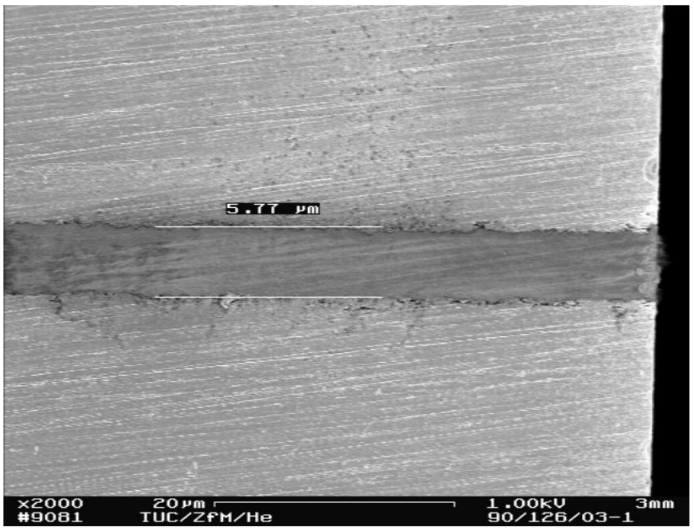

Figure 66: Cross-section SEM image of SU-8 bonded wafers. [66]

BCB is a hydrocarbon widely used as an intermediate layer in adhesive bonding. Several versions of BCB are available, depending on the processing requirements. Photosensitive BCB can be patterned using UV-light lithography in a similar manner to SU-8, while dry etch BCB patterning is performed via a photoresist mask on the BCB layer. The polymerization reaction of BCB occurs

withing the 250-300 ℃ range and the material is stable up to 350 ℃. BCB offers many advantages for bonding applications such as good chemical resistance to solvents, alkalines and acids, low dielectric constant and dielectric loss, absence of interface voids and 90% transparency to visible light. The last property makes BCB an ideal candidate for optical MEMS devices fabrication. However, adhesive bonding with BCB cannot produce hermetically sealed encapsulation for MEMS cavities applications [68].

The processing of the dry etch BCB layer starts with a cleaning step of the wafer substrates using oxygen plasma or wet etching in a sulphuric acid solution. In order to improve the bond strength, an adhesion promoter is next deposited on the surface of the substrate by spin-coating, contact printing or spray-coating in the case of free standing structures. This is followed by the BCB layer deposition via spin-coating which can achieve a thickness from 1 to 50 µm by varying the rotational speed and material viscosity. The subsequent soft cure bake step (<300 ℃) avoids creating a difference in the bond strength between the patterned and unpatterned layers caused by the polymer cross-linking reaction. Furthermore, the soft cure bake helps to reduce the formation of bubbles and lowers the distortion of the BCB layer while being compressed. If the polymerization reaction is insuficient, the layer will not provide the necessary adhesion to the substrate to achieve good quality bonding. If the polymerization level is too high, the adhesive layer lacks sufficient robustness to survive the patterning step. A good compromise is for the degree of polymerization to not exceed 50%. This is followed by resist spin-on and patterning using lithography. The patterned resist is used as a dry-etch mask to transfer the pattern to the BCB layer. After removing the resist layer, the wafers are ready for bonding. This is achieved by bringing the substrated into contact and applying pressure while heating them under a controlled atmosphere or vacuum. This is known as the hard cure of the BCB, performed within a temperature range of 180-320 ℃ for 30 min to 240 min, depending on the recquired layer properties. During this annealing step, the out-gassing of residual solvents is a major challenge. A vacuum environment can be utilized to remove the residual gases. Furthermore, the shrinking of the BCB layer can result in cracks, which prevent using this method for hermetic sealing of MEMS cavities [69]. An example of such crack formation in a BCB layer is depicted in Fig. 67 [70].

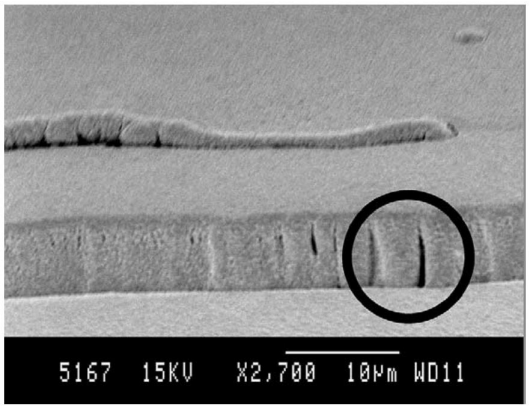

Figure 67: SEM image of 5 µm thick BCB layer covered with 0.5 µm Ti and 4.2 µm Au. Cracks in the metal seal causing leakage are emphasized [70].

7.5 Appendix E: Glass Frit Bonding

Glass frit bonding is a wafer bonding method based on an intermediate glass layer. It is also known as seal glass bonding or glass soldering. This technique relies on the decreasing viscosity of low melting glass with temperature to realize hermetic sealing between substrates. The effects of surface roughness

and particle contamination can be compensated by the viscous flow of the glass layer. This feature enables the realization of good quality bonding between substrates with high surface topography levels. Furthermore, using glass frit bonding leads to low stress level in the bonded wafers due to the low CTE mismatch of silicon and glass materials. This method can also be employed to bond materials such as silicon nitride, silicon oxide, glass or metals like titanium, copper or aluminium, provided that their CTE mismatch is low enough [71, 72].

The procedure starts with the deposition of the glass frit layer on the substrate. This can be done using spin coating or screen printing for layer thicknesses in the range of 5-30 µm. The glass frit material is a paste containing glass powder, inorganic fillers, solvents and organic binder. Milling is employed to fabricate a glass powder with grain size below 15 µm. The printable paste is produced by mixing the glass powder with the organic binder. Several properties of the melted glass paste (such as the CTE) can be altered by adding inorganic fillers to the mixture. Lead oxide can be added to lower the glass transition temperature under 400 ℃. However, the reduction of lead oxide by the silicon can result in the formation of lead precipitations at the silicon-glass interface, which can give rise to reliability issues. Glass frit pastes such as the FX-11-0366 from Ferro are commonly used, as they have good screen printing and bonding characteristics. An SEM image of two silicon wafers bonded using this paste is presented in Fig. 69 [72].

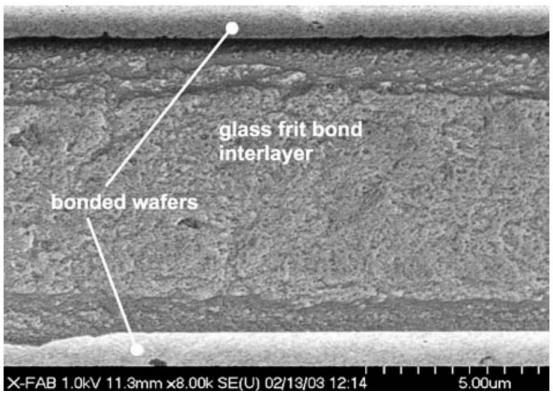

Figure 68: SEM image of glass structure at interface with silicon [72].

One of the main advantages of glass frit bonding is using the wetting effect to bond substrates with high surface topography. This has many applications, as the wafer surfaces have often a high roughness caused by previous deposition or plasma etching steps. Screen printing offers the advantage of selective bonding. This means that the glass layer is only deposited in areas where bonding is required. This is important for applications with microsystems containing moveable parts which have areas where bonding is not allowed. One important disadvantage of glass frit bonding is the possibillity of material flowing into structures which should be protected, such as moveable mechanical strucures, leading to them becoming blocked. Issues with screen printing and outgassing during bonding can lead to such blocking problems. Therefore, careful optimization and good control of screen printing and bonding processes are required for obtaining good results using glass frit bonding [72].

The main steps of glass frit bonding are the deposition of the paste using screen printing, the conditioning of the paste and the actual bonding. Structuring of the glass paste material and in-situ deposition are performed during the screen printing step. This method has the advantage of paste deposition on substrates with high surface topography such as cap wafers containing high steps or holes. No photolithographic steps are required, with feature sizes in the range of 100-200 µm being

possible to manufacture. During the thermal conditioning step, the paste is heated to an intermediate temperature, which is not high enough for the glass to melt. This is required for the outgassing of the organic additives. This is followed by the pre-melt step when the paste reaches the process temperature and fully melts, forming a compact glass layer without any gas inclusions. After the melting of the inorganic fillers, the glass layer properties stabilize and remain fixed. Aligned wafer bonding is performed using commercial equipment by applying pressure to the substrates, heating them to the process temperaure and cooling down. Clamping of the bond fixture is used to ensure good alignment accuracy [72].

The process temperature needs to be high enough to reduce the viscosity of the glass material to a value which enables the wetting of the substrate. This is essential in order to bring the glass and wafer surface into good contact, which leads to the formation of a very thin glass mixture at their interface. This is caused by atomic wafer surface layers being solved in the glass material. The formation of the thin layer provides a strong bond between the wafer and glass material. An SEM image showing the glass structure at this interface is presented in Fig. 69 [72].

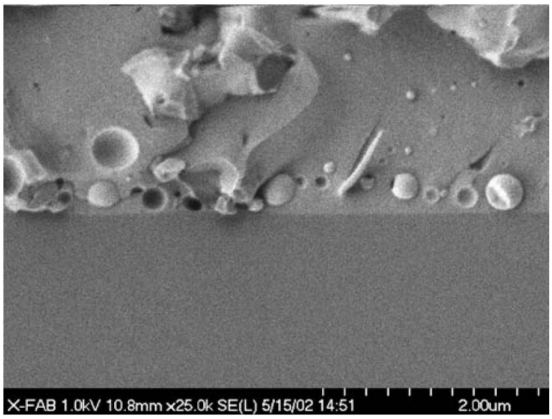

Figure 69: SEM image glass structure at interface to silicon [72].

7.6 Appendix F: Reactive Bonding

Reactive bonding is an intermediate wafer bonding technique which relies on using highly reactive multilayer films placed between the substrates. The multilayer system contains alternating metal layers of two different materials. The required energy for bonding is provided by the exothermic reaction occuring inside the multilayer system. An energy pulse using temperature, laser pulse or electrical spark is used to ignite the self-propagating reaction. The resulting heat bonds the solder layers encompassing the multilayer system. One important advantage of this technique it the limited temperature exposure to the substrate, which makes is applicable to bonding materials with large CTE mismatch such as metals, ceramics and polymers, as well as materials sensitive to thermal damage. However, reactive bonding cannot be used in the case of bond frame dimensions lower than several tens of micrometers. This is caused by the limited structuring and handling of the multilayer foils at such a small scale [73, 74].

One of the most commonly employed materials are alternating horizontal or vertical nano scale layers of Al/Ti, Ti/a-Si or Ni/Al. The metal layer thickness can range from 1 µm to 30 µm. The alternating metal films, known as the bilayer, contain a reactive and a low melting component which provide the necessary heat during their exothermic reaction. The velocity of the reaction decreases with increasing layer thickness, while the produced heat increases. A trade-off between the reaction

velocity and amount of heat exists and the correct balance requires a careful control of the bilayer thickness. Commercially available Ni/Al materials such as NanoFoil are widely spread for reactive bonding applications. A TEM image of the bilayer structure of this material is presented in Fig. 70 [73].

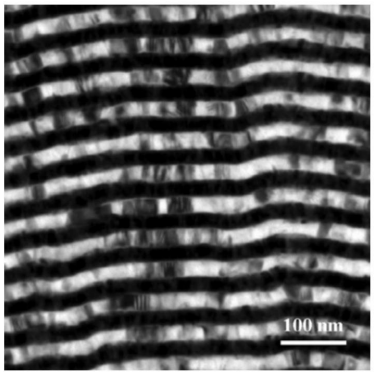

Figure 70: TEM image of reactive Ni/Al film (dark: Ni; bright: Al). [73]

The processing of freestanding foils faces many challenges regarding patterning, handling and positioning. Therefore, deposition on the wafer substrate is widely used for horizontal multilayer films. Several deposition methods are employed, including electroplating, etching and magnetron sputtering. A gold solder layer is first deposited on the wafer using physical vapour deposition (PVD), which provides good wetting of the solder. Cooling the substrate during the PVD process is required to minimize the material intermixing, which can adversely affect the exothermic reaction. The next step is depositing the multilayer system using magnetron sputerring. Up to thousands of thin films can be deposited in an alternate order using this technique. Alternative deposition methods include electroplating or electrochemical deposition (ECD). The first approach is based on alternating deposition using two different baths. The second approach requires a single bath based on an electrolyte which contains both film materials. This method offers the advantage of pattern plating, avoids the complex etching process and reduces time and complexity requirements. In the case of vertical structures, a two-step approach is employed. Dry etching of the silicon substrate is used to fabricate needles. Next, the second material is deposited on the needles by sputtering. By avoiding the deposition of thousands of single layers, this method results in significantly process time and complexity reduction.[74].

The bonding procedure based on nanoscale multilayer systems to achieve reactive bonding is illustrated in Fig. 71 [73].

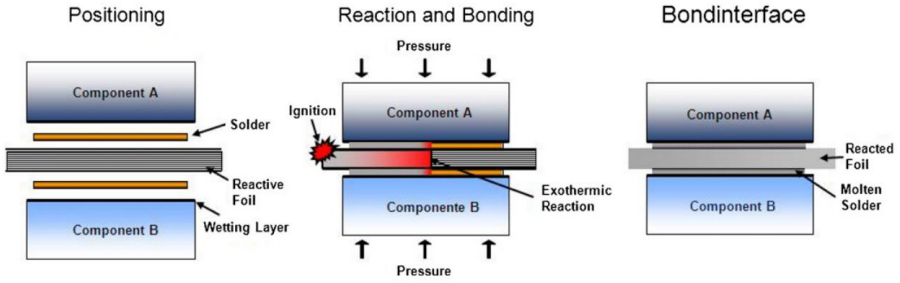

Figure 71: Principle of reactive bonding using reactive multilayer foils [73].

After positioning the two substrates, the exothermic reaction is ignited from an external source. The resulting self-propagating reaction relied on the reduction of chemical energy in the metal bilayers. A low layer thickness reduces the diffusion path, promoting the exothermic reaction. As the reaction progresses, an intermetallic compound is produced caused by atomic diffusion of the two metal films. The intermixing process generates heat which propagates the reaction to the adjoining layers, spreading through the multilayer system within a few miliseconds. The resulting heat leads to a high temperature of the bond interface, while the substrates are not exposed to significant thermal damage. The internal heat causes the solder layers to melt, forming a bond with both the substrates and multilayer system using diffusion. A mechanical pressure is applied to the substrates during bonding to increase the wetting of the substrate and improve the solder flow [73, 74].

Reactive bonding finds many applications for hermetic sealing and die attachements in MEMS device manufacturing. The distinctive advantage of this wafer bonding method is the localized temperature generated at the bond interface. This feature enables its use in microsystem technology to bond materials which are temperature-sensitive or have high CTE mismatch. For example, reactive bonding of a stainless steel membrane to a strain gauge fabricated out of quartz was successfully demonstrated using Ni/Al NanoFoils. Strong bond strength values were confirmed by tensile tests. However, some challenges with this bonding technique remain. Restrictions on the patterning level and compatibility problems limit the application of reactive bonding beyond die attachement level [73].

7.7 Appendix G: Surface Interactions

When two solids are brought into close proximity, various interaction occur between their surfaces. The types of interactions which dominate depend on many factors such as the environmental conditions (liquids, vacuum, gases). In the case of direct bonding of semiconductor wafers, three types of forces are relevant: (1) van der Waals attraction forces, (2) electrostatic Coulombic forces and (3) cappillary. These forces are presented schematically in Fig. 72 [37].

Van der Waals interactions are caused by atomic and molecular dipoles which attract one another according to their orientations. There are three types of van der Waals forces:

- The dipol-dipole force, which occurs between two polar molecules.
- The dipole-induced force, present between a polar and nonpolar molecule.
- The dispersion force, which arises between two nonpolar molecules. It results from the temporary dipole moment caused by charge distribution variations [75, 76].

The range of van der Waals forces depends on the scale used. On the atomic scale, they are considered long-ranged interactions, while on the macroscopic scale, they are regarded as short-ranged forces. This is based on their rapidly diminishing value F_v with the distance between molecules d, given by Eq. 10 [75].

$$F_v \propto d^{-7} \tag{10}$$

A first order approximation of the force acting between two flat plates can ne obtained through pair-wise summation of the interatomic forces present between every pair of atoms. In this case, the surface force F_v has a significantly longer range and decreases with the inverse of the second or third power of the surface separation d depending on the body geometry. The van der Waals dispersion force per unit area present between two flat plates, such as wafer surfaces, is given by Eq. 11, where A is the Hamaker constant, which is a function of temperature and the refractive indices of the two solids and their separating medium [76].

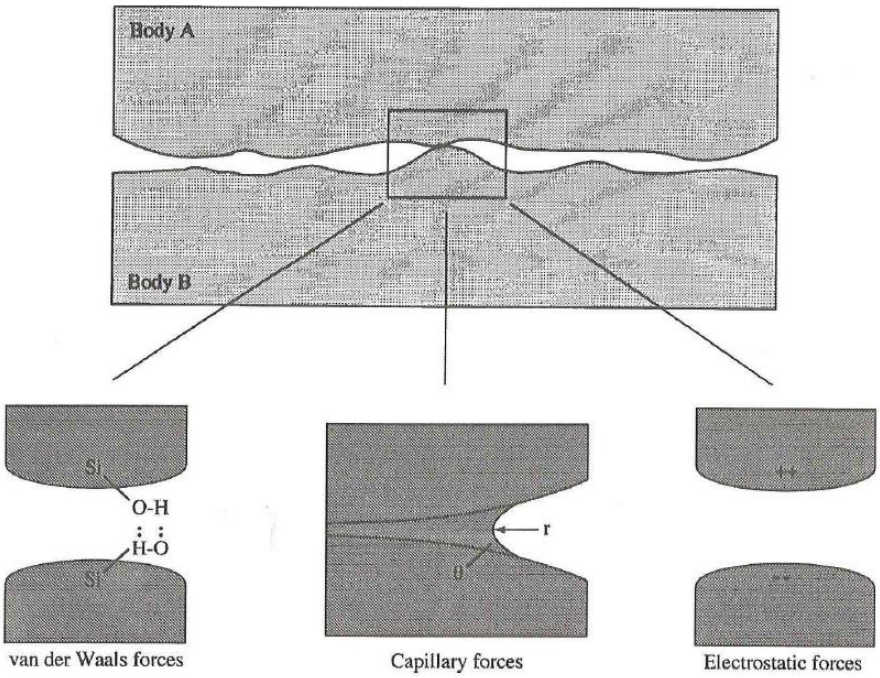

Figure 72: Schematic of interaction types between solids [37].

$$F_v = \frac{A}{6\pi d^3} \tag{11}$$

If we consider two wafer surfaces separated by distance d_0, which represents the lattice spacing of a crystalline material such as silicon, the equilibrium crack interface is illustrated in Fig. 73 [37].

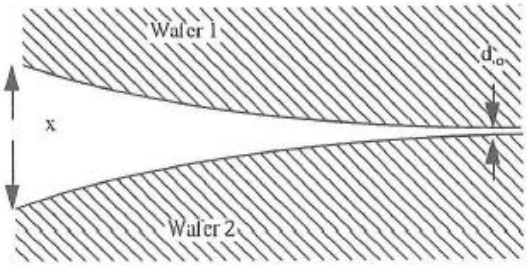

Figure 73: Schematic of a crack interface between two wafer surfaces in close proximity [37].

By ignoring the curvature of the surface, the van der Waals specific interaction energy W_v can be calculated based on the expression for the surface force in Eq. 11, with the result given by Eq. 12.

$$W_v = \int_{d_0}^{\infty} \frac{A}{6\pi d^3}\, dx = \frac{A}{12\pi d_0^2} \tag{12}$$

A particularly interesting case is the dipole-dipole attraction in hydrogen bonding. The hydrogen atom in the polar molecule can interact with an electronegative atom present in the same molecule or in an adjacent one. H-F, H-N and H-O bonds are known to be strongly polarized, resulting in a partial

positive charge of the hydrogen atom. This gives it a strong affinity for nonbonding electrons. Based on this effect, the hydrogen atom is able to form intermolecular attachements with electronegative atoms such as fluorine, nitrogen, or oxygen. A thin layer of water is ofter present on wafer surfaces. Since water is a polarized molecule, hydrogen bonding can form between the molecules in the water layer. The linkage of water molecules is thus able to bridge interacting atoms or molecules on the two surfaces, resulting in a long-ranged intermolecular force [77].

Electrostatic (Coulombic) forces occur between surfaces which were macroscpically charged by adsorbing or desorbing electrons or ions. These forces are generally dominant in the case of electrically charges surfaces. However, the presence of water or water vapour can partly compensate the effects of surface charging. Ionic materials consist of oppositely charges ions which are chemically bonded. When these bonds are broken by cleaving an ionic material, ions with opposite charges can remain attached to either surface. Since these ions are randomly distributed with an equal charge density σ, the surfaces have no macroscopic charge. However, on the microscopic level, an electrostatic attraction occurs between opposing surfaces with charge domains of linear dimension l. The expression for the force per unit area F_i is given in Eq. 13, where d is the wafer separation, ε is the dielectric constant of the intermediate medium and ε_0 is the permitivity of free space [78].

$$F_i = \frac{32\sigma^2}{\pi^2 \varepsilon \varepsilon_0} exp\left(-\frac{\sqrt{2}\pi d}{l}\right) \tag{13}$$

Vapours present on the surfaces can play an important role in electrostatic interactions. Such vapours are often terminated by adsorbates which determine the surface interactions. Furthermore, condensation of water vapour in a surface gap can result in screening of the Coulombic interaction [37].

Charge transfer between two dissimilar surfaces occurs when they are placed in good microscopic contact due to Fermi level effects, as they tend to achieve chemical equilibrium. This results in a strong electrostatic attraction between the surfaces with values of 10 MPa over several micrometers at relative humidity levels less than 5% [78].

In the case of two bodies places in a polar liquid such as aqueous electrolyte solution or water, charge accumulates on the surfaces until chemical equilibrium with the contacting solution is reached as ions of opposite charge are attracted to the two surfaces. An "electrical double layer" consisting of surface charge and the layer of opposite charge is thus formed, its thickness being a function of the ion concentrations in the solution. Similar bodies will experience a repulsive force, since they have the same charge. However, the magnitude of the forces is lower than in the case of direct electrostatic forces. This is due to a screening effect caused by the counteracting ions. The net force acting on surfaces in a polar liquid is a combination of the attractive van der Waals force and the repulsive electrostatic double layer force [37, 79].

The potential energy E is illustrated in Fig. 74 [37] as a function of surface separation between flat surfaces placed in a polar liquid. The double-layer potential has a exponentially decreasing behaviour as the surface separation d increases, being repulsive and having a positive value. The van der Waals potential energy E_v has a negative value and is inversely proportional to the surface separation d, according to Eq. 12. The net potential energy is obtained as the sum of the aforementioned energies and has a primary minimum where the two surface are in contact. A secondary energy minimum can occur due to high ion concentration in the solution which leads to very rapid decay of the double layer potential, resulting in high van der Waals force values outside the range of the repulsive forces. This secondary minimum corresponds to the separation value where the adhesion is weaker and therefore the contact is reversible [37, 79].

Capillary forces occur when a (condensed) liquid fills a narrow gap between two surfaces. The

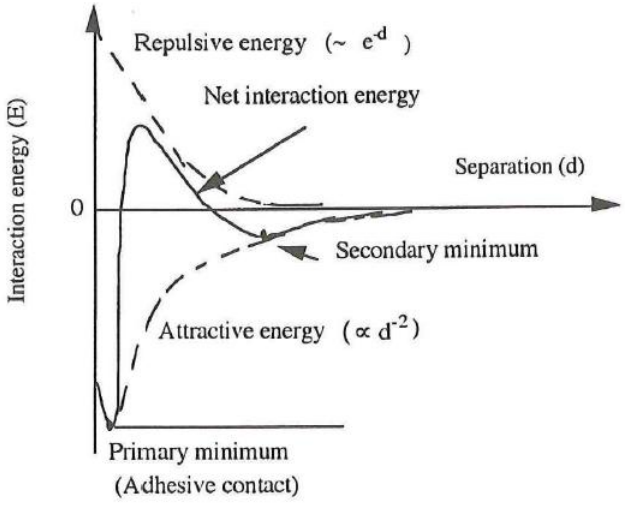

Figure 74: (a) Dotted line: Interaction potential energy as a function of surface separation distance and **(b)** Solid line: The interaction forces, as derivative of the potential energy [37].

conditions are that the contact angle of the liquid must be less than 90°and the surface separation should be smaller than the critical distance. Under these conditions, an attractive capillary force arises between the two surfaces. The critical distance is a function of the curvature radius of the liquid. A Laplace pressure p_{Lap} is introduces by the curvature 1/r of the cylindrical meniscus of the liquid, according to Eq. 14, where α is the surface tension of the liquid [37].

$$p_{Lap} = \frac{\alpha}{r} \tag{14}$$

In order to have an attractive force between the two surfaces, the Laplace pressure needs to be negative, which requires the meniscus to be concave. This leads to a maximum value of the surface separation known as the critical distance d_m, below which a liquid bridge can form between the two materials. This distance is a function of surface separation at contact d_0 and the contact angles θ_1 and θ_2 made by the liquid meniscus with the two surfaces. The espression for the critical distance in given by Eq. 15 [37].

$$d_m = r(cos\ \theta_1 + cos\ \theta_2) + d_0 \tag{15}$$

In the case of two flat surfaces such as those of semiconductor wafers with a contact area A, the capillary force can be expressed based on Eq. 14 as $A\alpha/r$. The capillary force for an equilibrium crack caused by an asperity between such surfaces gives rise to an interaction energy W_c, which can be calculated as the work needed to separate the two surfaces against the Laplace pressure. Its expression is given by Eq. 16 [78].

$$W_c = \int_{d_0}^{d_m} P_{Lap}\ dx \tag{16}$$

The interaction energy can be expressed using Eq. 14 and Eq. 15 as given by Eq. 17 [37].

$$W_c = \alpha(cos\ \theta_1 + cos\ \theta_2) \tag{17}$$

For typical small contact angles of 5°, flat silicon dioxide wafers with a thin water layer present on their surfaces experience an interaction energy of maximum 144 mJ/m^2. Most often, the wafers have a certain nonzero roughness, with asperities present on their surface . Without applying external pressure, the two surfaces are in contact only over isolated areas determined by such asperities. The liquid meniscus results in significant contact area increase, causing an important rise in adhesion between the two wafers [37].

Short-range forces become important for surfaces separated by very short distances in the range of 1-2 Å. When atoms are in such close proximity, the overlap of their electron clouds results in the formation of strong covalent and metallic bonds. Bonding under ultra high vacuum of wafers with very low surface roughness while applying external pressure to correct for flatness deviations is based on such short-range interactions [80].

List of Publications

Conference Papers

1. **A.A. Damian**, R.H. Poelma, H.W. van Zeijl, and G.Q. Zhang, "Low temperature hybrid wafer bonding for 3D integration," in *14th International Conference on Thermal, Mechanical and Multi-Physics Simulation and Experiments in Microelectronics and Microsystems (EuroSimE 2013)*, pp. 1–5.

Poster and Scientific Presentations

1. **A.A.Damian**, R.H. Poelma, H.W. van Zeijl, and G.Q. Zhang, "Low temperature wafer bonding for 3D integration," in DIMES day poster presentation session, September 25th 2012, Delft.

2. **A.A. Damian**, R.H. Poelma, H.W. van Zeijl, and G.Q. Zhang, "Low temperature hybrid wafer bonding for 3D integration," in *14th International Conference on Thermal, Mechanical and Multi-Physics Simulation and Experiments in Microelectronics and Microsystems (EuroSimE 2013)* poster presentation session, April 16th 2013, Wroclaw, Poland.

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References

[1] A.A. Damian, R.H. Poelma, H.W. van Zeijl, G.Q. Zhang. "Low Temperature Hybrid Wafer Bonding for 3D Integration". In *14th International Conference on Thermal, Mechanical and Multi-Physics Simulation and Experiments in Microelectronics and Microsystems (EuroSimE)*, pages 1–5, 2013.

[2] M.J. Wolf, P. Ramm, A. Klumpp, and H. Reichl. "Technologies for 3D wafer level heterogeneous integration". In *Symposium on Design, Test, Integration and Packaging of MEMS/MOEMS, 2008. MEMS/MOEMS 2008.*, pages 123–126, 2008.

[3] C. S. Tan, J. Fan, D. F. Lim, G. Y. Chong, and K. H. Li. "Low temperature wafer-level bonding for hermetic packaging of 3D microsystems". *Journal of Micromechanics and Microengineering*, 21(7):075006, 2011.

[4] Eun-Jung Jang, Seungmin Hyun, Hak-Joo Lee, and Young-Bae Park. "Effect of Wet Pretreatment on Interfacial Adhesion Energy of Cu-Cu Thermocompression Bond for 3D IC Packages". *Journal of Electronic Materials*, 38(12):2449–2454, 2009.

[5] D. F. Lim, S. K. Goulet, M. Bergkvist, J. Wei, K. C. Leong, and C. S. Tan. "Enhancing Cu-Cu Diffusion Bonding at Low Temperature Via Application of Self-assembled Monolayer Passivation". *Journal of The Electrochemical Society*, 158(10):H1057–H1061, 2011.

[6] Hanseup Kim and K. Najafi. "Characterization of low-temperature wafer bonding using thin-film parylene". *Journal of Microelectromechanical Systems*, 14(6):1347–1355, 2005.

[7] H. Nakanishi, T. Nishimoto, R. Nakamura, R. Yotsumoto, T. Yoshida and S. Shoji. "Studies on SiO_2-SiO_2 bonding with hydrofluoric acid. Room temperature and low stress bonding technique for MEMS". *Sensors and Actuators*, 79(3):237 – 244, 2000.

[8] S. Farrens. "Wafer-Bonding Technologies and Strategies for 3D ICs". In C.S. Tan and R.J. Gutmann and L.R. Reif, editor, *"Wafer Level 3-D ICs Process Technology"*, pages 49–85. Integrated Circuits and Systems. Springer US., 2008.

[9] S. Taniyama, Ying-Hui Wang, M. Fujino, and T. Suga. "Room temperature wafer bonding using surface activated bonding method". In *VLSI Packaging Workshop of Japan, 2008. VPWJ 2008. IEEE 9th*, pages 141–144, 2008.

[10] S. Kaimori, T. Nonaka, and A. Mizoguchi. The development of cu bonding wire with oxidation-resistant metal coating. *Advanced Packaging, IEEE Transactions on*, 29(2):227–231, 2006.

[11] P.L. Pai and C.H. Ting. "Selective electroless copper for VLSI interconnection". *Electron Device Letters, IEEE*, 10(9):423–425, 1989.

[12] Takahisa Nitta, Tadahiro Ohmi, Tsukasa Hoshi, Satoshi Sakai, Kunihiko Sakaibara, Shigeru Imai, and Tadashi Shibata. "Evaluating the Large Electromigration Resistance of Copper Interconnects Employing a Newly Developed Accelerated LifeTest Method". *Journal of The Electrochemical Society*, 140(4):1131–1137, 1993.

[13] K.C. Saraswat and F. Mohammadi. "Effect of scaling of interconnections on the time delay of VLSI circuits". *Electron Devices, IEEE Transactions on*, 29(4):645–650, 1982.

[14] M.T. Bohr and Youssef A. El-Mansy. "Technology for advanced high-performance microprocessors". *Electron Devices, IEEE Transactions on*, 45(3):620–625, 1998.

[15] Wong Wai Kwan, V. Kripesh, M.K. Iyer, M. Gupta, A. A O Tay, and R. Tummala. "Low temperature sintering process for deposition of nano-structured metal for nano IC packaging". In *Electronics Packaging Technology, 2003 5th Conference (EPTC 2003)*, pages 551–556, 2003.

[16] Yoshio Sakka, Tetsuo Uchikoshi, and Eiichi Ozawa. "Low-temperature sintering and gas desorption of gold ultrafine powders ". *Journal of the Less Common Metals*, 147(1):89 – 96, 1989.

[17] Chang Dong Zou, Yu Lai Gao, Bin Yang, Xin Zhi Xia, Qi Jie Zhai, Cristina Andersson, and Johan Liu. "Nanoparticles of the Lead-free Solder Alloy Sn-3.0Ag-0.5Cu with Large Melting Temperature Depression". *Journal of Electronic Materials*, 38(2):351–355, 2009.

[18] A.A. Zinn, R.M. Stoltenberg, A. T. Fried, J. Chang, A. Elhawary, J. Beddow and F. Chiu. "NanoCopper based solder-free electronic assembly material". *Nanotech 2012*, 2:71 – 74, 2012.

[19] T. Shimatsu and M. Uomoto. "Atomic diffusion bonding of wafers with thin nanocrystalline metal films". *Journal of Vacuum Science Technology B: Microelectronics and Nanometer Structures*, 28(4):706–714, 2010.

[20] S. Farrens and S. Sood. "Wafer Level Packaging: Balancing Device Requirements and Materials Properties". In *IMAPS. International Microelectronics and Packaging Society.*, 2008.

[21] Tsau, C.H. and Spearing, S.M. and Schmidt, M.A. "Characterization of wafer-level thermocompression bonds". *Microelectromechanical Systems, Journal of*, 13(6):963–971, 2004.

[22] C.H. Tsau, S.M. Spearing, and M.A. Schmidt. "Characterization of wafer-level thermocompression bonds". *Microelectromechanical Systems, Journal of*, 13(6):963–971, 2004.

[23] Kuan-Neng Chen, Sang Hwui Lee, P.S. Andry, C.K. Tsang, A.W. Topol, Yu-Ming Lin, Jian-Qiang Lu, A.M. Young, Meikei Ieong, and W. Haensch. "Structure, Design and Process Control for Cu Bonded Interconnects in 3D Integrated Circuits". In *Electron Devices Meeting, 2006. IEDM '06. International*, pages 1–4, 2006.

[24] T. H. Kim, M. M. R. Howlader, T. Itoh, and T. Suga. "Room temperature Cu–Cu direct bonding using surface activated bonding method". *Journal of Vacuum Science Technology A: Vacuum, Surfaces, and Films*, 21(2):449–453, 2003.

[25] Andy Fan Kuan-Neng Chen, Chuan Seng Tan and L. Rafael Reif. "Cu Wafer Bonding for 3D IC Applications". In C.S. Tan, R.J. Gutmann, and L.R. Reif, editors, *"Wafer Level 3-D ICs Process Technology."*, pages 117–124. Integrated Circuits and Systems. Springer US., 2008.

[26] Seonhee Jang and Youngkwan Seo and Joonrak Choi and Taehoon Kim and Jeongmin Cho and Sungeun Kim and Donghoon Kim. "Sintering of inkjet printed copper nanoparticles for flexible electronics". *Scripta Materialia*, 62(5):258 – 261, 2010.

[27] Y. C Lin, M. Baum, M. Haubold, J. Fromel, M. Wiemer, T. Gessner, and M. Esashi. "Development and evaluation of AuSi eutectic wafer bonding". In *Solid-State Sensors, Actuators and Microsystems Conference, 2009. TRANSDUCERS 2009. International*, pages 244–247, 2009.

[28] M. Hansen and K. Anderko. "Constitution of Binary Alloys"). McGraw-Hill, New York, 1958.

[29] W. Jost. "Diffusion in Solids, Liquids, and Gases". Academic Press, New York, 1969.

[30] R.F. Wolffenbuttel and K.D. Wise. "Low-temperature silicon wafer-to-wafer bonding using gold at eutectic temperature". *"Sensors and Actuators A: Physical"*, 43(1–3):223 – 229, 1994.

[31] R.K. Shukla and N.P. Mencinger. "A critical review of VLSI die- attachment in high-reliability applications". *"Solid-State Technol."*, pages 67 – 74, July 1985.

[32] A.-L. Tiensuu and M. Bexell and J.-Å. Schweitz and L. Smith and S. Johnsson. "Assembling three-dimensional microstructures using gold-silicon eutectic bonding". *Sensors and Actuators A: Physical*, 45(3):227 – 236, 1994.

[33] Lj. Ristic (ed). *Sensor Technology and Devices*, Artech House, London, UK, 1995.

[34] S. Farrens. "Latest Metal Technologies for 3D Integration and MEMS Wafer Level Bonding (Report)".

[35] Goran S Matijasevic and Chin C Lee and Chen Y Wang. "Au-Sn alloy phase diagram and properties related to its use as a bonding medium". *Thin Solid Films*, 223(2):276 – 287, 1993.

[36] Sumant Sood, Shari Farrens, Ron Pinker, James Xie, and Wilbur Cataby. "al-ge eutectic wafer bonding and bond characterization for cmos compatible wafer packaging". *ECS Transactions*, 33(4):93–101, 2010.

[37] Q.-Y. Tong and U. Gösele. "Semiconductor Wafer Bonding: Science and Technology". pages 17–24. John Wiley & Sons, Inc., 1999.

[38] A. Berthold. "Low-temperature wafer-to-eafer bonding for microchemical systems". *PhD Thesis Technical University Delft 2001, ISBN 90-75095-78-3*, page 1.

[39] Q.-Y. Tong and U. Gösele. "Semiconductor Wafer Bonding: Science and Technology". pages 33–47. John Wiley & Sons, Inc., 1999.

[40] Q.-Y. Tong and U. Gösele. "Semiconductor Wafer Bonding: Science and Technology". pages 49–56. John Wiley & Sons, Inc., 1999.

[41] A. Plößl and G. Kräuter. "Wafer direct bonding: tailoring adhesion between brittle materials". *Materials Science and Engineering: R: Reports*, 25(1–2):1 – 88, 1999.

[42] AMSC. "Test Method Standard Microcircuits, Mil-Std-883E Method 2019", FSC 5962, 1996.

[43] R.C Hibbeler . "Mechanics of Materials". page 32. New Jersey USA: Pearson Education, 2004.

[44] L. J. van der Pauw. "A method of measuring the resistivity and hall coefficient on lamellae of arbitrary shape". *Philips Tech. Rev.*, 59(8):220–224, 1958.

[45] John G. Webster. "The measurement, instrumentation, and sensors handbook.". pages 43–1. New York: CRC Press LLC, 1999.

[46] Reeves, Geoffrey K. and Holland, A. and Harrison, B. and Leech, Patrick W. "Electrical modelling of Kelvin structures for the derivation of low specific contact resistivity". In *Solid-State Device Research Conference, 1997. Proceeding of the 27th European*, pages 492–495, 1997.

[47] G. Roientan Y. Mei and K. Naja. ""A robust gold-silicon eutectic wafer bonding technology for vacuum packaging". In *Solid-State Sensor, Actuator and Micrysystems Workshop*, pages 86–89, 2002.

[48] Hong-seok Noh and Kyoung-sik Moon and Andrew Cannon and Peter J Hesketh and C P Wong. "Wafer bonding using microwave heating of parylene intermediate layers. *Journal of Micromechanics and Microengineering*, 14(4):625.

[49] Niklaus, F. and Enoksson, P. and Kalvesten, E. and Stemme, G. "Void-free full wafer adhesive bonding. In *Micro Electro Mechanical Systems, 2000. MEMS 2000. The Thirteenth Annual International Conference on*, pages 247–252, 2000.

[50] K.K. Nanda. "Size-dependent melting of nanoparticles: Hundred years of thermodynamic model". *Pramana - Journal of Physics*, 72(4):617–628, 2009.

[51] A.A. Zinn. "Private communication".

[52] Yuelin Wang and M. Esashi. "The structures for electrostatic servo capacitive vacuum sensors". *Sensors and Actuators A: Physical*, 66(1–3):213 – 217, 1998.

[53] A. Goyal, J. Cheong, and S. Tadigadapa. "Tin-based solder bonding for MEMS fabrication and packaging applications". *Journal of Micromechanics and Microengineering*, 14(6):819, 2004.

[54] N. Stavitski, J. H. Klootwijk, H.W. Van Zeijl, A.Y. Kovalgin, and R. A M Wolters. "A study of cross-bridge kelvin resistor structures for reliable measurement of low contact resistances". In *Microelectronic Test Structures, 2008. ICMTS 2008. IEEE International Conference on*, pages 199–204, 2008.

[55] A. Yabuki and N. Arriffin. "Electrical conductivity of copper nanoparticle thin films annealed at low temperature". *Thin Solid Films*, 518:7033–7037, September 2010.

[56] M. Eichler, B. Michel, P. Hennecke, and C.-P. Klages. "Effects on Silanol Condensation during Low Temperature Silicon Fusion Bonding". *Journal of The Electrochemical Society*, 156(10):H786–H793, 2009.

[57] Maik D. Wiemer, Jörg Bräuer, Dirk Wünsch, and Thomas Gessner. "Reactive Bonding and Low Temperature Bonding of Heterogeneous Materials". *Meeting Abstracts*, MA2010-02(27):1733, 2010.

[58] M. Eichler, B. Michel, M. Thomas, M. Gabriel, and C.-P. Klages. "Atmospheric-pressure plasma pretreatment for direct bonding of silicon wafers at low temperatures ". *Surface and Coatings Technology*, 203(5–7):826 – 829, 2008. Proceedings of the 35th International Conference on Metallurgical Coatings and Thin Films ICMCTF 2008 35th International Conference on Metallurgical Coatings and Thin Films.

[59] R.E. Belford and S. Sood. "Surface activation using remote plasma for silicon to quartz wafer bonding". *Microsystem Technologies*, 15(3):407–412, 2009.

[60] H. Jakobsen, A. Lapadatu, and G. Kittilsland. "Semiconductor Wafer Bonding: Science, Technology and Applications VI". pages 242–254. The Electrochemical Society, 2001.

[61] G. Gerlach and W. Dötzel. "Introduction to Microsystem Technology: A Guide for Students (Wiley Microsystem and Nanotechnology"). Wiley Publishing, 2008.

[62] A Berthold, L Nicola, P.M Sarro, and M.J Vellekoop. "Glass-to-glass anodic bonding with standard IC technology thin films as intermediate layers ". *Sensors and Actuators A: Physical*, 82(1–3):224 – 228, 2000.

[63] G. Wallis. "Field Assisted Glass Sealing". *ElectroComponent Science and Technology*, 2(1):45–53, 1975.

[64] H. J. Quenzer, C. Dell, and B. Wagner. "Silicon-silicon anodic-bonding with intermediate glass layers using spin-on glasses". In *Micro Electro Mechanical Systems, 1996, MEMS '96, Proceedings. An Investigation of Micro Structures, Sensors, Actuators, Machines and Systems. IEEE, The Ninth Annual International Workshop on*, pages 272–276, 1996.

[65] R.F. Wolffenbuttel. "Low-temperature intermediate Au-Si wafer bonding; eutectic or silicide bond". *Sensors and Actuators A: Physical*, 62(1–3):680 – 686, 1997.

[66] M. Wiemer, Chenping Jia, M. Toepper, and K. Hauck. "wafer bonding with bcb and su-8 for mems packaging". In *Electronics Systemintegration Technology Conference, 2006. 1st*, volume 2, pages 1401–1405, 2006.

[67] Liming Yu and Francis E H Tay and Guolin Xu and Bangtao Chen and Marioara Avram and Ciprian Iliescu. "Adhesive bonding with SU-8 at wafer level for microfluidic devices". *Journal of Physics: Conference Series*, 34(1):776.

[68] Christiaens, I. and Roelkens, G. and Kurt De Mesel and Van Thourhout, D. and Baets, R. "Thin-film devices fabricated with benzocyclobutene adhesive wafer bonding". *Lightwave Technology, Journal of*, 23(2):517–523, 2005.

[69] F. Niklaus and H. Andersson and P. Enoksson and G. Stemme. "Low temperature full wafer adhesive bonding of structured wafers". *Sensors and Actuators A: Physical*, 92(1–3):235 – 241, 2001.

[70] J. Oberhammer and F. Niklaus and G. Stemme. "Sealing of adhesive bonded devices on wafer level". *Sensors and Actuators A: Physical*, 110(1–3):407 – 412, 2004.

[71] Dresbach, C. and Krombholz, A. and Ebert, M. and Bagdahn, J. "Mechanical properties of glass frit bonded micro packages". *Microsystem Technologies*, 12(5):473–480, 2006.

[72] Knechtel, Roy. "Glass frit bonding: an universal technology for wafer level encapsulation and packaging". *Microsystem Technologies*, 12(1-2):63–68, 2005.

[73] Bianca Boettge, Joerg Braeuer, Maik Wiemer, Matthias Petzold, Joerg Bagdahn, and Thomas Gessner. "Fabrication and characterization of reactive nanoscale multilayer systems for low-temperature bonding in microsystem technology". *Journal of Micromechanics and Microengineering*, 20(6):064018, 2010.

[74] X. Qiu and J. Wang. "Bonding silicon wafers with reactive multilayer foils". *Sensors and Actuators A: Physical*, 141(2):476 – 481, 2008.

[75] C. Kittel. "Introduction to Solid State Physics". page 60. Wiley, New York, 2nd edition, 1986.

[76] R. G. Horn. "Surface forces and their action in ceramic materials". *J. Am. Ceram. Soc.*, (73):1117, 1990.

[77] T. A. Michalske and E. R. Fuller. "Closure and repropagation of healed cracks in silicate glass". *J. Am. Ceram. Soc.*, (68):586, 1985.

[78] K.-T. Wan, D. T. Amith, and B. R. Lawn. "Fracture and contact adhesion energies of mica-mica, silica-silica and mica-silica interfaces in dry and moist atmospheres". *J. Am. Ceram. Soc.*, (75):667, 1992.

[79] J. N. Israelachvili, P. McGuiggan, and R. Horn . "Basic physics of interactions between surfaces in dry, humid and aqueous environments". In *Proceedings of 1st International Symposium on Semiconductor Wafer Bonding: Science, Technology and Applications, The Electrochemical Society, Pennington, NJ, Vol.92-7*, page 33, 1992.

[80] G. Wallis. "Molecular bonding mechanism for solid adhesion". *J. Adhes.*, 37(187), 1992.