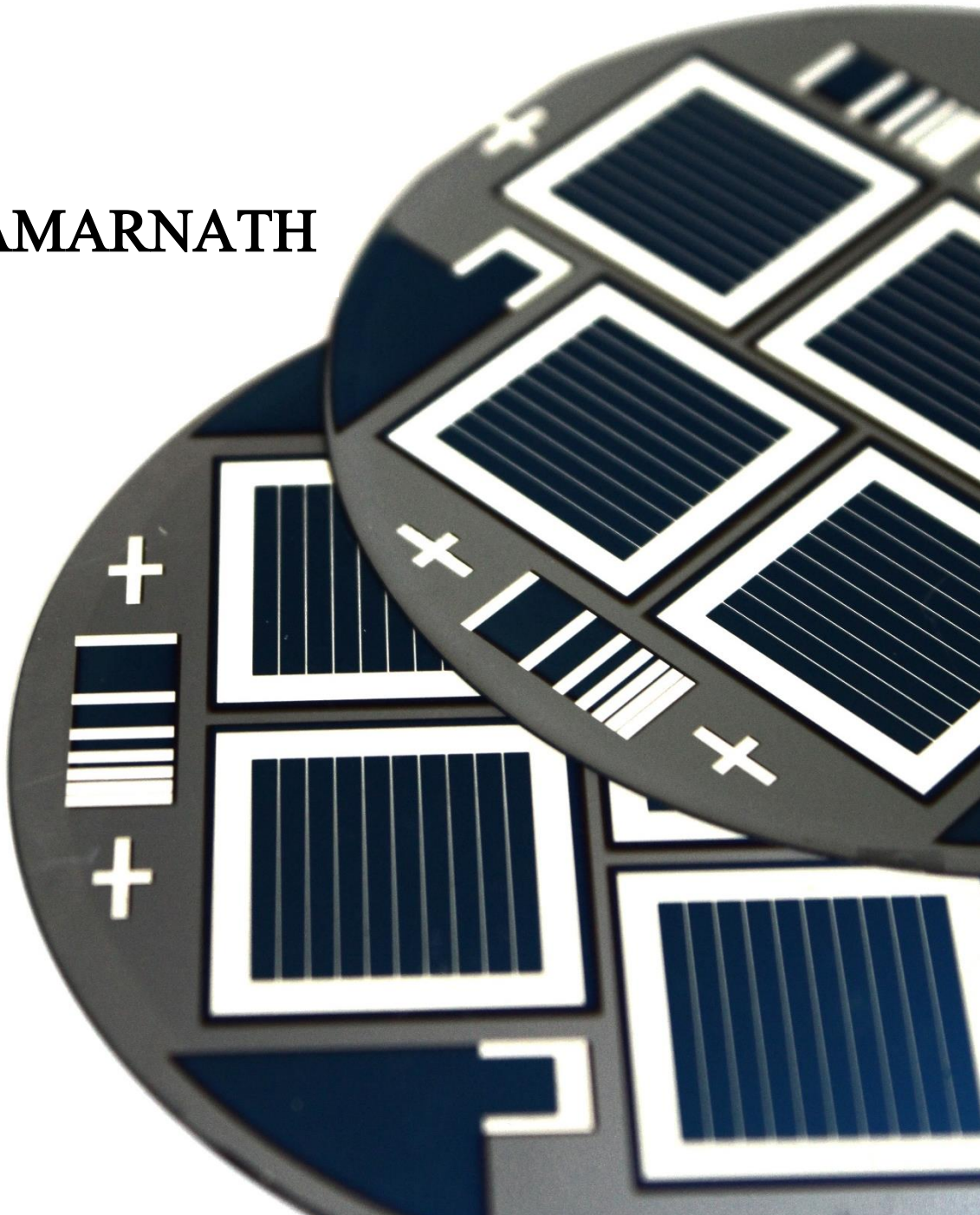
Fabrication of high efficiency poly-SiO_x passivated c-Si FBC solar cells

ASWATHY AMARNATH



TU Delft

Fabrication of high efficiency poly-SiO_x passivated c-Si FBC solar cells

Aswathy Amarnath

In partial fulfilment of the requirements for the

Master of Science degree on Sustainable Energy Technology

at the Delft University of Technology,

to be defended publicly on Monday, August 30th, 2021 at 13:00 PM.

Student number:	5116856	
Thesis Committee:	Prof. dr. Olindo Isabella	TU Delft, ESE-PVMD, Supervisor
	Dr. RACMM van Swaaij	TU Delft, ESE-PVMD, Associate Professor
	Dr. Massimo Mastrangeli	TU Delft, ECTM , Assistant Professor
	Dr. Guangtao Yang	TU Delft, ESE-PVMD, Supervisor
	Manvika Singh	TU Delft, ESE-PVMD, Daily Supervisor

TU Delft

EKL Else Kooi Laboratory

PVMD Delft University of Technology

ACKNOWLEDEGEMENT

Foremost, I would like extend my sincere gratitude to Prof. Olindo Isabella for having let me take on this challenging yet very exciting project. Working with you has been an absolute pleasure. I would also like to thank Guangtao for all the help and guidance you provided throughout the course of my project. The valuable insights I gained from our discussions definitely helped a lot. A big thank you to Manvika for the immense amount of support you have given me. Your utmost dedication towards your work and your students is commendable. Knowing you and working with you for the past ten months has been great.

A special mention to all the members of the c-Si group especially Can, Yifeng and Liqi for their valuable insights and timely help. And of course many thanks to Martijn, Stefaan and Daragh for the technical support and advice with regards to all the equipments.

My time at Delft would not have been the same if it weren't for all the beautiful friendships I hold very close to me. To begin with, a big thank you to Govind and Anirudh for the wonderful cooking sessions and great conversations. Achinth and Siri you guys are one among the first few friends I made here. Cheers to all the good times we have had. Of course Shivani for always being there to listen to me rant about things. For all the stressing sessions, we are finally done bro!

Lastly, my love and gratitude goes out to my biggest support system: my mom , my dad and my sister. TU Delft has always been a dream and I owe it to you guys for making this possible. I would also like to extend my thanks to the rest of my family and friends back home.

My time at TU Delft has been an eventful two-year journey. The extensive technical knowledge I have gained along with some remarkable memories made with some wonderful people makes this a wholesome experience. As my time at the Dutch land comes to an end, I look forward to what the future holds for me.

Signing Off!

Aswathy Amarnath

Delft 19th August 2021

ABSTRACT

Carrier selective passivating contacts (CSPC) have proven to effectively curtail the recombination losses emerging at directly metallised contacts of crystalline Silicon (c-Si) solar cells. CSPCs enabled using an ultra-thin interfacial tunnel oxide layer (SiO_x) capped by a doped polycrystalline Silicon (poly-Si) layer also referred to as Tunnel Oxide Passivating Contacts (TOPCon) have resulted in efficiencies as high as 25.8%. This thesis project addresses the development of oxygen alloyed poly-Si (poly-SiO_x) in combination with an interfacial oxide layer grown by dry thermal oxidation. The limited transparency of poly-Si based contacts brought on by high free carrier absorption (FCA) can be mitigated by the use of poly-SiO_x based passivating contacts owing to their wider bandgaps which induce stronger band bending.

To begin with, poly-SiO_x CSPC were optimised by determining the optimum thermal budgets for tunnel oxide growth and hydrogenation scheme. Tunnel oxide layers grown at 675 °C 6 minutes demonstrated very good passivation for p-type polished and n-type textured CSPCs indicated by their implied V_{oc} of 709 mV and 711 mV respectively. For the p-type textured CSPC identified as the primary limiting factor when deploying in c-Si solar cells, a tunnel oxide layer grown at 675 °C 3 minutes in conjunction with a two-step annealing scheme showed a crucial enhancement in passivation quality with a final implied V_{oc} of 687 mV.

The single side textured front back contacted (FBC) solar cell fabricated using the optimised p-type polished and n-type textured poly-SiO_x CSPC recorded a conversion efficiency of 20.94% on a 4 cm^2 screen printed solar cell. The reported efficiency is the maximum that has been attained so far for the configuration that uses a thermally grown tunnel oxide layer with poly-SiO_x CSPCs. Effective carrier transport and carrier collection was illustrated by a fill factor (FF) of 79.6%. A J_{sc} of 37.91 mA/cm^2 was recorded for the same. A comparison with a single side textured FBC solar cell that employed a tunnel oxide layer grown by nitric acid oxidation of Silicon (NAOS) revealed a superiority in performance by the thermally grown tunnel oxide layer resulting in better passivation and carrier selectivity.

Lastly, the optimised n-type textured and p-type textured CSPCs were implemented on a double side textured FBC solar cell. The two-step annealing scheme that showed beneficial results for the p-type textured CSPC was implemented within the FBC solar cell, leading to an implied V_{oc} of 698mV post hydrogenation. It is worth mentioning that this is the highest value achieved until now for this novel cell architecture. Implementation of screen printing resulted in a final conversion efficiency of 19.38% on a 4 cm^2 solar cell with a FF and J_{sc} of 77.89% and 37.65 mA/cm^2 respectively.

CONTENTS

ACNOWLEDGEMENT I

ABSTRACT II

CONTENTS III

NOMENCLATURE V

1 INTRODUCTION 1

1.1 WORKING OF A SOLAR CELL 3
1.2 RECOMBINATION MECHANISMS 4
1.3 SURFACE PASSIVATION 6
1.4 CARRIER SELECTIVE PASSIVATING CONTACTS (CSPC) 6
1.5 TUNNEL OXIDE PASSIVATING CONTACTS (TOPCON) 7
1.6 POLY-SiO_X AS AN ALTERNATIVE TO POLY-SI PASSIVATING CONTACTS 8
1.7 RESEARCH OBJECTIVES 8
1.8 OUTLINE 9

2 EXPERIMENTATION 10

2.1 FABRICATION PROCESS 10
2.2 CHARACTERIZATION TECHNIQUES 16

3 OPTIMISATION OF POLY-SIO_X PASSIVATING CONTACTS 20

3.1 PREPARATION OF SYMMETRIC SAMPLES 20
3.2 INTERFACIAL TUNNEL OXIDE LAYER (SiO_X) 22
3.3 METHODS OF TUNNEL OXIDE GROWTH 22
3.4 HIGH TEMPERATURE ANNEALING 22
3.5 OPTIMISATION OF TUNNEL OXIDE GROWTH AND ANNEALING CONDITIONS 23
3.6 RESULTS 24
3.7 CHOICE OF OPTIMUM THERMAL BUDGETS 31
3.8 HYDROGENATION 31
3.9 PASSIVATION TESTS POST TCO DEPOSITION 34
3.10 OVERVIEW 35

4 SINGLE SIDE TEXTURED FBC SOLAR CELLS 36

4.1 FABRICATION PROCESS 36
4.2 SOLAR CELL RESULTS 38
4.3 FABRICATION OF SINGLE SIDE TEXTURED FBC SOLAR CELL WITH NAOS 44
4.4 SOLAR CELL RESULTS 45
4.5 COMPARISON OF THERMAL OXIDE AND NAOS 46
4.6 OVERVIEW 48

5 DOUBLE SIDE TEXTURED FBC SOLAR CELLS 49
5.1 RE-OPTIMISATION OF POLY-SiO_X PASSIVATING CONTACTS 49
5.2 FABRICATION PROCESS 51
5.3 SOLAR CELL RESULTS 54
5.4 OVERVIEW 59
6 CONCLUSIONS AND RECOMMENDATIONS 60
6.1 CONCLUSIONS 60
6.2 RECOMMENDATIONS 62
BIBLIOGRAPHY 64

NOMENCLATURE

Carrier selective passivating contacts	**CSPC**
Crystalline Silicon	**c-Si**
Tunnel oxide passivating contacts	**TOPCon**
Tunnel oxide layer	**SiO_x**
Front back contacted	**FBC**
Nitric acid oxidation of Silicon	**NAOS**
Deionized	**DI**
Amorphous Silicon	**a-Si**
Hydrogenated amorphous silicon oxide	**a-SiO_x:H**
Atomic layer deposition	**ALD**
Rapid thermal process	**RTP**
Transparent conduction oxide	**TCO**
Implied open circuit voltage	**iV_{oc}**
Short circuit current density	**Jsc**
Poly-crystalline silicon oxide	**Poly-SiO_x**
Fill Factor	**FF**

External quantum efficiency	**EQE**
Low pressure chemical vapour deposition	**LPCVD**
Plasma enhanced chemical vapour deposition	**PECVD**
Open circuit voltage	**V_{oc}**
Indium tin oxide	**ITO**
Indium tungsten oxide	**IWO**
Pseudo fill factor	**PFF**
Anti-reflective coating	**ARC**
Forming gas annealing	**FGA**

1

Introduction

From the dawn of humanity to the genesis of industrial revolution, conventional sources of energy such as wood, coal, oil and natural gas have been an integral part of our industrial and domestic requirements. The excessive usage of these fossil fuels have contributed significantly to the ongoing climate change and there is an alarming need to palliate the damage caused by these sources [1]. However, the removal of these polluting sources from the energy system is a tedious task and despite the constant efforts to reduce the dependence on these energy sources, they still made up 84% of the total global energy consumption in 2019 [2]. The past 20 years have also seen a 45% increase in global energy consumption with the production of coal and natural gas rising even faster [3].

A cleaner and climate-resilient path towards meeting the goals of the Paris Agreement would be an increase in the contribution of renewable energy resources. Although their high costs and intermittencies pose as a challenge, the sustainable and replenishable nature of these resources make it the need of the hour solution and they are indeed pulling ahead in the electricity sector with over 260GW of new renewable energy capacity added in the year 2020 [4][5]. Solar Photovoltaics(PV), a pioneering technology in the field of renewables has been leading the power sector with a worldwide capacity of 583.5GW recorded at the end of 2019 [6].

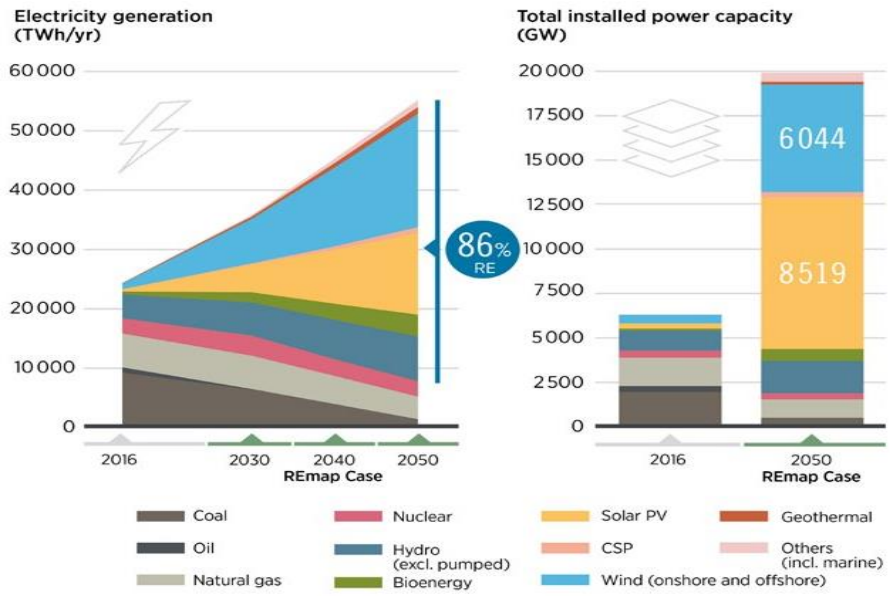


Figure 1 : Solar PV is expected to have largest installed capacity by 2050 [7].

The global solar market has been dominated by Asia with a cumulative capacity of 330.1GW followed by Europe with a capacity of 138.2GW by the end of 2019 [6].The increase in capacity of solar power has been attained by the remarkable cost reductions facilitated by government policies and extensive funding on Research and Development(R&D).The time frame between 2010 to 2019, saw the cost of solar PV drop by 82% globally [8]. With rapid technological improvements, the annual increase in PV capacity is expected to double by the end of 2030 and quadruple by the end of 2050 [9]. Figure 1 shows the estimated increase in PV capacity.

The concept of "PV Generations" established by Prof. Martin Green classifies the diverse field of photovoltaic technology into three different generations. According to this, the first generation (Gen I) consists of wafer based crystalline Silicon (c-Si) solar devices followed by the second generation (Gen II) which comprises of thin-film technologies such as CdTe, CIGS, amorphous Silicon (a-Si) and microcrystalline Silicon (µc-Si) and finally the third generation (Gen III) which is made up of tandem or stacked multi-junction devices [10].With a global market share of 95% in the year 2019, c-Si solar cells have become the most popular option in the manufacture of commercial solar panels [11].

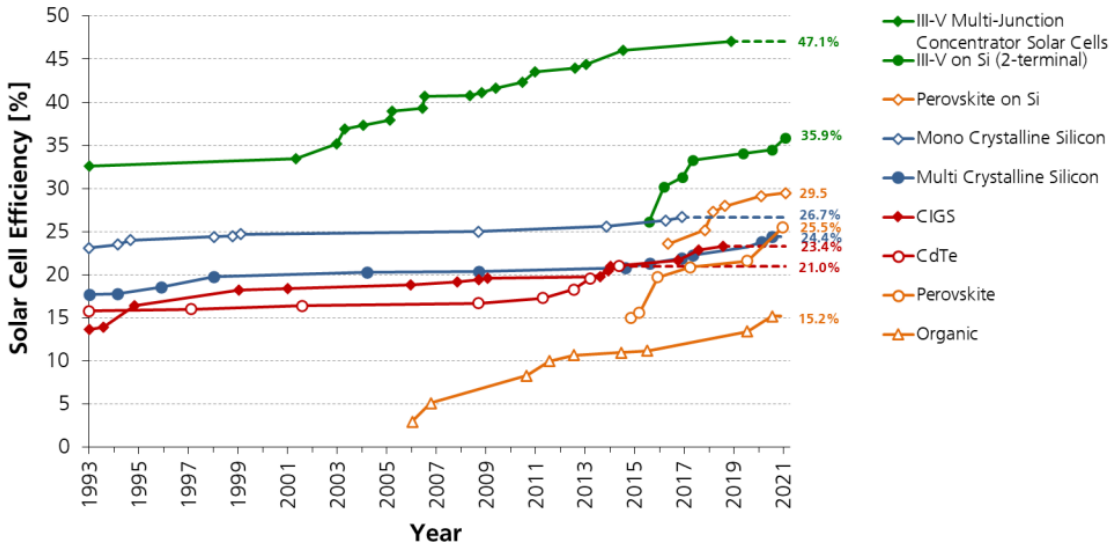


Figure 2: Solar Cell Efficiencies [11].

One of the primary reasons behind the success of these cells is the use of Silicon (Si) which is an abundant and non-toxic material that constitutes 26% of the earth's crust [12].In addition to this, Si has a bandgap of 1.12eV which equates to an absorption cut off wavelength of 1160nm which is well aligned with the optimum solar spectrum that facilitates solar to electric conversion using a single semiconductor observer material [13]. Silicon is an indirect bandgap material and this accounts for the ineffective radiative recombination which leads to longer charge carrier lifetimes and low absorption coefficient near the bandgap which can be rectified by means of surface texturing and anti-reflection coatings [13].Over the years, c-Si solar cells have witnessed rapid growth in technologies ranging from the basic homojunction solar cells to the state of the art Tunnel Oxide Passivating Contacts (TOPCon) cells. These technologies are discussed in detail in the upcoming sections. Mono-crystalline wafer based

technologies have witnessed a record breaking efficiency of 26.7% followed by an efficiency of 22.3% for poly-crystalline solar cells [11].With the overall production of all types of solar cells expected to grow in the coming years, c-Si based technology with its exemplary field operation and high efficiencies is expected to be a strong contender in the future photovoltaic market.

1.1 Working of a solar cell

A solar cell converts solar energy into electricity by means of a physical process called the photovoltaic effect which is the development of a potential difference at the intersection of two distinct materials in response to electromagnetic radiation. The built-in electric field within the solar cell, responsible for the voltage potential difference is induced by placing two distinct semiconductor layers – a positively charged p-layer and negatively charged n-layer in contact. The excess of holes in the p-layer and excess of electrons in the n-layer results in the formation of a p/n junction at the interface, thereby creating an electric field [14]. The working of a solar cell as seen in Figure 2 can be further explained using three primary processes: -

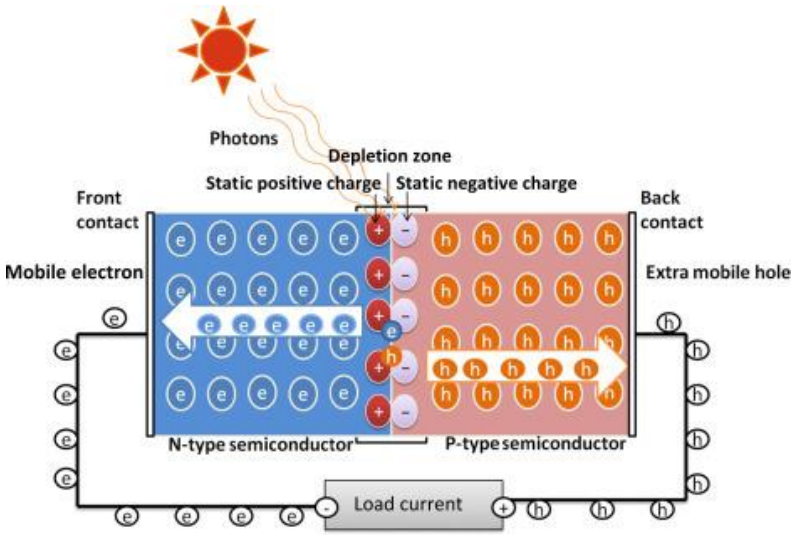


Figure 3: Schematic representation of a photovoltaic cell [15].

Generation of charge carriers

Only photons with energy (E_{ph}) greater than the band gap (E_g) of the semi-conductor which is the energy gap between the Valence Band (VB) and Conduction Band (CB) are absorbed. Those photons with lower energies are reflected or transformed to heat. The absorption of a photon of desired energy leads to the excitement of an electron from the VB to the CB which in turn leaves behind a hold (positive void) in the VB and thus an electron-hole pair is generated.

Separation of charge carriers

Separation of charge carriers is enabled by the usage of semi-permeable membranes such as the p-type and n-type material which form the p-n junction as discussed in the previous section. It is worth mentioning that the time required by the electrons and holes to reach the respective membrane should be lower than their lifetime and thus forcing the absorber material to be not very thick.

Collection of charge carriers

Electrical contacts are used for the collection of the separated charge carriers to create an external electrical current. The electrons collected at the n-side pass through the electric circuit and ultimately recombine with holes at the p-side and metal interface.

1.2 Recombination Mechanisms

Electrons in the CB are in a meta-stable state and thus would eventually attain a lower energy stage in the VB and thus recombining with a hole. This inexorable process of recombination can significantly deteriorate the working of a solar cell. Surface recombination and bulk recombination are the two primary recombination methods that occur in semiconductors.

Bulk recombination

Bulk recombination which occurs within the bulk of the substrate can be divided into three types as shown in Figure 4.

Radiative Recombination

This type of recombination is mainly seen in direct bandgap semiconductors such as gallium arsenide. It can be described as the direct band to band shift of an electron in the CB to the VB by emitting a photon which can otherwise be seen as the inverse of photon absorption[16]. c-Si is an indirect bandgap semiconductor which means it requires a phonon in addition to an electron and hold to enable band to band transition and thus radiative recombination can be neglected.

Shockley-Read-Hall (SRH) recombination

This type of recombination is enabled by lattice defects or an impurity atom. An electron or hole is trapped in energy states within the forbidden gap called trap states which are a consequence of defects in the crystal lattice. If a hole or an electron reaches the same trap state before the thermal emission of the electron to CB, recombination occurs. The extent to which a charge carrier can end up in a trap state highly depends on how far these defect states are from the edges of the VB and the CB. Chances of recombination are unlikely in cases where the trap states are closer to either of the band edges, as electrons to be emitted back into the CB instead of recombining with a hole that reaches the trap state. However, trap states that occur at the centre of band edges are effective sites for recombination. SRH recombination is the dominant recombination method in semiconductors at normal operating conditions [14].

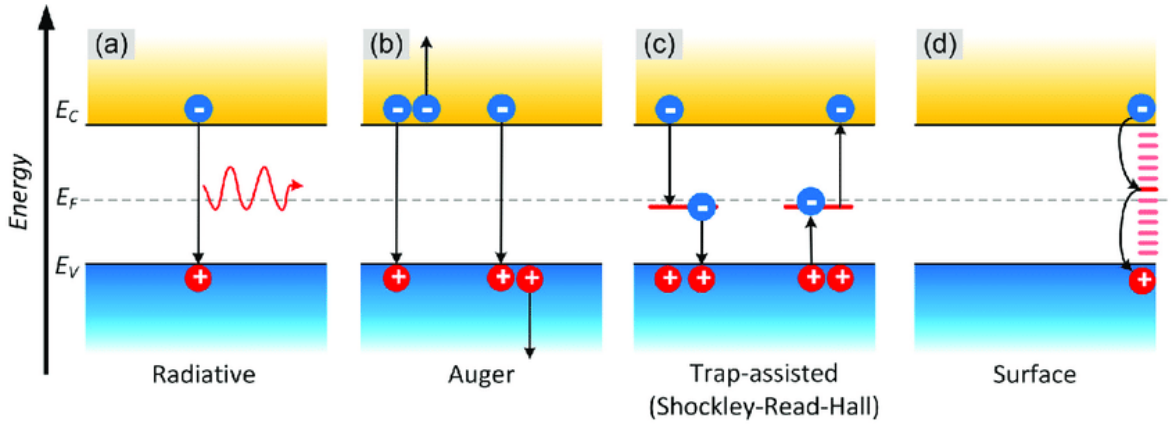


Figure 4: Recombination Mechanisms in Solar Cells. (a) Radiative recombination, (b) Auger recombination, (c) SRH recombination, (d) Surface Recombination [17].

Auger recombination

It is a three-carrier process in which the energy and momentum of the recombining carrier is preserved by transferring the momentum and energy to another carrier. If the receiving carrier is an electron, it will be excited to higher levels in the CB and if it's a hole, it will be excited into farther levels in the VB. The excited electron or hole will move back to the respective band edges by transferring its energy to phonon modes and heat. The rate at which this recombination occurs highly depends on the carrier concentrations which can be influenced by high levels of doping and carrier injection from incident light. As a result, auger recombination can be looked upon as a limiting factor in silicon based solar cells owing to the low lifetimes which deteriorate the cell efficiency [14].

Surface recombination

The presence of unsatisfied valence electrons on the surface of the silicon surface referred to as dangling bonds serve as defect sites and thus a number of trap states are created. These defect sites on the surface of the solar cell can serve as sites that initiate high level of recombination which leads to a reduction in the number of minority carriers. Surface recombination can be limited by the rate at which minority carriers reach the surface of the semiconductor. The term surface recombination velocity is used to describe the recombination at a surface. A low surface recombination velocity implies that minimal recombination occurs at the surface whereas a very high value of surface recombination velocity would mean that majority of the minority carriers reaching the surface end up recombining [14].

The impact of surface recombination can be reduced in two ways. The first one makes use of a thin layer of suitable material capable of forming covalent bond with the valence electrons present on the surface. In this way the trap densities are significantly reduced. This method is referred to as passivation which would be further explained in the sections below. The second method makes use of a heavily doped layer placed right beneath the surface. This doped layer would act as a barrier for the incoming minority carriers and hence reduces recombination.

1.3 Surface passivation

Surface passivation can be established by using passivation films that have the ability to reduce surface recombination by combining a chemical and an electric field component. The passivation films used for this purpose are chosen such that they also exhibit optical functions when placed on the surface of the semiconductor. The two components that enable the usage of passivation layers are described below:

Chemical passivation

This method of passivation aims at reducing the number of dangling bonds on the surface of the semiconductor by forming chemical bonds between the dielectric film and the semiconductor [18]. Thermally grown Silicon Oxide ($SiO_{x)}$ is a widely used passivation material due to its ability to provide low surface recombination velocities. Annealing in a hydrogen rich atmosphere can further passivate the dangling bonds with the end result being low defect densities and excellent chemical passivation.

Field Effect Passivation

This method of passivation uses an electric field to reduce the number of carriers that facilitate recombination. This is attained using dielectric films with fixed charges that can either be built-in during deposition or deposited controllably. The electric field will repel one type of charge carrier and thus minimise recombination [19].

1.4 Carrier Selective Passivating Contacts

The primary aim of carrier-selectivity is to utilise a virtual surface such as a semi-permeable membrane to maximise the flux of one type of charge carrier which is the collected carrier and to minimise the flux of the other type of charge carrier which is the blocked carrier. The flux of these charge carriers is determined by the conductivity (σ) and electrochemical potential gradient of holes and electrons. Thus carrier-selectivity calls for a high conductivity for the collected carrier and a low conductivity for the blocked carrier in order to eliminate the recombination of excess majority and minority carriers that can get extracted without the presence of a carrier-selective contact [20].

The effectiveness of a contact in a c-Si solar cell can be characterized using the recombination current density factor (J_o) and the contact resistivity ($\rho_{contact}$) and it is beneficial to reduce both these parameters to achieve good passivation. Both J_o and $\rho_{contact}$ are mutually dependent on the conductivity of electrons and holes. The simultaneous reduction of both Jo and $\rho_{contact}$ can be attained by increasing the conductivity of the collected carriers and minimising the conductivity of the blocked carriers at the same time. The charge carrier selectivity of a contact is determined by the ratio of these conductivities [21].

All c-Si solar cells require a set of external metal contacts to channel the potential and current developed within the solar cell to the external load. The most basic homojunction c-Si solar cell or the Al-BSF solar cell makes use of directly metallised doped silicon contacts and have exhibited efficiencies as high as 20% [22]. These structures have limited efficiency and surface passivation as they suffer from extreme recombination losses and a large density of states

within the c-Si bandgap which significantly promotes SRH recombination[20]. Further advancements in homojunction solar cells involved the usage of local contacts in the place of a full area contact. These structures were referred to as Passivated Emitter Rear Contacts (PERC) or Passivated Emitter with rear locally diffused (PERL). Efficiencies as high as ~23% have been recorded for this structure [23]. However, the direct contact between the metal and the c-Si at the local contacts still resulted in significant recombination losses. In addition to this, these cell structures also faced shadowing losses induced by the metal contacts in the front as metals do not facilitate the transmission of light though it. This problem was resolved by the usage of Interdigitated Back Contact (IBC) solar cells that consist of localised alternating n^+ and p^+ regions to which the metal is connected.

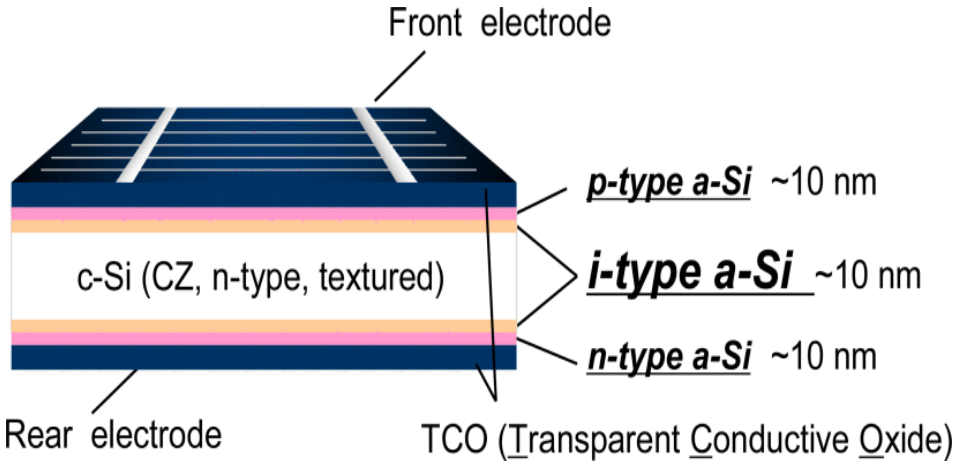


Figure 5: Structure of an HIT solar cell [24].

The heterojunction with thin intrinsic layer (HIT) solar cells shown in Figure 5, with an efficiency as high as 24.7% was the next advancement in the field as this structure made use of passivated contacts that eliminated the direct contact between the metal and the c-Si bulk [24]. HIT solar cells use passivating conductive layers that typically have a bandgap wider than c-Si (1.12 eV) [25]. Hydrogenated amorphous Silicon (a-Si:H) is used as the passivating layer in HIT cells owing to the higher bandgap (1.7-1.8 eV) and ease of doping [26]. The intrinsic a-Si:H layer which is in direct contact with c-Si facilitates chemical passivation and the doped layers deposited above it provide the required field effect passivation. Although the usage of HIT solar cells mitigate recombination losses from direct metal – c-Si contact, the low thermal budget of processing and high parasitic absorption in the doped and intrinsic a-Si:H layers pose as challenges to the same [27] [28].

1.5 Tunnel Oxide Passivating Contacts (TOPCon)

First exhibited by Lindhom et al. in 1985, full area heavily doped polycrystalline Silicon (poly-Si) passivating contacts turned out to be a rather efficient approach in reducing the recombination losses at the rear side and in the collection of only one type of charge carrier [29]. On the contrary to a-Si:H based HIT solar cells, the poly-silicon passivating contacts are a feasible option owing to their relatively higher tolerances to high temperature processes [30].

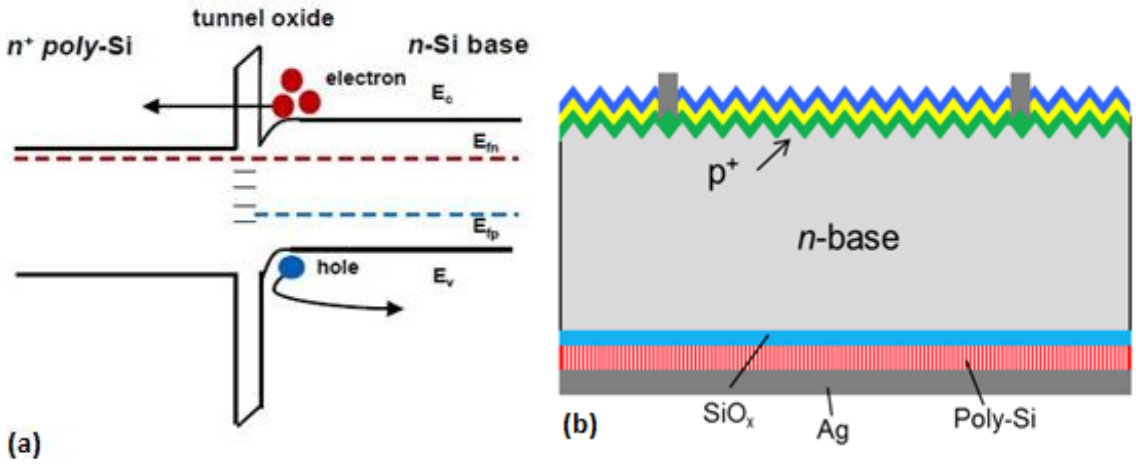


Figure 6: TOPCon (a) Band diagram of TOPCon [31] , (b) Schematic of the TOPCon Structure [32]

These poly-Si passivating contacts have been implemented in a new cell structure called the Tunnel Oxide Passivating Contacts (TOPCon) which makes use of an ultra-thin (<2.0nm) interfacial oxide layer (SiO_x) that is sandwiched between the doped poly-Si layer and the c-Si substrate to facilitate carrier transport through quantum tunnelling [33][34][35].Figure 6 demonstrates the schematic and band diagram of the TOPCon structure. TOPCon solar cells have been growing rapidly and an ultra-high efficiency of 25.8% has been achieved so far [32].

1.6 Poly-SiO_x as an alternative to poly-Si passivating contacts

Although poly-Si passivating contacts are more conductive and thermally resilient in comparison to the conventional a-Si:H based passivating contacts, they do suffer from a number of drawbacks. Poly-Si contacts suffer from high levels of parasitic absorption and as a result, incoming photons are absorbed by the passivation layers before reaching the c-Si bulk. In addition to this, the relatively lower bandgap of poly-Si makes it less transparent [36]. An alternative to this would be to use a thinner poly-Si contact, but this can cause severe damage to the tunnel oxide layer (SiO_x) [37].

The optical losses presented by the use of poly-Si contacts can be mitigated by the use of oxygen alloyed poly-Si layers also referred to as poly-SiO_x passivating contacts. Alloying the layer with oxygen results in lower absorption coefficients which ultimately makes the material more transparent especially in the longer wavelength regions. In addition to this the bandgap of the material is tuned (widened) which facilitates larger band bending. This contributes towards higher V_{oc} values which is a sign of excellent passivation [38][36]. Poly-SiO_x based passivating contacts also have the ability to withstand high temperature annealing conditions without deteriorating the passivation quality unlike SiC_x passivating contacts which is yet again another alternative to poly-Si contacts [39].

1.7 Research Objectives

The central goal of this project is the fabrication of high-efficiency solar cells that effectuate the usage of poly-SiO_x passivating contacts. In adherence to the TOPCon structure, the solar

cells will adopt the method of dry thermal oxidation for the growth of the tunnel oxide layer. The fabrication process consists of a number of stages which include the optimisation of poly-SiO_x passivating contacts, tunnel oxide growth conditions, annealing conditions and hydrogenation techniques. The final device fabricated is an amalgamation of these factors. The primary research objectives are:

- Optimisation of poly-SiO_x based passivating contacts by finding the optimum thermal oxidation budgets, thermal budgets for annealing and identifying the ideal hydrogenation techniques for n-type textured, p-type flat and p-type textured symmetric contacts.
- Fabrication of single side textured front back contacted (FBC) solar cells using the optimised n-type textured and p -type flat poly-SiO_x passivating contacts.
- Comparative study on the front back contacted (FBC) single side textured solar cells fabricated using two different methods of tunnel oxide growth: - dry thermal oxidation and nitric acid oxidation of Silicon (NAOS).
- Fabrication of double side textured front back contacted (FBC) solar cells using the optimised n-type textured and p-type textured poly-SiO_x passivating contacts.

1.8 Outline

The thesis report comprises of six chapters which looks into the optimisation of poly-SiO_x based passivating contacts and the subsequent fabrication of two types of front back contacted (FBC) solar cells.

Chapter 2 deals with the experimentation procedure adopted for this thesis. It addresses in detail the various equipment utilised for the fabrication process along with the different characterisation techniques adopted for further analysis of the solar cells.

Chapter 3 focuses on the optimisation techniques implemented on the n-type and p -type symmetric samples with the goal of attaining desired levels of passivation. It also discusses the annealing conditions and hydrogenation techniques adopted for the same.

Chapter 4 gives an insight on the results obtained from the fabricated single side textured FBC solar cells based on the optimised poly-SiO_x passivating contacts. This chapter also consists of a comparative study on the FBC single side textured cells that consists of tunnel oxides grown using two methods of oxidation: dry thermal oxidation and NAOS

Chapter 5 discusses the results obtained from the double side textured FBC solar cells fabricated once again using the optimised poly-SiO_x passivating contacts.

The conclusions obtained from the thesis project are discussed in Chapter 6 along with recommendations for future work which can be carried out in the PVMD group to further improve the performance of these solar cells.

2

Experimentation

This chapter looks into fabrication and characterization techniques adopted for the fabrication of FBC solar cells. Section 2.1 discussed the sequential steps involved in the fabrication followed by Section 2.2 that looks into the device characterization techniques used for the analysis of the solar cells.

2.1 Fabrication Process

This thesis project has utilised the cleanroom facilities provided by the EKL Laboratories and Kavli Nano Lab for the fabrication procedure of the solar cells followed by the characterization techniques performed at the ESP laboratory located at the Delft University of Technology.

2.1.1 Wafer Specification

The fabrication process makes uses of Phosphorus (P) doped n-type crystalline Silicon (c-Si) wafers manufactured by *TOP – SIL* with <100> surface orientation. The reason for using an n –type wafer base over a p-type wafer is multifold. Boron doped or p-type based solar cells have shown a significant reduction in cell performance due to the presence of light-induced degradation (LID) even when stored in a dark environment. The presence of oxygen during the fabrication process leads to the formation of (Boron-Oxygen) B-O complexes which serve as active centres for recombination under illumination of p-type solar cells. The primary advantage of n-type solar cells are the high minority carrier lifetime values [40]. n-type Si wafers are also resilient to contaminants introduced during the fabrication process due to the difference in impurity capture cross section for electrons and holes.

Table 1: Wafer Specifications

Parameter	**Value**
Diameter (mm)	100 +/- 2
Thickness (µm)	260 – 300
Doping	Phosphorous (n-type)
Resistivity (Ω cm)	1 - 5
Orientation	<100>
Method	Float Zone

2.1.2 Texturing

Surface texturing of solar cells which result in the formation of pyramids is a standard technique adopted for the reduction of reflectance and enhancement of light trapping as

shown in Figure 7. Pyramidal-like surface textures can be attained by mechanical engraving, chemical etching and plasma etching[41].

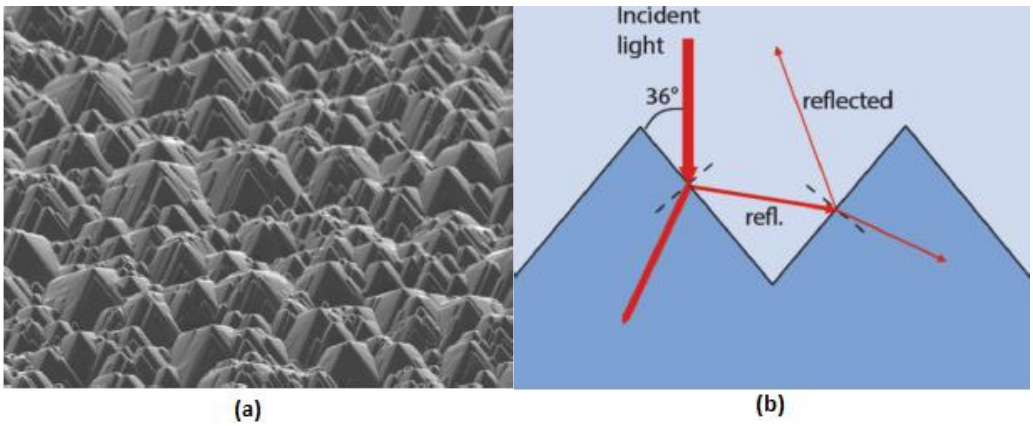


Figure 7: Textured surface on c-Si wafer and light trapping (a) SEM image of a TMAH textured c-Si wafer (b)Principle of light trapping [14].

In this thesis, a wet chemical etching using a Tetramethylammonium Hydroxide (TMAH) aqueous solution has been performed. With texturing, the <100> oriented silicon surface atoms would be etched resulting in the conversion of a planar surface to one covered with upright square-based pyramids or <111> facets. The alkaline solution used for texturing is composed of a mixture of TMAH and water in the ratio 1:4 along with 120 ml of ALKA_TEX solution maintained at 80 ˚C. The wafers are immersed in the solution for 15 minutes until there is no occurrence of reflection.

2.1.3 Standard Cleaning

Wafer cleaning is a critical step in the fabrication process. The standard cleaning performed helps in the removal of organic and inorganic contaminants from the surface of the wafer. The wafers are first immersed in a 99% HNO_3 solution and later rinsed in deionized (DI) water for approximately 5 minutes. This is followed by the immersion of wafers in a 69.5% HNO_3 solution maintained at 110 ºC for 10 minutes after which the wafers are once again rinsed in DI water for 5 minutes and dried in the Spin Rinse Dryer (SRD).

Exposure of the wafers to the cleanroom atmosphere during the cleaning process results in the formation of a porous native oxide layer on the surface. The presence of the native oxide can disrupt the SiO_x layer that would be deposited in the succeeding step. The native oxide layer is removed by the process of Marangoni cleaning and drying. This is executed by immersing the wafers in 0.55% HF for 4 min. The hydrophobic nature of the wafer, post the dip in 0.55% HF is an indication of the removal of the oxide. This wafer is then rinsed in DI water for 4 min followed by the introduction of isopropyl alcohol (IPA) for approximately 1 min to dry the wafers. It is advisable to perform Marangoni cleaning and drying before critical fabrication processes that require processing inside furnaces.

2.1.4 Thermal Oxide Growth

The tunnel oxide layer which forms the first window layer of the CSPC is grown by the method of dry thermal oxidation. Silicon oxidises when placed in an oxygen rich atmosphere at high temperatures as shown in equation (2.1). The process is typically performed at temperatures between 900 °C and 1100 °C [42].

$$Si(s) + O_2(g) \rightarrow SiO_2(s) \qquad (2.1)$$

In this thesis, thermal oxidation is executed in a Tempress System furnace. The wafers are lined up vertically in a slotted quartz wafer boat so that multiple wafers can be oxidised simultaneously. The undesired gases such as water vapour are flushed using Nitrogen gas (N_2) supplied at a constant rate of 6 SLM. The temperature and oxidation time can be varied as per requirement. The temperature at Zone 2 which is the centre of the reaction is ramped up at a rate of 10 ºC/min. A stabilisation time of 5 min has been applied to ensure that the furnace is at the required set temperature. This has been done because temperature plays a vital role in deciding the thickness of the oxide layer and slight variations in temperature can significantly influence the layer thickness. Oxygen is introduced and upon completion of oxidation, the oxygen flow is cut and temperature is ramped down. It has to be noted that the subsequent step that follows oxidation should be performed immediately as further exposure to cleanroom atmosphere would result in the growth of native oxide layers.

2.1.5 Growth of intrinsic amorphous Silicon (a-Si) layer using LPCVD

The LPCVD process used to grow the intrinsic a-Si:H layer has the benefit of being able to create pure, pinhole-free and uniform layers. This ensures that the interfacial tunnel oxide is protected against successive doping and chemical treatments [43]. The homogenous nature of the deposited layers, high reproducibility and high reliability are some of the other advantages of using LPCVD. Despite being able to be performed only at high temperatures, the reduction in rate of reaction when using LPCVD, gives great control over the thickness of the film and avoids variation in layer thickness [44]. Figure 8 is a schematic diagram of the LPCVD furnace.

The intrinsic layer deposition takes place at a temperature of 580˚C, Silane (SiH_4) gas flow at 45 sccm, pressure of 150 mTorr and at a deposition rate of 2nm/min. The deposition time used is 5 min which is expected to give a 10nm thick layer on flat or polished wafers. Post deposition, an annealing step at 600˚C for 1 hour is performed to release the stress. Before the succeeding deposition on the wafers, Marangoni cleaning and drying is performed to remove the native oxide layer formed on the a-Si layer.

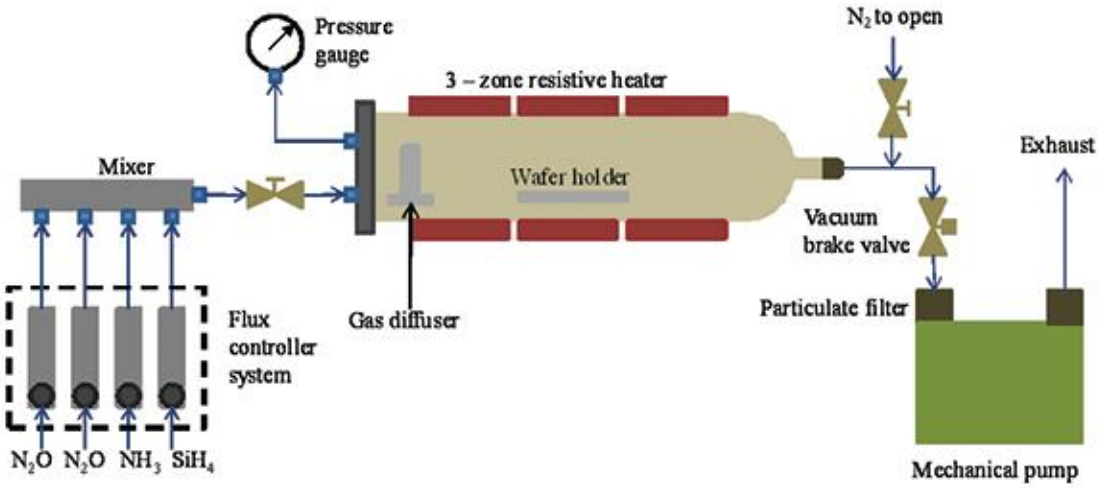


Figure 8: Schematic view of an LPCVD Furnace [45].

2.1.6 Plasma enhanced chemical vapour deposition (PECVD

PECVD is a hybrid chemical vapour deposition (CVD) method used for the deposition of thin films at low temperatures using plasma energy to pilot the reactions between the substrate and excited species. The deposition is carried out by the introduction of reactant gases between two parallel electrodes – an RF energized electrode and a ground electrode. A chemical reaction which results in the deposition on the substrate is induced by the capacitive coupling between the electrodes which excite the reactant gases into a plasma. Depending on the requirement, the substrate placed on the ground electrode is heated up to a temperature of range 250˚C to 350˚C [46]. The most commonly deposited films using PECVD are amorphous (a-Si), Silicon Carbide (SiC_x), Silicon Dioxide (SiO_2) etc. Figure 9 is the schematic representation of a PECVD reactor.

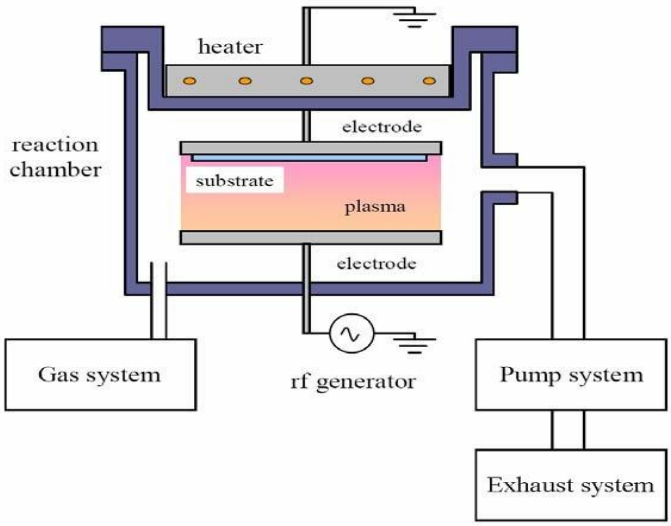


Figure 9: Schematic of a typical PECVD reactor [47][48]

In this thesis project, AMOR by Elettrorava is used as the PECVD equipment for the deposition of doped amorphous silicon oxide layers (a-SiO_x:H). It consists of four deposition chambers for respective material depositions and a fifth chamber to flip the wafers to facilitate

deposition on the front and back side of the wafers. A mixture of silane (SiH_4), carbon dioxide (CO_2), hydrogen (H_2), phosphine (PH_3) and diborane (B_2H_6) are supplied at the desired flow rates into the ultrahigh vacuum chamber for the growth of doped amorphous silicon oxide layer.

2.1.7 High Temperature Annealing

Annealing is performed on the wafers to facilitate dopant diffusion and to crystallise the doped hydrogenated amorphous silicon oxide (a-SiO_X:H) to poly-crystalline silicon oxide (poly–SiO_x). Choosing an optimum time and temperature is very crucial as prolonged annealing at temperatures higher than the optimum value can result in full crystallisation of the thin Si layer which ensures efficient doping and junction property but at the cost of a decrease in thickness of the tunnel oxide layer(SiO_2) and formation of pinholes in SiO_2 layer which would in turn deteriorates the carrier selectivity of the TOPCon structure [49]. On the other hand shorter annealing times can result in insufficient diffusion of dopants which restricts the field effect passivation [50] .This project makes use of the annealing furnace by TEMPRESS SYSTEMS. Annealing is performed at temperatures 900°C – 950°C for 5 to 15 minutes in a nitrogen (N_2) atmosphere.

2.1.8 Hydrogenation

Exposure of wafers to a high temperature annealing step results in the effusion of hydrogen from the SiO_x/c-Si interface creating dangling bonds that can be mitigated by a hydrogenation step [34]. Hydrogen passivation is a widely adopted chemical passivation technique that uses hydrogenated dielectric layers to passivate interface defects by forming Si-H bonds. Figure 10 demonstrates the passivation enabled by hydrogenation. Subsequent thermal processing helps in the diffusion of hydrogen into the c-Si bulk which in turn results in the passivation of defects throughout the bulk[51].In this thesis work, there are two types of hydrogenation and post annealing techniques performed: -

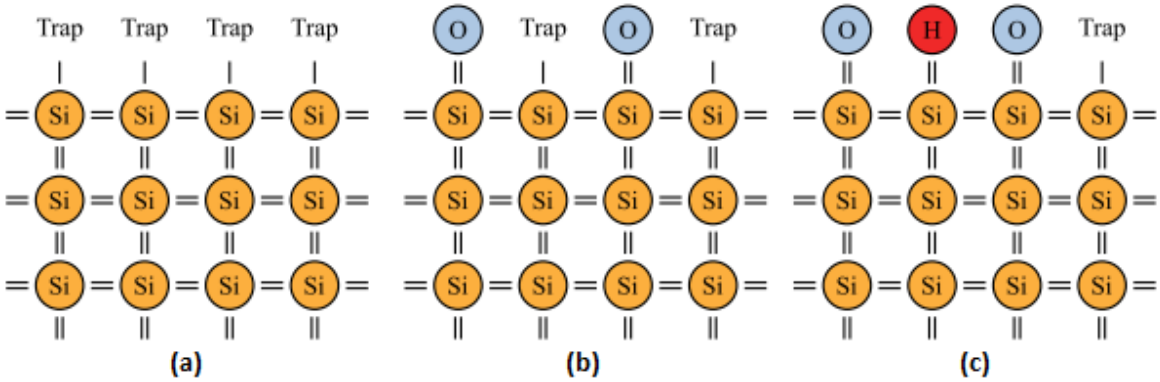


Figure 10: (a) Unpaired valence electrons forming interface traps at the Si surface (b) Interface traps are saturated by oxygen after oxidation (c) Further decrease in interface traps by hydrogenation [52].

- The first method uses SiN_x as a dielectric layer grown using PECVD followed by a forming gas annealing (FGA). The PECVD equipment used here is the Oxford Plasmalab80Plus. Two hydrogen rich gases Silane (SiH_4) and Ammonia (NH_3) supplied

at a flow rate of 20 sccm at a temperature of 400 °C and pressure of 87pa are used to enable the deposition of SiN_x. FGA annealing is carried out in the furnace by TEMPRESS SYSTEMS at 400 °C for 30 minutes in a forming gas atmosphere provided by hydrogen H_2 and nitrogen N_2 supplied at a flow rate of 0.3 SLM and 3 SLM respectively.

- The second method of hydrogenation makes use AlO_x as the dielectric layer followed by a rapid thermal process (RTP) annealing. Aluminium Oxide (AlO_X) is deposited using the method of Atomic Layer Deposition (ALD). ALD works on the principle of growing thin films over a number of cycles during which the surface is exposed to a number of gas-phase or vapour phase species in alternating doses. This thesis project used the ALD equipment Oxford Instruments OpALTM reactor. Trimethylaluinium (TMA) and water are used as the precursors for the growth of AlO_x which takes place over 100 cycles at a temperature of 105 °C, with every cycle followed by a purging step to remove excess water and by-products.

2.1.9 Transparent Conductive Oxide Layer (TCO)

A TCO layer is deposited on the front and rear side of the solar cells to facilitate high lateral conductivity with low resistive losses combined with high optical transmittance to light[53]. In this thesis, the TCO layer used is Indium Tin Oxide (ITO) which is composed of 90% Indium Oxide and 10% Tin Oxide. The wafers are sandwiched between aperture masks made of metal in order to ensure that the deposition taking place through sputtering occurs only in the areas specified by the masks. ITO layers of required thicknesses determined by the properties of light trapping and carrier transport have been deposited on the front and rear side of the solar cells deposition takes place at room temperature at a pressure of 2.2 10^{-5} bar.

2.1.10 Metallisation

Metallisation is a dual purpose technique that can influence the performance of a solar cell optically and electrically[54]. The gridline width can influence the shading which affects the short circuit current. The series contact established via contact will have an impact on the fill factor.

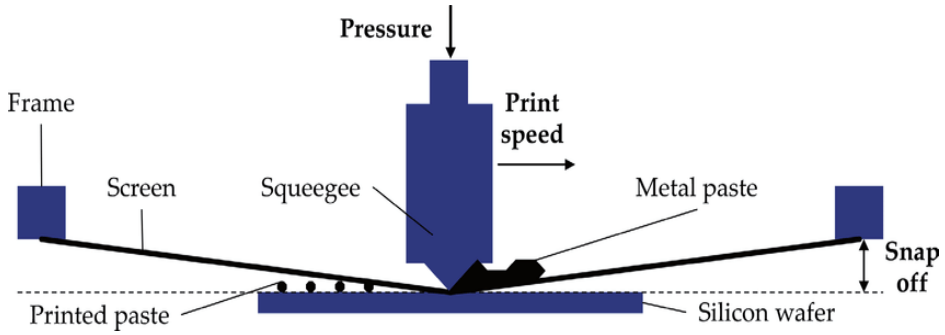


Figure 11: Schematic representation of screen printing [55].

In this thesis work, metal contacts have been developed using the method of Screen printing demonstrated in Figure 11. It uses a silver (Ag) paste at low temperature to define the fingers and the bus bars which act as the collector. The silver paste is applied on the screens which replicate the solar cell structure. The screen used would depend on the aperture mask utilised

using the previous step of ITO deposition. Upon application of the Ag paste, the cells are placed in the oven for approximately 30 minutes at 170 ˚C to dry the paste and seal the structure. Upon metallisation, the solar cells are annealed on a hot plate at a temperature of 350 ºC for time durations of 5 to 10 minutes to facilitate better performance attained by an improvement in J_{sc} and Fill Factor.

2.2 Characterization Techniques

This section looks into the various characterization techniques used to test and analyse the performance of the symmetric samples and the solar cells. The characterization tests performed on the symmetric samples at various stages have contributed significantly in improving the passivation of the samples.

2.2.1 Quasi Steady State Photo conductance (QSSPC)

The QSSPC is a contactless measurement technique used for the determination of minority carrier lifetime by using a photoconductance instrument which operates on a quasi-steady state mode. The data obtained upon analysing the quasi-steady state photoconductance as a function of light intensity can provide implicit information on the short circuit current (I_{sc}) and open circuit voltage (V_{oc}) of the solar cell being fabricated[56]. The PVMD group makes use of the Sinton WCT-120 Lifetime Tester measurement system shown in Figure 12 to measure the samples at individual stages of fabrication in order to evaluate the passivation quality.

The device consists of a coil platform for the placement of the wafer and a filtered xenon flash lamp. The flash light incident on the wafer results in the generation of excess charge carriers in the wafer bulk.

The increase in wafer conductance owing to the photogenerated excess charge carriers can be calculated based on the equation (2.2) under the assumption that the generation of holes and electrons are equal and uniform.

$$\sigma_L = q(\Delta n\mu_n + \Delta p\mu_p)W = q\Delta n(\mu_n + \mu_p)W \qquad (2.2)$$

Figure 12: Sinton WCT-120 Lifetime Tester [57].

Where q is the elementary charge, Δn and Δp are the excess electrons and holes respectively, μ_n and μ_p are the electron and hole charge carrier mobilities which are a function of both doping and level of injection and W is the width of the wafer.

The continuity equation for an n-type semiconductor under the assumption of no external electric field and a uniform distribution of excess charge carrier gives rise to equation (2.3).

$$G - \frac{d\Delta p}{\tau_{eff}} = \frac{d\Delta p}{dt} \qquad (2.3)$$

Thus, the effective minority carrier lifetime can be calculated as per equation (2.4),

$$\tau_{eff} = \frac{\Delta p}{G - \frac{d\Delta p}{dt}} \qquad (2.4)$$

The instrument makes use of the Quasi-Steady State (QSS) mode when the minority carrier lifetime is lower than 100µs. QSS lifetime measurements rely on the number of charge carriers available when a steady light is flashed on the wafer. It is assumed that variation in flash light intensity is very slow so that steady state is maintained at all times. As a result, for QSS mode measurements, $\frac{d\Delta p}{dt} = 0$.

For minority carrier lifetimes greater than 100µs, a transient mode of measurement is adopted. In this mode, the carriers are generated using a very short light pulse and it is assumed that the generation rate $G = 0$.

Based on the measured effective lifetime, the implied open circuit voltage (iV_{oc})of an n-type wafer can be determined by equation (2.4),

$$iV_{oc} = \frac{k_b T}{q} \ln \frac{(N_d + \Delta n)\Delta n}{{n_i}^2} \qquad (2.5)$$

Where k_b is the Boltzmann constant, T is temperature, N_d is the donor concentration and n_i is the intrinsic carrier concentration.

2.2.2 Illuminated J-V measurement

The performance of a solar cell can be characterized using four main parameters which are: the open circuit voltage (V_{oc}), the short circuit current density (J_{sc}), the fill factor (FF) and the conversion efficiency (η) [14]. The PVMD group makes use of the AAA class Wacom WXS-156SL2 solar simulator to precisely simulate the standard test conditions of: AM1.5 spectrum

using a combined Xenon and Halogen lamp setup, total irradiance of 1000W/m^2 and a temperature of 25 ºC which is facilitated by a temperature controller installed on the test stage where the solar cells are placed for measurement.

The short circuit current density (J_{sc}) is the maximum current delivered by a solar cell upon short circuiting the electrodes of the cell. The J_{sc} is area dependent and can also be influenced by optical properties such as absorption and reflection.

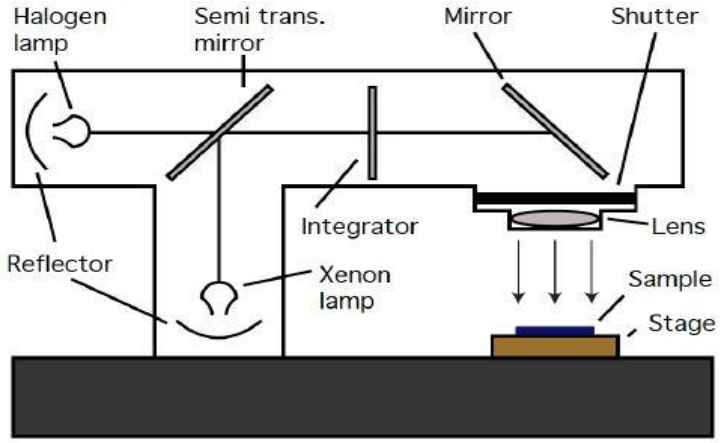


Figure 13: Schematic diagram of the Illuminated JV measurement setup[58].

The open circuit voltage (V_{oc}) is the maximum voltage delivered by the solar cell when the external circuit does not experience any current flow through it. It can be described by equation (2.6),

$$V_{oc} = \frac{k_b T}{q} \ln\left(\frac{J_{ph}}{Jo} + 1\right) \tag{2.6}$$

The fill factor is the ratio of the maximum power produced by the solar cell to the product of Voc and Jsc and can be calculated by equation (2.7),

$$FF = \frac{J_{mpp} V_{mpp}}{J_{sc} V_{oc}} \tag{2.7}$$

Where J_{mpp} and V_{mpp} are the short circuit current density and open circuit voltage at the maximum power point of the solar cell.

The conversion efficiency (η) of a solar cell is defined as the ratio of the maximum generated power to the incident power. It can be calculated as per equation (2.8).

$$\eta = \frac{J_{mpp} V_{mpp}}{I_{in}} = \frac{J_{sc} V_{oc} FF}{I_{in}} \tag{2.8}$$

2.2.3 External Quantum Efficiency (EQE) Measurement

The external quantum efficiency (EQE) is defined as the ratio of number photons collected by the absorber of the solar cell to the number of photons of a certain energy incident on the solar cell. EQE is a wavelength dependent phenomenon and it can be measured by the illumination of a solar cell using a monochromatic light source and measuring the photocurrent (I_{ph}) through the cell. The EQE can then be calculated from I_{ph} as per equation (2.9).

$$EQE(\lambda) = \frac{I_{ph}(\lambda)}{q\varphi_{ph,\lambda}} \tag{2.9}$$

Where q is the elementary charge and $\varphi_{ph,\lambda}$ is the spectral photon flux incident on the cell.

EQE at a particular wavelength is unity if all the photons of a certain wavelength are absorbed and the resulting minority carriers get collected. The ideal square shape of the EQE curve of a solar cell is reduced due to the recombination losses and parasitic absorption experienced by the cell.

The EQE measurement in this project has been carried out using a spectral response setup that consists of a chopper frequency generator, the light source – a xenon gas discharge lamp, the monochromator, the lens system, a mounting frame to place the solar cell, a lock-in amplifier, power supply and contact probes with gold tips. 300nm to 1200nm is the wavelength range relevant for the performance of c-Si solar cells.

The EQE setup can also be used for the determination of the short circuit current density (J_{sc}) of the solar cell. Spectral response setups can provide a more accurate J_{sc} measurement in comparison to the J-V measurement setup explained in the previous section. The J_{sc} is obtained by integrating the product of EQE and photon flow at a certain wavelength across all relevant wavelengths (300nm to 1200nm) as seen in equation (2.10).

$$J_{sc} = q\int_{\lambda_1}^{\lambda_2} EQE(\lambda)\varphi_{ph,\lambda}^{AM1.5}d\lambda \tag{2.10}$$

3

Optimisation of poly-SiO_x passivating contacts

This chapter discusses the optimisation of poly-SiO_x passivating contacts. For this purpose, three types of symmetric contacts: n-type textured, p-type flat/polished and p-type textured as shown in Figure 14 were utilised. Section 3.1 looks into preparation of the symmetric samples followed by sections 3.2 and 3.3 which discusses the properties and growth techniques of the tunnel oxide layer respectively. Section 3.4 looks into the high temperature annealing step. Sections 3.5 and 3.6 discusses the optimisation of thermal budgets for tunnel oxide growth and high temperature annealing. Section 3.7 is an overview on the optimal thermal budgets and annealing conditions obtained from the optimisation performed. Section 3.8 covers the implementation of various hydrogenation techniques used for further enhancement in passivation. Section 3.9 looks into passivation tests performed post TCO deposition. Finally section 3.10 is an overview of the findings presented in this chapter.

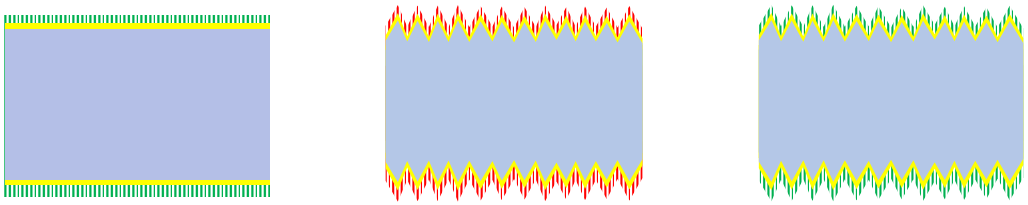


Figure 14: Symmetric Contacts for optimisation. From left to right: p-type flat, n-type textured and p-type textured.

3.1 Preparation of symmetric samples

A pictorial representation of the sequential steps involved in the preparation of the n-type textured symmetric contacts can be seen in Figure 15. The preparation of the p-type textured contacts will follow the same procedure with a change in dopant type and that of p-type flat symmetric contacts would be identical to the p-type textured contacts but would be devoid of texturing. The symmetric samples used for the optimization have been prepared using the following steps:

- The project makes use of both double side polished and double side textured n-type Float Zone (FZ) c-Si wafers with a thickness of approximately 280µm and <100> surface orientation. Double side textured wafers are obtained by immersing the double-side polished or flat wafers in an aqueous solution composed of TMAH and ALKA-TEX at a

temperature of 80 °C for approximately 15 minutes. This results in the formation of random pyramids on the surface of the wafers. This is followed by a poly-Si etch treatment for 2 minutes in order to round the edges of the pyramids which is known to slightly improve the passivation quality.

- The wafers are then made to undergo one round of standard cleaning in order to remove the organic and inorganic contaminants. This is followed by the Marangoni drying and cleaning step to remove the native oxide layer before the placement of the wafers in the oxidation furnace for the subsequent step.
- The tunnel oxide layer (SiO_x) is grown by the method of dry thermal oxidation. The optimisation of the growth conditions of SiO_x will be discussed in detail in the upcoming sections.
- The intrinsic amorphous Si ((i)a:Si:H) layer is grown in an LPCVD furnace at a deposition rate of 2nm/min. A deposition time of 5 min is utilised to deposit the layer which results in the formation of a 10nm thick layer on polished wafer surfaces. In the case of textured surfaces, the thickness would be reduced by a factor of 1.7.
- The doped a-SiO_x:H layers are deposited by PECVD by making use of the doping gases B_2H_6 for p-type contacts and PH_3 for n-type contacts.
- Post the PECVD process, the samples undergo high-temperature annealing in order to crystallize the a-SiOx:H layers and activate the dopants resulting in the formation of poly-SiO_x layers.
- Finally, the hydrogenation technique of SiN_x-FGA is performed on the samples to further enhance the passivation
- The implied V_{oc} (iV_{oc}) of the prepared samples are measured using Sinton WC-120 lifetime measurement setup.

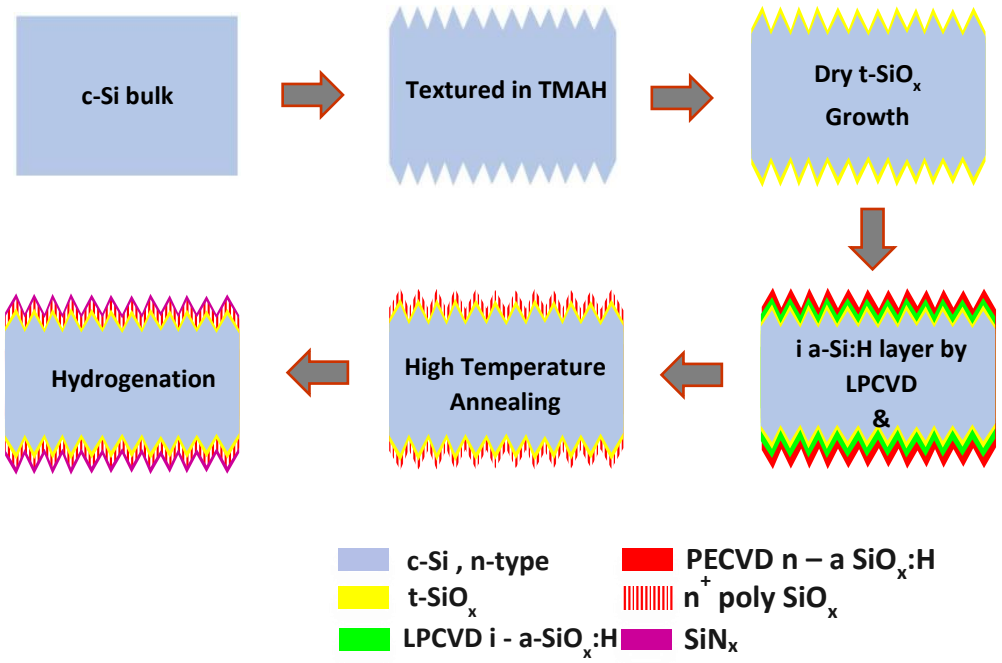


Figure 15: Preparation of n-type textured symmetric samples

3.2 Interfacial tunnel oxide layer (SiO_x)

The inclusion of the tunnel oxide layer (SiO_x) has resulted in a significant improvement in the passivation quality of solar cells due to the low c-Si/SiO_x interface defect densities [59]. The SiO_x layer is designed to facilitate efficient tunnelling of majority carriers to ensure a good fill factor. At the same time, the tunnel oxide layer acts as a hindrance to the minority carrier from reaching the poly-SiO_x layer. The reason for the inefficient tunnelling of minority carriers through the interfacial oxide layer is due to the difference in tunnelling barrier heights. In the case of n-type poly-Si/c-Si junctions, the difference in band offsets between SiO_2 and c-Si ie; 4.8 eV for the valence band and 3.1 eV for the conduction band implies that holes which are the minority carriers have a larger barrier to cross [60][61].

The ideal thickness regime for the SiO_x layer was found to between 1.2 nm to 1.5 nm [49].Thicker SiO_x (> 1.6nm) layers resulted in higher contact resistivity in the metal/poly-Si/SiO_x/*c*-Si stack which in turn results in poor tunnelling properties [62]. Exposure of thin SiO_x layer (< 1.2nm) to high temperature processes leads to the formation of pinholes although the dominant transport method is tunnelling. In the case of oxide layers(>1.2nm) charge carrier transport is also facilitated by pinholes which are formed by the thermal stress induced on the oxide layer during high temperature annealing [63]. POLO (Poly-Si on Oxide) structure solar cells make use of very thick tunnel oxide layers (>2nm) and the dominant transport mechanism is pinholes as the oxide layer is too thick for tunnelling [64].

3.3 Methods of tunnel oxide growth

The growth of tunnel oxide layer on the c-Si bulk can be facilitated by various methods such as wet chemical oxidation, UV/ozone photo-oxidation and dry thermal oxidation. The wet chemical oxidation method of NAOS (Nitric Acid Oxidation of Silicon) has been the preferred choice of method in the PVMD group. However, wet tunnel oxide layers have proven to show a high leaky interface which can significantly increase the out diffusion of dopants towards the c-Si bulk [65].On the other hand, thermal oxidation results in a more uniform, denser and less porous film with higher dielectric strength in comparison to wet oxide. Another major difference between dry and wet oxide is the growth rate, dry thermal oxide grows much slower than wet oxide [66]. Taking these factors into account, this project utilises the method of dry thermal oxidation for the growth of the interfacial tunnel oxide layers.

3.4 High Temperature Annealing

Thermal annealing facilitates the transition of doped a:SiO_x:H films into crystallized poly-Si along with changes in the thickness regime of the tunnel oxide layer. Although prolonged annealing leads to crystallisation, temperatures higher than 1000 °C have known to rupture the tunnel oxide layer with a significant drop in thickness well below the ideal value (1.2nm – 15nm) [49][67]. The variation in iV_{oc} observed upon altering the annealing conditions is the result of a surplus or inadequate in-diffusion of the dopants to the c-Si bulk. Longer annealing times can disrupt the tunnel oxide layer and facilitate excessive diffusion of dopants into the c-Si bulk which can serve as grounds for excessive recombination at the interface and thus deteriorating the chemical passivation [68]. On the other hand, field effect passivation can be

restricted by the lower annealing times which serve as grounds for insufficient dopant diffusion to the c-Si bulk. The gradient formed within the poly-SiO_x layer due to insufficient diffusion deteriorates the band bending required for development of a high built-in voltage [50]. The thickness of the tunnel oxide layer affects the extend of diffusion of dopants from the poly-Si layer to the c-Si bulk during high temperature annealing. In addition to this, extended annealing above 1000˚C are also known to create local breakage in the tunnel oxide layer which can serve as a direct contact between the c-Si and doped layer which reduces the carrier selectivity[49]. Previous research in the PVMD group has shown that using temperatures between 850˚C– 950˚C for time intervals of 5-90 minutes would be the ideal thermal annealing conditions to obtain excellent passivation [69][70].

3.5 Optimisation of tunnel oxide growth and annealing conditions

As mentioned in section 3.1, the first layer being grown on the wafer surface is the tunnel oxide layer using dry thermal oxidation. The optimisation of the thermal budget of the growth conditions is highly relevant as minute changes can drastically alter the thickness. Previous research within the group has shown that temperatures between 600 °C to 675 °C resulted in 1- 2nm thick oxide layers which are sufficient for optimal tunnelling [71], [72]. Thus, as a starting point, thermal budget combinations at 675 °C for different time intervals were used to grow the tunnel oxide layer. Table 2 comprises of the different thermal budgets that were used to optimise the oxide growth condition. The second critical step involved in the optimisation of the symmetric samples would be the identification of the ideal annealing thermal budget conditions. Thermally grown oxide layers have the ability to with stand higher temperatures in comparison to those grown via wet oxidation and thus annealing has been performed at 950 °C for three different time intervals – 5min, 10 min and 15min.The specific temperature and time combinations have once again been adopted based on previous research [72]. It is to be noted that the subsequent steps between the oxide growth and annealing ie; the intrinsic a-Si layer growth and doped a-SiO_x:H layer deposition remains unchanged for all the samples.

Table 2: Thermal Budgets used for Tunnel Oxide Growth

Serial No.	Thermal Budget
1	675˚C 2 minutes
2	675˚C 3 minutes
3	675˚C 4 minutes
4	675˚C 6 minutes
5	675˚C 8 minutes

3.6 Results

3.6.1 p-type flat symmetric samples

Figure 16 represents the iV_{oc} measured for p-flat symmetric samples with tunnel oxides grown at different thermal budgets followed by high temperature annealing at 950 °C for three different time intervals. It is evident from the figure that a maximum iV_{oc} of 691mV was obtained for three tunnel oxide thermal budgets of 675 °C 3 minutes, 675 °C 2 minutes and 675 °C 6 minutes when annealed at a temperature of 950 °C for 10 minutes. A drop in iV_{oc} could be observed for the annealing times of 5 minutes and 15 minutes. The occurrence of a restricted passivation for shorter and longer annealing times can be explained by the insufficient and over-diffusion of dopants respectively to the c-Si bulk. In addition to this, longer annealing time can also disrupt the tunnel oxide layer. Although the optimum annealing condition was found to be 950°C 10 minutes , the ideal tunnel oxide growth thermal budgets would be chosen among the best combinations based on the results of the n-type textured contacts as ultimately the single side textured FBC solar cells require identical tunnel oxide growth conditions for the n-type and p-type contacts.

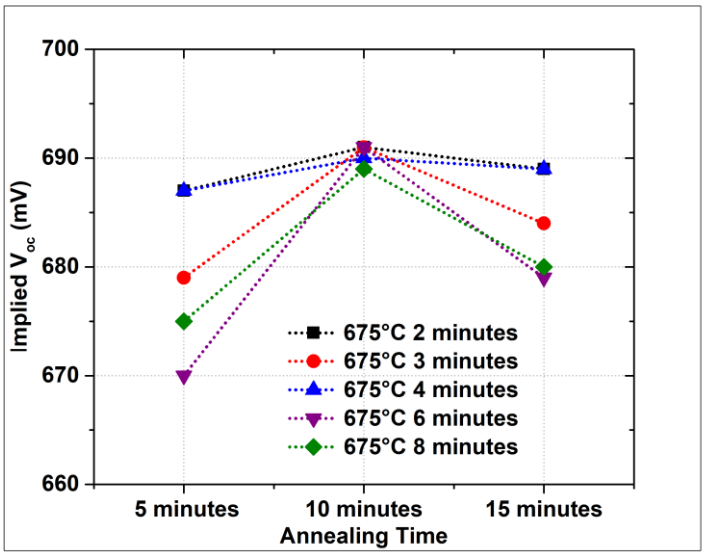


Figure 16: Optimisation of thermal budgets of tunnel oxide growth and high-temperature annealing for p-type flat contacts (Dotted lines are used for visual understanding of the trend)

3.6.2 n-type textured symmetric samples

The larger surface area of textured surfaces which is approximately 1.7 times higher than planar surfaces, results in a relatively thinner layer of SiO_x being grown during thermal oxidation. Texturing can also introduce additional defects and thus alleviating the improvements in optical properties by the additional recombination induced on the silicon surface [73]. The non-homogeneity in oxide layer thickness is also a consequence of thinner layers being grown at the valleys of pyramids on the textured surfaces [65].Owing to this, significant differences can be seen in the iV_{oc} measured for samples that have the tunnel oxide grown at different thermal budgets.

Figure 17 demonstrates the passivation levels indicated by the iV_{oc} for different thermal budgets of oxide growth and high-temperature annealing. It can be observed that the thermal budget of 675 °C 6 minutes gave the highest V_{oc} of 689mV when annealed at 950 °C for 10 minutes with a decrease in the passivation quality when the annealing time was prolonged or restricted.

The thermal budget of 675 °C 3 minutes which was one of the optimum thermal budgets in the case of p-type flat contacts did not give similar results in the case of n-type textured samples. The highest iV_{oc} obtained when using the thermal budget of 675 °C 3minutes was 666 mV when annealed at 950 °C 10 minutes. An increasing trend in iV_{oc} can be observed when moving from thermal budgets of 675 °C 2 minutes to 657 °C 6 minutes followed by a drop in iV_{oc} further ahead. This trend in iV_{oc} could be due to the variation in thickness of the tunnel oxide layer being grown which in turn affects the dopant diffusion by creating a larger barrier for the dopants when the layer is too thick and negligent barrier when the layer is too thin. Annealing times of 15 minutes and 5 minutes resulted in a drop in passivation.

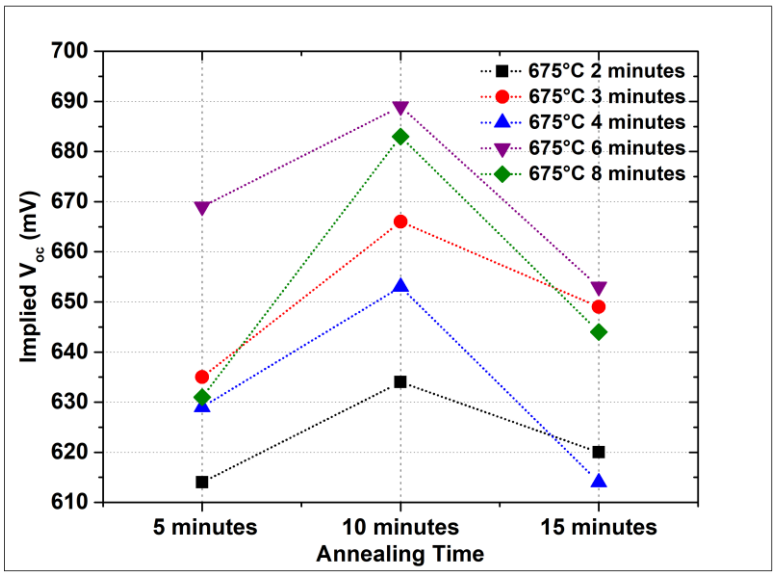


Figure 17: Optimisation of thermal budgets of tunnel oxide growth and high-temperature annealing for n-type textured contacts (Dotted lines are used for visual understanding of the trend)

3.6.3 p-type textured symmetric samples

The size and diffusivity of the Boron (for p-type doping) in comparison to Phosphorous (for n-type doping) as can be seen in Table 3 indicates that Boron diffuses faster than Phosphorous [74][75]. A decrease in surface passivation arises from the excessive diffusion of Boron through the tunnel oxide due to the formation of defects in the oxide layer combined with a shallow junction formation [76]. The compromised passivation quality combined with the defects introduced by texturing makes the optimisation of p-type textured samples rather challenging. The poor passivation obtained as a result of these factors makes the implementation of p-type textured layers, the primary limiting factor in the fabrication of double side textured FBC solar cells that make use of these specific contacts. In order to

improve the passivation quality of p-type textured samples, a few additional experiments were performed besides the optimisation of the thermal budgets. As a starting point, all the thermal budgets and annealing conditions used in the case of p-type flat and n-type textured symmetric samples were implemented in the case of p-type textured wafers as well. Upon obtaining the ideal thermal budget conditions for SiO_x growth and annealing conditions, further experiments were conducted.

Table 3: Size and diffusivity of dopants

Dopant Type	Size (pm)	Diffusivity(cm^2/s)
Boron (B)	180	6+- 10-2
Phosphorous (P)	195	8+-5 10-4

Figure 18 shows results from the first round of tests performed on the p-type textured samples. It can be seen that the thermal budget of 675 °C 3 minutes annealed at 950 °C 10 minutes gave the highest iV_{oc} of 638mV. It is very evident from the trend that the values obtained for the other thermal budgets are much lower than what was seen in the previous cases pf p-type flat and n-type textured symmetric contacts. Further annealing tests at 950 °C 5 minutes and 950 °C 15 minutes did not improve the passivation any further instead it only dropped even more. However, having obtained 675 °C 3 minutes as the optimal thermal budget, further methods of improving the passivation have been performed using the same.

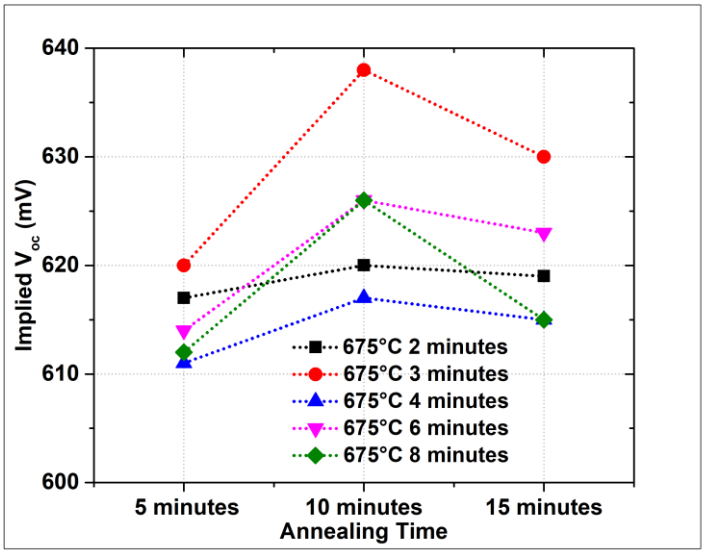


Figure 18: Optimisation of thermal budgets of tunnel oxide growth and high-temperature annealing for p-type textured contacts (Dotted lines are used for visual understanding of the trend)

3.6.4 Methods of improving the passivation of p-type textured contacts

3.6.4.1 LPCVD layer thickness

The poly-SiO_x/c-Si interface facilitates field effect passivation by the presence of dopants within the poly-SiO_x layer that induces strong band-bending and prevents the minority carriers from reaching the interface. The thickness of the intrinsic a-Si:H layer which is transformed into doped poly-SiO_x during high thermal annealing plays a vital role in achieving desired passivation. In addition to the deposition time of 5 minutes which gave an approximate layer thickness of 10nm on flat surfaces, three other layer thicknesses:- 6nm, 14nm and 20nm were also tested to check if any improvements in iV_{oc} could be obtained upon altering the thickness of the intrinsic layer. All the samples were prepared using a tunnel oxide layer grown at 675 °C 3 minutes and all the other steps involved in the sample preparation remained identical with the variable factor being the LPCVD layer thickness. Once again, the samples were annealed at 950 °C for 5 minutes, 10minutes and 15minutes.

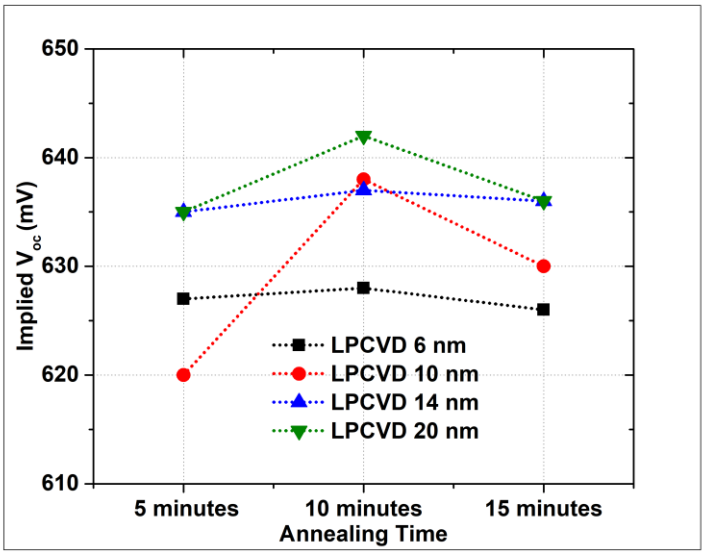


Figure 19: Optimisation of thickness of LPCVD grown intrinsic a-Si layers (Dotted lines are used for visual understanding of the trend)

Figure 19 depicts the iV_{oc} obtained for the samples that made use of different LPCVD i-a-Si layer thicknesses when annealed at 950 °C for three different intervals. An increasing trend in iV_{oc} can be observed upon varying the layer thickness from 6nm to 20 nm. Once again, the maximum passivation is attained for an annealing condition of 950 °C 10 minutes in all the four cases. The thin layer of intrinsic a-Si with a thickness of 6nm, could serve as grounds for over-diffusion of dopants or Boron atoms to be specific owing to their small size and diffusivity which enables them to easily penetrate through the poly-SiO_x layer, which increases the defect density at the SiO_x/c-Si interface which in turn lowers the carrier selectivity. The loss of passivation evident by the relatively lower V_{oc} value of 628mV when annealed at 950 °C 10 minutes explains this. In addition to this, although an improvement in passivation with an iV_{oc} of 642mV can be seen when using a thickness of 20nm, it is not feasible to use such thick layers as they can serve as grounds for high levels of parasitic absorption which can

significantly decrease the short circuit current of the solar cell. Having observed the passivation results obtained for the different intrinsic layer thicknesses, 10nm a-Si intrinsic layer that uses a deposition time of 5 minutes was chosen as the optimum taking into account all the factors.

3.6.4.2 Two-step annealing

The thickness of the interfacial tunnel oxide layer is a primary determinant of the type of dominant conduction that takes place through it. Carrier transport in a tunnel oxide layer can be facilitated via tunnelling or local pinhole formation. Literatures on experimental and simulation based analysis have shown that the presence of pinholes in oxide layers (>1.2nm) formed upon thermal annealing at high temperatures can indeed improve the Fill Factor (FF) and reduce the sheet resistance (Rs) [33]. Although a moderate level of pinhole density can improve the carrier tunnelling, excessive pinhole formation can result in high levels of dopant leakage into the c-Si bulk during thermal annealing [77]. In addition to this, studies have shown instances where high temperature does not result in complete crystallisation of the poly-Si layer which can infact limit it's dopant diffusion ability [78][79].

A two-step annealing scheme was implemented on the p-type textured symmetric samples with the goal of creating sufficient pinholes and complete crystallisation of the poly-SiO_x layer. The tunnel oxide layer was once again grown at the thermal budget of 675 °C 3 minutes followed by the intrinsic a-Si growth (10nm). The first annealing step was introduced after the intrinsic layer deposition, at a high temperature for very short durations sufficient to create pinholes or localised current flow regions and initiate crystallisation of the intrinsic a-Si layer. Temperatures within the range of 900 °C to 1000°C were tested for different time intervals ranging from 30 seconds to 2 minutes. This particular step was performed right after the LPCVD process in order to ensure that the extend of pinhole conduction was not influenced by the dopant diffusion of P or B. Upon the first round of annealing, doped a-SiO_x:H layers were deposited via PECVD and the samples are once again exposed to thermal annealing at a temperature of 950 °C for 5minutes, 10 minutes and 15minutes.

Figure 20 illustrates the iV_{oc} obtained for the samples fabricated different two-step annealing schemes. Results show that the first step annealing performed at 950 °C for 1 minute in combination with the second step annealing at 950 °C for 10minutes gave the highest improvement in iV_{oc}. A significant rise of approximately 27mV from the previously obtained 638mV was observed in this case with the final value resulting in an iV_{oc} of 663mV. The first step annealing conditions of 1000 °C 30seconds and 900 °C 2 minutes were also in close proximity. The optimum annealing conditions were chosen to be 950 °C 1 minute in combination with 950°C 10 minutes as the first and second steps respectively. It is also worth mentioning that although the improvement in passivation could be a combined effect of pinhole creation and complete crystallisation, the major contributing factor could be the latter as the extend of pinhole development is not certain with such short annealing times used in the first step.

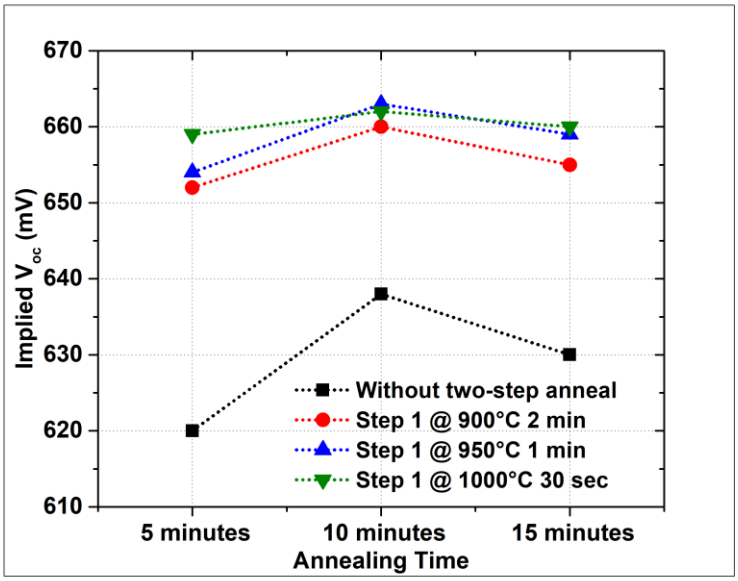


Figure 20: Optimisation thermal budgets of two-step annealing process for p-type textured contact (Dotted lines are used for visual understanding of the trend)

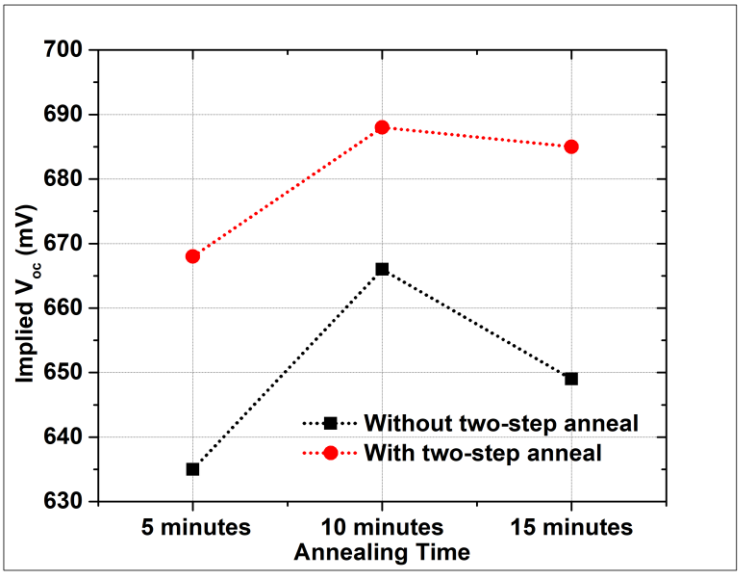


Figure 21: Optimisation of thermal budgets for two-step annealing process for n-type textured contacts (Dotted lines are used for visual understanding of the trend)

Having seen an improvement in the passivation quality of the p-type textured sample, the optimum two-step annealing process was repeated on the n-type textured samples with the tunnel oxide grown at 675 °C 3 minutes as the double side textured FBC solar cells to be fabricated will make use of both n and p contacts and a similar oxide growth thermal budget. The optimum annealing time of 950 °C 1 minute was utilised for the first round of annealing. This was followed by the second round of annealing at 950 °C for 5 minutes, 10 minutes and 15 minutes. Figure 21 shows the improvement in passivation quality of n-type textured

contacts with the inclusion of the two-step annealing scheme. A final iV_{oc} of 688 mV was observed with a final annealing step at 950 ° C 10 minutes which constitutes to an increase of 22 mV . A loss in iV_{oc} is observed for lower and longer annealing times..

3.6.4.3 High Temperature Oxidation (HTO)

G. Limodio et al. [80] proposed a wafer cleaning approach that makes use of High Temperature Oxidation (HTO) combined with a consequent step of SiO_2 etching in HF solution. The HTO results in the confinement of organic and metallic contaminants within the SiO_2 layer which can be removed during the etching process along with the implementation of impurity gettering which proved to improve the passivation quality of textured wafers.

For the implementation of this approach, post texturing and standard cleaning the wafers were introduced to an oxidation step that resulted in the formation of a SiO_2 layer with an approximate thickness of 250 nm. Prolonged oxidation at high temperatures showed an improvement the lifetime and iV_{oc} of the samples[80]. Post oxidation, the samples were etched in an HF solution till the surfaces turned hydrophobic to remove the SiO_2. Upon removal of the SiO_2 layer, the wafers were once again subjected to three rounds of standard cleaning followed by Marangoni Drying. Once the wafers were cleaned and dried, thermal oxide was grown at 675 °C 3 minutes followed by an intrinsic a-Si layer deposition in LPCVD and doped a-SiO_x:H layers in PECVD. Lastly the samples were annealed at 950 °C at three different time intervals of 5 minutes, 10 minutes and 15 minutes.

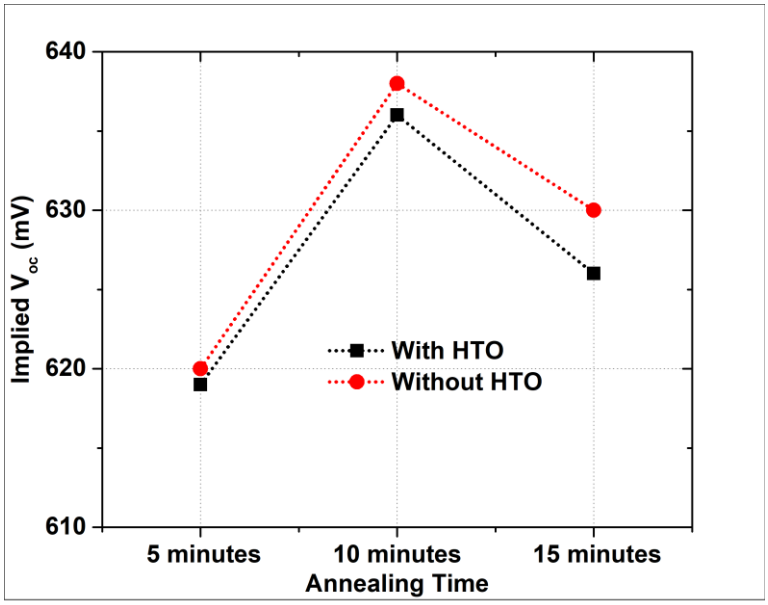


Figure 22: Optimisation of annealing conditions for p-type textured contacts using HTO (Dotted lines are used for visual understanding of the trend)

Figure 22 shows the passivation results obtained upon implementing the HTO process. It is evident that the highest V_{oc} of 636 mV was obtained for an annealing condition of 950 °C 10 minutes which is very close to the previous scenario of 638 mV obtained without the application of the HTO process. Although an improvement in chemical passivation was

expected owing to the removal of contaminants from the c-Si surface and the rounding of the pyramid tips of the textured surface upon etching the SiO_2 layer, no significant improvement was observed in this case as can be seen from the iV_{oc} value for the optimum annealing time and temperature. As a result, it was decided to not go forward with this additional cleaning step during the sample preparation.

3.7 Choice of optimum thermal budgets

The fabrication of high-efficiency solar cells requires a common thermal budget for tunnel oxide growth and high temperature annealing to be performed on the front and rear contacts. Table 4 is an overview on the optimum thermal budgets for tunnel oxide growth and high temperature annealing conditions that would be utilized for further processing. The p-type flat and n-type textured poly-SiO_x passivating contacts that would be implemented in a single side textured FBC solar cell structure would make use of the thermal budgets of 675 °C 6 minutes for the tunnel oxide growth and 950 °C 10 minutes for high temperature annealing.

The n-type textured and p-type textured poly-SiO_x passivating contacts to be used for the double side textured FBC solar cell will make use of the thermal budgets of 675 °C 3 minutes for the tunnel oxide growth and 950˚C 10 minutes for high temperature annealing. Although, 675 °C 3 minutes was not giving the best results for n-type textured contacts, a compromise had to be made here taking into account the fact that p-type textured samples underperformed for all the other thermal budgets. In addition to this, the two-step annealing would also be implemented on both the contacts in adherence with the improvement in passivation obtained in section 3.6.4.2.

Table 4: Optimum thermal budgets for solar cell fabrication.

Solar Cell Type	**Contact Type**	**Thermal Budgets**	
		SiO_x Growth	**High Temperature Annealing**
Single Side Textured	p-type flat	675°C 6 minutes	950°C 10 minutes
	n-type textured	675°C 6 minutes	950°C 10 minutes
Double Side Textured	p-type textured	675°C 3 minutes	950°C 10 minutes
	n-type textured	675°C 3 minutes	950°C 10 minutes

3.8 Hydrogenation

Further enhancement in passivation is attained by the method of hydrogenation that makes use of dielectric capping layers followed by thermal annealing that facilitates diffusion of hydrogen present in the capping layers to interfaces and thus providing chemical passivation. The project makes use of two types of hydrogenation techniques. The first SiN_x/FGA implemented on the n-type textured, p-type polished and p-type textured wafers. The second method is AlO_x/SiN_x/AlO_x /FGA-RTP also referred to ANA/FGA-RTP which is only executed on the p-type textured wafers with the sole purpose of improving the passivation of these

samples which act as a limiting factor. The use of a triple capping layer such as ANA has been opted taking into account the combined effects of high hydrogen content of the SiN_x layer and higher effusion barrier provided by the AlO_x layer which can result in maximum hydrogen being available for enhanced passivation effects [81].

The SiN_x/FGA hydrogenation technique makes use of a 120nm thick SiN_x layer deposited using PECVD followed by an FGA furnace annealing at 400 °C for 30 minutes. A deposition time of 8 minutes was used for the flat/polished samples and the textured samples required 13min 36sec to obtain the same thickness of SiN_x layer on flat and textured surfaces. The respective n-type and p-type doped symmetric samples were prepared following the previously optimised conditions and high temperature annealing shown in Table 4.The results presented below only look into the improvement in passivation obtained for the symmetric samples prepared using optimised thermal budgets and annealing conditions as mentioned in Section 3.7.

Figure 23 shows the improvement in passivation that has been obtained upon implementing the SiN_x/FGA hydrogenation scheme. In the case of p-type flat/polished samples with a tunnel oxide layer grown at a thermal budget of 675 °C 6 minutes, a 20mV increase was observed with the initial iV_{oc} of 691mV rising to a final value of 711mV.The n-type textured samples with a tunnel oxide layer grown at 675 °C 6 minutes exhibited a 20mV increase in iV_{oc} similar to the case of p-type flat samples, with a final of 709mV attained post SiN_x/FGA.

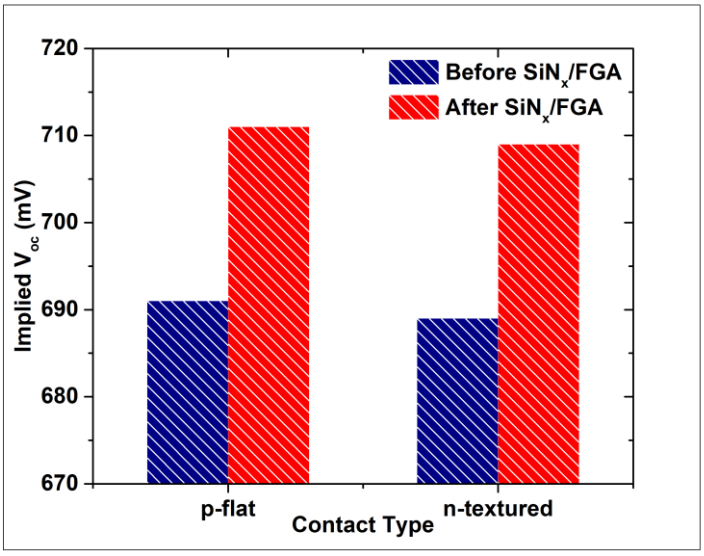


Figure 23: Passivation property of n-type textured and p-type flat contacts post hydrogenation

The p-type textured and n-type textured samples with a tunnel oxide layer grown at 675 °C 3minutes were exposed to hydrogenation with and without the implementation of the two-step annealing process. Figure 24 shows the results obtained post hydrogenation with and without the use of the two-step annealing scheme. For the samples devoid of the two-step annealing, the p-type textured contacts showed a 30mV increase post SiN_x/FGA resulting in a final iV_{oc} of 668mV. With respect to the n-type textured contacts, the improvement in iV_{oc} was

only 13mV with a final iV_{oc} of 679mV. The relatively smaller increase in iV_{oc} could be due to the trade-off made in picking the thermal budget condition for n-type textured contacts.

The p-type textured contacts prepared using the two-step annealing process showed an improvement of 24mV with the iV_{oc} rising from 663m to 687mV. However, a very negligible improvement of 3mV was observed in the case of n-type textured contacts fabricated using the two-step annealing process. This could be due to the fact that the samples have already reached a saturation point with respect to their chemical passivation and field effect passivation.

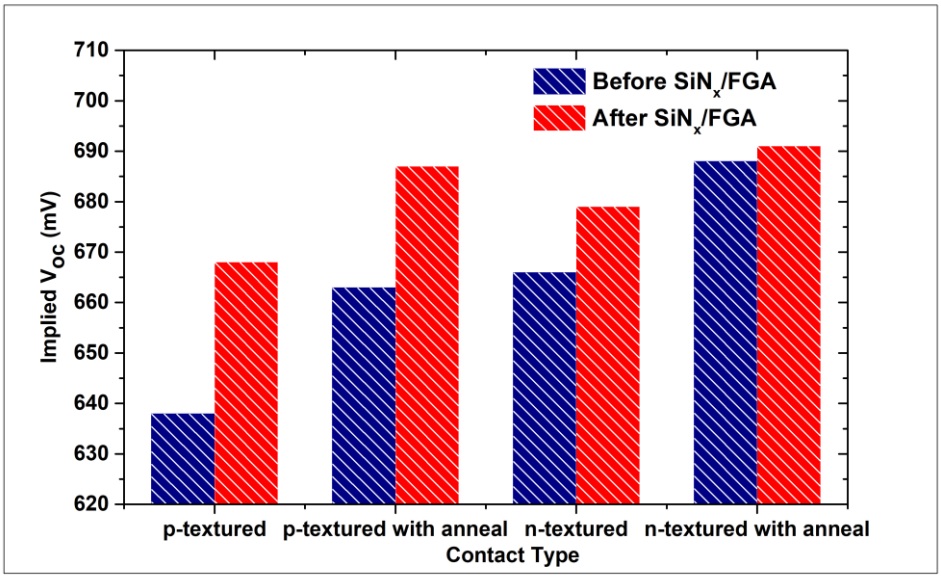


Figure 24: Passivation property of n-type textured and p-type textured contacts post hydrogenation

$AlO_x/SiN_x/AlO_x$/FGA-RTP or ANA/FGA-RTP, the second method of hydrogenation makes use of a deck of triple capping layers with three annealing steps performed sequentially. AlO_x layer is grown on both sides of the sample using ALD at a temperature of 105 °C. A 6.5nm thick layer of AlO_x is obtained on flat samples using a deposition cycle of 100. Post this the wafer is exposed to a round of RTP annealing at 600 °C for 10 minutes in N_2 atmosphere. This is followed by the deposition of a layer of SiN_x (120nm) and another round of AlO_x which corresponds to second and third layer respectively. The samples were then exposed to a round of FGA annealing at 400 °C for 30 minutes followed by one last round of RTP annealing in FGA at a temperature of 650 °C for 10minutes. It is to be noted that the thermal budgets used for RTP annealing were adapted from a previous work in the PVMD group [72].

The p-type textured samples used for this test were fabricated using a tunnel oxide layer grown at 675°C 3 minutes but without the inclusion of the two-step annealing scheme. Figure 25 shows the passivation attained upon using the two methods of hydrogenation. Having implemented the triple capping layer technique on the p-type textured samples, an increase of 30mV was observed with a final iV_{oc} of 668mV. The improvement in passivation was identical to what is obtained when using the SiN_x/FGA technique without the two-step

annealing scheme. Owing to the lack of additional improvements and long processing time of ANA, no further tests were conducted.

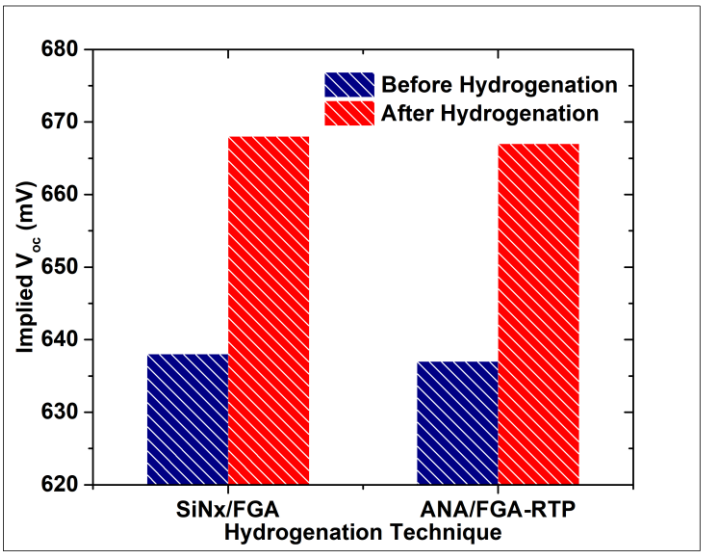


Figure 25: Passivation property of p-type textured contacts post hydrogenation

3.9 Passivation tests post TCO deposition

A significant deterioration in passivation levels is observed upon TCO deposition on thin poly-Si based solar cells owing to the sputtering damages induced during TCO deposition [82]. Can et al. [82] showed that post deposition annealing at 400 °C for 1 hour in H_2 can effectively help in the recovery of passivation quality in addition to the favourable alteration in opto-electrical properties of TCO layers which result in contact resistivities lower than 20 mΩ cm^2 for poly-Si/TCO contacts.

Prior to the direct implementation of TCO layers on solar cell precursors, symmetric poly-SiO_x contacts were first tested to get an estimate of the loss in passivation to be observed post TCO deposition. To begin with, the previously optimised n-type textured and p-type polished poly-SiO_x contacts with tunnel oxide layers grown at 675˚C 6 minutes and annealed at 950˚C 10 minutes followed by hydrogenation using SiN_x/FGA which would be implemented in single side textured FBC cells were used for this test. ITO layers utilised as the TCO was deposited on n-type textured and p-type flat contacts without the use of a hard mask by RF magnetron sputtering. Thicknesses of 75nm and 150nm were utilized for the n-type textured and p-type polished contacts respectively. It is to be noted that a BHF etch was performed on these samples prior to ITO deposition in order to remove the SiN_x layer deposited during hydrogenation. Post ITO deposition, thermal annealing was performed at 400 °C for 1 hour in H_2. The loss and recovery in passivation quality post ITO deposition and thermal annealing were measured using Sinton lifetime measurement setup.

Figure 26 demonstrates the variation in passivation indicated by the iV_{oc} obtained after subsequent steps for the p-type flat and n-type textured poly-SiO_x passivating contacts starting from high temperature annealing upto thermal annealing in H_2 performed post ITO deposition. A drop of approximately 20mV could be observed for the n-type textured contact

post ITO deposition. On the other hand, the p-type polished contact exhibited a drop of around 30mV post ITO deposition. Based on these results, a net drop of approximately 50mV is estimated upon ITO deposition on single side textured FBC cells that would be discussed in Chapter 4. The thermal annealing at 400 °C for 1 hour improved the passivation by 17mV and 26mV for the n-type textured and p-type polished contacts.

Further optimisation with regards to TCO deposition for the p-type textured and n-type textured poly-SiO_x passivating contacts used for the fabrication of double side textured FBC solar cells would be discussed in Chapter 5 of this report.

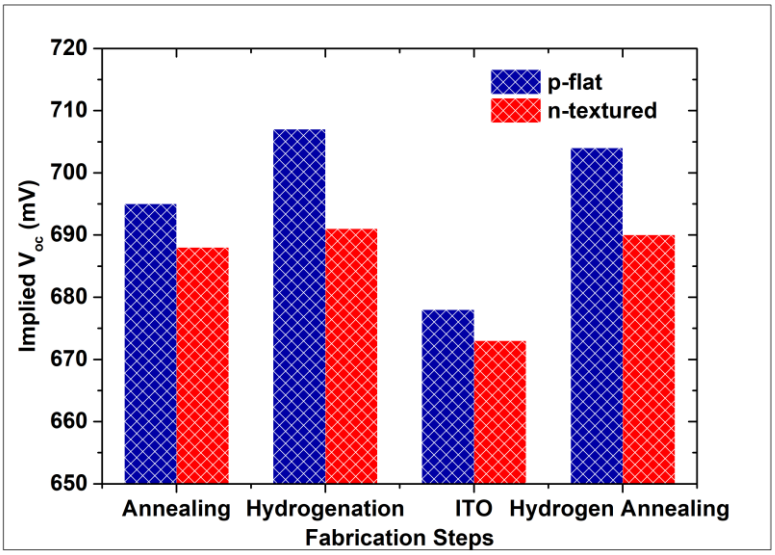


Figure 26: Change in passivation quality of symmetric contacts (for p-type polished and n-type textured poly-SiO_x passivating contacts)

3.10 Overview

This chapter focused on the optimisation of poly-SiO_x passivating contacts. The three types of contacts: n-type textured, p-type flat and p-type textured were optimised with respect to the thermal budgets for tunnel oxide growth and annealing conditions. The most fitting hydrogenation technique was found to be the method of SiN_x/FGA which showed significant improvement in the passivation for all three contacts. Lastly the additional improvisation techniques performed on the p-type textured samples showed that the two-step annealing process gave the maximum improvement in the iV_{oc} and thus it will be adapted for the solar cell fabrication explained in the upcoming sections. In addition to this passivation tests conducted on account of TCO deposition gave an estimate on the drop in passivation to be expected for the FBC solar cells fabricated using the optimised poly-SiO_x passivating contacts.

4

Single side textured FBC solar cells

This chapter discusses the fabrication process and results of single textured FBC solar cells fabricated using the optimised poly-SiO_x passivating contacts. Section 4.1 deals with the fabrication process of the FBC solar cells that use a tunnel oxide layer grown by dry thermal oxidation. Section 4.2 consists of the analysis of the fabricated FBC solar cell and additional process schemes implemented to enhance the overall performance of the solar cells. Section 4.3 looks into the fabrication of single side textured solar cells that make use of a tunnel oxide layer grown by NAOS. The solar cell results have been discussed in Section 4.4. Section 4.5 is a comparison of two single side textured FBC solar cells that use thermal oxidation and NAOS for the tunnel oxide layer growth. Lastly, section 4.6 is an overview of the chapter.

4.1 Fabrication Process

The sequential steps involved in the fabrication of single side textured FBC solar cells have been described below:

- Double side polished n-type FZ wafers with <100 orientation> and a thickness of 280µm have been used as the c-Si bulk.
- One side of the wafer is coated with a thin layer of SiN_x in order to prevent texturing of the surface.
- The wafers are then made to undergo texturing by immersing it in an aqueous solution composed of TMAH and ALKA-TEX at a temperature of 80 °C for 15 minutes.
- Post texturing the wafers are cleaned using DI water and dried in a spin dryer to remove water particles on the surface.
- A BHF dip is introduced in order to remove the SiN_x layer from the polished side of the wafers.
- Post the BHF dip, the wafers undergo a full round of standard cleaning and drying followed by the Marangoni drying to remove the native oxide layer formed on the surface of the wafer.
- The wafers are then exposed to thermal oxidation at 675 °C 6 minutes to facilitate the growth of the tunnel oxide layer. Prior to the oxidation time, a stabilisation time of 5 minutes has been incorporated in the oxidation recipe to ensure that the oxidation takes place at the right temperature. The tunnel oxide is a critical step in fabrication and minute changes in temperature can alter the layer thickness causing detrimental effects.
- The intrinsic amorphous Si ((i)a:Si:H) layer is grown in an LPCVD furnace at a deposition rate of 2nm/min. A 10nm thick layer is grown on polished wafer surfaces. In the case of textured surfaces, the thickness would be reduced by a factor of 1.7.

- After the intrinsic layer deposition, the wafers are processed inside an RF-PECVD chamber for the deposition of the doped a-SiO_x:H layers.The textured front side is deposited with Phosphorous doped a-SiO_x:H and the polished rear side is deposited with Boron doped a-SiO_x:H layers. The layer thicknesses and gas flows of respective gases can be seen in Table 5.
- High temperature annealing at 950 °C 10 minutes has been performed on the wafers to facilitate dopant diffusion and crystallization of doped a-SiO_x layer to doped poly-SiO_x layers.
- The wafers are introduced to the hydrogenation technique of SiN_x-FGA post high temperature annealing. SiN_x is deposited using PECVD on both side of the wafers. The flat side uses a deposition time of 8 minutes and the textured side uses 13min 36seconds to obtain the same thickness. The wafers are then subjected to Forming Gas Annealing (FGA) for 30 minutes at 400 °C.
- Post hydrogenation, the SiN_x layer is removed by a BHF dip prior to the ITO layer deposition. An ITO layer of 75nm is sputtered on the textured front side (n^+poly-SiO_x) followed by 150nm on the rear side (p^+ poly- SiO_x).
- Thermal annealing at 400 °C for 1 hour in H_2 atmosphere in implemented on the wafers to recover the loss in passivation caused by ITO deposition.
- The front and rear metal contacts are enabled on the wafer by Screen Printing of Silver (Ag). The wafers are then annealed in an oven for 30 minutes at 170 °C. This is followed by post metallization annealing step at 350 °C for 10minutes.
- The final parameters of the fabricated solar cells are measured using the illuminated JV measurement and EQE setup and have been discussed in section 4.2.Figure 27 is schematic representation of the fabrication process. Figure 28 is an image of the front an drear side of the fabricated single side textured FBC solar cells

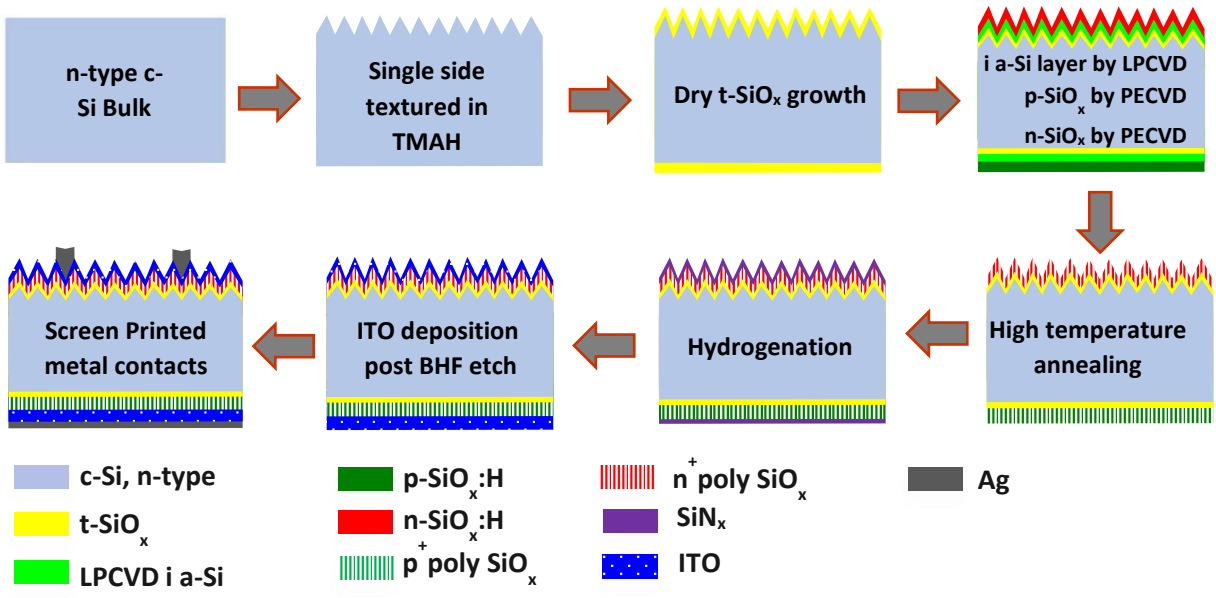


Figure 27: Schematic representation of the fabrication of single side textured FBC solar cell with thermally grown tunnel oxide layer

Table 5: Deposition parameters of the optimised poly-SiO_x contacts

Contact Type	Thickness	Gas Flows			
		SiH_4(sccm)	CO_2(sccm)	B_2H_6/PH_3(sccm)	H_2(sccm)
p-type flat	20nm	8	2	B2H6 = 5	100
n-type textured	20nm	4	6.4	PH3 = 4.8	35

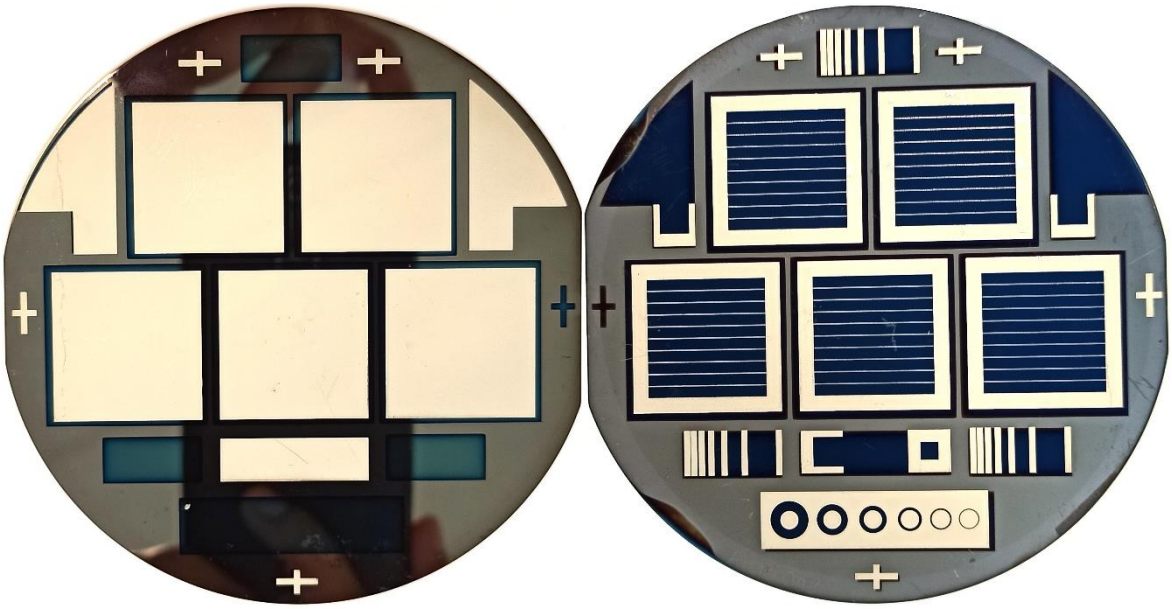


Figure 28: Fabricated Single side textured FBC solar cell. (Left: Screen printed rear side, Right: Screen printed front side)

4.2 Solar cell results

4.2.1 FBC solar cell with a double ITO layer

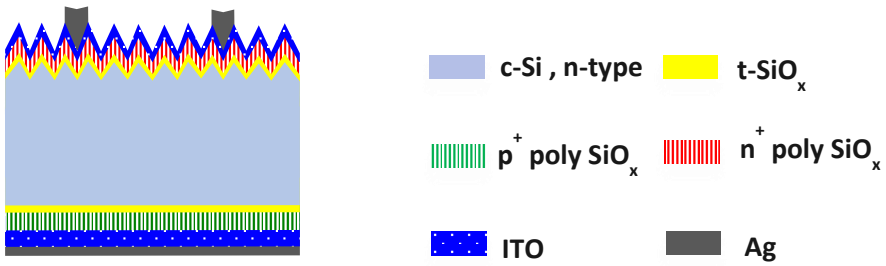


Figure 29 : Schematic structure of FBC solar cell with double ITO layer

This section addresses the results and analysis of the single side textured FBC solar cell that makes use of a thermally grown tunnel oxide layer and a double ITO layer as mentioned in the fabrication process in section 4.1. Figure 29 is a schematic structure of the FBC solar cell with a double ITO layer. Figure 30 is a depiction of the change in passivation of the solar cell after subsequent processing steps measured using the Sinton lifetime measurement setup.

The iV_{oc} 0f 695mV observed post high temperature annealing at 950 °C 10 minutes is well within the average values obtained for individual p-type flat and n-type textured symmetric contacts in section 3.6 of chapter 3. Although there is an increase of approximately 20 mV post hydrogenation (SiN_x/FGA) which implied significant improvement in passivation quality, an overall drop of around 30 mV is measured post ITO deposition. The drop that has been observed here is lower than the estimated value of 40mV obtained from passivation tests conducted on symmetric samples in Section 3.8 of Chapter 3. The disparity that is observed with respect to the passivation loss could arise from fluctuations during sputtering and the difference in wafer used for processing. The post ITO deposition annealing at 400 °C in H_2 for 1 hour helped in an almost complete recovery of the passivation quality which is indicated by an iV_{oc} of 712mV.

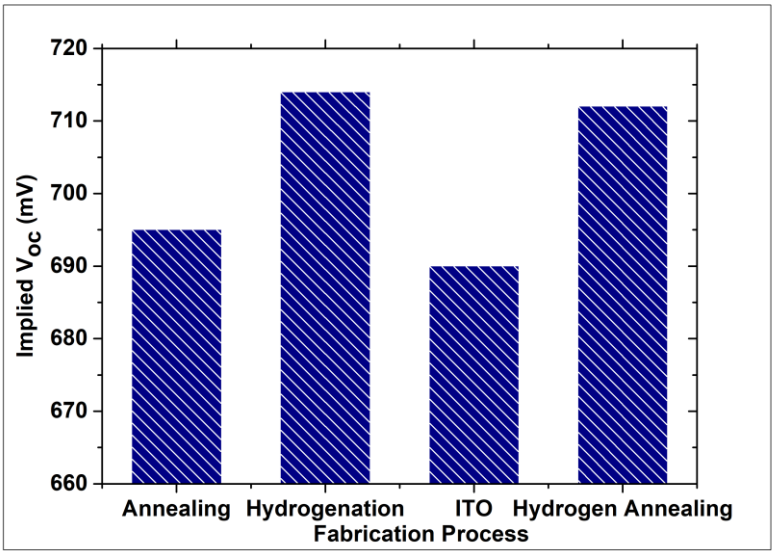


Figure 30: Change in passivation after subsequent steps for double ITO solar cell

The solar cell parameters obtained from the JV measurement and SunsV_{oc} measurement have been presented in Table 6 and Table 7 respectively. Screen printing metallisation resulted in a loss of passivation quality accounted for by the 20mV drop from the previously acquired value of 712mV upon annealing in H_2. In addition to this, the FF is also affected by the high contact resistance and low metal conductivity exhibited by screen printed contacts [83].Post metallisation annealing can benefit the performance of solar cells by an enhancement in FF and decrease in contact resistance [84]. The post metallisation annealing performed at 350 °C for 10 minutes on a hot plate resulted in an absolute 0.72% increase in FF and an absolute increase of 1.41 mA/cm^2 with regards to J_{sc}. A final efficiency of 20.94% has been recorded for the double ITO layer solar cell. The difference in FF and PFF observed from Table 6 and Table 7 respectively, indicates the presence of a high series resistance along the current path from the passivating contact to the metal electrodes.

Table 6: Solar cell parameters from JV measurement

Parameters	V_{oc} [mV]	$J_{sc\ (EQE)}$ [mA/cm^{2}]	FF [%]	(η) [%]
Post Screen Printing	693	36.50	78.88	19.95
Post metallisation annealing	694	37.91	79.60	20.94

Table 7: Solar cell parameters measured from SunsVoc measurement

Parameters	$SunsV_{oc}$ [mV]	PFF [%]	Pη[%]
Post metallisation annealing	713	84.50	22.8

4.2.2 Additional optimisation of process schemes

Despite the high values of V_{oc} and FF 694mV and 37.91% respectively obtained for the double ITO FBC solar cell in section 4.2.1, the efficiency is still limited by the relatively lower values of short circuit current density (J_{sc}) of 37.91mA/cm^{2}. In order to tackle this problem, three additional process schemes were implemented with the goal of improving the overall performance of the solar cell. The use of an anti-reflective coating (ARC), removal of the rear side ITO layer and the replacement of the ITO layer by an IWO layer are the implemented schemes. It is to be noted that all the experiments mentioned above were carried out on reference cells fabricated identically to the solar cell that has been previously analysed in section 4.2.1. Figure 31 depicts the change in passivation obtained after subsequent processing steps starting from high temperature annealing upto thermal annealing in H_2 post TCO deposition for the solar cells discussed in this section.

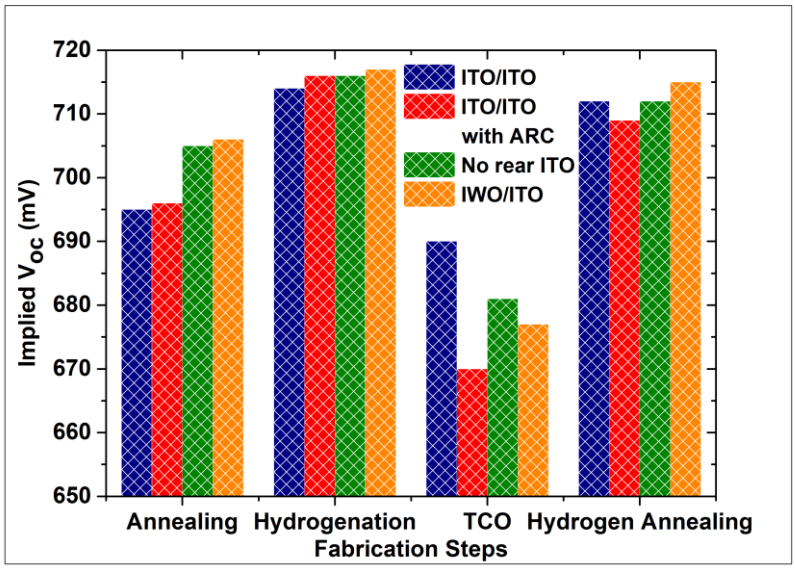


Figure 31: Change in passivation quality of fabricated solar cells after subsequent steps

4.2.2.1 Implementation of an Anti-Reflective Coating (ARC)

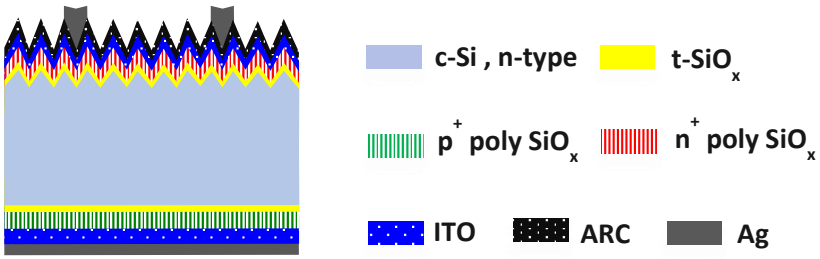


Figure 32: Schematic of solar cell structure for FBC solar cell with ARC

Front light reflection and parasitic absorption in the component layers of the solar cells are the main causes for the loss J_{sc} [85]. However, the implementation of a chemically textured surface on the front side of the solar cell effectively suppresses reflection losses. Further enhancement in light trapping can be achieved by the usage of an anti-reflective coating (ARC). For the implementation of the ARC, a solar cell was fabricated following the procedures in section 4.1.Figure 32 is a schematic structure of the FBC solar cell with an ARC. The implied V_{oc} obtained after subsequent steps starting from high temperature annealing upto thermal annealing post ITO deposition can be observed in Figure 31. From figure 31 it is evident that the drop in passivation post ITO deposition is slightly higher for this particular cell in comparison to the cell that has been discussed in section 4.2.1 which has a double ITO layer but is devoid of an ARC. Once again the difference in passivation that is observed could be a consequence of non-homogeneous layer sputtering. However, with thermal annealing the recovery in passivation is similar for the two cases regardless of the difference in passivation drop. Following this, the solar cell was screen printed and exposed to a round of hot plate annealing at 350˚C for 10 minutes. This was followed by the deposition of a single layer MgF_2 (ARC) of thickness 110nm on the front side of the solar cell by thermal evaporation. The thickness of the ARC that has been employed here has been based on previous optimisations within the PVMD group which gave beneficial results. It is to be noted that the metal contacts were isolated during the MgF_2 deposition to ensure that the ARC coating was only deposited on the active area.

Table 8 comprises of the solar cell parameters obtained before and after the implementation of the ARC. The utilization of an ARC resulted in a 1.45 mA/cm^2 increase in J_{sc} but at the cost of a drop in FF and V_{oc}. An absolute 0.34% drop in FF can be seen in combination with a 4mV drop in V_{oc}. As a result, despite the improvement in J_{sc} an overall drop in efficiency was observed. A final efficiency of 20.85% was recorded with the use of an ARC. The drop in these parameters could be an effect of the thickness of the MgF_2 layer that has been deposited. With further optimisation of the ARC thickness, there is still scope for this particular method to improve the overall performance of the solar cells.

Table 8: Solar cell parameters before and after the implementation of ARC

Parameters	V_{oc} [mV]	$J_{sc\ (EQE)}$ [mA/cm2]	FF [%]	η [%]
Before ARC	693	36.68	79.70	20.25
After ARC	689	38.13	79.36	20.85

4.2.2.2 Alternate TCO schemes

As mentioned in section 3.8 in Chapter 3 ,the highly conductive and transparent ITO layer is responsible for passivation degradation due to sputtering damages. In addition to this, these layers also account for optical losses brought on by parasitic absorption [86]. Taking these factors into consideration, tests were implemented by altering the TCO structures used on the solar cells as mentioned below. The passivation obtained after processing steps for the cells on which the TCO schemes have been implemented can be observed in Figure 31.

Removal of ITO layer from the rear side

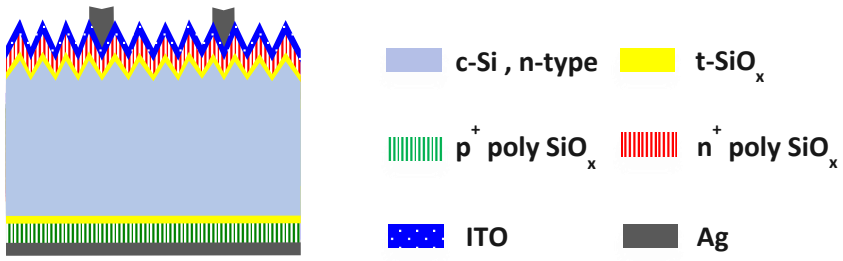


Figure 33: Schematic structure of FBC solar cell with no rear ITO

For this particular test, the front layer of the solar cell was sputtered with a 75nm ITO layer whereas no ITO layer was used at the rear side as shown in Figure 33. Post ITO deposition, the cell was subjected to thermal annealing at 400 °C for 1 hour in H_2 followed by screen printing. Figure 31 shows that the drop in passivation post ITO is reduced for this structure as the ITO layer is sputtered on only one side which in turn reduces the damage caused by the process. As the rear side of the solar cell was devoid of an ITO layer, a full area metal contact mask was used during screen printing. However, the alignment of such a mask was quite difficult and this resulted in some of the Ag paste used at the rear side smudging onto the front side. The low FF of 23.72% shown in Table 9, is an indication of high parasitic resistances which arise from the error in the metallisation process. The lack of a TCO layer at the rear side enables the Ag to inject through the poly-SiO_x layer during thermal curing which in turn increases the contact resistivity, a primary component of the series resistance in solar cells [87].

Table 9: Solar cell parameters with no ITO layer at rear side

Parameters	V_{oc} [mV]	J_{sc} [mA/cm^2]	FF [%]	η [%]
Post screen printing	541	34.19	23.72	4.38

Replacement of ITO layer with IWO layer at the front side

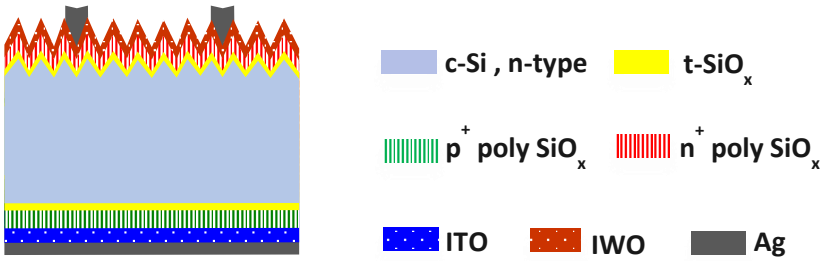


Figure 34: Schematic of solar cell structure for FBC solar cell with IWO layer as front TCO

As shown in Figure 34, for this particular experiment the front ITO layer was replaced by a 75nm thick IWO layer due to the lower parasitic absorption in the short wavelength region and the higher carrier mobility exhibited by IWO films in comparison to ITO films [88][89]. Once again ITO deposition was followed by a round of thermal annealing at 400 °C for 1 hour. Figure 31 shows the passivation quality obtained at consecutive steps. The replacement of the ITO layer by IWO did not show an additional improvement or decrease in passivation post sputtering. Rather it remained identical to cases that used a front and rear ITO. The final step of screen printing was performed along with the post metallisation annealing at 350 °C 10 minutes. The solar cell parameters obtained post metallisation annealing can be seen in Table 10.

Table 10: Solar cell parameters for IWO/ITO combination

Parameters	V_{oc} [mV]	$J_{sc\ (EQE)}$ [mA/cm^2]	FF [%]	(η) [%]
Post metallisation annealing	690	37.37	77.62	20.01

In comparison to the solar cell which made use of ITO layers at the front and back (Table 6), the FF was lower when using an IWO-ITO combination. This could be due to the higher resistivity values of the IWO layer [89]. In addition to this, comparable J_{sc} values were obtained when the ITO layer was replaced by an IWO layer. The lack of improvement in J_{sc} upon using this combination could be due to the fact that ITO layer used at the rear side absorbs a portion of the long wavelength light due to the lower transparency exhibited in this wavelength range [89].

Figure 35 depicts the EQE responses for the various solar cell structures fabricated in section 4.2.1 and 4.2.2. In the short wavelength region from 400nm to 600nm, the solar cell that makes use of a double ARC which is a combination of ITO and MgF_2 outperforms the other samples. This attributes to the reduction in reflectance enabled by the ARC coating which ultimately corresponds to a higher Jsc [90]. The solar cell that consists of ITO layers alone at the front and rear sides, are not too far behind with respect to their performance in this wavelength range. Although IWO layers were expected to behave better in the short wavelength region due to the lower absorption properties, the results obtained are however

contradictory [91]. The deterioration in EQE response could be a result of non-uniform layer deposition on textured surfaces.

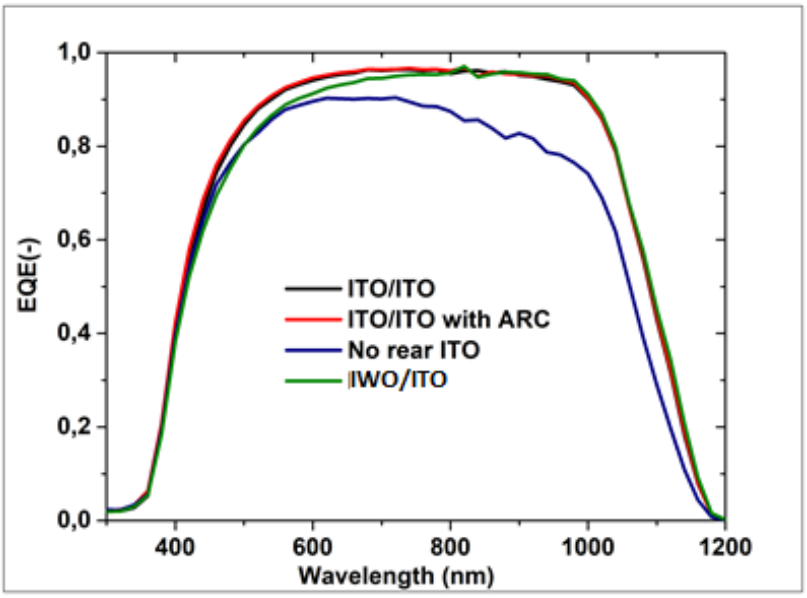


Figure 35: EQE response of fabricated solar cells

For the wavelength region between 600nm to 1000nm, the EQE is maximum for all the structures which implies efficient light trapping enabled by the textured surfaces. However, a crucial drop in response can be observed for the solar cell that does not use an ITO layer at the rear side. This is because a thick and transparent rear ITO is necessary to facilitate reflection at the rear side of the solar cell. This reflective property exhibited by rear TCOs reduces the parasitical absorption in the silver layer and thus providing better EQEs and higher current [92]. In addition to the low internal reflection, carrier collection ability is also limited by the direct contact between the metal and poly-SiO_x layer occurring from the flaw in metallisation in section 4.2.2.2. Wavelength regions beyond 1000nm demonstrate identical behaviour by all the solar cells that include an ITO layer at the rear side. Once again, the cell devoid of an ITO layer severely underperforms in this range.

4.3 Fabrication process of single side textured FBC solar cell with NAOS

The sequential steps involved in the fabrication of single side textured solar cells using NAOS is identical to the processes followed when fabricating the same solar cell using thermal oxidation discussed in section 4.1. The major change is in the tunnel oxide growth process in which the wafers are immersed in a 69.5% HNO3 solution for 60 minutes in order to grow the tunnel oxide layer with a thickness of around 1.4nm [50]. The growth of the intrinsic a-Si:H layer and doped a-SiO_x:H layers are same as before. The next major change is with regards to the annealing time and temperature. NAOS in general has a lower thermal budget in comparison to thermally grown oxide and thus 850 °C 45 minutes has been utilized as the annealing condition [58]. This particular thermal budget has been adopted from previous

works within the PVMD group. Further ahead all the processes are identical to the previously fabricated solar cells that made use of a thermal oxide layer. Figure 36 is a schematic representation of the fabrication process of FBC solar cells that used a NAOS grown tunnel oxide layer.

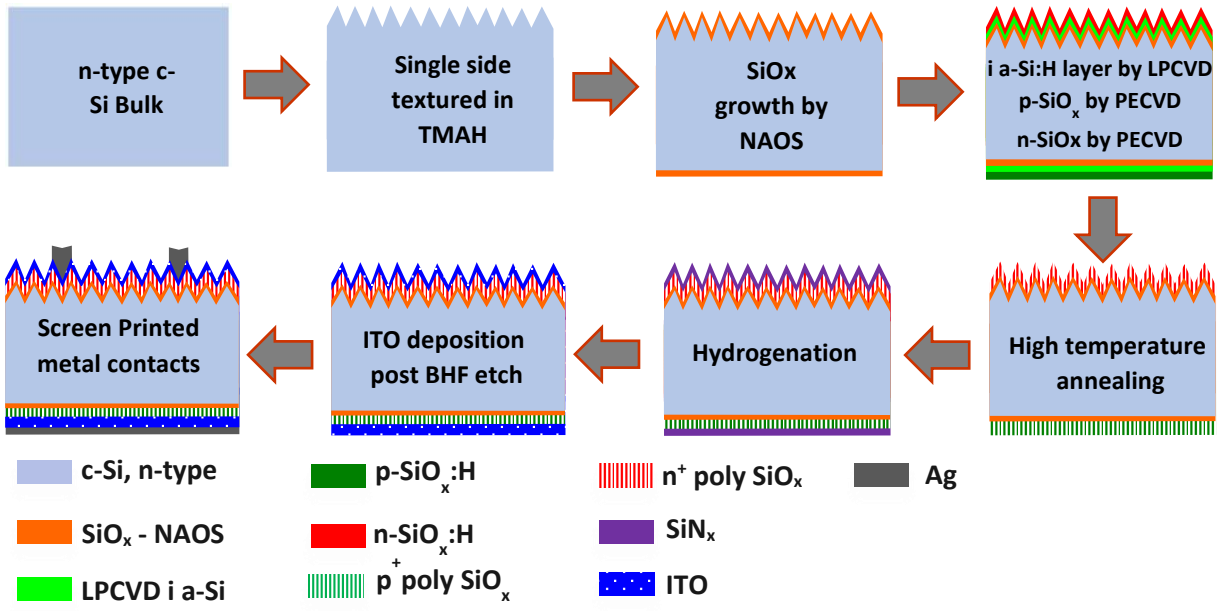


Figure 36: Schematic representation of the fabrication of single side textured solar cell with NAOS grown tunnel oxide layer

4.4 Solar cell results

Figure 37 illustrates the change in passivation obtained after subsequent processing steps. High temperature annealing at 850 °C 45 minutes resulted in an iVoc of 683mV followed by a 27mV increase in iV_{oc} post hydrogenation using SiN_x/FGA. It is worth mentioning that the drop in passivation obtained upon sputtering a 75nm thick layer ITO layer at the front side and 150nm thick ITO layer at the rear much was minimal in comparison to the solar cell that used a thermal oxide layer in section 4.2.1. Having observed only a 10mV drop post ITO deposition , no further thermal annealing or curing was performed on the sample.

Upon ITO deposition, the solar cell was screen printed and annealed on a hot plate at 350 °C for 10 minutes. Table 11 comprises of the solar cell parameters obtained post screen printing and after metallisation annealing. An absolute increase of 0.87% in FF followed by an increase of 1.67 mA/cm2 in J_{sc} could be observed upon annealing at 350 °C 10 minutes. However, a drop of 1mV was observed in the case of V_{oc} measured post hot plate annealing. A final efficiency of 20.37% was recorded for the FBC solar cell. Table 12 indicates the parameters obtained from the SunsV_{oc} measurement. The disparity in FF and PFF values constitutes to a high series resistance present in the solar cell as the SunsV_{oc} measurement does not take into account the effect of series resistance.

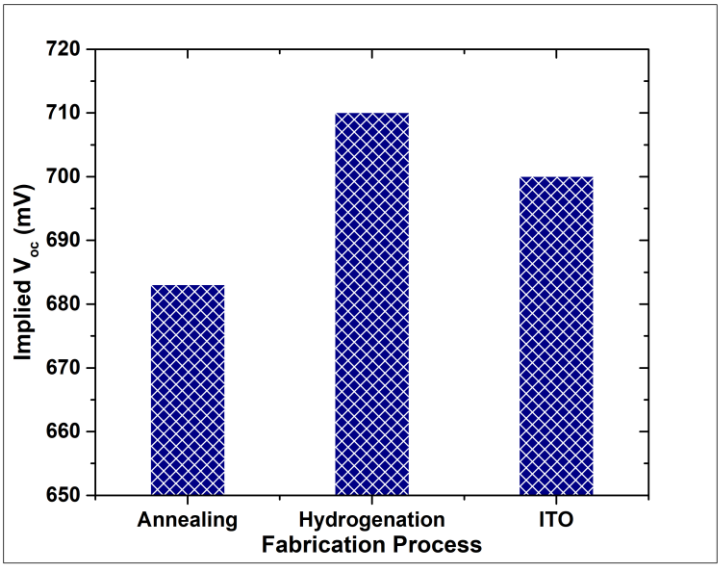


Figure 37: Change in passivation of NAOS – FBC solar cell

Table 11: Solar cell parameters from JV measurement

Parameters	V_{oc} [mV]	$J_{sc\ (EQE)}$ (mA/cm^2)	FF [%]	[η] [%]
Post Screen Printing	688	36.09	77.65	19.28
Post metallisation annealing	687	37.76	78.52	20.37

Table 12: Solar cell parameters from SunsV_{oc} measurement

Parameters	SunsV_{oc} [mV]	PFF [%]	Pη[%]
Post metallisation annealing	708	82.5	22.3

4.5 Comparison of Thermal Oxidation and NAOS

This section focuses on a comparative study performed on the best performing FBC solar cell with a thermally grown tunnel oxide layer from section 4.2.1 and the FBC solar cell that uses a NAOS grown tunnel oxide layer from section 4.4. Table 13 contains the final solar cell parameters obtained after post metallisation annealing for both the cells under inspection. To begin with, the high V_{oc} of 694mV and 687mV exhibited by both the thermal oxide and NAOS cell respectively is an indication of good chemical and field effect passivation. The high thermal stability shown by thermally grown oxides in comparison to those grown by NAOS especially for textured surfaces, could be a contributing factor towards the better passivation exhibited by the thermal oxide incorporated solar cell.

Table 13: Solar cell parameters of NAOS and Thermal Oxide solar cells

Parameters	V_{oc}[mV]	$J_{sc(EQE)}$ [mA/cm^2]	FF[%]	η [%]	PFF[%]	SunsV_{oc}[mV]
Thermal Oxide	694	37.91	79.6	20.942	84.5	713
NAOS	687	37.76	78.52	20.368	82.5	708

Yuheng et al. [93] demonstrated the impact of doping concentration and tunnel oxide thickness on the FF. For a particular value of doping concentration, an increase in tunnel oxide layer by 0.2nm resulted in an absolute drop of 49% in FF [93]. In the case of both the cell structures under inspection, besides the tunnel oxide growth method all the other supporting layers have been processed identically. Having said this, the lower FF exhibited by the NOAS implemented device is an indication that the tunnel oxide grown by NAOS is relatively thicker than that grown by thermal oxidation. As a result, the carriers have a difficult time tunnelling through the NAOS grown tunnel oxide layer which in turn lowers the FF. Although exact measurements of tunnel oxide thickness have not been performed here, in general wet chemically grown oxide layers are thicker than thermally grown mainly because thermal oxidation provides better control and flexibility in terms of layer thickness [94].

Once again taking into account the similarity in supporting layers for both the solar cell structures, it is safe to assume that both the solar cells would have identical series resistances. However, the higher V_{oc} and PFF shown by the solar cell that uses a thermally grown oxide layer is an outcome of tunnel oxide induced difference in junction formation. Efficient carrier collection and carrier selectivity is enabled by the junction that is formed which ultimately results in better passivation.

Figure 38 shows the EQE responses of the FBC solar cells that use tunnel oxide layers grown by NAOS and thermal oxidation. A higher response shown by the thermal oxide induced solar cell in the wavelength range of 400nm to 600nm, constitutes to effective carrier collection enabled by the thermally grown tunnel oxide layer. However, the longer wavelength region beyond 1000nm exhibits a better performance by the NAOS solar cell. This shift in performance in the long wavelength region could be from higher free carrier absorption within the ITO layer used on the thermal oxide solar cell. Although we assume that identical ITO layer thicknesses have been sputtered on the cells, fluctuations during processing can indeed lead to slight variations in thickness.

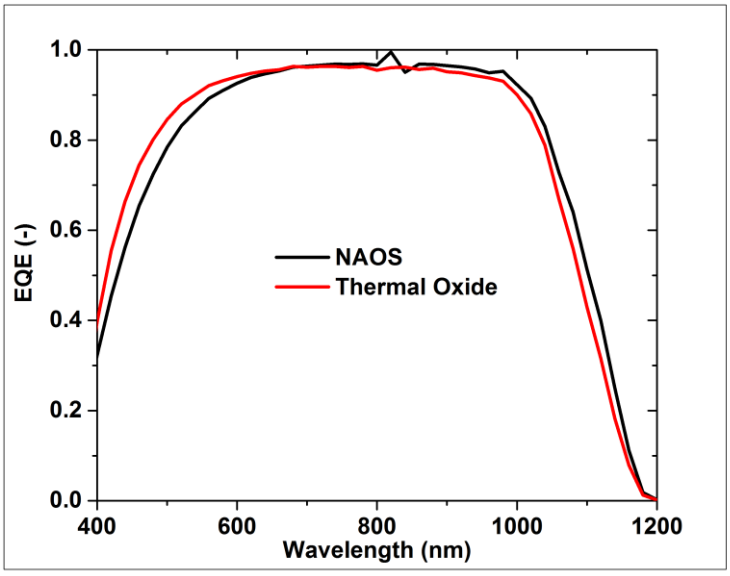


Figure 38: EQE response of NAOS and thermal oxide solar cells

4.6 Overview

This chapter focused on the fabrication of single side textured FBC solar cells using the optimised poly-SiO_x passivating contacts. The poly-SiO_x passivated FBC solar cell fabricated with a thermally grown tunnel oxide layer resulted in an efficiency of 20.94% with a maximum V_{oc} and FF of 694mV and 79.6% respectively. Additional tests performed with regards to the ARC and TCO layers on reference cells did not yield beneficial results. The usage of a NOAS grown tunnel oxide layer resulted in a a poly-SiO_x passivated FBC solar cell with an efficiency of 20.37%. The highest V_{oc} and FF obtained were 687mV and 78.52% respectively. In addition to this a comparison of the two tunnel oxide layers showed that a poly-SiO_x passivated FBC cell fabricated using a thermally grown tunnel oxide layer outperformed the one that made use of a tunnel oxide layer grown by NAOS.

5

Double side textured FBC solar cells

This chapter looks into the fabrication of double side textured FBC solar cells using the optimised poly-SiO_x passivating contacts. Section 5.1 discusses the re-optimisation of n-type textured and p-type textured poly-SiO_x passivating contacts. Section 5.2 describes the fabrication process of the double side textured FBC solar cells. This is followed by Section 5.3 which discusses the solar cell results and additional process schemes implemented with regards to TCO layers. Section 5.4 is an overview of this chapter summarising major findings and conclusions.

5.1 Re-optimisation of poly-SiO_x passivating contacts

5.1.1 Shift in optimum annealing condition

Chapter 3 looked into the optimisation of poly-SiO_x CSPCs symmetric contacts to be deployed in FBC solar cells. With regards to the n-type textured and p-type textured poly-SiO_x passivating contacts, which would serve as the front and rear contacts of double side textured FBC solar cells respectively, the thermal budget of 675 °C 3 minutes for tunnel oxide growth in combination with the two-step annealing scheme gave beneficial results. The two step annealing scheme consisted of a first round of annealing performed at 950˚C 1 minute post the intrinsic a-Si:H layer deposition followed by the second round of annealing performed at 950˚C 10 minutes after the doped a-SiO_x:H layer deposition. iV_{oc} of 687mV and 691mV was obtained for the p-type textured and n-type textured CSPCs respectively post hydrogenation.

However, owing to the time gap between the optimisation of symmetric samples and the final implementation of these contacts within the solar cell, a shift in operating conditions was observed with respect to the furnace utilised for the final (second round) annealing step. Repeated tests showed that the optimum annealing condition had shifted to 950 ˚C 15 minutes from the previous condition of 950 °C 10 minutes.

Figure 39 shows the passivation obtained for n-type textured and p-type textured contacts post the shift in optimum annealing condition. It should be noted that the shift has occurred only for the second round of annealing. The first round of annealing remains intact at 950˚C 1 minute. Test 1 corresponds to the passivation attained for the initially optimised annealing condition of 950˚C 10 minutes . Test 2 accounts for the recent annealing tests performed at 950˚C 10 minutes that indicates a drop of 20mV for the p-type textured contact and 50 mV for the n-type textured. Finally Test 3 is the re-optimised annealing condition of 950˚C 15 minutes that resulted in an iV_{oc} of 687 mV for the p-type textured contact and 691 mV for the n-type textured contact post hydrogenation (SiN_x/FGA).

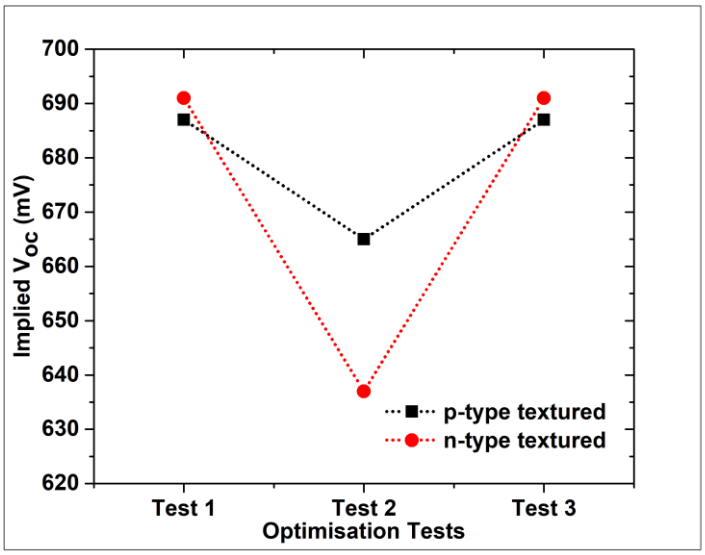


Figure 39: Shift in optimum annealing condition of symmetric contacts

5.1.2 Passivation tests for TCO deposition

Section 3.8 of Chapter 3 discusses the passivation tests conducted on poly-SiO_x passivating contacts to estimate the loss in passivation post TCO deposition. Similar tests were conducted on the re-optimised n-type textured and p-type textured poly-SiO_x passivating contacts developed using tunnel oxide layers grown at 675˚C 3 minutes in combination with the two-step annealing scheme. ITO layers which is the choice of TCO were deposited on the contacts post hydrogenation. It should be noted that the samples were introduced to a round of BHF etch prior to ITO deposition in order to remove the SiN_x layer deposited during hydrogenation. Post ITO deposition, the samples were exposed to thermal annealing in H_2 at 400˚C for 1 hour to help recover the loss in passivation brought on by sputtering damages.

Figure 40 shows the change in passivation indicated by the iV_{oc} obtained after subsequent steps for the p-type textured and n-type textured poly-SiO_x passivating contacts starting from high temperature annealing upto thermal annealing in H_2 performed post ITO deposition. The results obtained post ITO deposition showed a drop of approximately 20mV for both the n-type textured and p-type textured contacts. From this we can estimate a net drop of 40mV for the double sided textured FBC solar cells that would incorporate both the poly-SiO_x passivating contacts. Thermal annealing in H_2 performed on the samples helped in an almost complete recovery of passivation with regards to n-type textured contact whereas in the case of p-type textured contact, only a 1mV increase in passivation was observed. This limited recovery in passivation can indeed prove detrimental to the passivation quality of the solar cell that would be fabricated.

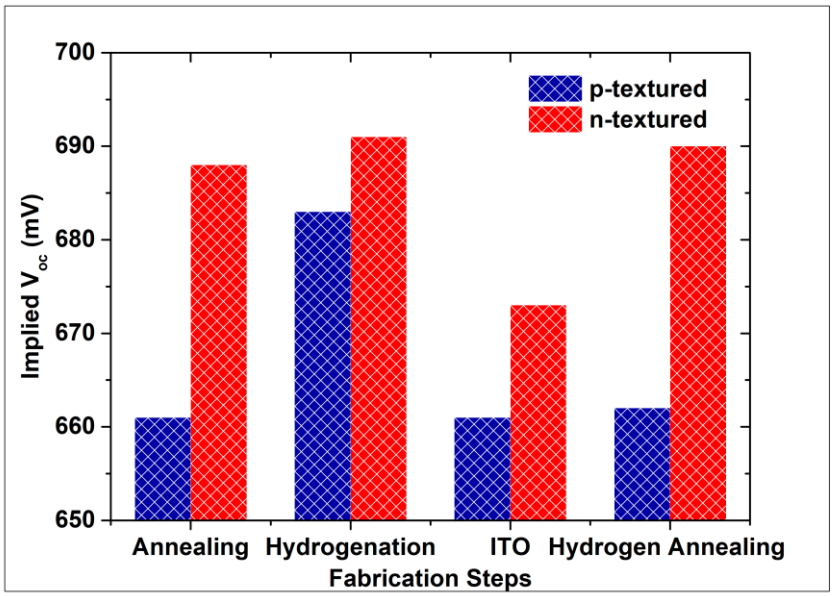


Figure 40: Change in passivation quality of symmetric contacts (for p-type textured and n-type textured)

5.2 Fabrication process

The sequential steps involved in the preparation of the double side textured FBC solar cells using the optimised poly-SiO_x passivating contacts is as follows :

- Double side polished n-type FZ wafers with <100 orientation> and a thickness of 280µm have been used as the c-Si bulk.
- The wafers are then made to undergo texturing on both the sides by immersing it in an aqueous solution composed of TMAH and ALKA-TEX at a temperature of 80 °C for 15 minutes.
- Post texturing the wafers are cleaned using DI water and dried in a spin dryer to remove water particles on the surface.
- A poly-Si etch is performed on the wafers for 2 minutes in order to round the edges of the pyramids formed during texturing. Post etching, the wafers undergo a full round of standard cleaning and drying followed by the Marangoni drying to remove the native oxide layer formed on the surface of the wafer.
- The wafers are then exposed to thermal oxidation at 675 °C 3 minutes to facilitate the growth of the tunnel oxide layer. As mentioned in Chapter 3, temperature plays a critical role in the growth of the oxide layer and thus a stabilisation time of 5 minutes has been incorporated in the oxidation recipe to ensure that the oxidation takes place at the right temperature.
- Intrinsic a-Si:H layer is grown on the wafer surface in an LPCVD furnace. A deposition rate of 2nm/min results in the formation of a 10nm thick layer on the polished side wafers. The thickness is reduced by a factor of 1.7 on the textured side.

- In accordance with the two-step annealing step which gave beneficial results for the optimisation of textured symmetric contacts in Chapter 3, the first round of annealing is performed at 950 °C for 1 minute post the intrinsic layer deposition.
- The wafers are then processed inside an RF-PECVD chamber for the deposition of the doped a-SiO_x:H layers. The texture front side is deposited with Phosphorous doped a-SiO_x:H and the textured rear side is deposited with Boron doped a-SiO_x:H layers. The deposition time and gas flows of respective gases can be seen in Table 14.
- Post the PECVD process, high temperature annealing at 950 °C 15 minutes is implemented on the wafers in accordance with re-optimisation performed in section 5.1 to facilitate dopant diffusion and crystallization of doped a-SiO_x layer to doped poly-SiO_x layers.
- The primary hydrogenation technique implemented is SiN_x/FGA. A deposition time of 13min 36 seconds have been used to deposit the SiN_x layer on both sides of the wafer at 400˚C. The wafers are then subjected to Forming Gas Annealing (FGA) for 30 minutes at 400 ˚C.
- Post hydrogenation, the SiN_x layer is removed by a BHF dip prior to the ITO layer deposition. An ITO layer of 75nm is sputtered on the textured front side (n^+poly-SiO_x) followed by 75nm on the rear side (p^+poly-SiO_x).
- Thermal annealing at 400 °C for 1 hour in H_2 atmosphere is implemented on the wafers to recover the loss in passivation caused by ITO deposition.
- The front and rear metal contacts are enabled on the wafer by Screen Printing of Silver (Ag). The wafers are then annealed in an oven for 30 minutes at 170 °C. This is followed by post metallization annealing step at 350 °C for 10minutes.
- The final parameters of the fabricated solar cells are measured using the illuminated JV measurement and EQE setup. Figure 41 is schematic representation of the fabrication process. Figure 42 is an image of the front and rear side of the fabricated double side textured FBC solar cell.

Table 15: Deposition parameters for the optimised poly-SiO_x contacts

Contact Type	**Thickness**	**Gas Flows**			
		SiH_4(sccm)	**CO_2(sccm)**	**B_2H_6/PH_3(sccm)**	**H_2(sccm)**
p-type textured	20nm	8	2	B_2H_6 = 5	100
n-type textured	20nm	4	6.4	PH_3 = 4.8	35

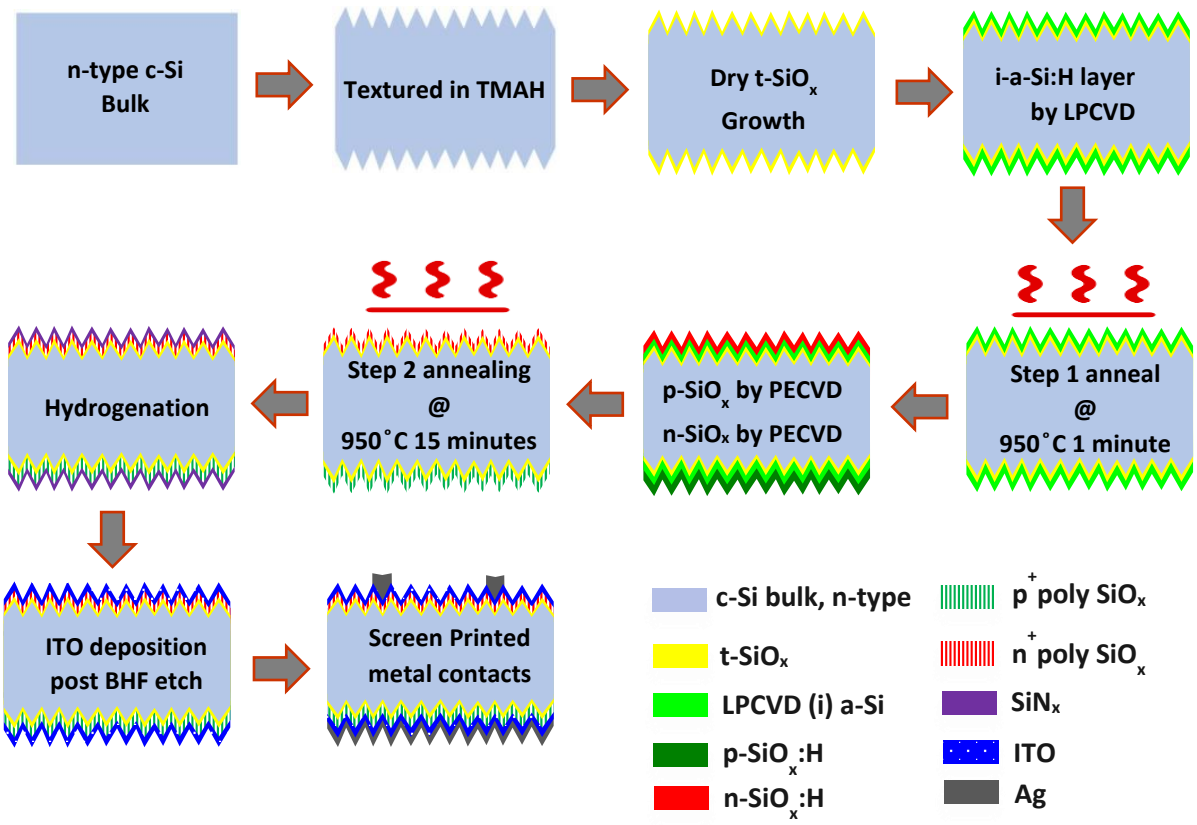


Figure 41: Schematic representation of the fabrication of double side textured FBC solar cell with thermally grown tunnel oxide layer

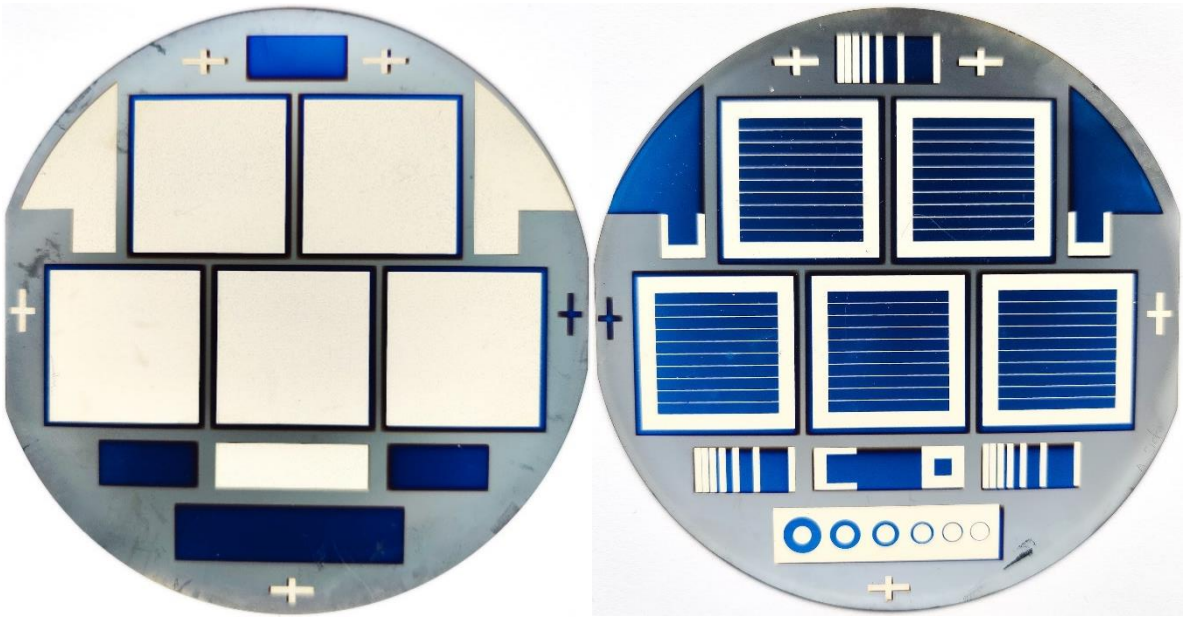


Figure 42: Fabricated double side textured FBC solar cell. (Left: Screen printed rear side, Right: Screen printed front side

5.3 Solar cell results

5.3.1 Double side textured FBC solar cell with double ITO layer

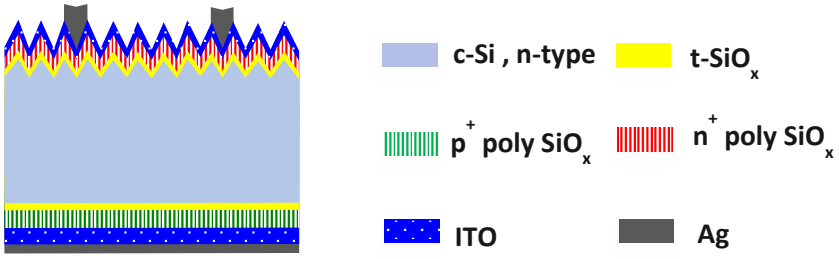


Figure 43 : Schematic structure of FBC solar cell with double ITO layer

Presented below are the results obtained for the double side textured FBC solar cell that makes use of a thermally grown tunnel oxide layer and a double ITO layer as mentioned in the fabrication process in section 5.2. Figure 44 is a depiction of the change in passivation of the solar cell after subsequent processing steps measured using the Sinton lifetime measurement setup. The iV_{oc} of 671mV which is a value within the range of passivation of individual symmetric contacts was obtained upon the implementation of the two-step annealing scheme with the final round of annealing taking place at 950 °C 15 minutes. An increase of 27mV is obtained post hydrogenation using SiN_x/FGA which results in an iV_{oc} of 698 mV which is a good starting point for further processing. The ITO depositions on both sides of the solar cells results in a net drop of 39 mV as expected from ITO tests performed on the n-type textured and p-type textured poly-SiO_x passivating contacts in section 5.1. However, the recovery in passivation upon thermal annealing in H_2 was not to the full extent as was observed in the case of single side textured FBC solar cells fabricated in section 4.2 of Chapter 4. An iV_{oc} of 685 mV was obtained upon annealing in H_2 at 400 °C for 1 hour. The restricted improvement in passivation could be a consequence of the lack of improvement from annealing for the p-type textured contacts as mentioned in Section 5.1.2

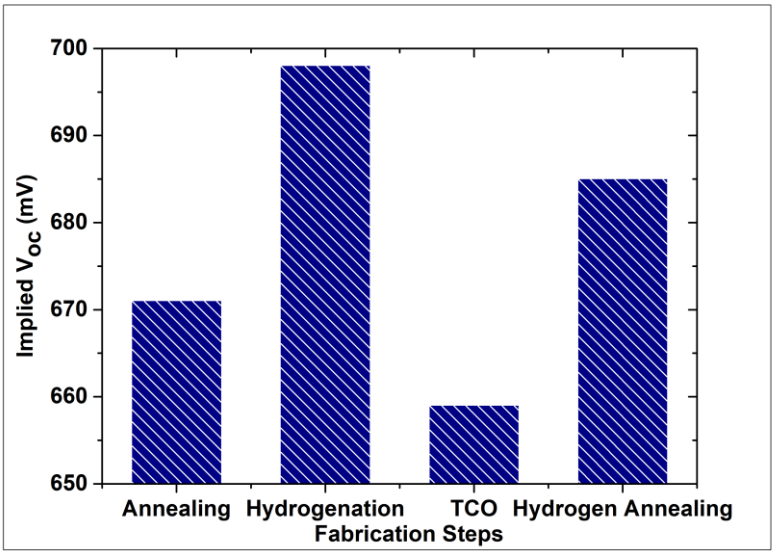


Figure 44: Change in passivation after subsequent steps for double ITO solar cell

Table 16 consists of the measured solar cell parameters. Screen printing results in a drop of approximately 30 mV with regards to the V_{oc}. A 3mV increase in V_{oc} is obtained upon hot plate annealing performed after metallisation. In addition to this an absolute increase 1.89% could be seen in the FF which is brought on by the reduction in contact resistivity. A 3.56mA/cm^2 gain in J_{sc} can also observed post hot plate annealing in. Lastly the fabricated FBC solar cell reported a final efficiency of 19.38%.

Table 16: Solar cell parameters from JV measurement

Parameters	V_{oc} [mV]	$J_{sc(EQE)}$ [mA/cm2]	FF [%]	η[%]
Post screen printing	658	34.09	76	17.047
Post metallisation annealing	661	37.65	77.89	19.38

Table 17 illustrates solar cell obtained from the SunsV_{oc} measurement post hot plate annealing resulted. An absolute difference of 3.84% observed in the case of FF and pseudo fill factor (PFF) is an indication of high series resistance. In addition to this the difference in Ag layer thickness arising from the uneven textured surface can also be a contributing factor to the loss in FF. The drop in V_{oc} associates to the metallisation step which can be rectified by further optimisation of the screen-printing setup.

Table 17: Solar cell parameters from SunsV_{oc} measurement

Parameters	SunsV_{oc} [mV]	PFF [%]	Pη [%]
Post metallisation annealing	682	81.7	20.7

5.3.2 Additional process schemes

One of the major issues that could be identified from the obtained parameters is the relatively low V_{oc} values of the solar cells. The low starting point of V_{oc} before metallisation serves as a hindrance owing to the resistance in recovery during thermal annealing. One approach towards limiting the overall loss in passivation prior to metallisation is to modify the TCO layers that are implemented.

In accordance with this, three additional experiments were performed with regards to the TCO layers. The use of a thinner ITO layer at the rear side of the solar cell, the removal of the ITO layer from the rear side and the replacement of ITO layers by the IWO layers were the tests conducted. It should be noted that all the experiments were conducted on reference solar cells fabricated using identical processes as the solar cell analysed in section 5.3.1. Figure 45 depicts the change in passivation observed after subsequent processing steps starting from high temperature annealing upto annealing in H_2 post TCO deposition.

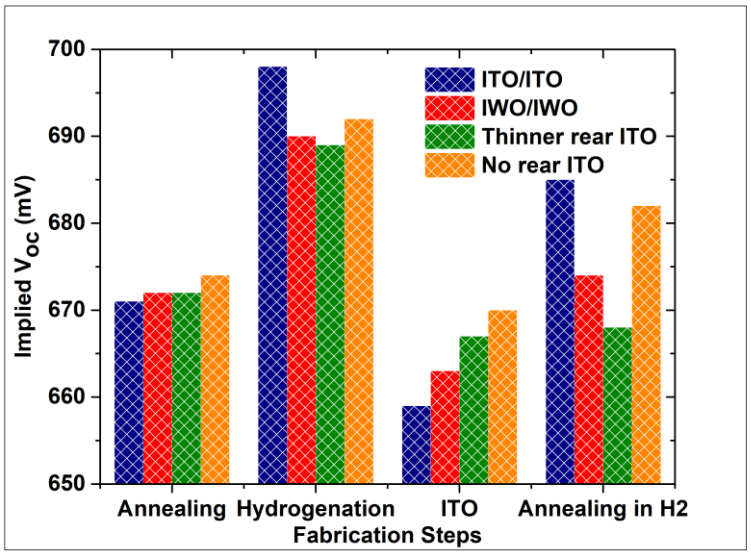


Figure 45: Variation in passivation quality of fabricated solar cells

Thinner ITO at rear side

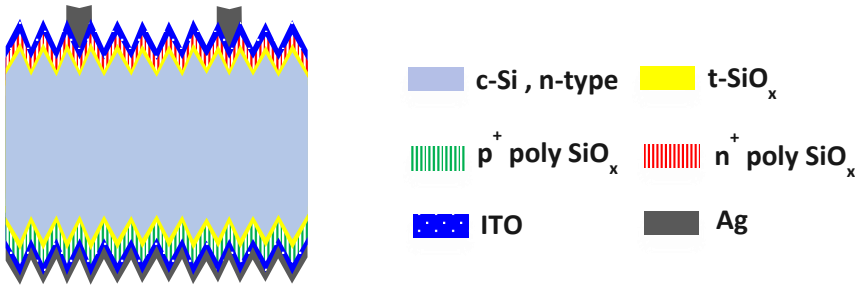


Figure 46: Schematic structure of FBC solar cell with thinner rear ITO layer

Figure 46 shows the FBC solar cell that has been fabricated for this process scheme. In this experiment ,the thickness of the rear side ITO layer was reduced by half which implied a thickness of 37nm whereas the front ITO layer was maintained at a thickness of 75nm. This particular change in thickness was implemented with the hope of seeing a lower reduction in passivation post ITO deposition as the sputtering damages induced at the rear side would be limited. As expected, the overall loss in passivation was 22 mV lower than what was seen in the case of using ITO layers of 75nm at the front and rear sides. However, no improvement in iV_{oc} was obtained during thermal annealing which resulted in an iV_{oc} of 668 mV before screen printing.

Table 18 shows the solar cell parameters obtained post metallisation annealing at 350 °C 10 minutes on a hot plate. The metallisation induced drop results in a final V_{oc} of 647 mV which is significantly lower than what was observed when using a thicker ITO layer at the rear side as seen in Table 16. Additionally, a lower FF and J_{sc} were also obtained for this specific experiment. Owing to the lack of improvement from thermal curing post ITO deposition combined with the effects of screen printing the solar cell parameters showed no improvements.

Table 18: Solar cell parameters from JV measurement

Parameters	Voc [mV]	$J_{sc(EQE)}$ [mA/cm2]	FF [%]	η[%]
Post metallisation annealing	647	36.87	76.06	18.144

Removal of ITO from rear side

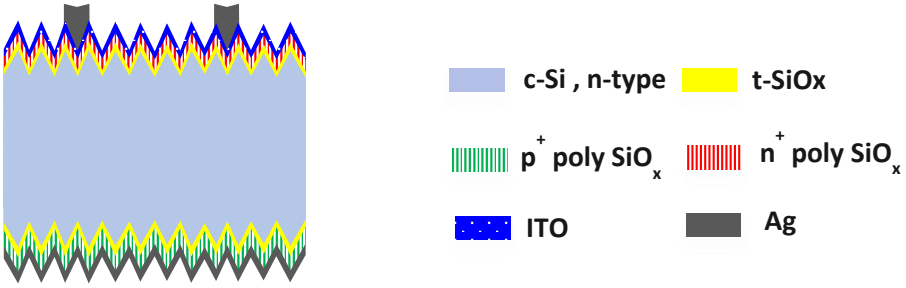


Figure 47: Schematic structure of FBC solar cell with no rear ITO layer

For this particular test, the FBC solar cell was fabricated devoid of an ITO layer at the rear side as can be seen in Figure 47. The removal of ITO layer from the rear side resulted in a 22mV drop in iV_{oc} post ITO deposition as can be seen in Figure 45. The limited drop in passivation upon ITO deposition corresponds to the reduced sputtering damages arising from the lack of an ITO layer at the rear side of the solar cell. Thermal annealing in H_2 resulted in an iV_{oc} of 682 mV. As the solar cell was devoid of an ITO layer at the rear side, screen printing was enabled using a full area metal contact mask. The difficulty in alignment during this process resulted in some silver paste smudging onto the front side of the solar cell. The low FF of 17.82% as shown in Table 19, is brought on by high parasitic resistances due to an increase in contact resistivity from the direct contact metal and p^+poly-SiO_x layers deposited at the back side.

Table 19: Solar cell parameters from JV measurement

Parameters	Voc [mV]	$J_{sc(EQE)}$ [mA/cm2]	FF [%]	η[%]
Post screen printing	485	34.69	17.82	2.99

IWO layer at the front and rear side

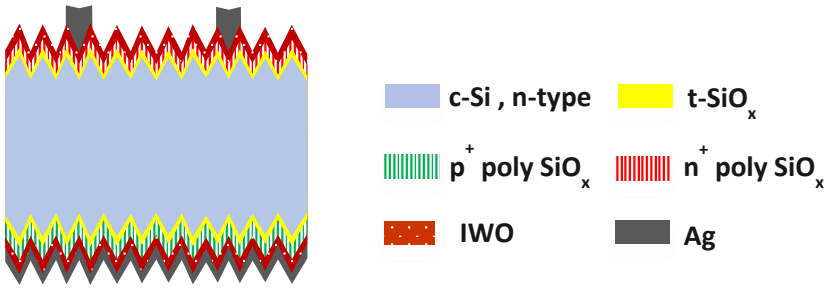


Figure 48: Schematic structure of FBC solar cell with IWO layers at the front and rear side

On account of the high mobility, better stability at high temperatures and lower absorption in the short wavelength region, 75nm thick IWO layers were utilised on the front and rear sides as shown in Figure 48 [91]. A 27mV drop in passivation was obtained post IWO deposition which is similar to what was observed in the case of ITO layers observed in Figure 45. Thermal annealing in H_2 resulted in an iV_{oc} of 674 mV. In comparison to the solar cell in section 5.3.1 that made use of ITO layers, the recovery in passivation is limited. This however could be from the difference in textured wafers used for processing or small fluctuations within the annealing chamber.

Table 20 shows the final solar cell parameters obtained post metallisation and hot plate annealing. The restricted recovery in passivation combined with metallisation leads to a final V_{oc} of 649 mv. In comparison to the solar cell that made use of ITO layers (Table 16) the lower FF of 74.6% obtained when using IWO could be due to the high resistivity demonstrated by IWO layers [89]. Additionally, no improvements in J_{sc} was obtained upon replacing the ITO layers by IWO layers.

Table 20: Solar cell parameters from JV measurement

Parameter	Voc [mV]	$J_{sc(EQE)}$ [mA/cm2]	FF [%]	η[%]
Post metallisation annealing	649	37.28	74.6	18.05

Figure 49 depicts the EQE responses for the various solar cell structures fabricated. In the short wavelength region from 400nm to 600nm, solar cells that make use of 75nm thick ITO layer at the front side perform better than the one which uses an IWO layer. Although the IWO layers were expected to behave better in the short wavelength region due to the lower absorption properties, the results obtained are however contradictory [91]. This change in expected performance could due to variations in IWO layers sputtered on the textured surface or because the thickness of IWO layers needs further optimisation. In addition to this, slight variation seen in the response of cells that use identically thick ITO layers at the front side could once again be from thickness non-uniformities during sputtering.

For the wavelength region between 700nm to 1000nm, the EQE is maximum for the solar cells which implies efficient light trapping enabled by the textured surfaces. However, the device that is devoid of a rear ITO layer shows a drop in response beyond 700nm. This arises from the low internal reflection from the lack of a TCO layer and ineffective carrier collection due to the direct contact between the metal and poly-SiO_x layer. For the wavelengths beyond 1000nm, the solar cell that uses an IWO layer performs better than the others. This can be explained by the better transparency and higher transmittance of the IWO layers, which results in lower free carrier absorption in this wavelength range [89]. It can also be seen that the using a thinner ITO layer at the rear side did not enhance or decline the EQE response in long wavelength region. This could be because the lower internal reflection exhibited by the ITO layer is counterbalanced by the low free carrier absorption.

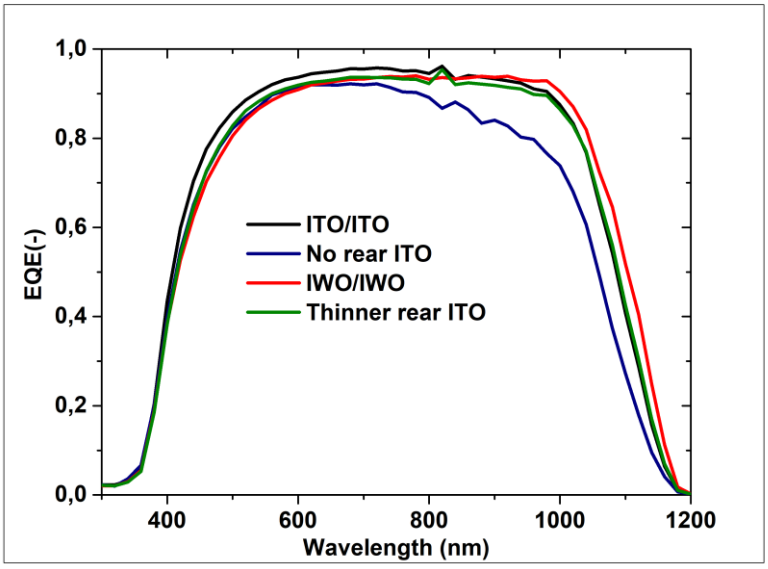


Figure 49: EQE response of fabricated solar cells

5.4 Overview

Chapter 5 looked into the re-optimisation of n-type textured and p-type textured poly-SiO_x passivating contacts. Following this double side textured FBC solar cells were fabricated using the optimised poly-SiO_x CSPCs. The FBC solar cell that consisted of double ITO layers demonstrated an efficiency of 19.38% along with a V_{oc} and FF of 661mV and 77.89%. Additional process schemes implemented to further enhance the passivation did not yield beneficial results. Loss in passivation upon TCO depositions and improper metallisation techniques were identified as the reasons for the restricted V_{oc} values recorded in all the solar cells.

6

Conclusions and Recommendations

This thesis project addressed the fabrication of single side textured and double side textured FBC solar cells using the optimised poly-SiO_x passivating contacts. Section 6.1 of this chapter summarises some of the major findings from the experiments conducted in order to achieve the primary objectives. Section 6.2 consists of recommendations for future work.

Section 6.1 Conclusions

Optimised poly-SiO_x passivating contacts

The first objective of this thesis dealt with the optimisation of p-type flat, n-type textured and p-type textured poly-SiO_x passivating contacts. Having used the method of dry thermal oxidation for the growth of the interfacial tunnel oxide layer, the first step towards achieving desired passivation quality was the identification of the optimum thermal budgets for oxidation and the optimum high temperature annealing conditions. With regards to the p-type flat and n-type textured contacts, the thermal budget of 675˚C 6 minutes was identified as the ideal tunnel oxide growth condition in combination with a high temperature annealing performed at 950˚C 10 minutes. The implementation of the SiN_x/FGA hydrogenation scheme on these resulted in an excellent passivation quality indicated by an iV_{oc} of 711 mV for the p-type flat contacts and an iV_{oc} of 709 mV for the n-type textured contacts.

Taking into account the p-type textured contacts which have been established as a major constraint owing to their limited passivation quality, the thermal budget of 675˚C 3 minutes was found to be the optimum tunnel oxide growth condition with 950˚C 15 minutes being the ideal high temperature annealing condition. Additional experiments performed using the same oxidation thermal budget to further improve the passivation of this specific contact showed that the two-step annealing scheme yielded beneficial results. A first round of annealing performed at 950˚C 1 minute post the LPCVD intrinsic layer ((i) a-Si) growth, in conjunction with a second round of annealing at 950˚C 10 minutes post the Boron doped a-SiO_x:H layer deposition in PECVD resulted in a 25 mV improvement in iV_{oc}. Finally, the execution of the SiN_x/FGA hydrogenation technique culminated in a final iV_{oc} of 687 mV which is the highest passivation quality that has been achieved for p-type textured poly-SiO_x symmetric samples. Having seen a difference in optimum thermal budgets for n-type textured and p-type textured contacts and the need to utilise a common thermal budget for solar cell fabrication, the thermal budget of 675˚C 3 minutes was implemented on the n-type textured

contacts with the inclusion of the two-step annealing scheme. A final iV_{oc} of 691mV was obtained for n-type textured contact post hydrogenation using the method of SiN_x/FGA.

Single side textured FBC solar cell with 20.94% efficiency

The second objective of this thesis focused on the fabrication of single side textured FBC solar cells using the optimised n-type textured and p-type flat poly-SiO_x contacts. The solar cell design made use of tunnel oxide layers grown thermally at 675 °C 6 minutes in accordance with the results obtained for the optimised contacts. The device made use a double side ITO layer in combination with the metallisation technique of screen printing which resulted in a conversion efficiency of 20.94% on a 4-cm^2 solar cell. The final V_{oc} of 694mV obtained despite losses from metallisation indicates excellent passivation properties enabled by the thermally grown tunnel oxide layer in combination with the poly-SiO_x passivating contacts. The FF of 79.6% corresponds to effective carrier transport through the passivating contacts and carrier collection at the metal contacts. The disparity between the pseudo-FF (PFF) of 84.5% and FF of 79.6% points towards high series resistance which can be rectified by further optimising the fabrication process with focus on the screen-printing technique known to have high contact resistivity. The relatively lower J_{sc} of 37.91mA/cm^2 could be a consequence of parasitic absorption in the LPCVD a-Si:H layer and the double-sided ITO layers. Although the inclusion of a front side ARC layer on reference solar cells showed improvements in J_{sc}, the obtained improvement was negated by a drop in FF and Voc.

Comparison of single side textured FBC solar cell using thermal oxide and NAOS

The third objective of this thesis was a comparison of single side textured FBC solar cells fabricated using two different tunnel oxide growth methods :- dry thermal oxidation and NAOS. Both the devices were fabricated using identical processes with the only difference being the tunnel oxide growth method. The use of a thermally grown tunnel oxide layer resulted in a conversion efficiency of 20.94% on a 4cm^2 screen printed solar cell. On the other hand, the tunnel oxide layer grown by the method of NAOS resulted in a conversion efficiency of 20.37% once again on a 4 cm^2 screen printed solar cell. The superiority demonstrated by the thermal oxidation over NAOS is a consequence of tunnel oxide induced junction formation that enables efficient carrier selectivity and carrier collection resulting in a stronger passivation quality. The difference in passivation quality of thermally grown oxide layers can be validated by the higher V_{oc} and FF of 694mV and 79.6% in comparison to a V_{oc} and FF of 687mV and 78.52% obtained when using NOAS grown oxide layers. In addition to this, the lower FF obtained when using NAOS also indicates the formation of a thicker tunnel oxide layer that creates a larger barrier for carriers to tunnel through.

Double side textured FBC solar cells with 19.38% efficiency

The final objective of this thesis looked into the fabrication of double side textured solar cells using the optimised n-type textured and p-type textured poly-SiO_x contacts. It is worth mentioning that this is the first time that the double side textured solar cell architecture has

been implemented using poly-SiO_x passivating contacts. The solar cell design made use of a tunnel oxide layer grown thermally at 675 ˚C for 3 minutes in accordance with the results obtained for the optimised contacts. The two-step annealing scheme that showed significant enhancement in passivation was implemented in the design. An iV_{oc} of 698mV was recorded post hydrogenation using SiN_x/FGA. Following this, the use of a double side ITO layer in combination with the metallisation technique of screen printing resulted in a conversion efficiency of 19.38% on a 4-cm^2 solar cell. Despite attaining high passivation post hydrogenation, the final V_{oc} of the solar cell was limited to 661mV owing to the losses from screen printing and ITO deposition. The inability to recover the passivation loss post ITO deposition to the full extend using thermal annealing in H_2 proved to be detrimental for this design. The optical enhancement brought on by the use of a textured surface at the rear side of the solar cell is curbed by the restricted passivation at the rear contact (p^+poly-SiO_x) evident from the J_{sc} value of 37.65mA/cm^2 which should typically be higher than what is recorded for the single side textured solar cell.

6.2 Recommendations

Accurate measurements of the tunnel oxide layer thickness using spectroscopic ellipsometry can provide better insights on the extent to which the tunnel oxide layer thickness impacts the dopant diffusion along with chemical and field effect passivation [95]. In addition to this, contact resistivity studies using the Transmission Line Method (TLM) can be performed to understand the change in resistivity through poly-SiO_x/SiO_x/c-Si (n-type) stack influenced by the tunnel oxide layer thickness. Fluctuations in contact resistivity with change in thickness of the tunnel oxide layer is also an indication of how effective the tunnelling transport is through the interfacial oxide layer [95]. Lastly pinhole conductivity measurements performed using conductive atomic force microscopy (cAFM) can help investigate the extent of pinhole emergence due to degradation of the tunnel oxide layer at high temperatures [96].

With regards to the single side textured FBC solar cells, further optimisation of the ARC layer thickness along with accurate measurement techniques could mitigate the observed loss in V_{oc} and FF. The performance degradation induced by screen printing especially in the case of thin poly-SiO_x layers can be resolved by using an alternative metallisation techniques that uses copper electroplated contacts with seed layers made of Ag or Ti [97]. The technique of copper plating known for its higher aspect ratios resulting in lower shading losses can contribute to higher Jsc and reduction in overall production costs [98]. Lastly, a TLM analysis can be performed to have an estimate of the metal-polySiO_x contact resistivity a major determinant of the series resistance of the solar cells.

For the double side textured FBC solar cells, adopting low damage sputter deposition techniques for ITO layers combined with thermal annealing could mitigate the loss in passivation to an extent. The use of a double layer ITO stack comprised of a low power sputtered thin transitional ITO layer below the standard thick high-power sputtered ITO layer has proven to alleviate the sputtering induced loss in passivation properties[99]. Lastly, as

mentioned in the case of single side textured solar cells, use of alternative metallisation techniques such as copper plating can reduce metallisation induced degradation in passivation quality and lead to higher J_{sc}s

Bibliography

[1] C. López, “Current Challenges in Energy,” *Packag. (Boston, Mass.)*, no. November, pp. 285–300, 2006.

[2] BP, “Statistical Review of World Energy globally consistent data on world energy markets . and authoritative publications in the field of energy The Statistical Review world of World Energy and data on world energy markets from is The Review has been providing,” p. 66, 2020.

[3] “How can we transition to renewable energy?” [Online]. Available: https://www.rics.org/nl/news-insight/future-of-surveying/sustainability/transition-to-renewable-energy/. [Accessed: 26-Apr-2021].

[4] “World Adds Record New Renewable Energy Capacity in 2020.” [Online]. Available: https://www.irena.org/newsroom/pressreleases/2021/Apr/World-Adds-Record-New-Renewable-Energy-Capacity-in-2020. [Accessed: 26-Apr-2021].

[5] I. Renewable and E. Agency, *Renewable capacity statistics 2016 Statistiques de capacité renouvelable 2016 Estadísticas de capacidad renovable 2016*. 2016.

[6] “World now has 583.5 GW of operational PV – pv magazine International.” [Online]. Available: https://www.pv-magazine.com/2020/04/06/world-now-has-583-5-gw-of-operational-pv/. [Accessed: 26-Apr-2021].

[7] IRENA, *Future of solar photovoltaic: Deployment, investment, technology, grid integration and socio-economic aspects (A Global Energy Transformation: paper)*, vol. November. 2019.

[8] “Solar PV costs fall 82% over the last decade, says IRENA | Solar Power Portal.” [Online]. Available: https://www.solarpowerportal.co.uk/news/solar_pv_costs_fall_82_over_the_last_decade_says_irena. [Accessed: 26-Apr-2021].

[9] International Renewable Energy Agency, *IRENA (2019), Global Energy Transformation: A Roadmap to 2050*. 2019.

[10] M. A. Green, “Third generation photovoltaics: Ultra-high conversion efficiency at low cost,” *Prog. Photovoltaics Res. Appl.*, vol. 9, no. 2, pp. 123–135, 2001.

[11] P. R. I. F. O. R. S. E. S. ISE, “Photovoltaics Report,” no. September, 2012.

[12] T. Saga, “Advances in crystalline silicon solar cell technology for industrial mass production,” *NPG Asia Mater.*, vol. 2, no. 3, pp. 96–102, 2010.

[13] C. Battaglia, A. Cuevas, and S. De Wolf, “High-efficiency crystalline silicon solar cells: status and perspectives,” | *Energy Environ. Sci*, vol. 9, p. 1552, 2016.

[14] M. Z. Arno Smets, Klaus Jäger, Olindo Isabella, René van Swaaij, “Solar Energy: The Physics and Engineering of Photovoltaic Conversion, Technologies and Systems,” *UIT*

Cambridge, p. 488, 2016.

[15] O. K. Simya, P. Radhakrishnan, A. Ashok, K. Kavitha, and R. Althaf, "Engineered nanomaterials for energy applications," *Handb. Nanomater. Ind. Appl.*, pp. 751–767, 2018.

[16] G. Hahn and S. Joos, "Advances in Photovoltaics: Part 3," *Semicond. Semimetals*, vol. 90, pp. 1–72, 2014.

[17] M. Plakhotnyuk, "Nanostructured Heterojunction Crystalline Silicon Solar Cells with Transition Metal Oxide Carrier Selective Contacts," *Phd Thesis*, 2018.

[18] G. E. Jellison and P. C. Joshi, "Crystalline silicon solar cells," *Springer Ser. Opt. Sci.*, vol. 212, no. May, pp. 201–225, 2018.

[19] R. S. Bonilla, C. Reichel, M. Hermle, and P. Wilshaw, "Electric field effect surface passivation for silicon solar cells," *Solid State Phenom.*, vol. 205–206, pp. 346–351, 2014.

[20] J. Bullock, "Advanced Contacts For Crystalline Silicon Solar Cells," no. February, 2016.

[21] J. Melskens, B. W. H. Van De Loo, B. Macco, L. E. Black, S. Smit, and W. M. M. Kessels, "Passivating Contacts for Crystalline Silicon Solar Cells: From Concepts and Materials to Prospects," *IEEE J. Photovoltaics*, vol. 8, no. 2, pp. 373–388, 2018.

[22] T. Fellmeth *et al.*, "20.1% Efficient Silicon Solar Cell With Aluminum Back Surface Field," *IEEE Electron Device Lett.*, vol. 32, no. 8, pp. 1101–1103, 2011.

[23] A. W. Blakers, A. Wang, A. M. Milne, J. Zhao, and M. A. Green, "22.8% Efficient Silicon Solar Cell," *Appl. Phys. Lett.*, vol. 55, no. 13, pp. 1363–1365, 1989.

[24] M. Taguchi *et al.*, "24.7% Record efficiency HIT solar cell on thin silicon wafer," *IEEE J. Photovoltaics*, vol. 4, no. 1, pp. 96–99, 2014.

[25] A. Ur Rehman and S. H. Lee, "Advancements in n-type base crystalline silicon solar cells and their emergence in the photovoltaic industry," *Sci. World J.*, vol. 2013, 2013.

[26] F. Gaspari, "Optoelectronic Properties of Amorphous Silicon the Role of Hydrogen: from Experiment to Modeling," *Optoelectron. - Mater. Tech.*, no. September 2011, 2011.

[27] D. C. Wu *et al.*, "Experimental and theoretical investigation of annealing effects on hetero-junction a-Si/c-Si solar cells," *Conf. Rec. IEEE Photovolt. Spec. Conf.*, pp. 002968–002971, 2011.

[28] G. Limodio *et al.*, "Front and rear contact Si solar cells combining high and low thermal budget Si passivating contacts," *Sol. Energy Mater. Sol. Cells*, vol. 194, pp. 28–35, 2019.

[29] I. Electron and D. Letters, "Heavily Doped Polysilicon-Contact Solar," no. 7, pp. 363–365, 1985.

[30] A. H. Tuan Le *et al.*, "Temperature-dependent performance of silicon solar cells with polysilicon passivating contacts," *Sol. Energy Mater. Sol. Cells*, vol. 225, no. March, p. 111020, 2021.

[31] Y. Tao, V. Upadhyaya, K. Jones, and A. Rohatgi, “Tunnel oxide passivated rear contact for large area n-type front junction silicon solar cells providing excellent carrier selectivity,” *AIMS Mater. Sci.*, vol. 3, no. 1, pp. 180–189, 2016.

[32] A. Richter, J. Benick, F. Feldmann, A. Fell, M. Hermle, and S. W. Glunz, “n-Type Si solar cells with passivating electron contact: Identifying sources for efficiency limitations by wafer thickness and resistivity variation,” *Sol. Energy Mater. Sol. Cells*, vol. 173, no. May, pp. 96–105, 2017.

[33] Z. Zhang *et al.*, “Carrier transport through the ultrathin silicon-oxide layer in tunnel oxide passivated contact (TOPCon) c-Si solar cells,” *Sol. Energy Mater. Sol. Cells*, vol. 187, no. June, pp. 113–122, 2018.

[34] F. Feldmann, M. Bivour, C. Reichel, H. Steinkemper, M. Hermle, and S. W. Glunz, “Tunnel oxide passivated contacts as an alternative to partial rear contacts,” *Sol. Energy Mater. Sol. Cells*, vol. 131, pp. 46–50, 2014.

[35] F. Feldmann, M. Simon, M. Bivour, C. Reichel, M. Hermle, and S. W. Glunz, “Efficient carrier-selective p- and n-contacts for Si solar cells,” *Sol. Energy Mater. Sol. Cells*, vol. 131, pp. 100–104, 2014.

[36] R. Santbergen *et al.*, “Optical analysis of poly-Si and poly-SiOx carrier-selective passivating contacts for c-Si solar cells,” *Opt. InfoBase Conf. Pap.*, vol. Part F71-P, no. 1, pp. 5–7, 2017.

[37] G. R. Wolstenholme, N. Jorgensen, P. Ashburn, and G. R. Booker, “An investigation of the thermal stability of the interfacial oxide in polycrystalline silicon emitter bipolar transistors by comparing device results with high-resolution electron microscopy observations,” *J. Appl. Phys.*, vol. 61, no. 1, pp. 225–233, 1987.

[38] T. Grundler, A. Lambertz, and F. Finger, “N-type hydrogenated amorphous silicon oxide containing a microcrystalline silicon phase as an intermediate reflector in silicon thin film solar cells,” *Phys. Status Solidi Curr. Top. Solid State Phys.*, vol. 7, no. 3–4, pp. 1085–1088, 2010.

[39] passco, “Passivating contacts for crystalline silicon solar cells,” p. 90, 2006.

[40] B. Singha and C. S. Solanki, “N-type solar cells: Advantages, issues, and current scenarios,” *Mater. Res. Express*, vol. 4, no. 7, 2017.

[41] J. Kim, D. Inns, K. Fogel, and D. K. Sadana, “Surface texturing of single-crystalline silicon solar cells using low density SiO2 films as an anisotropic etch mask,” *Sol. Energy Mater. Sol. Cells*, vol. 94, no. 12, pp. 2091–2093, 2010.

[42] J. X. J. Zhang and K. Hoshino, *Fundamentals of nano/microfabrication and scale effect*. 2019.

[43] M. K. Stodolny *et al.*, “n-Type polysilicon passivating contact for industrial bifacial n-type solar cells,” *Sol. Energy Mater. Sol. Cells*, vol. 158, pp. 24–28, 2016.

[44] K. Hieber, M. Stolz, and C. Weiczorek, “PLASMA ENHANCED CHEMICAL VAPOR DEPOSITION OF TaSi//2.,” *Proc. - Electrochem. Soc.*, vol. 84–6, no. Cvd, pp. 205–212, 1984.

[45] J. Alarcón-Salazar *et al.*, "Silicon-Rich Oxide Obtained by Low-Pressure Chemical Vapor Deposition to Develop Silicon Light Sources," *Chem. Vap. Depos. - Recent Adv. Appl. Opt. Sol. Cells Solid State Devices*, no. Cvd, 2016.

[46] Plasma-Therm, "Plasma-Therm: PECVD." [Online]. Available: http://www.plasma-therm.com/pecvd.html. [Accessed: 13-Apr-2021].

[47] M. K. Stodolny *et al.*, "Material properties of LPCVD processed n-type polysilicon passivating contacts and its application in PERPoly industrial bifacial solar cells," *Energy Procedia*, vol. 124, pp. 635–642, 2017.

[48] J. Melskens, "Optimisation of a protocrystalline hydrogenated amorphous silicon top solar cell for highest stabilised efficiency," no. March, 2007.

[49] S. Choi *et al.*, "Structural evolution of tunneling oxide passivating contact upon thermal annealing," *Sci. Rep.*, vol. 7, no. 1, pp. 1–11, 2017.

[50] G. Yang, A. Ingenito, N. Van Hameren, O. Isabella, and M. Zeman, "Design and application of ion-implanted polySi passivating contacts for interdigitated back contact c-Si solar cells," *Appl. Phys. Lett.*, vol. 108, no. 3, 2016.

[51] B. J. Hallam, P. G. Hamer, A. M. Ciesla née Wenham, C. E. Chan, B. Vicari Stefani, and S. Wenham, "Development of advanced hydrogenation processes for silicon solar cells via an improved understanding of the behaviour of hydrogen in silicon," *Prog. Photovoltaics Res. Appl.*, vol. 28, no. 12, pp. 1217–1238, 2020.

[52] R. Entner, "Modeling and Simulation of Negative Bias Temperature Instability," no. April 2007, p. 137, 2007.

[53] J. Loffler, *Transparent Conductive Oxides for Thin-Film Silicon Solar Cells*. 2005.

[54] A. Ebong and N. Chen, "Metallization of crystalline silicon solar cells: A review," *2012 9th Int. Conf. High Capacit. Opt. Networks Enabling Technol. HONET 2012*, pp. 102–109, 2012.

[55] E. Rodríguez *et al.*, "We are IntechOpen , the world ' s leading publisher of Open Access books Built by scientists , for scientists TOP 1 %," *Intech*, vol. 32, no. tourism, pp. 137–144, 1989.

[56] R. A. Sinton, S. Consulting, S. Jose, A. Cuevas, and M. Stuckings, "Cell Material and Device Characterization," *Time*, pp. 457–460, 1996.

[57] "WCT-120 - Sinton Instruments." [Online]. Available: https://www.sintoninstruments.com/products/wct-120/. [Accessed: 24-Jun-2021].

[58] P. Guo, "contacts for high-efficiency solar cells Master of Science Thesis Development of in-situ doped poly- SiO x passivating contacts for high- efficiency solar cells."

[59] A. G. Aberle, S. W. Glunz, A. W. Stephens, and M. A. Green, "High-eficiency silicon solar cells: Si/SiO2, interface parameters and their impact on device performance," *Prog. Photovoltaics Res. Appl.*, vol. 2, no. 4, pp. 265–273, 1994.

[60] R. Peibst *et al.*, "Working principle of carrier selective poly-Si/c-Si junctions: Is tunnelling the whole story?," *Sol. Energy Mater. Sol. Cells*, vol. 158, pp. 60–67, 2016.

[61] R. Williams, “Photoemission of Electrons from Silicon into Silicon Dioxide-,” *IEEE Trans. Electron Devices*, vol. 12, no. 9, p. 503, 1965.

[62] A. S. Kale *et al.*, “Effect of silicon oxide thickness on polysilicon based passivated contacts for high-efficiency crystalline silicon solar cells,” *Sol. Energy Mater. Sol. Cells*, vol. 185, pp. 270–276, 2018.

[63] T. F. Wietler *et al.*, “Pinhole density and contact resistivity of carrier selective junctions with polycrystalline silicon on oxide,” *Appl. Phys. Lett.*, vol. 110, no. 25, 2017.

[64] H. Guthrey *et al.*, “Effect of Surface Texture on Pinhole Formation in SiO x-Based Passivated Contacts for High-Performance Silicon Solar Cells,” *ACS Appl. Mater. Interfaces*, vol. 12, no. 50, pp. 55737–55745, 2020.

[65] M. Lozac’h, S. Nunomura, and K. Matsubara, “Double-sided TOPCon solar cells on textured wafer with ALD SiOx layer,” *Sol. Energy Mater. Sol. Cells*, vol. 207, no. November 2019, 2020.

[66] P. Specialities, “PSI Processing Services.” [Online]. Available: http://www.processspecialties.com/waferpro.htm. [Accessed: 13-Apr-2021].

[67] M. Zacharias and P. Streitenberger, “Crystallization of amorphous superlattices in the limit of ultrathin films with oxide interfaces,” *Phys. Rev. B - Condens. Matter Mater. Phys.*, vol. 62, no. 12, pp. 8391–8396, 2000.

[68] G. Nogay *et al.*, “Interplay of annealing temperature and doping in hole selective rear contacts based on silicon-rich silicon-carbide thin films,” *Sol. Energy Mater. Sol. Cells*, vol. 173, no. April, pp. 18–24, 2017.

[69] G. Limodio *et al.*, “Implantation-based passivating contacts for crystalline silicon front/rear contacted solar cells,” *Prog. Photovoltaics Res. Appl.*, vol. 28, no. 5, pp. 403–416, 2020.

[70] O. I. G. Yang, S.K. Senthil Kumar, P.A. Procel Moya, Y. Zhao, C. Han, M. Singh, G. Limodio, L. Mazzarella, A.W. Weeber, M. Zeman, “Development of Poly-Si Passivating Contacts on Textured Si Surface for Bottom c-Si Solar Cell Application.” [Online]. Available: https://www.eupvsec-planner.com/presentations/c49213/development_of_poly-si_passivating_contacts_on_textured_si_surface_for_bottom_c-si_solar_cell_application.htm. [Accessed: 15-May-2021].

[71] R. Van Der Vossen, F. Feldmann, A. Moldovan, and M. Hermle, “Comparative study of differently grown tunnel oxides for p-type passivating contacts,” *Energy Procedia*, vol. 124, pp. 448–454, 2017.

[72] S. Kumar, “Ultra-thin thermal SiOx,” 2020.

[73] K. R. McIntosh and L. P. Johnson, “Recombination at textured silicon surfaces passivated with silicon dioxide,” *J. Appl. Phys.*, vol. 105, no. 12, 2009.

[74] J. S. Christenserr, H. H. Radamson, A. Y. Kuznetsov, and B. G. Svensson, “Phosphorus and boron diffusion in silicon under equilibrium conditions,” *Appl. Phys. Lett.*, vol. 82, no. 14, pp. 2254–2256, 2003.

[75] D. A. Antoniadis, “Diffusion in Silicon.,” *NATO ASI Ser. Ser. E Appl. Sci.*, no. 62, pp. 1–48, 1983.

[76] F. Feldmann, J. Schön, J. Niess, W. Lerch, and M. Hermle, “Studying dopant diffusion from Poly-Si passivating contacts,” *Sol. Energy Mater. Sol. Cells*, vol. 200, no. May, p. 109978, 2019.

[77] W. Liu *et al.*, “Polysilicon Passivating Contacts for Silicon Solar Cells: Interface Passivation and Carrier Transport Mechanism,” *ACS Appl. Energy Mater.*, vol. 2, no. 7, pp. 4609–4617, 2019.

[78] M. Lozac’h, S. Nunomura, and K. Matsubara, “Double-sided TOPCon solar cells on textured wafer with ALD SiOx layer,” *Sol. Energy Mater. Sol. Cells*, vol. 207, no. December 2019, 2020.

[79] J. Stuckelberger *et al.*, “Passivating electron contact based on highly crystalline nanostructured silicon oxide layers for silicon solar cells,” *Sol. Energy Mater. Sol. Cells*, vol. 158, pp. 2–10, 2016.

[80] G. Limodio *et al.*, “High temperature oxidation pre-treatment of textured c-Si wafers passivated by a-Si:H,” *Mater. Sci. Semicond. Process.*, vol. 97, pp. 67–70, 2019.

[81] B. W. H. Van De Loo *et al.*, “Solar Energy Materials and Solar Cells On the hydrogenation of Poly-Si passivating contacts by Al 2 O 3 and SiN x thin films,” *Sol. Energy Mater. Sol. Cells*, vol. 215, no. May, p. 110592, 2020.

[82] C. Han *et al.*, “Realizing the Potential of RF-Sputtered Hydrogenated Fluorine-Doped Indium Oxide as an Electrode Material for Ultrathin SiO x/Poly-Si Passivating Contacts,” *ACS Appl. Energy Mater.*, vol. 3, no. 9, pp. 8606–8618, 2020.

[83] L. Y. Mai, “Overcoming the Performance and Limitations of Commercial Screen-Printed Solar Cells,” no. August, p. 225, 2010.

[84] S. Kontermann, A. Grohe, and R. Preu, “Detailed analysis of annealing silver front side contacts on silicon solar cells,” *Conf. Rec. IEEE Photovolt. Spec. Conf.*, 2008.

[85] A. Nakane, S. Fujimoto, and H. Fujiwara, “Fast determination of the current loss mechanisms in textured crystalline Si-based solar cells,” *J. Appl. Phys.*, vol. 122, no. 20, 2017.

[86] D. Choi, H. Yoon, K. H. Kim, H. D. Um, and K. Seo, “ITO-free carrier-selective contact for crystalline silicon solar cells,” *J. Mater. Chem. A*, vol. 7, no. 5, pp. 2192–2199, 2019.

[87] L. Serenelli, M. Miliciani, M. Izzi, R. Chierchia, A. Mittiga, and M. Tucci, “Advances in screen printing metallization for a-Si:H/c-Si heterojunction solar cells,” *2014 IEEE 40th Photovolt. Spec. Conf. PVSC 2014*, pp. 2528–2532, 2014.

[88] C. Han *et al.*, “Room-temperature sputtered tungsten-doped indium oxide for improved current in silicon heterojunction solar cells,” *Sol. Energy Mater. Sol. Cells*, vol. 227, p. 111082, 2021.

[89] J. Yu *et al.*, “Tungsten doped indium oxide film: Ready for bifacial copper metallization of silicon heterojunction solar cell,” *Sol. Energy Mater. Sol. Cells*, vol. 144, pp. 359–363,

2016.

[90] D. Zhang *et al.*, “Design and fabrication of a SiOx/ITO double-layer anti-reflective coating for heterojunction silicon solar cells,” *Sol. Energy Mater. Sol. Cells*, vol. 117, pp. 132–138, 2013.

[91] P. C. Hsiao, W. Zhang, Z. Li, U. Romer, and A. Lennon, “Direct Copper Plating to IWO for Silicon Heterojunction Solar Cells,” *2018 IEEE 7th World Conf. Photovolt. Energy Conversion, WCPEC 2018 - A Jt. Conf. 45th IEEE PVSC, 28th PVSEC 34th EU PVSEC*, pp. 3719–3721, 2018.

[92] Z. C. Holman *et al.*, “Infrared light management in high-efficiency silicon heterojunction and rear-passivated solar cells,” *J. Appl. Phys.*, vol. 113, no. 1, 2013.

[93] Y. Zeng *et al.*, “Theoretical exploration towards high-efficiency tunnel oxide passivated carrier-selective contacts (TOPCon) solar cells,” *Sol. Energy*, vol. 155, pp. 654–660, 2017.

[94] A. Anusha, C. Parameswaran, P. Revathi, and V. Velmurugan, “Numerical simulation of dry and wet oxidation of Silicon by TCAD Sprocess,” *Proc. Int. Conf. "Advanced Nanomater. Emerg. Eng. Technol. ICANMEET 2013*, no. July 2013, pp. 513–516, 2013.

[95] A. S. Kale *et al.*, “Effect of silicon oxide thickness on polysilicon based passivated contacts for high-efficiency crystalline silicon solar cells,” *Sol. Energy Mater. Sol. Cells*, vol. 185, no. February, pp. 270–276, 2018.

[96] K. Lancaster, S. Großer, F. Feldmann, V. Naumann, and C. Hagendorf, “Study of Pinhole Conductivity at Passivated Carrier-selected Contacts of Silicon Solar Cells,” *Energy Procedia*, vol. 92, pp. 116–121, 2016.

[97] G. Limodio *et al.*, “Copper-Plating Metallization with Alternative Seed Layers for c-Si Solar Cells Embedding Carrier-Selective Passivating Contacts,” *IEEE J. Photovoltaics*, vol. 10, no. 2, pp. 372–382, 2020.

[98] D. S. Kim, E. J. Lee, J. Kim, and S. H. Lee, “Low-cost contact formation of high-efficiency crystalline silicon solar cells by plating,” *J. Korean Phys. Soc.*, vol. 46, no. 5, pp. 1208–1212, 2005.

[99] L. Tutsch, M. Bivour, W. Wolke, M. Hermle, and J. Rentsch, “Influence of the Transparent Electrode Sputtering Process on the Interface Passivation Quality of Silicon Heterojunction Solar Cells,” *33rd Eur. PV Sol. Energy Conf. Exhib.*, no. September, 2017.