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DOI
10.1002/cta.2377

Publication date
2017

Document Version
Final published version

Published in
International Journal of Circuit Theory and Applications

INTERNATIONAL JOURNAL OF CIRCUIT THEORY AND APPLICATIONS
Int. J. Circ. Theor. Appl. 2017; **45**:1901–1919
Published online 26 July 2017 in Wiley Online Library (wileyonlinelibrary.com). DOI: 10.1002/cta.2377

Synthesis-oriented double-loop feedback model

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SUMMARY

This paper presents a new feedback model that focuses on the synthesis rather than the analysis of feedback amplifiers. First, a single-loop synthesis-oriented feedback model is developed that enables the full synthesis of such amplifiers in a hierarchical and systematic way. This model is subsequently extended to a double-loop synthesis model, so that also feedback amplifiers with a characteristic input or output impedance—employing two feedback loops—can be synthesized through the same systematic approach. That these new models are suitable for synthesis lies in the fact that they map directly to the circuit level, such that the intended, asymptotic behavior as well as the various individual contributors to the deviation from this intended behavior, like finite loop gain, non-ideal input and output impedances of the forward gain block, direct feed-through and attenuations outside the feedback loop(s), are clearly distinguished and can be assigned to the responsible sections of the network. For this purpose, the double-loop synthesis model makes the transfers of the two feedback networks explicitly visible, so that it gives immediate insight in how to design these networks to get the required signal transfer and characteristic impedance.

Received 19 December 2016; Revised 9 April 2017; Accepted 7 May 2017

KEY WORDS: feedback model; synthesis; asymptotic-gain; negative feedback amplifiers; double-loop; characteristic impedance

1. INTRODUCTION

In many receiver and transceiver systems, a characteristic impedance is required at the input or output of an amplifier. A very common example is the characteristic input impedance of low-noise amplifiers in wireless receivers. Also, amplifiers that terminate or drive a surface-acoustic-wave filter require a specific input or output impedance. In broadband systems, like broadcast radio receivers or multi-band data transceivers, this characteristic impedance has to be frequency independent over a wide band. One well-known technique for this is to employ double-loop negative feedback.

When designing a feedback amplifier, the designer usually employs a design method that is based on the iterative analysis of a (sometimes large) collection of known feedback amplifiers after which the most suitable topology is tailored: Its circuit parameters are found by solving 1^{st}-order equations obtained from detailed analysis and, if necessary, iteratively optimized towards the given requirements. Although this method often seems to be efficient, it requires a relatively high level of experience, while it bears the risk of missing design solutions that fall outside the designer's experience window. Also, the fact that the design starting point is preset by previous examples blocks the full exploitation of new degrees of freedom in case of unprecedented changes in technology, application, or specifications.

This paper focusses on the *full synthesis* of double-loop feedback amplifiers. With full synthesis (in the remainder of this paper called, in short, synthesis), the methodology is meant in which both the

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amplifier topology and circuit parameters are created from scratch in a systematic, non-iterative way, basically traversing a decision tree by means of explicit design rules and criteria that do not require complex analyses or calculations [1, 2]. It directly leads the designer to the optimal topology and design solution, and as early as possible, in the synthesis process, it tells the designer if the given requirement specifications may be or certainly will not be feasible. This full synthesis approach does not require a great deal of experience and always keeps the path open towards new solutions, without being biased by the knowledge of existing designs or common habits that naturally come with experience.

Many feedback models, like the original models of Black [3] and Bode [4], signal flow diagram models [5, 6], cut-based models [7–10], and two-port network models [11], have been developed to analyze feedback amplifiers. These models are, however, not suitable for full synthesis for the simple reason that at the start of this synthesis process there is nothing to be analyzed.

To facilitate full synthesis, the model needs to explicitly show the *hierarchy* in the synthesis process. In addition, it should *map directly to the circuit level*, such that the intended as well as the relevant unwanted effects that occur in (double-loop) feedback amplifiers are reflected explicitly in the model and can be assigned to specific sections of the circuit network. As much as possible, it should clearly show what relevant (circuit related) design aspects are laying ahead when starting the synthesis, so that the various design criteria, required for synthesis, become apparent to the designer. In fact, as opposed to an analysis model, a synthesis model cannot and *should not* be fully circuit topology agnostic, because it has to guide the designer towards the correct topology.

The asymptotic-gain model, as presented in [1, 12], is considered as a good first step towards this goal. It has been used to support synthesis [2], but it lacks direct mapping to the circuit level, and in case of double-loop feedback amplifiers, it partially behaves as a black-box model, not indicating the presence of two feedback loops. Hence, it is not able to point towards the double-loop feedback-specific design criteria.

In this paper, the single-loop synthesis model is introduced first, using the asymptotic-gain model as starting point, such that it optimally suits the requirements imposed by synthesis. Secondly, it is extended to a double-loop synthesis model that enables the designer to synthesize double-loop feedback amplifiers in a *hierarchical and systematic* way, similar to their single-loop counterparts. With the help of this extended feedback model, the existing structured design methodology [2]—mainly focusing on the full synthesis of single-loop negative feedback amplifier—is complemented with additional design criteria for double-loop feedback amplifiers.

Although in principle, the double-loop synthesis model can be extended to three-loop and four-loop feedback configurations, it has been explicitly limited to double-loop systems with a characteristic impedance at one port only. Double-loop and triple-loop configurations with characteristic input and output impedances are not unilateral, causing the input impedance to depend on the load and/or the output impedance to depend on the source. An impedance mismatch at one side is reflected at the other port, making these topologies not very suitable for impedance matching purposes. The four-loop configuration does offer a unilateral amplifier with a characteristic input and output impedance. However, it is generally not a very practical topology because of its inherent complexity. If a characteristic impedance is required at both input and output, it is much more practical to cascade two double-loop amplifiers, each having just one characteristic port.

First, the properties that are required from a hierarchical synthesis model are discussed in Section 2. Section 3 briefly describes a feedback model that is currently popular for synthesis and explains why that model is not very suitable for the synthesis of single-loop and double-loop feedback amplifiers. Section 4 introduces a new single-loop model, including the interpretation of its elements, which fully suits the purpose of synthesis. Subsequently, from this new model, a double-loop synthesis model is derived in Section 5. To illustrate the model, Section 6 gives an example of the synthesis of a double-loop feedback amplifier, as far as it involves the design steps that are specific to double-loop amplifiers. Conclusions are given at the end.

2. PROPERTIES OF A HIERARCHICAL FEEDBACK MODEL

Hierarchy is a key element in the synthesis of feedback amplifiers. It is used to reduce the complexity of the design process. It basically consists of splitting up the design in two or more parts, one of which is

DOI: 10.1002/cta

mainly responsible for the performance aspect that is considered—the dominant part—and the other(s) introducing deviations from this dominant behavior—the errors. This enables the designer to find the best-case behavior with respect to a certain aspect without complex, time consuming calculations, and quickly judge if this aspect may or will certainly not meet the specifications.

Hierarchy can be created at various design levels, like signal transfer level, noise or distortion level, or transistor level. For the synthesis model discussed in this paper, we focus on the signal transfer level. At this level, the feedback amplifier is split up in two parts:

(i) the feedback network, which is (supposed to be) dominant in the behavior of the amplifier; and
(ii) the nullor implementation, where each step towards a more practical circuit implementation of the nullor generally introduces deviations.

The dominant behavior for which the feedback network is (supposed to be) responsible is called the *asymptotic behavior* and is obtained when the loop gain is infinitely large, in other words, when a nullor is assumed. Generally, the deviations from this asymptotic behavior manifest themselves in two ways: as an additive error and as a multiplicative error. This is mathematically represented as δ and ε, respectively, in

$$A_t = A_{t\infty} \cdot \varepsilon + \delta \tag{1}$$

with A_t the actual transfer and $A_{t\infty}$ the asymptotic transfer. If a nullor is present, ε is 1 and δ is zero.

It is this hierarchy that the feedback model needs to make clear explicitly. Hence, the following properties need to be satisfied:

- The asymptotic behavior and the deviations from it must be distinguished very clearly.
- The transfer of the feedback network must be present in the model explicitly.
- The additive and multiplicative errors must be modeled separately.

3. ASYMPTOTIC-GAIN MODEL

Several models have been developed in the past [1, 3–13]. Although none of them fully complies with the aforementioned requirements, the asymptotic-gain model, which will be discussed here, is of particular interest as it matches Eq. (1) and complies with two of the previously given requirements. It forms the basis of our synthesis-oriented double-loop feedback model—in the remainder of this paper referred to as synthesis model in short—developed in Section 5.

The asymptotic-gain model, developed in [12] and also derived in [1], is graphically represented by the diagram of Figure 1. It is mathematically described by

$$A_t = A_{t\infty} \frac{-A\beta'}{1 - A\beta'} + \frac{\rho}{1 - A\beta'} \tag{2}$$

with

$$A_{t\infty} = \rho - \frac{\xi\nu}{\beta'}, \tag{3}$$

the asymptotic transfer when the gain of the active part A is infinite. Coefficient β' is the feedback factor, ρ is the direct transfer from input to output, and ξ and ν are measures for the signal attenuation at the input and output of the active part, respectively.

Although this model makes a clear distinction between the asymptotic transfer $A_{t\infty}$—which targets the ideal transfer—and the additive and multiplicative errors ($\rho/(1 - A\beta')$ and $-A\beta'/(1 - A\beta')$, respectively), it does *not* model the feedback network explicitly. It seems that β' represents the feedback network, but it does not. Instead, it models the feedback *path* from E_c to E_i (Figure 1), which contains, but is not limited to, the transfer of the feedback network. To make a clear distinction between the feedback factor as used in the original asymptotic-gain model, and the feedback network transfer, in this paper, the former is designated with β', while β is strictly reserved for the transfer of the feedback network.

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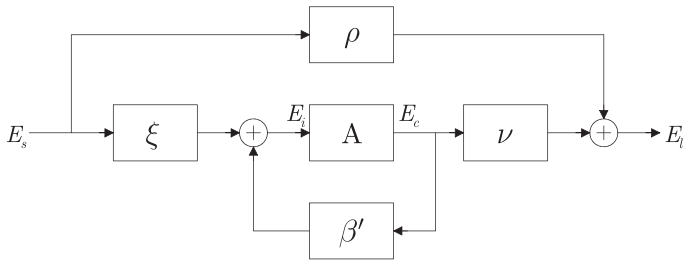

Figure 1. The asymptotic-gain model, which is not optimally suitable for the purpose of full synthesis.

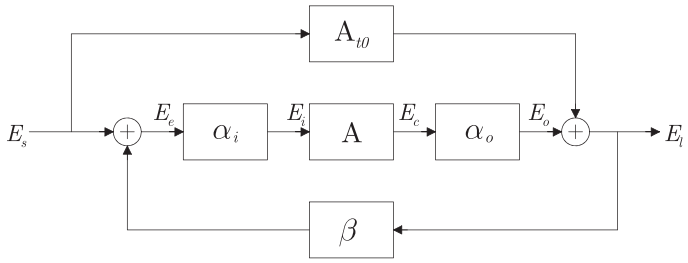

Figure 2. Synthesis-oriented single-loop feedback model, including input and output attenuations α_i and α_o, respectively, and direct transfer A_{t0}.

4. SYNTHESIS-ORIENTED SINGLE-LOOP FEEDBACK MODEL

Because the original asymptotic-gain model is not suitable for synthesis and does not meet the requirements given in Section 2, a new model is derived called the *synthesis-oriented single-loop feedback model* (in short: the synthesis model). The transfer of the feedback network β is made explicit by just defining β as being this transfer. This new single-loop synthesis model is depicted in Figure 2, where forward gain A and direct transfer $A_{t0} = \rho$ are identical to the original asymptotic-gain model and the attenuations inside the loop due the non-ideal input and output impedance of the forward active part are modeled by α_i and α_o, respectively.[‡]

From Figure 2, the transfer A_t can be calculated as

$$A_t = \frac{A'}{1 - A'\beta} + \frac{A_{t0}}{1 - A'\beta} = A_{t\infty}\frac{-A'\beta}{1 - A'\beta} + \frac{A_{t0}}{1 - A'\beta} \tag{4}$$

with $A' = \alpha_i A \alpha_o$ and $A_{t\infty} = -1/\beta$ the asymptotic transfer, that is, the transfer when $A'\beta \to \infty$. At this stage, the feedback network transfer β, as defined in our model, directly determines the asymptotic transfer $A_{t\infty}$. The relation of the feedback network transfer β to a required $A_{t\infty}$ is made explicit, which is crucial in the process of amplifier synthesis. Notice that A_{t0} is defined exactly the same as ρ in the original asymptotic-gain model.

Still missing are the possible attenuations outside the feedback loop (e.g., when a phantom-zero is created at the input or output), which have been added to the model in Figure 3. It is crucial to model these source (α_s) and load (α_l) attenuations explicitly because

(1) it enables the distinction between the feedback network, which is *supposed* to define the asymptotic behavior and the error terms (α_s and α_l) that degrade this behavior;
(2) in practical double-loop feedback amplifiers, one feedback loop will *unavoidably* face one of these attenuations, leading to new design criteria for minimizing its impact on the asymptotic behavior of such amplifiers.

[‡]At this state, the model resembles the return-difference model as given in [11], if the forward gain is made equal to $-\alpha_i A \alpha_o$. For synthesis, still, it is key to model α_i and α_o explicitly, as will be explained in Section 4.5.

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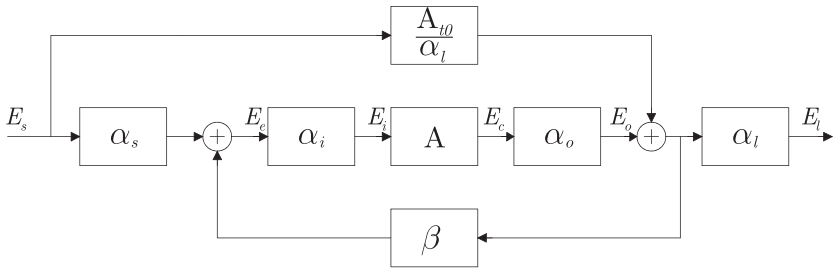

Figure 3. The complete single-loop synthesis model explicitly including all essential blocks for the evolution towards the double-loop feedback model.

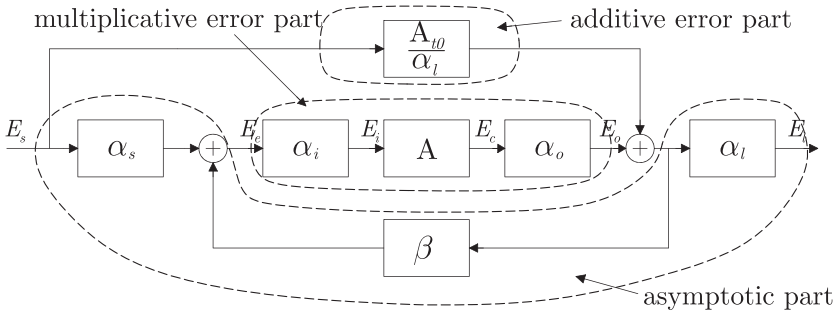

Figure 4. Single-loop synthesis model, hierarchically subdivided for synthesis: First, design the asymptotic part and then focus on the blocks in the error part.

Hence, they are key in the evolution towards a hierarchical double-loop feedback model suitable for synthesis. Notice that the addition of factor α_l in the model necessitates a rescaling of the direct transfer block with the same factor to maintain a direct transfer that equals A_{t0}.

The asymptotic transfer now becomes

$$A_{t\infty} = \alpha_s \alpha_l \cdot \left(-\frac{1}{\beta}\right) \tag{5}$$

where α_s and α_l are ideally equal to 1.

As discussed at the beginning of Section 2, hierarchy is crucial for the synthesis of feedback amplifiers. The single-loop synthesis model reflects this hierarchy by its subdivision into the asymptotic part on one side that is responsible for the asymptotic behavior of the amplifier and the multiplicative and additive error parts on the other side that represent the deviations from this asymptotic behavior according to Eq. (1) (Figure 4). The asymptotic part is designed first, assuming no error terms. If, after this first design phase, the amplifier does not meet the required specifications, it makes no sense to move to the more complex design steps that follow. But if it does, the error parts can be designed subsequently, and the final amplifier design could meet the specifications if the designer managed to keep the error terms sufficiently low.

To ensure the correct interpretation and circuit mapping of the model elements, a nullor has to be assumed for the active part of the amplifier when dealing with model elements from the asymptotic part (β, α_s, and α_l). Likewise, when dealing with model elements from the multiplicative error part (A, α_i, and α_o), the additive error is assumed to be zero; that is, no direct transfer is present: $E_s = 0$.

In the following sections, the various elements of the model are discussed in more detail, in the order in which they are dealt with during the synthesis process.

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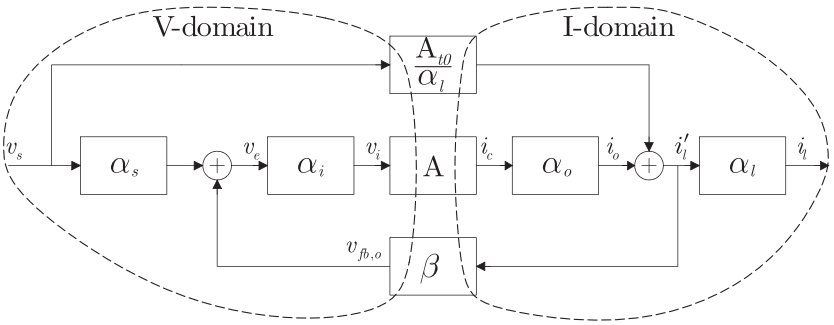

Figure 5. Single-loop synthesis model showing the assignment of the electrical signal quantities: A voltage and current have been assigned to the input and output branches of the model, respectively, for the example of a voltage-to-current amplifier.

4.1. Electrical signal quantity assignment

Besides providing hierarchy, this new single-loop synthesis model allows its various model elements to be directly mapped to the circuit level: Each of them can be assigned to a specific section of the amplifier network to be designed. This is a key property to facilitate the full synthesis of feedback amplifiers, where these amplifiers can be designed without prior knowledge of existing feedback circuits or topologies. Because the (ideal) target values for the various model elements is known ($\beta = 1/A_{t\infty}$, $A \to \infty$, $\alpha_x = 1$ with $x \in \{s, i, o, l\}$ and $A_{t0} = 0$), all related sections of the amplifier network can (and should) be designed to meet these target values as much as possible.

For this mapping, it is required to assign the quantity of the source to all branches at the input side of the amplifier model and the quantity of the load to all branches at the output side of the model, because that is what the synthesized feedback amplifier network is going to be like. For instance, in a transconductance amplifier, the input side operates in the voltage domain, so voltages are assigned to the signal branches located on this side, as shown in Figure 5. Likewise, because the output is in the current domain, currents are assigned to the branches at the output side of the model. A correct assignment leads to a straightforward mapping of the model elements to specific parts of the circuit network that is being created and ensures that, for each model element, the correct chain matrix parameter is being used of the circuit network that represents that element.

4.2. Feedback block β

Feedback block β is the one that would define the asymptotic transfer of the amplifier completely, if $\alpha_s = \alpha_l = 1$. By definition, it corresponds to the inverse of the corresponding chain matrix parameter of the feedback network. For example, in the voltage amplifier of Figure 6, the voltage-to-voltage relation of the feedback network is used. Hence, $\beta = -1/A_{fb} = -Z_1/(Z_1 + Z_2)$.[§]

4.3. Source en load attenuations α_s and α_l

The elements α_s and α_l model the attenuations at the source and load, respectively, that are beyond the control of the feedback loop. Ideally, they should be one. Smaller values indicate a (possibly significant) reduction in noise (if $\alpha_s < 1$) or linearity performance (if $\alpha_l < 1$) [14] and should be prevented.

Just like with β, formally, the active part has to be replaced by a nullor when calculating the source attenuation. Practically, though, α_s can be found as the transfer from the source to the input of the ideal transactor, with the controlled source of this transactor switched off. The type of transactor has to match the amplifier input and output quantities.[¶] For example, a v→i amplifier requires a voltage-controlled current source. Likewise, the load attenuation is the transfer from the controlled source of the ideal

[§]The minus sign is because the output voltage of the feedback network is *subtracted* from the source voltage.

[¶]This ensures that $\alpha_i = \alpha_o = 1$ and $A_{t0} = 0$, so that the output signal of α_s indeed ends up directly at the input of the transactor (A).

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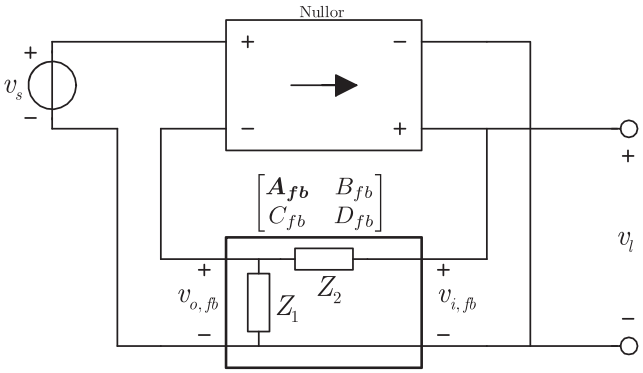

Figure 6. Interpretation of feedback block β in case of a voltage feedback amplifier.

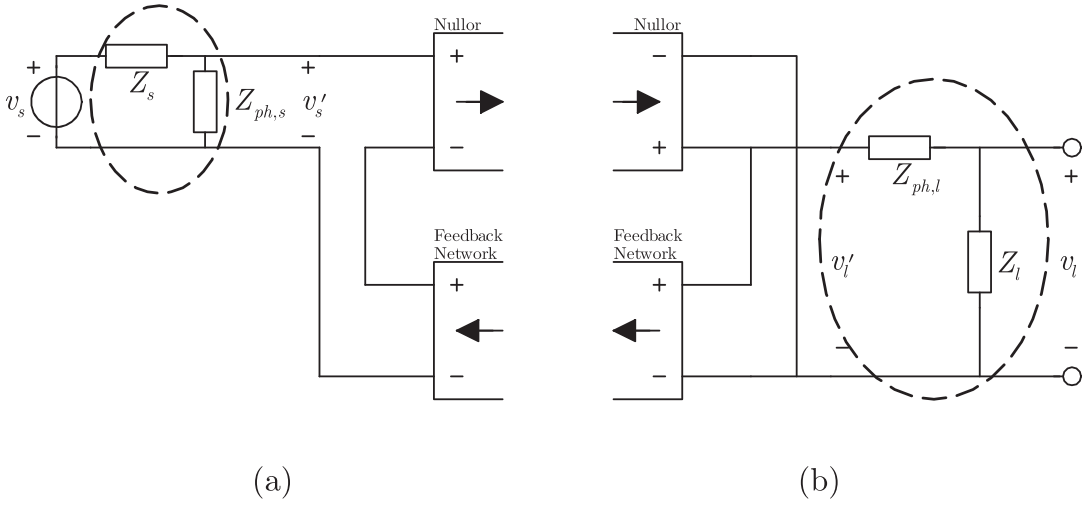

Figure 7. Attenuations *outside* the feedback loop at the source (a) and load (b), due to, for example, the implementation of a phantom-zero (frequency compensation) at the input ($Z_{ph,s}$) and output ($Z_{ph,l}$).

transactor to the load, with the signal source turned off. Also, here it is often possible to isolate the source and load attenuation networks and use their respective chain matrices. Figure 7(a) shows a voltage division at the source with $\alpha_s = v_s'/v_s = Z_{ph,s}/(Z_{ph,s} + Z_s)$ and Figure 7(b) a similar division at the load: $\alpha_l = v_l/v_l' = Z_l/(Z_l + Z_{ph,l})$.

4.4. Gain block A

This element is directly visible as the gain of the active part. It is the inverse of the corresponding chain matrix parameter: In a voltage amplifier, the inverse of the A-parameter is used (the voltage gain). The higher this gain, the smaller the additive and multiplicative errors (δ and ε) and the better the performance of the feedback amplifier.

4.5. Loop attenuations α_i and α_o

The attenuation factors at the input and output of the active part are due to the non-ideal input and output impedances (Z_i and Z_o, respectively) of the nullor implementation. If α_i is less than one, the (often not very predictable) source impedance influences the loop gain, which for instance could cause stability problems. Likewise, $\alpha_o < 1$ causes the load impedance to influence the loop gain. It is these effects that make them important to be modeled explicitly.

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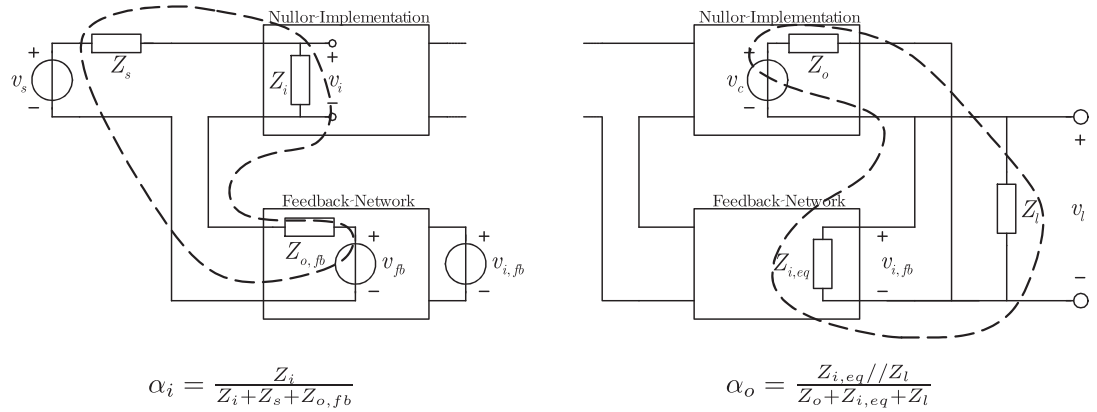

$$\alpha_i = \frac{Z_i}{Z_i + Z_s + Z_{o,fb}} \qquad \alpha_o = \frac{Z_{i,eq} // Z_l}{Z_o + Z_{i,eq} + Z_l}$$

Figure 8. Attenuations *inside* the feedback loop at the input (left) and output (right) of the active part, due to a non-ideal input (Z_i), respectively, output impedance (Z_o) of the nullor implementation. Z_s is the source impedance, Z_l the load impedance.

Figure 8 shows these attenuations in a voltage amplifier, where $Z_{i,eq}$ is the *equivalent* impedance when looking into the input port of the feedback network and $Z_{o,fb}$ is the output impedance of just the feedback network. Attenuation α_o is the voltage division at the output of the active part due to a non-zero Z_o and α_i the voltage division at the input due to a finite Z_i.

4.6. Direct transfer A_{t0}

All elements of the synthesis model are considered to be unilateral. Of course, circuit elements and electronic networks are generally not. One of the consequences is that a signal from the source can reach the load even when the controlled source of the active part is turned off. This is called the direct transfer and is modeled separately as if it is a concentrated effect.

The direct transfer can be determined by switching off the controlled source of the active part (but its input and output impedances should not be removed) and calculating the transfer from source to load.

Another consequence of the fact that the model elements are unilateral, while the actual circuit is not, is that the internal nodes of the model do not reflect actual voltages or currents of the circuit network. This is, however, not required for synthesis. The mapping of the model elements on the circuit level is applied, while obeying the hierarchical subdivision discussed earlier in this section (e.g., when α_i is interpreted/mapped, A_{t0} is forced to be zero by keeping the source quantity off).

5. SYNTHESIS-ORIENTED DOUBLE-LOOP FEEDBACK MODEL

So far, a single-loop synthesis model has been presented, which is prepared for extension towards a double-loop synthesis model. Although a number of mathematical multi-loop feedback models have been developed [15, 16] they are, again, more suitable for analysis than synthesis. Because the synthesis model explicitly models the feedback network, it can be extended to a double-loop model that is suitable for synthesis (and analysis).

5.1. Extension towards double-loop configurations

Conceptually, four double-loop feedback topologies exist: the [V,I]→V, [V,I]→I, V→[V,I], and I→[V,I] topology. Here, the [V,I] notation indicates a port with a characteristic impedance Z_{char}, which implies that at this port the electrical signal quantity can be arbitrarily considered as a voltage or current, which are mutually related by Z_{char}.

As an arbitrary vehicle, the [V,I]→I double-loop feedback amplifier, as depicted in Figure 9, is used to show how the single-loop model is expanded towards a double-loop synthesis model. At the end

DOI: 10.1002/cta

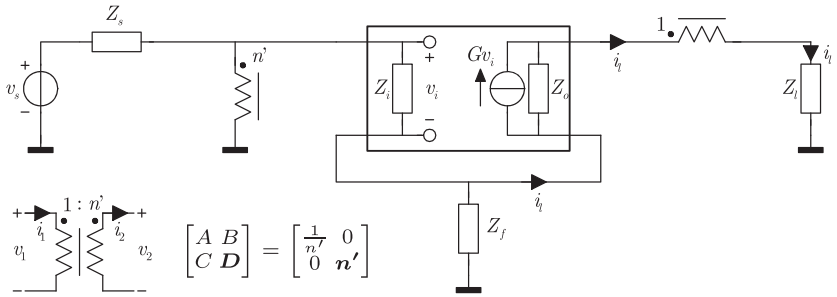

Figure 9. Double-loop feedback [V,I]-to-current amplifier. The ideal transformer, used here as current attenuator in the outer feedback network, and its chain matrix are shown in the corner.

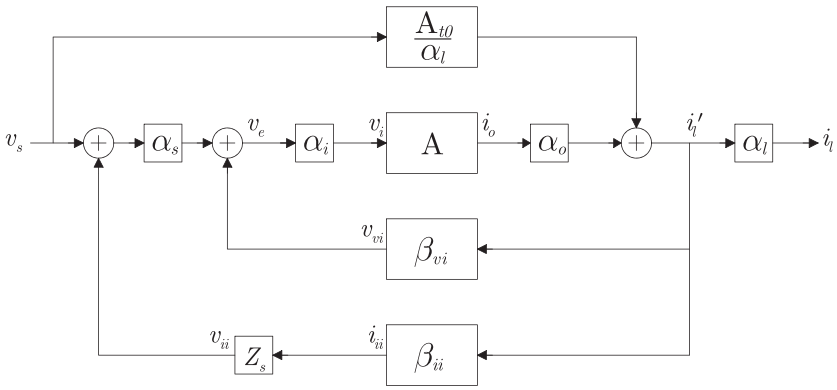

Figure 10. Double-loop synthesis model of a [V,I]-to-current amplifier.

of this section, the double-loop synthesis model is given for feedback amplifiers with a characteristic output impedance.

Resistor Z_f and the ideal transformer both sense the output current and feed it back to the input as a voltage and current, respectively. This results in a characteristic impedance at the input of $Z_{in} = n'Z_f$, with n' the transformer ratio as defined in Figure 9. Because the only difference with a transconductance amplifier is the presence of the current feedback transformer, an i→i feedback path is added to the single-loop synthesis model of a v→i amplifier, as shown in Figure 10. The output current of the i→i feedback network is transformed via Z_s into a Thévenin equivalent voltage so that it can be added to the source voltage (Figure 11). A finite output impedance of the i→i network will cause an attenuation α_s at the source. The expressions for the various double-loop feedback model elements for the [V,I]→I amplifier of Figure 9 are given in Table I, and almost all can be found directly from inspection.

If the output quantity of the inner feedback loop was chosen to be a current and that of the outer loop a voltage, this voltage is transformed across the source impedance and the obtained Norton current is added to the signal source as shown in Figure 12. As may have become clear, the signal quantity at the source is assigned such that it matches with the inner loop: If the inner loop has a voltage output, the source is modeled as a voltage source; if it has a current output, the source is modeled as a current source.

From the model given in Figure 10, it already becomes clear that two sub-configurations exist for a [V,I]-to-current amplifier: Either the current-to-current feedback network is placed in the outer feedback loop, as has been chosen in Figure 10, or the current-to-voltage feedback network is placed in the outer loop. In other words, there is a choice in the order of the feedback loops. This holds for the other double-loop feedback configurations as well, of course.

It is important to notice that both error terms α_s and α_l belong to the 'asymptotic' class, like in the single-loop synthesis model (Figure 4). Hence, they are both *independent* of Z_i, Z_o or any other components inside the active part A.

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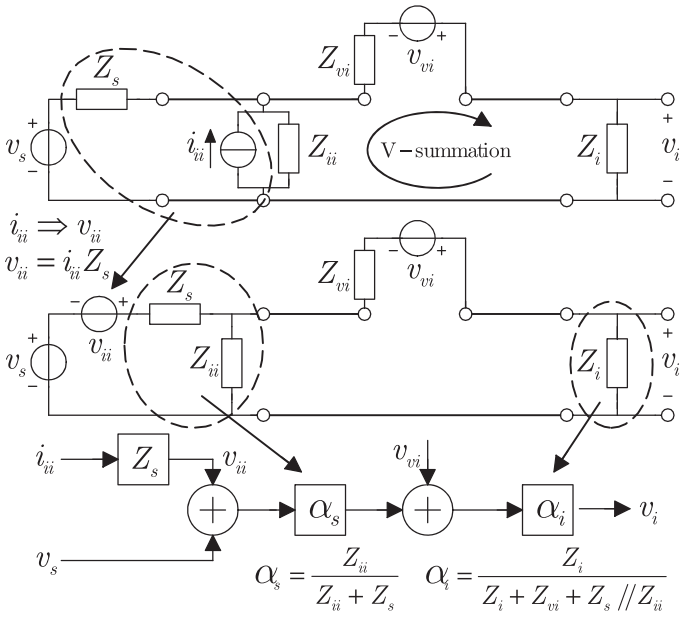

Figure 11. Thévenin equivalent of the feedback current i_{ii} and the appearance of the source attenuation α_s due to a finite output impedance Z_{ii} of the current feedback network.

Table I. Model parameters of the synthesis-oriented double-loop feedback model for the [V,I]-to-current amplifier of Figure 9 (approximations hold for $n' \gg 1$).

Asymptotic behavior	Multiplicative error	Additive error
$\beta_{vi} = Z_f$	$A = G$	$A_{t0} \approx \frac{Z_f}{Z_i+Z_s+Z_f} \times$
$\beta_{ii} = \frac{1}{n'}$	$\alpha_i = \frac{Z_i}{Z_i+Z_s+Z_f}$	$\frac{1}{Z_l'+Z_f'[1-Z_i/(n'Z_f)]+Z_i/n'}$
$\alpha_s = 1$	$\alpha_o \approx \frac{Z_o}{Z_o+Z_l+Z_f'}$	$Z_l' = Z_o + Z_l$
$\alpha_l = 1$	$Z_f' = Z_f // (Z_s + Z_i)$	$Z_f' = Z_f // (Z_s + Z_i)$

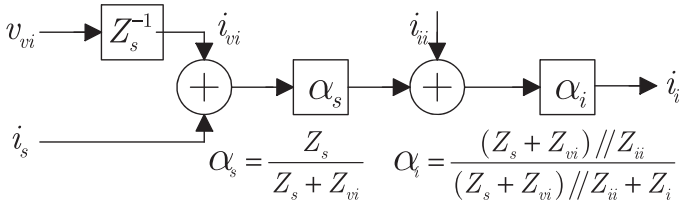

Figure 12. Norton transformation of feedback voltage v_{vi} and the appearance of source attenuation α_s due to the current division from Z_s and the non-zero output impedance Z_{vi} of the i→v feedback network.

It also implies that they both have a (negative) effect on the asymptotic behavior of the amplifier. Where in single-loop amplifiers both α_s and α_l can be made 1 in a trivial way, one of them will inherently be smaller than one in double-loop feedback amplifiers, because of the non-ideal output respectively input impedance of the outer feedback network. A non-unity value for this term results in an error in the asymptotic signal transfer and asymptotic characteristic impedance of the double-loop feedback amplifier, which will be discussed in more detail in Sections 5.2 and 5.3, respectively.

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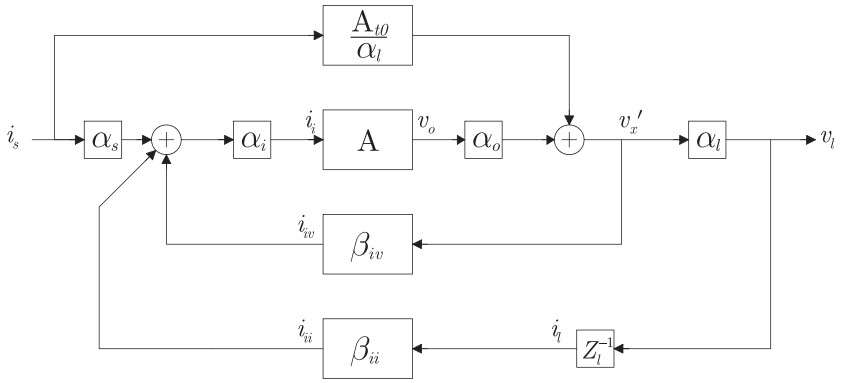

Figure 13. Double-loop synthesis model of a current-to-[V,I] amplifier with current attenuation feedback network in the output loop.

In case of a double-loop feedback amplifier with a characteristic output impedance, the two feedback networks have different input quantities, while sharing the same output quantity. Again as example, the model of an I→[V,I] amplifier with the current feedback network in the outer loop is shown in Figure 13. Here, the load voltage is transformed into an equivalent Norton current by dividing the load voltage by Z_l, similar to the transformations discussed earlier. If the outer loop was formed by the current-to-voltage feedback network, the assigned load current i_l is transformed through Z_l into the equivalent Thévenin voltage.

Also here, the signal quantity at the load is assigned such that it matches with the inner loop: If the inner loop has a voltage input, the load is modeled as a voltage; if it has a current input, the load is modeled as a current.

5.2. Signal transfer of double-loop feedback amplifiers

The signal transfer of double-loop feedback systems can be calculated from the double-loop synthesis model. For a [V,I]-to-current amplifier, the asymptotic-gain is calculated by using the model of Figure 10.

$$i_l' = A_{t0}' v_s + A' \left[\beta_{vi} i_l' + \alpha_s (v_s + Z_s \beta_{ii} i_l')\right] \tag{6}$$

with $i_l' = i_l/\alpha_l$, $A_{t0}' = A_{t0}/\alpha_l$, and $A' = \alpha_i A \alpha_o$. Rearranging terms results in

$$\frac{i_l}{v_s} = \frac{\alpha_s \alpha_l A' + A_{t0}}{1 - A'(\beta_{vi} + \alpha_s Z_s \beta_{ii})}. \tag{7}$$

Now when the effective feedback transfer β_{eff} is defined as

$$\beta_{eff} = \beta_{vi} + \alpha_s Z_s \beta_{ii}, \tag{8}$$

Eq. (7) can be rewritten as

$$A_t = A_{t\infty} \cdot \frac{A' \beta_{eff}}{1 - A' \beta_{eff}} + \frac{A_{t0}}{1 - A' \beta_{eff}} \tag{9}$$

with

$$A_{t\infty} = \alpha_s \alpha_l \cdot \left(-\frac{1}{\beta_{eff}}\right). \tag{10}$$

Clearly, the transfer of the double-loop feedback amplifier is identical to that of a single-loop amplifier when β_{eff} is used instead of β. The existence of β_{eff} could already be expected, because a multi-loop

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feedback system has still only *one* particular loop gain, although distributed across the various feedback loops. It is β_{eff} that—together with A'—constitutes the loop gain. For the other double-loop feedback topologies, β_{eff} is given in Table II, where β_{vi} equals the transfer of the $i{\rightarrow}v$ feedback network, β_{iv} the $v{\rightarrow}i$ network, and so on.

5.3. Characteristic impedance

The only reason to synthesize double-loop feedback amplifiers is to create a well-defined input or output impedance. Although [1, 17] give expressions for the characteristic impedance of double-loop feedback amplifiers, here it is derived from the ratio of two transfer parameters of the amplifier, which leads to expressions much more suitable for synthesis. For instance, the asymptotic input impedance of a [V,I]-to-current amplifier, shown in Figure 14, is found from

$$Z_{t\infty,s} = \left.\frac{v_i(s)}{i_i(s)}\right|_{A\to\infty} = \left.\frac{i_l(s)}{i_i(s)}\right|_{A\to\infty} \cdot \left.\frac{v_i(s)}{i_l(s)}\right|_{A\to\infty} = \frac{A_{t\infty,ii}}{A_{t\infty,iv}} \tag{11}$$

with $A_{t\infty,ii} = i_l/i_i$, the asymptotic gain from input *current* to output current, and $A_{t\infty,iv} = i_l/v_i$, the asymptotic gain from input *voltage* to output current. Both $A_{t\infty,ii}$ and $A_{t\infty,iv}$ can be expressed in terms of $A_{t\infty}$. If A_t is defined as i_l/v_s, these relations are given by

Table II. Effective feedback transfers for the various double-loop feedback topologies.

Characteristic port	Non-characteristic quantity	Configuration	Inner loop	$A_t =$	$\beta_{eff} =$
Input	Voltage	[V,I]→V	V→V	v_l/v_s	$\beta_{vv} + \alpha_s Z_s \beta_{iv}$
			V→I	v_l/i_s	$\beta_{iv} + \alpha_s Z_s^{-1} \beta_{vv}$
	Current	[V,I]→I	I→V	i_l/v_s	$\beta_{vi} + \alpha_s Z_s \beta_{ii}$
			I→I	i_l/i_s	$\beta_{ii} + \alpha_s Z_s^{-1} \beta_{vi}$
Output	Voltage	V→[V,I]	I→V	i_l/v_s	$\beta_{vi} + \alpha_l Z_l \beta_{vv}$
			V→V	v_l/v_s	$\beta_{vv} + \alpha_l Z_l^{-1} \beta_{vi}$
	Current	I→[V,I]	I→I	i_l/i_s	$\beta_{ii} + \alpha_l Z_l \beta_{iv}$
			V→I	v_l/i_s	$\beta_{iv} + \alpha_l Z_l^{-1} \beta_{ii}$

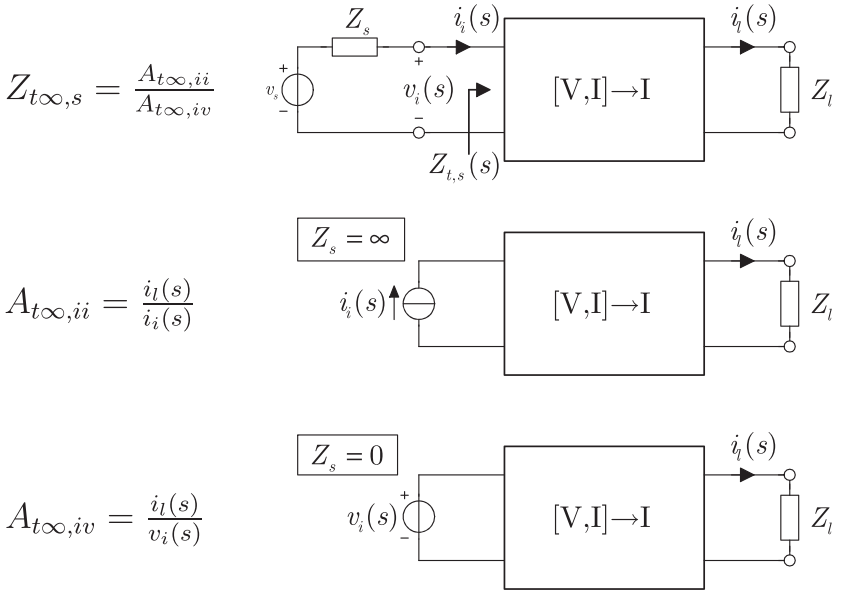

Figure 14. Input impedance of a feedback amplifier, calculated as the ratio between two transfers $A_{t\infty,ii}(s) = i_l(s)/i_i(s)\big|_{A\to\infty}$ and $A_{t\infty,iv}(s) = i_l(s)/v_i(s)\big|_{A\to\infty}$.

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$$A_{t\infty,ii} = Z_s A_{t\infty}\big|_{Z_s\to\infty} = -\alpha_l \frac{\alpha_s Z_s}{\beta_{eff}}\bigg|_{Z_s\to\infty} \tag{12}$$

$$A_{t\infty,iv} = A_{t\infty}\big|_{Z_s=0} = -\alpha_l \frac{\alpha_s}{\beta_{eff}}\bigg|_{Z_s=0} \tag{13}$$

where (10) has been used. For the [V,I]-to-current amplifier with the $i\to v$ feedback network in the inner loop and $A_t = i_l/v_s$, the asymptotic input impedance can be written as

$$Z_{t\infty,s} = \frac{\beta_{vi}/\alpha_s + Z_s\beta_{ii}\big|_{Z_s=0}}{\beta_{vi}/(\alpha_s Z_s) + \beta_{ii}\big|_{Z_s\to\infty}} = \frac{\beta_{vi}}{\beta_{ii}}//Z_{ii} \tag{14}$$

where it should be noticed that α_l is independent of Z_s and $\alpha_s Z_s|_{Z_s\to\infty} = Z_{ii}$ is the output impedance of the outer feedback network, that is, the current-to-current feedback network (recall that $\alpha_s = Z_{ii}/(Z_s + Z_{ii})$; see also Figure 11). If the output impedance of the outer feedback network were ideal, error term α_s would be one and the asymptotic input impedance would equal the ratio of the transfers of the two feedback loops. Similar results can be found for the input impedances of the three other double-loop feedback amplifier topologies with a characteristic input impedance, as well for the output impedances of the topologies with a characteristic output impedance. The asymptotic input (output) impedances of these various double-loop feedback amplifiers are listed in Table III. $Z_{t\infty}$ always equals the ratio of the two feedback loops plus some series or parallel error due to the non-ideal output (input) impedance of the outer feedback loop. If the outer loop is connected in parallel with the characteristic input (output) port, its output (input) impedance *shunts* this port, resulting in a Z_t of the form $(\beta_1/\beta_2)//Z_{fb}$. An outer feedback loop that is connected in series will have its output (input) impedance in *series* with the characteristic input (output) port, $Z_t = (\beta_1/\beta_2) + Z_{fb}$. The expressions for $Z_{t\infty}$ in Table III are generic expressions, independent of the implementation of the feedback networks.

When the expressions for β_{eff} from Table II and $Z_{t\infty}$ are combined and substituted in (10), the last column of Table III is obtained. This shows the (not very surprising) fact that $A_{t\infty}$ equals the transfer of the *single*-loop amplifier, using only the inner feedback loop, multiplied with the voltage or current division at the characteristic port due to $Z_{t\infty}$ and the source or load impedance.

Table III. Asymptotic characteristic impedances and gains for all double-loop feedback topologies.

Characteristic port	Non-characteristic quantity	Inner loop	$Z_{t\infty} =$	$A_{t\infty} =$
Input	Voltage	V→V	$(\beta_{vv}/\beta_{iv})//Z_{iv}$	$-\frac{1}{\beta_{vv}}\frac{Z_{t\infty}}{Z_{t\infty}+Z_s}\alpha_l$
		V→I	$(\beta_{vv}/\beta_{iv}) + Z_{vv}$	$-\frac{1}{\beta_{iv}}\frac{Z_s}{Z_{t\infty}+Z_s}\alpha_l$
	Current	I→V	$(\beta_{vi}/\beta_{ii})//Z_{ii}$	$-\frac{1}{\beta_{vi}}\frac{Z_{t\infty}}{Z_{t\infty}+Z_s}\alpha_l$
		I→I	$(\beta_{vi}/\beta_{ii}) + Z_{vi}$	$-\frac{1}{\beta_{ii}}\frac{Z_s}{Z_{t\infty}+Z_s}\alpha_l$
Output	Voltage	I→V	$(\beta_{vi}/\beta_{vv})//Z_{vv}$	$-\frac{1}{\beta_{vi}}\frac{Z_{t\infty}}{Z_{t\infty}+Z_l}\alpha_s$
		V→V	$(\beta_{vi}/\beta_{vv}) + Z_{vi}$	$-\frac{1}{\beta_{vv}}\frac{Z_l}{Z_{t\infty}+Z_l}\alpha_s$
	Current	I→I	$(\beta_{ii}/\beta_{iv})//Z_{iv}$	$-\frac{1}{\beta_{ii}}\frac{Z_{t\infty}}{Z_{t\infty}+Z_l}\alpha_s$
		V→I	$(\beta_{ii}/\beta_{iv}) + Z_{ii}$	$-\frac{1}{\beta_{iv}}\frac{Z_l}{Z_{t\infty}+Z_l}\alpha_s$

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5.4. Properties under matched-impedance condition

In the specific but very common case that the asymptotic port impedance $Z_{t\infty}$ equals the source (load) impedance Z_s (Z_l), a simple relation between the two feedback loops can be found. The [V,I]-to-current amplifier of Figure 9 is taken as example. Similar results can be found for the other amplifier types.

The inner loop gain is found from Figure 10 and given by

$$L_{inner} = A'\beta_{vi} \tag{15}$$

with $A' = \alpha_i A \alpha_o$. The outer loop gain is found as

$$L_{outer} = A'\beta_{ii} Z_s \alpha_s. \tag{16}$$

Assuming that $Z_{t\infty} = Z_s$ and using the third row of Table III, the following relation is obtained:

$$Z_s = \frac{\beta_{vi} Z_{ii}}{\beta_{vi} + \beta_{ii} Z_{ii}} \Leftrightarrow \beta_{vi} = \beta_{ii} \frac{Z_{ii} Z_s}{Z_{ii} - Z_s} \tag{17}$$

with Z_{ii} the output impedance of the $i \rightarrow i$ feedback network in the outer loop. Now recall that the attenuation at the source equals $\alpha_s = Z_{ii}/(Z_{ii} + Z_s)$. Substituting this in (17) yields

$$\beta_{vi} = \beta_{ii} Z_s \frac{\alpha_s}{2\alpha_s - 1} \text{or} L_{outer} = L_{inner}(2\alpha_s - 1). \tag{18}$$

When the output impedance of the outer feedback loop is negligible with respect to the source impedance ($\alpha_s \approx 1$), the inner loop gain is approximately equal to the outer loop gain. Under the impedance matched condition, the total loop gain is now found as

$$L = A'\beta_{eff} = 2\alpha_s L_{inner} \approx 2L_{inner}. \tag{19}$$

Eqs (18) and (19) hold for all [V,I]-to-current and [V,I]-to-voltage amplifiers, while replacing α_s by α_l gives the two relations for all voltage- or current-to-[V,I] amplifiers.

When the asymptotic input impedance of the [V,I]→I amplifier equals the source impedance, Eq. (18) can be substituted into Eq. (8), which gives $\beta_{eff} = 2\beta_{vi}\alpha_s$. Irrespective of the double-loop feedback amplifier topology, this relation can be generalized to

$$\beta_{eff} = 2\beta_{inner}\alpha_{s,l} \tag{20}$$

where α_s has to be used when considering a characteristic input impedance and α_l in case of a characteristic output impedance. This simplifies the asymptotic transfer Eq. (10) to

$$A_{t\infty} = -\frac{1}{2\beta_{inner}} \tag{21}$$

assuming the attenuation at the non-characteristic port is unity.

This result is not a surprise (see also the last column in Table III), because a source impedance matched double-loop feedback amplifier will have exactly half the source voltage across its input terminals, while the inner feedback loop defines the relation between this input voltage and the output quantity. Likewise, a load impedance matched amplifier will generate exactly half its output Thévenin voltage or Norton current at the load, while the inner feedback loop defines the relation between this Thévenin voltage/Norton current and the input quantity.

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6. EXAMPLE OF DOUBLE-LOOP SYNTHESIS MODEL AND ITS APPLICATION

To demonstrate the application of the developed double-loop synthesis model, a design example of a double-loop feedback amplifier is given here. Arbitrarily, an amplifier is chosen with a characteristic input impedance of $Z_{char,in} = 50\ \Omega$ and a voltage output, that is, a [V,I]→V amplifier. The voltage gain $|A_v| = |v_l/v_s|$ is 10. The source impedance is $R_s = 50\ \Omega$; the load impedance equals $R_l//C_l = 10\ \text{k}\Omega//200\ \text{fF}$. The signal frequency band is from 1 to 10 GHz.

The corresponding synthesis model is depicted in Figure 15, where, to start with, the voltage-to-voltage feedback network β_{vv} has been placed in the inner feedback path and the voltage-to-current network β_{iv} in the outer feedback path. Considering the relatively low $Z_{char,in}$, it is likely that, because of the finite, non-zero output impedances of the feedback networks ($Z_{o,iv}$ and $Z_{o,vv}$ resp.), $Z_{char,in}$ will be degraded more by a series connected outer network than by a *parallel* connected outer network at the amplifier input (Section 5.3). This choice will be re-assessed in step 3 of Section 6.1. This synthesis model is used now as *design target* for the double-loop feedback amplifier.

After the source and load signal quantities have been identified and assigned to the branches in the model, the synthesis of the feedback amplifier consists of two parts: the design of the asymptotic behavior and the design of the nullor approximation. In the following two sections, they will be dealt with to an extend that is relevant for the topic of double-loop feedback amplifiers.

6.1. Design of the asymptotic behavior

The design of the asymptotic behavior consists of three consecutive design steps:

(i) design of the amplifier topology;
(ii) design of the feedback networks; and
(iii) design of the asymptotic error terms.

Hereafter, they will be discussed in this order.

6.1.1. Design of the amplifier topology: hook-up of the feedback networks. The first step in the design of the asymptotic behavior of the amplifier is to correctly hook-up the two feedback networks to the active part, source, and load. According to the synthesis model, both β_{vv} and β_{iv} networks need to sense the load voltage ($\alpha_l = 1$ at this stage), which implies they have to be connected in parallel to the load, while they have to add to the input signal in voltage and current respectively, requiring a series respectively parallel connection to the source.

6.1.2. Design of the feedback networks: β_{vv} and β_{iv}. The second step is the design of the first two asymptotic blocks β_{vv}, β_{iv}, while assuming that the two other—two error terms α_s and α_l—are still at

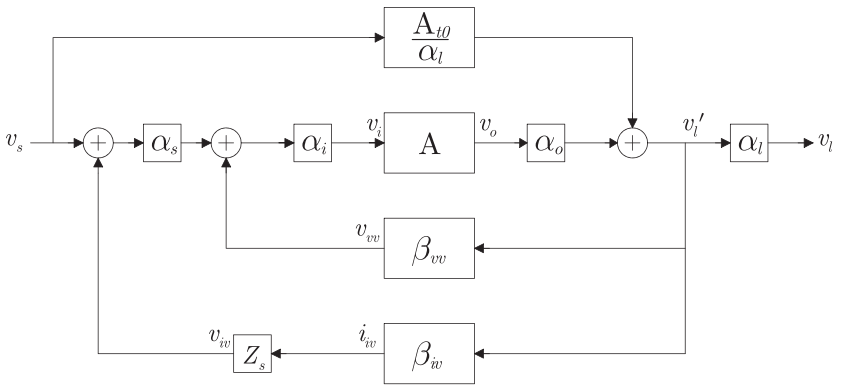

Figure 15. Synthesis model of a [V,I]-to-voltage amplifier with the voltage-to-voltage feedback network in the inner feedback path.

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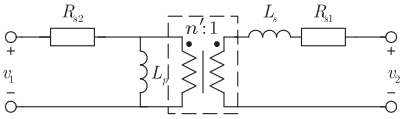

$$\begin{bmatrix} A_{fb} & B_{fb} \\ C_{fb} & D_{fb} \end{bmatrix} = \begin{bmatrix} n' \frac{R_{s1}+sL_p}{sL_p} & B_{fb} \\ C_{fb} & D_{fb} \end{bmatrix}$$

$L_1 = 4.3$ nH	$k = 0.19$
$L_2 = 0.3$ nH	$n' = 20$
$R_{s1} = 1.6\ \Omega$	
$R_{s2} = 4.4\ \Omega$	

Figure 16. Model of a pair of coupled inductors L_1 and L_2 with coupling factor k, where $L_p = L_1$, $L_s = L_2(1-k^2)$, and $n' = \frac{1}{k}\sqrt{L_1/L_2}$. This transformer is used as example voltage feedback network, because it is closest to the optimal non-energic and linear ideal transformer [4] (located inside the dashed box).

their target value 1 at this stage. The asymptotic input impedance $Z_{t\infty}$ now equals the ratio of the two feedback network transfers (Section 5.3), viz.,

$$Z_{t\infty} = \frac{\beta_{vv}}{\beta_{iv}} = Z_{char,in}, \tag{22}$$

and the asymptotic transfer $A_{t\infty}$ (voltage gain) is readily found from the synthesis model in Figure 15 as

$$A_{t\infty} = \frac{v_l}{v_s}\bigg|_{A\to\infty} = -\frac{\alpha_s\alpha_l}{\beta_{eff}} = -\frac{\alpha_s\alpha_l}{\beta_{vv}+\beta_{iv}Z_s\alpha_s} = -\frac{1}{2\beta_{vv}} \tag{23}$$

assuming a matched input impedance $Z_{char,in} = Z_s$, as required. Together with Eq. (22) and $|A_v| = 10$, this leads to $\beta_{vv} = 1/20$ and β_{iv} =1 mS.

Ideally, the feedback networks need to be accurate, linear, and non-energic,[‖] like an ideal transformer and gyrator. For this conceptual example, the closest practical approximations of them are selected, which are still linear and accurate: A pair of coupled inductors[**] for β_{vv}, of which a 1^{st}-order model, associated model parameters and voltage transfer $1/A_{fb}$ are given in Figure 16, and a resistor R_f for β_{iv}. This results in a required effective voltage attenuation of the transformer of $n' = 1/\beta_{vv} = 20$ and a feedback resistor value of $R_f = 1/\beta_{iv} = 1$ kΩ.

6.1.3. Design of the asymptotic error terms: source and load attenuation α_s and α_l. Source attenuation α_s—one of the two error terms in the asymptotic behavior—has to be made unity to make sure that neither $A_{t\infty}$ nor $Z_{t\infty}$ is negatively affected, as already pointed out at the end of Section 5. Given the chosen feedback network implementations and loop order, this can only be achieved by adding an ideal current follower at the output of the β_{iv} network. To prevent the additional complexity, it is decided to omit this follower. As a consequence, the non-ideal output impedance of the outer feedback network $Z_{o,iv} = R_f$ causes α_s to be smaller than 1:

$$\alpha_s = \frac{Z_{o,iv}}{Z_{o,iv}+R_s} = \frac{R_f}{R_f+R_s} = 0.95. \tag{24}$$

Now that the feedback networks have been implemented, the currently selected loop order has to be re-evaluated to see if it indeed leads to a value of α_s closest to 1. With the β_{iv} network in the outer loop, the voltage attenuation at the source is 0.95 as given by Eq. (24). If the loops were exchanged, α_s would become a current attenuation factor that equals

$$\alpha_s = \frac{R_s}{R_s+R_{s2}+sL_s+(R_{s1}//sL_p)/n'^2} \approx \frac{R_s}{R_s+R_{s2}+sL_s}, \tag{25}$$

the magnitude of which, given the transformer model parameters listed in Figure 16, varies between 0.87 and 0.92 over the specified frequency band. The initially chosen loop order results in the smallest aggravation of $A_{t\infty}$ and $Z_{t\infty}$, and hence, it is the optimal order of the feedback loops. On top of this,

[‖] Non-energic implies that the noise performance and power efficiency are not degraded by these networks [1].

[**] If concessions have to be made to silicon area, a smaller implementation like resistive or active feedback may be required with an inherent reduction in noise and/or linearity performance of the amplifier as a consequence.

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because α_s is frequency independent, it is possible to compensate for its impact on $Z_{t\infty}$ by just increasing the feedback resistor to 1.05 kΩ:

$$Z_{t\infty} = \frac{\beta_{vv}}{\beta_{iv}} // R_f = \frac{R_f}{n'} // R_f = R_s \Leftrightarrow R_f = R_s(n'+1) = 1.05\ \text{k}\Omega. \tag{26}$$

What load attenuation α_l is concerned, there is no reason to make it smaller than 1 at this stage of the design. A non-unity value makes $A_{t\infty}$ depend on the (often inaccurate) load impedance, which is undesired.

Now the feedback topology as well as all transfers of the asymptotic blocks have been designed, the final asymptotic gain and input impedance equations can be found as

$$A_{t\infty} = \frac{v_l}{v_s} = -\frac{\alpha_s \alpha_l}{\beta_{eff}} = -\frac{\alpha_s \alpha_l}{\beta_{vv} + \beta_{iv} Z_s \alpha_s} = -\frac{n'}{2} \cdot \frac{1 + sL_p/R_{s1}}{n'/(2n'+2) + sL_p/R_{s1}} \overset{\omega \gg R_{s1}/L_p}{\approx} -\frac{n'}{2} \tag{27}$$

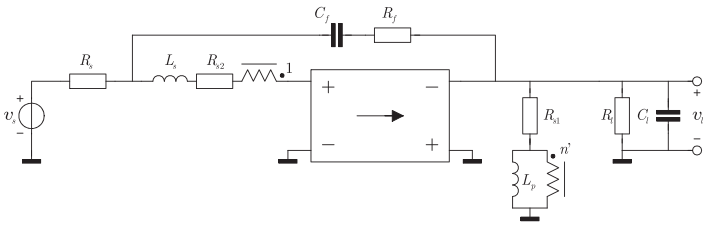
$$Z_{t\infty} = \frac{\beta_{vv}}{\beta_{iv}} // R_f = \frac{R_f}{n'+1} \cdot \frac{sL_p/R_{s1}}{n'/(n'+1) + sL_p/R_{s1}} \overset{\omega \gg R_{s1}/L_p}{\approx} \frac{R_f}{n'+1}. \tag{28}$$

The pole L_p/R_{s1} in $Z_{t\infty}$ can be canceled with a zero in R_f by placing a small capacitor $C_f = \frac{1}{n' R_s} \frac{L_p}{R_{s1}} =$ 2.7 pF in series with R_f.

At this stage, the asymptotic behavior of the amplifier has been design. The aforementioned design steps have led to the amplifier schematic shown in Figure 17.

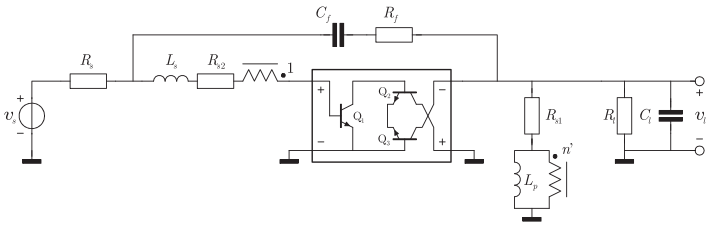
6.2. *Design of the nullor approximation*

What remains to be designed is the implementation of the nullor approximation—the active part—which basically involves the design of A, α_i, and α_o. Most design steps are not different from single-loop feedback amplifiers, apart from one: the design of phantom zeroes as frequency compensation method. For this reason, the implementation of the active part is assumed to be given (Figure 18), so that the focus can be on the phantom zero compensation.[††]



$R_s = 50\ \Omega$	$L_1 = 4.3$ nH
$R_l = 10$ kΩ	$L_2 = 0.3$ nH
$C_l = 200$ fF	$k = 0.19$
	$L_p = 4.3$ nH
$n' = 20$	$L_s = 0.29$ nH
$R_f = 1.05$ kΩ	$R_{s1} = 1.6\ \Omega$
$C_f = 2.7$ pF	$R_{s2} = 4.4\ \Omega$

Figure 17. Schematic diagram of the transformer feedback [V,I]-to-voltage amplifier that fully defines its asymptotic behavior.



Q_1	Q_2, Q_3
$I_c = 10$ mA	$I_c = 5$ mA
$L_e = 5\ \mu$m	$L_e = 5\ \mu$m
$W_e = 0.12\ \mu$m	$W_e = 0.12\ \mu$m
mult = 10	mult = 10

Figure 18. Schematic diagram of the transformer feedback [V,I]-to-voltage amplifier with the small-signal implementation of the active part.

[††]Phantom zero compensation is chosen here as frequency compensation technique, because it does not reduce the loop gain at higher frequencies, as opposed to pole-splitting (Miller compensation), resistive board-banding, and dominant pole compensation. Hence, it does not (significantly) degrade the input impedance or linearity [18].

DOI: 10.1002/cta

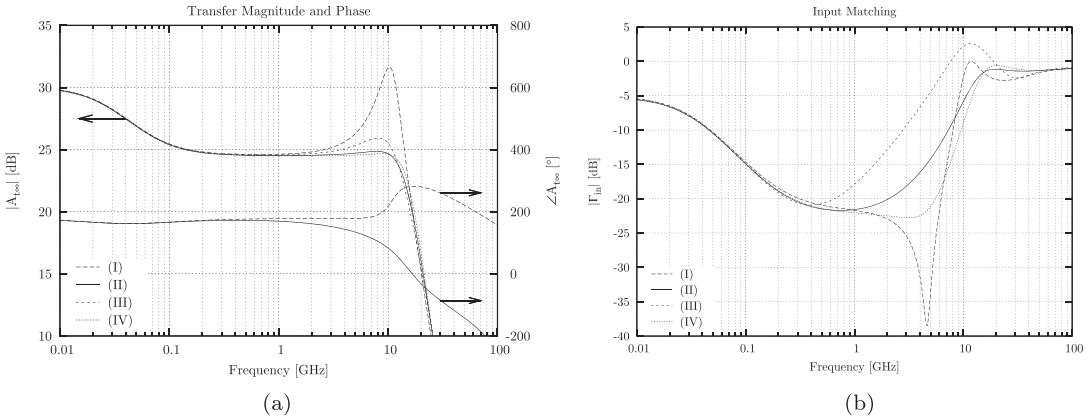


Figure 19. Simulated small-signal behavior: transfer magnitude and phase (a) and input matching (b). Legend: (I) no frequency compensation, (II) phantom zero in both feedback networks, (III) phantom zero in outer network only, and (IV) phantom zero in both feedback networks, but skewed to compensate for the high-frequency roll-off of the loop gain.

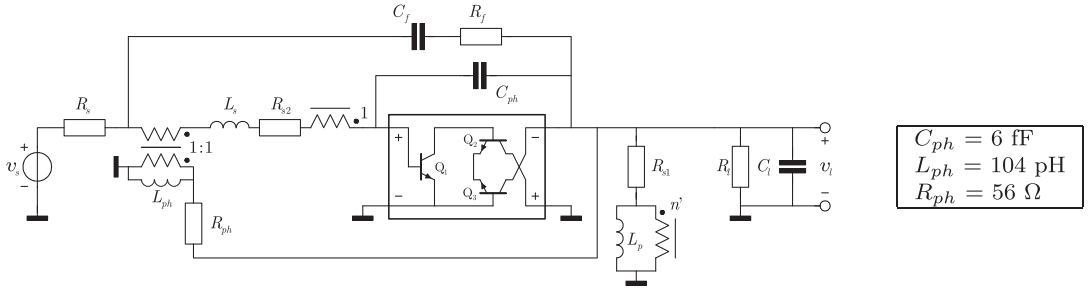


Figure 20. Schematic diagram of the complete transformer feedback [V,I]-to-voltage amplifier including the phantom-zero implementation corresponding to trace (IV) of Figure 19. In practice, the phantom-zero transformer can be combined with the main feedback transformer without any area penalty.

Trace (I) in Figure 19 shows the transfer magnitude[‡‡] and phase (a) and the input matching (b) of the uncompensated amplifier: It is clearly unstable. From a pole-zero analysis, it is found that a phantom zero at 10.5 GHz is required to get a maximally flat magnitude response. From the synthesis model in Figure 15, it becomes immediately clear that a phantom zero in the feedback path has to be implemented in *both* feedback networks, because only then will a zero be present in $\beta_{eff} = \beta_{vv} + \beta_{iv} Z_s \alpha_s$ and will $Z_{t\infty} \approx \beta_{vv}/\beta_{iv}$ be unaffected. Trace (II) in Figure 19(a) and (b) is the result of the frequency compensated amplifier.

If a zero was placed in only one of the two networks, the other loop would bypass this zero and, given the fact that $\beta_{vv} \approx \beta_{iv} Z_s \alpha_s$, shift it to a two times higher frequency, making it two times less effective. On top of this, a pole or zero becomes apparent in $Z_{t\infty} \approx \beta_{vv}/\beta_{iv}$, which degrades the input matching significantly. This is clearly observed in Figure 19(a) and (b) trace (III).

With a zero present in both β_{vv} and β_{iv}, it is possible to deliberately shift the resulting pole and zero in $Z_{t\infty}$ apart, such that the increase or decrease of $Z_{t\infty}$ due to the frequency roll-off of the loop gain can be (partly) counteracted, while maintaining the zero location in β_{eff}. The result is shown in trace (IV), where the maximum frequency for which the input matching is better than -10 dB has moved up from 7.3 to 9.5 GHz.

In general, a phantom zero can also be implemented by adding a pole in α_s or α_l. A pole in α_s (i.e., at the characteristic side of the amplifier) will deteriorate $Z_{t\infty}$ in a similar way as having phantom

[‡‡]Notice that the transfer magnitude is 1.5 dB less than the expected 26 dB. This is because the mid-band loop-gain magnitude is no more than 5.3 dB, which results in an error (Eq. (9)) in the transfer of $20\log[5.8/(1+5.8)] = -1.5$ dB.

DOI: 10.1002/cta

zero implemented in only one feedback network. And a pole in α_l (i.e., at the non-characteristic side) will bring the attenuation further away from unity. Hence, a phantom zero implementation in the two feedback paths is strongly preferred.

The resulting circuit schematic is depicted in Figure 20, where the phantom zero component values are given in the table.

7. CONCLUSION

A new synthesis-oriented feedback model has been derived that is suitable for the full synthesis of single-loop feedback amplifiers. It directly maps to the circuit level of feedback amplifiers: The individual model elements, each representing an important design aspect, can be assigned to specific sections of the circuit. The model not only visualizes the hierarchy in the design process but also points to fundamental design criteria, both key for the process of full synthesis.

Based on this model, a synthesis-oriented double-loop feedback model has been developed, which describes the two feedback loops explicitly and enables the full synthesis of double-loop feedback amplifiers in a structured and systematic way. It models the errors made by non-ideal feedback networks, which creates the path to additional design criteria that are specific for double-loop feedback amplifiers. With this model, the relations between the loop gain and the gains of the two individual loops are easily found, as well as the relation between the feedback network characteristics and the characteristic input or output impedance of the amplifier.

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DOI: 10.1002/cta