Bsc Thesis - Powerline Communication

Distribution of the electricity grid of a tiny house community

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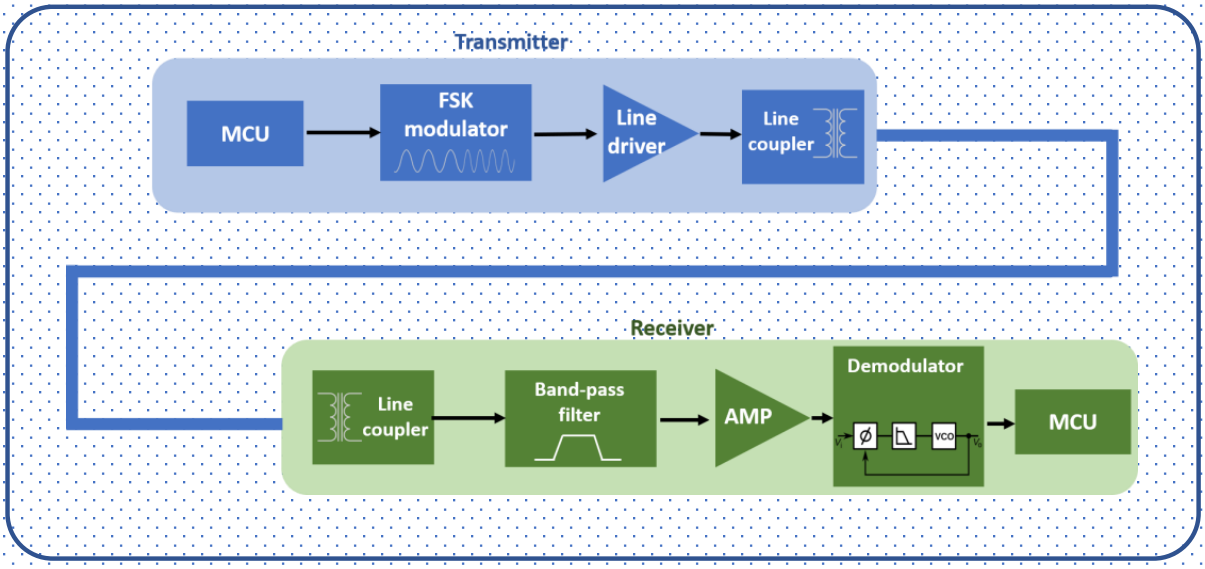

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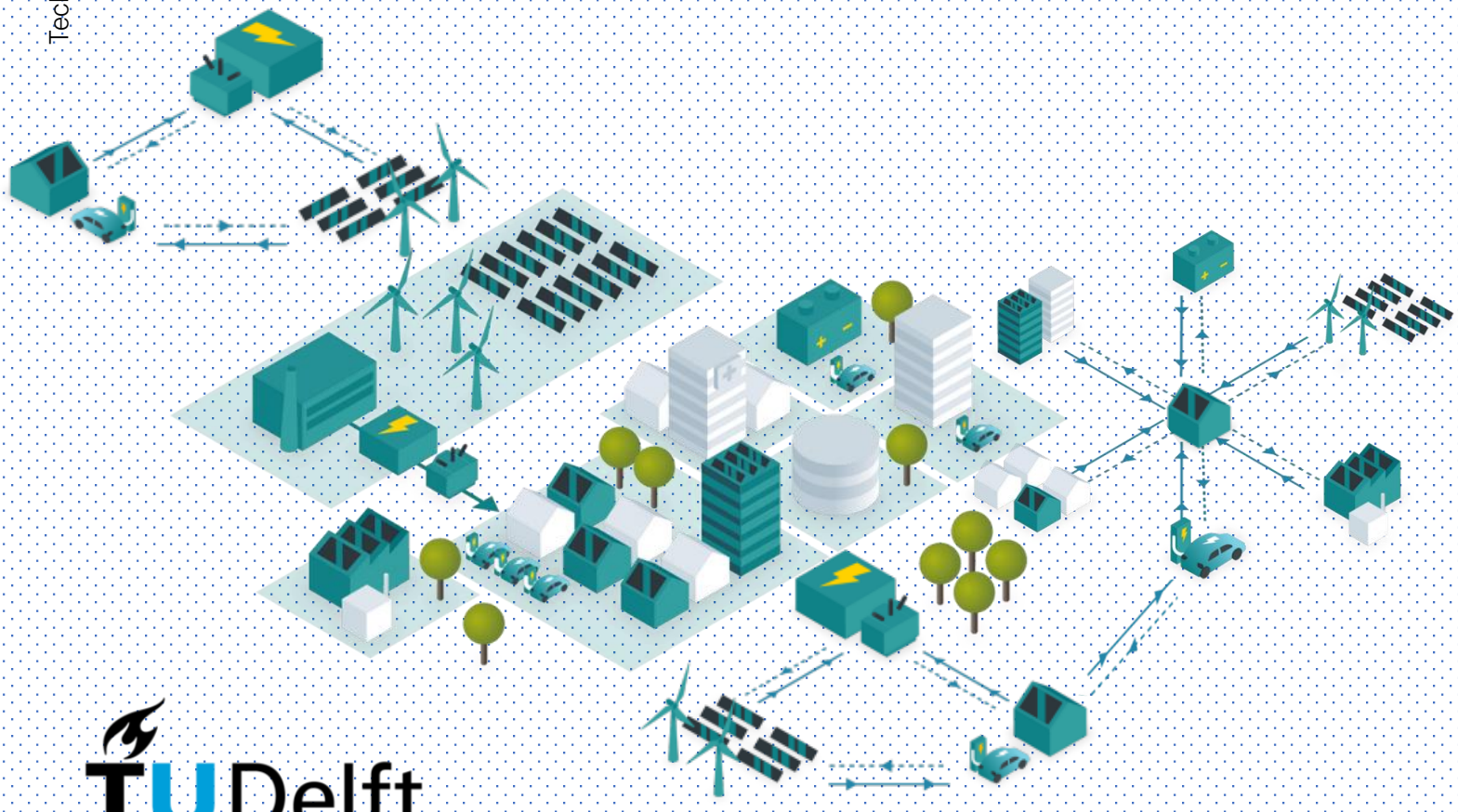

TU Delft

Distribution of the electricity grid of a tiny house community

Power line communication

by

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Preface

This thesis is written in the context of the bachelor graduation project of Electrical Engineering at the Delft University of Technology. With climate change being a more pressing matter than ever, many people are looking for ways to minimize their ecological footprint. One of the most effective ways for an individual to reduce their impact on the environment is by sustainable living. In the last two decades sustainable housing has been gaining popularity with at the forefront of the movement a concept called "tiny houses". This thesis will describe the design of a prototype powerline communication system that will enable communication within the DC energy grid of a tiny house community. Together with the control software and DC grid design created by our colleagues the communication systems will be able to transfer important control data to grid devices and houses to increase the energy efficiency.

We would like to express our gratitude to our supervisors Dr. Sijun Du and Dr. Pedro Vergara Barrios for their guidance during the project. Furthermore, we would like to thank Martin Schumacher and Ton Slats from the Tellegenhal staff for their help with the setup of the measurement equipment. Finally, we would like to thank our colleagues: Paul Kluge, Jesse Richter, Aart Rozendaal and Pieter van Santvliet for an enjoyable and productive collaboration.

Imad Bellouki, Luuk Pijnenburg
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Abstract

This thesis will discuss the design, simulations and measurements of a powerline communication system that utilizes FSK modulation in order to transfer information from a transmitter to a receiver at a baud rate of 1kbps, in order to reach the requirement of having an effective data rate of at least 6bps. This system is designed specifically to be implemented in the smart DC grid of a sustainable "tiny house" community. This thesis investigates the different subsystems needed to create this communication system and compares different methods and implementations. This research led to the conclusion that the communication system was successfully build and could reliably reach a baud rate of 700bps, which appeared to be more than enough to reach a data rate of 6bps. The system also showed to be resistant to 'high levels' of noise on the communication channel as defined in the CELENEC standard. Furthermore, in order to decrease the bit error rate further, additional bit error detection and correction has been implemented using microcontrollers. This led to a robust and nearly error free communication system over a tested powerline of 50 meters long.

Contents

1 Introduction

With the growing need of more sustainable housing in the world, a lot of different innovative solutions have already been tested and implemented with the goal to achieve the highest possible energy efficiency. One of the key components recent green housing projects around the world have in common is a "smart energy grid". Here, the term smart means that there is some form of data communication between different houses or between some other central computer that is able to control the energy flow to achieve higher efficiency. This field concerns itself the most with low speed communication on an AC grid, here however a system will be designed to be operated on a DC grid in this thesis.
This bachelor thesis will discuss the design of the communication system responsible for transferring important information within a "tiny house community" [1]. This housing community will consist of 12 small houses that will be connected to a central control system that will be designed by another subgroup that will handle the correct and most efficient transfer of power inside the DC grid. The central control system is placed in a common building to all tiny house residents where also larger house appliances are located. The DC grid itself will be designed by another subgroup of this bachelor graduation project. The average distances that these powerlines span between the houses and different appliances will be a few hundred meters at most.
The information that will be transferred over the communication channel (powerlines) consists of the control and status information of different energy storage and generation devices, such as batteries and windmills.
The communication system is placed at each house and will only transfer the information from and to the central control system every hour for this prototype. However, for future implementations the transfer frequency is higher, so the aim for this project will be to provide information speeds enough to update every 5 minutes. This information consist of the amount of generated energy and the house energy demand in kWh. This information is measured by a meter that is installed in the house and sends this information to the microcontroller (MCU) that handles the communication.
Another important part of the information that is being sent is the "control level". This part of the signal represents a value between 0 and 4 which indicates a certain control level to which receivers in the system act upon and adjust their power usage. A detailed description of all communication signals that are being sent and the implemented communication protocol are described in appendix B.1.
For the communication channel of the system the existing DC powerlines in the grid are chosen to carry the information from transmitter to receiver. This method of transferring information is also called powerline communication (PLC). This method of transferring the information in the DC grid has advantages over other option for the use in the tiny house community. The first advantages of the PLC implementation over other communication channels based on wireless transfer such as WiFi or cellular data networks is that there is no need to place addition wireless access points between the house and grid appliances when using WiFi as communication. The housing communities this product aims for can also be located in more rural or developing areas where cellular networks are not sufficiently and reliably covered. The communication through the power lines will result here in a more reliable system, since even when there might be a power outage in the DC grid the PLC will still be able to transfer information through the channel (if back-up power for the transceivers is present of course).
The system was designed, built and tested accordingly. The final PLC system functions as intended and a reliable baud rate of 600bps was achieved with a very low bit error rate (BER) using Manchester encoding for the communication protocol. Adding more noise to the channel to achieve a worst case scenario showed no increased BER and the system would still be able to reliably communicate.

2

PLC system architecture & requirements

Within this project, the PLC system will form the bridge between the control and DC grid subgroups. The size of the messages and the frequency of transmission is set by the needs of the control subgroup. Other grid related requirements that are of importance to the PLC system are set by the DC grid subgroup. These requirements consist of the amount of transceivers needed in the grid (the amount of addresses needed), the requirements on the allowable disturbance levels on the powerline and the powerline length. This chapter will describe a top-level overview of the PLC system that will be designed and built. First, a brief overview is given of the top-level system, then the requirements of the complete system and the subsystems are listed in a program of requirements. In the next chapter, the implementation of the different subsystems is discussed.

2.1. Subsystem overview

The PLC system is divided into 3 separate parts, these being the transmitter, receiver and the low voltage DC (LVDC) powerline. In figure 2.1 the proposed architecture of the system is shown. Both transmitter and receiver sides utilize a MCU that is responsible for sending the received digital data from the central control unit to the modulator. The MCU that will be used is the ESP8266.

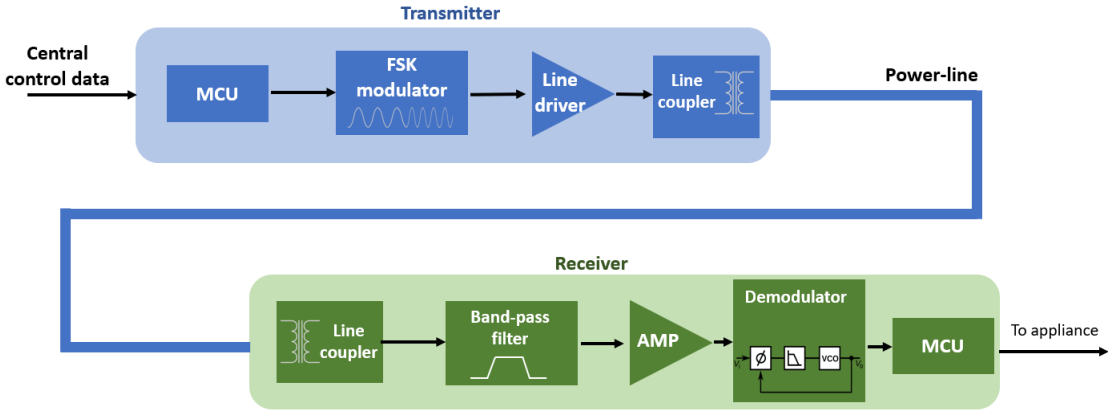

Figure 2.1: Schematic description of the proposed PLC system.

2.1.1. Transmitter side

The transmitter consists of a MCU, modulator, line driver and line coupler. The functionality of the MCU is already discussed in the section above. The modulator is responsible to transform the binary signal into a information carrying analog signal that will be reliably sent over the powerline. Here, it is important for the modulation frequency to be chosen such that it is less susceptible to noise and interference which it gets introduced to in the other circuits and in the powerline.
The line driver has to increase the current driving capabilities of the modulated signal such that it will increase the available power for the modulated signal. This is needed to drive the communication signal over the long powerline. The line coupler has some maximum input/output ratings that should be considered. The line coupler at both the receiver and transmitter side are reciprocal. It should offer galvanic isolation from the powerline and superimposes the information carrying signal on top of the 400V DC voltage of the powerline.

2.1.2. Receiver side

The receiver side consists of a line coupler, a band-pass filter (BPF), an amplifier, a demodulator and a MCU. The MCU and line coupler here are the same as at the transmitter side. The BPF is responsible to filter most out of band noise and disturbances in order to increase the signal-to-noise ratio (SNR) of the signal.
An amplifier stage might be needed to amplify the voltage of the filtered signal such that the signal level is within the input voltage specification of the demodulator. The demodulator is responsible for retrieving the original data from the modulated signal.

2.1.3. Powerline

For this system a LVDC powerline acts as the communication channel, the length of this cable for a first prototype is set to be 50 meters. Next to the cable, the communication channel also consists of a 50 Ω load and a voltage source of 400V DC. Because of limitations in resources however, most of the testing will be conducted using a 30V DC source.

2.2. Methodology

The design and simulations of the different subsystems will be done separately first in LTspice. Here, the separate subsystems will be designed and their behaviour validated. Noise and tolerance analysis are performed for each of the subsystems, these results and conclusions can be found in appendix A. Besides the receiver and transmitter parts of the system, the powerline will also be modelled in LTspice which is used to optimize the design. After the design process of each subsystem is completed the circuits are build and tested on their specific parameters, such as total harmonic distortion on the oscillator sine waves and the frequency response in case of the band pass filter to name a few.

2.3. Program of requirements

This section will list all the requirements that were set up at the start of the project. The requirements form the backbone of the design process and are an important measure to asses the final product. The validation of each of these requirements are listed in appendix E.

2.3.1. system requirements

The following subsection will discuss the top-level system requirements of the self proposed Bachelor Graduation Project 'Distribution of the electricity grid of a tiny house community'. The MoSCoW method[10] will be used to prioritize requirements. The method involves dividing requirements into 'Must have', 'Should have', 'Could have' and 'Won't have'. 'Must haves' are essential requirements (primary). 'Should haves' are secondary and will be done after primary requirements are achieved. 'Could haves' are nice to have (tertiary/bonus requirements). 'Won't haves' are beyond the scope of the project and will not be implemented.

2.3.1.1. Functional requirements

Must have

- **RQ-M.SYS.1:** The system must use the designed DC grid, where information will be sent to the Control and Software subsystem (CNS) using the designed Power Line Communication (PLC).
- **RQ-M.SYS.2:** The system must be able to supply the 12 tiny houses and the common usage of TUNECT[1].
- **RQ-M.SYS.3:** The system must use renewable energy sources as supply units only.
- **RQ-M.SYS.4:** The system should have an availability of at least 90%.
- **RQ-M.SYS.5:** The system must be able to do forecasting based on the users behaviour and the weather.
- **RQ-M.SYS.6:** The system must be able to communicate grid information over the powerlines, using a powerline communication system.

Should have

- **RQ-S.SYS.1:** The system should be designed such that the costs are minimized for the given functional requirements.
- **RQ-S.SYS.2:** The system should be designed such that the efficiency is optimized.

Could have

- **RQ-C.SYS.1:** The system could be designed to operate in islanded mode for all of the time.

2.3.1.2. Non-functional requirements

Below, all non-functional requirements of the top level system will be given. They describe how the system should operate.

- **RQ-NF.SYS.1:** The minimum speed of the powerline communication system should be such that it can sustain a transfer that is fast enough such that all data can be delivered to the devices within a timely manner.

2.3.2. Powerline communication

The following subsection will deal with the specific requirements for the powerline communication subsystem.

2.3.2.1. Functional requirements

Must have

- **RQ-M.PLC.1:** The system must consist out of a separate receiver and transmitter module connected to a powerline.
  The information is carried over a powerline using a receiver-transmitter system.
- **RQ-M.PLC.2:** The system must establish reliable communication over distances specified in RQ-NF1.
  The system must provide reliable communication over at least the distance from the main control to the furthest receiver. Reliable is defined in telecommunications as an eventual bit error rate (BER) that is smaller than 10^{-9}.
- **RQ-M.PLC.3:** The system must superimpose the information carrying signal onto a LVDC powerline.
  The information signal will be converted from a digital signal into a small analog signal, the system then needs to be able to superimpose this signal on the LVDC powerline in order to transfer the information to the receiver.
- **RQ-M.PLC.4:** The receiver must be able to extract the information carrying signal from the LVDC powerline.
  The receiver must be coupled to the line such that it only transfers the information carrying signal and filters out the DC power component of the powerline.
- **RQ-M.PLC.5:**The SNR of the signal at the receiver side must be larger than unity for the required distance in order to correctly retrieve the data.
  In order to extract the information signal back from the powerline without implementing correlation the transmitter must be designed such that the SNR at the receiver is larger than unity.
  The system must have a line driver that is able to increase the available power of the information carrying signal.
- **RQ-M.PLC.6:** The system must use a form of FSK as a modulation technique.
  FSK is a modulation technique that shows the best performance and it is feasible to implement for this project, as is explained in chapter 3.1.

Should have

- **RQ-S.PLC.1:** The band-pass filter should be implemented as an active filter.
  A more accurate and reliable filter is desired and a possible pass-band amplification is needed in any case.
- **RQ-S.PLC.2:** A protection circuit to protect against voltage and current surges is desired.
  The line coupler, that couples both the receiver and transmitter to the powerline, should contain a protection circuit to protect against voltage and current transients in the DC grid, that can harm the other electronics.
- **RQ-S.PLC.3:** A PCB should be designed to implement the final design of the system.
  In order to improve the system even further and conduct proper testing a PCB should be designed and fabricated in time.

Could have

- **RQ-C.PLC.1:** The system could have automatic gain control (AGC) to work over a wider range of distances.
  Different path lengths can result in different signal levels which could be dynamically compensated for.
- **RQ-C.PLC.2:** The system could be designed to transfer information over DC-converters.
  The system could have extra hardware to overcome the boundary that DC-converters impose for the information carrying signal.

- **RQ-C.PLC.3:** The system should implement a Gaussian filter to achieve a higher spectral efficiency.
  Better spectral efficiency is desired in order to limit the power and decrease the required bandwidth, a Gaussian filter should be added to achieve this.

Won't have

- **RQ-W.PLC.1:** The final built system will not be bidirectional.
  Due to limited time and resources the built system will not be bidirectional. Also, from a testing perspective this wouldn't add any advantage.
- **RQ-W.PLC.2:** The system won't have a separate power supply and will be powered from the MCU that controls a subpart of the GRID.
  Every subpart where communication is required already contains an MCU to control the subsystem. The PLC system can be added to this system and should thus be able to get powered from this MCU.
- **RQ-W.PLC.3:**
  The system won't implement MSK to achieve a higher spectral efficiency.
  MSK is a special form of FSK with a lower spectral density. However, due to its difficult implementation this technique won't be implemented.

2.3.2.2. Non-functional requirements

The non-functional requirements will describe the boundaries that the powerline communication system will be designed around. They are as measurable as possible and facilitate as a reference guide for testing.

- **RQ-NF.PLC.1:** The system must be able to communicate over a range from 0 meters to at least 50 meters.
  The order of the length that the tiny houses should span between the different energy systems and such is around 100 meters. In order to build a practical test setup a length of 50 meters seems sufficient.
- **RQ-NF.PLC.2:** The band of the used frequencies for the communication should lie in the A or B band of the CENELEC standard[16], this band covers the 3kHz - 95 kHz range and 95-125 kHz respectively.
  The A band is the most suitable option since this band is reserved for energy providers and their concession holders. The B band is reserved for customers of energy providers. There is no access protocol defined for the bands. Therefore, it is less suitable to use but the higher frequencies may prove useful if a higher baudrate is really needed.
- **RQ-NF.PLC.3:** The maximum transmission voltage level of the information carrying signal can't exceed 120 dBμV and 116 dBμV for the A and B band respectively.
  These values are defined directly in the CENELEC standard and explained further in [30].
- **RQ-NF.PLC.4:** The data rate of the system should be at least 6 bits/s.
  The control of the DC grids requires 38 information packages of 40 bits to be send every 5 minutes (see Appendix B.1. This results in a minimum data rate of 6 bits per seconds.
- **RQ-NF.PLC.5:** The baud rate should be 1 kbps to provide sufficient speed to achieve the data rate specified in requirement RQ-NF.PLC.4
  The system will aim to provide the highest possible baud rate, in order to provide very reliable communication where extra bits can be used for, for example, error detection and correction and synchronization, this baudrate is limited by choice of carrier and modulation frequencies and the SNR.
- **RQ-NF.PLC.6:** The system must be able to function on a DC grid with a voltage of 400V.
  The voltage on the DC grid is managed by the other subgroup (grid design) and it is given that it will be 400V.
- **RQ-NF.PLC.7:** The supply voltage of the system is 5 volts.
  The supply voltage of the system is based on the supply voltage of the MCU, since most MCU have a operating voltage of 5V.
- **RQ-NF.PLC.8:** The maximum power for both the receiver and the transmitter should not exceed 1W.
  This is the maximum that the ESP8266 MCU can deliver from it's on board 5V power supply.

3
Implementation

This chapter will discuss the theory, design, simulations, considerations and measurements of the different subsystems of the PLC system.

3.1. Modulator

3.1.1. Modulation technique and parameters

The communication signal that the system will provide on the DC powerline needs to be generated, for this, several different modulation techniques exist. The modulation techniques that were considered were:

1. ASK (Amplitude-shift keying)
2. FSK (Frequency-shift keying)
3. PSK (Phase-shift keying)

However, more complex modulation techniques are available but these were not taken into account due to their complexity, also their increased performance is not needed to achieve the baud rate goal of this system (RQ-NF.PLC.5). A more detailed description of the 3 modulation techniques is given in [32]. The list above of the considered modulation techniques is given in the order of their implementation complexity on a system level. For ASK the most common and simple implementation is on-off keying (OOK), the following paper discusses a possible system implementation for low-speed powerline communication using OOK[31]. The main difference between implementing the PSK and FSK system lies in the complexity of their demodulation circuits, therefore FSK was preferred.

The most important consideration for choosing the modulation technique is choosing a modulation that will result in a signal that will suffer the least from noise and interference on the powerline. The following paper conducted an analysis on both ASK, FSK and PSK signals on a powerline communication smart grid [22]. The conclusion is that both PSK and FSK yield noticeable better performance compared to ASK on the effect of the added noise in the system. Since the (non-coherent) demodulation of the FSK signal is simpler than for PSK the final decision on the modulation technique for this system is FSK.

Additionally, there is another modification that can be made to the FSK modulation to increase the performance of the system, that is using a Gaussian filter (this is called GFSK). GFSK uses a Gaussian filter to 'smooth' the transition of each digital symbol before the frequency modulation, this is done to limit its spectral bandwidth. The Gaussian filtering avoids the high frequencies due to the switching, and thus reduces the signal spectral bandwidth which will reduce the adjacent channel interference [33][12].

Another method to decrease the bandwidth of the FSK modulated signal, is by using MSK. MSK is continuous-phase FSK with a minimum modulation index that will produce orthogonal signaling [14]. This essentially creates smooth transitions when the data changes sign. This will significantly reduce the high frequency distortion that the communication transmitter induces on the powerline. MSK can be combined with the aforementioned Gaussian filter to create even better bandwidth performance. This type of modulation is called GMSK.

3.1.1.1. Data rate and bandwidth

The required data rate, which is defined as the rate at which information can be transferred from one MCU to the other, is directly dependent on the control subgroup. They can decide on a minimum value for the data rate that is required to make a functional control system for the DC grid. This data rate has a minimal requirement of 6 bits per seconds but will most likely be much higher. The baud rate is a specification of the communication system, and gives states how often the provided digital signal can change signs during

transmission. The baud rate will always be higher then the data rate due to necessary bits for, for example, clock synchronization and bit error correction. The bandwidth of the signal (BW) is given by the following equation [19]:

$$BW = 2\Delta f + 2B \tag{3.1}$$

Here B is the bandwidth of the baseband signal which depends on the baud rate, and Δf the difference in frequencies for the binary signal. Using a Gaussian filter can decrease the bandwidth even more, and also creates a smoother frequency spectrum.

3.1.1.2. Carrier frequency

Because low speeds and long distances are required, a narrowband signal will be used. For communication over powerlines using narrowband signals an European standard is developed: CENELEC [16], which assigns the bands of the powerline communications to different applications (see Table 3.1). This means that the band that can be used is the A band, with frequencies from 3-95 kHz. In this band the carrier frequency is chosen at 85kHz and 90kHz to obtain the highest possible data rate. Which using equation 3.1 will result in a bandwidth of 6kHz.

Table 3.1: The different bands of the CENELEC standard with their specifications [16].

Band	**Frequency range [kHz]**	**Maximum transmission level** [dBμV]	**Maximum disturbance level** [dBμV]
A	3-95	134-120	89-75.5
B	95-125	116	75.5-65.97
C	125-140	116	75.5-65.97
D	140-148.5	116	75.5-65.97

Another factor that should be taken into account when choosing a carrier frequency is interference, for example from the DC converters. These create large disturbances at their switching frequencies. However, according to the DC subgroup these switching frequencies will be much higher than the chosen modulation frequencies. The communication should also not cause any interference for the DC appliances connected to the grid, this is achieved by staying within the boundaries set by the CENELEC standard (RQ-NF.PLC.3).

3.1.2. Design and simulation

The FSK modulator will be implemented using a oscillator from which the oscillation frequency can be changed using a digital control signal. Here three different implementation will be discussed to determine which is the best possible implementation for the system.

3.1.2.1. Astable 555 timer oscillator

A first method is to implement an oscillator for the FSK modulator using a 555 timer IC. To be more precise the 555 timer is used as an astable multivibrator that produces a very accurate square wave. This implementation is another form of a relaxation oscillator for producing square waves up to a frequency of 500kHz at a duty cycle between 50%-100%. In order to asses the capability of the astable 555 timer to use as the FSK modulator it has to produce a good (pure) sine wave at the designed frequency. In order to maintain the maximum signal power a duty cycle close to 50% is desired for the square wave output. For this reason a topology as shown in figure 3.1 is used. In order to change the frequencies between 85kHz and 90kHz the effective resistance of one of the two resistors is changed. This is done by connecting another resistor in parallel that is controlled using a BJT, which is in turn controlled by the digital data signal. The charging and discharging time of the capacitor can be approximated using equations 3.2 and 3.3.

$$t_{charge,1} = R2 \cdot C \tag{3.2}$$

$$t_{discharge,1} = R1 \cdot C \tag{3.3}$$

$$t_{charge,0} = \frac{R2 \cdot R3}{R2 + R3} \cdot C \tag{3.4}$$

When a digital signal of 0V is applied to the input R3 will conduct current and will parallel with R2 charge the capacitor and decrease the charging time (see equation 3.4), while the discharging time remains the same. This will result in a change of frequency.
For the chosen space and mark frequencies it was calculated that R1 = 2.6kΩ, R2= 2.8kΩ, R3= 22kΩ. Which resulted in a duty cycle of 48% for 85kHz and a duty cycle of 51% for 90kHz. In order to obtain a sine wave at the output, the output square wave is connected to a 3-stage RC low pass filter, also called a ladder network,

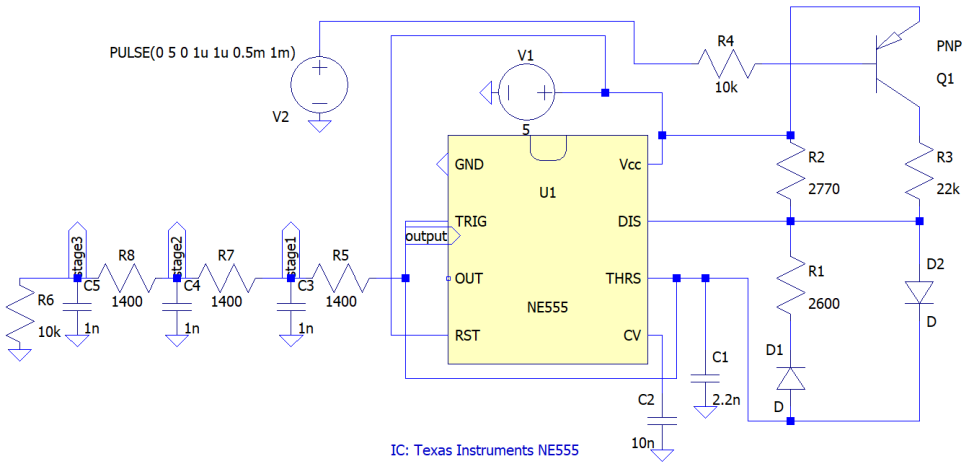

Figure 3.1: The final astable 555-timer implementing a close to 50% duty cycle for a FSK modulator.

each with a cut-off frequency of 113kHz. Because of the semiconductor components, the simulated wave forms did not met the expectations. Tuning the values was needed in order for the circuit to behave according to the requirements as much as possible, the results are shown in figure 3.2. The frequency spectrum of the sine output showed an oscillation frequency of 86kHz and 92kHz (see Figure 3.2). However, the duty cycle of the square wave is approximately 65%. These resulting values were ,however, the best possible performance that could be achieved. Although this method seems to give quite accurate results the use of the nonlinear BJT would result in too much uncertainties when building the system. Also, when looking at the frequency spectrum it can be seen that the SNR at the output is quite low, in the range of 20dB.

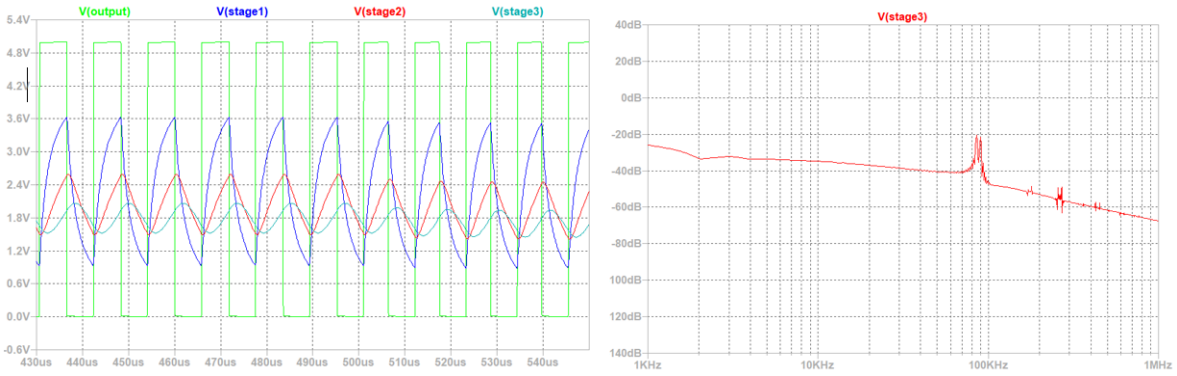

Figure 3.2: Left: The resulting waveform and the different output stages of the FSK modulator, directly at the output wave of the 555 timer and the 3 intermediate stages of the low-pass filters. Right: the FFT of the output of the FSK modulator using the 555 timer.

3.1.2.2. Crystal oscillators

In modern circuit design the use of a piezoelectric crystal in order to generate (high frequency) sinusoidal signal is common practice. A crystal oscillator operates on the inverse piezoelectric effect, where an alternating voltage is applied across the crystal surface causes it to vibrate at its natural frequency. The mechanical vibrations eventually get converted into the desired oscillations. This means that the oscillation frequency of the oscillator is determined during the fabrication process, since it is completely determined by the physical dimensions of the Crystal (and the material). The crystal is mounted between 2 parallel plates and the crystal can be modelled as a series RLC circuit shown in figure 3.3. Due to the parallel connected capacitance of the parallel plates the crystal resonates at a series resonance frequency f_s and a parallel resonance frequency f_p (see Equations 3.5 and 3.6).

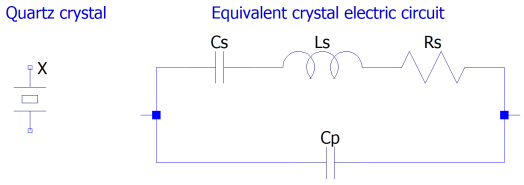

Figure 3.3: Equivalent circuit of a quartz crystal.

$$f_s = \frac{1}{2\pi\sqrt{(L_s C_s)}} \tag{3.5}$$

$$f_s = \frac{1}{2\pi\sqrt{\left(L_s \frac{C_p C_s}{C_p + C_s}\right)}} \tag{3.6}$$

Between the 2 resonance frequencies the crystal will exhibit an inductive behavior while below f_s and above f_p the crystal will behave capacitive. The range between the 2 frequencies is dependent on the shape of the crystal. When incorporating a crystal in an oscillator design a choice between operating in series resonance (offering low impedance) or parallel resonance (offering high impedance) can be made. The oscillators are constructed using bipolar transistors or FETs for high frequency operation or an opamp in case of low frequency operation (<100 kHz) due to the lower bandwidths an opamp can operate on. The downside of using a crystal for the FSK modulator is that at lower frequencies (<100 kHz) of 85kHz and 90kHz not many crystals are available, crystal oscillators are mostly used for high frequency operation. However, a counter circuit can be used together with a crystal in order to divide or multiply the oscillation frequency. Such an implementation would remove any easy way to tune the oscillator frequency during testing which is an important requirement for this prototype. Hence, using a crystal oscillator is not used for the FSK modulator.

3.1.2.3. Wien bridge oscillator

In this section 3 different sine producing oscillators will be discussed, before the design of the wien bridge oscillator is discussed 2 other similar oscillator circuits are presented. The first possibility being the Hartley oscillator (see Figure 3.4). This oscillator builds further upon the standard LC tuned oscillator, but adds a way to control the amplitude and frequency. Another advantage is that an opamp can be used instead of a BJT or FET transistor, this adds the advantage that the gain of the active stage can now be easily adjusted through the feedback resistors. To sustain the correct oscillation the gain of the opamp must be set to be equal to or slight above the ration $\frac{L1}{L2}$.

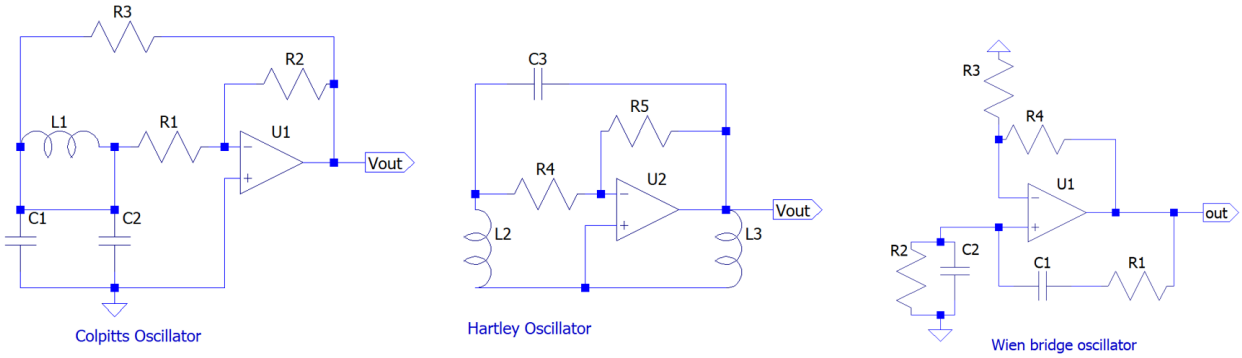

Figure 3.4: Example of the standard Colpitts, Hartley and Wien bridge oscillators using an opamp.

Second, is another LC oscillator, the Colpitts oscillator (see figure 3.4). This oscillator is somewhat opposite to the previous Hartley oscillator. Just as the Hartley oscillator, a minimum gain is needed to start and sustain the oscillation, this being a minimum gain of 2.9. The main advantage of the Colpitts oscillator compared to the Harley oscillator is that it produces a more pure sine wave. This is mostly due to the low impedance path that exists at high frequencies through the capacitors.
The final possible implementation for the oscillator is using a so-called Wien bridge oscillator (see Figure 3.4). This oscillator solves the biggest problem for practically using the previously 2 LC oscillators, that being that tuning the output frequency requires tuning the capacitance or inductance of one or both of the capacitors

and inductors of the circuits. Now, both the amplitude and the oscillation frequency can be tuned by changing the resistor values, this will be realised by using multi turn potentiometers. The Wien bridge oscillator is based on a standard RC oscillator using an opamp. The oscillator uses 2 RC stages that has good stability at its resonance frequency, low distortion and is relatively easy to tune. For the RC circuits R1=R2 and C1=C2. This would theoretically produce a pure sine wave at its output.

The 2 RC circuits form a series connected low-pass and high-pass filter resulting is a very selective band-pass filter with a high quality factor Q at the selected frequency. This leads to the output phase advancing the input phase at lower frequencies and lagging the input phase at higher frequencies. The 2 signals are in phase at the oscillation frequency given by

$$f_c = \frac{1}{2\pi RC} \tag{3.7}$$

In order to sustain the oscillation, the attenuation by the network needs to be compensated correctly. The transfer function of the Wien bridge oscillator is shown in equation 3.8[11].

$$\frac{Vo}{Vi} = \frac{j\omega C_1 R2}{1 + j\omega(C_1R_2 + C_2R_2 + C_1R_1 - \omega^2(C_2C_2R_1R_2))} \tag{3.8}$$

For the condition to have 0°phase shift equation 3.9 is used.

$$\omega^2 = \frac{1}{C_1C_2R_1R_2} \tag{3.9}$$

Then, the transfer function becomes:

$$\frac{Vo}{Vi} = \frac{C_1R_2}{C_1R_2 + C_2R_2 + C_1R_1} \tag{3.10}$$

Now taking R1=R2 and C1=C2 gives:

$$\frac{Vo}{Vi} = \frac{1}{3} \tag{3.11}$$

Therefore, a gain of 3 is needed to fulfill the requirements of having 0°phase shift at the output and unity gain. The wien bridge oscillator uses a standard inverting negative feedback network, thus the gain is simply determined by $\frac{Vo}{Vi} = 1 + \frac{R_4}{R_3}$. An important note to keep in mind is that increasing the gain much more than 3 will give a more distorted output, thus the gain should be close to 3. The first implementation of the oscillator in LTspice is built using a general purpose opamp (LM741) since the behaviour of the opamp would not influence the oscillator much or any. In accordance to figure 3.4 the capacitor value is calculated to be $C_1 = C_2 = 1$nF and the resistor value $R_1 = R_2 = 1872\Omega$. And the selected gain equals 3.1 by using $R_3 = 10k\Omega$ and $R_4 = 21k\Omega$.

Figure 3.5 shows the simulation result of the oscillator, the result shows that the current topology can't sustain a stable amplitude however the output sine is very pure. When increasing the gain to 4 the output amplitude is flat, however, the sinusoidal wave has diminished to a sharp triangular wave.

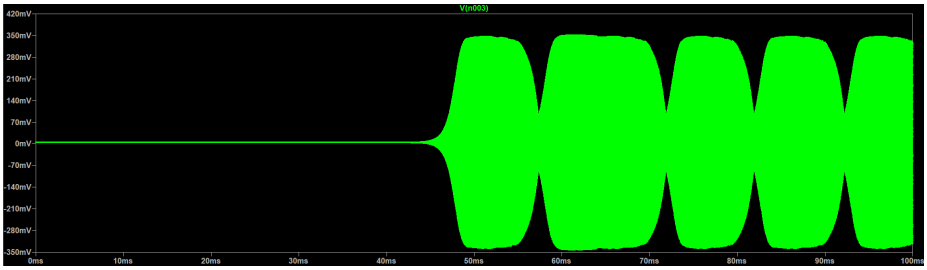

Figure 3.5: Measurement simulation of the Wien bridge oscillator.

amplitude stabilization

In order to control the output amplitude of the oscillator there are 2 possible consideration for an implementation to aid the current design. First, a JFET can be used in the feedback network to implement AGC [11] or a diode clamp can be used in the feedback network [15]. Here an implementation using a diode clamp will be discussed. In figure 3.6 the diode clamp together with a high value resistor is placed in parallel to the feedback resistor R_3.

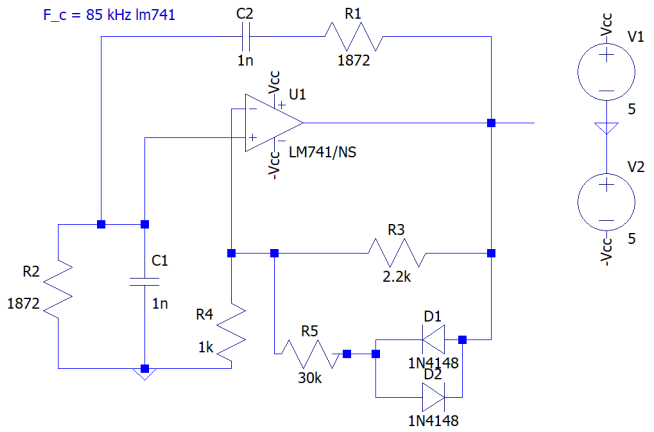

Figure 3.6: Circuit of a Wien bridge oscillator at an oscillating frequency of 85kHz using a LM741 opamp and a diode clamp.

The diodes act as an amplitude reduction mechanism, when the diodes are on (conducting) the gain is reduced by the parallel combination of R_3 and R_5. The current implementation has a gain at start up that is slightly higher than 3 to ensure that the oscillation starts. The alternating conduction from the diodes ensures that the gain is momentarily slightly below 3 to stabilize the oscillation. Furthermore, the values of the feedback resistors were lowered by a factor of 10 in order to reduce the generated thermal noise. Figure 3.7 shows the simulation result of the amplitude stabilized Wien bridge oscillator, now the amplitude stays approximately flat as expected. The lowering of the resistor values in the feedback network reduced the start up time dramatically from approximately 40 ms to 5 ms, also the output amplitude increased to 1.3V peak-to-peak.

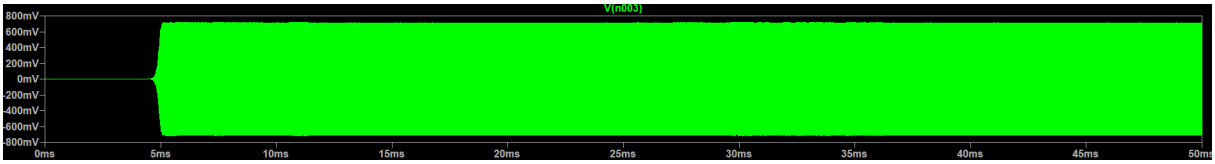

Figure 3.7: Measurement simulation of the Wien oscillator with amplitude stabilization.

However, when plotting the frequency spectrum of the obtained waveform the oscillation frequency of the obtained peak is at 58.2kHz. Apparently the LTspice simulation of the complete Wien bridge oscillator shows quite a large deviation to the ideal frequency of 85kHz. To determine the correct values for the RC networks the step function in LTspice is used to iteratively obtain the correct values. After the simulation the values for R=3500Ω and c=0.5nF yield a oscillation frequency very close to 85kHz. The same process is done for 90kHz, now obtaining R=3300Ω and C=0.5nF.

3.1.2.4. FSK modulator

Now that the oscillator is designed properly, it has to be implemented as a FSK modulator. There are 2 different methods to implement the modulator. First, in order to change the oscillation frequency the two resistors in the RC networks can be replaced by digital potentiometers in order to change the frequency dynamically between 85kHz and 90kHz. This would theoretically lead to a smooth transition between the 2 symbols. However, since the Wien bridge oscillator would not behave as ideally as in the simulation the tuning with the digital controlled potentiometers can result in quite inaccurate results. The second method is using 2 different Wien bridge oscillators of which one is tuned at 85kHz and the other at 90kHz and then using a digital

controlled analog multiplexer to switch between the two frequencies. This, however, would lead to possible (sharp) discontinuities between the 2 symbols and thus reduce the bandwidth. However, tuning would be much easier and therefore this method is chosen.
Another change that needs to be made to the initial designed Wien bridge oscillator is the opamp, in the previous design the LM741 is used. However, a better opamp can be chosen to improve the final result. After some research the LT1358 came up to be the best option that was available, this opamp also has a LTspice model available from the manufacturer. This opamp is characterized by its high speed, high slew rate, low input offset voltage and low input current bias. However, as with the LM741 both require a differential supply voltage, but the final system will use a single ended 5V power supply (RQ-NF.PLC.7). To solve this problem a virtual ground at 2.5V can be created to use as the reference of the system (see figure 3.8). To isolate the oscillation caused by the RC network an additional buffer using the LT1358 is placed. In order to digitally switch between the 2 frequencies an analog multiplexer is used. After some research the ADG408 was chosen, the ADG408 delivers low power dissipation, low on resistance and can be operated using a single ended voltage supply. Also, a suitable LTspice model is provided by the manufacturer. In figure 3.8 the complete FSK modulator is shown and the connections to the multiplexer. An additional decoupling capacitor of 15nF is placed in parallel to the output in order to filter out the present high frequency noise that was seen during simulation. A load of 300 Ω is connected to drive the multiplexer signal. Finally, additional 100nF and 10uF capacitors are placed over the power supply connections and at the virtual ground output in order to filer out any present distortions in the power supply.

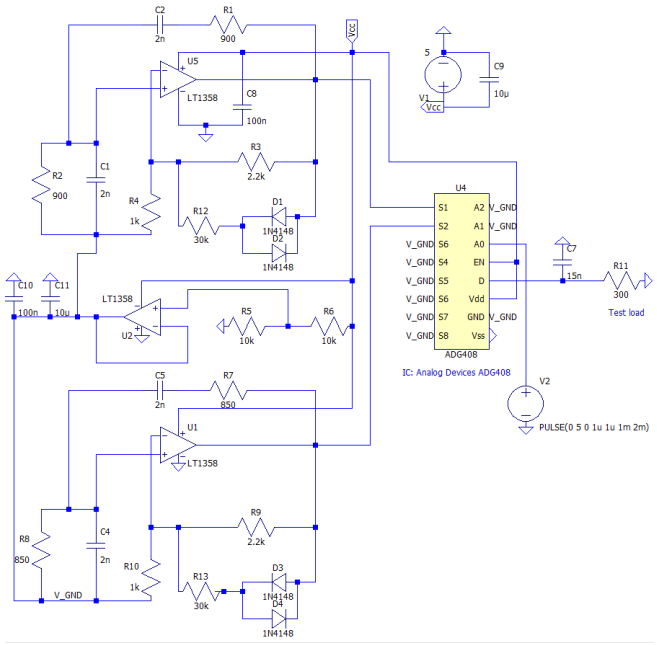

Figure 3.8: Circuit of FSK modulator consisting of 2 separate wien bridge oscillators connected to a digitally controlled analog multiplexer.

For testing of the system a pulse generator is connected to the first selection port of the multiplexer while grounding the other 2 selection ports. The resulting simulation waveform is shown in figure 3.9.
As expected, there is a discontinuity at the switching time as shown in the figure above, the frequency spectrum is shown in figure 3.10. The two peaks of the oscillation frequency are located at 85.00kHz and 89.50kHz, which is close enough to the specified modulation frequencies.

3.1.3. Noise and tolerance analysis

Now that the basis of the system has been designed, a noise and tolerance analysis using LTspice is conducted to tune different component values even further to obtain lower noise and to determine which components contribute most to system stability. When all the noise is measured of each individual subsystem the noise can be added at the end of the system. At the demodulator input, this noise can be represented as a additional noise source that is added to perform a transient simulation while including the present noise floor. The simulation results and more detailed information can be found in appendix A.1.1 and A.2.0.1 for the noise

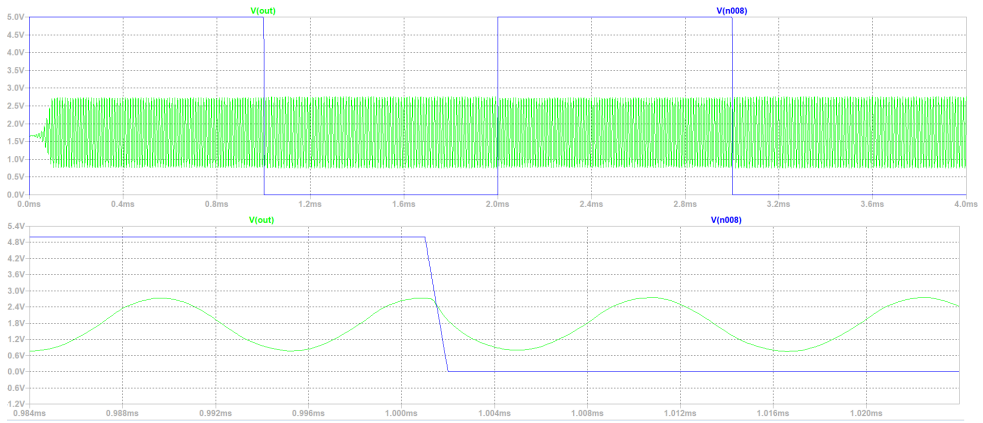

Figure 3.9: Simulation waveform of the FSK modulator.

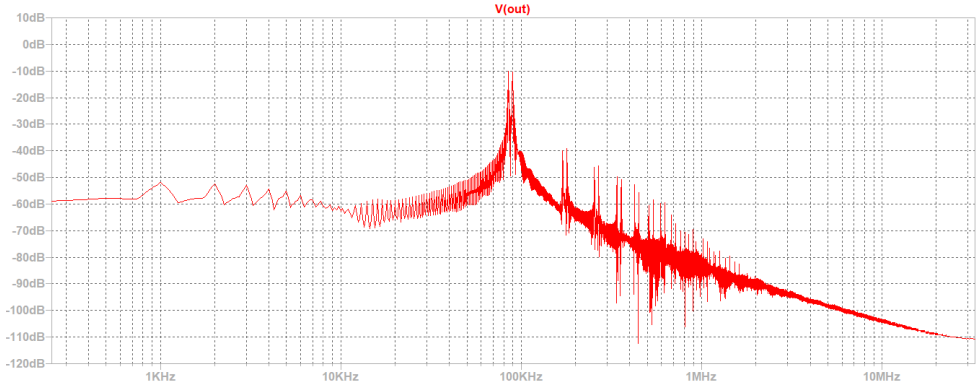

Figure 3.10: Simulationof the frequency spectrum of the FSK modulator.

and tolerance analysis respectively. According to the simulation, the resistor values of the oscillator were lowered to 900Ω while increasing the capacitor values to 2nF to reduce the noise level further. The tolerance analysis using a 10% value deviation also shows correct functioning of the system.

3.1.4. Building and validation of the subsystem

Now that the design and simulation process of the modulator has been completed the subsystem is built. The system is built on a perfboard, first the 85kHz Wien bridge oscillator together with the virtual ground is built and then tuned by the potentiometers. The initially oscillating frequency measured using an oscilloscope was 82.9kHz, as expected there is a slight difference with the simulated circuit. Using a spectrum analyzer the gain and the frequency of the oscillator was changed such that the best possible sine wave was produced at 85kHz. The 85kHz output signal is shown in figure 3.11 together with a 85kHz sine wave from a signal generator as reference. For the same frequency span (10kHz to 300kHz) the measured signal power on the fundamental frequency of the Wien bridge oscillator (84.9kHz) was approximately -0.40dBm. The 2^{nd} harmonic was -24.3dBm and the 3^{rd} harmonic was -9.5dBm. The 85kHz signal from the function generator measured at the fundamental frequency also -4.0dBm, 2^{nd} harmonic = -26.3dBm and 3^{rd} harmonic = -4.3 dBm. So in total the wien bridge oscillator seems to have a lower total harmonic distortion (THD) compared to the signal generator from which can be concluded that the wien bridge oscillator works properly. The same procedure was followed for building, tuning and testing the 90kHz wien bridge oscillator. In figure 3.11 the measured frequency spectrum is shown. Here, at the fundamental frequency of 89.9kHz the signal power is measured at -4.0 dBm, the 2^{nd} harmonic for 179.1kHz is at -24.15dBm and the 3^{rd} harmonic of 269.9kHz is at -9.65dBm. Now adding the analog multiplexer and a square wave digital control signal from the signal generator at 500Hz (so a 1kbps baud rate) the total output spectrum of the signal is measured. In figure 3.12 the measured spectrum is shown, the highest peaks were detected on 84.94kHz and 90.11kHz. Here the signal power on the fundamental frequency increases and the side band power decreases for lowering the baud rate as expected. At 1kbps the obtained spectrum had a SNR or approximately 27dB when measuring the noise floor of the

frequency spectrum, which is good enough for the subsystem. The build circuit is shown in figure 3.13.

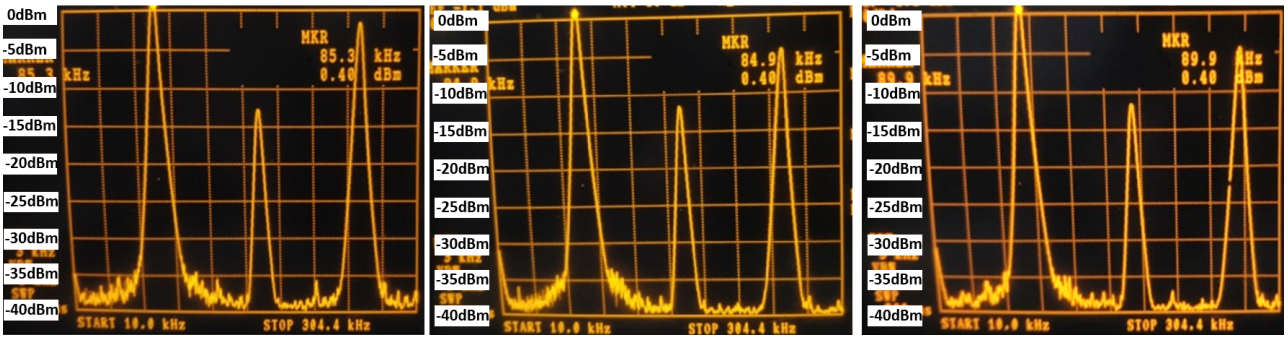

Figure 3.11: Measured frequency spectrum of a 85 kHz sine wave from a function generator (left) and the 85 kHz wien bridge oscillator (middle) and 85 kHz wien bridge oscillator (right).

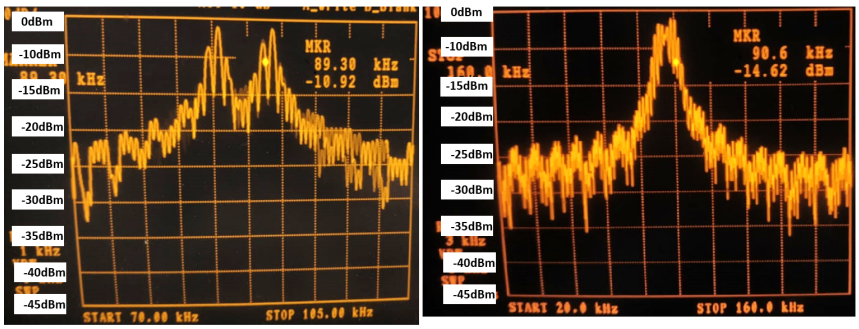

Figure 3.12: Measured frequency spectrum at the output of the analog multiplexer for different frequency spans.

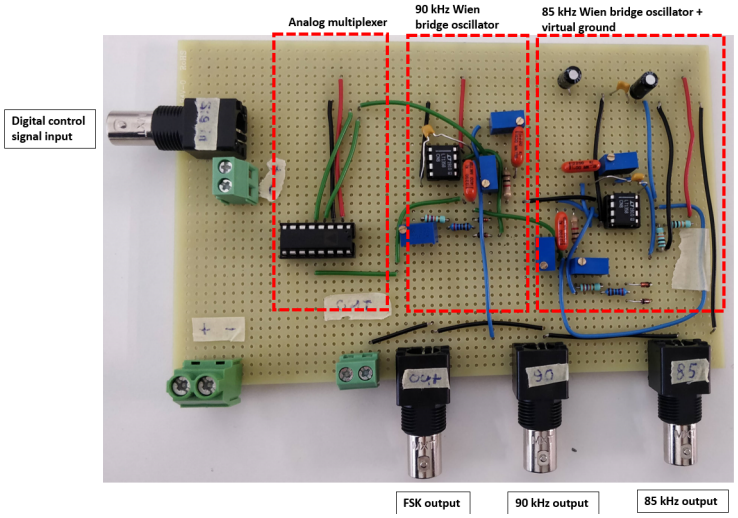

Figure 3.13: Picture of the final FSK modulator circuit.

3.1.4.1. Driving capability

Since the modulator is directly connected to the line driver, it is important to measure how low the input impedance of the line driver can be before distortion occurs at the modulator output. It is beneficial to have a lower input impedance at the line driver to reduce the noise at the output of the line driver as much as possible. Therefore, a variable load is connected to the modulator output which is connected to an oscilloscope and a spectrum analyzer. The resistance was gradually lowered from 5kΩ until the distortion was clearly visible. From values below 2.5kΩ the signal amplitude started to decrease gradually but only below 260Ω the

output signal became noticeable distorted. At this value the peak-to-peak voltage of the signal had decreased from 3.06V to 2.58V.

3.2. Line coupler and cable characterization

The system being designed is a PLC system. Thus, circuitry has to be designed in order to couple both the transmitter and receiver to a LVDC powerline as specified in the requirements. The line coupler circuit thus needs to superposition the signal from the transmitter onto the powerline and needs to extract this signal again at the receiver side. The following requirements can be written for the line coupler circuit:

- The line coupler needs to provide galvanic isolation from the LVDC powerline.
- The line coupler needs to provide a flat transfer over the frequency range of interest for communication.
- The line coupler needs to include circuitry that protects sensitive circuitry against voltage and current transients on the LVDC powerline.
- The line coupler needs to be identical for the transmitter and receiver side in order for bidirectional communication to be possible in a future implementation.

3.2.1. Line simulation and measurements

In order to design an optimal line coupler circuit, electric parameters can be extracted from the powerline which will act as the channel for this communication system. These parameters can be used to provide an accurate model of the powerline with which the line coupler can be designed. The following paper provides an extensive method to arrive at the transmission parameters using a vector network analyzer [4]. Unfortunately, this equipment was not available and a simpler transmission line model presented in [13] will be used, which is given in Figure 3.14. The parameters can be approximated using a precise LCR meter.

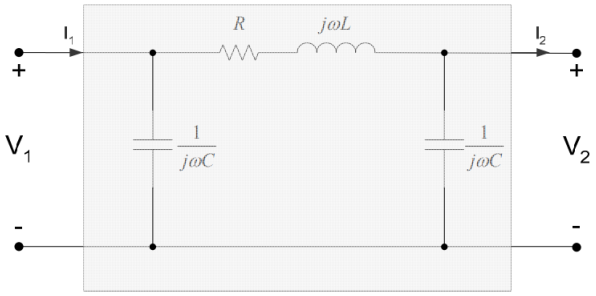

Figure 3.14: The simplified model for a transmission cable from [13].

Next to the the model of the powerline there are two other design considerations, namely the load and the source, have to be considered to complete the model of this communication channel. A purely resistive load will be assumed in this model of which the value can be determined using the data of the DC grid subgroup. It was determined that one house draws an average of 3200W of power, which at 400V represents a resistive load of about 50Ω. The source is modelled as an ideal voltage source with a resistive source impedance. The value of this source impedance is determined by matching the attenuation of the model at the desired frequency with the attenuation measured by a network analyzer of the actual test setup. The final channel model is given in figure 3.15. Both attenuation plots of the model and that of the actual test channel are given in figure 3.16. As can be seen from this figure, the model is quite accurate for the frequency range of interest, there is an attenuation of approximately 10dB for the frequencies that will be used for the communication.
Finally, the modeling of noise in the PLC channel has to be considered. A lot of extensive studies have been conducted to accurately model the noise in a communication channel [34] [20]. The noise on powerline communication channels can be split up into three different types of noise: impulsive noise, background noise and additive white noise. Of these different types impulsive noise, is the most dominant. The communication system is for the LVDC grid which means that this type of noise will mainly be at the switching frequencies of the converters. As described in chapter 3.1 the FSK signals are chosen to be not near these switching frequencies. Also, because of limitations of the generators in the test setup, only white noise will be considered for this study. In the model (see Figure 3.15), this white noise is added as an extra source in series with the powerline with a peak value of 6mV as given as the requirement of the maximum noise value on a powerline in subsection 3.1.1.2.

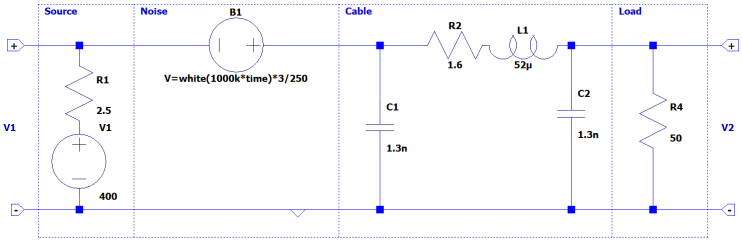

Figure 3.15: The full communication channel model with all circuit values.

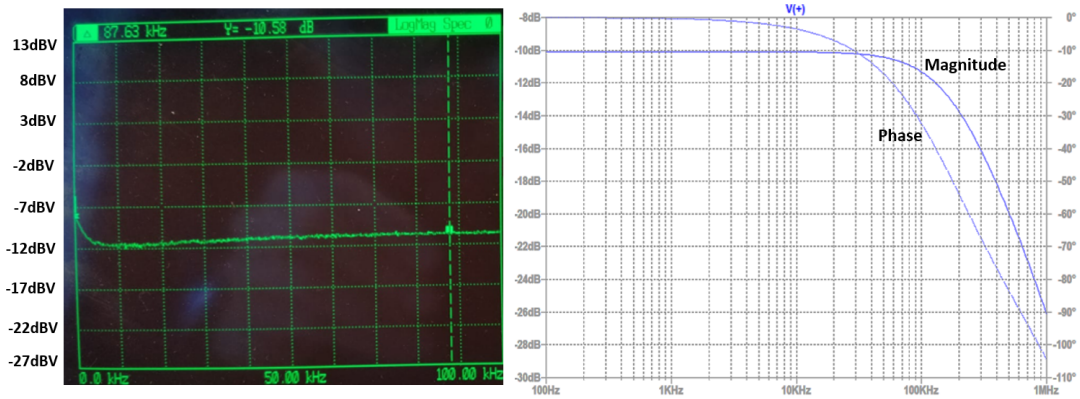

Figure 3.16: Left: the attenuation graph of the full channel measured with a network analyzer. Right: The attenuation of the final model simulated with LTspice.

3.2.2. Different topologies

There are three different basic line coupler implementations that exist for DC lines: resistive line couplers, capacitive line couplers and inductive line couplers. Resistive line couplers consist out of a large voltage divider that is used to bring down the DC voltage to an acceptable level such that it can be filtered out by a conventional signal filter. A large downside of this implementation is that the to be extracted signal is also attenuated, which makes it harder to detect. Also, due to a resistor being placed in series with the signal path a lot of noise is added to the signal. On top of that, a resistive line coupler does not provide galvanic isolation which is highly desirable for a good line coupler.
Next, the capacitive line coupler circuit. Which is in its most basic form just a capacitor connected to the DC line. This capacitor will block all DC voltage and thus will be able to act as a line coupler. This capacitive filter will act as a low-pass filter together with the load impedance. This load impedance might be undefined as both the transmitter and receiver need to be able to connect to this line coupler. This will result in a variable transfer which is undesirable. On top of that, this capacitive coupler will also not provide galvanic isolation.
Finally, the inductive line coupler, which in its most basic form consists out of a transformer. The big advantage of this configuration is that it provides total galvanic isolation. Also, by adjusting the turn ratio, the circuit can be adjusted for the right load impedance and powerline impedance. A transformer will damage when a DC voltage is applied to its terminals, for that reason it will be combined with a capacitor as shown in figure 3.17. This capacitor, together with the primary inductance of the transformer, will combine to a high-pass filter, this will prevent any DC current from flowing into the transformer. The cut-off of this filter needs to be well below the frequency range of interest. For a second order LC low-pass filter the cut-off frequency is given by:

$$f_c = \frac{1}{2\pi\sqrt{LC}} \tag{3.12}$$

3.2.3. Transformer choice

The winding ratio of the transformer in the line coupler circuit should be determined. In the following paper an experiment was conducted to determine the optimal winding ratio for certain powerline resistances and load resistances[29], the results are given in figure 3.18. The idea is that the communication signal should

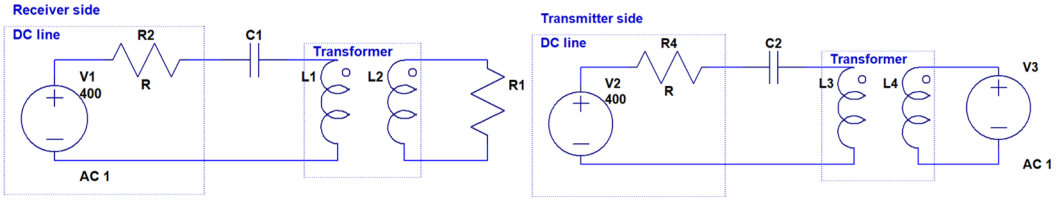

Figure 3.17: Inductive line coupler circuit with DC blocking capacitor, the top circuit shows the line coupler in a receiver setting, the bottom circuit shows the line coupler in a transmitter setting.

be attenuated for a higher load and line impedance, because of the large current this will draw from the transformer. The final transfer of the system won't be influenced because it will be amplified again at the receiver line coupler. Care should be taken however that the SNR at the powerline does not become too small. Using the parameters described in section 3.2.1 the optimal winding ratio is around 2:1. The transformer that will be used in the line couplers will be of the type: WBT2010, these have a winding ratio of $\sqrt{2}$:1. A transformer with a larger winding ratio and a flat frequency response for the desired frequencies was not available. The attenuation as a function of frequency is given in figure 3.19. The attenuation for the frequency range of interest is perfectly flat, the attenuation due to the winding ratio is not taken into account in this graph.

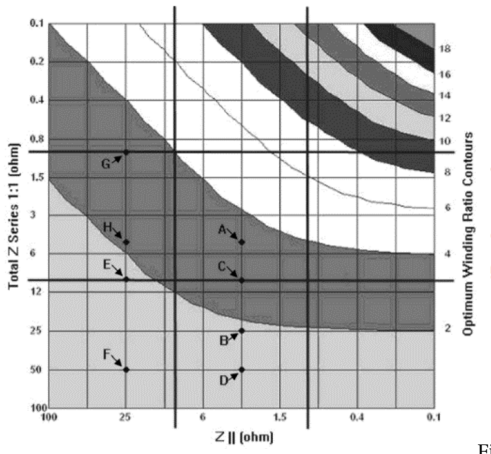

Figure 3.18: This figure from [29], shows the optimal winding ratio for different load and line impedances.

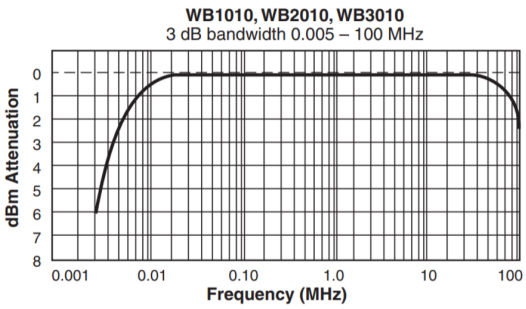

Figure 3.19: This is the attenuation of as a function of frequency for the used transformer of the type WBT2010 [6].

3.2.4. Capacitor value

As specified in the datasheet [6], the inductance of the primary winding is 390 μH. Using equation 3.12 and a cut-off frequency of 11.8 kHz, well below the frequency range of interest, a 470nF value is calculated for the capacitor. Important is that this capacitor needs to be able to handle the 400V DC as is specified as the maximum voltage of the powerline (RQ-NF.PLC.6).

3.2.5. Protection circuit

The line coupler needs to protect the sensitive transmitter and receiver circuitry against large voltage transients. This protection circuit is implemented by using two times 2 diodes in series, to limit both the positive voltage as well as the negative voltage. These diodes preferably are low noise diodes in order to not add too much extra noise to the communication signal. The diode 1N914 was chosen as a protection diode, this diode has a forward voltage drop of 1V, which makes the protection circuit protect the sensitive circuitry against signal amplitudes larger than 2V.

3.2.6. Simulation

A model in which the interwinding capacitance and winding resistance are included will be used to model the coupling transformer. First, the receiver and transmitter line coupler circuits are simulated separately.

The circuits that are simulated are shown in figure 3.20. The simulation results are given in figure 3.21. Next, the whole system including the line model as described in section 3.2.1 will be simulated. The final simulated transfer from the input of the transmitter line coupler to the output of the receiver line coupler is also given in figure 3.21. From this simulation it can be concluded that the line coupler system works as desired, the attenuation at the desired frequencies is about 10dB.

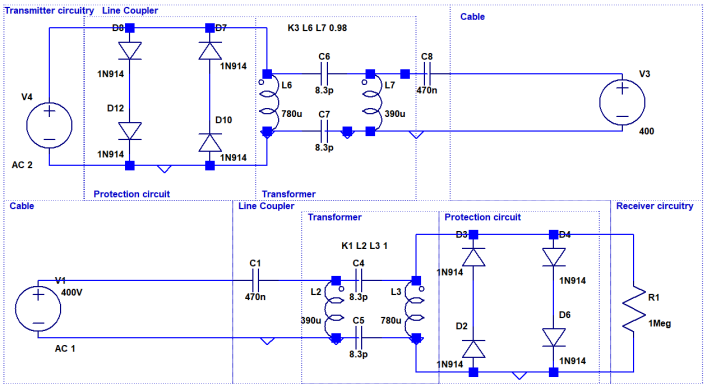

Figure 3.20: The final circuit implementation of the line coupler. In the top figure the transmitter implementation of the line coupler is shown. In the bottom figure the receiver implementation of the line coupler is shown.

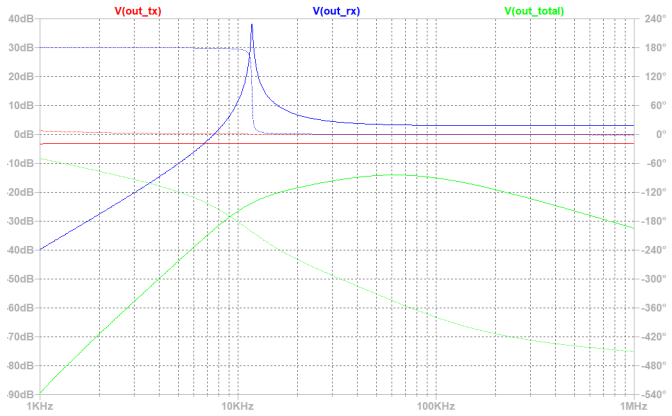

Figure 3.21: The simulation result of the implemented line coupler. The red trace indicates the transmitter, the blue trace indicates the receiver the green trace indicates the full transmitter-receiver line coupler system including the full channel model.

3.2.7. Building and validation of the system

Since the receiver and transmitter line coupler are designed to be equal, the circuit was built twice on separate perfboards. The attenuation graph of both the transmitter and receiver was measured with a network analyzer and the results are given in figure 3.22. After this, the two line couplers modules were directly connected, so using a perfect lossless channel. The results of this measurement is also given in figure 3.22. Finally, the line couplers were connected to the communication channel as described in section 3.2.1, the result of this measurement can also be found in figure 3.22. The final build circuit is shown in figure 3.23. From these results it can be concluded that the line coupler works as desired, the signal is transferred over the communication channel with a attenuation of approximately 10dB for the desired frequencies, the signal is also transferred well when the line couplers are directly connected which indicates that the line couplers will also function for shorter lengths.

3.3. Line driver

The available power from the FSK modulator is not enough to drive the communication signal over the powerline. As can be found in the datasheet of the WBT2010 the maximum driving current of the transformer is given to be 176mA [6]. Therefore, the voltage gain of the line driver should be such that this limit is never

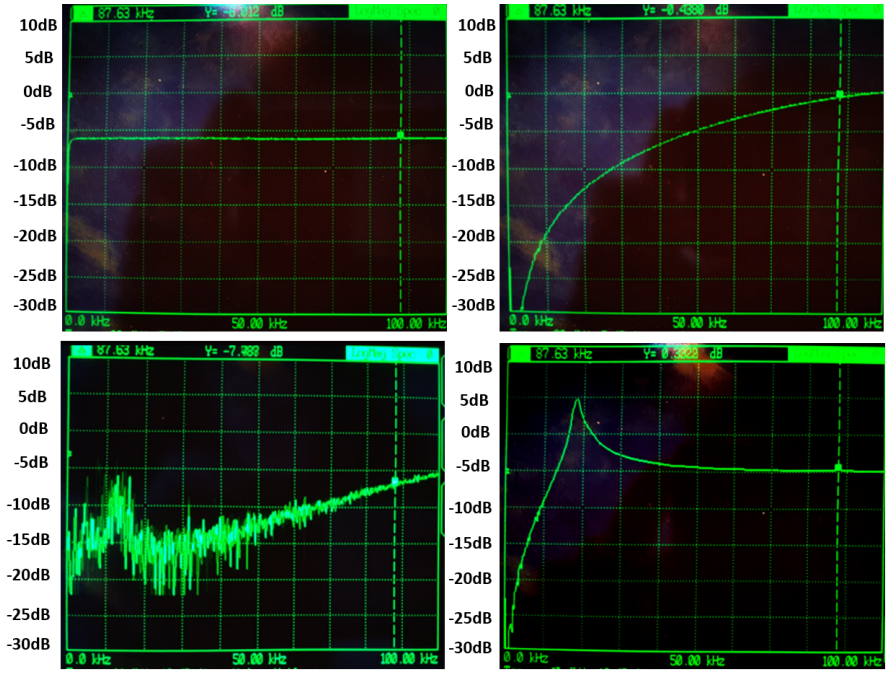

Figure 3.22: The measurements for the line coupler using a network analyzer. The top left figure shows the attenuation graph from the line coupler when used as a transmitter. The top right figure shows the attenuation graph from the line coupler when used as a receiver. The figure in the bottom left corner shows the attenuation from transmitter to receiver when connected to the channel. The figure in the bottom right shows the attenuation graph from transmitter to receiver when directly connected over a perfect channel.

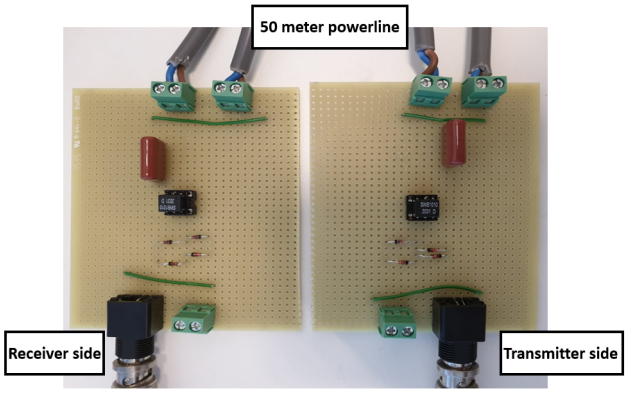

Figure 3.23: Picture of the build circuit.

exceeded. Another requirement as given in RQ-NF.PLC.3 is that the amplitude of the communication signal that is superimposed on the powerline should never exceed 120 dBμV, or 1V. The gain of the line driver should be such that this value is not exceeded, also accounting for the winding ratio of the transformer of the line coupler

One last requirement is that the transformer will break if a too large DC voltage is applied to the inputs. For this reason the signal applied to the line coupler should be differential, so with no voltage offset. An opamp with a differential output can be used for this purpose. The AD8138 was chosen to use for this system. It has a current driving capability of only 90mA, but a differential opamp with a larger current driving capability was not available.

3.3.1. Design and simulation

The circuit diagram of a line driver amplifier circuit using the AD8138 is given in figure 3.24, the differential output is connected to the line coupler model with the channel as designed in section 3.2. The system is run from a single 5V power supply as defined in requirement RQ-NF.PLC.7. The AD8138 requires a symmetrical power supply, for this reason a virtual ground as also designed in section 3.1 is added to the circuit. The gain

of the differential opamp can be set by equation 3.13.

$$\left|\frac{V_{OUT}}{V_{IN}}\right| = \frac{R_F}{R_G} \tag{3.13}$$

The input impedance of the line driver circuit is given by:

$$R_{IN} = \left(\frac{R_G}{1 - \frac{R_F}{2\cdot(R_G+R_F)}}\right) \tag{3.14}$$

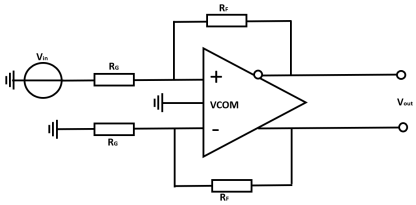

Figure 3.24: A standard differential amplifier circuit using the AD8138.

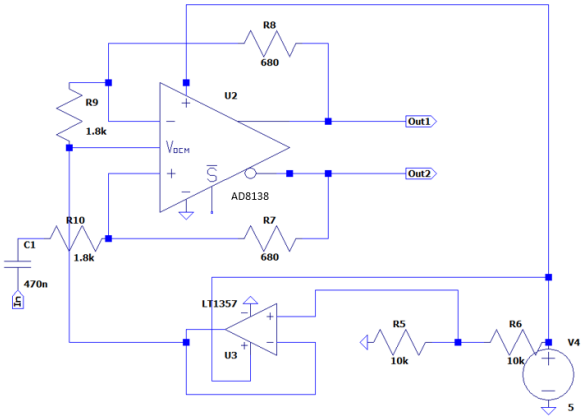

Figure 3.25: The final build line driver circuit.

The requirement for this input impedance is that it should be large enough in order to not cause any disturbances in the modulated signal. A minimal value of 260Ω was determined in section 3.1. The circuit however introduces a resistor in series with the signal path, so it is desired to keep this resistor at a low value in order to keep the added noise as low as possible. It was decided that R_F will take a value of 680Ω, and R_G will be a 5k potentiometer in order to have some flexibility in the gain. But according to simulations this will be in the 1.8kΩ range. This will result in an input impedance of approximately 2kΩ, which is well above the required value. An extra capacitor is added at the input to form a low-pass filter together with the input impedance to remove any unwanted DC voltages (see equation 3.7). This value was chosen to be 470nF which creates a cut-off frequency at approximately 170Hz. The final circuit is given in figure 3.25. Finally, a noise and tolerance analysis was performed on the design of the system given in appendix A.1.3 and A.2.1 to asses the performance and reliability of the circuit. From these simulation it is concluded that the system functions as intended with a note that the exact circuit values (the four resistor values from the line driver) need to be set very accurately in order to achieve the intended behaviour.

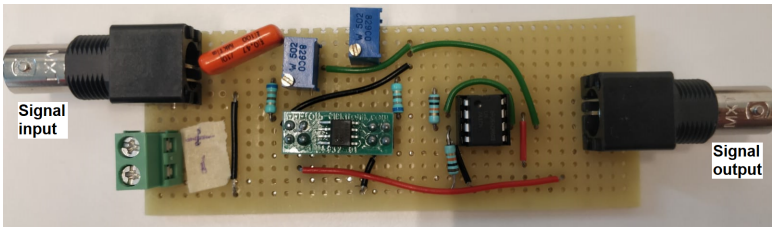

Figure 3.26: The final build line driver circuit.

3.3.2. Building and validation of the system

The line driver circuit was built on a perfboard using the aforementioned potentiometers (see Figure 3.26). Calibration was done with these variable resistors by starting at a value of 5kΩ (a very large attenuation), and reducing this until either the current limit was reached or a distortion occurred on the output signal. The circuit was connected to both the modulator and to the line coupler including the communication channel.

The current and the voltage wave forms of three different resistor values are shown in table 3.2 and figure 3.27 respectively. All values where below the maximum limit of 90mA, but because of the distortion occurring for lower values it was decided to take for R_G a final value of 1.5kΩ.

Table 3.2: Current measurement line driver output

Resistor value [kΩ]	Measured current [mA]
2.6	27.1
1.5	41.1
1.0	46

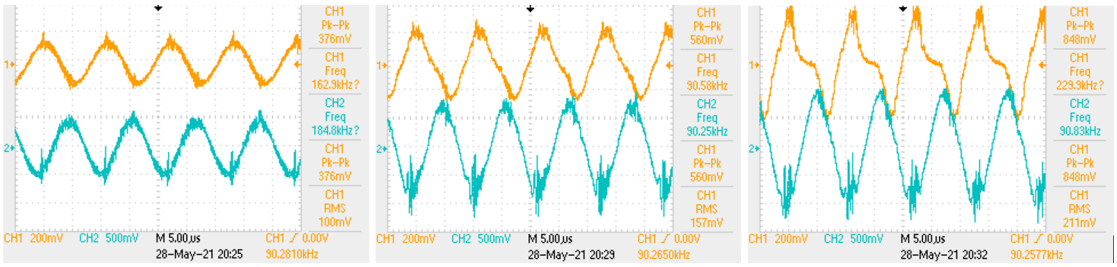

Figure 3.27: Waveform distortion for increasing resistance values, left R=2.6kΩ, middle R=1.5kΩ and right R=1kΩ.

3.4. Band-pass filter and amplifier

In this chapter the design of the band-pass filter will be discussed. The goal of this filter is to filter out any of the out of band noise and interference that the signal might collect from the line driver, line couplers, fluctuations of the DC voltage and the 50 meter long powerline to name a few. In this chapter different design considerations will be mentioned and discussed in order to achieve the best suited filter design for the system.

3.4.1. Design considerations

The goal of the band-pass filter is to achieve the best possible performance according to the desired specifications of the system. In order to set these requirements, measurements are needed of the real system at the output of the receiver-side line coupler. Most important is the frequency spectrum of the received signal to determine where and by how much the noise and interference in the system needs to be attenuated. Based on the measurements the filter response has to be designed to have the best trade-off between performance and complexity. First, the BPF topology also needs to be determined. The filter can be implemented as a active or passive filter. The advantages of the active filter is that there are no insertion losses, so at the pass-band the gain would be equal to 0 dB. The active filter could be designed such that it would add an additional pass-band gain, then no separate amplification stage before the demodulator would be needed. Another advantage is that the active filter can realize a more complex filter without using inductors, which are beneficial to the practical design of the circuit. However, the active filter is of course limited in its frequency range since practical opamps have a finite gain-bandwidth product (GBP). However, since the system operates at low frequencies (<100kHz) this design issue would not be considered a problem using modern opamps. As a final consideration the design of the active filter should include a separate input buffer stage, since the filter would in most practical cases not have a large/infinite input impedance, since the line coupler would not be able to driver smaller loads.

3.4.1.1. Design approach

As described in the previous section, a higher order active filter design is going to be realized for the PLC system. There are two classes the design of the active higher order filter can be divided in, either filter design by using a aggregated approach (placing all components in one stage) or using a multistage approach. Since, for the design of the prototype tunability of the different subsystems is very important the choice is made to design the filter using multiple cascaded stages. In order to realize the filter, multiple 2^{nd} order filter stages are cascaded to create a higher order filter. Here, there are two methods to design the filter stages that are considered, these being staggered tuning and synchronous tuning techniques. With staggered tuning each

second order stage is tuned at a slightly different center frequency. While with synchronous tuning each stage is tuned identically. The advantages that staggered tuning provides is that it creates a wider bandwidth at the expense of a reduced gain. To further elaborate, with synchronous tuning each stage will add 3dB to each band edge of the first stage. Thus, the 3dB bandwidth will become more and more narrow with each additional stage. The overall gain reduction can be explained by considering what happens at resonance in the filter. Since each stage is tuned to a slightly different frequency when one stage is at resonance the other stages are not, thus the entire filter will not be able to achieve its maximum gain.
Also, staggered tuning provides a sharper transition from the pass-band to stop-band regions, this transition regions is also called the skirt. Thus overall it will provide better selectivity. For these reasons, the staggered tuning technique is chosen. For the filter, the center frequency f_c is set at 87.5 kHz, the pass-band spans from 80 kHz till 95 kHz.

3.4.1.2. Filter topology

For the BPF filter, 2 different topologies are considered, the Sallen-Key (SK) and multiple-feedback (MF) filters (see Figure 3.28). In order to select the best suited topology for the PLC system the filters are analysed for both their high-pass and low-pass performance. The BPF typologies shown in figure 3.28 are designed such that they can both realize a pass-band gain larger than unity.

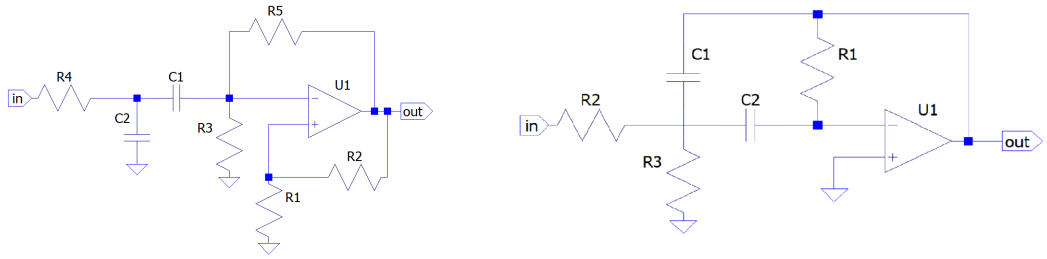

Figure 3.28: Circuit topologies for the Sallen-Key BPF (left) and the multiple-feedback BPF (right).

A big advantage of the MF BPF is that it uses less components compared to the SK BPF, this will also make the tuning of the filter easier. According to the following book the MFB is mostly used for BPF design because the filter response is less sensitive than for the SK configuration [23]. Furthermore, the MF BPF can deliver a higher quality factor Q and a higher gain. The quality factor is a measure of peaking at the center frequency f_c, thus a higher value of Q will give more selectivity. The quality factor for a second order system is defined as:

$$Q = \frac{f_c}{B} = \frac{f_c}{f_2 - f_1} \tag{3.15}$$

Here f_2 and f_1 are the -3dB cut-off frequencies of the pass-band. An advantage of the SK configuration is that the Q factor can be tuned via the amplifier gain $1 + \frac{R1}{R2}$ without modifying the center frequency f_c [23]. However, the Q factor and the pass-band gain A_m cannot be adjusted independently. With the MFB configuration the Q factor, A_m and f_c can be adjusted independently, here A_m is the pass-band gain. Therefore, the MFB configuration is chosen to be implemented in the system.

3.4.1.3. Filter response

The filter response will determine the frequency response of the filter, here three different filter responses were considered. These being, butterworth, chebyshev and bessel. The filter response will determine the transition region of the filter, how fast the pass-band goes down to the stop-band. Also, the amount of ripple in the pass-band or stop-band are determined by the filter response. The mentioned three responses are all-pole filter responses, thus the location of the poles on the s-plane determines the frequency behaviour of the filter. The butterworth will result in a maximally flat amplitude in the pass-band. The chebyshev has better stop-band attenuation but has a large(er) overshoot at the edges of the passband, and the chebyshev suffers from equal-ripple in the amplitude of the pass-band. The bessel has the lowest stopband attenuation of all the responses, however, has the best in-band group delay. The group delay is, however, not an important measure for the PLC system. Since there are no significant high noise levels or disturbances close to the passband a chebyshev implementation will not be necessary (see Section 3.4.2). The flat passband transfer of the butterworth is beneficial to retain the highest signal as possible.

3.4.1.4. Stage ordering

In case a BPF with an order higer than 2 is chosen there are multiple opamp stages in the design as discussed earlier. The ordering of these stages may affect the noise behaviour of the filter and the voltage range at the output of the filer. In the case that one filter stage has a Q < 1 and another having a Q >1, the first stage will cause attenuation compared to the second stage. In the case the voltage range might be of concern a stage with Q<1 is placed first, this will also help in the case the slew rate might cause a problem to the design. In the other case, when low noise is desired, it is better practice to have the stage with Q<1 as the second stage.

3.4.2. System measurement

In order to design the frequency response of the BPF a frequency measurement is needed of the signal input of the BPF. For this the subsystems at the receiver side are connected and the communication channel is connected to both line couplers. A spectrum analyser was used to obtain the measured frequency spectrum shown in figure 3.29.

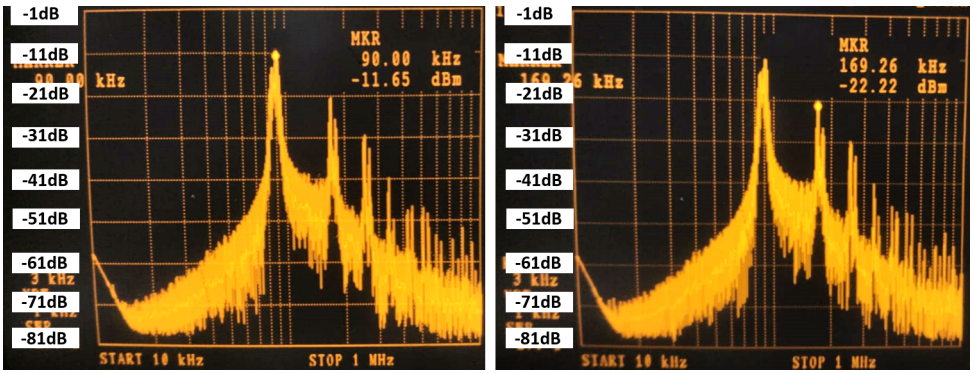

Figure 3.29: Frequency spectrum of the measured system at the output of the receiver side line coupler with a 30V voltage on the powerline.

From the obtained measurement the first large out of band peak is located at 169kHz measuring at -22.22dBm. The peaks at the FSK frequencies are measured to be -11.65dBm. Fortunately, the amount of noise close to the edge of the frequency band of interest is not too high in this measurement. To suppress the present noise and disturbances even further the goal is to attenuate the peak at 169kHz with an extra 20dBm. Since achieving a higher SNR is one of the most important goals to have the highest success of demodulating the signal. To calculate how much attenuation in dB is needed per decade the relative frequency difference is calculated:

$$\mathrm{Log}_{10}\frac{f2}{f1} = \mathrm{Log}_{10}\frac{169}{90} = 0.27 \tag{3.16}$$

Thus, in order to have 20dBm attenuation at 169kHz a filter with a 80dB per decade roll-off is needed. This corresponds to a 8th order filter. However, also a 4th order filter with a 40dB per decade roll-off can be used with a Q>1. Since a 4th order filter with 2 stages is not too complex in design this filter order is chosen to be designed. The goal is to achieve the highest possible attenuation at frequencies outside the pass-band of 80-90 kHz while keeping the pass-band as flat as possible.

3.4.2.1. Filter design

During the design process of the BPF, two different design methods were used from [33] and [23]. The first uses synchronous tuning and the second discusses a method using staggered tuning to design a MFB BPF. Using the filter topology shown in figure 3.28 the synchronous tuned 4th order filter can be designed using the design equations given in equations 3.17, 3.18, 3.19 and 3.20 [33]. Here, the difference in the stages is the Q-factor to achieve a butterworth response, in appendix C.1 a design table for butterworth responses is shown. From this it can be obtained that Q_1 = 0.5412 and Q_2 = 1.3065 are required for the two stages. First, the value of capacitor C1 can be chosen, for this 10nF is chosen. Then, the constant k can be calculated using equation 3.17. Setting C2 = C1, the value of R_2 is calculated using equation 3.18. In equation 3.18 H is the pass-band gain, which is now set to 1 (0dB). Then, using the different Q-factor values for the different stages the values of R_3 and R_1 can be calculated using equation 3.19 and 3.20. The obtained circuit values are shown in table 3.3.

$$k = 2\pi \cdot f_c \cdot C_1 \quad (3.17) \qquad R_2 = \frac{1}{H \cdot k} \quad (3.18) \qquad R_3 = \frac{1}{(2Q-H)k} \quad (3.19) \qquad R_1 = \frac{2Q}{k} \quad (3.20)$$

Table 3.3: Obtain circuit values for a 4th order butterworth MFB BPF using synchronous tuning.

Filter stage 1 circuit values		**Filter stage 2 circuit values**	
C1 = C2	10 nF	C1 = C2	10 nF
R_1	196.87 Ω	R_1	475.26 Ω
R_2	181.88 Ω	R_2	181.88 Ω
R_3	2207.33 Ω	R_3	112.76 Ω

Secondly, a filter using staggered tuning is designed. The following book is used to give a approximated method to design a butterworth response MFB BPF using the idea behind staggered tuning [23]. For this design approach, again the table in appendix C.1 is used, here the butterworth coefficients for a second order system are taken, $a_2 = 1.4142$ and $b_1 = 1.000$ derived from the butterworth polynomial. Now, the Q for the filter can be set and a simulation of the filter to analyse the frequency responses can be done. The design equations 3.21 till 3.31 are used for the design. First, a factor α is determined in equation 3.21 through successive approximation, here $\Delta\Omega = \frac{1}{Q}$.

$$\alpha^2 + \left[\frac{\alpha \cdot \Delta\Omega \cdot a_1}{b_1(1+\alpha^2)}\right]^2 + \frac{1}{\alpha^2} - 2 - \frac{(\Delta\Omega)^2}{b_1} = 0 \quad (3.21)$$

Then, the two different tuning frequencies f_{c1} and f_{c2} are determined with α using equations 3.22 and 3.23. Now, the individual pole quality Q_i can be determined with Q using equation 3.24, this is equal to both filter stages. Next, the individual filter stage pass-band gain A_{ci} is determined using equation 3.25.

$$f_{c1} = \frac{f_c}{\alpha} \quad (3.22) \qquad f_{c2} = f_c \cdot \alpha \quad (3.23)$$

$$Q_i = Q \cdot \frac{(1+\alpha^2)b_1}{\alpha \cdot a_1} \quad (3.24) \qquad A_{ci} = \frac{Q_i}{Q} \cdot \sqrt{\frac{A_c}{b_1}} \quad (3.25)$$

Finally, the resistor values can be determined for both the first filter stage R_{1i} and R_{2i} while the capacitor values can be set at the start, here taking $C_1 = C_2 = 1$nF (see Figure 3.28):

$$R_{12} = \frac{Q_i}{\pi f_{c1} C_1} \quad (3.26) \qquad R_{11} = \frac{R_{12}}{2A_{ci}} \quad (3.27) \qquad R_{13} = \frac{A_{ci}R_{11}}{2Q_i^2 + A_{ci}} \quad (3.28)$$

$$R_{22} = \frac{Q_i}{\pi f_{c2} C_1} \quad (3.29) \qquad R_{21} = \frac{R_{22}}{2A_{ci}} \quad (3.30) \qquad R_{23} = \frac{A_{ci}R_{21}}{2Q_i^2 + A_{ci}} \quad (3.31)$$

Table 3.4: Obtain circuit values for a 4th order butterworth MFB BPF with Q = 2 using staggered tuning.

Filter stage 1 circuit values, Q = 2		**Filter stage 2 circuit values, Q =2**	
C1 = C2	1 nF	C1 = C2	1 nF
R1	12499.1 Ω	R1	8745.39 Ω
R2	4349.02 Ω	R2	3042.93 Ω
R3	348.03 Ω	R3	243.51 Ω

Now, for different values of the Q factor the frequency response is plotted in LTspice, figure 3.30 shows the different frequency responses of the discussed filter designs. For the simulation the LT1358 opamp is again chosen, the opamp provides a gain bandwidth product of 25MHz which is more than sufficient for the filter. The synchronous tuned filter shows a very symmetric frequency response centered at the correct center

frequency as expected. However, the staggered tuned filters with Q=1, Q=1.5 and Q=2 also show an approximately flat pass-band but have a much smaller skirt region to the stop-band as expected. The filter with Q=5 shows a very high peaking and is centered 78kHz, which do not comply with the requirements of the filter. Based on the simulation results the filter with Q=2 is chosen since it provides a approximately flat pass-band region and a short skirt region, table 3.4 shows the calculated circuit values for this filter.

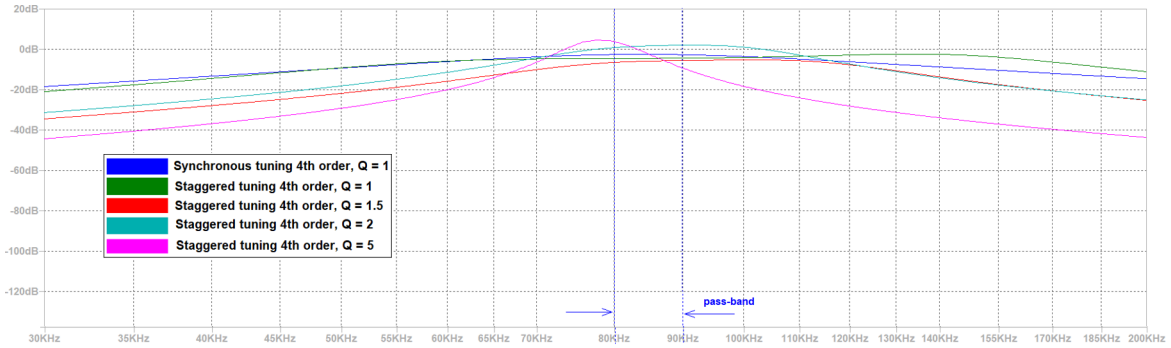

Figure 3.30: Simulation results of the frequency responses for the 4^{nd} order butterworth MFB BPF, for the synchronous tuned filter and the staggered tuned filter for different values of Q.

After the two BPF stages the amplitude of the signal has to be amplified before it can be send to the input of the demodulator. For this a additional non-inverting amplifier stage can be placed after the BPF or the BPF can be designed such that the pass-band gain is larger than unity (0dB). In order to find any differences in these two methods they are both simulated. Here the pass-band gain A_c is set to 2 and the different circuit values were again calculated. The second method is applied by cascading a LT1358 opamp in a non-inverting configuration having a gain of 2. This resulted in a very close overlap without any big difference. Therefore, the method using a separate amplification stage is chosen since it will make the tuning of the amplification much easier since only 2 resistor values need to be changed instead of 6. Finally, a noise and a tolerance analysis were performed on the designed subsystem, which can be found in appendix A.1.4 and A.2.2. From these simulations it was concluded that the system performed according to the design and all deviations were well within the goal of suppressing the higher frequency noise.

3.4.3. Building and validation of the subsystem

The final step is to build and measure the BPF, the total circuit diagram of the filter and the amplifier is shown in figure 3.31. As discussed at the beginning of this section the filter also needed very high/infinite input impedance due to the low driving capabilities of the line coupler. For this reason a buffer stage is added at the input of the first filter stage. The amplifier stage consists of an opamp in a non-inverting configuration where both feedback resistors consist of potentiometer in order to vary the gain of the output easily. Figure 3.32 shows the final built circuit for the BPF and the amplifier. In the circuit potentiometers were used for the resistors in both filter stages in order to set the circuit values as accurately as possible.

The circuit is measured using a spectrum analyzer to obtain the frequency response of the filter. For this the two filter stages are connected to both the input buffer stage and an amplifier stage. Bot the amplified and non-amplified outputs were measured. Unfortunately, the spectrum analyser used had only an input matched at 50Ω and no high impedance input to measure the system. However, a network analyzer with a 1MΩ input impedance was also available, unfortunately this device was limited to measuring till 100kHz which is too low for the designed system. In order to correct for the added attenuation, the spectrum analyzer was first measured by itself using a function generator. This resulted in a -27.62dBm and -30.22dBm measured attenuation between 70 kHz and 110kHz due to the low impedance input of the spectrum analyzer.

Next, the filter was measured in a frequency span from 10kHz till 1MHz using the frequency sweep function of a function generator (applying a 500mV peak-to-peak sine wave with a 2.5V offset). Figure 3.33 shows the obtained frequency response of the filter without an additional amplifier stage. The peak of the frequency response was located at 83.72kHz with a magnitude of -24.57dBm. This means that at the center frequency of the pass-band there is a gain of approximately 3.60dB. Then, measuring the -3dB bandwidth resulted in a bandwidth spanning from 71.96kHz till 107.5kHz.

The measurements show a symmetric frequency response similar to what was designed using LTspice. The roll-off characteristics at the cut-off frequency at the higher frequencies seem to be a bit steeper compared

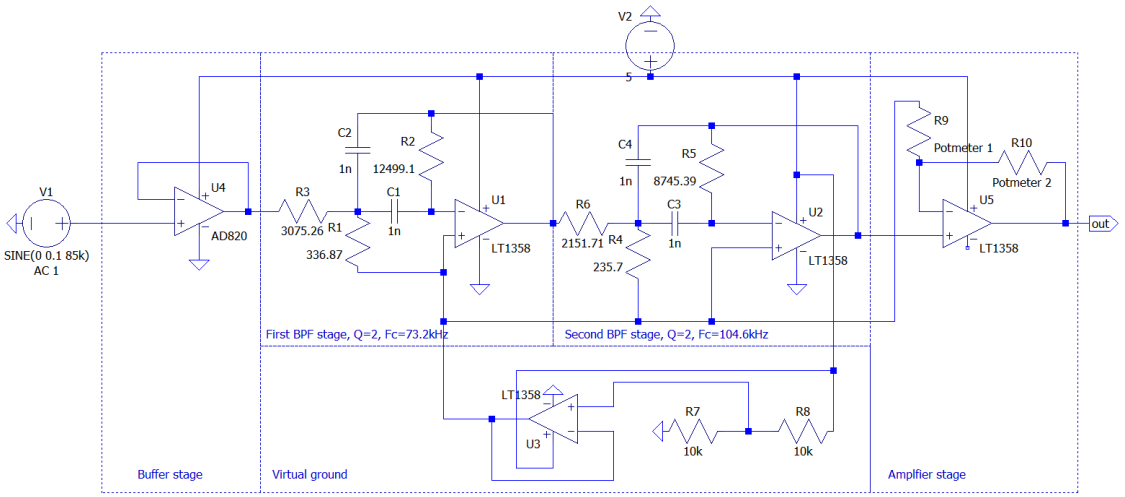

Figure 3.31: Circuit diagram of the 4th order butterworth MFB BPF.

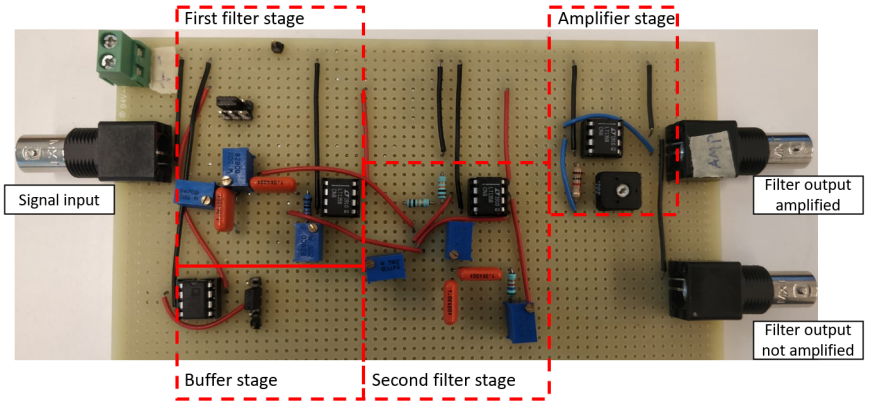

Figure 3.32: The final build circuit of the BPF and amplifier.

to the lower frequencies. However, since the attenuation at the higher frequencies is at interest this does not pose a problem. The -3dB bandwidth of the pass-band, however, is wider than designed, spanning 35.54kHz instead of 15kHz. The pass-band width could be further reduced by tuning the different resistor values of the two filter stages.
Finally, the amplifier stage is measured. For the amplifier the output voltage is amplified to a peak-to-peak voltage of 3.40V, at this output voltage the output wave seem to get distorted for any higher value. In figure 3.33 the frequency spectrum is shown of the amplified output signal. As expected there are some higher frequency components present due to the close distortion of the output signal. The -3dB bandwidth has become wider and the peak has shifted to the lower frequencies. The -3dB bandwidth now spans between 60.25kHz and 121.81kHz. The gain of the filter is determined by connecting the different subsystems together and measuring the output signal of the BPF together with the input signal to the demodulator that is designed in the next chapter.

3.5. Demodulator

After the filtering and amplification of the received signal, the FSK signal has to be demodulated. There are different methods to implement a demodulation system for a FSK signal. The following source describes the general ideas behind FSK demodulation [7]. There are 2 different forms of FSK demodulation that are considered, FM detector demodulators and filter-Type FSK demodulators. The FM detector demodulator treats the FSK signal as a simple FM signal with binary modulation. Filter-type demodulators attempt to optimally match the FSK signal parameters to the demodulator configuration to optimize demodulator error performance. This is done by using very narrowband BPF that are not feasible for this project. Due to the relative

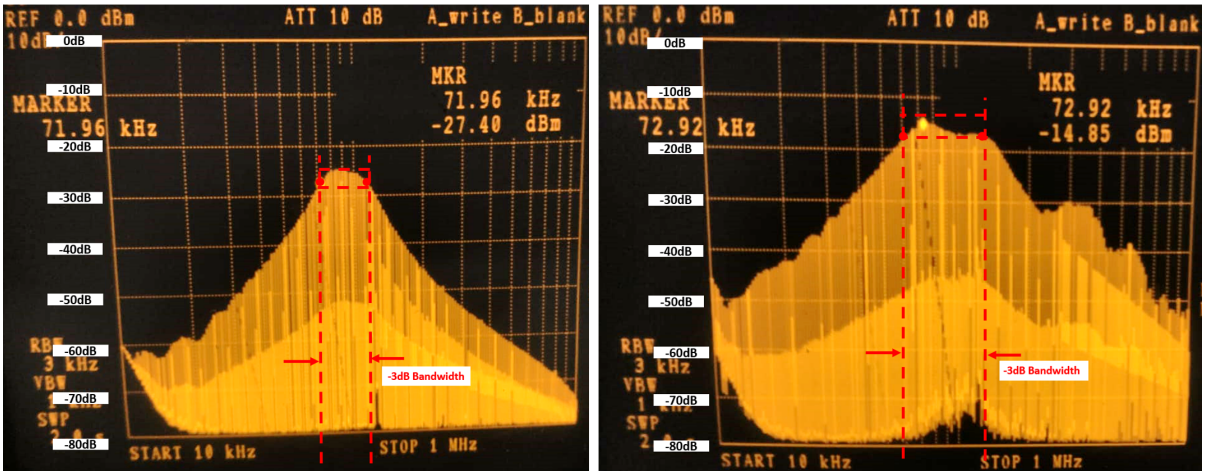

Figure 3.33: Measured frequency spectrum of the BPF without the amplifier stage (left), and the BPF with the amplifier stage (right) .

simplicity of FM detector demodulator this is the preferred option to consider for the system. Nowadays a phase-locked-loop (PLL) demodulator (similar to the FM detector demodulator) is more commonly used.

3.5.1. Demodulation theory

The demodulation technique that is used for this system is a PLL. As can be seen in figure 3.34, this demodulator consists of three parts:

- Phase comparator (PC): A PC gives an output relative to the phase difference between the two input signals
- Low-pass filter
- Voltage controlled oscillator (VCO): A VCO takes an analog voltage level and converts this into square wave with a frequency related to the input level, optimally as linear as possible.

The 4046 PLL ICs series will be used to design the PLL for this system. These ICs come in different versions, this will be addressed later.

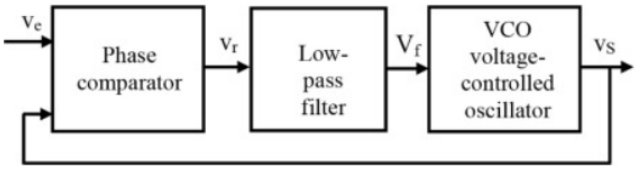

Figure 3.34: Phase locked loop demodulator block diagram.

3.5.1.1. Phase comparator

A PC has a discrete output proportional to the phase difference between two input signals (see Figure 3.35). A lot of different implementations of PC's exist, but the two that are most used are the exclusive-or network and the three-state phase comparator [9]. The advantage of this second PC is that it can differentiate between a phase difference of -90°and 90°. However, for this implementation the PC being able to detect this difference is not of the importance, an exclusive-or network is chosen as a PC because of its higher speed. If it is assumed that average value of the output seen in figure 3.34 is taken, the output voltage of the phase comparator can be written as shown in equation 3.32 [21]. The gain, which will be later used to design the PLL controller can then be written as shown in equation 3.33.

$$V_{PC\_OUT} = \frac{Vcc}{\pi}(\phi_{SIG\_IN} - \phi_{COMP\_IN})[V] \qquad (3.32)$$

$$K_p = \frac{Vcc}{\pi} = \frac{5}{\pi}[V/\text{rad}] \qquad (3.33)$$

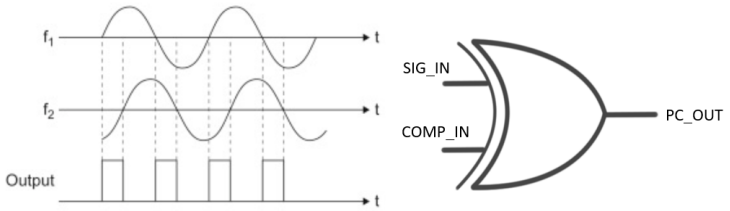

Figure 3.35: The behaviour of a phase comparator.

3.5.1.2. Voltage-controlled oscillator

Next, the VCO has to be designed. A VCO is a oscillator where the frequency is proportional to a input voltage. The 4046 series have a build-in VCO that can be set using external components. A procedure to determine these external component values is given in the following datasheet [27]. In accordance to figure 3.40 the values are determined. R2 together with C1 determines the lower limit of the frequency. The ratio of R1 over R2 then determines the higher limit of the oscillating frequency. The required parameters as defined in figure 3.36 and the determined component values are given in table 3.5. These parameters were partly determined by precisely reading out a graph in the datasheet [27]. For this reason both R1 and C1 will be made tunable in the final design in order to correctly calibrate the VCO. The gain of this VCO can be written as shown in equation 3.34.

$$K_v = \frac{\Delta\omega}{\Delta V} = \frac{2f_L \cdot 2\pi}{V_{IN\_max} - V_{IN\_min}} = \frac{2 \cdot 5000 \cdot 2\pi}{5 - 0.9 - (0 + 0.9)} = 19.6 \cdot 10^3 \ \text{[rad/s/V]} \tag{3.34}$$

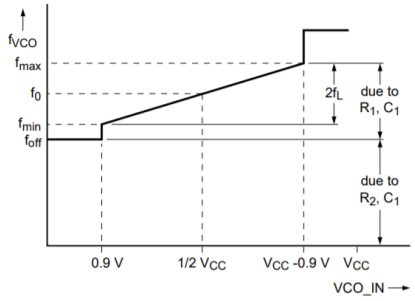

Figure 3.36: Definition of the parameters needed to calibrate the VCO.

Table 3.5: This table contains the values of the components to calibrate the VCO

Required paramters		**Determined parameters**	
f_{min}	82.5kHz	R_1	300kΩ
f_{max}	92.5kHz	C_1	500pF
$f_l = \frac{(f_{max} - f_{min})}{2}$	5kHz	R_2	100kΩ
$f_o = \frac{(f_{max} + f_{min})}{2}$	87.5kHz		

3.5.1.3. Loop filter design

To complete the PLL design the final element that has to be designed is the loop-filter. The function of this loop-filter is to remove the ripple in the output of the PC in order for the VCO to function properly. The loop-filter, however, needs to be designed such that the PLL has an impulse response that doesn't have a too high ripple but is still able to quickly react to changes in the input frequency. There are a lot of possible possible implementations for a loop-filter for a PLL [2]. It was chosen to use a passive lag-lead filter because of its relatively easy design (see Figure 3.37). Compared to a simple low-pass RC filter it implements an extra zero which gives extra freedom when designing for the impulse response.
The voltage gain of this loop-filter can be written according to equation 3.35. Then, using figure 3.34 the open-loop gain can be written as shown in equation 3.36.

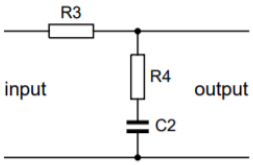

Figure 3.37: Circuit diagram of the lead-lag filter implemented as loop filter.

$$K_f(s) = \frac{1 + R4 \cdot C2 \cdot s}{1 + (R3 \cdot C2 + R4 \cdot C2)s} = \frac{1 + \tau_2 s}{1 + (\tau_1 + \tau_2)s} \quad (3.35)$$

$$H_o(s) = K_p \cdot K_f(s) \cdot K_v / s \quad (3.36)$$

The extra division by the complex variable s is to be able to connect the frequency output of the VCO to the phase input of the PC. There is no feedback gain, this means the closed-loop gain of the PLL can be written as (see Equation 3.37):

$$H(s) = \frac{H_o(s)}{1 + H_o(s)} = \frac{K_p \cdot K_f(s) \cdot K_v / s}{1 + K_p \cdot K_f(s) \cdot K_v / s} = \frac{K_p \cdot \frac{1+\tau_2 s}{1+(\tau_1+\tau_2)s} \cdot K_v / s}{1 + K_p \cdot \frac{1+\tau_2 s}{1+(\tau_1+\tau_2)s} \cdot K_v / s} = \frac{(1+\tau_2 s)K_v K_p}{s^2 + \frac{1+K_v K_p \tau_2}{\tau_1+\tau_2} s + \frac{K_v K_p}{\tau_1+\tau_2}} \quad (3.37)$$

When comparing the denominator of this closed-loop gain with the standard characteristic equation: $s^2 + 2\zeta\omega_n s + \omega_n^2$, equations for the parameters of the natural frequency (ω_n) and damping value (ζ) can be extracted (see Equation 3.38 and 3.39).

$$\omega_n = \sqrt{\frac{K_v K_p}{\tau_1 + \tau_2}} \quad (3.38)$$

$$\zeta = \frac{1 + K_p K_v \tau_2}{2 \cdot \omega_n (\tau_1 + \tau_2)} \quad (3.39)$$

The values for the natural frequency and the damping factor can be acquired from requirements for the impulse response to a change in frequency. These requirements are the maximum overshoot and the 2% settling time (when the overshoot becomes less then 2%). For the maximum overshoot a value of 8% is required to not exceed the boundaries of the VCO. For the 2% settling time it is desired that at 50% of a bit width the system is settled, for that reason this settling time is set at 0.5ms for a baud rate of 1 kbps. The overshoot and natural frequency can then be calculated using equations 3.40 and 3.41 [3].

$$\zeta = \sqrt{\frac{\ln(\frac{O_{\%}}{100})}{\pi^2 + \ln(\frac{O_{\%}}{100})^2}} = 0.63 \quad (3.40)$$

$$\omega_n = \frac{4}{\zeta \cdot t_s} = 12.7 \text{ krad/s} \quad (3.41)$$

The resulting impulse response is given in figure 3.38. There are now 2 equations (3.38 and 3.39) with 2 unknowns. Solving these results in $\tau_1 = 125.8\mu$s and $\tau_2 = 67.2\mu$s. When taking C2 to be 10 nF this results in R3= 12.6k Ω and R4 = 6.72k Ω in accordance to figure 3.40.

3.5.1.4. Schmitt-trigger

The output of the PLL won't be a perfect square wave, but rather a sloped wave oscillating between 2 discrete voltage levels. For the MCU it is desired to input a square wave with 5V representing a binary '1' and 0V representing a binary '0'. For this conversion a schmitt-trigger comparator can be used (see Figure 3.39). The high-level and low-level voltages can be determined using equations 3.42 and 3.43 [8]. The exact values will be determined with the exact measurements of the output of the PLL.

$$V_{th\_low} = \frac{R_3}{R_3 + R_4} V_{cc} - \frac{R_1}{2R_2} V_{out} \quad (3.42)$$

$$V_{th\_high} = \frac{R_3}{R_3 + R_4} V_{cc} + \frac{R_1}{2R_2} V_{out} \quad (3.43)$$

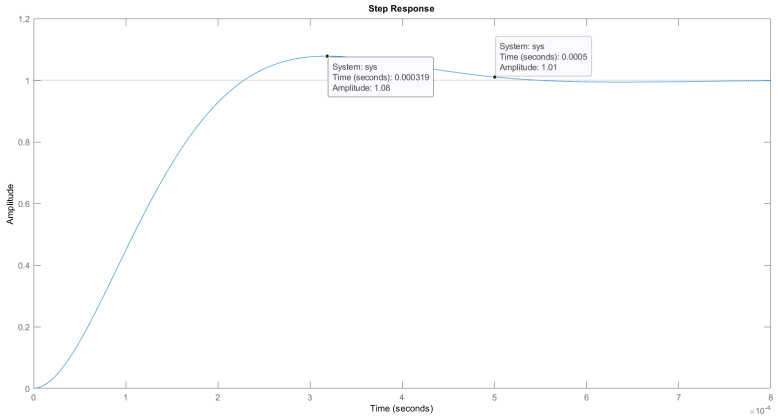

Figure 3.38: The impulse response complies with requirements for overshoot and settling time. Simulated with MATLAB.

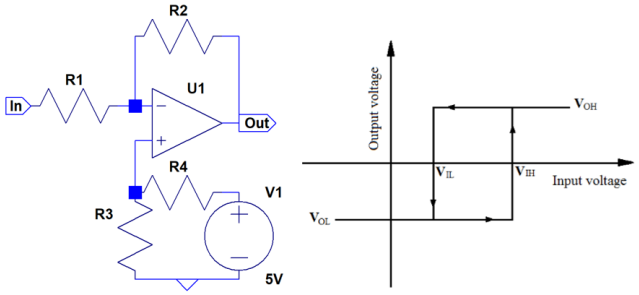

Figure 3.39: Left: the circuit diagram of a standard non-inverting Schmitt-trigger circuit with offset. Right: the voltage transfer of the Schmitt-trigger, with the high-level and low-level threshold voltages.

3.5.2. Simulation

The circuit of the PLL (see Figure 3.40) was first simulated in LTspice. The demodulator circuit was connected to an ideal FSK modulator. The results of this simulation can be seen in figure 3.41, as can be seen from the simulation results it works quite well. A tolerance analysis was done in LTspice, this can be found in Appendix A.2.3.

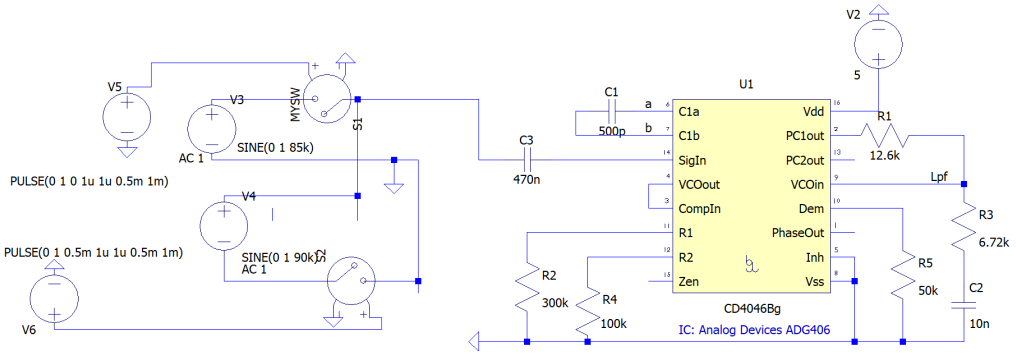

Figure 3.40: The circuit of the PLL simulated using the CD4046 PLL IC.

3.5.3. Building and validating the system

The circuit was built on a perfboard and tested using the CD4046 IC. The PLL was in this test directly connected to a signal generator generating a FSK signal at 500bps. It however, did not seem to give entirely correct results as the transition time from high to low was quite high (see Figure 3.42). This would result in a wrong duty cycle and would give issues when communicating. It was therefore decided to use the more

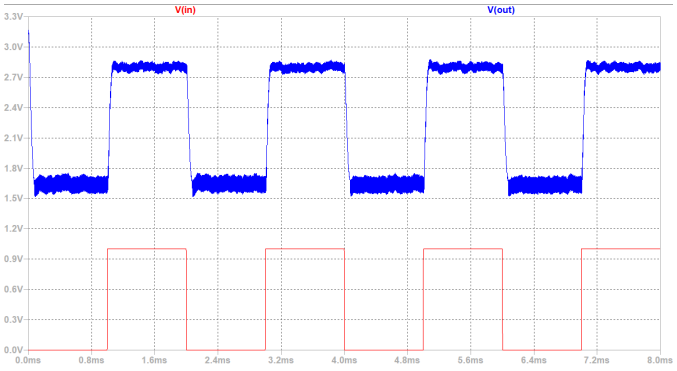

Figure 3.41: The simulation results of the demodulator. The red line indicates the bit sequence given as input of the FSK modulator. The blue line represents the output of the PLL.

newer version of this IC, the 74HC4046. This IC has an improved VCO and PC, but was more difficult to implement because of it only coming in an SMD package. This seemed to give a lot better results (see Figure 3.42). Finally, for the design of the Schmitt-trigger figure 3.42 can be used to extract threshold voltages. Using equation 3.42 and 3.43 it was determined that R1=10kΩ, R2=2kΩ, R3=10kΩ, R4=10kΩ (see Figure 3.39), which resulted in $V_{th_{low}} = 2V$ and $V_{th_{high}} = 3V$. During testing the PLL output became unstable when loaded, even for very high loading impedances. For this reason an extra buffer stage was added between the PLL and the Schmitt-trigger. For both these subsystem circuits the AD820 was used. The final built prototype contained both PLL ICs, switching between these is done using jumper connectors (see Figure 3.43).

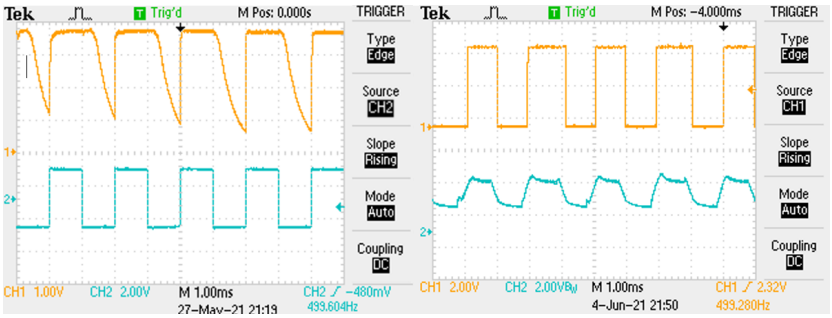

Figure 3.42: Left: the measurements of the PLL using the CD4046 IC, the blue wave represents the input bit sequence, the yellow wave represents the output of the PLL. Right: the measurements of the PLL using the 74HC4046, the yellow wave represents the input bit sequence, the blue wave represents the output of the PLL.

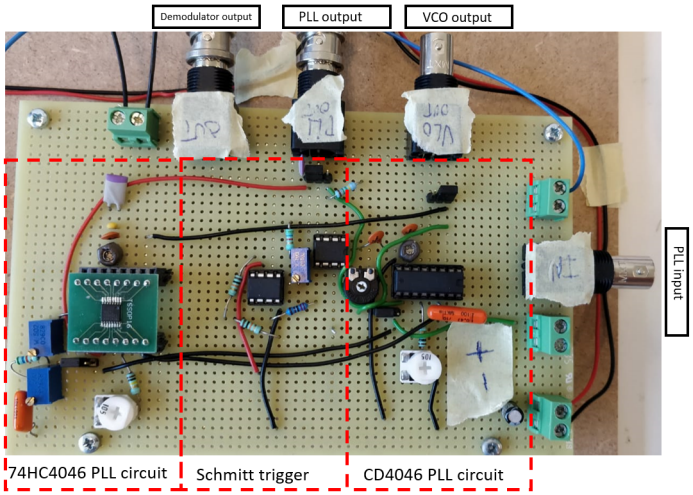

Figure 3.43: The demodualtor was built using two different PLL ICs, switching between these is done using jumper connectors.

3.6. MCU and communication protocol

This section will discuss the MCU that is responsible for sending and receiving the digital communication signals. The MCU that is used is the ESP8266. Appendix B.1 lists the communication protocol and the different data signals that should be send through the system, as well as the proposed data package sent using the Manchester encoding in more detail. As an additional topic to this thesis a method to detect and correct bit errors is implemented to lower the BER. In order to achieve a lower BER a bit error has to be detected by the MCU and correction needs to be taken place whenever possible.

3.6.1. Bit error detection and correction

The system is not perfect, this means a bit error can occur every once in a while. In order to cope with these bit errors a detection and correction system is implemented. The following source gives an overview of a few different detection techniques, such as repetition, parity, checksum and CRC [24]. For the correction, the main two methods are automatic repeat request codes (ARQ), for bidirectional communication and forward error correction codes (FEC), for unidirectional systems. The prototype consists a unidirectional system, for this reason an FEC bit repetition detection and correction will be implemented. Repetition is known as an inefficient, but relatively easy to implement bit error detection method where a single bit is sent multiple times and at the receiver side the hamming distance is determined to recover the signal. With this technique bit errors of 1 bit within these 3 bits can still be corrected. This, however, requires the data part of the package to become three times as long. Because in the tiny house community data only has to be sent up to every 5 minutes, this is not an issue. Combining the information from Appendix B.1 and the repetition coding the package length for the system to be sent can now be calculated to be:

$$\text{Bits}_{\text{total}} = (14 \cdot 2) + (2 \cdot 2) + (3 \cdot 2 \cdot 40) + 3 = 275[\text{bits}] \tag{3.44}$$

3.6.2. Implementation

All the MCU code written for the communication protocol can be found in appendix D. The implementation of the Manchester encoding on the ESP8266 MCU's is done using a Manchester encoding library [17]. This library is configured such that it transmits packages as specified in Appendix B.1. The code for the repetition error correction was also implemented in the code. The downside of using this Manchester library is that the baud rate is selectable between only 600bps and 1200bps. According to requirement RQ-NF.PLC.5 a baud rate of 1000bps should be the maximum the system is capable of sending, but as will be later seen in the system validation results the option of a 600bps baud rate gives much better results. The total time it will then take to sent a single package can be calculated as:

$$t_{\text{single\_package}} = \frac{\text{Bits}_{\text{total}}}{\text{Baudrate}} = 0.46[\text{s}] \tag{3.45}$$

This value is acceptable and according to requirement RQ-NF.PLC.4 very sufficient for the tiny house community. The code is written in such a way that the data format as described in the appendix can be directly given as an input in the serial monitor of a PC, and is again printed in the serial monitor at the receiver side in the correct format.

4

Prototyping and system measurements

This chapter will discuss the different system measurements of the prototype system. In order to perform the system measurements, first the transmitter side is measured without the communication channel (powerline) connected to the line driver. Then, the receiver side is measured at the output of the BPF and at the output of the demodulator. Additionally at the end additional white Gaussian noise (AWGN) is added on the powerline using a function generator connected to an additional line coupler circuit, here the goal is to measure the system with additional 75.5dBμV AWGN as a measure of the worst case scenario. Since this is stated in the CELENEC standard to be the maximum allowed disturbance level on the grid. The BER of the system will also be measured for different baud rates and different noise levels. Finally, packages in the correct format are sent from one MCU to another using the code given in Appendix D. For completeness a list of all used equipment is given in appendix F together with a detailed list of all circuit components of the PLC system. Finally, a complete circuit diagram and more detailed pictures of the final prototype system are given in appendix G.

4.1. System measurements

Figure 4.1 shows the measurement setup that is used. The different designed subsystems discussed in the previous chapter are connected to each other and using additional coaxial connections the subsystems can be easily connected to the different measurement tools. The measurements in this section are performed by generating a 5V peak-to-peak square wave on a function generator and connect this signal to the selection pin on the analog multiplexer of the modulator.

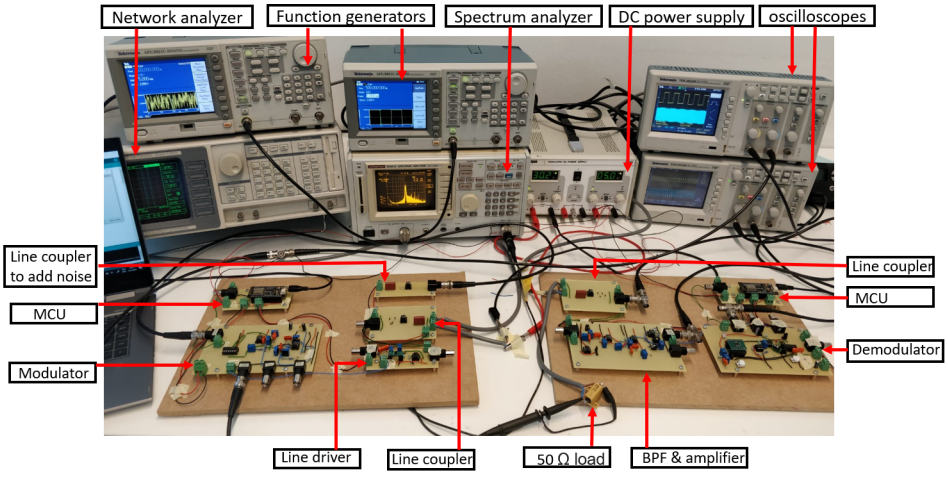

Figure 4.1: Measurement setup of the complete PLC system connected to a 50 meter long powerline. In this particular measurement a function generator generates a sequence of bits to go from the transmitter (left) to the receiver (right) and are picked up again by the oscilloscope. The dual power supply provides 5V to the receiver and transmitter as well as 30V for the powerline. The frequency spectrum at the powerline is measured by the spectrum analyzer. An additional function generator adds extra noise to the cable using an additional line coupler.

Figure 4.2 shows the measured output of the line driver circuit. The measurements show the correct expected behaviour of the line driver. From examining the waveforms no additional distortion is present on the output

wave of the line driver.

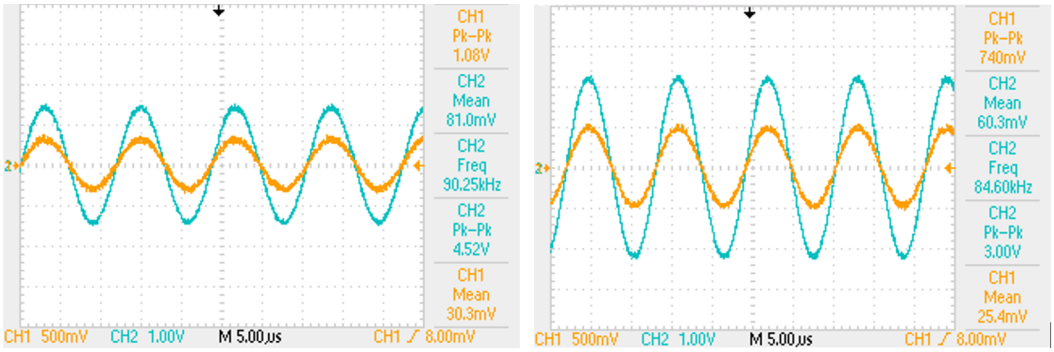

Figure 4.2: Measured signal output of the transmitter side without a channel connected. Left, the space frequency (85kHz). Right, the mark frequency (90kHz). Here the blue waveform is the signal at the input of the line driver and the orange waveform the measured output of the line driver.

Next, the powerline is connected to both line couplers on which a DC voltage of 30V is supplied to a 50 Ω load. The output of the amplifier stage of the BPF is shown in figure 4.3. Here the noisy input signal (line coupler output) of the BPF is shown which is filtered by the BPF and amplified to approximately 1V peak-to-peak for the space frequency by the amplifier stage. Additionally, white noise is added on the channel with a peak-to-peak voltage of 5V to show the filtering capabilities of the filter for white noise. Figure 4.3 shows the measured output signal of the amplifier stage and the input signal of the BPF. From these results it follows that the BPF is able to filter much of the higher frequency noise present in the input signal.

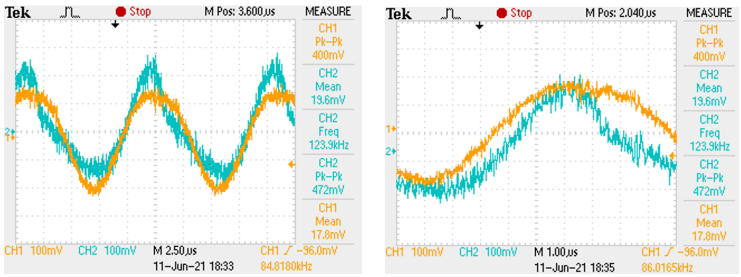

Figure 4.3: Measured signal output of the BPF (orange), compared to the output of the line coupler on the receiver side (blue) with the channel connected and a 50 Ω load. Also AWGN with a peak-to-peak voltage of 5V is added on the channel.

Finally, the output of the demodulator and the output of the Schmitt-trigger stage are measured. Figure 4.4 shows the output waveforms of the output of the demodulator and Schmitt-trigger, here also an instance of a bit error is shown. However, at first sight these bit errors seem to occur relatively infrequent. In the following section the BER is approximately determined by using a MCU. Also, in figure 4.5 the frequency spectrum of the input signal of the demodulator is shown. With the procedure described in appendix E the power of the system is measured to be 148mW for the transmitter side and 145mW for the receiver side.

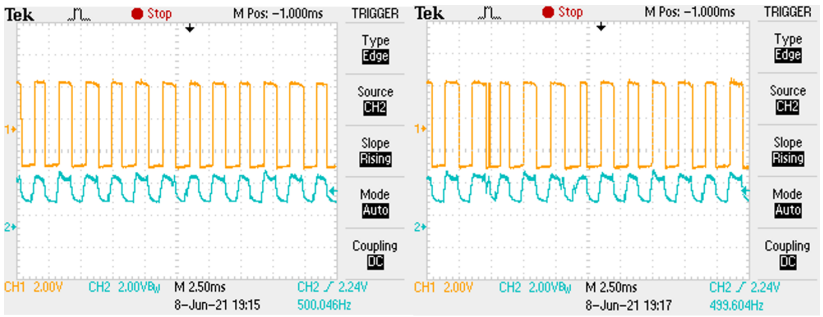

Figure 4.4: Measured signal output of the demodulator (blue), and the measured output of the schmitt-trigger (orange). Left: the correct signal, Right: a bit error error captured in the demodulated signal.

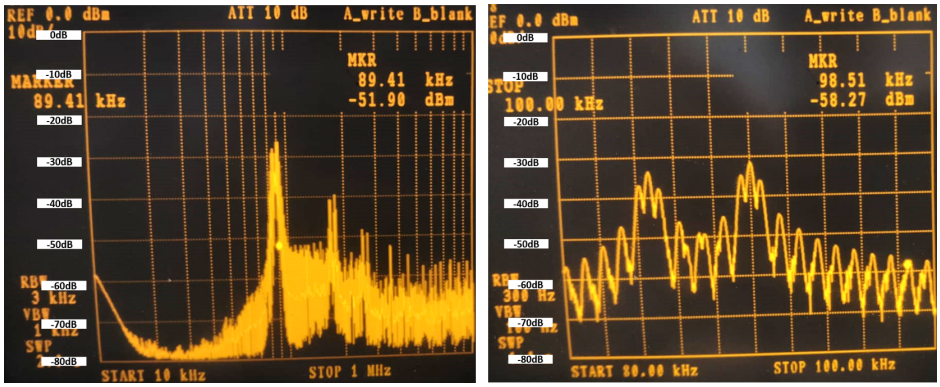

Figure 4.5: Measured frequency spectrum of the input of the demodulator.

4.2. BER measurement communication test

In order to test the communication system properly, the BER is the most important figure of merit to measure. In order to measure the BER a program on the MCU is run that measures the received binary signal compares this to the binary input signal (random sequence of 1's and 0's) and count the amount of single bit errors. For this first measurement the SNR of the system is increased by adding white noise from a function generator and the baud rate of the system is at 1kbps. Initially, the system measured a SNR of 32dB (without added noise). For each measurement a total of 300.000 bits were send, the results are shown in table 4.1. From the results it is evident that the BER does not change (significantly) with the added noise on the channel. Unfortunately, the tools were not available to decrease the SNR even more. Expected is that at some SNR the BER will rapidly increase.

Table 4.1: Measurement results of the BER for different SNR with the system transferring data at 1kbps.

SNR (dB)	Peak-to-peak noise voltage (V)	Amount of bit errors	BER (%)
32	0	3058	1.02
29	10	2926	0.98
26	20	2945	0.98

Next, the BER is determined for different baud rates, here the frequency of error occurring in every 1000 bits send is counted, this to check whether bit errors are distributed randomly or that bit errors mostly consists out of burst errors with multiple errors happening close together. Baud rates between 0.7kbps till 1kbps are measured by sending 880000 random bits. Figure 4.6 shows the results of the measurements. From these measurements it can be concluded that the BER rapidly increases when a baud rate higher than 800bps is used for this system. Also, a normal distribution can be deduced from the measurement of 1000bps which indicates that the bit errors are randomly distributed. As a final test the communication protocol as described in section B.1 was tested including the Manchester coding and the bit error correction using repetition. For the test 100 random packages were sent over the communication line all of which were received correctly.

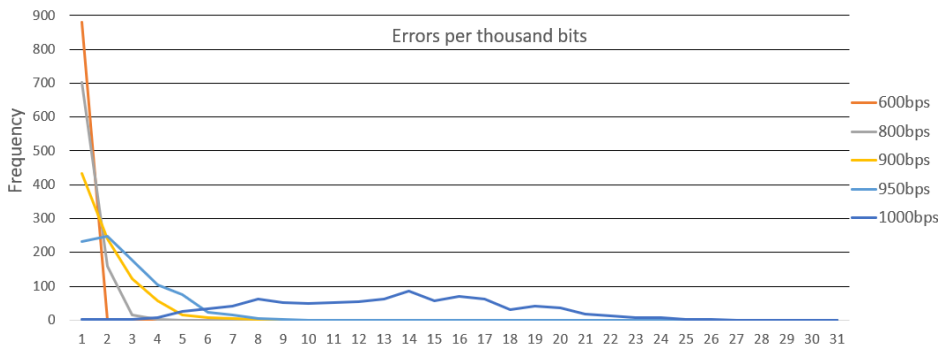

Figure 4.6: The frequency that a certain number of bit errors occurred within 1000 bits sent for different baud rates.

5
Conclusion and Future work

5.1. Conclusion

The goals of this bachelor graduation project was to design and build a prototype PLC system for communication of the DC grid control for a tiny house community. The initially proposed system architecture was correct and provided reliable and fast (according to the requirements) communication. All requirements listed in chapter 2 were thoroughly tested and validated, these results can be found in appendix E. The prototype was tested on a 50 meter long powerline on which a DC voltage of 30V was present. At a baud rate of 600bps, a nearly 0% BER was reached. This falls short from the 1kbps baud rate requirement initially given. The most important requirement, the minimal data rate of 6 bps was however fulfilled and even much higher information speeds up to 80 bps were possible. A final test at 400V could not be done due to both time and resource restrictions, however the system was designed to function on these voltage levels, and theoretically would not pose any significant difference on the system performance. Having followed the CENELEC standard, the maximum transmission voltage level on the powerline was not exceeded. This CENELEC standard also gave a maximum level for the noise present on the powerline which was also tested and seemed to have no severe impact on the performance on the PLC system. The final system measurements of the different subsystems all showed their intended behaviour without any large deviations.
The modulator was able to successfully create a FSK signal that could be digitally operated and produce the required frequencies at 85kHz and 90kHz for the space and mark frequencies respectively. The FSK signal consisted of a very pure sine wave, however due to the implemented switching mechanism there were some sharp discontinuities present in the transition region. The line driver could successfully, without distortion, increase the available signal power of the signal before it was transmitted on the long powerline. An inductive line coupler was designed with a DC blocking capacitor and a transformer winding ratio of $\sqrt{2}$:1 was selected, this resulted in a accurate signal transfer over the communication channel and complete galvanic isolation from the powerline, a protection method was also successfully incorporated.
Next, the BPF and amplifier were successfully designed and build. A 4^{th}order MFB butterworth BPF was designed and gave a sufficient transfer. Testing the system with added noise showed that the filter was able to successfully filter out a large portion of the higher frequency noise as intended. The demodulator was implemented as a PLL and the impulse response requirements were used to correctly determine the values of the components. This implementation was able to correctly demodulate the FSK signal and a Schmitt-trigger was used to convert back to a binary signal. Finally, Manchester encoding to recover the clock was implemented. A correction algorithm using repetition codes, with a bit repetition of 3 was used to further improve the reliability of the PLC system. The power drawn by the complete transmitter is measured to be 148mW and 145mW for the complete receiver.
To conclude, the designed PLC system for use in a tiny house community worked correctly, where almost all requirements were successfully validated.

5.2. Future work

For a final PLC system implementation based on this prototype in the future some additional improvements can be made:

Modulator

The current FSK modulator uses 2 precise tuned Wien bridge oscillators to generate the needed sine waves. In a more practical situation, where this tunability is not needed, a crystal oscillator would yield much more

accurate and reliable performance. Together with a accurate counting network to divide and multiply the oscillation frequency the desired FSK frequencies can be reached more accurately.

Modulation technique
To increase the spectral efficiency of the communication system at the powerline, GFSK and MSK can be implemented (of which the theory can be fond in section 3.1). GFSK could be easily implemented in a future version by using a linear VCO which is also used in the current demodulator design for the PLL. MSK is very hard to implement in analog electronics and digital electronics are necessary to give a good design [26].

Automatic gain control
The exact impedance and attenuation of the signal in the communication channel are not known beforehand, as this varies with different loads and cable lengths. It is therefore desired to implement an automatic gain control (AGC) for both the line driver as well as the receiver amplifier. This AGC system could make sure that the maximum transmission voltage and current is never exceeded. For the amplifier at the receiver side this AGC could make sure that the input voltage levels of the demodulator are within specification. A possible implementation of AGC using CMOS is given in [5].

Improved loop filter
The BER of the system becomes quite high for higher baud rates, and seemed to be independent of the SNR. This indicates that the BER is caused by limitations due to hardware. The demodulator is unable to timely adjust to the frequency change for this higher baud rate. A possible solution for this is to improve the loop-filter. For the loop filter in the PLL of the demodulator a lead-lag filter is now implemented to filter out the ripples of the PC. However, far more complex loop filters can be used such as higher order active loop filters, which could improve the impulse response of the PLL, and improve the performance of the system. An extended theory research on these loop-filters can be found in [2].

Bidirectional communication protocol
The current communication protocol of the prototype would not be able to be implemented in a system where bidirectional communication is needed with multiple receiver/transmitter systems. The current prototype is not able to be silent on the powerline. Therefore a separate enable port on the output of the modulator is needed to stop and start the FSK transmission of the PLC system.
Also, a more robust communication protocol is needed using ARQ instead of FEC in order to reliably start the communication between a receiver and transmitter on the grid. A communication protocol based on stop-and-wait ARQ could be used for a simple but robust implementation to start the communication [18].

DC converters
For this implementation for the grid of the tiny house it is not required for the information of the PLC to go through the DC-DC converters. However, in a future implementation this might be required to get the information also at the lower voltage parts of the grid. For this, additional line couplers and amplifier circuitry can be added to every converter. Also research can be done in using the switching frequency of the converter to implement FSK [28].

A

Appendix A – Noise and tolerance analysis

This appendix will list the noise and tolerance analysis performed on the different PLC subsystems in LTspice. The goal here is to obtain noise levels from the different subsystems and the powerline in order to perform a more accurate simulation of the entire system that will be discussed at the end of this appendix. Different circuit values could be changed during design in case it will yield lower noise and not cause any drawbacks on the functionality of the circuit. The added noise in the system is of special interest to the demodulator, for this a noise source equal to the addition of all noise prior to the input of the demodulator can be added to the demodulator input. This noise can be represented as a additional signal source at the signal input in order to perform a transient simulation while including the present noise floor. Next a tolerance analysis is performed on the different subsystems using Monte Carlo simulations. Here different circuit components will be given a realistic deviation from their nominal values. With this a attempt to achieve more realistic behaviour of the different subsystems is made before the subsystems are build.

A.1. Noise analysis subsystems

A.1.1. Modulator

Now that the basis of the system has been designed in section 3.1.2.4 a noise analysis using LTspice is conducted to tune different component values even further to obtain lower noise. First the noise analysis is conducted on a single Wien bridge oscillator (including the virtual ground), then the noise of the multiplexer is analysed. Since no noise specifications are given in the datasheet of the ADG408. The noise simulation is run on a bandwidth of 1Hz to 200kHz. The circuit used for this simulation is shown in figure A.1, and the simulation results are shown in figure A.2. The total measured RMS noise of the system is 77.3μV. The LT1358 itself produces 8.0$\frac{nV}{\sqrt{Hz}}$ noise, and totals 3.1103μV RMS noise on the measured bandwidth.

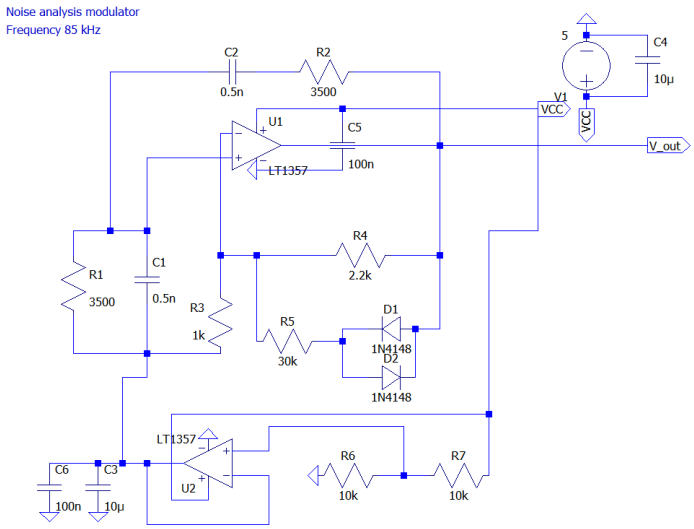

Figure A.1: Circuit used for the noise analysis of the Wien bridge oscillator.

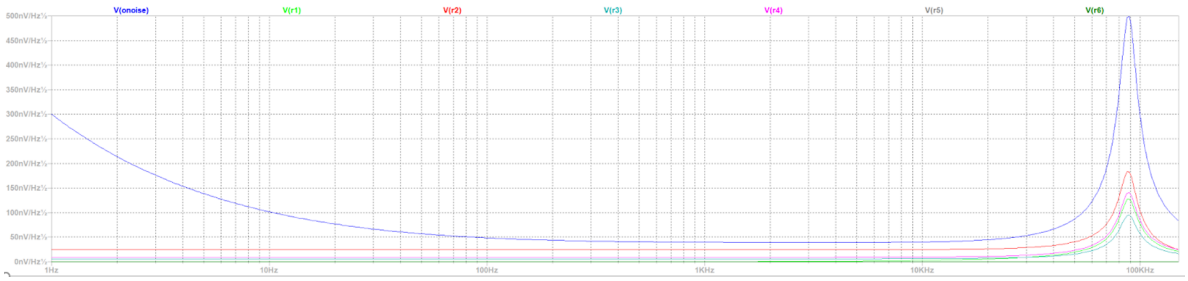

Figure A.2: Measured noise spectrum of the 85kHz wien bridge oscillator, here the noise values are the values referred to the input (the voltage supply).

From the noise analysis it follows that the resistors R1 and R2 contribute to the most noise. Therefore the values of these resistors are lowered while the values of C1 and C2 are increased in order to obtain the correct oscillation frequency. Eventually the resistor values were lowered to 900Ω and the capacitors C1 and C2 were increased to 2nF. The obtained noise analysis is now shown in figure A.3. The total RMS noise is now lowered to 51.125μV.

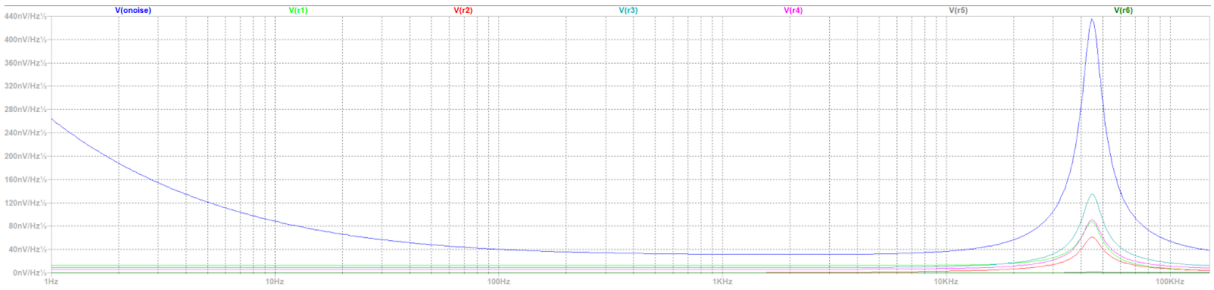

Figure A.3: Measured noise spectrum of the 85kHz wien bridge oscillator after lowering the resistor values in the RC networks.

The same process was performed for the 90kHz wien bridge oscillator, here the resistor values in the RC networks were lowered to 850Ω while increasing the capacitors also to 2nF. Then, the noise analysis was performed on the entire wien bridge oscillators, so consisting of both the 85 and 90kHz tuned oscillators. Now the noise at the output of the 85kHz tuned oscillator is 68.466μV and at the 90kHz output this is 69.885μV. The same noise simulation is now performed on the analog multiplexer for which no signal is put on the data input (see Figure A.4). As expected the obtained noise generated by the multiplexer is very low (therefore is was most likely not noted on the datasheet), the obtained RMS noise of the multiplexer is 442.71nV.

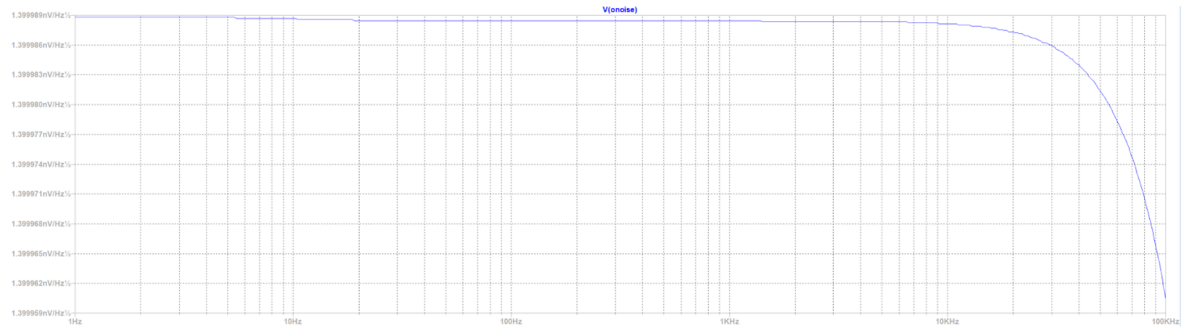

Figure A.4: Measured noise spectrum analog multiplexer.

A.1.2. Line coupler and powerline

In section 3.2 the design of both the communication channel (powerline) and the line coupler are discussed. The noise level present on the powerline was not determined using a simulation but selected according to the literature described in section 3.2. The noise level on the powerline equals 6mV peak-to-peak. The line

coupler circuit consist only of a transformer and diodes. Since the diodes do not conduct under normal operation there is no significant noise that can be generated in the line coupler circuit. The final circuit element is the 50 Ω source resistance of the DC power supply that is added as a load on the powerline, since the resistance is very low compared to all previously used resistors in the circuit design any noise generated by this load can be neglected.

A.1.3. Line driver

In section 3.3 the design, simulation and measurements of the line driver are shown. Here, also a noise simulation was performed. Using the line driver circuit presented in section 3.3 the differential output noise of the two output nodes were simulated, the simulation is performed using the same methods as the previous noise analysis. Figure A.5 shows the simulation results. From the simulation the noises added from the resistors around the line driver circuit show a low impact on the output noise level. The majority of the output noise is thus due to the AD8138 differential driver. In total the rms noise values on both outputs equal 20.267μV and 20.269μV for the high and low side differential outputs respectively.

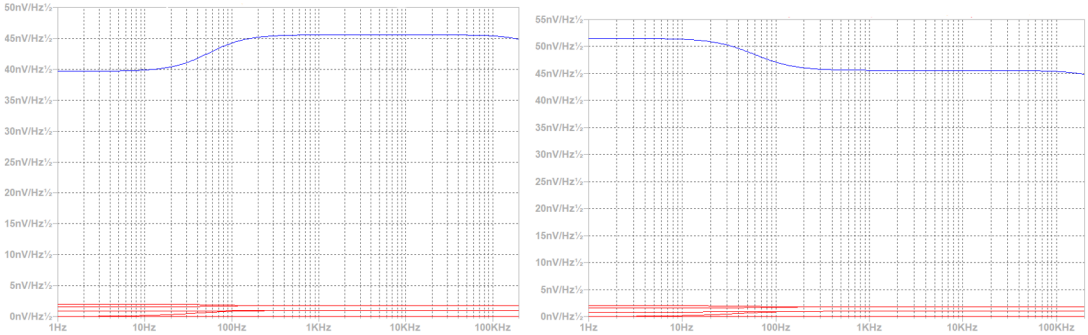

Figure A.5: Measured noise spectrum of the line driver differential output referred to the input of the opamp. Blue is the total noise present at each of the two outputs and the red lines are the noise contributions of the resistors in the network around the line driver.

A.1.4. Band-pass filter and amplifier

The following measurements are taken from the MFB BPF consisting of 2 staggered tuned stages, the amplifier stage and the circuit to provide a virtual ground presented in section 3.4.2.1. The noise analysis is performed again using the same method as described previously. Figure A.6 shows the obtained simulated noise results. The total RMS noise of the output of the system is measured to be 69.82μV_{RMS}. The results show a low noise contributions from both of the filter stages and the largest contribution to the output referred noise is due to the 10KΩ resistors at the virtual ground circuit. Based on these results no change to the circuit values is needed to lower the noise contribution of this circuit.

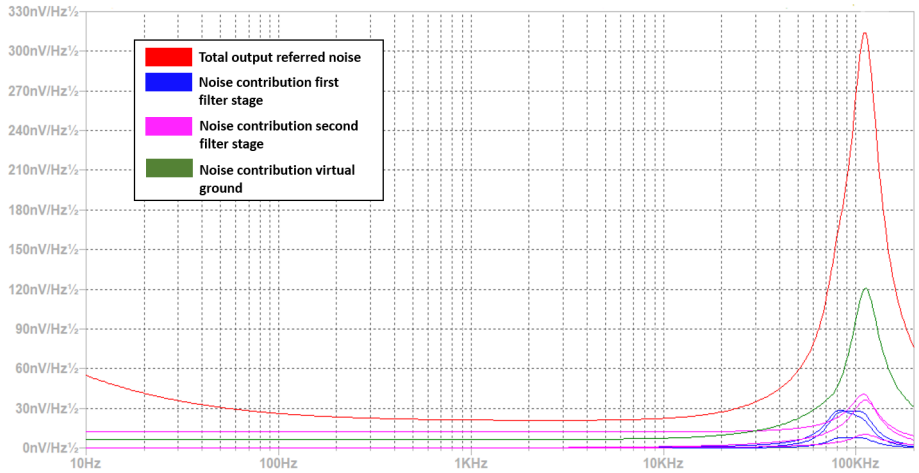

Figure A.6: Noise simulation results for the BPF, for the filter stages the contributions each of the resistor noise is plotted.

A.2. Tolerance analysis subsystems

A.2.0.1. Modulator

Now that the basis of the system has been designed in section 3.1.2.4 a tolerance analysis using LTspice is conducted to determining which component values contribute most to system stability. For the tolerance analysis in this report both a worst case (WC) and Monte Carlo (MC) simulation are considered. With the Monte Carlo method at each simulation run the different circuit components that are set to be varied are varied by a randomly selected values between the nominal value and the defined maximum deviation. As designers of a electrical system the most important tolerance simulation that is of interest is how the system will behave at it's absolute limits defined by the design. As even at a high number of runs the Monte Carl analysis only has a chance to depict the system at it worse it is not the most insightful method. On the other hand there is also the worst case simulation method that does perform this exact simulation however, running such a simulation is not very practical since the amount of runs needed to perform the simulation increases dramatically with the amount of components that are included in the worst case simulation (increasing with 2^n with n the amount of varies components). Thus for simulating the larger parts of the system the Monte Carl simulation method is the most viable option. However a single wien bridge oscillator could in this case be simulated using the worst case simulation method in a relatively short time span. For the tolerance simulation the values of the resistors and capacitors is set at both 10%. LTspice does not native support a worst case simulation method, therefore a function can be implemented in LTspice that is able to perform a worst case analysis with the minimum number of runs, this being 2^n (see Figure A.7) with n the number of components that are variable during the simulation [25].

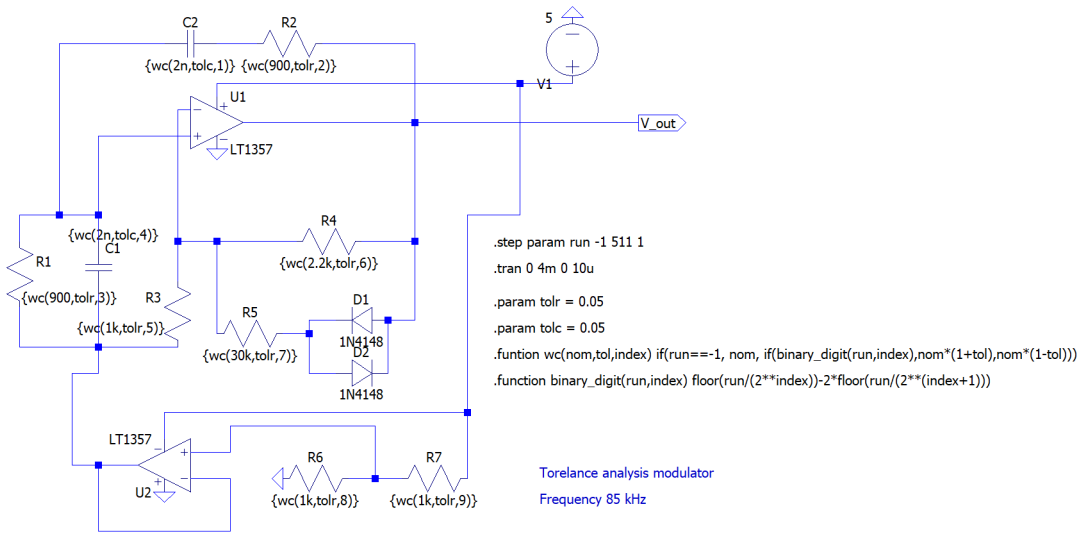

Figure A.7: Simulation results of a single Wien bridge oscillator.

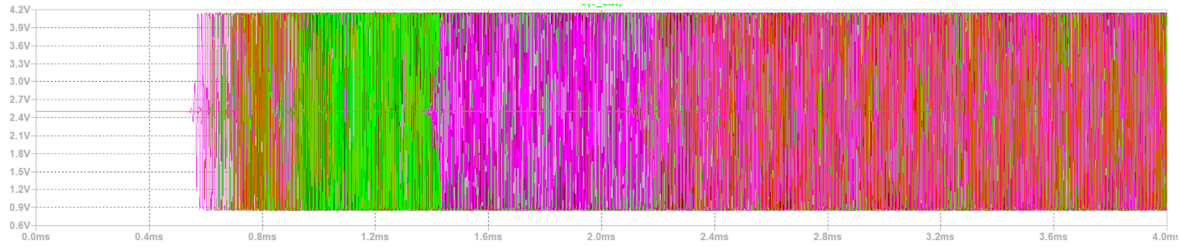

Figure A.8: Simulation results of a single Wien bridge oscillator after a worst case simulation.

The most important observations that had to be made during the simulation the possibility that the gain would reduce too much resulting in an unstable oscillation amplitude or a too large shift in oscillation frequency. After running the worst-case simulation (512 runs) the obtained result did not suffer from any of the 2 problems (see Figure A.8).

A.2.1. Line driver

For performing the tolerance analysis with the line driver circuit presented in section 3.3 the line driver circuit is connected to a sinusoidal voltage source producing a 85kHz sine wave with a 1V peak-to-peak voltage level. The different resistor and capacitor values each have a tolerance value of 10% from their nominal value. A Monte Carlo simulation is run to investigate if the current circuit values are able to not produce any distortions on the output sine wave as shown in section 3.3. Figure A.9 shows the simulation results of the Monte Carlo simulation using 1000 runs. From the results no distortion is visible on the outputs. However the maximum measured voltage deviation between the 1000 runs amounted to a 76.3mV and 80.3mV difference on the high and low differential output side respectively. This however is a relatively large deviation from the intended simulation results presented in section A.9, therefore the resistor values need to be set precisely using multi-turn precision potentiometers and accurately measured to ensure the intended behaviour of the system.

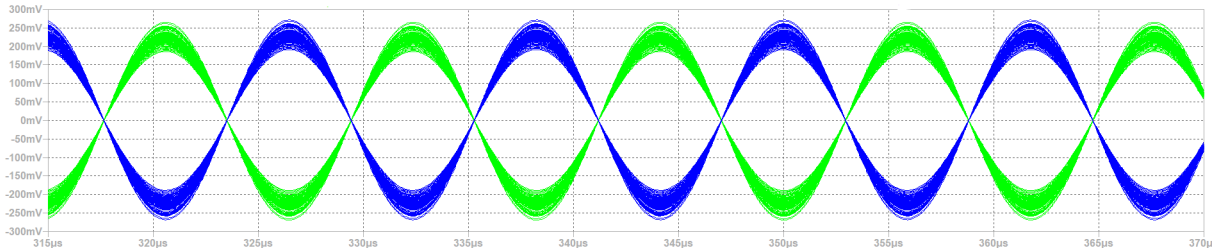

Figure A.9: Simulation results of the tolerance analysis of the line driver using a Monte Carlo simulation with 1000 runs.

A.2.2. Band-pass filter and amplifier

The following measurements are taken from the MFB BPF consisting of 2 staggered tuned stages, the amplifier stage and the circuit to provide a virtual ground presented in section 3.4.2.1. Here, all capacitor and resistor values of the BPF (including the circuit for a virtual ground) are given a 10% tolerance on their nominal values. A Monte Carlo simulation is run for 2000 cycles to obtain the approximated deviation that might occur after the system has been build and measured. This resulted in a maximum variation between 2.8dB and -4.6dB in the pass-band of the filter at 87.5kHz, and a -3dB bandwidth that was span at most between 66.5kHz and 126kHz (see Figure A.10). Which is much wider that ideally designed. Therefore the current design might need additional tuning of the circuit values after the system has been build. However, these results are still considered within the intended behaviour of the BPF since the frequency range of interest (>170kHz) that should be attenuated is still far outside the pass-band region of the filter.

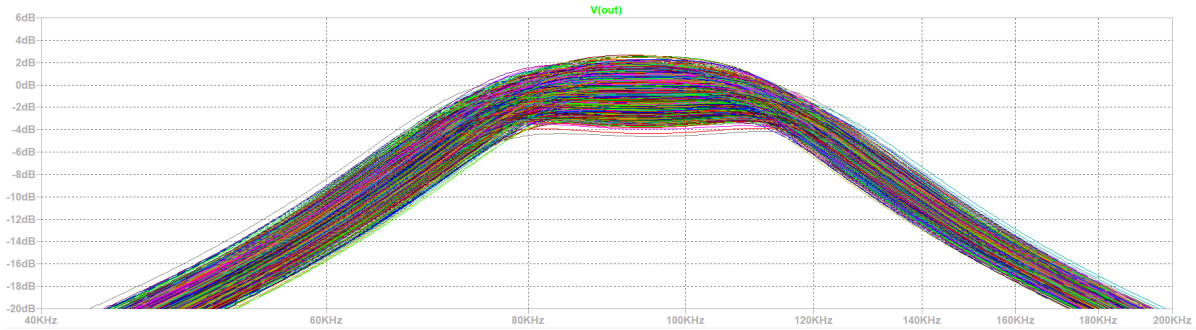

Figure A.10: Tolerance simulation result of the BPF and amplifier circuit using a Monte Carlo simulation with 2000 runs.

A.2.3. Demodulator

Finally, a tolerance analysis using a Monte Carlo simulation is performed on the demodulator circuit presented in section 3.5.2. For this subsystem two Monte Carlo simulation are performed. The different resistor and capacitor values are given to have a tolerance of 5% and 2% respectively. The Monte Carlo simulations are run for 100 runs each (due to long simulation time) and the simulation result is shown in figure A.11. The tolerance simulation shows that even with a very low tolerance level of 2% there still appears one instance

where the PLL was unable to track the frequency of the input wave. The simulation using a more realistic 5% tolerance shows even worse performance. Therefore a lot of tuning a precise measurements of the circuit components is needed when building the system. Furthermore a large deviation between the voltage levels of the demodulated output is visible, therefore the Schmitt-trigger stage described in section 3.5.2 needs to be set accurately based on the measurements taken after the system has been build.

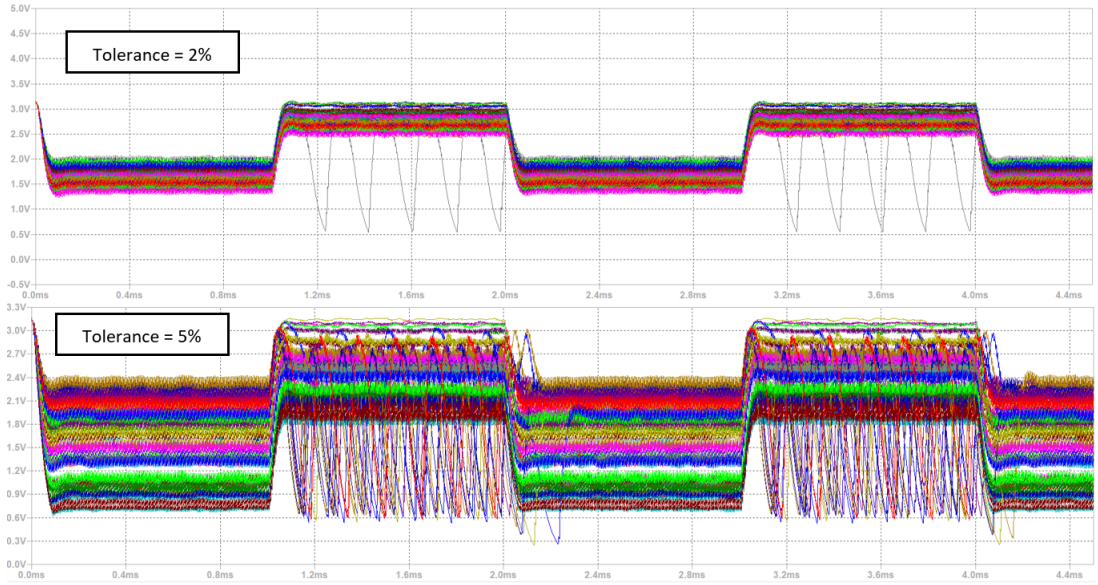

Figure A.11: Tolerance simulation result of the demodulator circuit using a Monte Carlo simulation with 100 runs, top plot has a circuit tolerance of 2% and the bottom plot has a tolerance of 5%

A.3. Total LTspice simulation PLC system

Finally, the entire PLC system is simulated using LTspice according to the system design presented in chapter 3. Additionally a white noise source is added at the input of the demodulator circuit to present a more realistic simulation. The measured RMS values of the noise need first to be converted to a peak value in order to sum the noise contributions and create a white noise source of equal magnitude. The noise amplitude of a (white) noise signal has a probability density function that approximates a Gaussian distribution with a mean value (μ) of 0 and a standard deviation (σ) equal to 1. Because the noise is a random signal the peak to peak value can only be defined. With $\mu = 0$ and within 1 σ around 68.27% of the samples are within the standard deviation. For the system the peak-to-peak value will be defined as 99.9% of all samples within a Gaussian distribution. This equals to 6.6 σ, or in other words within $\mu+3\sigma$ and $\mu-3\sigma$. Therefore the peak-to-peak noise value can be calculated using equation A.1.

$$V_{peak} = 6.6 \cdot V_{RMS} \tag{A.1}$$

From the noise measurements in section A.1 the total peak noise value is calculated by adding the highest output contributions of the different subsystems. This amounts to:

$$V_{peak} = 6.6 \cdot (461.22 \cdot 10^{-6} + 2921.886 \cdot 10^{-9} + 267.54 \cdot 10^{-6} + 460.81 \cdot 10^{-6}) + 6.6 \cdot 10^{-3} = 6.922 \cdot 10^{-3} [V] \tag{A.2}$$

From this result the noise contribution by the powerline causes the largest noise source in the system. This peak value is implemented as a white noise source in LTspice in order to perform a transient analysis with the added noise of the entire system, here all previous subsystems are connected to each other. Figure A.12 shows the noise source that is placed in series with the input signal path of the demodulator. The white noise source that LTspice includes only supports a 1V peak-to-peak value, therefore the source value is scaled to the intended 6.922mV. The term "1000k*time" means that the noise source has a bandwidth of 1MHz.
The system is simulated in LTspice with and without the added noise source. Figure A.13 shows the output of the system with the added noise. Also a simulation without the added noise was run, however no visible

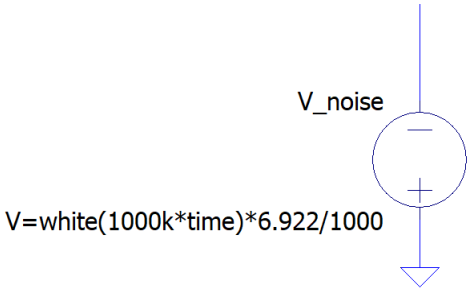

Figure A.12: The implemented noise source at the input of the demodulator to achieve the transient analysis with the total system noise contributions.

deviations from the output signal could be found due to the added noise on the input signal. Therefore it is concluded that the designed system should be able to work reliably after the system has been build.

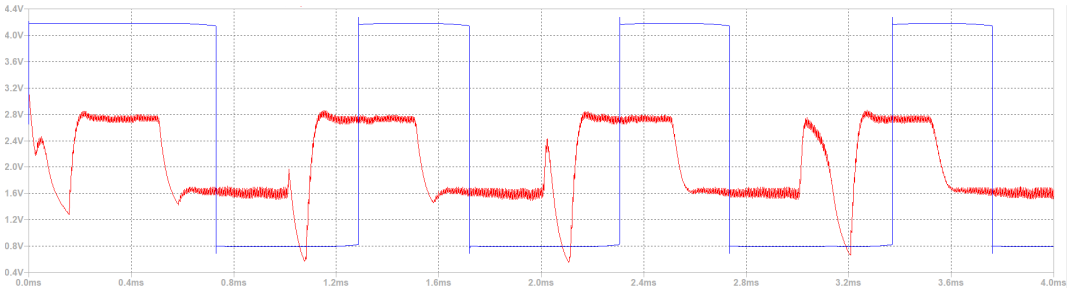

Figure A.13: The simulation results of the output of the demodulator with the added noise source at the input of the demodulator. Here the red trace is the direct output of the demodulator PLL and the blue trace is the output at the schmitt trigger stage.

B

Appendix B – Communication protocol

This appendix will list all information regarding the communication protocol and the signal definitions for all the data that is send through the PLC system.

B.1. Communication signal definition

The data package is split in three parts, the address, the control level and the data. The DC grid of the tiny house community consist of one centralized building where the control system is located together with the larger household appliances. The grid consists of 12 interconnected houses from which different data, such as the total power usage in kWh is measured and stored. These houses each have a unique address for the communication system together with the centralized building. The community also has access to a centralized battery from which the status of the battery has to be communicated to the central control system, this also has a unique address for the communication system. And finally there are 6 wind turbines accessible to the community, here again data and a unique address is needed. In table B.1 the 5 bit addresses of the PLC system are given.

Table B.1: List of all address locations and their 5 bit string

Address bits	Address location
00001	Centralized house
00010	House 1
00011	House 2
00100	House 3
00101	House 4
00110	House 5
00111	House 6
01000	House 7
01001	House 8
01010	House 9
01011	House 10
01100	House 11
01101	House 12
01110	Battery
01111	Wind turbine 1
10000	Wind turbine 2
10001	Wind turbine 3
10010	Wind turbine 4
10011	Wind turbine 5
10100	Wind turbine 6

Next, are the control level bits. The systems uses for all communication a so called "control level" which is a value between 0 and 4. This value represents the importance of the message to the different grid appliances and systems. This value in encoded in a 3-bit binary value where 000 represents 0 and 001 represents 1, and so forth. And finally the data bits, the different grid appliances and houses send different data to and from

the control system, this information is represented by a 32-bit integer value. Figure B.1 shows how the total message looks like for the PLC system. The total message that the PLC system must be able to sent is 40 bits long.

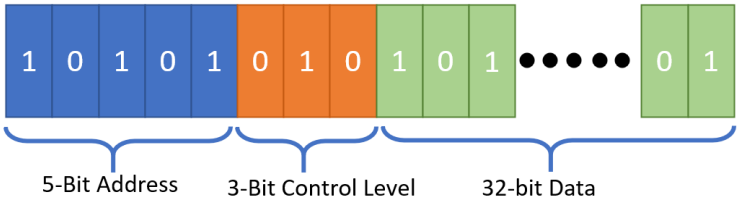

Figure B.1: Layout of the template of the data signal that is send by the PLC system on the DC grid.

Now that the message definition is clear a robust communication protocol is needed to ensure correct and reliable communication on the channel. This prototypes only considers unidirectional communication, in order to ensure a protocol can work on a channel that uses a bidirectional communication system some of the following consideration have to be changed. This will be later discussed in this section. Since the PLC system communicates asynchronous the clock signal is not sent to the receiver. From different measurements taken in Chapter 3 and 4 the duty cycle of the demodulated signal is not always equal to 50% which will make the clock recovery rather difficult. For this reason Manchester encoding will be used where the clock signal is incorporated into the signal. Disadvantages of this encoding is that the effective symbol-rate will be halved. Since information from the houses and devices only has to be updated every hour this won't give any limitations. In order for the receiver to synchronize with the transmitter clock first 14 sequences of '10' are send. After these sequence it is ended with a single '01' sequence after which the data is send. At the end of the sequence 3 consecutive '0' are sent to terminate the transmitting sequence. The proposed communication protocol is shown in figure B.2. The total bits needed to be sent over the system can be calculated as:

$$Bits_{total} = 14 \cdot 2 + 2 \cdot 2 + 2 \cdot 40 + 3 = 115 bits \tag{B.1}$$

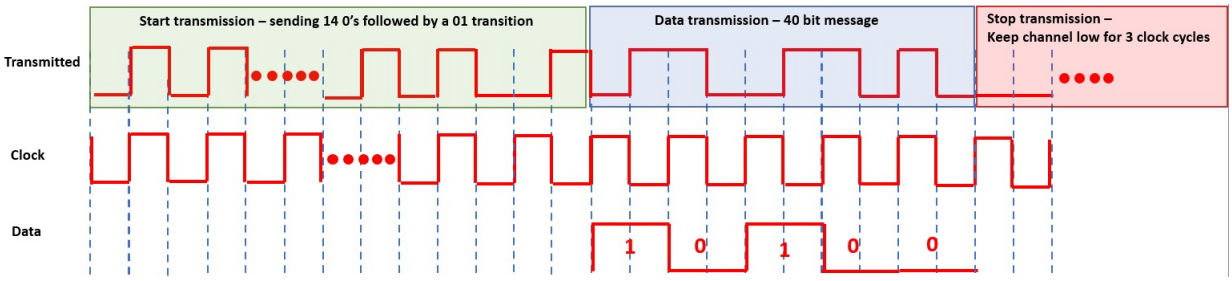

Figure B.2: Picture of the proposed communication protocol that will run on the MCU using Manchester encoding.

B.1.1. Bidirectional communication

In this prototype only unidirectional communication was considered, but in the final system for the Tiny-House community a bidirectional communication system should be implemented. The best method to implement this is by using a "master-slave" system where the master is the main control unit which requests sends and requests information from the houses, windmills and the battery. For this the data package as described above does not have to be altered. The 32-bit of data can be used by the master to request certain information. In this bidirectional communication system where a request and answer needs to be conducted every to 19 devices every 5 minutes (to achieve correct control of the DC grid), the symbol rate can be calculated and rounded up as:

$$\text{symbolrate} = \frac{symbols}{time} = \frac{2 \cdot 19 \cdot 40}{5 \cdot 60} = 6 \text{ symbols/second} \tag{B.2}$$

C

Appendix C – Butterworth design table

The following table given in this appendix is used in chapter 3.4 in order to design the active MFB BPF filter. The table shows all the butterworth coefficients for different higher order butterworth polynomials [33].

ORDER	SECTION	REAL PART	IMAGINARY PART	F_o	α	Q	-3 dB FREQUENCY	PEAKING FREQUENCY	PEAKING LEVEL
2	1	0.7071	0.7071	1.0000	1.4142	0.7071	1.0000		
3	1	0.5000	0.8660	1.0000	1.0000	1.0000		0.7071	1.2493
	2	1.0000		1.0000			1.0000		
4	1	0.9239	0.3827	1.0000	1.8478	0.5412	0.7195		
	2	0.3827	0.9239	1.0000	0.7654	1.3065		0.8409	3.0102
5	1	0.8090	0.5878	1.0000	1.6180	0.6180	0.8588		
	2	0.3090	0.9511	1.0000	0.6180	1.6182		0.8995	4.6163
	3	1.0000		1.0000			1.0000		
6	1	0.9659	0.2588	1.0000	1.9319	0.5176	0.6758		
	2	0.7071	0.7071	1.0000	1.4142	0.7071	1.0000		
	3	0.2588	0.9659	1.0000	0.5176	1.9319		0.9306	6.0210
7	1	0.9010	0.4339	1.0000	1.8019	0.5550	0.7449		
	2	0.6235	0.7818	1.0000	1.2470	0.8019		0.4717	0.2204
	3	0.2225	0.9749	1.0000	0.4450	2.2471		0.9492	7.2530
	4	1.0000		1.0000			1.0000		
8	1	0.9808	0.1951	1.0000	1.9616	0.5098	0.6615		
	2	0.8315	0.5556	1.0000	1.6629	0.6013	0.8295		
	3	0.5556	0.8315	1.0000	1.1112	0.9000		0.6186	0.6876
	4	0.1951	0.9808	1.0000	0.3902	2.5628		0.9612	8.3429
9	1	0.9397	0.3420	1.0000	1.8794	0.5321	0.7026		
	2	0.7660	0.6428	1.0000	1.5320	0.6527	0.9172		
	3	0.5000	0.8660	1.0000	1.0000	1.0000		0.7071	1.2493
	4	0.1737	0.9848	1.0000	0.3474	2.8785		0.9694	9.3165
	5	1.0000		1.0000			1.0000		
10	1	0.9877	0.1564	1.0000	1.9754	0.5062	0.6549		
	2	0.8910	0.4540	1.0000	1.7820	0.5612	0.7564		
	3	0.7071	0.7071	1.0000	1.4142	0.7071	1.0000		
	4	0.4540	0.8910	1.0000	0.9080	1.1013		0.7667	1.8407
	5	0.1564	0.9877	1.0000	0.3128	3.1970		0.9752	10.2023

Figure C.1: Butterworth design table[33].

D

Appendix D – MCU code

This appendix shows all the code that is used to transmit a package as described in appendix B.1. It contains Manchester coding as well as repition for the error correction.

D.1. Receiver code

```

/*
 * Receiver function MCU for PLC system
 * Authors: Luuk Pijnenburg and Imad Bellouki
 * Last edited: 12 June 2021
 */
#include <Manchester.h>
#define RX_PIN D3
int bitnummer;
byte received[15];
void setup()
{
  man.setupReceive(RX_PIN, MAN_300);
  man.beginReceive();
   Serial.begin(115200);
  bitnummer = 0;
}

void loop() {
  if (man.receiveComplete()) {
    uint16_t m = man.getMessage();
    man.beginReceive(); //start listening for next message right after you retrieve the message
    Serial.println(m);
    received[bitnummer]=m;
    //do something with your message here
    bitnummer = bitnummer+1;
  }
  if(bitnummer == 15){
    for(int i =0; i<15; i++){
     // Serial.println(received[i]);
    }
    Serial.println("gedecodeerd");
    byte out = byte_decode(received[0],received[1],received[2]);
    Serial.print((out&0b00011111),DEC);
    Serial.print(",");
    Serial.print((out&0b11100000)>>5,DEC);
    Serial.print(",");
    long val = 0;
    val +=  byte_decode(received[3],received[4],received[5]);
    val +=  byte_decode(received[6],received[7],received[8])<< 8;
    val +=  byte_decode(received[9],received[10],received[11])<< 16;
    val += byte_decode(received[12],received[13],received[14])<< 24;
    Serial.println(val);
    bitnummer=0;
  }
}

byte byte_decode(byte a,byte b, byte c){
```

```
    byte out = 0b00000000;
    bitWrite(out,0,bitRead(hamming(a&0b00000111),0));
    bitWrite(out,1,bitRead(hamming((a&0b00111000)>>3),0));
    byte bitintermediate=((a&0b11000000)>>6);
    bitWrite(bitintermediate,2,bitRead(b,0));
    bitWrite(out,2,bitRead(hamming(bitintermediate),0));
    bitWrite(out,3,bitRead(hamming((b&0b00001110)>>1),0));
    bitWrite(out,4,bitRead(hamming((b&0b01110000)>>4),0));
    bitintermediate=((c&0b00000011)<<1);
    bitWrite(bitintermediate,0,bitRead(b,7));
    bitWrite(out,5,bitRead(hamming(bitintermediate),0));
    bitWrite(out,6,bitRead(hamming((c&0b00011100)>>2),0));
    bitWrite(out,7,bitRead(hamming((c&0b11100000)>>5),0));
   return out;
}

byte hamming(byte in){
  byte out=0;
  if(in==0b00000000){
    out=0b00000000;
  }
  if(in==0b00000001){
    out=0b00000000;
  }
  if(in==0b00000010){
    out=0b00000000;
  }
  if(in==0b00000100){
    out=0b00000000;
  }
  if(in==0b00000111){
    out=0b00000001;
  }
  if(in==0b00000110){
    out=0b00000001;
  }
  if(in==0b00000101){
    out=0b00000001;
  }
  if(in==0b00000011){
    out=0b00000001;
  }
  return out;
}
```

D.2. Transmitter code

```

/*
 * Transmitter function MCU for PLC system
 * Authors: Luuk Pijnenburg and Imad Bellouki
 * Last edited: 12 June 2021
 */

#include <Manchester.h>
//define the transmitter pin
#define TX_PIN D3
byte b[3];

void setup()
{
  //setup the baudrate of the transmitter at 600bps
  man.setupTransmit(TX_PIN, MAN_600);
  Serial.begin(115200);
}

void loop() {
```

```
21      if (Serial.available() > 0) {
          // read input according to the data package specified with the address, control and data signals.
23        String address = Serial.readStringUntil(',');
          String control = Serial.readStringUntil(',');
25        String data = Serial.readStringUntil(',');

27        //this piece of code converts the data to 5 separate bytes
          int address2 = address.toInt();
29        int control2 = control.toInt();
          int data2 = data.toInt();
31        byte firstbyte = address2;
          byte control3 = control2;
33        control3 = control3<<5;
          firstbyte = control3 | firstbyte;
35        byte secondbyte = data2;
          byte thirdbyte = data2>>8;
37        byte fourthbyte = data2>>16;
          byte fifthbyte = data2>>24;
39
          //All bytes of data is converted to 3 bytes of data with bit repetition and then sent
41        //according to the manchester encoding
          convert_hamming(firstbyte);
43        man.transmit(b[0]);
          Serial.println(b[0]);
45        man.transmit(b[1]);
          Serial.println(b[1]);
47        man.transmit(b[2]);
          Serial.println(b[2]);
49        convert_hamming(secondbyte);
          man.transmit(b[0]);
51        man.transmit(b[1]);
          man.transmit(b[2]);
53        convert_hamming(thirdbyte);
          man.transmit(b[0]);
55        man.transmit(b[1]);
          man.transmit(b[2]);
57        convert_hamming(fourthbyte);
          man.transmit(b[0]);
59        man.transmit(b[1]);
          man.transmit(b[2]);
61        convert_hamming(fifthbyte);
          man.transmit(b[0]);
63        man.transmit(b[1]);
          man.transmit(b[2]);
65        delay(100);
        }
67    }

69  //this function converts a byte of data into three bytes of data with repetition
    void convert_hamming(byte n){
71    if(bitRead(n,0)==0){
        bitWrite(b[0],0,0);
73      bitWrite(b[0],1,0);
        bitWrite(b[0],2,0);
75    }
      if(bitRead(n,0)==1){
77      bitWrite(b[0],0,1);
        bitWrite(b[0],1,1);
79      bitWrite(b[0],2,1);
      }
81
      if(bitRead(n,1)==0){
83      bitWrite(b[0],3,0);
        bitWrite(b[0],4,0);
85      bitWrite(b[0],5,0);
      }
87    if(bitRead(n,1)==1){
        bitWrite(b[0],3,1);
89      bitWrite(b[0],4,1);
        bitWrite(b[0],5,1);
91    }
```

```
  if(bitRead(n,2)==0){
    bitWrite(b[0],6,0);
    bitWrite(b[0],7,0);
    bitWrite(b[1],0,0);
  }
  if(bitRead(n,2)==1){
    bitWrite(b[0],6,1);
    bitWrite(b[0],7,1);
    bitWrite(b[1],0,1);
  }
    if(bitRead(n,3)==0){
    bitWrite(b[1],1,0);
    bitWrite(b[1],2,0);
    bitWrite(b[1],3,0);
  }
  if(bitRead(n,3)==1){
    bitWrite(b[1],1,1);
    bitWrite(b[1],2,1);
    bitWrite(b[1],3,1);
  }
    if(bitRead(n,4)==0){
    bitWrite(b[1],4,0);
    bitWrite(b[1],5,0);
    bitWrite(b[1],6,0);
  }
  if(bitRead(n,4)==1){
    bitWrite(b[1],4,1);
    bitWrite(b[1],5,1);
    bitWrite(b[1],6,1);
  }
  if(bitRead(n,5)==0){
    bitWrite(b[1],7,0);
    bitWrite(b[2],0,0);
    bitWrite(b[2],1,0);
  }
  if(bitRead(n,5)==1){
    bitWrite(b[1],7,1);
    bitWrite(b[2],0,1);
    bitWrite(b[2],1,1);
  }
  if(bitRead(n,6)==0){
    bitWrite(b[2],2,0);
    bitWrite(b[2],3,0);
    bitWrite(b[2],4,0);
  }
  if(bitRead(n,6)==1){
    bitWrite(b[2],2,1);
    bitWrite(b[2],3,1);
    bitWrite(b[2],4,1);
  }
  if(bitRead(n,7)==0){
    bitWrite(b[2],5,0);
    bitWrite(b[2],6,0);
    bitWrite(b[2],7,0);
  }
  if(bitRead(n,7)==1){
    bitWrite(b[2],5,1);
    bitWrite(b[2],6,1);
    bitWrite(b[2],7,1);
  }
}
```

E

Appendix E – Program of requirements validation

In this chapter the tests needed to validate the requirements are described. Table E.1 shows all the requirements of the subsystem and the requirements of the total system that apply to this subsystem with the corresponding test.

Table E.1: This table shows the tests corresponding to each requirement.

Subsystem requirements			
Requirement	Short description	Tests	Requirement met
RQ-M.PLC.1	Separate TX and RX	No test necessary	Yes
RQ-M.PLC.2	Reliable communication	T1	Partly
RQ-M.PLC.3	Superimpose information carrying signal	T2	Yes
RQ-M.PLC.4	Extract information carrying signal	T3	Yes
RQ-M.PLC.5	SNR larger than unity	T4	Yes
RQ-M.PLC.6	FSK modulation technique	No test necessary	Yes
RQ-S.PLC.1	Active band-pass filter	No test necessary	Yes
RQ-S.PLC.2	Protection circuit	T5	Yes
RQ-S.PLC.3	Implementation on PCB	No test necessary	No
RQ-NF.PLC.1	Minimum distance	T6	Yes
RQ-NF.PLC.2	Correct CENELEC band	T7	Yes
RQ-NF.PLC.3	Maximum transmission voltage level	T2	Yes
RQ-NF.PLC.4	Symbol rate	T8	Yes
RQ-NF.PLC.5	Baud-rate	T1	Partly
RQ-NF.PLC.6	Grid voltage	T9	Not tested
RQ-NF.PLC.7	Supply voltage	T10	Yes
RQ-NF.PLC.8	Maximum power	T11	Yes
Relevant system requirements			
Requirement	Short description	Tests	Requirement met
RQ-M.SYS.1	Communication over powerline from main control	T8	Yes
RQ-M.SYS.6	Communication over powerline to main control	T8	Yes
RQ-NF.SYS.1	Sufficient speed	T8	Yes

E.1. T1: BER test

Requirements to be validated

RQ-M.PLC.2
RQ-NF.PLC.5

Experiment setup

Connect the receiver and the transmitter to the 30V powerline
Connect the MCU to the computer

Power the transmitter and receiver module

Testing method

Run a program that sends and receives random bits
Count how much of these bits arrived successful without any errors
Repeat for different baud-rates

Validation criteria

BER of 10^{-9} for speed of 700 bps, **Partly passed**
BER of 10^{-9} for speed of 800 bps, **Failed**
BER of 10^{-9} for speed of 900 bps, **Failed**
BER of 10^{-9} for speed of 950 bps, **Failed**
BER of 10^{-9} for speed of 1000 bps, **Failed**

Explanation of results

Validation criteria of BER of 10^{-9} not met for speeds larger than 700bps. For speeds below 700bps a BER of maximally 1 in 880000 was determined, but more testing would be necessary to fully validate the requirement. The results of this test are shown in table E.2. The validation criteria for requirement RQ-M.PLC.3 are met for lower baud-rates. The exact baud-rate requirement for RQ-NF.PLC.5 is not met.

Table E.2: BER for different baud-rates

Speed	BER_{max}	BER_{max}**[%]**
700bps	1/880000	0.00011%
800bps	199/880000	0.023%
900bps	788/880000	0.090%
950bps	9112/880000	1,04%
1000bps	10722/880000	1.22%

E.2. T2: Superimpose information signal

Requirements to be validated

RQ-M.PLC.3
RQ-NF.PLC.3

Experiment setup

Connect the transmitter to the powerline of 30V
Connect the function generator to the demodulator
Connect the oscilloscope at AC mode to the powerline

Testing method

Set the function generator to generate a 500Hz square wave

Validation criteria

The 90kHz signal from the transmitter can be seen at the oscilloscope, **Passed**
The 85kHz signal from the transmitter can be seen at the oscilloscope, **Passed**
The peak-to-peak voltage of the 90kHz signal at the DC voltage line is not larger than 1V, **Passed**
The peak-to-peak voltage of the 85kHz signal at the DC voltage line is not larger than 1V, **Passed**

Explanation of results

All validation criteria for requirement RQ-M.PLC.3 and RQ-NF.PLC.3 are met.

E.3. T3: Extract information signal

Requirements to be validated

RQ-M.PLC.4

Required tests to be first validated

T2

Experiment setup

Connect the transmitter to the powerline of 30V
Connect the receiver to the powerline of 30V
Connect the function generator to the demodulator
Connect the oscilloscope at AC mode to the small-signal side of the receiver line coupler

Testing method

Set the function generator to generate a 500Hz square wave

Validation criteria

The 90kHz signal at the receiver line coupler can be seen at the oscilloscope, **Passed**
The 85kHz signal at the receiver line coupler can be seen at the oscilloscope, **Passed**

Explanation of results

All validation criteria for requirement RQ-M.PLC.4 and are met.

E.4. T4: SNR measurement

Requirements to be validated

RQ-M.PLC.5

Experiment setup

Connect the transmitter to the powerline of 30V
Connect the receiver to the powerline of 30V
Connect the function generator to the demodulator
Connect the noise source with the required value to the communication channel
Connect the spectrum analyzer to the small-signal side of the receiver line-coupler.

Testing method

Set the function generator to generate a 500Hz square wave
Measure the SNR by extracting the noise floor amplitude (dB) from the signal amplitude (dB).

Validation criteria

The SNR at the receiver side is larger than unity, **Passed**

Explanation of results

As can be seen in figure E.1 the SNR is larger than unity: 29dB. All validation criteria for requirement RQ-M.PLC.4 are met.

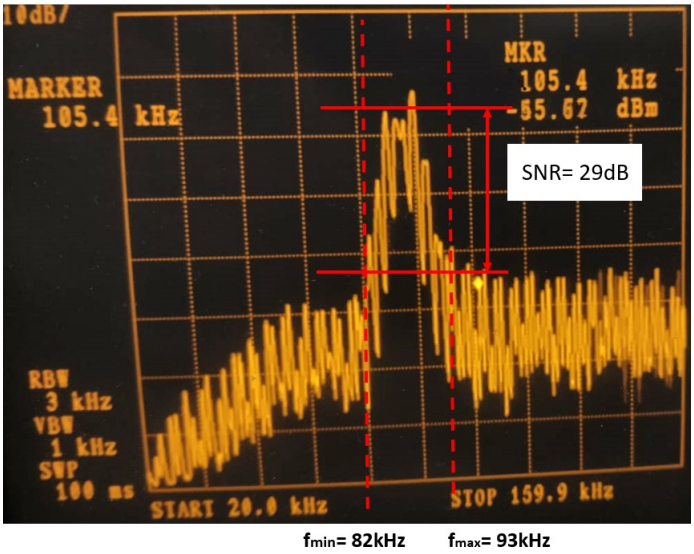

Figure E.1: The measurements of the SNR at the receiver side using the spectrum. The exact frequency band that is taken on the channel is also indicated, and is within the CENELEC requirements.

E.5. T5: Protection circuit

Requirements to be validated

RQ-S.PLC.2

Experiment setup

Connect a line driver to a function generator at the powerline side.
Connect the small-signal side of the line driver to an oscilloscope

Testing method

Set the function generator to generate white noise from 1kHz to 1Mhz.
Steadily increase the amplitude of the white noise

Validation criteria

The signal at the small-signal side of the line coupler never becomes larger than 5V peak-to-peak regardless of amplitude of the noise, **Passed**

Explanation of results

As can be seen in figure E.2 for an input of 20V peak-to-peak noise the amplitude at the small signal line coupler side does not exceed 5V. The requirement validation for requirement RQ-S.PLC.2 are met.

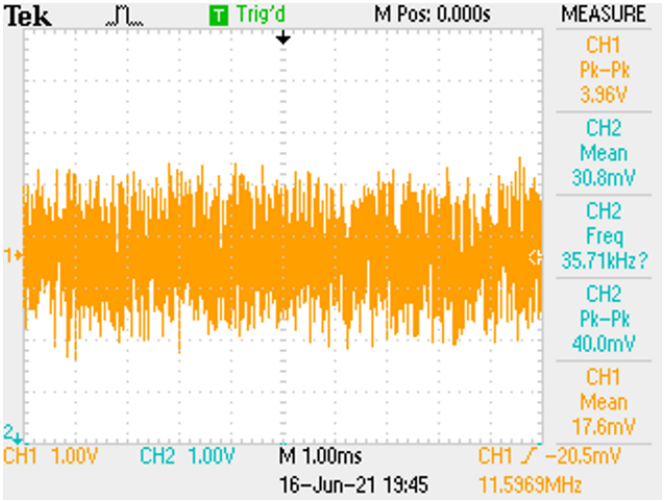

Figure E.2: The measurements of a single line coupler where a 20Vpp random signal was given at its input, as can be seen the 5V limit is not exceeded. It can be concluded that the protection circuit works well.

E.6. T6: Distance

Requirements to be validated

RQ-NF.PLC.1

Experiment setup

Connect both the receiver and transmitter to the powerline

Testing method

Send random bits and measure the BER at a baud rate of 600bps
Measure the BER for different length of the power cable

Validation criteria

No bit errors are measured for a length of 10cm of powercable in 880000 random bits, **Passed**
No bit errors are measured for a length of 50m of powercable in 880000 random bits, **Passed**
No bit errors are measured for a length of 100m of powercable in 880000 random bits, **Could not be tested**

Explanation of results

The test with 100meters could not be conducted because of limited resources. The requirement validations for requirement RQ-NF.PLC.1 are met, the requirement stated 50 metres.

E.7. T7: Transmission band

Requirements to be validated

RQ-NF.PLC.2

Experiment setup

Connect both the receiver and transmitter to the powerline
Connect the function generator to the transmitter side
Connect the spectrum analyzer to the powerline

Testing method

Set the function generator to generate a 500Hz signal

Measure the spectrum of the signal at the powerline

Validation criteria

The band of frequencies send is within the A or B band of the CENELEC standard, between 3kHz and 125kHz, **Passed**

Explanation of results

As can be seen from figure E.1 the band is approximately between 82kHz and 93kHz. The requirement validations for requirement RQ-NF.PLC.2 are met.

E.8. T8: Symbol rate

Requirements to be validated

RQ-NF.PLC.5
RQ-M.SYS.1
RQ-M.SYS.6
RQ-NF.SYS.1

Experiment setup

Connect both the receiver and transmitter to the powerline
Connect the receiver and transmitter MCUs to the PC with the correct code

Testing method

Send a random data package from the sender PC
Measure the transmission time of the random package

Validation criteria

The transmission time of the random package is less than $\frac{300}{2 \cdot 19} = 10.7s$, **Passed**

Explanation of results

The transmission time for one package was measured to be approximately 0.5 seconds. The requirement validations for requirement RQ-NF.PLC.4 and RQ-NF.SYS.1 are met. Although this prototype is not bidirectional it can still be stated that both requirement RQ-M.SYS.1 and RQ-M.SYS.6 are met, communication is possible when two prototypes are used.

E.9. T9: Grid voltage

Requirements to be validated

RQ-NF.PLC.6

Experiment setup

Connect both the receiver and transmitter to the powerline
Connect the function generator to the transmitter side of the powerline

Testing method

Set the function generator to create a 500Hz square wave signal
Check whether this square wave is correctly received at the receiver side
Repeat for different voltages at the powerline side

Validation criteria

The square wave is correctly received for a voltage of 0V at the powerline, **Passed**
The square wave is correctly received for a voltage of 30V at the powerline, **Passed**
The square wave is correctly received for a voltage of 380V at the powerline, **Not conducted**

Explanation of results

Due to limited resources the test with 380V could not be conducted. It can therefore not be said whether the requirement RQ-NF.PLC.4 is met.

E.10. T10: Supply voltage

Requirements to be validated

RQ-NF.PLC.7

Experiment setup

Connect both the receiver and transmitter to the powerline
Connect the receiver and transmitter to a 5V power supply

Testing method

Set the function generator to create a 500Hz square wave signal

Check whether this square wave is correctly received at the receiver side

Validation criteria

The square wave is correctly received for a supply voltage of 5V, **Passed**

Explanation of results

The system functions properly for a supply voltage of 5V. The requirement validations for requirement RQ-NF.PLC.7 are met.

E.11. T11: Power usage

Requirements to be validated

RQ-NF.PLC.8

Experiment setup

Connect both the receiver and transmitter to the powerline
Connect the receiver and transmitter to a 5V power supply
Connect a multimeter for current measurements in series with the power path.

Testing method

Set the function generator to create a 500Hz square wave signal
Check whether this square wave is correctly received at the receiver side

Validation criteria

The power drawn by the transmitter is below 1W, **Passed**
The power drawn by the receiver is below 1W, **Passed**

Explanation of results

The transmitter draws an average 29.69mA of current (148mW), the receiver draws an average of 28.97mA of current (145mW). The requirement validations for requirement RQ-NF.PLC.8 are met.

F

Component and equipment list

This appendix contains a list of all components used in the final implemented prototype in table F.1. Table F.2 lists all the equipment used for measuring the prototype.

Table F.1: Table of all used circuit components of the prototype, corresponding with the circuit diagram shown in appendix G.

Part name	type	value/ Manufacturer	Amount	Subsystem used for
Resistor	metal-film 5%	10kΩ	10	BPF, Virtual ground, schmitt trigger, demodulator
	metal-film 5%	5.6kΩ	1	BPF
	metal-film 5%	1kΩ	3	Amplifier, modulator
	metal-film 5%	100kΩ	1	Demodulator
	metal-film 5%	2kΩ	1	schmitt trigger
	metal-film 5%	30kΩ	2	Modulator
	metal-film 5%	4.7kΩ	1	Demodulator
	metal-film 5%	680Ω	2	Line driver
	metal-film 5%	6.8kΩ	1	schmitt trigger
Potentiometer	Multiturn: 25-turn	5kΩ	15	modulator, BPF, line driver, schmitt trigger, demodulator
	Single turn	250kΩ	1	Amplifier
	Single turn	500kΩ	1	demodulator
Capacitors	Electrolitic	10uF	4	Power stabilization, virtual ground
	ceremamic	100nF	4	Power stabilization, virtual ground
		470nF	3	Line coupler, demodulator
		1nF	4	BPF
		10nF	1	demodulator
		470pF	1	demodulator
		2nF	4	modulator
	Variable prallel plate	100pF	1	demodulator
Transformers	RF transformers	winding ration 1:√2	2	Line coupler
Diodes	N914	ON semiconductors	8	Line coupler
	1N4148	Vishay	4	Modulator
Opamps	LT1358	Analog devices	8	Modulator, virtyual ground, BPF, amplifier, schmitt trigger
	AD802	Analog devices	2	Buffer
	AD8138	Analog devices	1	Line driver
PLL	74HC4046	Nexperia	1	Demodulator
Analog multiplexer	ADG408	Analog devices	1	Modulator
MCU	ESP8266	Firebeetle	2	MCU

Table F.2: List of all used measuring equipment

Equipment model name	Manufacturer	Description
SR770	Stanford research systems	FFT network analyzer
R3361A	Advantest	Spectrum analyzer
AFG4021C	Tektronix	Single channel arbitrary function generator
TDS2022B	Tektronix	Two channel oscilloscope
ZT3202	Aplab	Regulated DC power supply
177	Fluke	True RMS multimeter

G

Total circuit diagram & build system

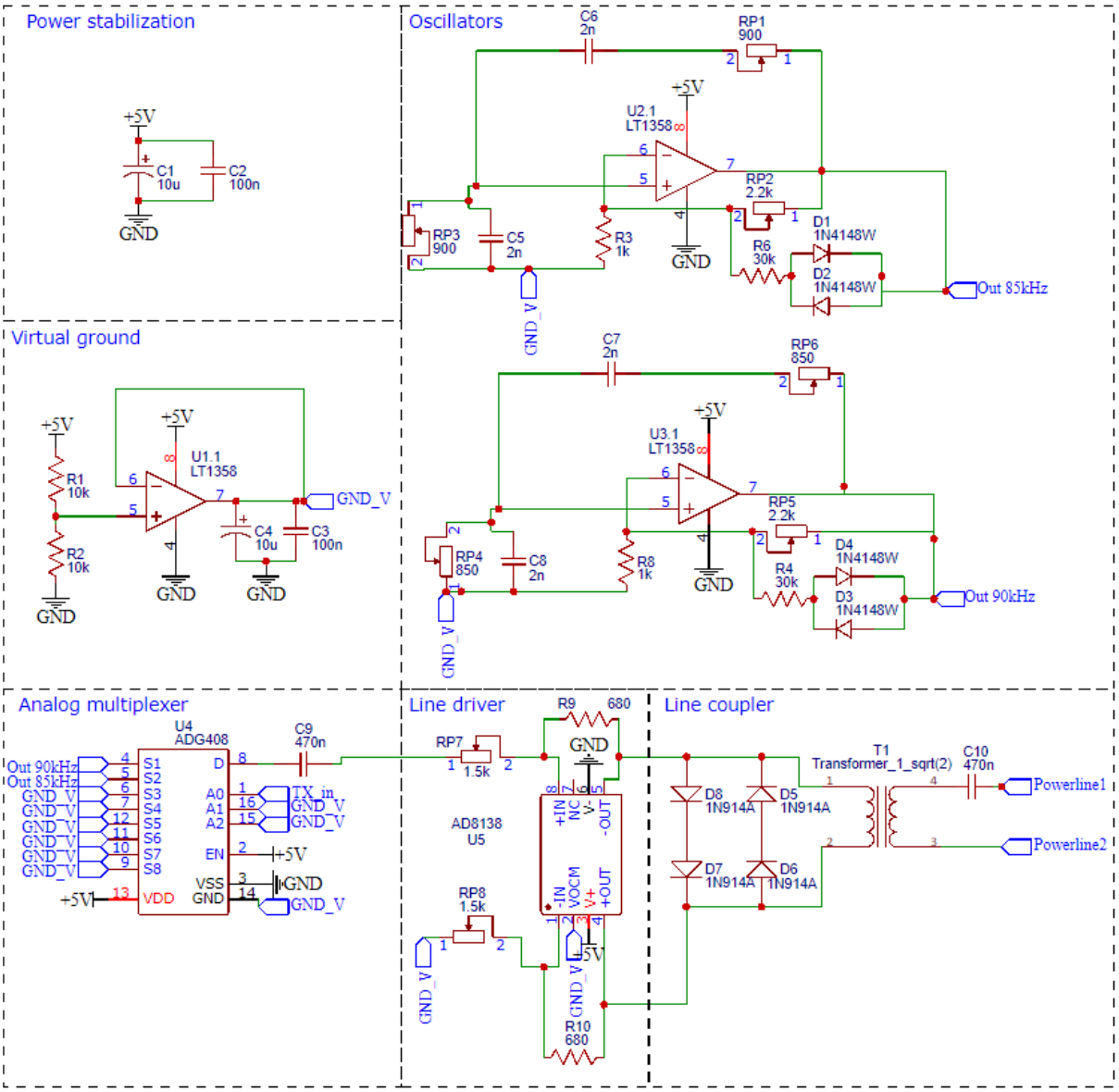

Figure G.1: This figure shows the entire circuit diagram of the final implemented transmitter.

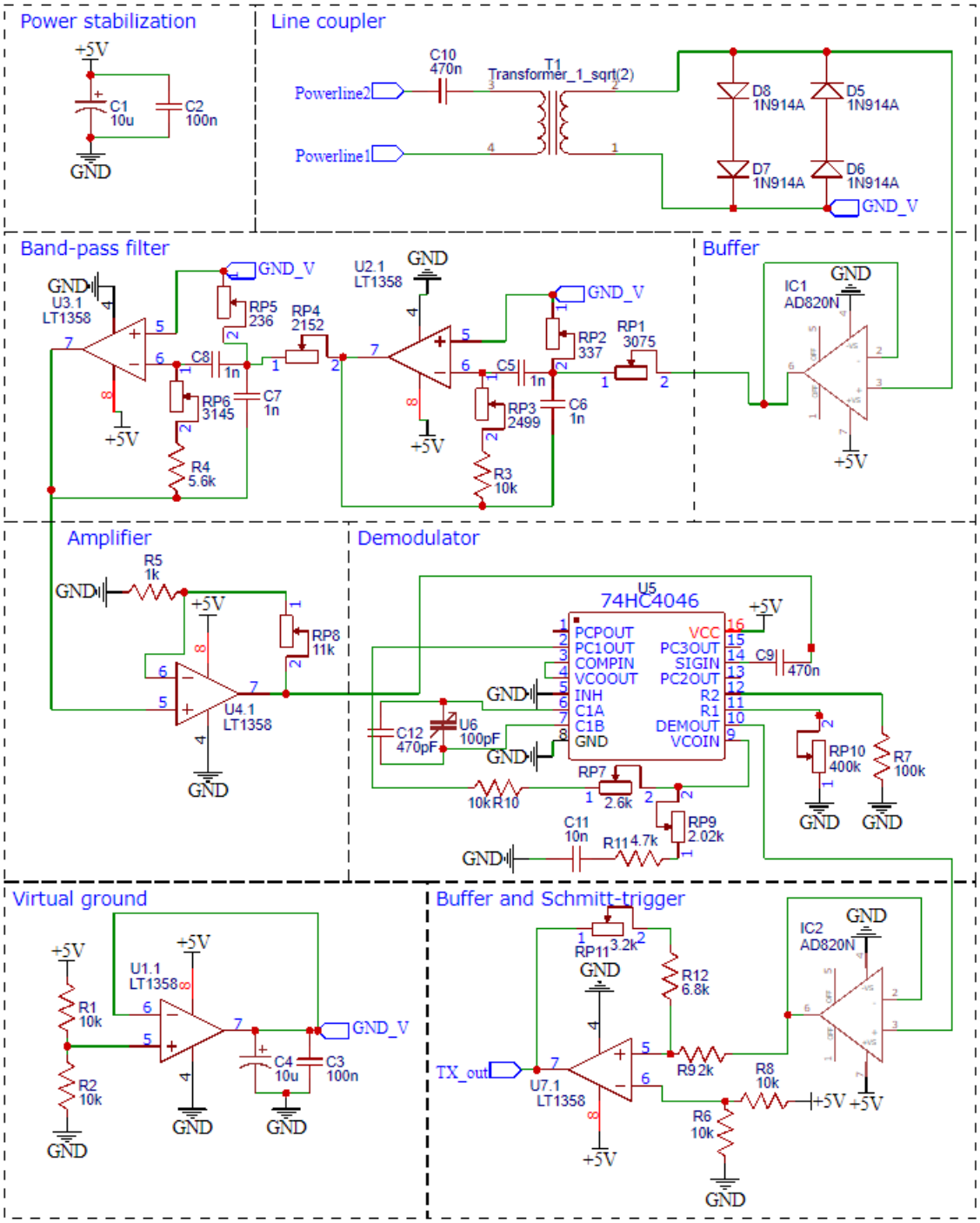

Figure G.2: This figure shows the entire circuit diagram of the final implemented receiver.

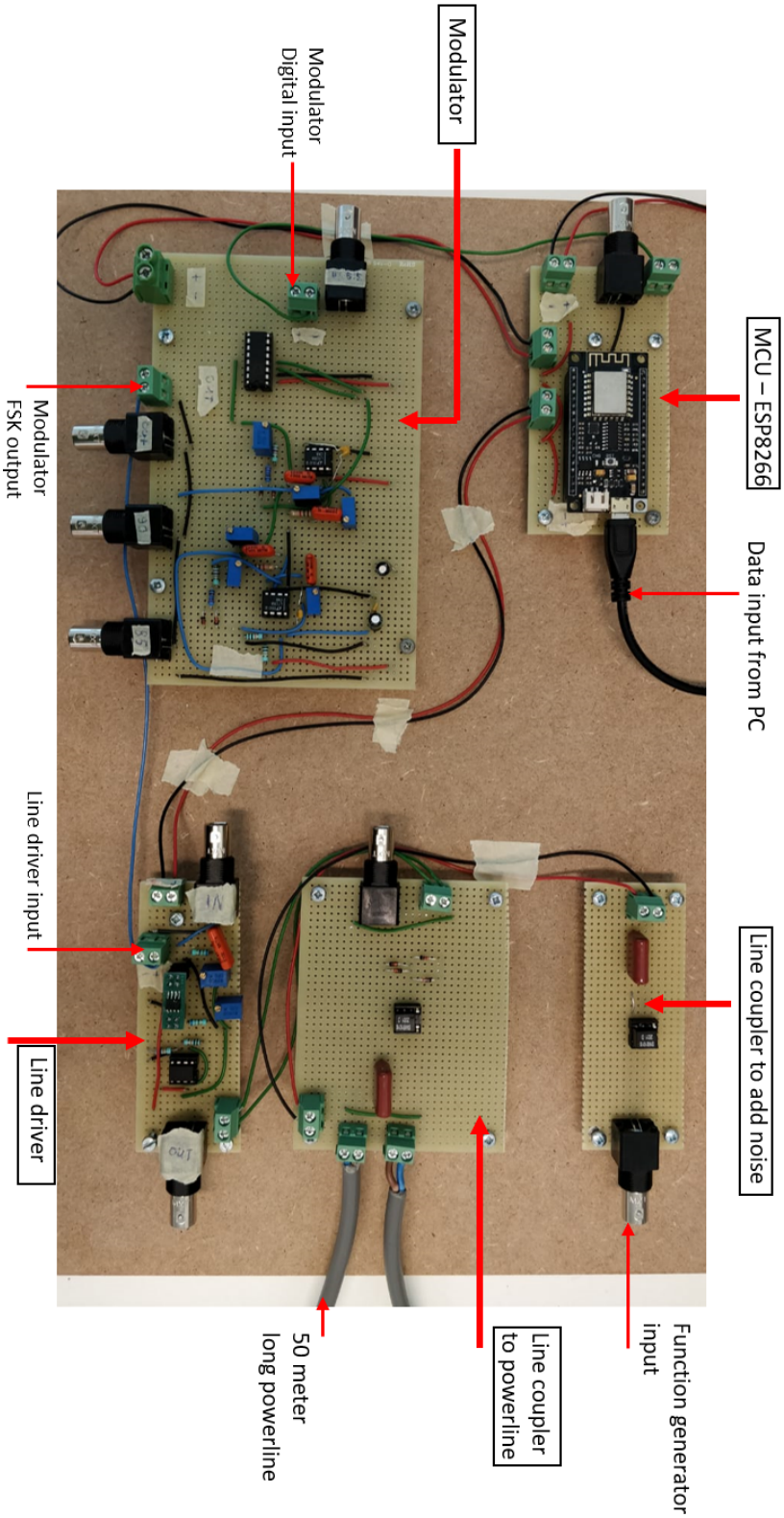

Figure G.3: Picture of the build and measured transmitter side of the PLC system.

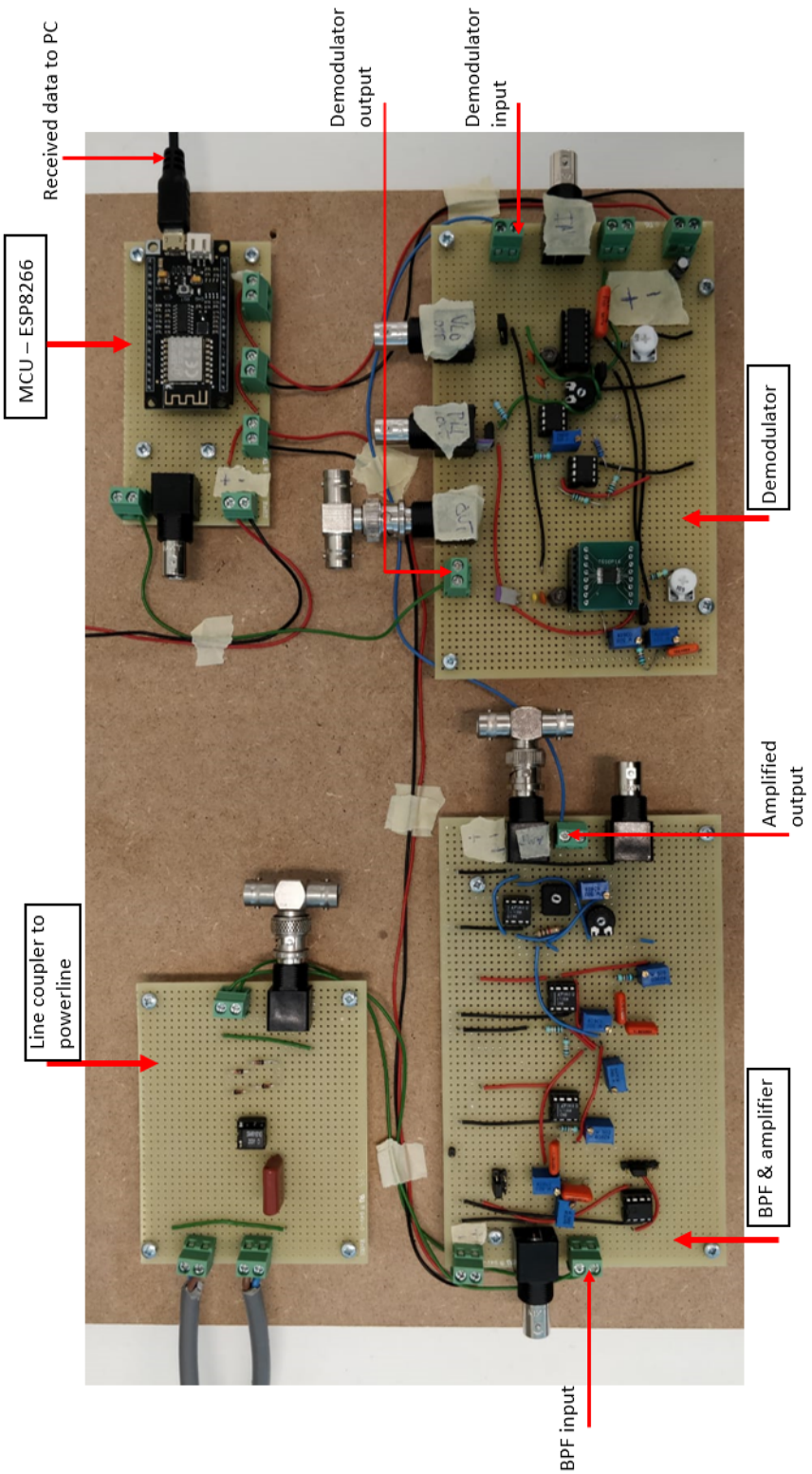

Figure G.4: Picture of the build and measured receiver side of the PLC system.

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