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3.4 A 16MHz CMOS RC Frequency Reference with ±400ppm Inaccuracy from -45°C to 85°C After Digital Temperature Compensation

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Systems-on-chip traditionally rely on bulky quartz crystals to comply with wired communication standards like CAN or USB 2.0. Integrated frequency references with better than 500ppm inaccuracy could meet this need, resulting in higher integration and lower cost. Candidate architectures have employed RC, LC or TD (thermal diffusivity) based time constants, all of which can be realized in standard CMOS. Compared to LC (~20mW, ~100ppm) [1] or TD (~2mW, ~1000ppm) [2] references, RC references offer the lowest power consumption and competitive accuracy (< 1mW, 200ppm) [3]. However, due to the nonlinear temperature dependency of on-chip resistors, such references require complex temperature-compensation schemes based on higher-order correction polynomials and extensive calibration [3,4], or complicated analog compensation networks [5].

In this work, we present a 16MHz RC-based frequency reference that achieves ±400ppm inaccuracy from -45˚C to 85˚C after a digital 2-point trim. As shown in Fig. 1, it consists of a frequency-locked loop (FLL), which locks the frequency f_{DCO} of a digitally-controlled oscillator (DCO) to the phase-shift of a Wien bridge (WB) RC filter [6]. The temperature dependence of the WB is compensated by information provided by a Wheatstone bridge (WhB) temperature sensor [7]. The temperature dependencies of both bridges exhibit similar non-linearity, allowing high accuracy to be achieved with a 2-point trim.

To relax the accuracy requirements on the temperature sensor, the temperature coefficient (TC) of the WB should be minimized. In this work, the WB is implemented with MIM capacitors (–30ppm/˚C) and p-poly resistors (–200ppm/˚C), which are standard components in the chosen 180nm process. The inaccuracy of the WhB sensor, typically <0.2˚C over temperature [7], then results in negligible frequency error. The Wheatstone bridge consists of a p-poly resistor, as well as a silicided-diffusion resistor, which has a higher TC than the silicided poly resistor used in [7]. This choice ensures that the accuracy of the frequency reference only depends on the spread of two types of resistors.

The phase-shift of the WB (Φ_{WB}) is digitized by a 2nd-order Phase Domain ΔΣ-Modulator (PDΔΣM) [6]. As shown in Fig. 2 (top), its phase DAC (ΦDAC) uses the DCO output to generate a square-wave that drives the WB at its center frequency f_{drive} (= f_{DCO}/32 = 500kHz), along with phase references, Φ_0 and Φ_1, and the modulator's sampling clock, $f_{s,WB}$ (=f_{drive}). Chopper switches demodulate the WB's phase shift (Φ_{WB}) to DC, using the phase reference selected by the bitstream. The gain of the loop filter drives the output of the chopper demodulator to zero, ensuring that, on average, the selected phase references ($\Phi_{\Delta\Sigma}$) are in quadrature with Φ_{WB}, and that the bitstream average μ_{WB} is a digital representation of Φ_{WB}.

Fig. 2 (bottom) shows a simplified block diagram of the WhB sensor, which is readout by a CTΔΣM [7]. Unlike [7], it is not trimmed and its FIR resistor DAC only varies the resistance of the p-poly part of the bridge, which improves accuracy by maintaining constant bridge sensitivity. The modulator then balances the bridge by appropriately connecting these elements in parallel, such that the average output current of the bridge is zero. The bitstream average μ_{WhB} then represents the ratio of the two resistors, which is a strong function of temperature, but is independent of the driving frequency.

Via a 1st-order polynomial, μ_{WhB} is used to generate a compensating phase Φ_{Comp} that cancels the temperature dependence of Φ_{WB}. Both bitstreams are decimated by a factor of 1024 by 2-stage CIC filters, resulting in a sampling rate of ~500Hz. The phase error Φ_e, is then driven to zero by the FLL's digital integrator, thus locking f_{DCO} to the desired temperature independent frequency. The overall FLL bandwidth can be programmed by adjusting the gain of the digital integrator, and is set to ~50Hz.

Fig. 3 shows the circuit diagram of the ΔΣDCO. It consists of a 9-stage current-starved ring oscillator, driven by a 4-bit coarse current-steering DAC, and a 1-bit fine digital ΔΣ DAC (ΔΣDAC). A coarse-fine structure is utilized to achieve high frequency resolution (~30ppm) and sufficient range to handle process variations. The coarse DAC covers the expected batch-to-batch spread (±40%) around the 16MHz nominal output frequency; while the 1-bit fine ΔΣDAC covers 1.5× the expected temperature spread (±7.5%), which is minimized by driving the ring oscillator with a CTAT current. The fine ΔΣDAC is driven by a 2nd-order digital modulator, which converts the 16-bit loop-filter output into a 2MHz bitstream. It employs a current mirror structure, which ensures that the average current through M_3 (i_{fn}) can be smoothly varied between two CTAT reference currents $i_{ref,p}$ and $i_{ref,n}$. A 3rd-order RC filter is used to suppress the modulator's quantization noise and the wide-band noise of the on-chip CTAT current generator. Its 4kHz corner frequency defines an OSR of ~250, resulting in a quantization noise floor of about 30ppm (1.8ps jitter).

The frequency reference was fabricated in a TSMC 180nm CMOS process and packaged in ceramic DIL (Fig. 7). The WB, WhB and their readout circuitry occupy 0.25mm^2 and draw 100μW from a 1.8V supply. The ΔΣDCO occupies 0.05mm^2 and draws 250μW. For flexibility, the decimation filters, the 1st-order polynomial and the integrator were implemented in an external FPGA.

With f_{DCO} fixed at 16MHz, the WB and WhB of 16 samples were characterized over temperature (Fig. 4, top). As expected, the temperature dependence of the WB output is quite low (–200ppm/˚C from –45˚C to 85˚C), and has roughly the same non-linearity as the WhB output. After a 2-point trim, the spread of the WhB is <0.075˚C from –45˚C to 85˚C, in line with the state-of-the-art (Fig.4, bottom right) [7]. As shown in Fig. 4 (bottom left), the 1st-order polynomial that maps μ_{WhB} to Φ_{Comp} is quite linear, and so its coefficients can be accurately determined by trimming Φ_{Comp} at two temperatures (–35˚C and 75˚C) until f_{DCO} = 16MHz. This approach is insensitive to variations in the actual trimming temperature, since both the WhB and WB are on the same die, and so can be assumed to be at the same temperature [4]. The accuracy of the compensated output frequency is then determined by conducting a second temperature sweep.

Fig.5 (top left) shows the frequency output and the residual frequency error for 20 samples. Over a –45˚C to 85˚C range, the frequency error with the linear mapping is less than ±400ppm, corresponding to a residual TC of 6.15ppm/˚C (box method). Fig. 5 (top right) shows that over the 1.6-2V supply range, the worst-case peak-to-peak frequency error is 500ppm, corresponding to a worst-case supply sensitivity of 0.12%/V. Fig. 5 (bottom left) shows the closed-loop (39ps$_{rms}$) and open-loop (37ps$_{rms}$) period jitter of f_{DCO}, which demonstrate that the jitter contribution of the temperature-compensation scheme is negligible compared to that of the DCO itself. With a fixed digital input, the Allan Deviation of the DCO exhibits a 20ppm noise floor, which drops to 320ppb in the closed-loop configuration (Fig. 5, bottom right).

Fig. 6 summarizes the performance of the proposed RC frequency reference and compares it to state-of-the-art designs that achieve < 10ppm/˚C residual TC. The proposed frequency reference maintains state-of-the-art accuracy over multiple samples over the industrial temperature range, while its calibration complexity and thus manufacturing cost is greatly reduced. This work demonstrates that integrated RC frequency references can be used in wireline applications such as CAN and USB 2.0.

Acknowledgements:

The authors would like to thank Zu-yao Chang for his invaluable contribution and Infineon Technologies for the financial support.

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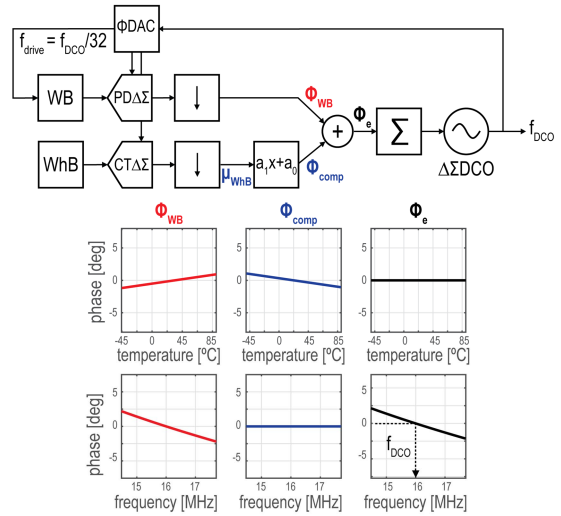

Figure 3.4.1: Block diagram of the proposed frequency reference (top) and simulated phase responses of the Wien Bridge, Wheatstone Bridge and the compensated loop error signal (bottom).

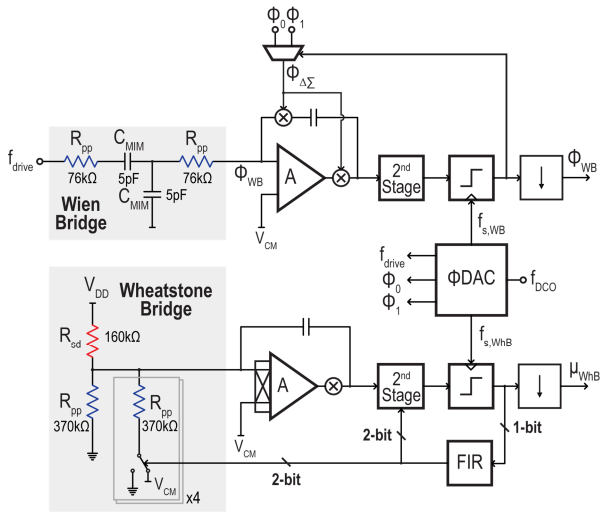

Figure 3.4.2: Simplified single-ended circuit diagrams for the Wien Bridge & PDΔΣM (top) and Wheatstone Bridge & CTΔΣM with FIR-DAC feedback (bottom).

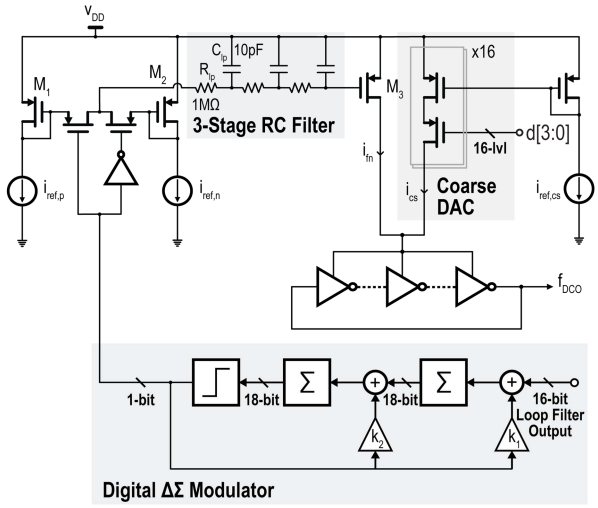

Figure 3.4.3: Circuit diagram of the ΔΣDCO.

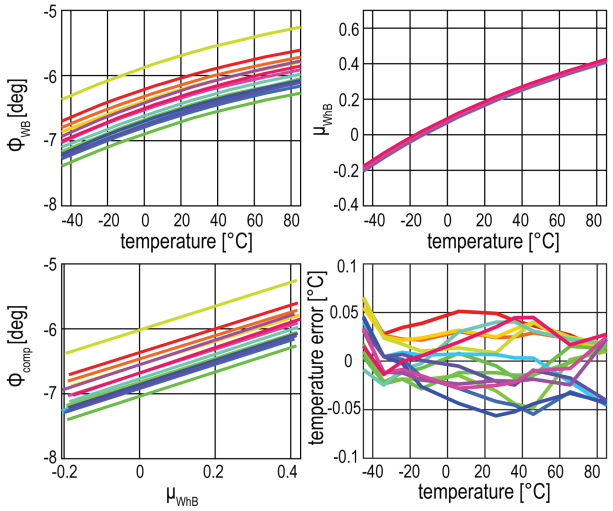

Figure 3.4.4: Measured Wien Bridge (WB) phase (top left), Wheatstone Bridge (WhB) bitstream average (top right), P(.) mapping WhB average to WB phase (bottom left) and WhB temperature sensing inaccuracy (bottom right).

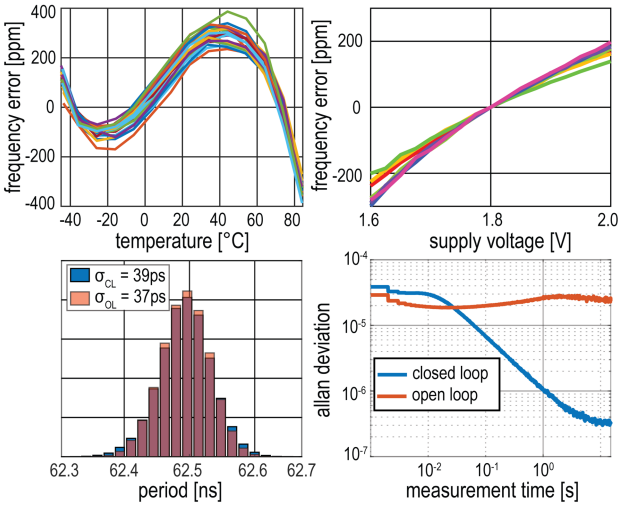

Figure 3.4.5: Measured frequency inaccuracy vs. temperature (20 samples, top left), vs. supply voltage (top right), period jitter (bottom left) and Allan Deviation (bottom right) in closed-loop and open-loop configurations.

	This Work	Gurleyuk [3] JSSC'18	Satoh [4] VLSI'14	Zhang [5] VLSI'17	Chen CICC'19	Liu JSSC'19
Process [nm]	180	180	180	180	180	65
Area [mm²]	0.3	1.65	1.04	0.17	0.145	0.051
Frequency [MHz]	16	7	2 to 40	24	0.0669	1.05
TC [ppm/°C]	6.15	2.5	2.43	3.2	9.6	4.3
# of Trimming Points	2	2 + Batch	> 4	3	2	> 2
Temperature Range [°C]	−45 to 85	−45 to 85	0 to 70	−40 to 150	−20 to 100	−15 to 55
Supply sensitivity [%/V]	0.12	0.18	0.017	0.03	0.4	4.25
Supply Range [V]	1.6 to 2.0	1.7 to 2.0	1.62 to 1.98	1.8 to 5.0	1.2 to 1.9	0.98 to 1.02
# of Samples	20	8	12	1	5	1
Allan Deviation [ppm]	0.32	0.33	-	-	50	-
Power [µW]	400	750	2900	200	0.056	69

Figure 3.4.6: Performance summary and comparison table with state-of-the-art.

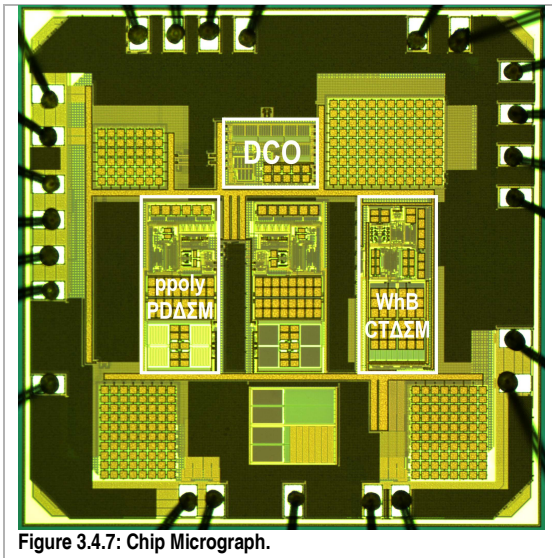

Figure 3.4.7: Chip Micrograph.

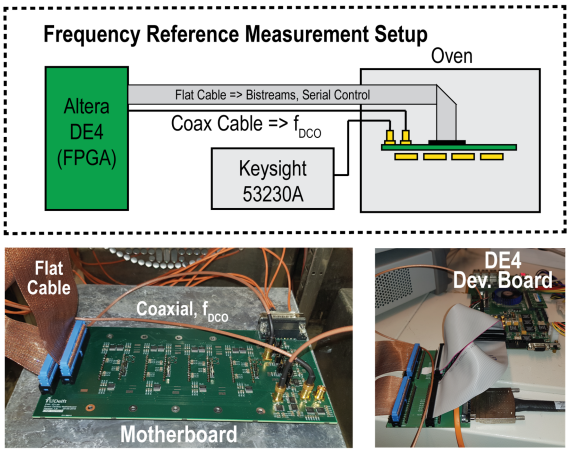

Figure 3.4.8: The frequency reference measurement setup (top) consists of a motherboard carrying 4 samples. This is placed in an oven, and the samples are controlled by an FPGA. The PC (via a DAQ card) is only used to control the

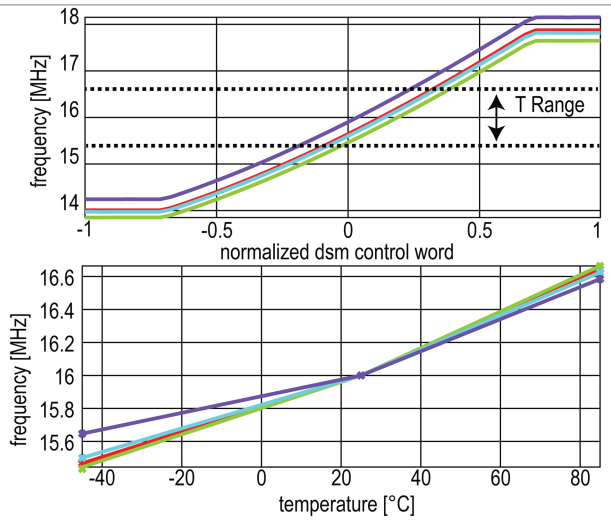

Figure 3.4.9: DSM control word vs. DCO output frequency (top) and DCO output frequency vs. temperature, after setting the control word at 16MHz at the output (bottom). 4 samples show a comfortable fit.