Fully Integrated Discrete-Time Superheterodyne Receiver in Nano-Scale CMOS

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Fully Integrated Discrete-Time Superheterodyne Receiver in Nano-Scale CMOS

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To my dear parents, Minoo and Hossein-Ali

To my dear brothers, Mahdi and Mohammad

To my uncles, Hamid, Amir, and Ali

And last, but not least, to my lovely wife Zahra

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Chapter 1

Introduction

After the first demonstrations of radio wave transmission and reception by Hertz in 1887 and spurred by the invention of triode vacuum tube, tuned radio frequency (TRF) receivers became popular in early 1920s. A TRF receiver consisted of several tuned RF amplifiers and a detector at the end. Each triode provided only a small RF gain and so the TRF had a poor sensitivity. Soon after the invention of superheterodyne receiver by Armstrong, the TRF radios were quickly supplanted in 1930s. In a superheterodyne receiver, the RF signal is mixed with a local oscillator and down-converted to a *fixed* intermediate frequency (IF). At IF, triodes had a high amplification gain, and also implementation of fixed bandpass filters was easier. For more than half a century, the superheterodyne receiver has outperformed other architectures in terms of sensitivity, selectivity and cost [1].

With the invention of transistor and later integrated circuits in 1958, a new goal of making a monolitically *integrated* receiver came up. In late 1960s, integrated superheterodyne receivers were developed but they needed external IF filters. The IF filter was traditionally made of passive bulky components (SAW, ceramic or external LC filters), nearly impossible to integrate in silicon. Simplicity of a zero-IF architecture (a.k.a, direct-conversion or homodyne invented in 1902), has attracted designers to make fully monolithic receivers. In that architecture, instead of the IF band-pass filter (BPF) used in a superheterodyne, a low-pass filter (LPF) is used, which makes it easy to be implemented monolithically. In this way, receivers could be made much cheaper and smaller [1].

An essential part of transmitter/receiver (transceiver) is a local oscillator (LO) circuit to drive

the RF mixer for frequency translation (upconversion/downconversion) and to generate all other clocks. An LC-tank is an excellent candidate for RF oscillation since it ensures low phase noise. Integration of inductor and capacitor in combination with the fast transistors in silicon have made it possible to have fully integrated LC-oscillators in the GHz range.

1.1 Motivation

1.1.1 Why Nanoscale CMOS?

A radio system-on-chip (SoC) conventionally includes RF front-end, frequency synthesizer, analog baseband circuitry, analog-to-digital and digital-to-analog converters (ADC/DAC), digital baseband signal processor, and digital application processor. Among all the different blocks, the combined digital baseband/application processor occupies most of the area, hence it defines the SoC fabrication process. The rest of the circuitry then needs to be adopted for the chosen process.

For example, if a 28-nm bulk CMOS is selected, the receiver frontend of the SoC also has to be implemented with a supply voltage of 0.9 V or less, which is imposed by the technology. In this respect, new RF/analog techniques are required to be able to function at the reduced voltage headroom. In addition, new oscillator structures need to be developed that can work at low supply voltages while providing high spectral purity. In addition, cost reduction is always under tremendous push so the oscillator costs must be reduced by occupying less silicon area. However, conventional oscillator structures with lower area sacrifice spectral purity. In this respect, a new oscillator structure that features reduced area at low phase noise would be considered very attractive.

1.1.2 Why Discrete-Time?

While main motivations of CMOS scaling have been to reduce transistor cost and to improve digital performance, conventional RF/analog designs have not benefited significantly. A finer process node produces shorter digital gate delays while a lowered supply voltage and gate capacitance reduce power consumption. As shown in Figure 1-1, going from 180-nm to 28-nm CMOS, V_{DD} is reduced almost by half while MOS threshold voltage (V_{th}) has not changed considerably. Therefore, the precious available voltage headroom for RF/analog design is now reduced dramatically [2]. Considering also the reduced MOS intrinsic gain [2] and its saturation

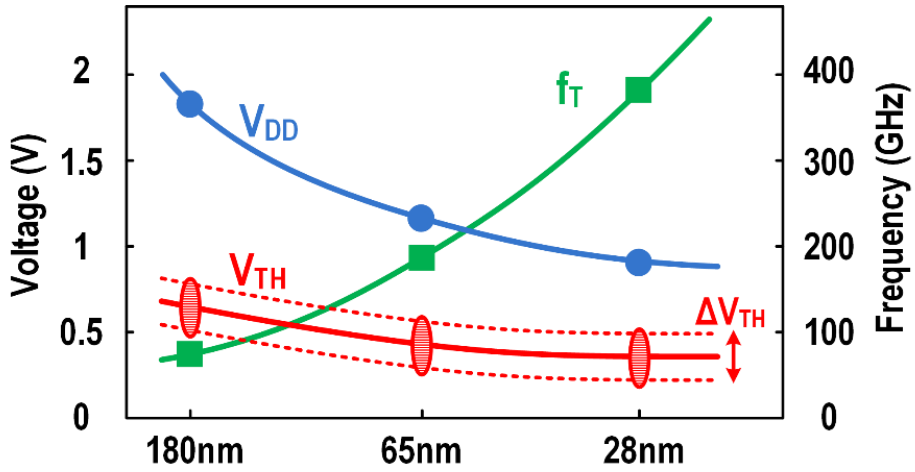


Figure 1-1: Typical CMOS scaling trends for low-power/low-leakage process technology.

linearity in scaled CMOS [3], continuous-time (CT) RF/analog design is becoming generally more difficult. In this way, power consumption and area of the traditional RF/analog designs are not directly process scalable.

On the other hand, majority of cellular and wireless standard frequency bands are allocated from 400 MHz to 6 GHz, and have not significantly changed for many years. Meanwhile, transistor cutoff frequency (f_T) has improved dramatically with scaling, as shown in Figure 1-1. For example, the period from 1999 to 2011 has seen f_T increasing from 65 GHz in 0.18μm to 400 GHz in 28-nm process. This suggests that conventional CT techniques that were optimized for the older technology do not effectively use the ultra-high speed of transistors of scaled CMOS to improve the performance of RF/analog designs[1].

In contrast, the newly introduced discrete-time (DT) RF/analog blocks (Figure 1-2) avoid using complicated traditional analog components such as opamps, and most of signal processing and filtering are done using passive switched-capacitor circuits [4], [5]. Waveforms required for driving the switches are also generated using digital logic. To provide signal gain, DT techniques use inverter-based gm-cells that avoid transistor stacking and are *always* compatible with digital technology. As the technology scales, MOS switches become faster and tinier with lower parasitic capacitances. Digital waveform generator becomes also faster and more power efficient. Moreover, metal capacitor density improves from one process node to the next, resulting in a reduced area. In addition, the inverter-based gm-cell structure is fully scalable with

[1] An exception is noise figure that improves with f_T increase [2].

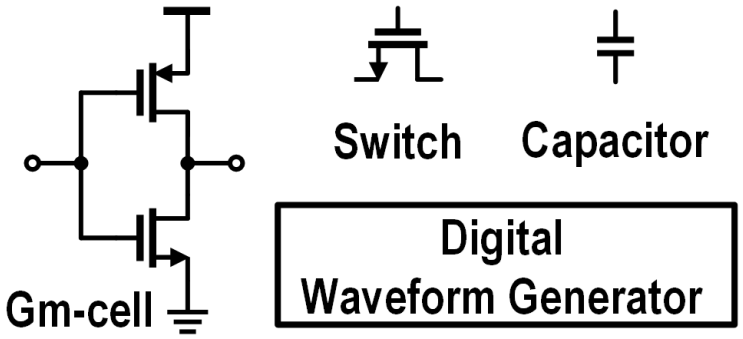


Figure 1-2: Components used in DT signal processing.

improved gm over bias current. In this way, DT receivers directly benefit from scaling similar to digital circuits. [6]–[12] are examples of DT process-scalable receivers.

1.1.3 Why Superheterodyne Receiver?

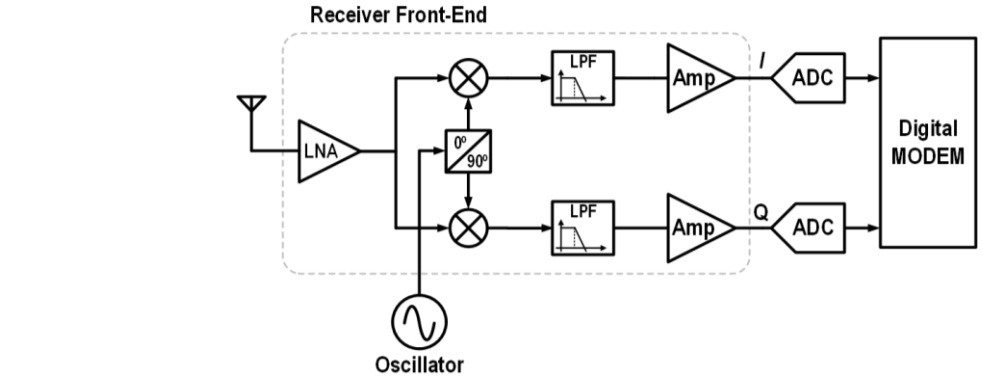
The zero/low-IF (ZIF/LIF) receiver architecture (Figure 1-3(a)) has been predominant in wireless applications chiefly due to its high level of integration. However, that architecture suffers from several handicaps. LO self-mixing [13] creates a time-varying DC offset that could be up to 2 to 3 orders of magnitude larger than the wanted signal. In addition, ZIF/LIF receivers suffer from limited IIP2 that degrades signal-to-noise ratio (SNR) of the wanted signal in the presence of a large blocker [13]. Since most of the filtering and amplification in a ZIF/LIF receiver are done at low frequencies, flicker noise of devices leads to a higher NF of the receiver.

In contrast, superheterodyne with a high IF (HIF) does not experience these problems at all. The high IF separates the wanted signal from the DC offset and 2^{nd}-order intermodulation, thus the LO self-mixing and limited IIP2 problems are avoided. Also, filtering and amplification in a superheterodyne are done normally at higher frequencies than the device flicker corner.

Therefore, accounting for the recent advancements in the CMOS process technology, it appears that it is now time to return to the historical superheterodyne RX architecture by a fully integrated solution.

1.2 The Thesis Objectives

The main goal of this dissertation research is to invent a new receiver architecture that would take advantage of the future CMOS technology scaling and offer better performance, power consumption and cost than the traditional architectures. This dissertation describes principles,



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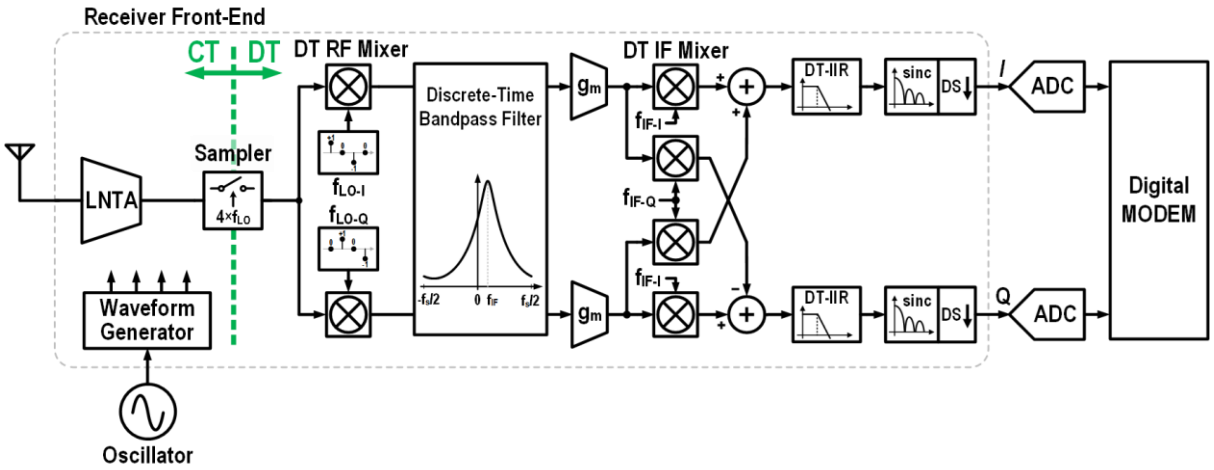


(b)

Figure 1-3: Simplified top-level diagram of (a) a state-of-the-art continuous-time low-IF receive, and (b) the newly proposed discrete-time superheterodyne receiver.

design, modeling and implementation of a fully integrated receiver in nanoscale CMOS with its simplified top-level diagram shown in Figure 1-3(b).

Based on the previously explained motivations, the first objective is designing a fully integrated discrete-time receiver, using superheterodyne (high-IF) architecture that avoids the aforementioned handicaps of the ZIF/LIF architecture. To achieve this, system level analysis of a signal sampling scheme at RF needs to be carried out. Since both downconverter mixer and sampling in a receiver perform frequency translations and folding, this introduces a rather complicated frequency domain analysis of a DT receiver. A unified yet simple model describing the DT receiver has to be developed. A suitable low-noise transconductance amplifier (LNTA), instead of an LNA in CT implementations, should be designed with a low noise figure (NF) to guarantee adequate RF performance. The challenge of efficiently integrating the DT bandpass filter in CMOS needs to be solved. Since the whole signal processing needs to be done in DT, a

low-power baseband processing is required such that by means of filtering and decimation the received signal gets adapted to a low power and low resolution ADC.

As an important part of a fully integrated receiver, the second objective of this dissertation is the low-voltage oscillator (see Figure 1-3(b)) optimized for nanoscale CMOS. At first, a high-swing class-C oscillator is targeted that is able to efficiently use the severely reduced voltage headroom in advanced CMOS. Meanwhile, the class-C operation of this oscillator provides a high power efficiency that leads to reduced phase noise. In another low-voltage design, a low-cost low-phase-noise oscillator is targeted. This oscillator should provide an excellent phase noise performance with considerably reduced silicon area. Then, this oscillator can be integrated with other blocks in an SoC for very low cost applications.

1.3 Thesis Outline

This thesis is composed of two parts. In the first part, the principles, design and implementation of a fully integrated DT superheterodyne receiver are covered. At first, the required sampling scheme in a high-IF receiver is explained. It is followed by sequentially introducing all the required circuits. At the end of the first part, the operation of the whole receiver chain is explained. In the second part, design and implementation of low-voltage fully integrated oscillators in nano-scale CMOS are discussed and demonstrated.

The first part starts with Chapter 2 by explaining how the historical superheterodyne RX architecture implemented in nano-scale CMOS can solve the problems of zero-IF architecture, such as limited IIP2, time-varying DC offset, and high levels of flicker noise. Next, various sampling schemes used in state-of-the-art zero-IF DT receivers are discussed. Then, a 4x-sampling concept is proposed in order to avoid the image problem of DT high-IF architectures. In the following three chapters, required blocks to implement the proposed DT superheterodyne receiver are proposed.

In Chapter 3, a novel DT high-order low-pass filter is proposed. This filter to be used at the receiver baseband has an exceptionally low noise and high linearity. Deep analysis, verified by test-chip measurements, is presented. In addition, basic sampling concepts, such as charge sampling versus voltage sampling, are explained.

In Chapter 4, a very high sampling rate DT bandpass filter (BPF) using I/Q charge sharing

is proposed. After explaining the operation of this filter, its analysis is carried out. The filter is then compared to other IF filter structures. Then, a simple DT model of the gm-cell used as a DT gain block is described. At the end, an extension of the DT BPF to a higher quality factor and higher order is mentioned.

In Chapter 5, a novel wideband noise-cancelling LNTA is proposed. It is developed step-by-step from two basic LNA structures. In this LNTA, a two-fold noise cancellation is implemented that, in addition to canceling the noise of input matching transistor pair, noise of another LNA transistor pair is also cancelled.

In Chapter 6, a fully integrated DT superheterodyne receiver is proposed and further elaborated. After discussing the proposed structure and its DT model, frequency translations, as well as image rejection mechanisms, are explained. Then, the baseband signal processing, which features an ultra-low power consumption, is discussed. Afterwards, measurement results of an implemented test chip in 65-nm CMOS are presented and compared with other state-of-the-arts receivers. At the end, an extension of the superheterodyne DT receiver to a SAW-less operation is discussed and measurement results of a test chip in 28-nm CMOS are reported.

The second part starts with Chapter 7, where a high-swing class-C oscillator is proposed. It efficiently uses the drastically reduced supply voltage headroom in nanoscale CMOS. The maximum output swing of this structure is calculated and compared with the original class-C oscillator. Implementation details of a low-power low-voltage test chip in 90-nm CMOS, supported by measurement results, are also presented. At the end, the idea of high-swing class-C oscillator is extended to an ultra-low phase noise dual-core oscillator implemented in 65-nm CMOS. This oscillator is the first-ever fully integrated design that meets phase noise requirements of a GSM BTS standard in a bulk CMOS technology.

In Chapter 8, another novel low-voltage oscillator topology is proposed. It uses a series-LC tank ring structure. The first version, realized in 40-nm CMOS, targets low silicon area using low-Q inductors and exhibits 7–20 dB better phase noise than other state-of-the-art low area oscillators. At the end, this idea is extended to ultra-low phase noise by means of regularly sized inductors.

Finally, Chapter 9 concludes this dissertation and presents suggestions for future developments.

Part I:

Fully Integrated DT Superheterodyne RX in Nano-Scale CMOS

Chapter 2

DT RF Receiver Architectures

In this chapter, zero-IF and superheterodyne receiver architectures are first compared by elaborating on their advantages and disadvantages. Then, different sampling schemes present in the state-of-the-art zero-IF DT receivers are studied using a simplified DT receiver. At the end, a 4x-sampling concept is introduced for use in DT high-IF receivers [14].

2.1 Superheterodyne vs. Zero-IF

The zero-IF (ZIF), and closely related low-IF (LIF), architecture of monolithic receivers has been predominant in wireless radios. This is mainly because of high level of integration that lowers the total system cost. Instead of the BPF used earlier in a superheterodyne, the zero-IF receiver requires a low-pass filter, which can be easily integrated in CMOS. Since a local oscillator (LO) frequency is the same as the RF signal frequency, the zero-IF receiver does not experience the IF image problem, or in low-IF it is easily solvable in digital baseband. In contrast, IF image in a superheterodyne is normally out-of-band and requires a high phase accuracy of quadrature LO clocks.

The advantages of the ZIF architecture obviously do not come for free. Since the LO coincides with the RF frequency, immediately LO self-mixing problems arise [13]. The LO leakage to the LNA input is amplified and then mixed with LO again, creating a DC offset. This offset could be up to 2 to 3 orders of magnitude larger than the wanted signal at the mixer output [13]. Considering the LO leakage to antenna, it could be radiated and subsequently reflected

from a moving subject back to the antenna. In this case, the DC offset is time-varying and thus much harder to be canceled. In general, DC offset cancelation loop is required to dynamically remove it [15]. The low-IF architecture somewhat mitigates these phenomena by shifting IF from zero to a very low offset frequency that is a fraction of a channel bandwidth. However, superheterodyne with a high IF (HIF) does not experience these problems at all.

Furthermore, ZIF/LIF receivers suffer from limited IIP2, imposed mainly by the RF downconversion mixer. When a large blocker signal (especially a modulated one) enters the receiver, second-order nonlinearity causes the blocker to be downconverted to around zero frequency, where the wanted signal also resides. This effect deteriorates the signal-to-noise ratio (SNR). Since in the superheterodyne frontend the wanted signal resides at a high IF, this architecture shows an infinitely high IIP2. While an analog or digital (through ADC) baseband backend might introduce some nonlinearity, the 2^{nd}-order intermodulation (IM2) product will be rather infinitesimal due to the IF filtering such that IIP2 remains extremely high.

The IIP2 problem in zero-IF receivers is usually relieved by calibration. RF mixers typically have an uncalibrated IIP2 of about 50–60 dBm that, including the LNA gain, becomes 35–45 dBm at the receiver input. This poor IIP2 alone or in combination with a preselect filter could be acceptable for certain applications. However, for a SAW-less receiver aimed at tough wireless/cellular standards, such as WCDMA, a total IIP2 of more than 60 dBm is required [15], [16]. This high IIP2 is achieved in ZIF receivers by elaborated IIP2 calibration techniques [16]–[20]. These calibrations require a period of time to find an optimum setting for the mixer. Background techniques could take a considerable amount of time to settle in the presence of wanted signal [16], [17]. Offline (foreground) techniques need to generate an input test tone and introduce their own complications [15], [18], [19]. While the total calibrated IIP2 of a ZIF receiver can reach 60 dBm, it is very dependent on circuit operating conditions, such as temperature, V_{DD}, blocker offset and also LO frequency [17]–[20]. As each of these parameters is changed slightly, a new calibration need to be re-run [17], [20]. In addition, some calibration techniques are sensitive to DC offsets, which rather need to be removed before the IIP2 calibration through a separate DC offset cancellation loop [15], [16], [20]. All the above calibration handicaps are a strong motivation to use a receiver architecture inherently without such inherent IIP2 problems.

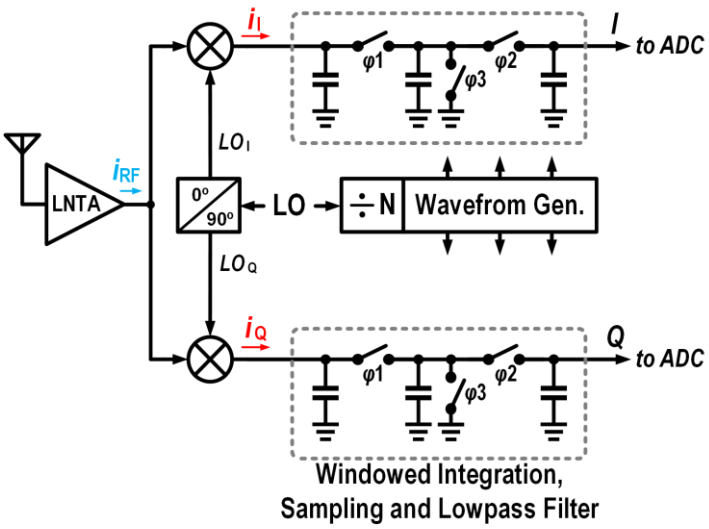
Most of the filtering and amplification in a zero-IF receiver are done after the mixer at low frequency. In CMOS implementations, flicker noise of devices at low frequencies corrupts the wanted signal, leading to a higher NF of the receiver. In contrast, filtering and amplification in a superheterodyne are done normally at higher frequencies than the devices flicker corner.

Considering advantages and disadvantages of a superheterodyne compared to ZIF, and accounting for the recent advancements in CMOS process technology, it appears that it is now time to return to the historical superheterodyne for high performance applications. The main remaining challenge is the CMOS integration of the IF filter, which is discussed in Chapter 4. Examples of modern fully integrated superheterodyne receivers are [6], [7], [14], [21].

2.2 DT ZIF Receiver: 1x and 2x Sampling

A simplified conceptual diagram of a DT ZIF receiver is shown in Figure 2-1(a). The receiver consists of a low-noise transconductance amplifier (LNTA), a pair of quadrature mixers and two DT sampling low-pass filters. After the antenna, the received RF signal is amplified and converted into current, i_{RF}, by the LNTA with high output impedance. This current is then downconverted to zero-IF by the quadrature mixers. The mixers are driven by $LO_{I,Q}$ signals, which are differential 25% duty-cycle clocks with 90º phase shift. Considering a narrow-band modulated RF signal, Figure 2-1(b) shows signal waveforms at various stages. The current leaving the mixers is integrated over a time window T_i and sampled in the form of DT charge packets [5], $q_{I,Q}$[n]. This DT data is then low-pass filtered by a passive switch-cap circuit (e.g., a 2nd-order IIR [4], [5]). The windowed integration forms a continuous-time (CT) *sinc* anti-aliasing filter just before the sampling (Figure 2-2), and attenuates unwanted signals folded from multiples of the sample frequency f_s (i.e., sampling images) [10], [22]. The window time (and sampling rate) is set easily by the clock rate of the waveform generator circuit.

In most of the DT ZIF receivers, this sampling is done at a significantly lower rate than the LO frequency (f_{LO}, which is the mixer downconversion frequency) [8]–[10], [23], [24]. For example in [10], a sample rate of 480 MS/s is used for a 2.4 GHz RF signal. A lower sample rate increases attenuation of sampling image frequency at a fixed offset, but creates also extra sampling images at lower offsets [10].



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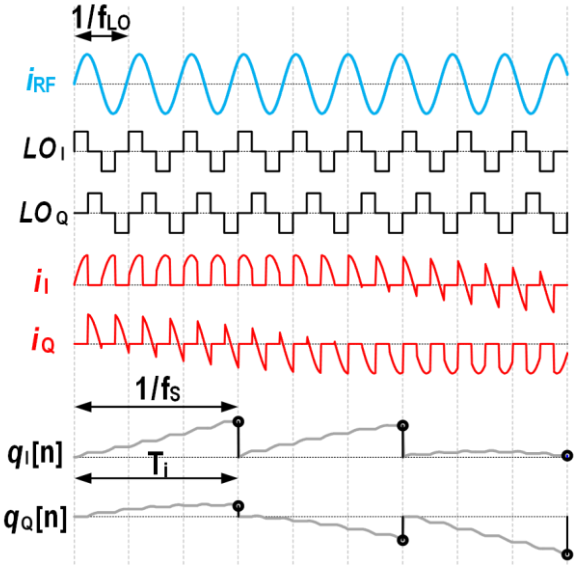


(b)

Figure 2-1: (a) A simple DT receiver with passive LPF; and (b) its waveforms at various nodes

2.2.1 1x Sampling in Zero-IF

For the time being, the signal sampling in a DT receiver with the simplified structure of Figure 2-3 is focused. Consider the case of a ZIF reception where the signal is sampled at the same rate as the LO frequency [9], hereafter *1x sampling*. Drawn in Figure 2-4(a), the narrow-band modulated current signal i_{RF} is downconverted as i_I and i_Q baseband quadrature currents, windowed integrated (WI), and then sampled in form of charge packets, $q_I[n]$ and $q_Q[n]$, at the end of each LO cycle.

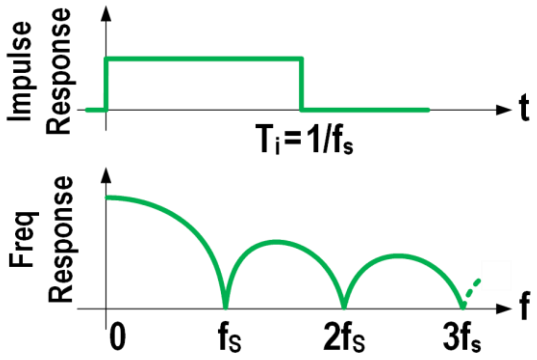


Figure 2-2: Impulse and frequency response of windowed integration.

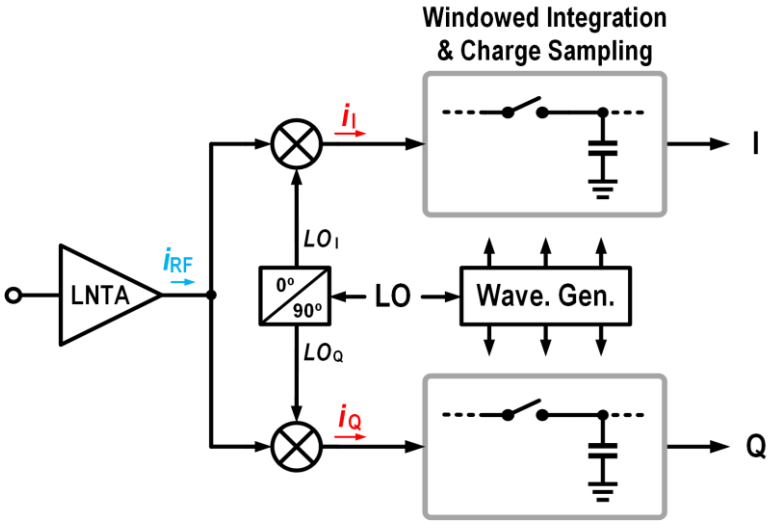
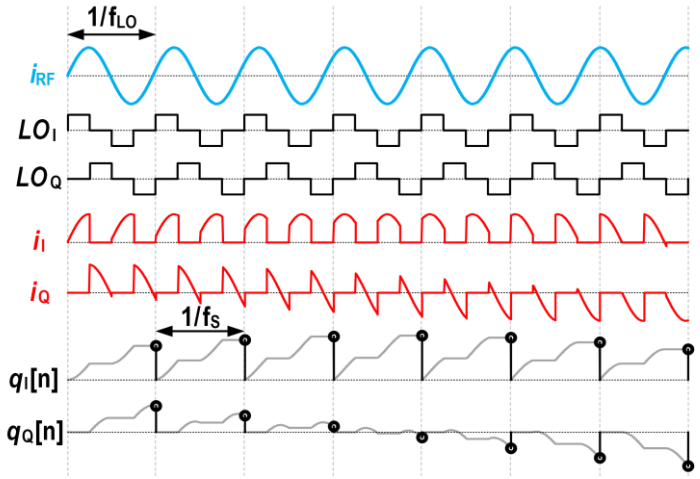


Figure 2-3: Signal sampling in a DT receiver.

ZIF architecture with 1x sampling has image frequencies at multiples of LO frequency. Figure 2-4(b) shows the frequency translation. The wanted RF signal (depicted in blue) is downconverted to zero by mixing with the quadrature LO (black tone). At the same time, frequency bands near zero and $2f_{LO}$ (in yellow) are translated to $\pm f_{LO}$. The windowed integration of $i_{I,Q}$ and sampling forms a continuous-time (CT) antialiasing filter (shown in green), with its notches coinciding with the sampling images. The narrower the required bandwidth, the stronger the image attenuation [10]. After the sampling, attenuated images at multiples of $\pm f_s$ are folded over the wanted signal at baseband.

2.2.2 2x Sampling in Zero-IF

By increasing the sample rate to two times the LO frequency (hence, *2x sampling*), the ZIF receiver does not introduce any sampling images other than those caused by mixer's odd harmonics, (i.e., 3rd, 5th, and so on). This should promote wideband reception, which benefits



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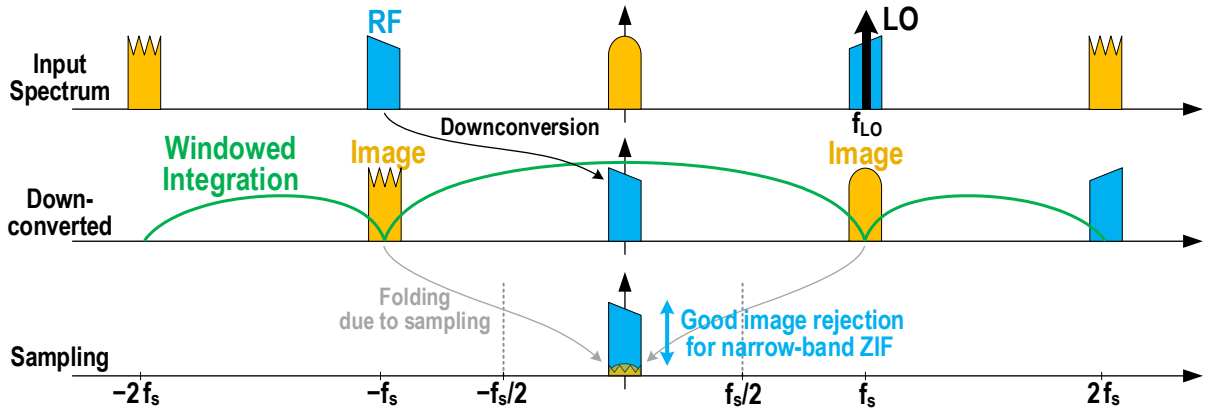
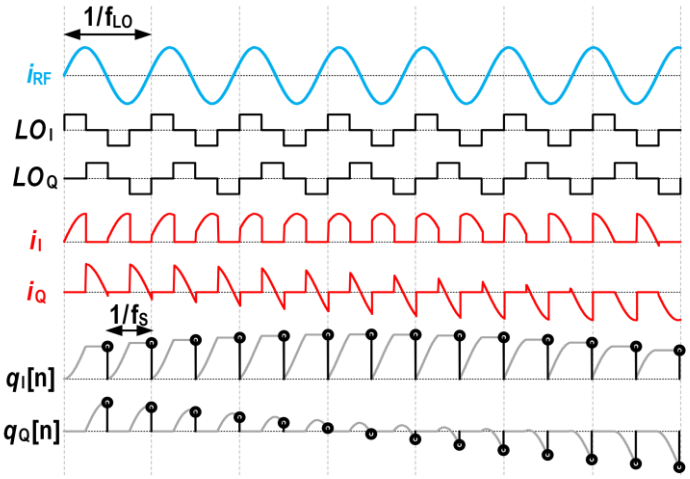


(b)

Figure 2-4: (a) Time-domain signal waveforms; and (b) frequency translation in a 1x sampling zero-IF DT receiver: input spectrum is shifted to right (RF downconversion) and after windowed integration is sampled.

less from the protective notches of the antialiasing WI filter. Figure 2-5(a) shows transient signal waveforms. The sample rate (f_s) is now doubled with respect to the 1x sampling by reading the integrated currents at twice the rate. It needs to be emphasized that the doubling of sampling rate is independent of the clocks used for the mixer, which is still at f_{LO}.

As shown in Figure 2-5(b), antialiasing filter caused by WI is widened twofold. After sampling at 2x, the "yellow" bands still remain at high frequency and are not mixed with the wanted signal. Therefore, in the 2x sampling, it is possible to further filter the images prior to decimation and folding over the wanted signal. The only images created by sampling are self-image of the wanted RF signal and the images that come from odd harmonics of f_{RF} (e.g., $3f_{RF}$, not shown in the figure), all attenuated earlier by the antialiasing filter. Note that in Figure 2-5(b),



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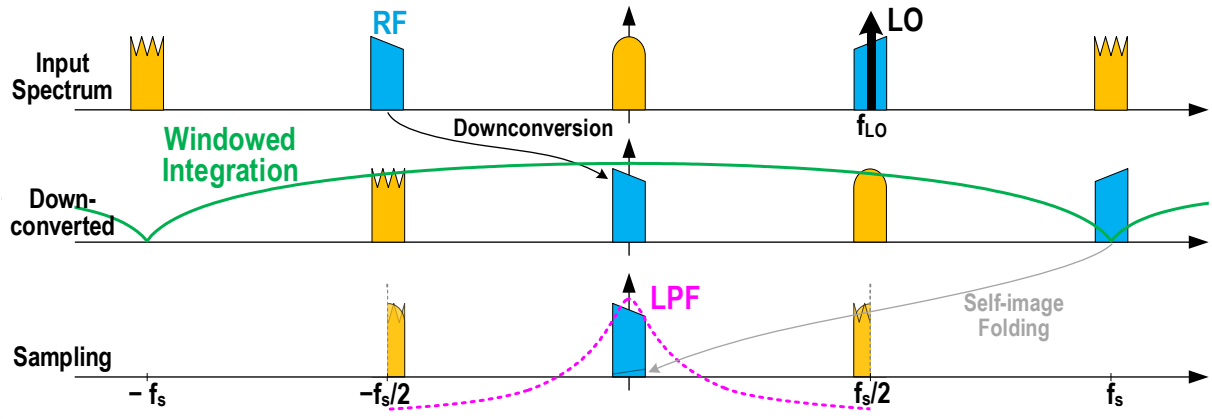


(b)

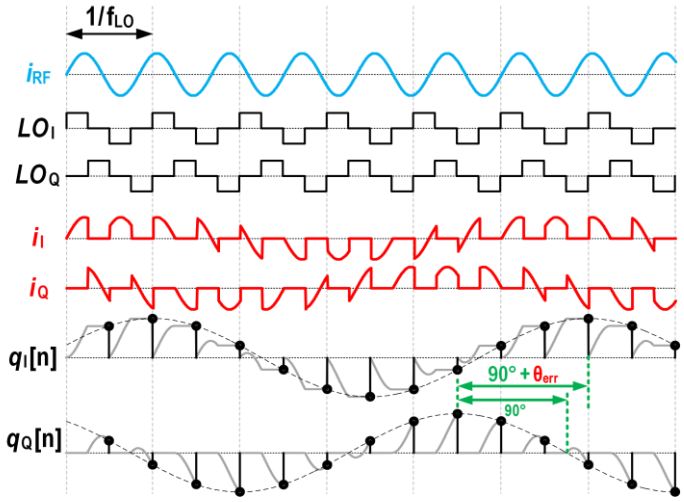
Figure 2-5: (a) Time-domain signal waveforms; and (b) frequency translation in a 2x sampling zero-IF DT receiver. "Yellow" bands after the sampling are folded on themselves, but remaining apart from the wanted signal and can be filtered afterwards by a DT LPF.

mixer harmonics that produce mixer images are not shown for the sake of clarity in illustrating the sampling process.

2.3 Proposed 4x Sampling for DT High-IF Receiver

2.3.1 2x Sampling in Superheterodyne

If the 2x sampling concept were to be used in a DT superheterodyne receiver, in which the IF frequency (f_{IF}) is high, where $f_{LO} = f_{RF} + f_{IF}$, the receiver would show a poor image rejection. To illustrate that, let us assume spectrum of the input signal as depicted in Figure 2-6(b). The



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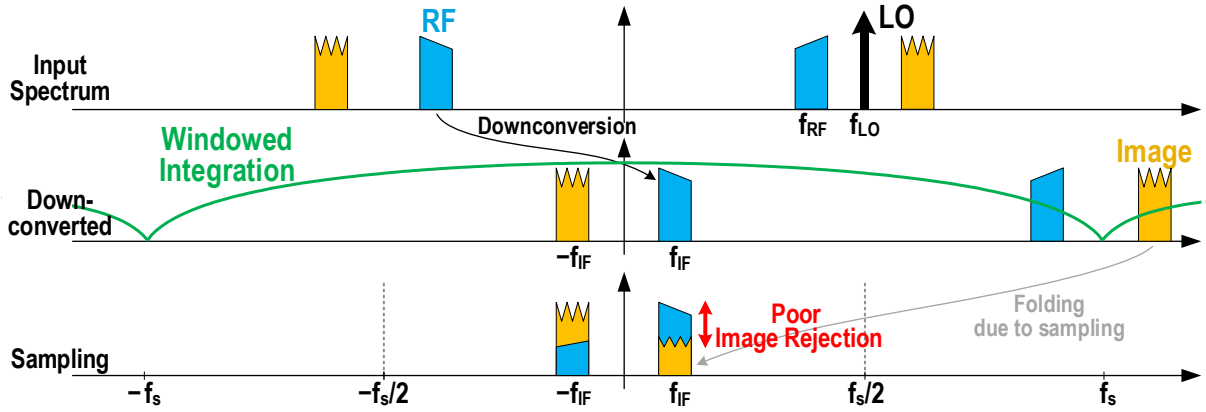
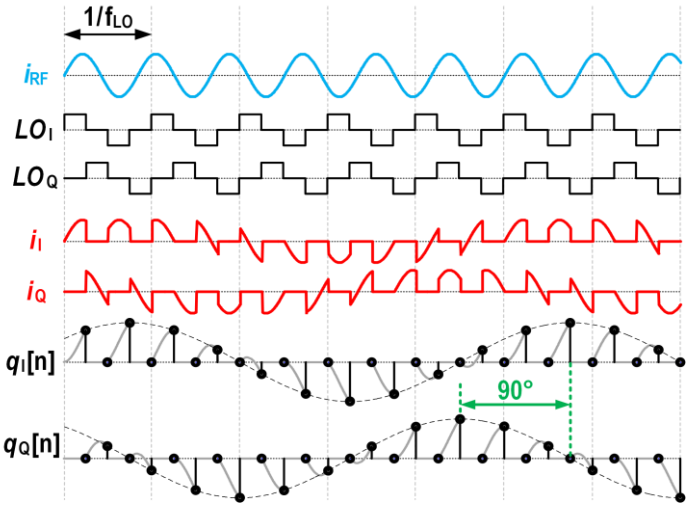


(b)

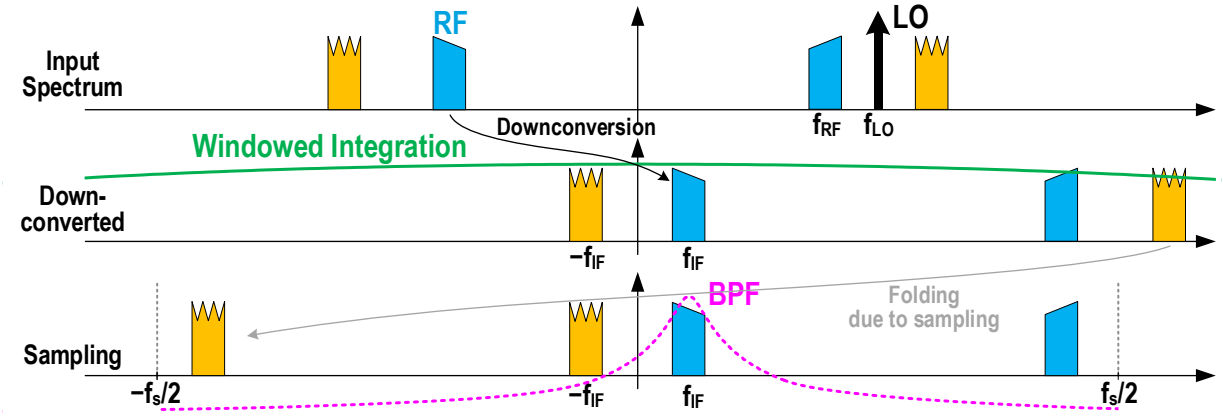
Figure 2-6: (a) Time-domain signal waveforms; and (b) frequency translation in a 2x sampling DT superheterodyne receiver. After the sampling, image is aliased on the wanted signal without enough attenuation.

wanted signal is downconverted to $+f_{IF}$ after the mixer[2], while part of the image power is upconverted to $2f_{LO}+f_{IF}$. By sampling this signal at the 2x rate, this image (whose absolute frequency is higher than the Nyquist rate, $f_s/2$) folds over the wanted signal at $+f_{IF}$. In addition, note that in the superheterodyne the notch of the windowed integration is not aligned (unlike in ZIF) with the image (it is separated by f_{IF}). Therefore, the image signal is not effectively filtered out and this leads to an unacceptable image rejection of the receiver.

[2] Assuming I/Q signals are at baseband, the complex signal defined as $I+jQ$ could have asymmetric spectrum around zero. Also, the sampling Nyquist (alias-free) range is from $-f_s/2$ to $f_s/2$ instead of 0 to $f_s/2$ for real signals.



(a)



(b)

Figure 2-7: (a) Time-domain signal waveforms; and (b) frequency translations in a 4x sampling DT superheterodyne receiver. Since f_s *is increased to 4*f_{LO}*, IF image is completely distinct from the wanted signal and can be filtered afterwards by a DT BPF.*

To get further insight, let us inspect the time-domain signals of this structure in Figure 2-6(a). As expected, the RF signal after downconversion and sampling is centered at a high IF and the two sampled signals (q_I[n] and q_Q[n]) have quadrature sinusoidal waveforms. Looking more closely, the phase shift between *I* and *Q* is not exactly 90º, as normally expected for quadrature signals. There is an error of half a cycle of sampling that creates $\theta_{err} = (T_s/2)\times 2\pi f_{IF}$ [25]. This limits image rejection of this structure.

2.3.2 Proposed 4x Sampling

To solve the problem of the DT superheterodyne image introduced by sampling, we proposed advancing to a *4x sampling*, i.e., $f_s = 4f_{LO}$ [14]. Shown in Figure 2-7(a), *I* and *Q* signals

have precisely 90º phase shift after sampling. Although samples with zero value between non-zero samples seem to be non-informative, they are ensuring quadrature accuracy between *I* and *Q*.

Considering the signal spectrum in Figure 2-7(b), the windowed integration filter with its first notch located at $\pm 4f_{LO}$ obviously cannot filter out the image signal. However, this time, the upconverted image (at $2f_{LO} + f_{IF}$) after sampling folds over $-f_s+f_{IF}$, apart from the wanted signal. Therefore, this signal is not aliased after sampling, thus making a clear frequency separation between the wanted signal and its potential image. Then a DT complex bandpass filter (BPF) is able to select the wanted signal and filter the rest of spectrum (dashed-line transfer function in Figure 2-7(b)). The only images that are translated directly on top of the wanted signal are the mixer's odd harmonics images. In this respect, further increasing the sample rate (e.g., to 8x) without using a harmonic rejection mixer would not be beneficial. In [25], an 8x sampling DT mixing architecture is proposed that also implements harmonic rejection.

2.4 Conclusion

As advantages and disadvantages of superheterodyne and zero-IF receiver architectures are compared, superheterodyne receiver with a high IF features a promising future for high performance applications with the recent advancements in CMOS process technology.

The 4x-sampling concept was introduced for superheterodyne architectures which does not inherently make any images other than LO odd harmonics. This image-free sampling will be later used in Chapter 6 to propose a fully integrated DT receiver. The rest of required blocks of such a receiver are introduced in Chapter 3 to Chapter 5.

Chapter 3

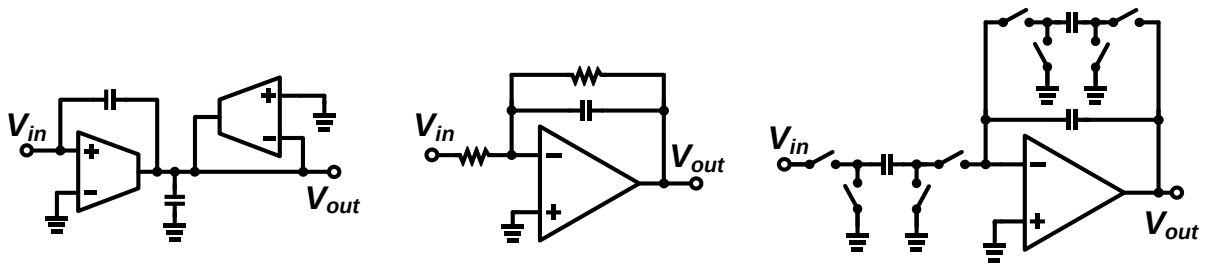
DT High-Order LPF

One of the main building blocks in a receiver is a low-pass filter used at the baseband. This block is responsible for selecting a desired channel. In zero-IF receivers, this block is placed directly after the RF downconversion mixer. In a high-IF receiver, the low-pass filter (LPF) is required after a second downconversion from the IF to baseband. In addition to wireless communication applications [9]–[11], [21], [26]–[28], integrated LPF's are key building blocks in various other types of applications, such as hard-disk drive read channel [29], [30], video signal processing [31], smoothing filtering in a DAC [32], and anti-aliasing filtering before a sampling system. Noise of these filters is one of the key system-level concerns. This noise can be usually traded off with the total filter capacitance and, consequently, total power and area. Therefore, for a given system-level noise budget, a filter with a lower noise coefficient reduces the area and power consumption. On the other hand, linearity of the filter should be high enough to maintain fidelity of the wanted signal.

In this chapter, after a short comparison of different LPF structures, an overview of a basic DT passive LPF is presented. Next, the proposed high-order DT filter [5] is described accompanied by design and implementation of its test chip. At the end, measurement results of the test chip is explained.

3.1 LPF Structures

As shown is Figure 3-1, three types of commonly used analog filters are: Gm-C, active RC



(a) *(b)* *(c)*

Figure 3-1: Conventional analog filters: (a) Gm-C (b) active-RC and (c) active switched-capacitor.

and active switched-capacitor (SC) filters [33]–[38]. In Gm-C and active RC filters, pole/zero locations are set by g_m value, capacitance (C) and resistance (R). Due to the poor matching of g_m/C, and R/C values, process-voltage-temperature (PVT) variations have considerable impact on filter transfer function. Therefore, many applications require component (i.e., g_m, R and C) calibration/tuning [37], [38]. However, pole/zero locations of active SC filters are accurately set by capacitor ratio, thus minimizing the effect of PVT variations.

Implementation of such filters in deep nanoscale CMOS is getting increasingly difficult, especially due to the design challenges of high-quality opamps and high linearity gm-cells. In contrast, switching performance of MOS transistors is getting improved due to the technology scaling. Consequently, passive switched-capacitor filters are expected to work at much higher sampling rates than do the active SC filters, where the speed is limited to opamp settling. Also, the passive filters will consume much less power. However, it might not be possible to synthesis complex poles in a fully passive structure.

A passive LPF proposed in this chapter benefits from these advantages. Using a sampling capacitor to rotate charge between several history capacitors, a high-order IIR low-pass filter is created. To further increase sampling rate, a pipelining technique of the sampling capacitor is introduced. Using these techniques, a 7^{th}-order LPF is implemented, that operates up to 1GS/s [4]. In [9]–[11], [26], [27], passive switched-capacitor FIR/IIR filters have been used for baseband signal processing of an RF receiver. However, none of the prior publications have proposed such a high-order passive filtering in one stage. A somewhat similar structure resembling the charge rotating filter has been reported in [39]. However, a 3^{rd}-order LPF filter is used in an N-path filter to form a band-pass transfer function. Furthermore, its LPF does not

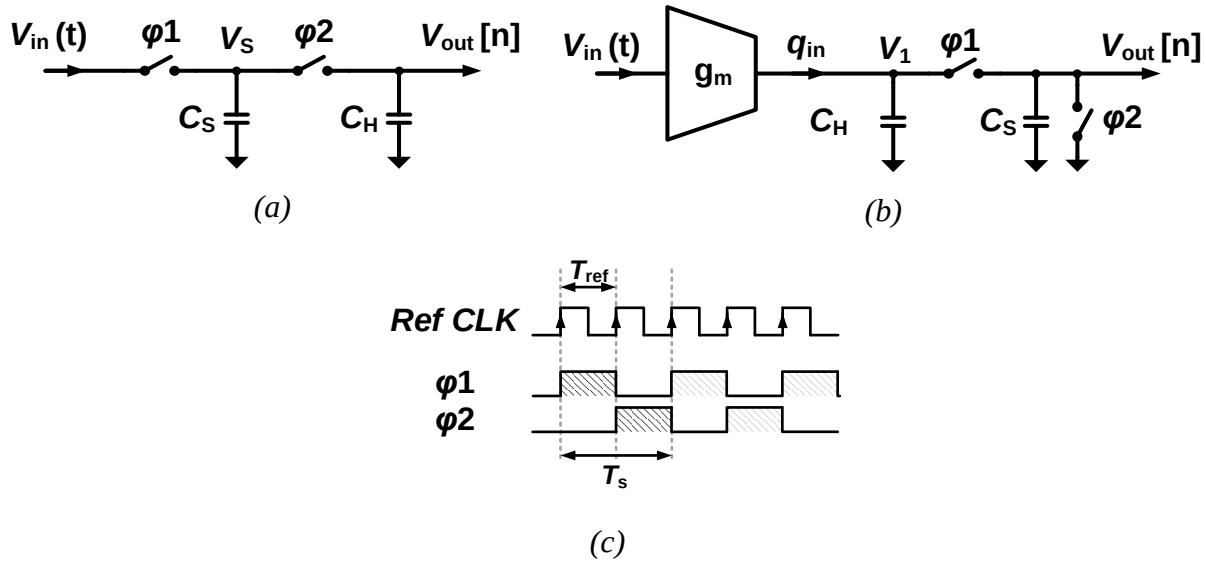


Figure 3-2: (a) Voltage sampling and (b) charge sampling 1st-order DT IIR filter with (c) their clock waveforms.

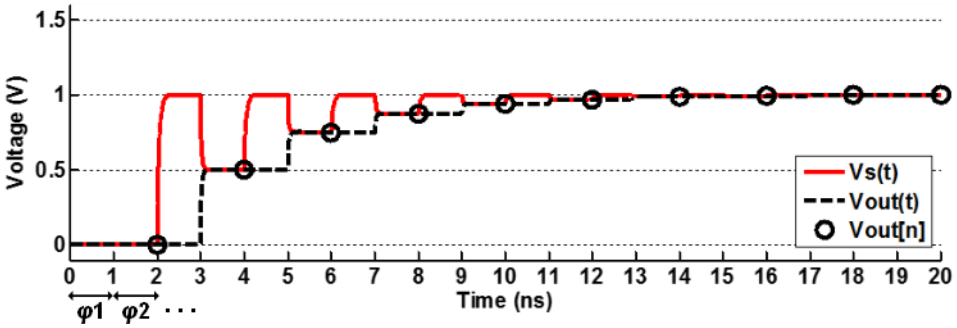
exploit any pipeline techniques such as one introduced in this work.

The proposed filter has a very low input-referred noise, because of using only one sampling capacitor for all the filtering stages. Thanks to the passive operation, is has an extremely high linearity. A simple invertor-based gm-cell might be used in front of this filter to provide gain. This filter consists of only switches, capacitors, clock waveform generator and a simple gm-cell. Therefore it is amenable to the digital deep nanoscale CMOS technology. The proposed filter has been successfully verified at the system level in a discrete-time superheterodyne receiver [21]: The 6th-order charge-rotating filter is employed there as the first baseband channel selection filter.

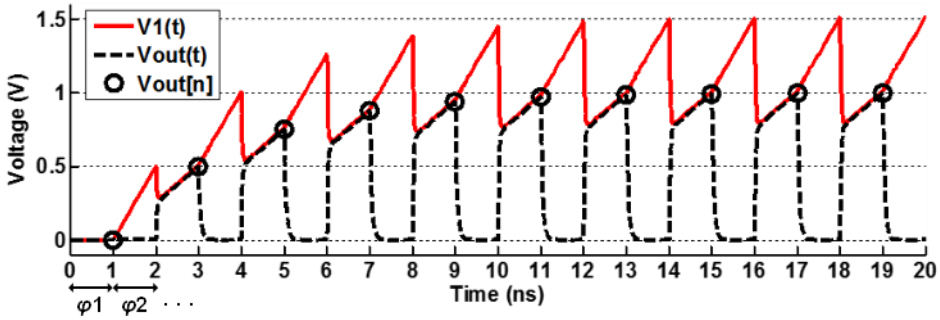
3.2 Basic Discrete-Time Low-Pass IIR Filters

3.2.1 First-Order Filter

Perhaps the simplest analog discrete-time (DT) filter is a passive first-order IIR low-pass filter, as depicted in Figure 3-2(a) [40]. In each cycle at $\varphi 1$, a sampling capacitor C_S samples a continuous-time input voltage $V_{in}(t)$. Hence, it is called a *voltage* sampling filter. Then at $\varphi 2$, C_S shares its stored charge with a history capacitor C_H. At the end of $\varphi 2$, we have the following equation for the discrete-time output voltage:



(a)



(b)

Figure 3-3: Step response of (a) the voltage sampling, and (b) charge sampling 1st-order DT filter (C_H=C_S=1 pF, g_m=0.5 mS, f_{ref} = 1 GHz, and f_s=500 MS/s).

$$V_{out}[n]=\frac{C_H}{C_H+C_S}V_{out}[n-1]+\frac{C_S}{C_H+C_S}V_{in}[n-0.5] \tag{3.1}$$

Hence, its transfer function can be written in z-domain as:

$$\frac{V_{out}(z)}{V_{in}(z)}=\frac{(1-\alpha)z^{-0.5}}{1-\alpha z^{-1}}, \tag{3.2}$$

where, coefficient α is $C_H/(C_H+C_S)$. This is a standard form of a DT low-pass filter (LPF) with unity dc gain and half-a-cycle delay, $T_s/2$. Switch driving clock waveforms are shown in Figure 3-2(c).

Step response of this filter is shown in Figure 3-3(a). C_S and C_H are chosen 1pF each, just for illustration sake. Discrete-time output samples are available in each cycle at the end of $\varphi 2$.

Figure 3-2(b) shows an alternative 1st-order DT LPF (IIR1) exploiting *charge* sampling [10], [40], [41]. At first, the continuous-time input voltage is converted into current by the gm-cell of transconductance gain g_m. This current is integrated over a time window T_s on C_H and C_S during $\varphi 1$ and on C_H during $\varphi 2$. However, we can assume for simplicity that discrete-time input charge packets arrive only at $\varphi 1$:

$$q_{in}[n] = \int_{(n-1)T_s}^{nT_s} g_m V_{in}(t) \cdot dt\,, \tag{3.3}$$

Although this assumption slightly changes transient waveforms of C_H and C_S voltages, it leads to exactly the same values of the output samples while simplifying the analysis of the filter. During $\varphi 1$, C_H shares its charge with Cs and a new charge is input. Consequently, we have the DT output samples at the end of $\varphi 1$:

$$V_{out}[n] = \frac{C_H}{C_H + C_S} V_{out}[n-1] + \frac{1}{C_H + C_S} q_{in}[n], \tag{3.4}$$

$$\frac{V_{out}(z)}{q_{in}(z)} = \frac{1}{C_S} \times \frac{1-\alpha}{1-\alpha z^{-1}}\,. \tag{3.5}$$

Step response of this filter is drawn in Figure 3-3(b). In this example, C_S and C_H are 1pF and g_m is 0.5mS. At first, suppose that voltage at C_H is zero. The input step voltage appears at 1ns and causes a constant 0.5mA current from the gm-cell. This current is integrated on C_H during $\varphi 2$. Also at this time, C_S is reset to zero. Then, at $\varphi 1$, C_H is connected to C_S thus sharing its charge. During $\varphi 1$, the input current is integrated on both capacitors. At the end of $\varphi 1$ (i.e., at 3 ns) an output sample of 0.5V is produced. Likewise, it is transferred to the next cycles thus producing 0.75V, 0.875, etc., as output samples.

In the above two structures, C_S behaves like a lossy component that leaks a time-averaged current from C_H to ground. We might call it a *DT resistor* (a.k.a., *switched-cap resistor*). This resistor in parallel with the capacitor makes a first order low-pass filter.

Figure 3-4 shows top-level behavioral models of the IIR1 filters. In the voltage-sampling structure of Figure 3-4(a), the sampler first samples the continuous-time (CT) analog input voltage $V_{in}(t)$ at $\varphi 1$ and converts it into a DT analog voltage. Then, this signal is fed to a first-order LPF with half-a-cycle delay ($z^{-1/2}$) and the output comes out every cycle at $\varphi 2$. DC voltage gain of this filter is unity. Based on the Nyquist sampling theory, sampling of a CT signal folds frequencies around $k \times f_s$ (for k = 1, 2, 3 …) into around dc, where f_s is the sampling frequency. As depicted in Figure 3-5(a), we observe the folding image frequencies at f_s, $2f_s$ and so on. Figure 3-5(b) shows the transfer function, which has a roll-off of 20dB/dec.

Behavioral model of the charge-sampling IIR1 is depicted in Figure 3-4(b). Integrating the gm-cell current in the time window, as described in (3), forms a CT *sinc*-type antialiasing filter

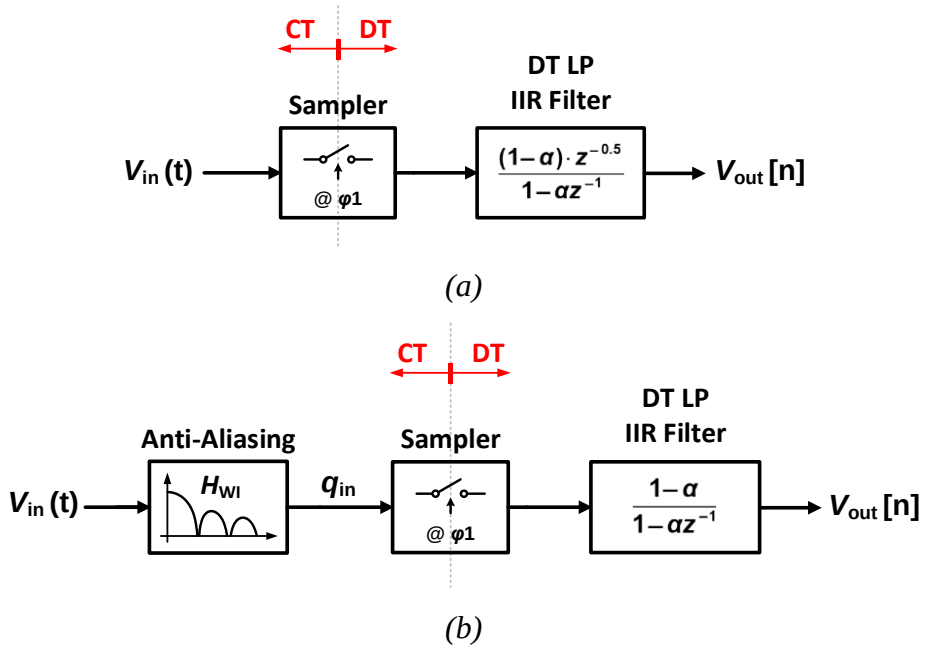


Figure 3-4: Top-level block diagram model of (a) voltage sampling, and (b) charge sampling IIR1.

prior to sampling [10], [40]–[42]. Transfer function of this windowed integration (WI) from the input voltage to the output charge is:

$$H_{WI}(f) = g_m T_s \times \frac{\sin(\pi f T_s)}{\pi f T_s}. \tag{3.6}$$

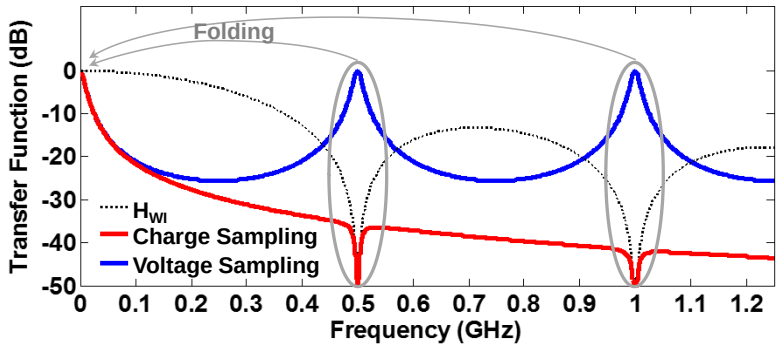
This *sinc*-shape filter has notch frequencies at k/T_i (k =1, 2, 3, …). Assuming ideal clock waveforms, T_i is the same as T_s=1/f_s. In next step, the sampler converts the CT signal to a DT signal and, at the end, a 1st-order DT LPF performs the main filtering. As shown in Figure 3-5(a), notch frequencies of the antialiasing filter are on top of the folding image frequencies thus offering some protection. DC voltage gain is calculated by multiplying the dc gain of the antialiasing filter by the dc gain of the DT filter:

$$A_V = \frac{V_{out}}{V_{in}} = g_m T_i \times \frac{1}{C_S} = g_m \times \frac{1}{C_S f_s}. \tag{3.7}$$

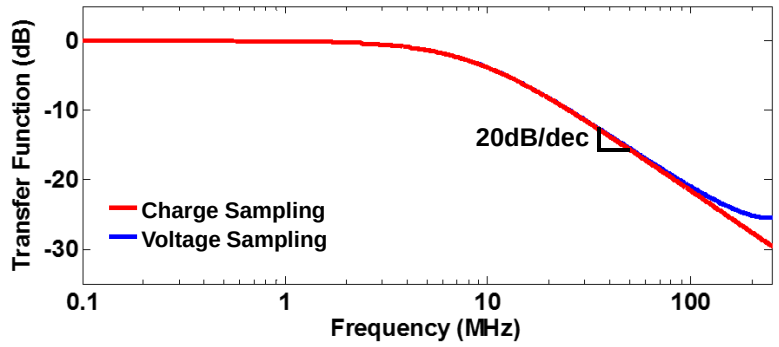
In this equation, 1/($C_S f_s$) is an equivalent DT resistance of the sampling capacitor.

3.2.2 Second-Order Filter

As shown in Figure 3-6(a), a second-order DT low-pass filter (IIR2) can be synthesized by adding a second history capacitor to the charge sampling 1st-order LPF [9], [26], [28], [40]. The previously analyzed charge sampling filter, IIR1, is indicated here within the blue dotted box.



(a)



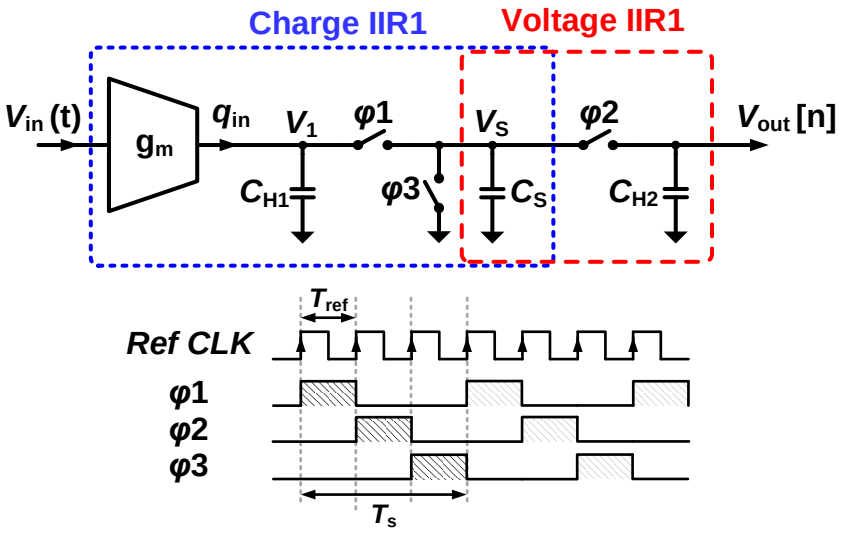
(b)

Figure 3-5: (a) Wideband transfer function, and (b) Bode plot frequency response of IIR1 (C_S=1 pF, C_H=9 pF, g_m=0.5 mS, f_{ref} =1 GHz, and f_s=500 MS/s).

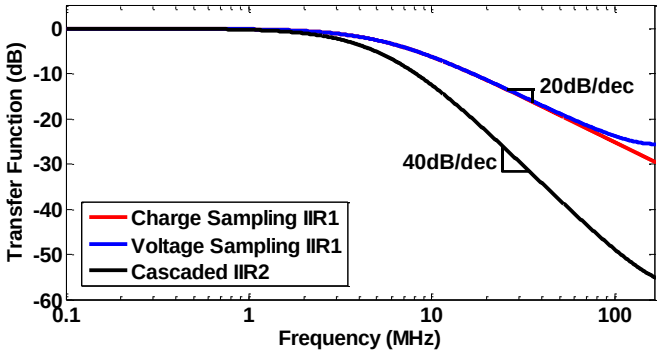
At the end of $\varphi 1$, C_S contains the output sample of the IIR1. Then, by connecting C_S to a second history capacitor C_{H2} at $\varphi 2$, another 1st-order LPF is formed, whose structure is indicated within the red dashed box in Figure 3-6(a). Then at $\varphi 3$, the remaining history of C_S is cleared by discharging it to ground. This ensures proper operation of the first IIR1.

In this filter, the voltage-sampling IIR1 has been cascaded with the charge-sampling one, raising the total order of the filter to the 2nd-order. It should be noted that cascading two CT conventional filter stages without any loading effect would require an active buffer to isolate the first stage from the second stage. In contrast, in the DT filter of Figure 3-6(a) there is an inherent reverse isolation between the stages through a time-slot separation, which does not require a separate active buffer. This is due to the time switching sequence and reset of C_S at the end of each cycle. In this way, the charge is only transferred from left to right and, therefore, we thus obtain the reverse isolation.

Charge sharing equations of this filter at the end of $\varphi 2$ are:



(a)



(b)

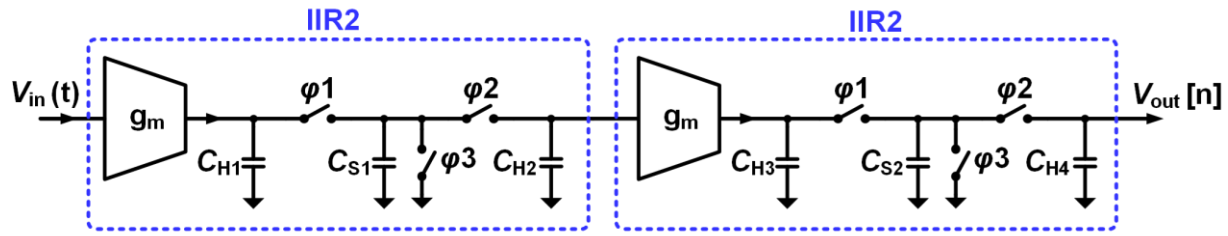
Figure 3-6: (a) Second-order DT low-pass filter and (b) its frequency response (C_H=C_S=1 pF, g_m=0.33 mS, f_{ref} =1 GHz, and f_s=333 MS/s).

$$\begin{cases} V_{out}[n] = \dfrac{C_{H2}}{C_{H2}+C_S} V_{out}[n-1] + \dfrac{C_S}{C_{H2}+C_S} V_1\left[n-\tfrac{1}{3}\right] \\ V_1\left[n-\tfrac{1}{3}\right] = \dfrac{C_{H1}}{C_{H1}+C_S} V_1\left[n-\tfrac{1}{3}-1\right] + \dfrac{1}{C_{H1}+C_S} q_{in}\left[n-\tfrac{1}{3}\right] \end{cases}, \tag{3.8}$$

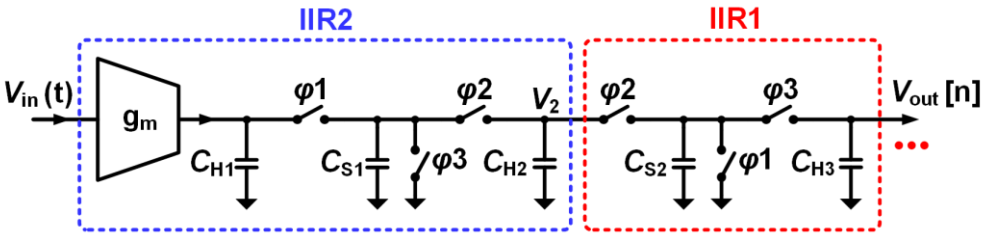
which produces the filter transfer function

$$\frac{V_{out}}{q_{in}} = \frac{1}{C_S} \cdot \left(\frac{1-\alpha_1}{1-\alpha_1 z^{-1}} \times \frac{(1-\alpha_2) z^{-\frac{1}{3}}}{1-\alpha_2 z^{-1}} \right), \tag{3.9}$$

where $\alpha_{1,2}$=$C_{H1,2}$/($C_{H1,2}$+C_S). This results in the same dc gain as (3.7). Transfer function of this filter is plotted on Figure 3-6(b). The 2nd-order IIR filter has a 2x steeper slope of 40dB/dec compared to the IIR1 with 20dB/dec.



(a)



(b)

Figure 3-7: (a) 4th-order filter synthesized by cascading two IIR2. (b) 3th-order filter synthesized by resampling output of an IIR2.

3.2.3 Higher-Order Filters

Many applications require higher orders of filtering. The easiest way to build a high-order filter is to cascade two or more first and/or second-order filters. Figure 3-7(a) shows a 4th-order filter synthesized by cascading two identical IIR2 filter stages. A similar approach has been used in [10] and [27], where two gm-cells and passive filters are cascaded. This higher order is achieved at a cost of a higher power consumption. Since nonlinearities of the first and second IIR2 filters are added together, linearity is also worsened. Similarly, the total input-referred noise of this filter is higher than a single IIR2.

Another way of increasing the filter order is to cascade the IIR2 filter with a passive 1st-order switched-capacitor filter. Figure 3-7(b) shows this concept in which a 3rd-order filter is synthesized by cascading the IIR2 and an IIR1. A similar concept is used in [10] and [11], where two passive SC filters are cascaded. The filter in Figure 3-7(b) works as follows: At the end of $\varphi 1$, C_{S1} holds the sample of first-order filtered signal. Then at $\varphi 2$, it is connected to C_{H2} to perform charge-sharing. At the same time, a second sampling capacitor C_{S2} that was empty before, is also connected to C_{H2} to resample the result of the second-order filtering. Therefore, C_{S1} shares its charge with both C_{H2} and C_{S2}. Afterwards at $\varphi 3$, C_{S2} that contains the sample of the IIR2, shares its charge with a third history capacitor C_{H3}. This sharing makes another 1st-

order IIR filtering, which is cascaded with the previous IIR2, thus giving rise to the 3rd-order filtering. To have proper cascading of the IIR2 and IIR1, we require a reverse isolation between them. Hence, at $\varphi 1$ of the next cycle, C_{S2} is discharged to zero to clear its remaining charge. This way, is does not transfer any charge back to C_{H2} at $\varphi 2$. The cascaded 1st-order filter is indicated with dotted line at the right side of Figure 3-7(b). Several of the IIR1 blocks can be cascaded to achieve higher orders. This filter has the following transfer function:

$$\frac{V_{out}}{q_{in}} = \frac{1}{C_{S1}+C_{S2}} \cdot \left(\frac{1-\alpha_1}{1-\alpha_1 z^{-1}} \times \frac{1-\alpha_2}{1-\alpha_2 z^{-1}} \times \frac{1-\alpha_3}{1-\alpha_3 z^{-1}} \times z^{-\frac{2}{3}} \right), \tag{3.10}$$

where

$$\alpha_1 = \frac{C_{H1}}{C_{H1}+C_{S1}}, \quad \alpha_2 = \frac{C_{H2}}{C_{H2}+C_{S1}+C_{S2}}, \quad \alpha_3 = \frac{C_{H3}}{C_{H3}+C_{S2}}. \tag{3.11}$$

The main drawback of this structure is a gain loss. Comparing (3.10) and (3.9), this 3rd-order filter has a lower dc gain than the IIR2, caused by the second sampling capacitor C_{S2}. It leaks part of the system charge to ground in addition to the resetting of C_{S1} and, therefore, introduces more loss. Input-referred noise of this structure is also higher versus that of IIR2. First, because of extra noise of the IIR1 part in Figure 3-7(a). Second, because of the lowered gain of its preceding stage. In contrast, linearity of the filter is almost the same because the switched-capacitor circuit cascaded with IIR2 is extremely linear compared to the gm-cell active circuitry.

3.3 The Proposed High-Order DT IIR Low-Pass Filter

The above reasoning makes it apparent that extending the IIR filter order using the conventional approach carries two serious disadvantages: First, the increased reset-induced charge loss lowers the gain and signal-to-noise ratio. Second, the active buffers between the stages worsen both the noise and the linearity. We propose a new structure that does not suffer from these two handicaps.

3.3.1 Charge Rotating DT Filter

Before introducing a new high-order filter, the IIR2 is redrawn in Figure 3-8(a). C_S is placed at the center of the (yet incomplete) circle. In each cycle, C_S is "rotating" clockwise and is sequentially connecting to C_{H1}, C_{H2} and then ground.

To extend this idea [5], we add in Figure 3-8(b) a few phase slots between $\varphi 2$ and the last

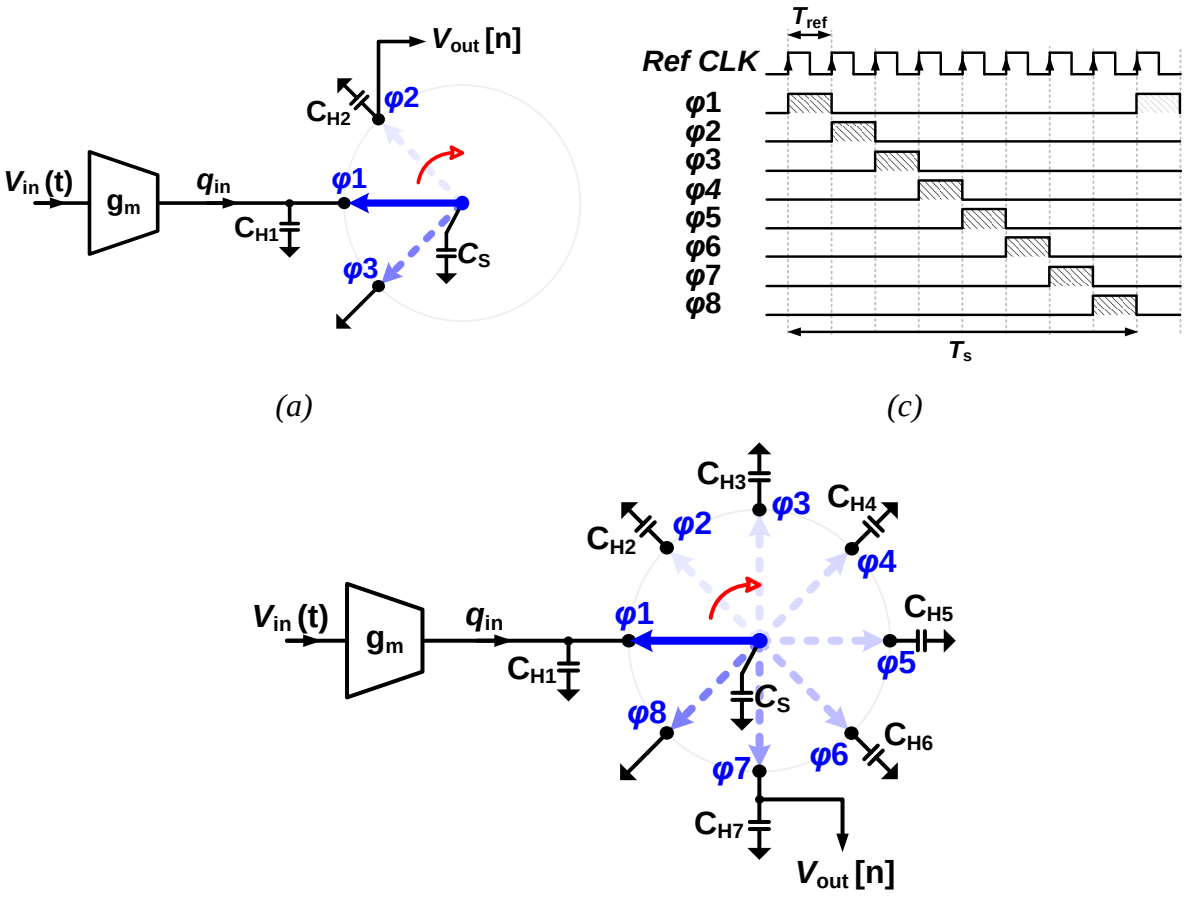
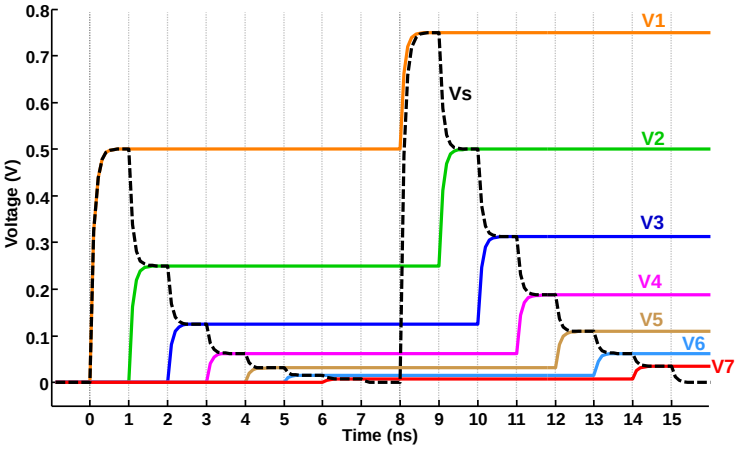


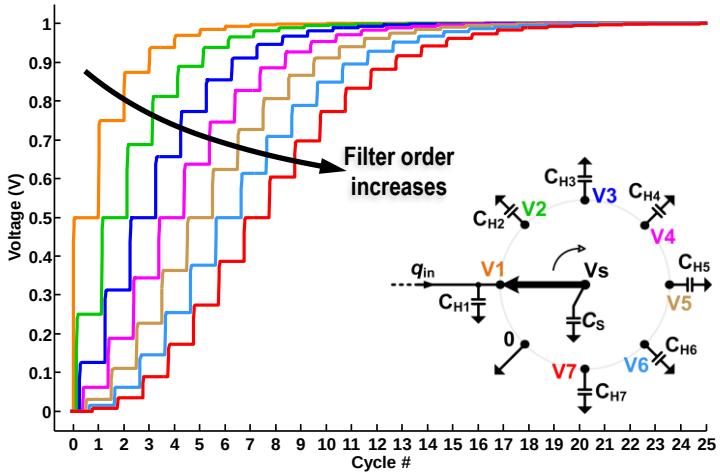
Figure 3-8: (a) The IIR2 is redrawn. (b) Charge rotating 7th-order filter with (c) its clock waveforms. A closed switch is shown with a solid arrow, and an open switch is shown with a dimmed dashed.

reset phase, together with more history capacitors. By moving to the next new phase, $\varphi 3$, C_S which now holds the sample of the 2nd-order filter, shares its charge with a third history capacitor C_{H3}. This charge sharing creates another IIR1, cascaded with the previous IIR2. Hence, we now have a 3rd-order filtering function on C_{H3} that can be read out at the end of $\varphi 3$. We can continue doing so until the seventh history capacitor C_{H7} (or arbitrarily higher), in order to make a 7th-order filter. In the last phase $\varphi 8$, C_S is finally reset. Since the C_S capacitor rotates charge between the history capacitors, we call this structure a "charge rotating" DT filter. As shown at the bottom of Figure 3-8(c), required multiphase clock waveforms to drive the switches can be generated from a reference clock.

Proper cascading of seven 1st-order IIR filters in this structure, requires reverse isolation between them. This reverse isolation is provided by rotating C_S located at the center of the



(a)



(b)

Figure 3-9: (a) A zoom-in and (b) the whole step response of the charge rotating IIR7 (C_H=C_S=1 pF, g_m=0.125 mS, f_{ref} =1 GHz, and f_s=125 MS/s).

structure only in one direction (i.e. clockwise here). Also, the resetting phase at the end of each cycle is necessary to prevent transferring charge from the last stage, C_{H7}, to the first stage at the next cycle.

Compared to the IIR2 structure in Figure 3-6(a), the new charge rotating (CR) structure preserves its gain and linearity even at much higher filtering orders. Gain remains the same simply because no additional charge loss occurs in the system. In this filter structure, the switched-capacitor circuit is remarkably linear and so the gm-cell appears to be the bottleneck of the linearity. Also, the CR filter has the same noise as IIR2, which will be discussed.

3.3.2 Step Response

To better understand the operation of the filter, its step response is plotted in Figure 3-9. At

first, suppose all the capacitors are empty. For simplicity, we choose C_S=C_H=1pF. Also, we suppose that the input charge packet q_{in}[n]=1pC arrives every cycle at φ1. A zoom-in of the step response is plotted in Figure 3-9(a). At φ1, the input charge is transferred to C_{H1} and C_S that sets the 0.5 V potential on both capacitors. C_S which contains a sample of the 1st-order filter at the end of φ1, is then connected to C_{H2} at φ2. The result is 0.25V on both capacitors. Next at φ3, C_S containing the sample of the 2nd-order filter is connected to C_{H3} and the result is 0.125V. In this way, C_S transfers charge from one history capacitor to the next until C_{H7}. Then, it gets reset at φ8. As plotted in Figure 3-9(b), the outputs of higher-order stages are growing more slowly. This is because their respective input sample has been accumulated several times earlier, meaning slower but longer and smoother integration.

3.3.3 Transfer Function

Considering that samples of the main output V_{out}=V_7 are ready at the end of φ7, we have:

$$\begin{cases} @\varphi 7:\ V_7[n]=\dfrac{C_{H7}}{C_{H7}+C_S}V_7[n-1]+\dfrac{C_S}{C_{H7}+C_S}V_6\left[n-\frac{1}{8}\right] \\ @\varphi 6:\ V_6\left[n-\frac{1}{8}\right]=\dfrac{C_{H6}}{C_{H6}+C_S}V_6\left[n-\frac{1}{8}-1\right]+\dfrac{C_S}{C_{H6}+C_S}V_5\left[n-\frac{2}{8}\right] \\ \vdots \\ @\varphi 2:\ V_2\left[n-\frac{5}{8}\right]=\dfrac{C_{H2}}{C_{H2}+C_S}V_2\left[n-\frac{5}{8}-1\right]+\dfrac{C_S}{C_{H2}+C_S}V_1\left[n-\frac{6}{8}\right] \\ @\varphi 1:\ V_1\left[n-\frac{6}{8}\right]=\dfrac{C_{H1}}{C_{H1}+C_S}V_1\left[n-\frac{6}{8}-1\right]+\dfrac{1}{C_{H1}+C_S}q_{in}\left[n-\frac{6}{8}\right] \end{cases} \quad (3.12)$$

In these equations, each -1/8 in the discrete-time argument means one phase delay. At φ7, V_7 is a function of its value at previous cycle (-1 delay) and a sample V_6 that comes from the previous phase (-1/8 delay). Likewise, charge sharing equations from φ1 to φ6 are derived. Converting all these equations into z-domain, we can derive the following general equation for different outputs:

$$H_k(z)=\frac{V_k}{q_{in}}=\frac{1}{C_S}\cdot z^{-\frac{k-1}{8}}\cdot\prod_{i=1}^{k}\frac{1-\alpha_i}{1-\alpha_i z^{-1}}, \quad (3.13)$$

for k=1,2, …,7. In this equation, α_i=$C_{H,i}$/($C_{H,i}$+C_S). Normally, we prefer to have all the poles identical and so we choose all the history capacitors of the same size $C_{H1\text{-}7}$=C_H. Then transfer function of the main output (i.e., V_7) is simplified to:

$$H(z)=\frac{V_{out}}{q_{in}}=\frac{1}{C_S}\cdot z^{-\frac{6}{8}}\cdot\left(\frac{1-\alpha}{1-\alpha z^{-1}}\right)^7. \tag{3.14}$$

From this equation, dc gain of V_{out} from the input charge, q_{in}, is $1/C_S$. Then, by using (6), the overall dc gain of this filter from the input voltage to its output is:

$$A_V=\frac{V_{out}}{V_{in}}=g_m T_i\times\frac{1}{C_S}=g_m\times\frac{1}{C_S f_s}. \tag{3.15}$$

In this equation, $T_i=T_s$ is the time period of the cycle, i.e., the 8 phases. Also, $1/(C_S f_s)$ is an equivalent dc resistance of the sampling capacitor. This filter has the same dc gain as the IIR2 filter in (7).

For frequencies much lower than f_s, we can use bilinear transform to obtain the continuous-time transfer function of the filter:

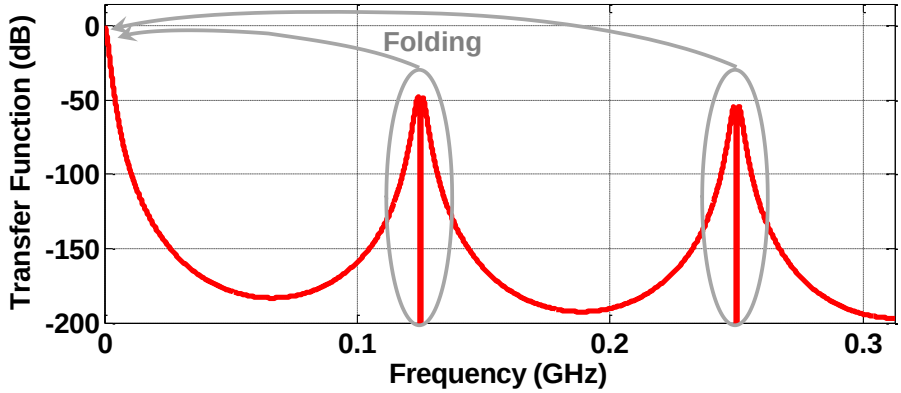
$$\frac{V_k(s)}{V_{in}(s)}=A_V\times\frac{1}{\left(1+\frac{1}{C_S f_s}\cdot C_H\cdot s\right)^k}. \tag{3.16}$$

This equation is similar to a transfer function of an RC LPF, i.e., $1/(1+RCs)$. Poles of this equation are all located at $s = -C_S f_s/C_H$. It indicates that bandwidth of this filter only depends on ratio of capacitors and the sampling frequency, thus making it much less sensitive to PVT variations. This salient feature eliminates any need of calibration, which is necessary for other filter types [33]–[38].

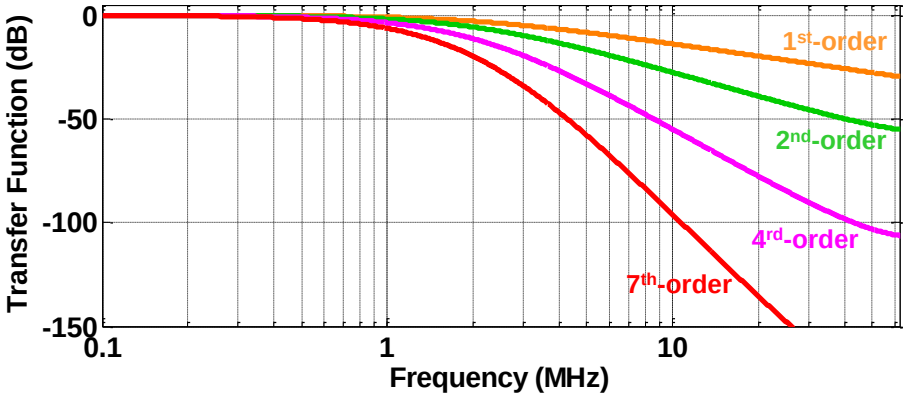
Wideband transfer function of this filter is plotted in Figure 3-10(a). Similar to Figure 3-4(b), the antialiasing filter attenuates signals around f_s, $2f_s$, and so on, before the sampling folds them to dc. Also, transfer functions at outputs of different orders are shown in Figure 3-10(b). The slope of the 7th-order output transfer function reaches a maximum of 140dB/dec for far-out frequencies.

3.3.4 Equalization of the Transfer Function

In many applications, the wanted signal could be accompanied by a strong interferer. Analog-intensive receivers traditionally use continuous-time (CT) Butterworth or Chebyshev type of filters with complex conjugate poles to select the wanted channel out of adjacent channels while filtering out interferers and blockers. In this way, most of the filtering is done in the CT analog domain, and a low dynamic range ADC can be used afterwards. However, digitally intensive DT



(a)

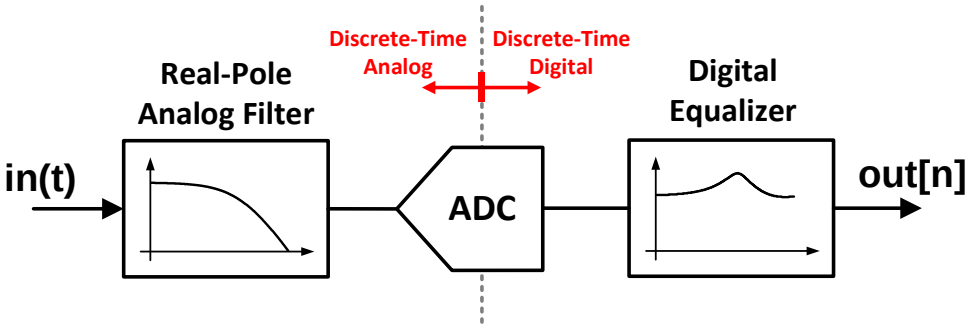


(b)

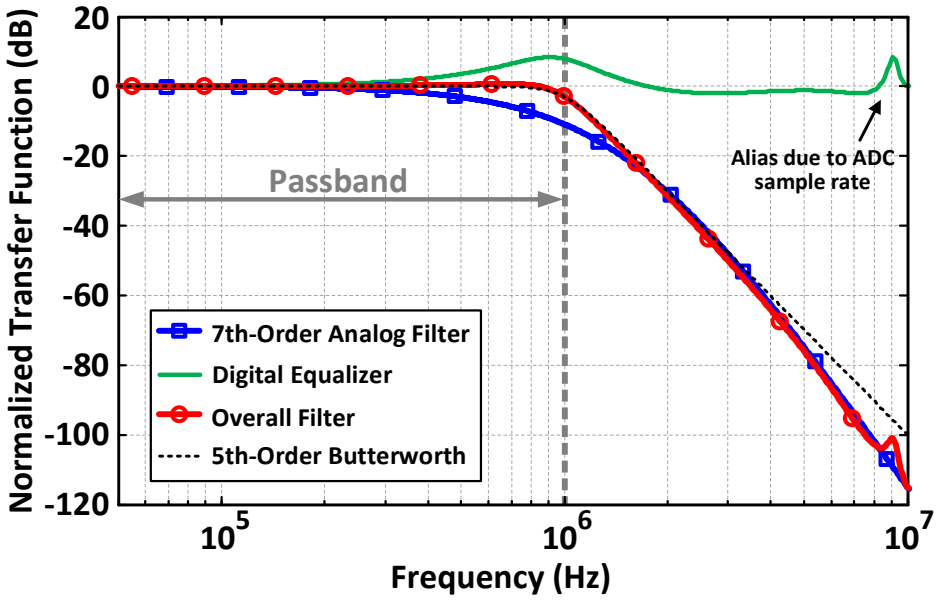
Figure 3-10: Bode plot frequency response of the CR IIR7 (C_S=1 pF, C_H=9 pF, g_m=0.125 mS, f_{ref} =1 GHz, and f_s=125 MS/s).

receivers distribute the channel select filtering between the pre-ADC analog filter and post-ADC digital filter. In [9]–[11], [21], [26]–[28], 2^{nd}/3^{rd}/6^{th}-order real-pole analog filters are used before the ADC, and the rest of filtering is done in digital domain with minimum power consumption. Considering a 3-dB BW, the transfer function of real-pole filters exhibits a gradual and smooth transition region between the flat pass-band into the sharp roll-off (see Figure 3-11(b)). Therefore, the real-pole filters are used mostly to filter far-out interferers/blockers, while they have a moderate selectivity between wanted and adjacent channels.

The proposed DT CR filter could be converted *at the system level* to a sharp high selectivity filter (e.g. Butterworth) with digital assistance in the form of post-emphasis equalizer. The idea is to "pull in" the 3-dB cutoff frequency transition region of the analog filter to well within the channel and digitally compensate for the extra droop at the channel edges. The gradual roll-off region of the analog filter is masked by flattening it out in digital domain such that only the sharp



(a)



(b)

Figure 3-11: (a) Proposed system for digital equalization of the filter transfer function. (b) An example of equalizing transfer function of a 7th-order real-poles DT CR filter and comparison with a 5th-order Butterworth.

roll-off remains. Figure 3-11(a) shows the concept. The digital equalizer can be an all-pass IIR filter with 0 dB gain and a small peaking at a certain frequency, thus of insignificant incremental area and power penalty, especially in scaled CMOS. Transfer function of this filter is easily calculated by dividing the targeted total transfer function by the transfer function of the analog CR filter. In practice, its transfer function is merged with the existing digital part of the channel select filtering, sample-rate decimation, VGA, offset cancellation, I/Q mismatch compensation and demodulation [9], [26], [28].

An example is shown in Figure 3-11(b). The equalizer is designed to map the 7th-order real-pole transfer function of the CR filter to a 5th-order Butterworth filter. The goal of this mapping is to flatten the passband of the overall transfer function, while keeping it unchanged or better

Table 3-1: Mapping of the 7th order real-pole IIR filter to the overall (i.e., analog and digital) 5th to 7th order Butterworth filter of 1 MHz 3-dB bandwidth ($BW_{overall}$).

Order of mapped Butterworth (1 MHz BW)	**5th**	**6th**	**7th**
3dB BW of analog filter (7th-order, real-pole)	490 kHz	415 kHz	340 kHz
Gain loss (RMS averaged within 1MHz BW)	4.9 dB	7.2 dB	11.2 dB
Attenuation of analog filter @ 2 / 4 MHz	31 / 64 dB	37 / 75 dB	43 / 85 dB

for far-out frequencies. To maximally reduce power consumption, the digital equalizer operates in this example at a decimated rate of 10 MS/s while the analog CR filter runs at 800 MS/s. Note that the CR filter also serves as an effective anti-aliasing filter for the decimation.

The overall transfer function (including the analog filter and the digital equalizer) has a higher 3-dB bandwidth ($BW_{overall}$) than the real-pole analog filter itself (BW_{analog}). Consequently, the input signal undergoes some attenuation by the analog filter inside the overall passband, which is compensated by the small peaking of the digital equalizer. While the signal experiences an overall flat transfer function within the passband, the peaking increases noise at the transition region frequencies of both the analog filter and the ADC to some extent. To be able to compare the overall filter with a stand-alone CT analog filter, we consider that the overall filter transfer function is lumped before the ADC, but with a gain loss caused by the analog filter. This loss is equal to the RMS averaged value of transfer function of the digital equalizer within $BW_{overall}$.

Table 3-1 summarizes the analog gain loss for three different digital equalizers that map the 7th-order real-pole IIR filter to the 5th- to 7th-order Butterworth filters with a target 3-dB $BW_{overall}$ of 1 MHz. Due to large over-sampling ratio (800MS/s compared to the filter BW), the reported gain losses remain almost the same in case BW_{analog} and $BW_{overall}$ are scaled proportionally. In equalization into 5th-order Butterworth, for example, a 490 kHz BW_{analog} is used to reach 1 MHz $BW_{overall}$, while 4.9 MHz BW_{analog} can be used for 10 MHz $BW_{overall}$. Since in both cases the filtering profile is similar, passband gain loss remains almost the same 4.9dB (from Table 3-1).

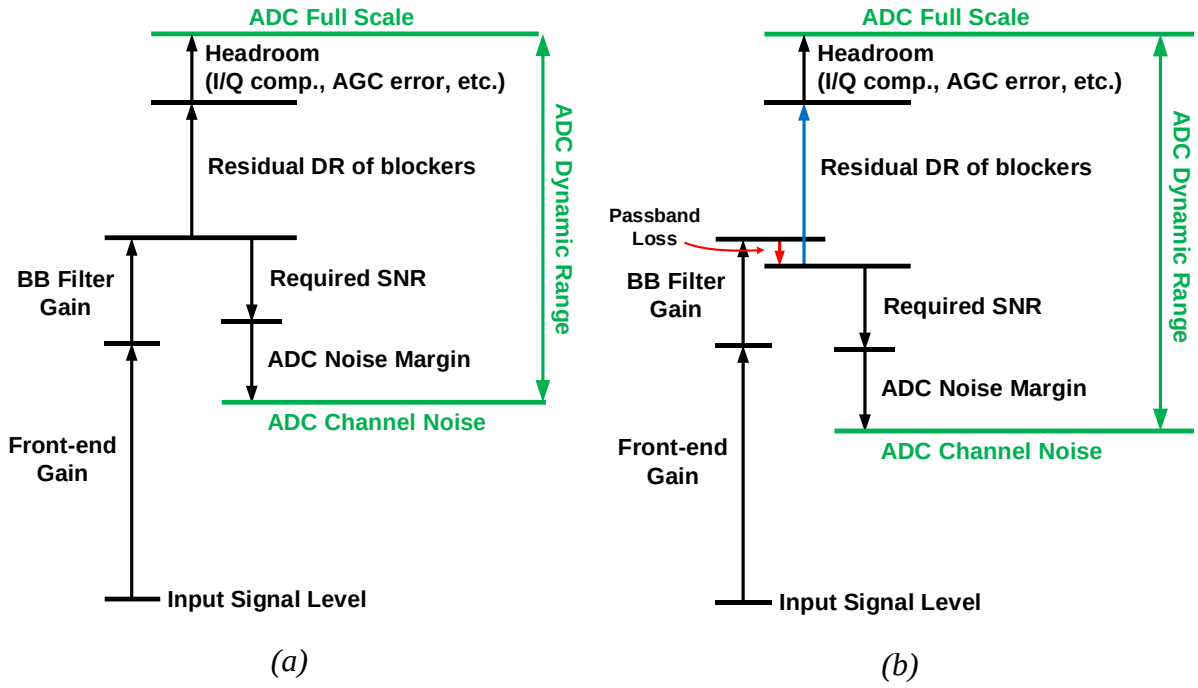


Figure 3-12: ADC dynamic range calculation considering a baseband filter (a) without, and (b) with passband loss.

Depending on the application, the order of the analog filter and the mapped transfer function should be chosen in a way that provides enough analog stopband attenuation and minimizes gain loss.

As this filter has passband loss for specific spot frequencies, it increases input-referred noise of the ADC at such spot frequencies. Therefore, a straightforward suggestion (i.e., rule-of-thumb) is to compensate this effect by increasing gain of the frond-end (before the filter) or the filter itself by the same amount. This suggestion holds very well for reasonably small droop values and when decreasing the filter order (e.g. going from 7^{th}-order real-pole to 5^{th}-order Butterworth).

However, in a communication channel one needs to consider interferers/blockers. There, not only the channel noise of the ADC in considered, but also its dynamic range (DR) in order to absorb residual blockers. As shown in Figure 3-11(b), "absolute" out-of-band blocker attenuation of the real-pole filter is the same (or better) than the mapped Butterworth filter. However, the real-pole filter has an average passband gain loss. So, its "relative" blocker attenuation is lowered by this loss. Figure 3-12 compares the required ADC dynamic range for two cases of a baseband filter without and with passband loss (i.e. Butterworth and real-pole

filters, respectively). When the filter has a passband loss, dynamic range of the blockers at its output is increased by the same amount (see red and blue arrows in Figure 3-12). So, the ADC full scale remains the same. However, the required ADC channel noise is reduced. So, the ADC needs an extra dynamic range equal to the amount of average passband gain loss. If one uses a higher front-end gain to return the ADC channel noise to its original value, it increases the ADC full scale level by the same amount. Hence, in this case, the ADC requires the same amount of extra dynamic range. Therefore, the ADC could require 0.8 to 1.8 extra ENOB (1 bit per 6 dB loss) when the transfer function is mapped to the 5^{th}- to 7^{th}-order Butterworth, respectively. However, under certain circumstances in which the equalized TF has a higher attenuation than the desired one (e.g., far-out blockers and when decreasing the filter order from 7^{th}-order real-pole to 5^{th}-order Butterworth; e.g., for frequencies higher than 4MHz in Figure 3-11(b)), the DR loss can be prevented altogether.

3.3.5 Sampling Rate Increase

Sampling rate of the Figure 3-8(b) CR filter is one sample per cycle, with each cycle comprising 8 phases. Therefore, the sampling frequency f_s is $f_{ref}/8$. By increasing the sampling rate, the frequency folding would be pushed higher, thus making it less of a concern. Also, the filter can achieve a wider bandwidth.

Operation of the CR IIR7 filter as shown in Figure 3-8(b) can be considered as 8 different stages in series. As new data arrives at $\varphi 1$, it is sequentially processed at each stage until $\varphi 8$. Only then the next data sample arrives. In this way, we have not used the full capacity (data rate) of each stage. For example, while the data is being processed at $\varphi 7$ on C_{H7}, other capacitors, C_{H1} to C_{H6}, are unused awaiting a new sample. As history capacitors $C_{H1\text{-}7}$ are holding the data between different stages, we are able to readily increase the data rate by *pipelining*.

Suppose that instead of only one C_S, we have now 8 sampling capacitors, each of them connected to one of the "history" nodes. Then, by going to the next phase, all of them are moving to the next node in the clockwise direction. At each new phase of this pipeline structure, a new data ($q_{in}[n]$) comes into C_{H1}, a new data is transferred from C_{H1} to C_{H2}, from C_{H2} to C_{H3} and so on until C_{H7}, and one sampling capacitor is reset to ground. Therefore, a new data comes in and a new data comes out at each phase (instead of each cycle). In this way, functionality of the filter

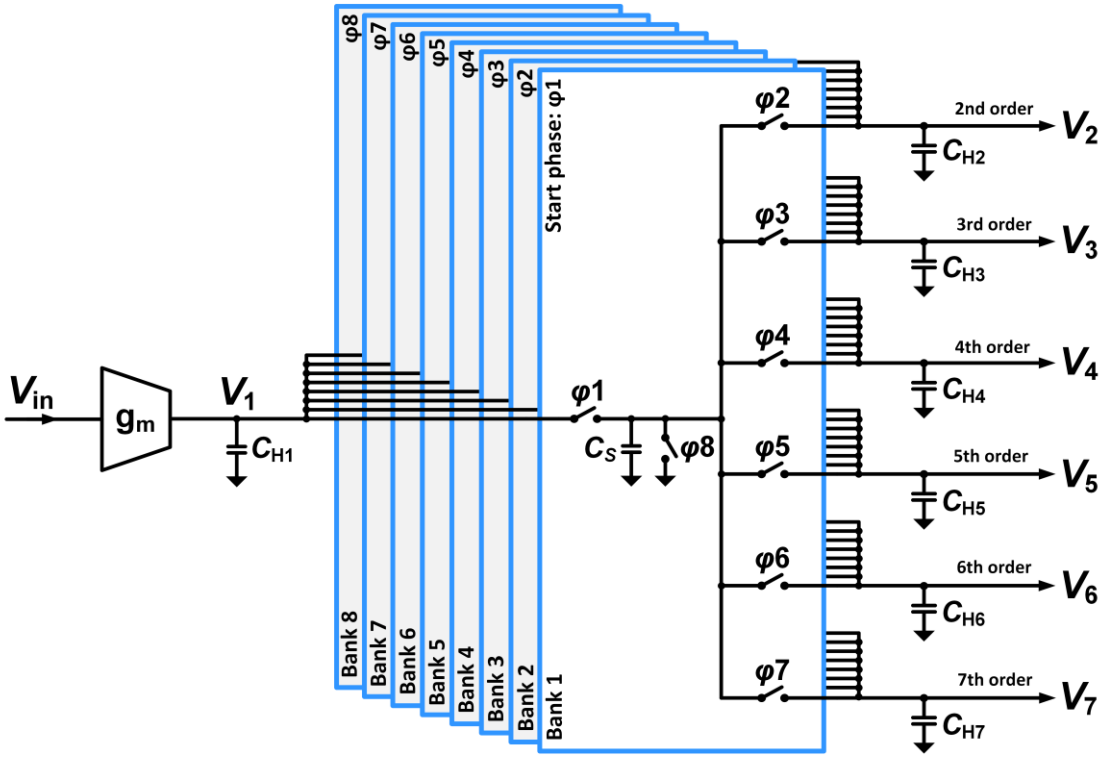


Figure 3-13: Full-rate CR IIR7 filter using pipelining ($f_s=f_{ref}$).

has not changed while its sampling rate has increased by 8 times ($f_s=f_{ref}$). Schematic of this full-rate CR IIR7 filter is shown in Figure 3-13. For each sampling capacitor and its rotation network, a separate switch bank is used.

The pipeline SC structure has the same charge sharing, transfer function and gain equations as (8)-(11), but with replacing each 1/8 delay with a unit delay and considering the new f_s.

In this filter, if there is a mismatch between different C_H, it would slightly shift the pole locations. Since these capacitors have typically a large value and are of the same type, they are very well matched, thus removing the matching concern. However, if the mismatch exists between the different C_S in the pipeline structure, it could alias some amount of signal from harmonics of $f_{ref}/8$ inside the passband. However, any signal around the harmonics is filtered before the aliasing. In practice, this non-ideal effect is too small to be observed.

3.3.6 Robustness to PVT Variations

Active-RC and gm-C filters are quite sensitive to PVT variations because of poor matching between different types of elements (i.e. resistor, capacitor and gm-cell). However, switched-capacitor filters are quite robust to PVT variations. Transfer function and BW of SC filters are set by capacitor ratio, which are normally implemented of the same device type (e.g., MOS,

MiM, or MoM capacitor). Active-SC filters are very robust to PVT, especially when parasitic capacitance cancellation techniques (e.g. correlated double sampling) are used.

In the proposed passive SC filter, the effective C_S is provided by MoM type of capacitor and also parasitic capacitance of 8 MOS switches connected to it (see Figure 3-13). In this design, 8% to 26% of C_S is the MOS parasitic capacitance, depending on a C_S value selection code. On the other hand, C_H has also some switches to select its value. In this design, MOS parasitic capacitance connected to C_H ranges from 0.5% to 20%, depending on the C_H selection code. Being subject to the PVT variation, MoM part of the effective C_S and C_H track each other very well. Also, their common percentage part of the remaining MOS parasitic capacitance matches well (they are of the same type). The only part that could be affected by PVT variation is the difference between the MOS parasitic capacitance percentages of C_S and C_H. Depending on the selected C_S and C_H codes, this difference is limited to a few percent of the whole capacitance. In this way, PVT variation effect is reduced, but still somewhat higher than an active-SC filter.

3.4 Noise Analysis

Output noise of the charge rotating 7th-order DT filter contains two main contributors: noise of the input gm-cell and noise of the passive switched-capacitor network.

3.4.1 Noise of gm-cell

Figure 3-14 shows a top-level signal flow diagram of the high-order IIR filter. At first, assume that V_{in} is zero for this noise analysis. $\overline{V_{n,gm}^2}$ is an input-referred noise of the gm-cell (see node A in Figure 3-14). Output noise of the gm-cell is shaped by H_{WI} in (3.6) before sampling, (node B in Figure 3-14). The sampling process folds frequencies higher than $f_s/2$ to the fundamental 0-to-$f_s/2$ range. Since the noise in various bands is uncorrelated, their power is added up. It can be shown that the output is a flat noise for a white input noise [11] (node C in Figure 3-14). Power spectral density (PSD) of the sampled noise charge (q_{in}) can be found by equating power of the sampled noise with power of the shaped noise before sampling:

$$\int_0^{f_s/2} \overline{Q_{n,in}^2}\, df = \int_0^{\infty} \overline{V_{n,gm}^2} \times \left|H_{WI}(f)\right|^2 df \ . \tag{3.17}$$

By substituting (3.6) into the above equation and considering $T_i=1/f_s$ in our case, noise PSD of

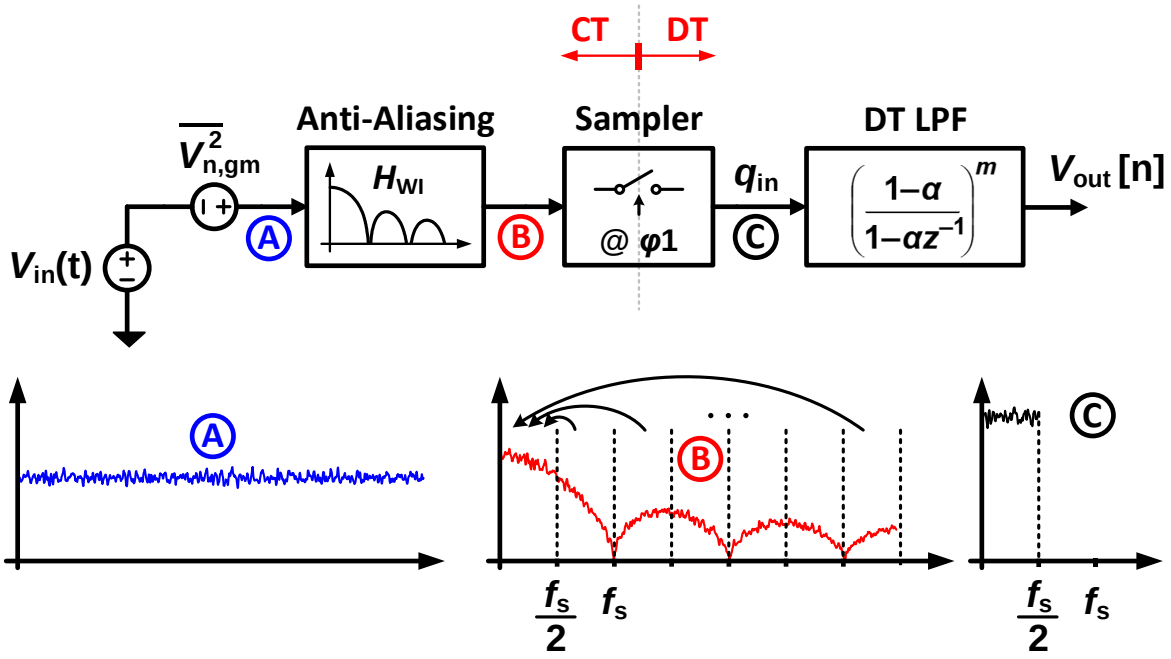


Figure 3-14: Block diagram model of the CR IIR7 for m-th order output. (A) input-referred noise of the gm-cell. (B) The noise shaped by antialiasing filter. (C) Sampled noise fed into DT filter.

the sampled input charge simplifies to:

$$\overline{Q_{n,in}^2} = \frac{g_m^2}{f_s^2}\overline{V_{n,gm}^2}\,. \tag{3.18}$$

The above noise is fed to the switched-capacitor filter and is shaped by its transfer function:

$$\overline{V_{n,out}^2} = |H(z)|^2 \times \overline{Q_{n,in}^2}\,. \tag{3.19}$$

For example, output voltage noise PSD of the CR IIR7 can be calculated by substituting (3.14) and $z=e^{j\Omega} = e^{j2\pi f/fs}$ into (3.19):

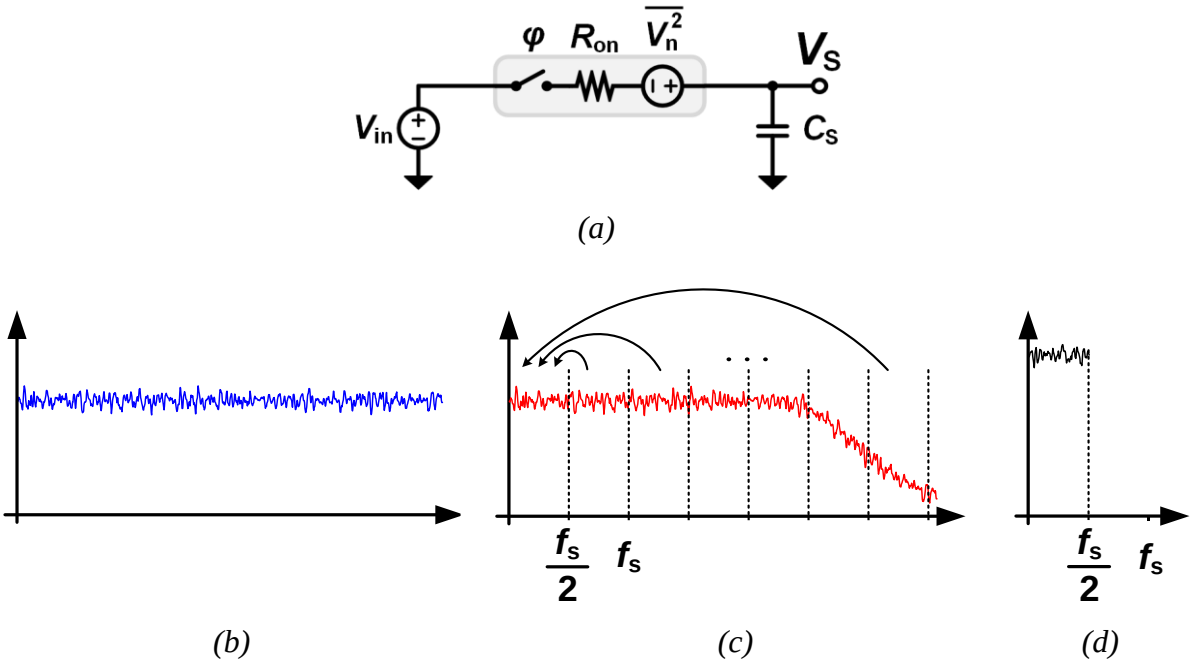
$$\overline{V_{n,out}^2} = \left|\frac{1}{C_S}\cdot e^{-j\frac{6}{8}\Omega}\cdot\left(\frac{1-\alpha}{1-\alpha e^{-j\Omega}}\right)^7\right|^2 \times \frac{g_m^2}{f_s^2}\overline{V_{n,gm}^2}$$

$$= \left(\frac{1-2\alpha+\alpha^2}{1-2\alpha\cos\Omega+\alpha^2}\right)^7 \times \left(\frac{g_m}{C_S f_s}\right)^2 \overline{V_{n,gm}^2}\,. \tag{3.20}$$

In the above equation, $g_m/(C_S f_s)$ is the voltage gain of the filter calculated also in (3.15).

3.4.2 Noise of Switched-Capacitor Network

The second key noise contributor of the filter is from the switched-capacitor network. Before calculating this noise we first discuss noise of a voltage sampling process.



(a)

(b) *(c)* *(d)*

Figure 3-15: (a) Noise circuit model of a voltage sampling process. (b) Noise of switch resistance. (c) The noise shaped by RC filter. (d) Sampled noise.

In Figure 3-15(a), a voltage sampler that includes noise of its switch is drawn. In this circuit, assume that V_{in} is zero. When the switch is on, it has a finite resistance (R_{on}). A series voltage source models the resistor's thermal noise with a constant PSD, as shown in Figure 3-15(b):

$$S_R(f) = 4kTR_{on}, \quad f \geq 0, \tag{3.21}$$

where k is Boltzmann's constant and T is the absolute temperature. When the switch is *on*, noise of the resistor is shaped by the RC filter with a time constant of $\tau = R_{on}C_S$ and then appears at the output. At the moment the switch is disconnected, the output noise is sampled and held on C_S. The sampling causes noise folding from frequency higher than $f_s/2$, to the 0-to-$f_s/2$ range and they are added up, as shown in Figure 3-15(c). If the time constant τ is much lower than "on" duration of the switch, it can be shown that the summation of all folded noise will be flat (i.e., white noise) [43]. As shown in Figure 3-15(d), single-side noise spectral density of the sampled noise at the output is [43]:

$$\overline{V_S^2}(f) = \frac{kT}{C_S \cdot f_s/2}, \quad 0 \leq f \leq f_s/2. \tag{3.22}$$

If we integrate this noise over the entire frequency range, its power is kT/C_S.

To simplify the problem for more complicated switched-capacitor circuits, we can use the following assumption: the continuous-time noise source $\overline{V_n^2}$ with PSD of (3.21), can be

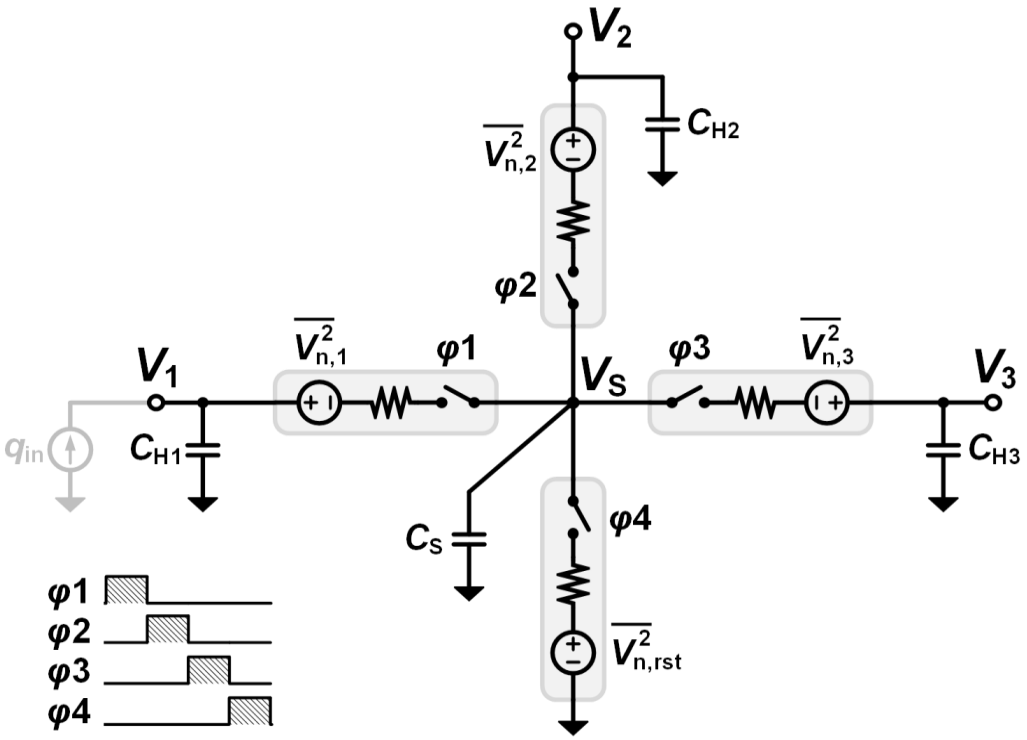


Figure 3-16: Noise model of a charge rotating 3rd-order filter.

considered as a discrete-time noise source with PDS described in (3.22). In this way it is not anymore necessary to consider the effect of RC filter in switched-capacitor noise analysis.

To calculate output noise of the CR IIR7, we first start with a lower order for simplicity, and then extend it to the seventh order. Figure 3-16 shows a charge rotating 3rd-order filter. In this filter, the input current signal is considered zero. The aim of the following calculation is to find the DT output noise at different outputs, i.e. V_1, V_2 and V_3, generated by noise sources $\overline{V_{n,rst}^2}$, $\overline{V_{n,1}^2}$, $\overline{V_{n,2}^2}$ and $\overline{V_{n,3}^2}$. To simply equations, for the rest of calculation we define:

$$\alpha_{1\text{-}3} = \frac{C_{H1\text{-}3}}{C_{H1\text{-}3} + C_S} \ . \tag{3.23}$$

As defined in (22), PSD of $\overline{V_{n,rst}^2}$ is:

$$\overline{V_{n,rst}^2} = \frac{kT}{C_S \cdot f_s / 2} \ . \tag{3.24}$$

However, other noise sources are differently calculated. Since from $\varphi 1$ to $\varphi 3$, C_S is in series with C_{H1} to C_{H3}, the total capacitance at each phase should be taken into account for noise PSD:

$$\overline{V_{n,1\text{-}3}^2} = \frac{kT}{\frac{C_{H1\text{-}3}C_S}{C_{H1\text{-}3}+C_S}\cdot f_s/2} = \frac{kT}{\alpha_{1\text{-}3}C_S\cdot f_s/2} = \frac{\overline{V_{n,rst}^2}}{\alpha_{1\text{-}3}}. \tag{3.25}$$

Sampling frequency, f_s, in the above two equations is the repetition frequency of each phase, equal to $f_{ref}/4$ in this case.

At $\varphi 4$, C_S is reset. In other words, the effects of noise sources at other phases on C_S are all cleared. At the end of this phase, it samples noise of the reset switch $\overline{V_{n,rst}^2}$:

$$@\varphi 4: \quad v_S[n] = v_{n,rst}[n]. \tag{3.26}$$

Then, C_S is connected to C_{H1} at $\varphi 1$. Charge sharing equations at this phase are:

$$@\varphi 1: \quad v_1[n] = \frac{C_{H1}}{C_{H1}+C_S}v_1[n-1] + \frac{C_S}{C_{H1}+C_S}v_{n,1}[n] + \frac{C_S}{C_{H1}+C_S}v_S[n-\tfrac{1}{4}], \tag{3.27}$$

where $v_1[n\text{-}1]$ is the previous history of C_{H1}, $v_S[n\text{-}1/4]$ is a voltage sample of V_S from the previous phase (i.e. $\varphi 4$), and $v_{n,1}[n]$ is noise of switch at $\varphi 1$. Combining the above two equations and (3.23) we obtain:

$$@\varphi 1: \quad v_1[n] = \alpha_1 v_1[n-1] + (1-\alpha_1)v_{n,1}[n] + (1-\alpha_1)v_{n,rst}[n-\tfrac{1}{4}]. \tag{3.28}$$

Now, we can calculate noise transfer functions to the output V_1 by using z-transform:

$$V_1 = \frac{1-\alpha_1}{1-\alpha_1 z^{-1}}V_{n,1} + \frac{(1-\alpha_1)z^{-\frac{1}{4}}}{1-\alpha_1 z^{-1}}V_{n,rst}. \tag{3.29}$$

To see PSD of V_1, we substitute $z=e^{j\Omega}$ and it follows that:

$$\overline{V_1^2}\left(e^{j\Omega}\right) = \left|\frac{1-\alpha_1}{1-\alpha_1 e^{-j\Omega}}\right|^2 \overline{V_{n,1}^2} + \left|\frac{(1-\alpha_1)e^{-\frac{1}{4}j\Omega}}{1-\alpha_1 e^{-j\Omega}}\right|^2 \overline{V_{n,rst}^2}. \tag{3.30}$$

Then, it reduces to:

$$\overline{V_1^2}\left(e^{j\Omega}\right) = \frac{1-2\alpha_1+\alpha_1^2}{1-2\alpha_1\cos\Omega+\alpha_1^2} \times \left(\overline{V_{n,1}^2} + \overline{V_{n,rst}^2}\right). \tag{3.31}$$

Before going to the next phase, we need to calculate the remaining noise on C_S at the time it is disconnecting from C_{H1}:

$$@\varphi 1: \quad v_S[n] = v_1[n] - v_{n,1}[n]. \tag{3.32}$$

Using (3.29), noise transfer function on V_S at the end of $\varphi 1$ is:

$$@\varphi 1:\quad V_S = -\frac{\alpha_1(1-z^{-1})}{1-\alpha_1 z^{-1}}V_{n,1} + \frac{(1-\alpha_1)z^{-\frac{1}{4}}}{1-\alpha_1 z^{-1}}V_{n,rst}\,. \tag{3.33}$$

Then, its noise PSD is simplified to:

$$\overline{V_S^2}\left(e^{j\Omega}\right) = \frac{\alpha_1(2-2\cos\Omega)}{1-2\alpha_1\cos\Omega+\alpha_1^2}\overline{V_{n,1}^2} + \frac{1-2\alpha_1+\alpha_1^2}{1-2\alpha_1\cos\Omega+\alpha_1^2}\overline{V_{n,rst}^2}\,. \tag{3.34}$$

Substituting (3.25) in this equation, it reduces to:

$$\begin{aligned}\overline{V_S^2}\left(e^{j\Omega}\right) &= \left(\frac{\alpha_1(2-2\cos\Omega)}{1-2\alpha_1\cos\Omega+\alpha_1^2}\times\frac{1}{\alpha_1} + \frac{1-2\alpha_1+\alpha_1^2}{1-2\alpha_1\cos\Omega+\alpha_1^2}\right)\times\overline{V_{n,rst}^2} \\ &= 1\times\overline{V_{n,rst}^2}\,.\end{aligned} \tag{3.35}$$

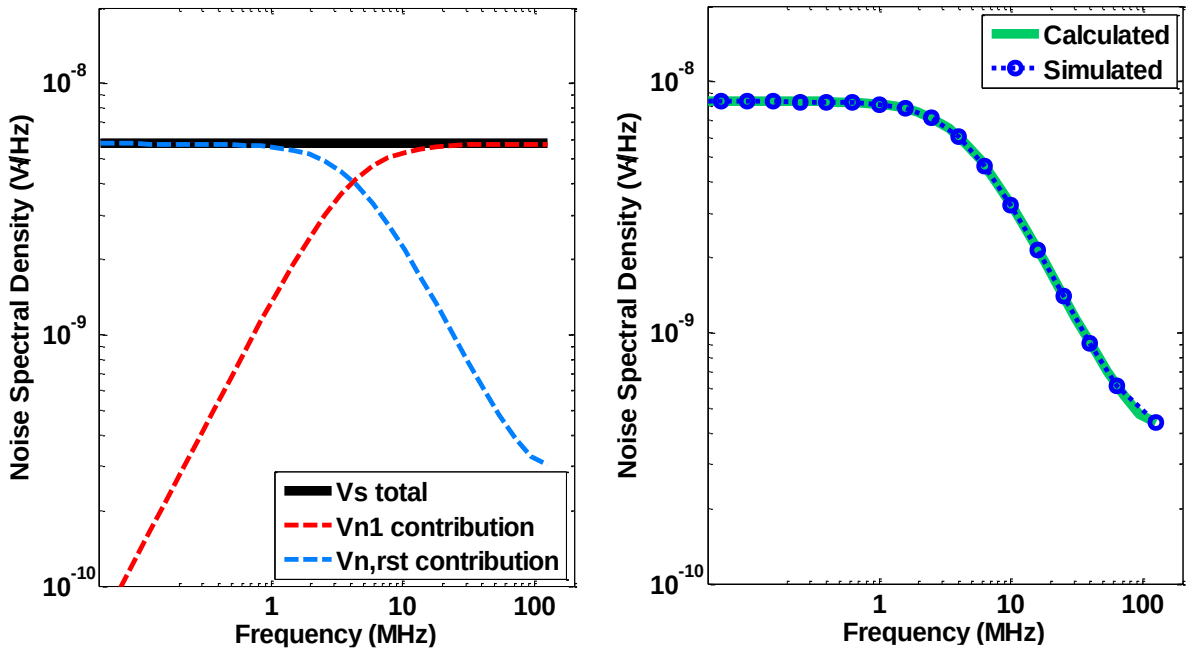
This appears to be a very interesting and important result. It suggests that the noise PSD of V_S at $\varphi 1$ is exactly the same as its PSD at previous phase, $\varphi 4$, which is the reset phase. It can be explained as follows: at the end of $\varphi 4$, V_S has a PSD of $\overline{V_{n,rst}^2}$, which is a flat noise. Next, when C_S is connected to C_{H1} at $\varphi 1$, this noise is low-pass filtered (the second term of (3.34)). However, at this phase a high-pass filtered noise originated from $\overline{V_{n,1}^2}$ is added to V_S (the first term of (3.34)). These two noise contributions are shown in Figure 3-17(a). The latter noise compensates for the attenuated part of the former noise in a way that the total PSD remains constant and equal to the original one, $\overline{V_{n,rst}^2}$. This result is independent of history capacitor value.

Similar to what was described for $\varphi 1$, the same set of equations, (3.27)–(3.35), are valid for other phases executing before the reset phase ($\varphi 4$ in this case). Therefore, in general we have:

$$\overline{V_i^2}\left(e^{j\Omega}\right) = \frac{1-2\alpha_i+\alpha_i^2}{1-2\alpha_i\cos\Omega+\alpha_i^2}\times\left(\overline{V_{n,i}^2}+\overline{V_{n,rst}^2}\right). \tag{3.36}$$

for i=1,2,3 in the CR 3rd-order filter. Also, V_S at the end of each phase has the same noise PSD as calculated in (3.35).

Although it would seem at first that noise of higher order outputs should be increased due to the accumulation of the noise coming from different noise sources, surprisingly, (3.36) rejects this hypothesis. Suppose all the history capacitors are equal, then noise PSD of all different outputs become the same. In other words, it does not built up by going to higher orders. This advantage of DT CR filter is in contrast with conventional filters. For example, in an active-RC filter, more resistors and opamps are required to increase an order thus leading to a higher output



(a) *(b)*

Figure 3-17: (a) Calculated noise spectral density of V_S at the end of $\varphi 1$ and (b) noise spectral density of V_1 (C_S=1 pF, C_H=9 pF, f_{ref} =1 GHz, and f_s=250 MS/s).

noise.

Figure 3-17(b) plots noise spectral density of different outputs with equal C_H. To validate the above equations, noise of the switched-capacitor circuit is simulated by means of Cadence SpectreRF PNOISE simulation. Simulation results match very close to (3.36). An interesting point is that spot noise of the filter for frequencies inside the BW is:

$$\overline{V_i^2}\Big|_{in-band} = 4kT \times \frac{1}{C_S f_s} \tag{3.37}$$

for α near 1, which is noise of the equivalent resistor, $R_{eq}=1/(C_S f_s)$.

Another interesting point is about total noise power of each output:

$$P_{n,i} = \int_0^{f_s/2} \overline{V_i^2}\left(e^{j2\pi f/fs}\right)df = \int_0^{f_s/2} \frac{1-2\alpha_i+\alpha_i^2}{1-2\alpha_i\cos\left(2\pi f/f_s\right)+\alpha_i^2}\left(\overline{V_{n,i}^2}+\overline{V_{n,rst}^2}\right)df$$

$$= \frac{f_s}{2} \times \frac{1-\alpha_i}{1+\alpha_i} \times \left(\overline{V_{n,i}^2}+\overline{V_{n,rst}^2}\right) \quad . \tag{3.38}$$

Using (3.25) it reduces to:

$$P_{n,i} = \frac{f_s}{2} \times \frac{1-\alpha_i}{1+\alpha_i} \times \left(\frac{1}{\alpha_i} + 1 \right) \times \frac{kT}{C_S \cdot f_s / 2} = \frac{kT}{C_{H,i}} \,. \tag{3.39}$$

This result is same as the well-known output noise power of an RC filter that is kT/C.

All the above results and equations are valid and extendable to higher order filters, e.g. the CR IIR7 discussed before and beyond. Note that if pipeline technique is used, all the above equations remain the same except that the new sampling frequency should be used.

3.5 Design and Implementation

The proposed high-order charge-rotating DT filter consists of a gm-cell, switches, capacitors and a clock waveform generator circuit. Therefore, it is amenable to the digital deep nanoscale CMOS technology. If we implement this filter in a finer process, area of the capacitors, switches and the waveform generator reduces while preserving or improving the performance according to Moore's law of scaling.

3.5.1 Design of the 7th-Order Charge Rotating DT Filter

The final design is implemented differentially while, for the sake of simplicity, it is shown single-ended in Figure 3-18. The designed filter is software controlled to operate in one of the two modes: 1) charge-sampling, and 2) voltage-sampling. Although in the charge-sampling mode we have an active gm-cell, the filtering network is fully passive, making the overall filter semi-passive. In the voltage-sampling mode, the gm-cell is bypassed and disconnected from the power supply, resulting in a fully passive filter. Also, C_{H1} is disconnected via "Mode Control" to prevent loading the input. The removal of C_{H1} lowers the filtering order by one to 6th[3]. In this mode, the input voltage (instead of the input charge) is directly sampled by C_S capacitors.

The simple inverter-based gm-cell (Figure 3-19) makes the filter amenable to process scaling. In this pseudo-differential gm-cell, a bias voltage V_{bias} comes from a diode-connected NMOS and mirrors a bias current into the gm-cell. Also, a feedback circuit sets the common-

[3] The 7th-order of the filter in voltage sampling mode can be kept by replacing GND with a history capacitor at $\varphi 8$. However, we did not do this in the current implementation.

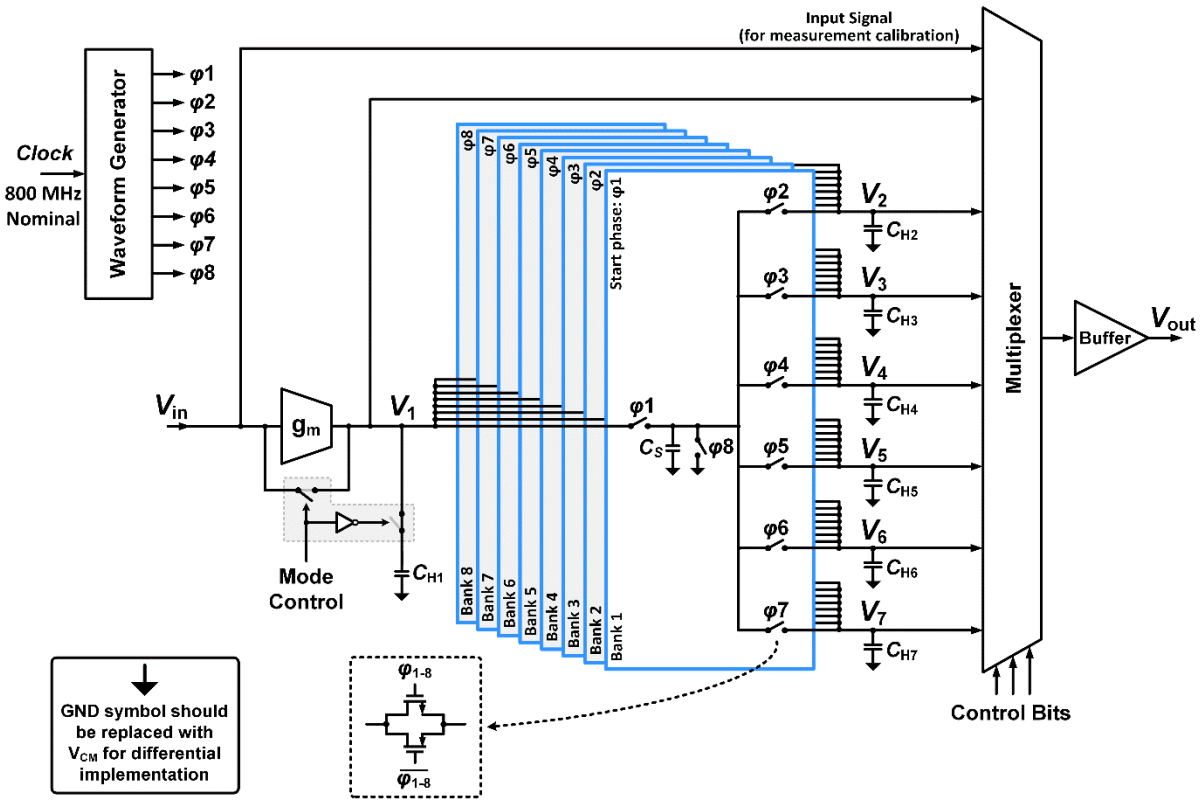


Figure 3-18: Implementation of the full-rate CR IIR7. The circuit has been implemented differentially while it has been shown single-ended here for simplicity.

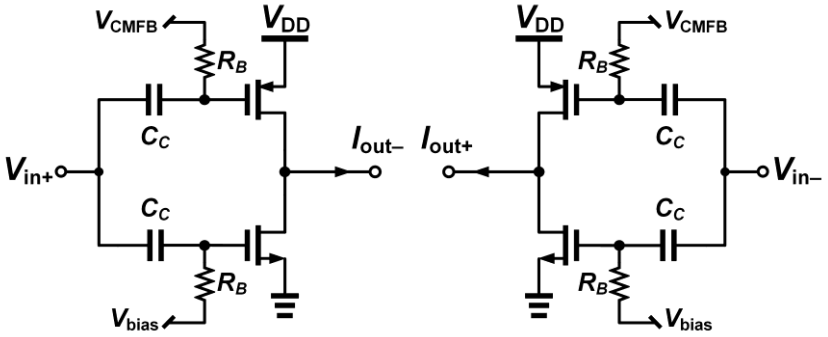


Figure 3-19: Inverter-based pseudo-differential gm-cell.

mode output voltage to $V_{DD}/2$ by adjusting V_{CMFB}. Coupling capacitors C_C and bias resistors R_B set a lower limit in frequency response. By using large C_C and R_B, this limit is pulled down to few kHz, which is acceptable for most applications. As the gm-cell, a simple invertor is used to be amenable to scaling and provide a good linearity. By properly sizing of NMOS and PMOS transistors, their nonlinearities could be canceled out perfectly for square-law transistors [44]. However, in nanoscale CMOS a partial cancellation is carried out. We have used transistors with a large channel length to make their behavior closer to the square-law model. Moreover, a low

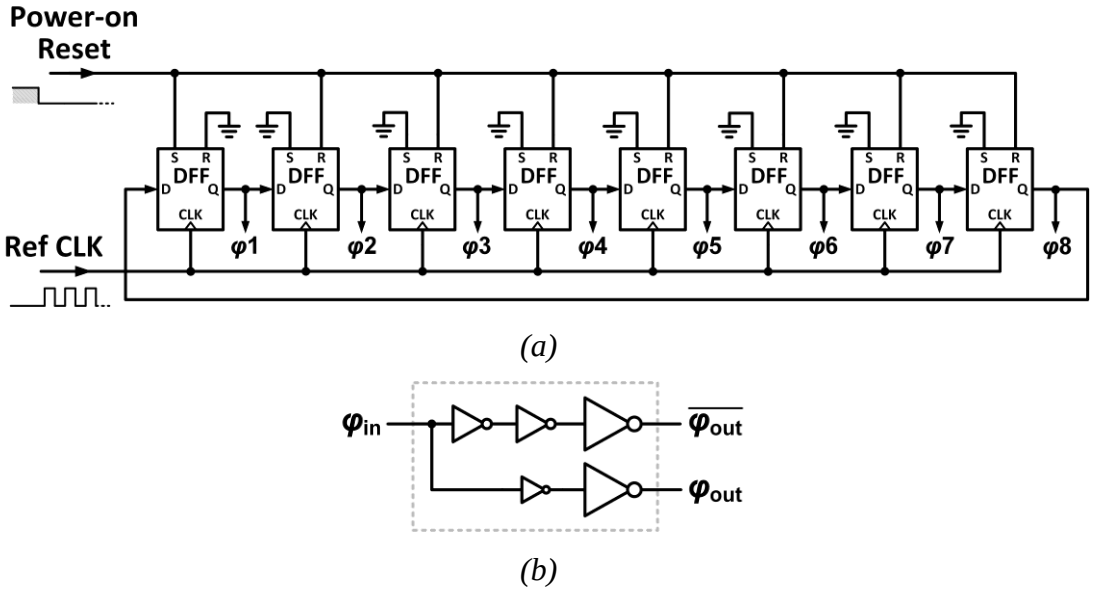


Figure 3-20: (a) Waveform generator circuit with (b) its output buffer.

resistance load by the SC circuit allows a high IIP3.

The differential history capacitors $C_{H1\text{-}7}$ range from 0.25-to-64 pF digitally selectable via 8 bits. For both history and sampling capacitors, we used MOM capacitors to have a very good matching. This minimizes variations due to PVT. Differential value of the sampling capacitors C_S range from 0.4-to-2.2 pF digitally selectable by 4 bits. Instead of implementing C_S differentially, we implement each as two single-ended capacitors. Then we can set common-mode voltage of the filter by terminating C_S to V_{CM} instead of ground. To adjust the filter bandwidth, we keep C_S fixed and change C_H. In this way, both the gain and linearity of the circuit do not change. Also, if the sampling frequency is changed, we change C_S inversely to keep the bandwidth and the gain constant.

As shown in Figure 3-18, the filter's switches are implemented with transmission gates. We have chosen equal NMOS and PMOS sizes to reduce charge injection and cancel out clock feedthrough by at least an order of magnitude [43], [45], and at the same time having a lower on-resistance (R_{on}). To have a low R_{on}, low-V_T transistors are chosen. These transistors should be sized carefully to have a low enough R_{on} for fast settling on the sampling capacitors.

The waveform generator shown in Figure 3-20(a), is a digital logic block. It consists of eight D flip-flops (DFF). At power-on, the DFFs are set/reset to "10000000". Then, at each successive clock cycle, the code is rotated one step. In this way, all the required phases are generated from a reference clock. Outputs of the DFFs are fed to buffer cells before driving the switches

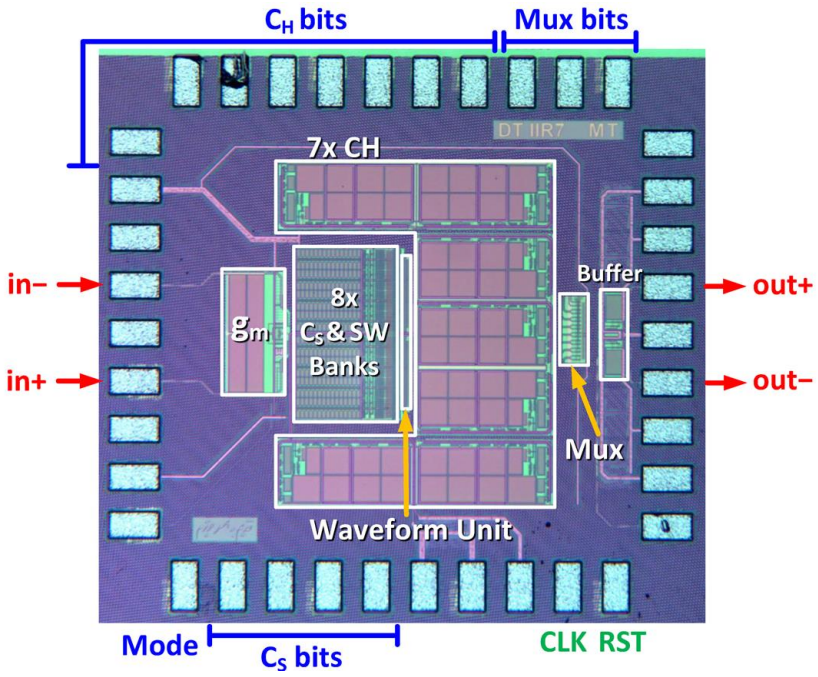


Figure 3-21: Chip micrograph of the full-rate CR IIR7 implemented in TSMC 65nm CMOS. Die size is 1.2×1.27mm.

(Figure 3-20(b)). The buffer is able to drive the switches with sharp rising and falling edges. Size of NMOS and PMOS transistors in the buffer are skewed to ensure non-overlapping between consecutive phases.

3.5.2 Implementation

The filter has been implemented in TSMC 1P7M 65nm CMOS process. It operates at a 1.2V power supply. The gm-cell drains 250μA. The waveform generator unit and its buffers clocked at a reference frequency f_{ref} of 800MHz consume 1.40mA. The latter current consumption is proportional to f_{ref}. The filter has been verified to work properly up to 1 GS/s.

As shown in Figure 3-18, an analog multiplexer is added to allow monitoring different outputs (orders) of the filter as well as the internal on-chip input of the filter. After the multiplexer, an output buffer isolates the chip internals from the outside. Figure 3-21 is a chip micrograph of the implemented filter.

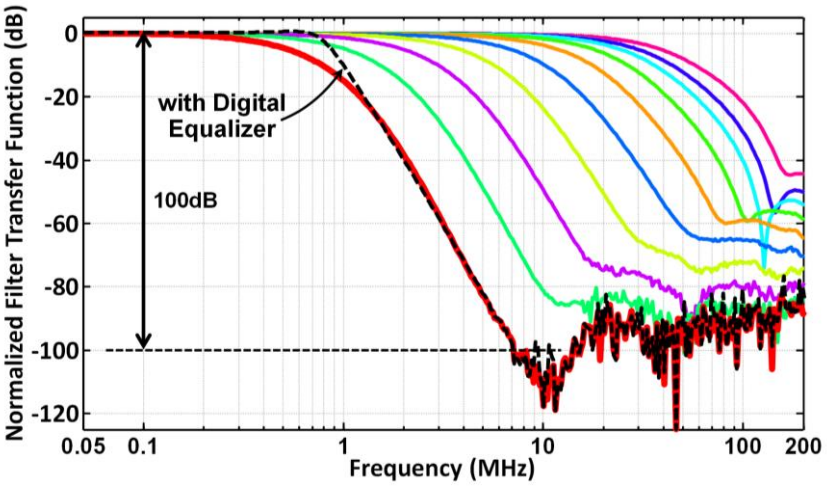
3.6 Measurement Results

To verify the proposed filter, a single-ended input signal is converted to differential with a wideband transformer, terminated with a 50Ω resistor on the PCB and then fed to the chip. Differential output of the chip with zero-order-hold is converted back to a single-ended signal

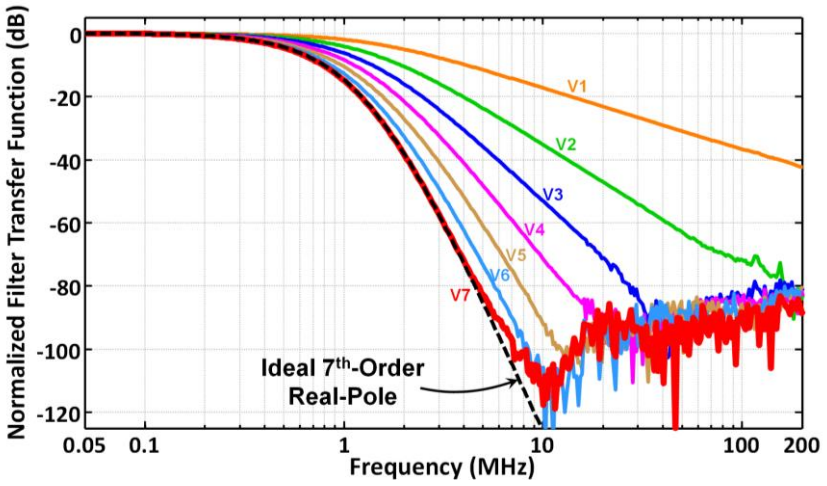
Table 3-2: Performance summary and comparison with state-of-the-art.

	This Work [4], [5]				**JSSC'11 [36]**	**JSSC'10 [35]**	**JSSC'09 [34]**	**JSCC'06 [33]**	**JSSC'06 [37]**	**JSSC'07 [38]**
Topology	DT IIR @ 800MS/s				G_m-C, Low Power Hi. Linearity	G_m-C, Noise Reduction	G_m-C, Wide Tuning	Source Follower	Active RC	Active RC
	Charge-Sampling		Voltage-Sampling							
	without Equalizer	with Equalizer	without Equalizer	with Equalizer						
Technology	65nm		65nm		90nm	90nm	0.18µm	0.18µm	0.12µm	0.13µm
Order	7th	5th	6th	4th	6th	4th	3rd	4th	3rd, 5th	5th
Type	Real Poles	Butter.	Real Poles	Butter.	Butterworth	Butterworth	Butterworth	Butterworth	Cheb. Elliptic	Chebyshev
Supply Voltage (V)	1.2		1.2		1.0	2.5	1.2	1.8	1.0	1.5
Power (mW)	1.98	-	1.68	-	4.35	1.25	4.1 – 11.1*	4.1	4.6	11.25
3dB BW (MHz)	0.4 – 30	0.82 – 61	0.43 – 32	0.77 – 57	8.1 – 13.5	2.8	0.5 – 20	6 – 14	5, 10	8.9, 19.7
Gain (dB)	9.3	4.4	0	-3.5	-2.7	15	0	-3.5	0	2
Max. Stopband Rejection (dB)	>100		>85		≈ 90	55	60	-	50	-
In-band / Out-of-band IIP3 (dBm)	21.7† /11.7‡		24† / 25‡		21.7 – 22.1 / 17.5 – 18.9	10 / 35.6	22.3 – 19 / 17.5 – 13*	18 / 12	18.8 – 21.3/ -	18.3 / -
In-band / Out-of-band IIP2 (dBm)	55† / 60§		61† / 68§		- / 51.9 – 53.4	- / -	40 – 30.8* / -	- / -	- / -	- / -
$P_{1dB,out}$ (dBm)	+10		+13		+3.9	-	-	0.5	-4.1 – 2.6	+7
IRN (nV/√Hz)	4.57	4.72	4.97	7.27	75	22.6	425 – 12*	7.5	85, 143	30
SFDR (dB)	75 – 68*	74 – 66*	82 – 69*	77 – 66*	54.3	58	51 – 61	65	-	55.2
1% HD3 DR (dB)	93 – 81*	91 – 79*	103 – 83*	96 – 78*	63	67	80	79	-	69
Active Area (mm²)	0.42		0.35		0.239	0.5	0.23	0.26	0.17	0.2

* In the same order of the filter BW † 3 MHz and 4 MHz tones ‡ 20 MHz and 35 MHz tones § 30 MHz and 35 MHz tones



(a)

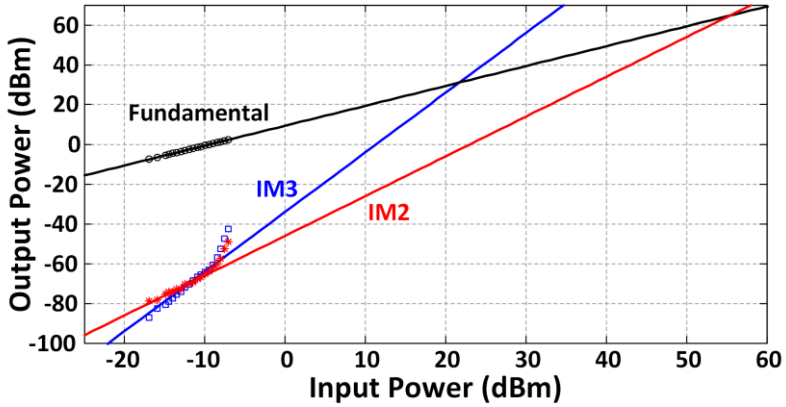


(b)

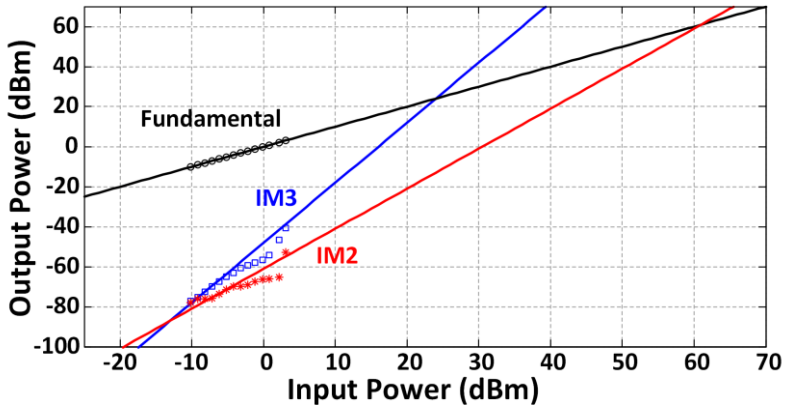
Figure 3-22: Measured transfer function of the CR IIR7 for (a) the 7th-order output with different BW settings, and (b) for different orders in 400 kHz BW setting. The filter is in charge-sampling mode clocked at 800MHz.

with another transformer. Table 3-2 summarizes the filter performance in its two operational modes, including the effects of the suggested digital equalizer, and compares with recent state-of-the-art filters.

Transfer function of the filter has been evaluated using HP8753E network analyzer. To lower the measurement noise floor, a wideband RF amplifier (HP8347A) is used. Figure 3-22(a) plots the measured frequency response of the filter in the charge-sampling mode at the 7th-order output for different bandwidth settings. The 3dB bandwidth is programmable from 400 kHz to 30 MHz. By applying a digital equalizer to map the transfer function to a 5th-order Butterworth, the overall 3-dB bandwidth would be tunable from 0.82 – 61 MHz. As an example, the overall transfer



(a)



(b)

Figure 3-23: In-band IIP2 and IIP3 measurement of the CR IIR7 filter in (a) charge-sampling and (b) voltage-sampling modes.

function including the equalizer is plotted with the black dashed line in Figure 3-22(a). A maximum 100 dB of stop-band rejection is measured for the narrowest bandwidth setting. Depicted in Figure 3-22(b) is the measured transfer function of the filter in the charge-sampling mode, but now for different outputs (orders). In this measurement, the 400 kHz analog bandwidth setting is used. The measured 7^{th}-order output is also compared with the ideal mathematical transfer function shown in the black dashed line, indicating a very good agreement with theory. Transfer function of the filter in the voltage sampling mode is similar to Figure 3-22 except that the filtering order is 6th.

To evaluate linearity of the filter, a two-tone signal is fed to the filter and its output is evaluated by Agilent E4446A spectrum analyzer. For this test, analog bandwidth is set to about 9 MHz. Figure 3-23 shows the measured 2^{nd} and 3^{rd} order intermodulation products versus the input power for both charge-sampling and voltage-sampling modes. Measured in-band IIP2 and IIP3 (with

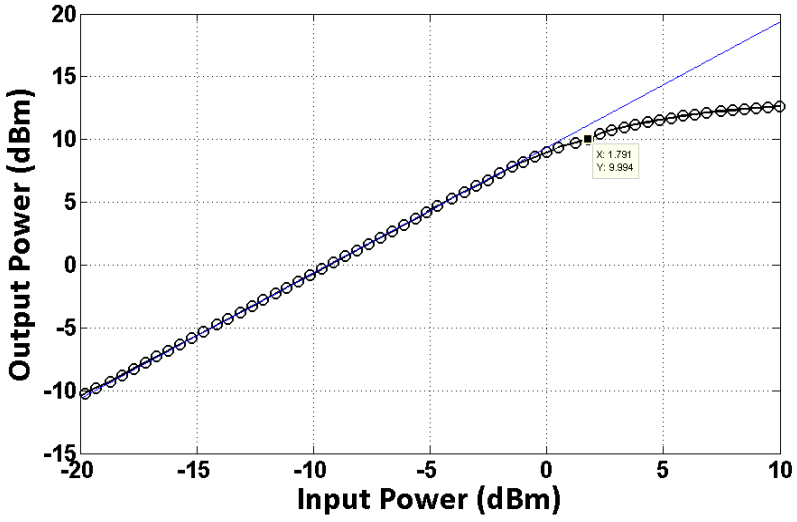
respect to 50Ω) are +55 dBm and +21 dBm in charge-sampling, and +61 dBm and +24 dBm in voltage-sampling mode, respectively. In the charge-sampling mode, where the linearity is limited by the gm-cell, IIP3 might be lowered by a few dBs in practice, caused by PVT variations. As listed in Table 3-2, IIP3/IIP2 in the charge-sampling mode is among the best. Thanks to the fully passive operation, the filter in the voltage-sampling mode has an exceptionally high IIP3/IIP2.

Measured out-of-band IIP2 and IIP3 are +60 dBm and +11.7 dBm in charge-sampling, and +68 dBm and +25 dBm in voltage-sampling mode. IIP3 of an inverter-based gm-cell depends also on its output resistance [46]. The gm-cell is designed to have the best IIP3 when it is loaded with nominal resistance seen from the switched capacitor filter. When out-of-band tones are applied, the gm-cell sees a lower impedance than the nominal value for those frequencies, and therefore its IIP3 is reduced. This is the reason why charge sampling filter has a lower out-of-band linearity than in-band. However, this effect does not exist for voltage sampling mode, resulting in almost the same in-band and out-of-band IIP3.

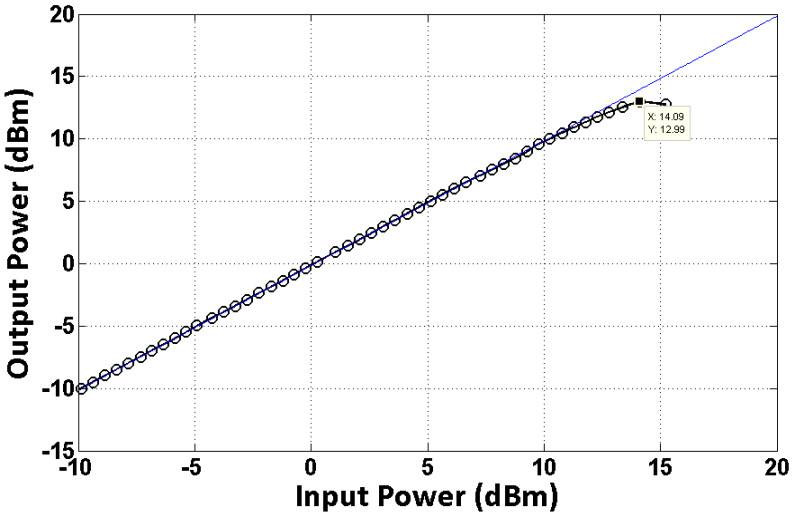
Comparing in-band IIP3 of charge and voltage sampling modes, it seems that IIP3 of voltage sampling should be higher than what reported (due to lower gain than charge sampling). However, the lower IIP3 than expected is caused by the extra switch that shorts the gm-cell in voltage sampling mode (Figure 3-18). This switch in series with the voltage sampling filter has regarded original linearity of the filter.

To be able to fairly compare the 1-dB compression point of our filter in its two operational modes to other filters with various gains, we compare the output compression point as $P_{1dB,out} = P_{1dB,in} + Gain - 1$. Measured output compression point of the filter in the charge-sampling mode is +10 dBm, while in the voltage-sampling mode, this value goes to +13 dBm (Figure 3-24). These are outstanding values compared to other works listed in Table 3-2.

In charge-sampling mode, P_{1dB} of the gm-cell is limited by its output saturation between near 0 and V_{DD}. The $P_{1dB,out}$ of +10dBm is translated to 1V peak-to-peak swing for each of the gm-cells, while V_{DD} is 1.2V. So in this case, P_{1dB} is not only set by 3rd order non-linearity, but also with higher orders caused by output clipping of gm-cell between ~0.1V and ~1.1V. In voltage sampling mode, $P_{1dB,out}$ of +13dBm is equal to ≈1.4V peak-to-peak single-ended swing that exceeding barely the supply limit. This happens thanks to the fully passive structure made of only the switches and capacitors. After this point, bulk diodes of the transistors are starting



(a)



(b)

Figure 3-24: Measured P_{1dB} (a) in charge-sampling and (b) voltage-sampling modes.

leaking current and compressing signal. Furthermore, $P_{1dB,in}$ = +14dBm in this mode is also very close to typical prediction of $P_{1dB,in}$ = IIP3 - 10.

Noise of the filter is evaluated by the spectrum analyzer. For this measurement, input of the filter is grounded. A two-step experiment is carried out: 1) measuring total output noise (including noise of the filter and output buffer), 2) disabling the filter and measuring noise of only the output buffer. Then, since noise of the buffer and the filter are uncorrelated, the filter noise is calculated by subtracting the total noise PSD and the buffer noise PSD.

Figure 3-25(a) shows the measured input-referred noise (IRN) spectral density of the filter in the charge-sampling mode for the 9 MHz BW_{analog} setting (C_S = 0.75pF, C_H = 2.35pF). The

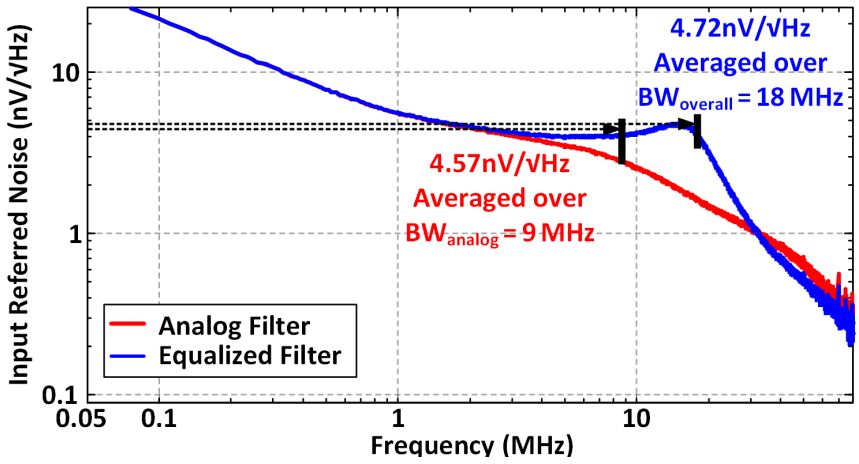
slope below 1 MHz is due to the flicker and bias noise of the gm-cell. Noise between 1 MHz and 20 MHz is mainly the thermal noise of the gm-cell shaped by the filter transfer function, and the rest is dominantly noise of the switched-capacitor circuit. The averaged spot noise over the bandwidth is 4.57 nV/√Hz. Integrated noise, P_N, from 50 kHz to 9 MHz is 13.6 μV_{rms}, which increases to 16.4 μV_{rms} for the entire frequency range. This gives a 71 dB spurious-free dynamic range (SFDR) as defined in [13]. As measured by a single-tone test, a -3.5 dBm input signal (422 mV peak-to-peak differential) creates -40 dB 3rd-harmonic distortion (HD3) at the output, giving an 81 dB dynamic range (1% HD3 DR). By applying the digital equalizer to map the analog transfer function to a 5th-order Butterworth, the equivalent IRN of the total filter increases to 4.72 nV/√Hz, resulting in 68 dB SFDR for 18 MHz $BW_{overall}$.

Measured input-referred noise of the filter in the voltage-sampling mode for the 3.1 MHz BW_{analog} (C_S = 0.75pF, C_H = 8.25pF) is illustrated in Figure 3-25(b). In this mode, the whole noise spectrum is due to the switched-capacitor network. The spot IRN averaged over the bandwidth is 4.97 nV/√Hz. The integrated IRN over the bandwidth is 8.6 μV_{rms} and rises to 22.2 μV_{rms} for the entire frequency range. This results in 75 dB SFDR. As measured, a single tone input signal as large as 8.8 dBm (1.75 V peak-to-peak differential) creates 1% HD3 in this mode. This results in 97 dB dynamic range. By mapping the 6th-order real-pole transfer function of this filter to a 4th-orther Butterworth using the equalizer, the overall IRN of the filter rises to 7.27 nV/√Hz giving 71 dB SFDR for 5.4 MHz $BW_{overall}$.

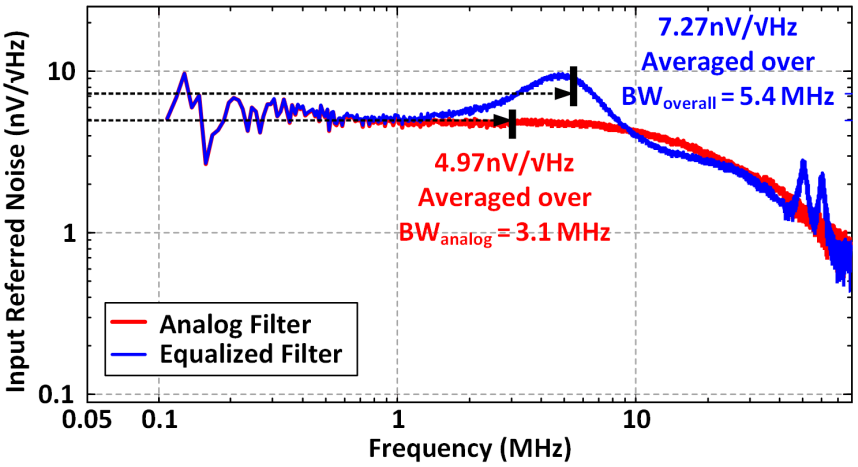
Base on hand calculation in (3.37), in-band spot noise is $4kT/(C_S f_s)$ for the switch capacitor circuit itself. In the voltage sampling mode, this value is about 5.2 nV/√Hz, for the used C_S=750 fF in the filter. As shown in Figure 3-25(b), measured in-band spot noise is about 5 nV/√Hz, in a good agreement with the hand calculated value. Using a gm-cell before the SC circuit with a gain of 9.3 dB, reduces input referred noise of the SC circuit in charge-sampling mode. However, the gm-cell itself adds some extra noise, increasing the total input-referred noise. Considering input-referred noise of gm-cell as $4kT\gamma/g_m$ we have:

$$IRN = \sqrt{\frac{4kT}{C_s f_s} \times \frac{1}{A_V^2} + \frac{4kT\gamma}{g_m}} = 3.6\text{nV}/\sqrt{\text{Hz}}\,, \tag{3.40}$$

where, A_V=9.3 dB, g_m=1.7 mS, and γ=1. This is expected value for an ideal gm-cell. However, RC bias used in the gm-cell further increases noise at low frequencies (see Figure 3-25(a)). As



(a)



(b)

Figure 3-25: Measured input-referred noise of the filter in (a) charge-sampling and (b) voltage-sampling mode.

measured, the average spot noise in the charge sampling mode is 4.57 nV/√Hz, aligned with the above hand calculation.

Measured clock feedthrough at the output of this filter is less than -110 dBm at f_{ref}/8=100 MHz. This very low value avoids any noise and spur problems caused by the clock signal.

3.7 Conclusion

In this chapter, a high-order discrete-time (DT) charge rotating (CR) IIR filter structure is proposed and experimentally verified. The implemented 7th-order charge-sampling/ 6th-order voltage-sampling DT filter is elaborated in detail. The order of this filter is easily extendable to even higher orders. Using a pipelining techniques, sample rate of the filter is increased up to 1GS/s. The CR filter is process-scalable according to Moore's law and friendly to digital

nanoscale CMOS technology. Transfer function of this filter is precise and robust to PVT variations. Even though the CR filter features real poles, modern system applications, such as wireless receivers, could expend digital post-processing to equalize the droop at the pass-band edge of the transfer function. Its state-of-the-art performance includes: very low power consumption, the lowest input-referred noise, very wide tuning range and excellent linearity. This filter will be later used at baseband of the receiver in Chapter 6.

Chapter 4

DT I/Q Charge-Sharing BPF

In this chapter, a very high sample rate DT bandpass filter (BPF) using I/Q charge sharing is proposed. This filter is required at IF of the superheterodyne receiver proposed in Chapter 6. This filter is mainly responsible to reject out-of-band blockers/interferes at IF strip of the receiver. After explaining operation of this filter and its analysis, the proposed BPF is compared with other IF filter structures. Then, a simple DT model of gm-cell used as a DT gain block is described. The gm-cells are required to cascade different stage of BPFs. At the end, extension of the DT BPF to a higher quality factor / higher order is explained.

4.1 Filter Structure

Figure 4-1 shows the discrete-time I/Q charge sharing bandpass filter (CS-BPF, first disclosed in [6]) used in the IF strip of the proposed receiver [14]. Input of this filter are DT *I* and *Q* charge packets ($q_{in,I}$[n] and $q_{in,Q}$[n]), and its output are *I* and *Q* voltage samples ($V_{o,I}$[n] and $V_{o,Q}$[n]). Since the physical wires are shared but their electrical properties are interpreted differently from the input and output standpoints, this is considered a 1-port complex structure. This filter is based on the idea of polyphase filter where input signals with different phases (e.g., quadrature *I/Q*) are combined with different phase shifts [47]. In this way, a real-input/output transfer function that is symmetric around dc could be shifted to positive or negative frequencies. Refs. [48] and [49] are examples of CT complex bandpass and notch filters, respectively. In a DT implementation, charge sharing between *I* and *Q* can shift the transfer function. In [24] an

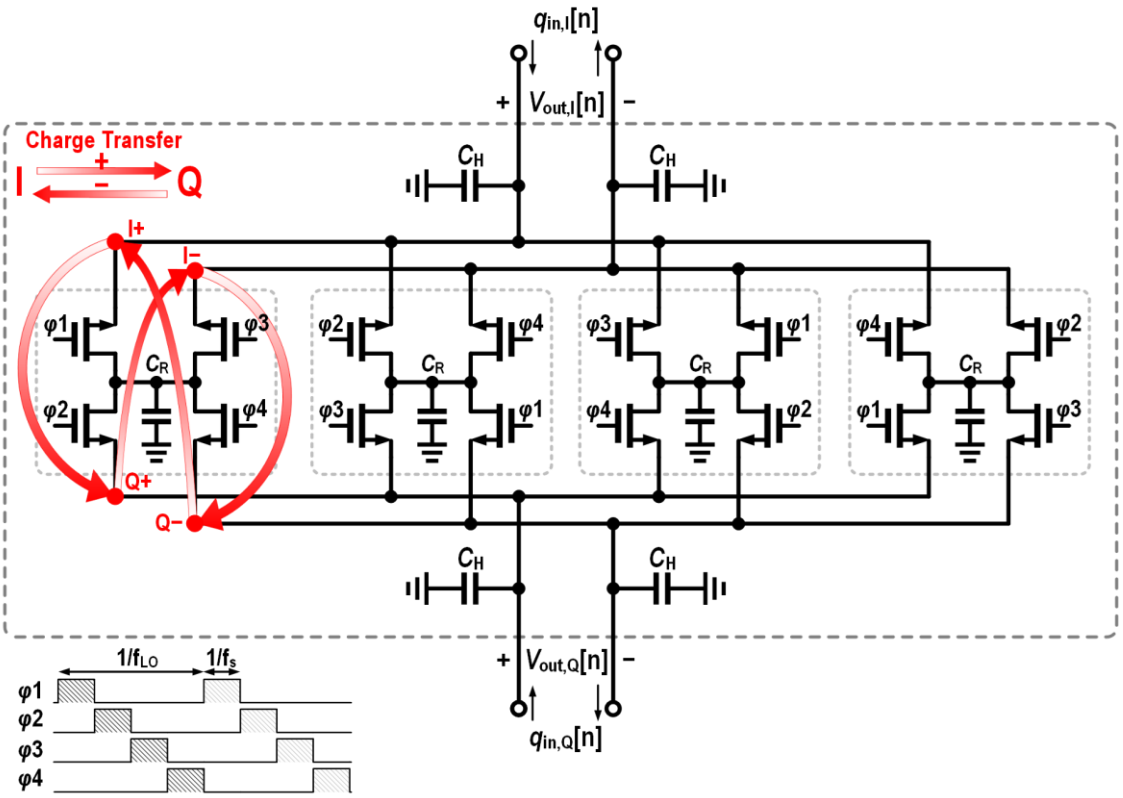


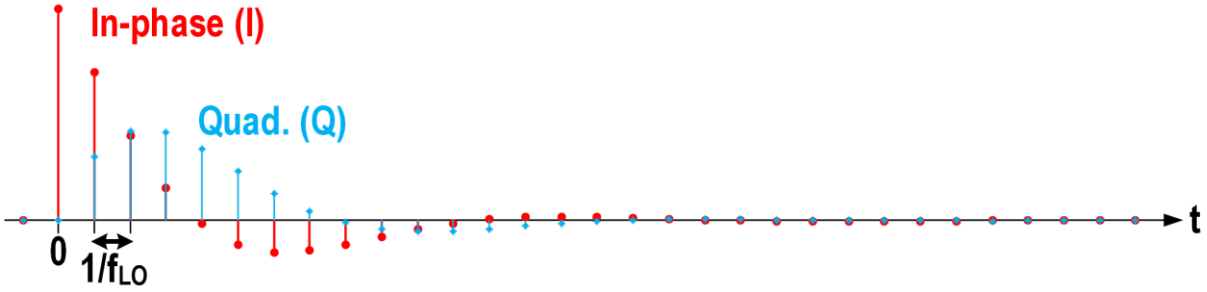
Figure 4-1: Discrete-time passive I/Q charge-sharing bandpass filter.

implementation of such a DT BPF was presented using opamps. While linearity in [24] is very poor as it is limited by opamps, *passive* implementation of our proposed filter provides a very high linearity (IIP3 > +30dBm). In addition, it allows the filter to operate at a very high sample rate, more than 12 GS/s in the present work, rather than the MHz-level range limited by opamp settling [24].

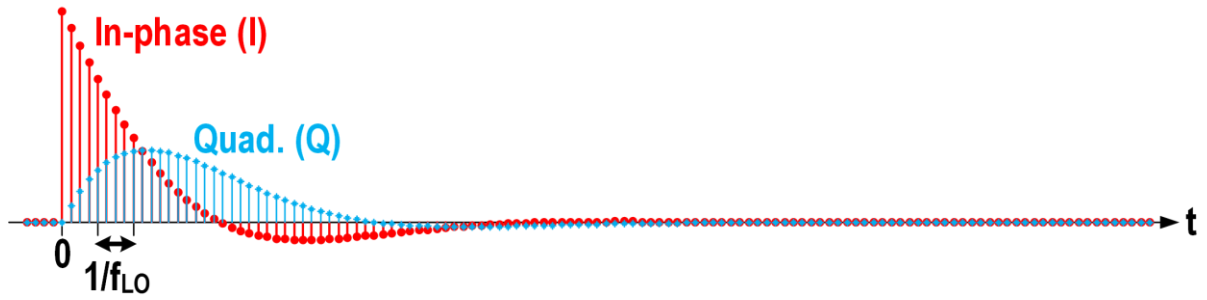
To visualize the operation of the proposed filter, consider first only one of the switched-capacitor banks in Figure 4-1. In each cycle ($\varphi1$ to $\varphi4$), C_R keeps on sequentially charge-sharing with a part of a C_H residing at $I+$, then $Q+$, then $I-$ and finally, $Q-$. Therefore, during the whole cycle, part of charge is transferred from I to Q path with positive sign, and from Q to I path with negative sign. As this charge sharing lasts 4 phases, it does not satisfy the requirement of the 4x sampling.

Sample rate of this single block is increased 4x through *parallelized operation*[4] , which could

[4] This is different than the traditional parallelism and pipelining techniques [50], [51] used in digital implementation.



(a)



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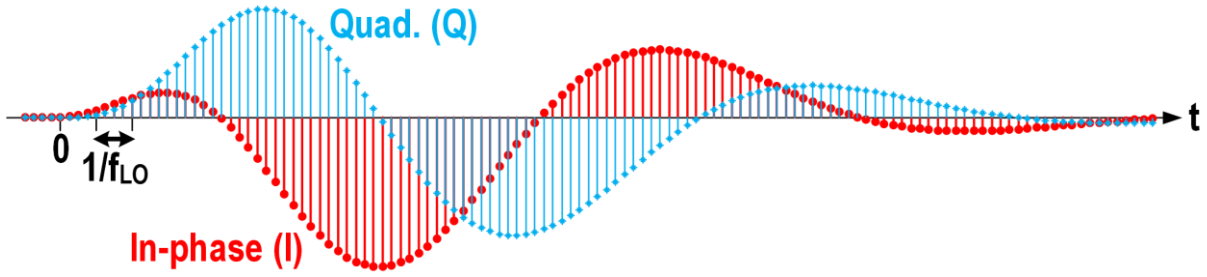


(c)

Figure 4-2: In-phase impulse response of DT I/Q charge-sharing BPF: (a) single-stage before, and (b) after 4x parallelized operation; (c) 4-stage with parallelized operation. Note that phase shift between I and Q is 90º.

be implemented in a straightforward manner, as shown in [5]. To do so, an array of four rotating capacitor banks, which replaces the single C_R bank, is used in parallel, each with one additional phase delay. This way, one charge sharing is performed from each of the input lines to any of the three remaining lines at each phase, instead of the entire cycle. Thus, sample rate is increased to $4f_{LO}$, satisfying the requirement of high-IF DT receiver. Figure 4-2 compares response of this filter to an in-phase impulse in two cases of with and without parallelized operation for 1-stage and 4-stage CS-BPF. The ringing in the response time sequence indicates a bandpass characteristic of the filter.

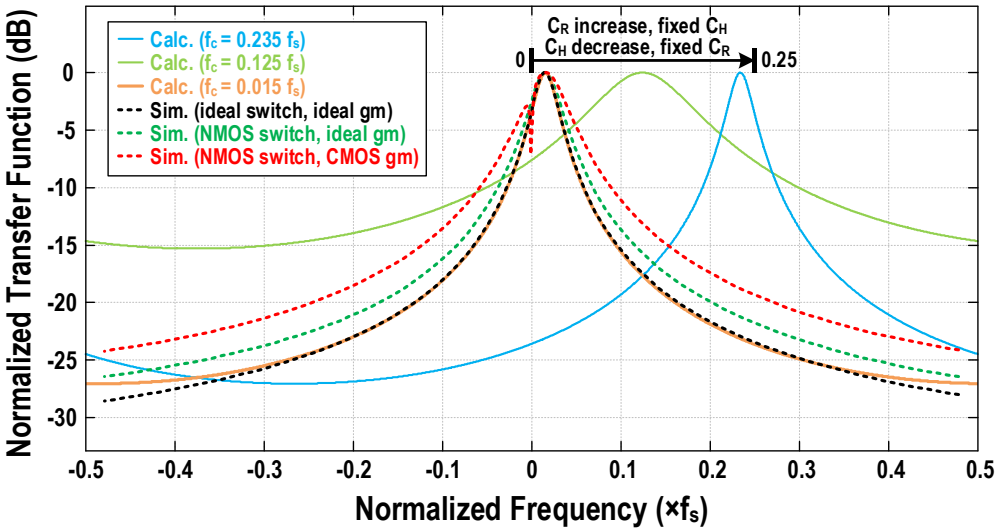


Figure 4-3: Normalized transfer function of the I/Q charge-sharing BPF.

4.2 Transfer Function

To derive the DT transfer function of this filter, first we assume that complex input and output signals are $q_{in}[n] = q_{in,I}[n] + j \cdot q_{in,Q}[n]$ and $V_{out}[n] = V_{out,I}[n] + j \cdot V_{out,Q}[n]$. Considering, for example, voltage of the *I* path at the end of each cycle, it consists of the remaining history from the previous cycle, $C_H / (C_H + C_R) \cdot V_{out,I}[n\text{-}1]$, the charge coming from *Q* path converted to voltage, $-C_R / (C_H + C_R) \cdot V_{out,Q}[n\text{-}1]$, and the contribution from the newly coming input charge. Then, we arrive at the following charge-sharing equations:

$$V_{out,I}[n] = \alpha \cdot V_{out,I}[n-1] - (1-\alpha) \cdot V_{out,Q}[n-1] + \frac{1}{C_H + C_R} q_{in,I}[n], \tag{4.1}$$

$$V_{out,Q}[n] = \alpha \cdot V_{out,Q}[n-1] + (1-\alpha) \cdot V_{out,I}[n-1] + \frac{1}{C_H + C_R} q_{in,Q}[n]. \tag{4.2}$$

In the above equations, α is defined as $C_H / (C_H + C_R)$. By solving (4.1) and (4.2) in z-domain, transfer function of the filter is derived as [52][5]:

$$H_{BPF}(z) = \frac{V_{out}}{q_{in}} = \frac{1/(C_H + C_R)}{1 - [\alpha + j(1-\alpha)] z^{-1}}. \tag{4.3}$$

Figure 4-3 plots the normalized transfer functions and compares them with circuit simulations. As C_H increases, center frequency (f_c) of the transfer function moves towards zero

[5] Ref. [52] performs full noise analysis of this filter and derives its transfer function.

where the BPF gets closer to a low-pass filter (LPF), similar to that in [9]. By increasing C_R, charge sharing between *I/Q* increases as well and shifts the f_c away from zero towards $f_s/4$. In addition, it reduces the passband gain. In the case where C_H is zero, the BPF turns to a complex N-path filter (N=4) with center frequency at $f_s/4$ (i.e., same as f_{LO}), similar to the one in [53]. The center frequency could be flipped to negative by reversing the sequence of clock signals ($\varphi_{4\text{-}1}$). Also calculated in [24], the f_c derived from (4.3) is:

$$f_c = \frac{f_s}{2\pi} \arctan\left(\frac{C_R}{C_H}\right). \tag{4.4}$$

This shows that transfer function of this filter is set only by the sampling frequency and C_R/C_H capacitor ratio. Therefore, it has little sensitivity to process, voltage and temperature (PVT) variations. Passband gain of this filter is calculated by replacing $z=e^{j\cdot 2\pi f\cdot Ts}$ in (4.3) at the center frequency (4.4):

$$A_{BPF} = \frac{1}{C_R + C_H\left(1-\sqrt{1+\left(C_R/C_H\right)^2}\right)} \approx \frac{1}{C_R} \quad for\ C_R << C_H\,. \tag{4.5}$$

As in practical applications, f_s is in GS/s range while IF (and so f_c) is around tens of MHz, the assumption that C_R is much smaller than C_H is reasonable. Unit of (4.5) is volt/coulomb.

4.3 Comparison with Other Types of BPF

Three categories of filters potentially suitable for high-IF receivers are Gm-C, N-path, and DT bandpass filters. As shown in Figure 4-4(a), Gm-C filter could provide a very good bandpass transfer function with a high quality factor [54], [55]. However, a very high power will be consumed in this filter to bring its noise to an acceptable level. On the other hand, as gain of the LNTA is also considered, a Gm-C filter can hardly provide enough linearity required in a high performance receiver.

An N-path filter basically upconverts a lowpass transfer function through an N-phase mixing operation [56]–[59]. As it could be also modeled as a DT filter, a higher *N* increases the equivalent sample rate, and therefore moves the first folding image to higher frequencies [57], [58] (this is very similar to the folding images of a sampling system). However, the transfer function of N-path filter (Figure 4-4(b)) has extra replica peaks due to the harmonics of mixing operation. Though these peaks are non-folding, a blocker signal at one of these frequencies will

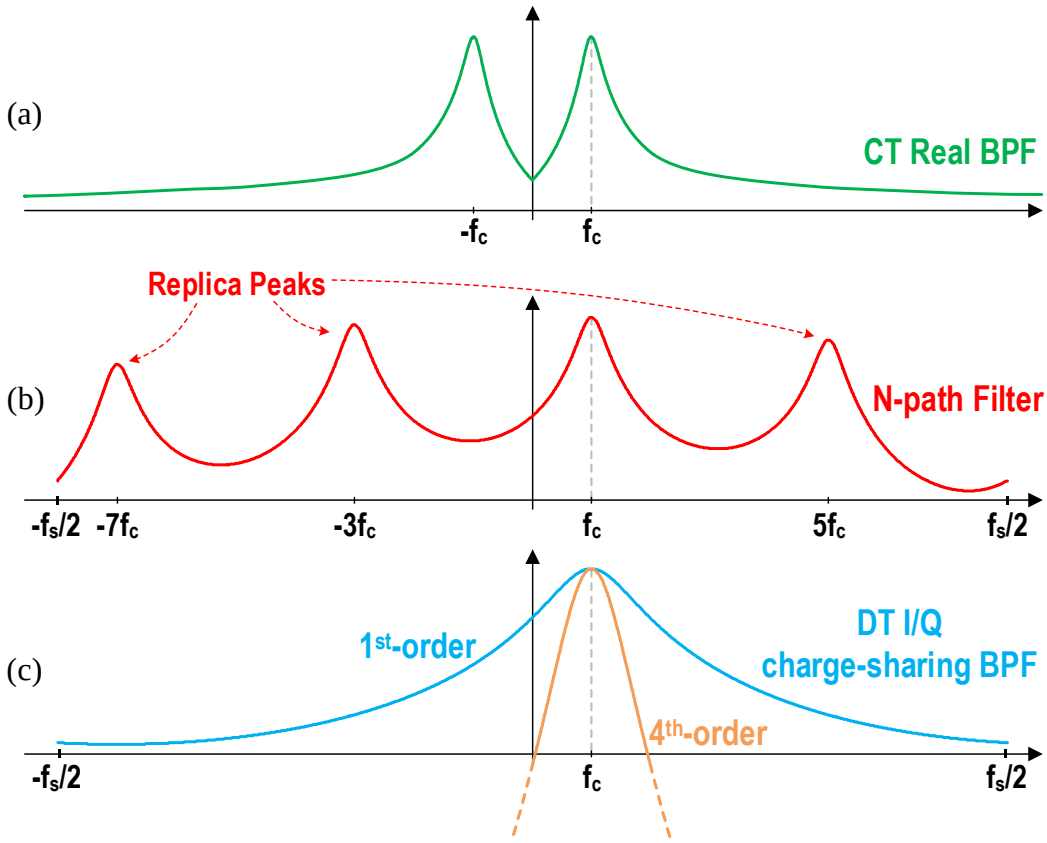


Figure 4-4: Comparison of transfer functions of various BPFs: continuous-time, N-path (N=16), and the proposed I/Q charge-sharing. While N-path filter has unwanted replica peaks, the DT charge-sharing BPF does not have any across its Nyquist range.

not get attenuated and is able to block the wanted signal by saturating the filter nodes. In addition, second-order nonlinearity of the mixers create an intermodulation (i.e., IM2) product near dc at low-pass side, which is upconverted to the passband by the mixers again [60]. This mechanism is responsible for the limited IIP2 of N-path filters.

In [7], a complex N-path filter is used at an IF stage of a superheterodyne receiver. In addition, an N-path filter is also translated to RF via a mixer and it placed in front of LNA. Though this filtering provides a narrow wanted passband directly at RF, it still has the problem of replicas (at multiples of $\pm 4f_{IF}$) and also folding images. As this image is created at the upstream with a limited rejection of only about 36 dB, it cannot be filtered afterwards in the rest of receiver chain.

An active (i.e., opamp based) switched-capacitor filter is able to provide a high-Q bandpass transfer function with a high linearity. However, it is power hungry and, more importantly, it has a low sample rate (normally less than 100 MS/s) as a result of slow opamps settling. In contrast,

the proposed DT bandpass filter is able to work in the GS/s range with very high linearity and low power consumption, thanks to its fully passive structure. As shown in Figure 4-4(c), it does not have the problem of replicas of N-path filters. The IM2 product that could be created in this filter is located near dc and it normally cannot find its way to the passband (e.g., there are no IF clocks present until this stage in the system to be able to translate the IM2 to around f_{IF}). Consequently, this type of filter has no theoretical limitation on IIP2 for modulated or closely spaced two-tone blockers.

The only bottleneck of this filter is its relatively low quality factor, expressed as f_c/BW, of about 0.5 for low IF frequencies. Similarly to [59], adding a negative resistance to the filter nodes can increase its quality factor, although by severely trading off its IIP3. Alternatively, out-of-band filtering at IF can be improved by lowering the IF frequency to reduce the bandwidth, and also by cascading more stages to increase the filter's order.

As will be shown later in Chapter 6, four CS-BPFs are cascaded to effectively filter out unwanted interferers and blockers. Each filter stage improves input-referred IIP3 of the following stages.

4.4 DT Gain Stage

Gm-cells are exploited to facilitate cascading single-stage bandpass filters at IF. They act to isolate the filter stages to avoid loading, as well as to subsequently re-convert voltage to current. Figure 4-5(a) shows one of the gm-cells together with its loading environment. Considering that the filters are operating in the DT domain but the gm-cell is natively a CT element, we can use the model in Figure 4-5(b) to describe its operation [61]. By neglecting a small transient voltage settling at the beginning of each phase, CT voltage $v(t)$ at the output capacitor of the preceding DT stage is approximated as zero-order hold (ZOH). This is captured by the first two blocks in the model of Figure 4-5(b).

$$v(t) = v[n] \quad \text{for} \quad (n-1)T_s < t \le nT_s . \tag{4.6}$$

This voltage is converted to current by the gm-cell (third block in the model) that is then integrated over the sampling period (T_S) of the subsequent filter. After sampling of the output result (fourth block in the model) and using (4.6), we have:

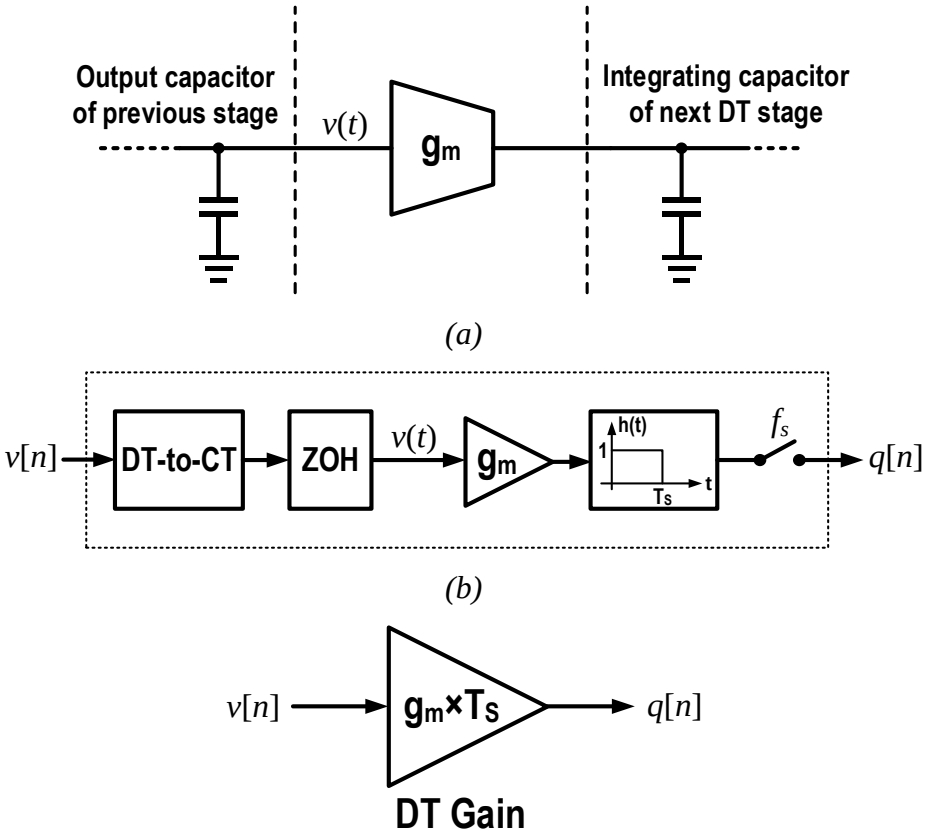


Figure 4-5: (a) The gm-cell gain stage, with (b) the model describing its operation, and (c) its simple DT representation.

$$q[n] = \int_{(n-1)T_s}^{nT_s} g_m v(t) \cdot dt = g_m T_s \times v[n]. \tag{4.7}$$

It shows that the whole process can be modeled as a DT gain stage (Figure 4-5(c)) with the gain of $A_{gm,IF} = g_m T_S$.

Using (4.5) and (4.7), voltage gain from the input of gm-cell to the output of its subsequent filter is

$$G_{BPF} = A_{gm,IF} \times A_{BPF} = g_m T_S \times \frac{1}{C_R} = g_m \frac{1}{C_R f_s}. \tag{4.8}$$

The last fraction, $1/C_R f_s$, is usually called a DT-equivalent resistance in the switched capacitor analysis [5].

Implementation of the IF gm-cell as a simple inverter-based gm [5], [62] (Figure 4-6) makes it process scalable. By properly sizing of NMOS and PMOS transistors, their nonlinearities could be canceled out perfectly for square-law transistors [44], [63]. However, in nanoscale CMOS only a partial cancellation can be achieved. To help, we resort to devices with a large channel

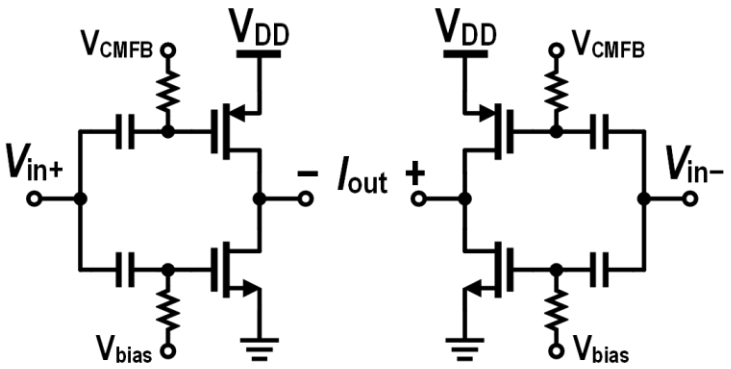


Figure 4-6: Implementation of IF gm-cell.

length to make their behavior closer to the square-law model. Moreover, a low DT resistance load by the succeeding filter promotes high IIP3 of this cell.

4.5 Extension to Higher Quality/Order CS-BPF

The proposed I/Q charge-sharing BPF filter can be extended to multiphase inputs [64], [65]. For example in Figure 4-7(a), number of phases from 4 in *I*/*Q* only, each with 90º phase shift difference, is extended to 8 phases, each with 45º phase shift difference. In this way, transfer function of the BPF is improved, and consequently, close-in *Q* is increased from 0.5 to 1.21. Figure 4-8 compares transfer function of 4-phase input (4/4) and 8-phase input (8/8) BPFs. The multiphase input idea can be extended to higher number of phases (e.g. 16).

The second extension of CS-BPF can be done in another dimension. As shown in Figure 4-7(b), between each input charge-sharing, a 1st-order pole (LPF) can be inserted [64], [65]. This pole has two effects: 1) it increases close-in quality factor of the filter (i.e., a narrower bandwidth of a given f_c). 2) Output of the filter at the LPF side (V_{o2}, at the right side of Figure 4-7(b)) has one 1st-order LPF cascaded with the BPF. Therefore, by reading the output from this node set instead of the same previous node set (V_{o1}), out-of-band filtering of the BPF is also increased. Since the filter in Figure 4-7(b) has 8-phase input and 16-phase charge rotation, we call it 8/16-phase CS-BPF. In general, more 1st-order poles can be inserted between each input charge-sharing and this idea can be extended to an M/N-phase CS-BPF. Number of charge rotation phases can be found by $N=M\times(1+n)$, where n is number of the inserted 1st-order poles.

The same *parallelized operation* that explained earlier in subsection 4.1is application here to increase sample rate. In Figure 4-8, CS-BPFs with different 1st-order poles is also compared.

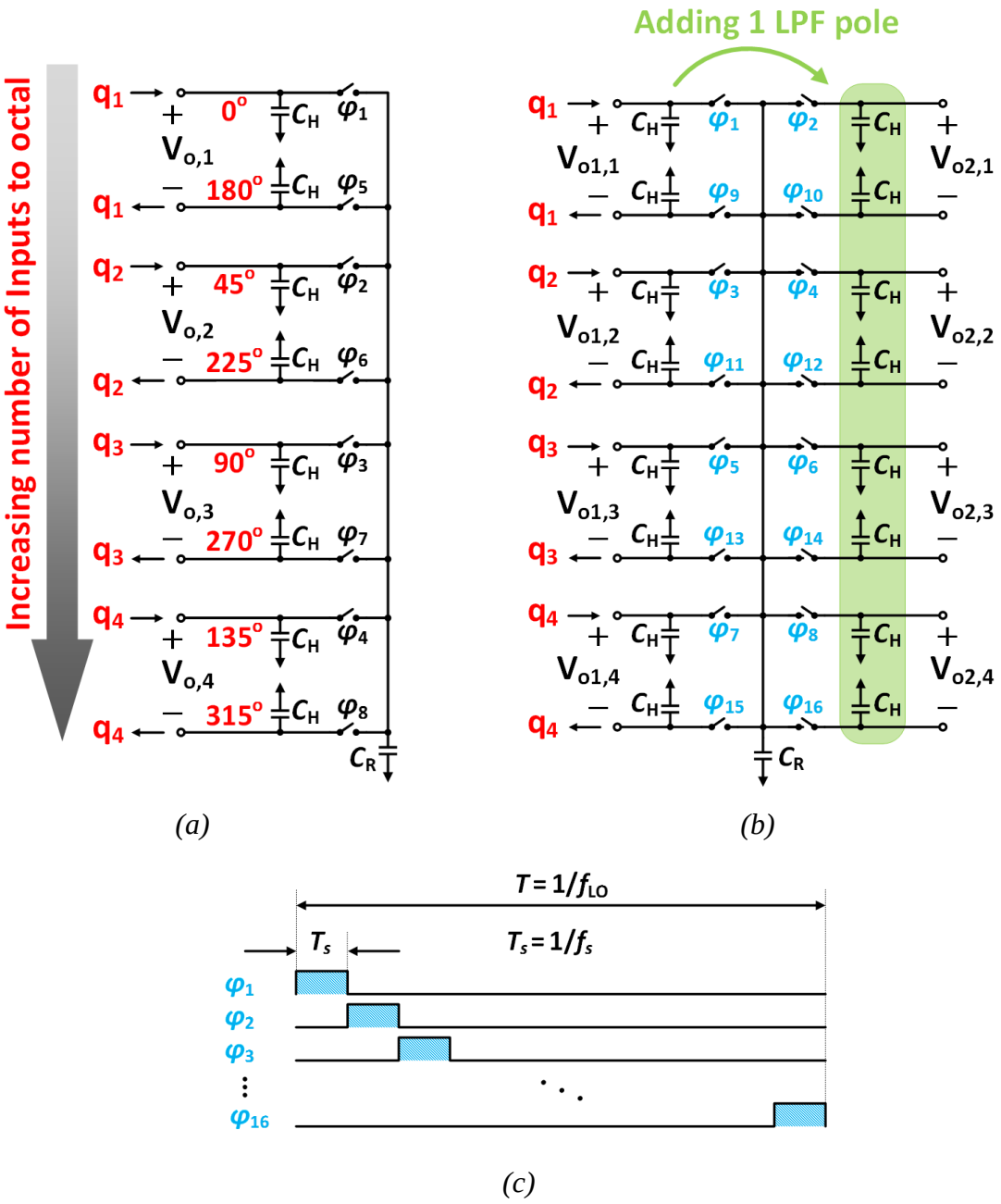


Figure 4-7: (a) Multiphase charge-sharing BPF with 8-phase input (8/8 CS-BPF). (b) Adding one LPF pole between each charge-sharing: 8-phase input/ 16-phase rotation (8/16 CS-BPF). (c) Clock waveforms required to drive 8/16 CS-BPF.

Comparing 8/8-phase with 8/16-phase, close-in Q is increased from 1.21 to 2.5. Also, far-out filtering order is increased one order, from 1st-order to 2nd-order. Comparing 4/4-phase, 4/8-phase, and 4/16-phase, close-in Q is increased from 0.5 to 1.14, and to 2.49, respectively. Also, far-out filtering order is increased from 1st-order to 2nd-order, and to 4th-order, respectively.

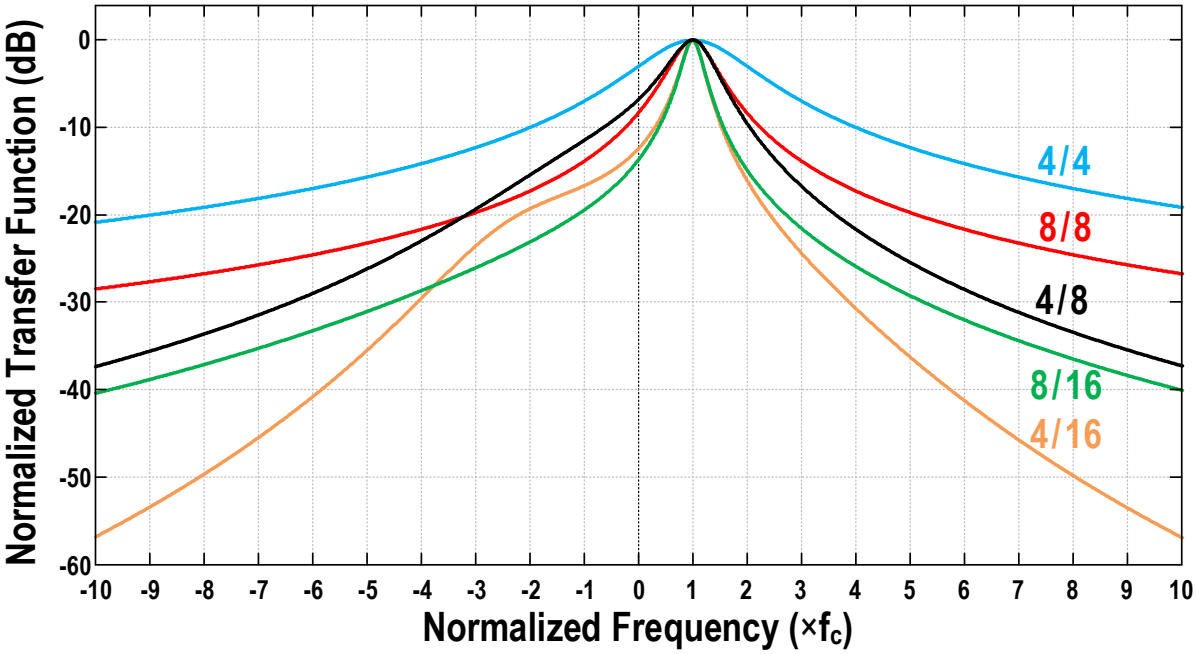


Figure 4-8: Transfer function comparison of different M/N-phase charge-sharing BPFs.

4.6 Conclusion

In this chapter, a discrete-time (DT) charge-sharing (CS) band-pass filter (BPF) suitable for superheterodyne receivers was proposed and analyzed. The filter is entirely passive and uses transistors only as switches. The center frequency is digitally controllable via clock frequency and capacitor ratios and thus insensitive to PVT variations. Its transfer function is free from aliasing and replicas while operating at a GS/s rate. The CS-BPF will be later used at IF strip of the proposed receiver in Chapter 6.

Chapter 5

Wideband Noise Cancelling LNTA

To be able to amplify an RF signal located at any of the supported frequency bands in a receiver, wideband noise cancelling LNA [66] appears to be a good choice. As the proposed receiver in Chapter 6 is based on sampling the input charge, the RF amplifier needs to provide current rather than voltage, thus acting as a transconductance amplifier (TA) exhibiting a high output impedance, as compared to the input load of its subsequent stage. An LNTA (i.e., LNA+TA) could trivially be constructed by cascading the LNA and TA (gm) stages [8]–[11]. However, to improve noise and linearity, both of these circuits should be co-designed and tightly coupled [12], [46].

5.1 Basic Wideband LNA Structures

5.1.1 Cross-Coupled Common-Gate LNA

As the first basic LNA structure, cross-coupled common-gate LNA [67] is shown in Figure 5-1. To have input source impedance (R_S) matching in this structure, input transistors ($M_{a,n}$ and $M_{a,b}$, here after M_a) should have transconductance of:

$$g_{m,a} = \frac{1}{2R_S}. \tag{5.1}$$

This is half the required g_m for a common-gate LNA without the cross-coupling, which saves power consumption.

To analyze noise of this structure, initially noise of $M_{a,p}$ (indicated in red in Figure 5-1) is

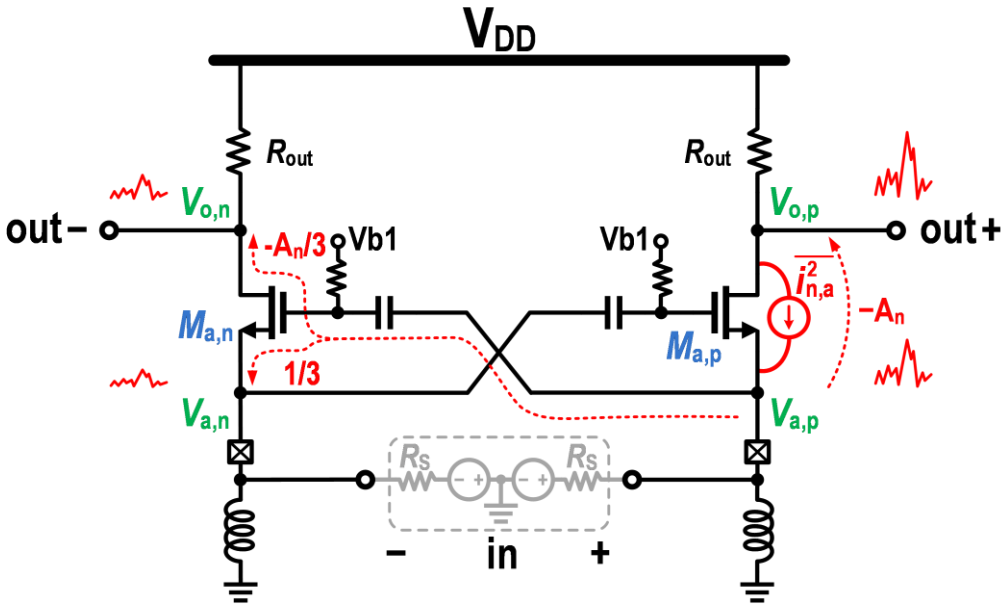


Figure 5-1: Cross-Coupled Common-Gate LNA [67] *with reduced required input matching transconductance and partial noise input noise-cancellation at differential output.*

only considered in the right branch. First by writing KCL at $V_{a,n}$, we have:

$$\frac{V_{a,n}}{R_S} = \left(V_{a,p} - V_{a,n}\right) g_{m,a} . \tag{5.2}$$

Substituting (5.1) in (5.2) gives:

$$V_{a,n} = \frac{1}{3} V_{a,p} . \tag{5.3}$$

Then, by writing KCL at $V_{a,p}$, we have:

$$\frac{V_{a,p}}{R_S} = \left(V_{a,n} - V_{a,p}\right) g_{m,a} + i_{n,a} , \tag{5.4}$$

where $\overline{i_{n,a}^2}$ is a spectral density of $M_{a,p}$ noise current .Replacing (5.3) in (5.4) and considering the input matching condition, it is simplified to:

$$V_{a,p} = \frac{3}{4} i_{n,a} \times R_S . \tag{5.5}$$

It could be easily shown that the $M_{a,p}$ noise appears the $V_{o,p}$ with $-A_n$ times $V_{a,p}$, where A_n is given by:

$$A_n = \frac{R_{out}}{R_S} . \tag{5.6}$$

Therefore, using (5.3), (5.5) and (5.6), the effect of $\overline{i_{n,a}^2}$ on $V_{a,p}$ and $V_{a,n}$ is found:

$$\begin{cases} V_{o,p} = -\frac{3}{4} i_{n,a} R_{out} \\ V_{o,n} = -\frac{1}{4} i_{n,a} R_{out} \end{cases} \Rightarrow V_{o,diff} = -\frac{1}{2} i_{n,a} R_{out} . \quad (5.7)$$

In addition to $M_{a,p}$ noise, R_{out} noise ($\overline{v_{n,Rout}^2}$) also goes to the output. Note that noise of the left branch is also the same amount. Moreover, all noise source are uncorrelated.

While the input is matched, signal gain from input to output is calculated:

$$A_V = \frac{V_{out,d}}{V_{in,d}} = \frac{V_{o,d}}{V_{a,d}} = g_{m,a} \times 2R_{out} = \frac{R_{out}}{R_S} . \quad (5.8)$$

Now, noise figure (NF) of the LNA can be found by referring the effect of different noise sources from the output $V_{o,diff}$ to the input $V_{a,diff}$, and normalizing to the noise of input source (R_S):

$$\begin{aligned} NF &= 1 + \frac{\frac{2 \times \left((1/2) i_{n,a} R_{out}\right)^2}{A_V^2} + \frac{2 \times v_{n,Rout}^2}{A_V^2}}{2 \times (1/2)^2 \times v_{n,R_S}^2} \\ &= 1 + \frac{\frac{2 \times (1/2)^2 \times 4kT\gamma_a g_{m,a} \times \left(R_{out}\right)^2}{\left(R_{out}/R_S\right)^2} + \frac{2 \times 4kTR_{out}}{\left(R_{out}/R_S\right)^2}}{2 \times (1/2)^2 \times 4kTR_S} . \end{aligned} \quad (5.9)$$

The 2x multiply in the numerators and the denominator is to account for noise of both branches differentially. Also, the 1/2 coefficient in the denominator is because of the gain of 1/2 from input source to LNA input made by input matching. $M_{a,p}$ noise, $\overline{i_{n,a}^2}$, is considered $4kT\gamma g_m$, where k, T, and γ are Boltzmann constant, absolute temperature, and MOS noise excess factor, respectively. After simplification and considering input matching condition, (5.9) can be written as:

$$NF = 1 + \frac{\gamma_a}{2} + \frac{4}{\left(R_{out}/R_S\right)} . \quad (5.10)$$

The second term is noise contribution of M_a transistors that is reduced to half due to the cross-coupling and less required $g_{m,a}$ for input matching. Supposing $\gamma_a \approx 1$ in nano-scale CMOS and 20 dB voltage gain, NF of this LNA is limited to > 2.8 dB.

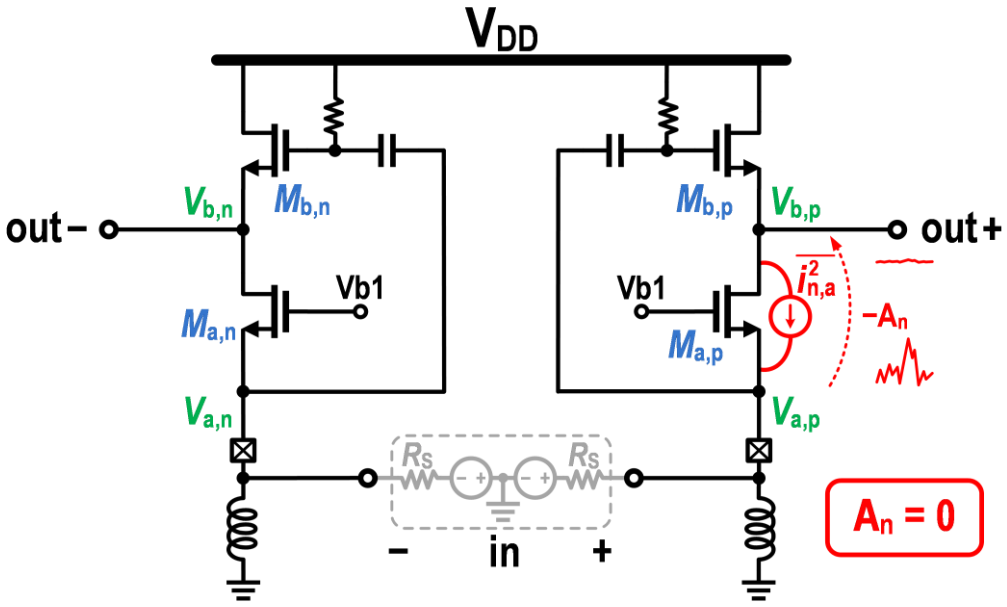


Figure 5-2: Common-gate-source-follower noise cancelling LNA [68] *with noise cancellation of the input matching transistors.*

5.1.2 Basic Common-Gate Noise Cancelling Structure

The common-gate-source-follower noise cancelling LNA structure [68] shown in Figure 5-2 is able to cancel noise of the input matching transistors. In this LNA, R_{out} is replaced with two transistors, M_b, that transfer signal and noise of the input nodes (V_a) to the outputs (V_b). Input signal goes to the output from two paths, through M_a and M_b that are added in-phase on V_b node. However, M_a noise reaches to the output from the two paths anti-phase, and therefore can be reduced or canceled out.

Input matching in this LNA is achieved by:

$$g_{m,a} = \frac{1}{R_S}. \tag{5.11}$$

First, noise of $M_{a,p}$ is only considered in the right branch. By writing KCL at $V_{a,p}$, we have:

$$\frac{V_{a,p}}{R_S} = -V_{a,p} g_{m,a} + i_{n,a}. \tag{5.12}$$

Substituting (5.11) in (5.12) gives:

$$V_{a,p} = \frac{1}{2} i_{n,a} \times R_S. \tag{5.13}$$

Then, KCL at $V_{b,p}$ node gives:

$$i_{n,a} - g_{m,a}V_{a,p} = \left(V_{a,p} - V_{b,p}\right)g_{m,b}. \tag{5.14}$$

By replacing (5.11) and (5.13), it is simplified to:

$$V_{b,p} = \frac{1}{2} i_{n,a}\left(R_S - \frac{1}{g_{m,b}}\right). \tag{5.15}$$

Here $M_{a,p}$ noise transfer ration ($-A_n$) from $V_{a,p}$ to $V_{b,p}$ is found from (5.13) and (5.15):

$$A_n = -\frac{V_{b,p}}{V_{a,p}} = \frac{1}{g_{m,b}R_S} - 1. \tag{5.16}$$

To have perfect noise cancelation of $M_{a,p}$, A_n should become zero. Hence we have:

$$A_n = 0 \;\Rightarrow\; g_{m,b} = \frac{1}{R_S}. \tag{5.17}$$

With this condition, the amount of $M_{a,p}$ noise current that directly goes to the output ($V_{b,p}$) is the same amount transferred from $M_{b,p}$, but with opposite direction. In this way, only $M_{b,p}$ noise is left in the right branch that it output noise voltage is trivially:

$$\overline{v_{n,b}^2} = \overline{i_{n,b}^2} \Big/ g_{m,b}^2 . \tag{5.18}$$

Considering the input matching (5.11) condition, signal voltage gain from the two path is derived:

$$A_V = \frac{V_{out}}{V_{in}} = \frac{g_{m,a}}{g_{m,b}} + 1 = \frac{1}{g_{m,b}R_S} + 1, \tag{5.19}$$

where, the first and second terms are through M_a and M_b paths, respectively. Noise that signal gain (A_V) in (5.19) is different than M_a noise ratio (A_n) in (5.16). Also accounting for M_a noise cancellation (5.17) condition, (5.19) is reduced to:

$$A_n = 0 \;\Rightarrow\; A_V = 2. \tag{5.20}$$

Therefore, the noise cancellation condition forces a fixed voltage gain in this LNA.

Noise figure of this LNA is found by considering the only left noise source in (5.18):

$$\begin{aligned} NF &= 1 + \frac{\dfrac{i_{n,b}^2 \Big/ g_{m,b}^2}{A_V^2}}{(1/2)^2 \times v_{n,R_S}^2} = 1 + \frac{\dfrac{4kT\gamma_b / g_{m,b}}{(2)^2}}{(1/2)^2 \times 4kTR_S} \\ &= 1 + \gamma_b . \end{aligned} \tag{5.21}$$

Although noise of the input matching is eliminated compared to (5.10), Mb noise still imposes

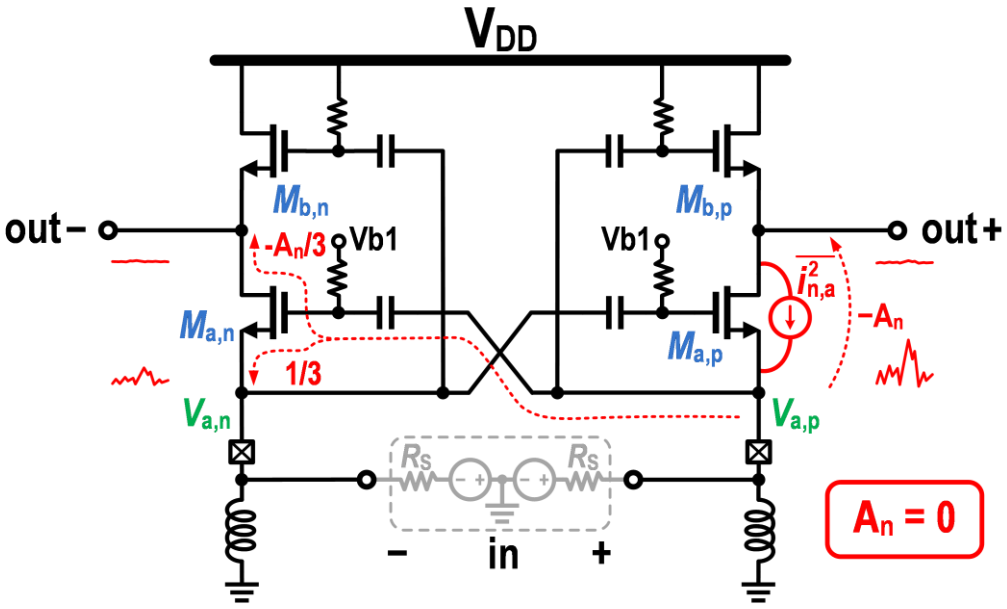


Figure 5-3: Common-gate-source-follower noise cancelling LNA with input cross-coupling.

a high NF. Supposing $\gamma_b \approx 1$, NF of this LNA is limited to > 3 dB while providing only 6 dB voltage gain.

5.2 Noise Cancelling Structure with Input Cross-Coupling

The first step to reach to the proposed LNTA structure is combining the two cross-coupled common-gate LNA and the basic common-gate noise cancelling structures (Figure 5-3).

In this structure, input matching condition is the same as (5.1), $g_{m,a} = 1/(2R_S)$. Also similar to the cross-coupled common-gate LNA in Figure 5-1, $M_{a,p}$ noise appears on the input nodes:

$$\begin{cases} V_{a,p} = \dfrac{3}{4} i_{n,a} \times R_S \\ V_{a,n} = \dfrac{1}{3} V_{a,p} \end{cases}. \tag{5.22}$$

KCL at $V_{b,p}$ gives us:

$$i_{n,a} + g_{m,a}\left(V_{a,n} - V_{a,p}\right) = \left(V_{a,p} - V_{b,p}\right) g_{m,b}\,. \tag{5.23}$$

By substituting (5.22), $M_{a,p}$ noise on the output node is found:

$$V_{b,p} = \frac{3}{4} i_{n,a} \left(R_S - \frac{1}{g_{m,b}} \right). \tag{5.24}$$

Therefore, this structure has also the same noise ratio as in (5.16):

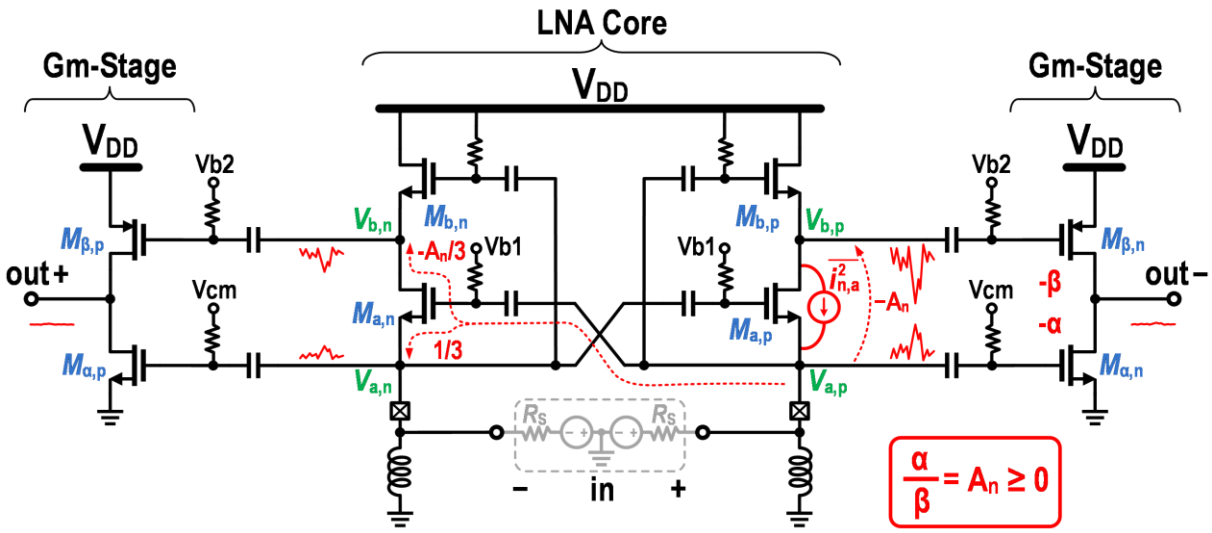


Figure 5-4: Noise-cancelling LNTA (proposed structure #1).Noise of the input matching transistors are cancelled out with an arbitrary gain of LNA core.

$$A_n = -\frac{V_{b,p}}{V_{a,p}} = \frac{1}{g_{m,b}R_S} - 1 . \tag{5.25}$$

Again here, $g_{m,b}$=1/R_S leads to complete M_a noise cancellation. Signal voltage gain is similarly derived the same as (5.19) that can be alternately written as:

$$A_V = A_n + 2 . \tag{5.26}$$

This LNA structure still has the noise figure of (5.21). However, it requires less power consumption to provide the input matching.

In addition to the problem of a high NF limitation, this structure still does not have freedom to set voltage gain (A_V).

5.3 Adding Gm-Cell

As the final design goal is to have an LNTA, an inverter-based gm-stage is added at the output of the LNA core of Figure 5-3. However, instead of connecting both NMOS and PMOS to V_b node, one is connected to V_b and the other one to V_a (see Figure 5-4, the proposed LNTA #1). In this way, M_a noise cancellation can be done for an arbitrary voltage gain (A_V) by exploiting an available degree-of-freedom in the gm-stage, where signals from $V_{a,p}$ and $V_{b,p}$ to *out*- has a voltage-to-current gain of $-g_{m,\alpha}$ and $-g_{m,\beta}$, respectively. Then, instead of setting $g_{m,b}$ =1/R_S to cancel M_a noise in the LNA core itself, a lower $g_{m,b}$ can be used. Consequently, A_V is increased that lowers input-referred noise of M_b and the gm-stage.

To cancel M_a noise at the output of gm-stage we have:

$$g_{m,\alpha} \cdot V_{a,p} + g_{m,\beta} \cdot V_{b,p} = 0 \ . \tag{5.27}$$

Substituting (5.25) into (5.27) gives:

$$g_{m,\alpha} \cdot V_{a,p} + g_{m,\beta}\left(-A_n \cdot V_{a,p}\right) = 0 \ \Rightarrow \frac{g_{m,\alpha}}{g_{m,\beta}} = A_n \ . \tag{5.28}$$

With this condition satisfied, noise of $M_{a,p}$ does not appear at $out-$ node. As calculated in (5.22), this noise appears on each corresponding node at the left side of LNA core with a gain of 1/3 (Figure 5-4). Consequently, in the same way it is also canceled at $out+$.

Total gain of the LNTA from input to output is provided by two paths: through V_a and V_b nodes. Using (5.26) and (5.28), the total single-ended transconductance is derived:

$$g_{m,tot} = -\left(g_{m,\alpha} + A_V g_{m,\beta}\right) = -2g_{m,\beta}\left(1 + A_n\right). \tag{5.29}$$

Total noise figure of the LNTA is calculated by input-referring noise of M_b, M_α and M_β from the output to the input:

$$\begin{aligned} NF &= 1 + \frac{\dfrac{\left(\overline{i_{n,b}^2}/g_{m,b}^2\right)\times g_{m,\beta}^2}{g_{m,tot}^2} + \dfrac{\overline{i_{n,\alpha}^2} + \overline{i_{n,\beta}^2}}{g_{m,tot}^2}}{\left(1/2\right)^2 4kTR_S} \\ &= 1 + \frac{\dfrac{\left(4kT\gamma_b/g_{mb}\right)\times g_{m,\beta}^2}{g_{m,tot}^2} + \dfrac{4kT\left(\gamma_\alpha g_{m,\alpha} + \gamma_\beta g_{m,\beta}\right)}{g_{m,tot}^2}}{kTR_S}. \end{aligned} \tag{5.30}$$

After assuming $\gamma_\alpha = \gamma_\beta$ and replacing (5.29), the noise figure is simplified to:

$$NF = 1 + \frac{\gamma_b}{\left(1 + A_n\right)} + \frac{2\gamma_\alpha}{g_{m,tot}R_S} \ . \tag{5.31}$$

The second term is due to noise of M_b that is reduced $1+A_n$ times by signal gain from other paths. The third term is the total noise contribution of the gm-stage that is reduced 2 times by the total multipath gain provided in the LNA core (compared with NF of a standalone gm-stage).

5.4 Final Structure with a 2nd Noise-Cancellation

As was derived in (5.31), noise of gm-stage can be reduced by increasing the total g_m. Also, M_b noise can be lowered by increasing voltage gain of the LNA core. However, to reach a very low NF in range of 1–2 dB, excess increase of voltage gain degrades linearity of the gm-stage.

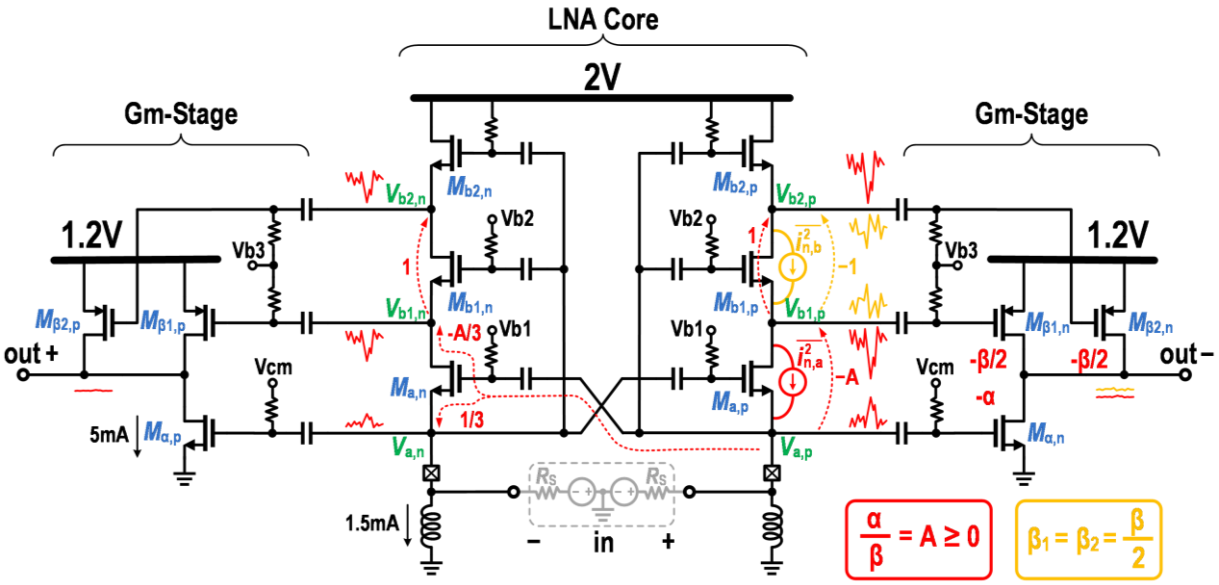


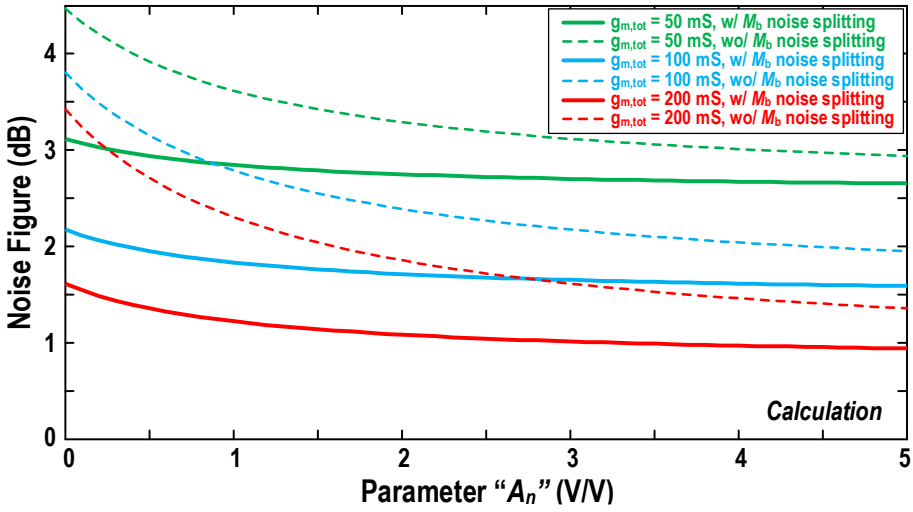
Figure 5-5: Wideband noise cancelling LNTA (proposed structure #2). Noise cancellation mechanisms of M_a and M_{b1} is show in red and yellow, respectively, that is cancelled at the output. Noise of $M_{b2,p}$ goes to the output with half gain, $\beta/2$.

To achieve this with a reasonable LNA core gain, M_b noise in Figure 5-4 is also reduced substantially, in addition to complete cancellation of M_a noise.

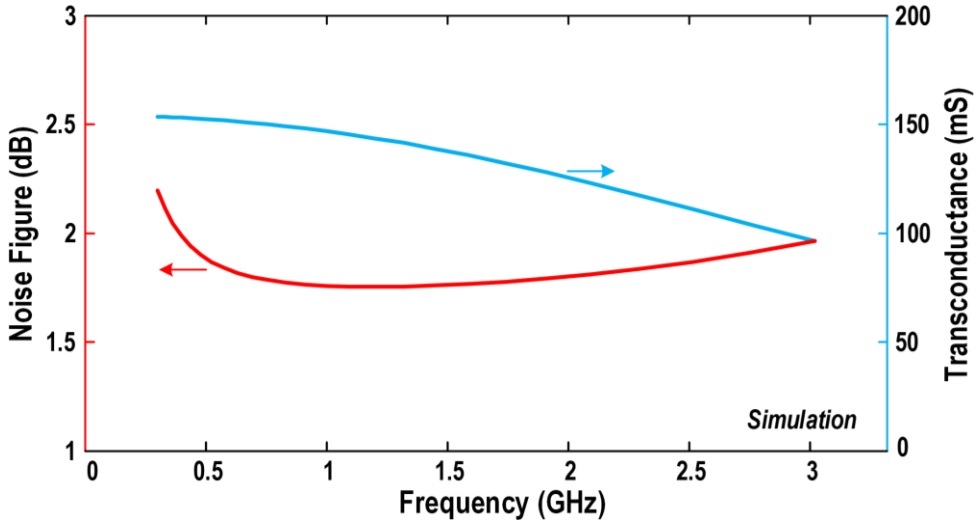
Instead of using only one M_b on each side of the LNA core, two identical transistors M_{b1} and M_{b2} are stacked (see Figure 5-5, the proposed LNTA #2 [14]). Although the amplified input signal appears in-phase with the same gain, noise of $M_{b1,p}$, ($\overline{i_{n,b}^2}$ shown yellow in Figure 5-5), appears anti-phase on $V_{b1,p}$ and $V_{b1,n}$. Then, splitting $M_{\beta,n}$ into two half transistors ($M_{\beta 1,n}$ and $M_{\beta 2,n}$) cancels noise of $M_{b1,p}$ at the output via the proposed *noise splitting technique*. This way, only noise of $M_{b2,p}$ contributes to the output, but with a reduced gain of $g_{m,\beta}/2$ instead of previously $g_{m,\beta}$ in (5.30). The noise splitting technique can be further utilized to cancel noise of M_{b2} at the cost of a higher LNA core supply voltage.

Now, total gain of LNTA from input to output is provided by three paths: through V_a, V_{b1}, and V_{b2} nodes. However, the same equation in (5.29) is still valid here (signal voltage gain from V_{b1} to V_{b2} is 1).

Total new noise figure of the LNTA is derived by referring noise contribution of M_{b2}, M_α and M_β from the output to the input (the same way as (5.30) is derived) and is simplified to:



(a)



(b)

Figure 5-6: (a) Calculated LNTA noise figure versus "A_n" parameter (in Figure 5-5), and (b) simulated noise figure and total g_m versus frequency, with S_{11}<-10 across the range. Note that LNA core gain is $A_V=A_n+2$.

$$NF = 1 + \frac{\gamma_b}{4(1+A_n)} + \frac{2\gamma_\alpha}{g_{m,tot}R_S}. \tag{5.32}$$

The second term is due to noise of M_{b2} that is substantially reduced 4 times by the proposed noise splitting technique, and $1+A_n$ times by signal gain from other paths.

Figure 5-6(a) plots noise figure of the LNTA with and without the noise splitting technique. A noise figure of even sub-1dB could be achieved by increasing $g_{m,tot}$ and A_n values. Simulated noise figure and gm of our implementation with a target of 120 mS is shown in Figure 5-6(b). The parameter A_n is chosen to be about 1 (LNA core gain about 10 dB) in this design to have a

balance between NF and IIP3. The covered LNTA frequency range is wideband: measured from 300 MHz up to 3 GHz. The cores of LNA and Gm-stages drain totally 3 mA and 10 mA from 2-V and 1.2-V power supplies, respectively.

5.5 Conclusion

A novel wideband noise-cancelling low-noise transconductance amplifier (LNTA) is proposed. It features two-fold noise cancellation core transistor pairs: in addition to noise of the input matching transistor pair, noise of another transistor pair in the LNA core is also cancelled. As showed through calculations, this LNTA could even achieve sub-1dB noise figure by increasing gain of LNA core and the total transconductance. This LNTA constructs the first stage of the proposed DT receiver in Chapter 6.

Chapter 6

Proposed DT Superheterodyne Receiver in 65nm CMOS

This chapter presents the fully integrated DT superheterodyne receiver [14]. The receiver uses the concepts and blocks proposed throughout Chapter 2 to Chapter 5. After discussing the proposed structure and it DT model, internal frequency translations as well as image rejection mechanisms are explained. Then, baseband signal processing using an ultra-low power implementation is discussed. Afterwards, measurement results of the implemented test chip in CMOS 65-nm are presented and compared with other state-of-the-arts receivers. At the end, extension of the superheterodyne DT receiver to a SAW-less operation is discussed and measurement results of a test chip in CMOS 28-nm are reported.

6.1 The Structure

Figure 6-1(a) shows the simplified DT receiver. In this RX signals at the mixer outputs are still continuous-time (CT). In addition to the main harmonic of the mixer clocks, $LO_{I/Q}$, they also possess odd harmonics (i.e. $+3^{rd}$, -5^{th}, $+7^{th}$, etc.) due to their square-like waveforms (see Figure 6-1(b)). These harmonics not only downconvert high-frequency images on top of the wanted signal, but also upconvert the input spectrum to high frequencies around the harmonics. In reality, the windowed current integration, sampling and DT processing of samples happen in the subsequent switched-capacitor block. As mentioned earlier, the sampling folds spectrum of

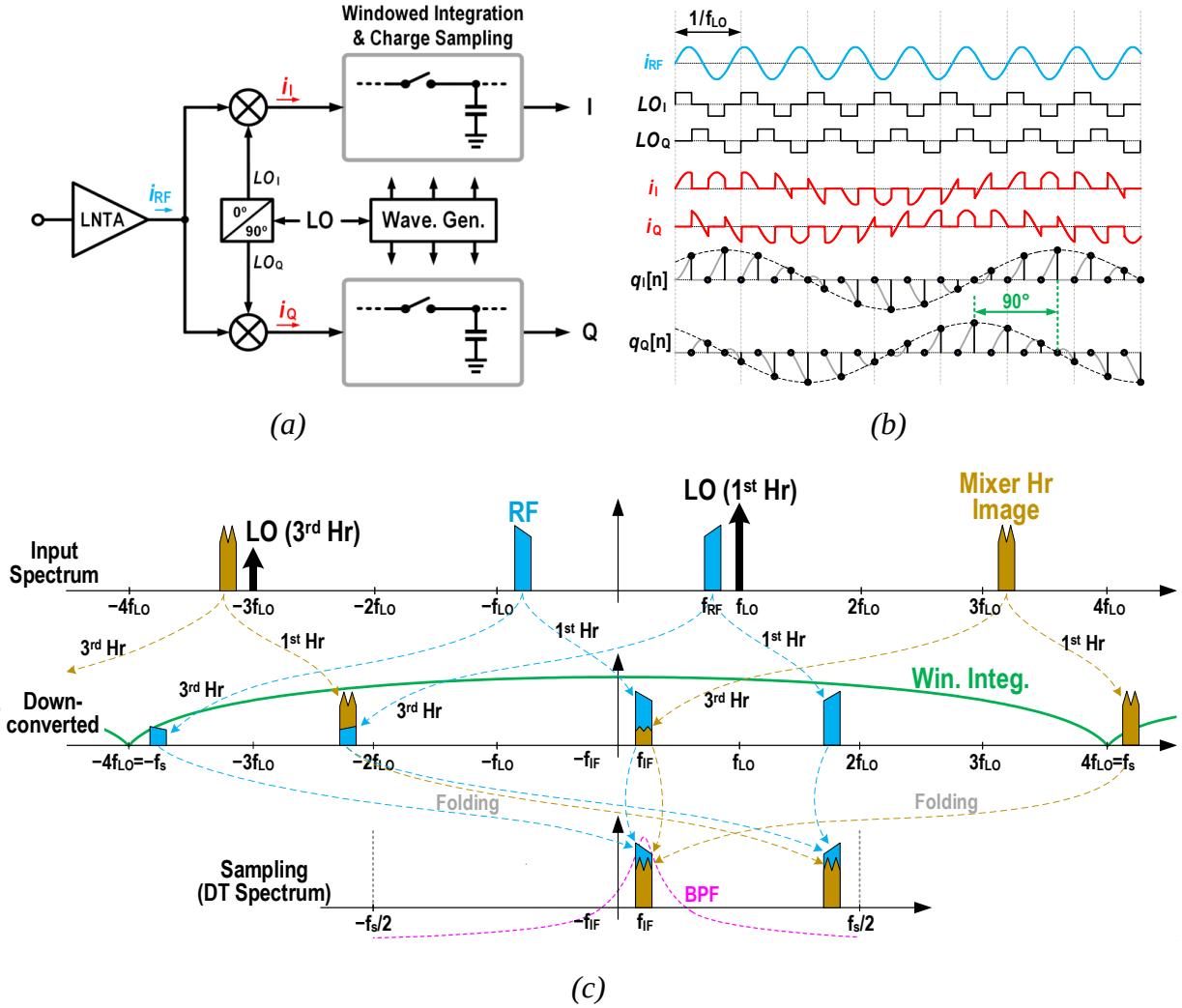


Figure 6-1: (a) Signal sampling after the mixer in a DT receiver with (b) its time-domain signal waveforms (repeated from Figure 2-3 and Figure 2-7). (c) Frequency translation considering CT mixing and then sampling. Although only the main and 3rd harmonics of mixer are shown, it still make a rather complicated frequency translations.

the signal that is outside of the Nyquist range into the $-f_s/2$ to $+f_s/2$ range. Since both *mixing* and *sampling* processes translate frequencies with respect to the LO harmonics and sampling rate, respectively, they make a rather complicated matrix to calculate total frequency translations from RF input to the sampled output of the receiver (see Figure 6-1(c)).

The top-level diagram, shown in Figure 6-2, provides a straightforward yet accurate model for the DT receiver, illustrating its functionality and the scheme of frequency translations. Since the accumulated charge is read out by the switched-capacitor filter at the 4x rate, and also the states of mixer clocks are changing with the same rate (i.e., 4 times in each cycle), these operations are mutually commutative so it would make no difference if we consider the WI and

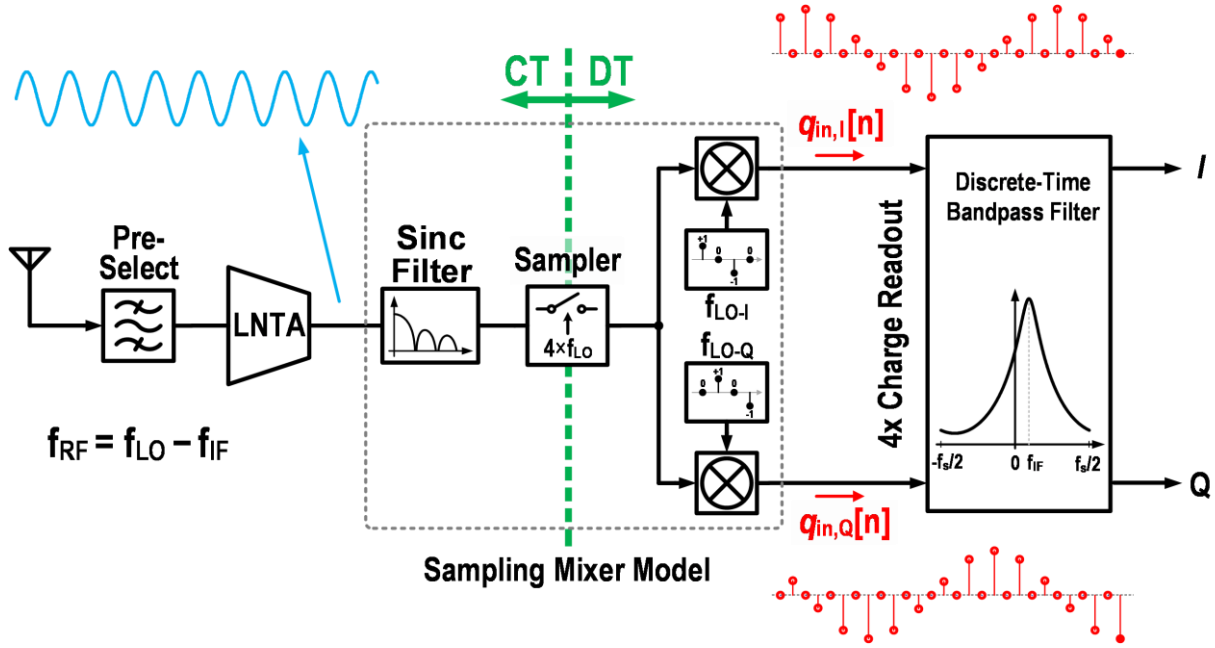


Figure 6-2: The proposed DT superheterodyne receiver model using 4x sampling.

sampling executed ahead of the mixing. In this way, the rest of signal processing after the sampling is done in the discrete-time domain[6]. Therefore, the "DT mixers" interpret their input signals as DT input sequences instead of the CT square waveform. Also, the outputs of DT mixers become sampled-charge data rather than the CT i_I and i_Q waveforms of Figure 6-1(b). This model will be later used to calculate the gain and to illustrate the frequency translations of the DT receiver. Moreover, this model can be used also for other IF sample rates (e.g. 1x/2x) by placing a DT decimation block after the DT mixer in Figure 6-2.

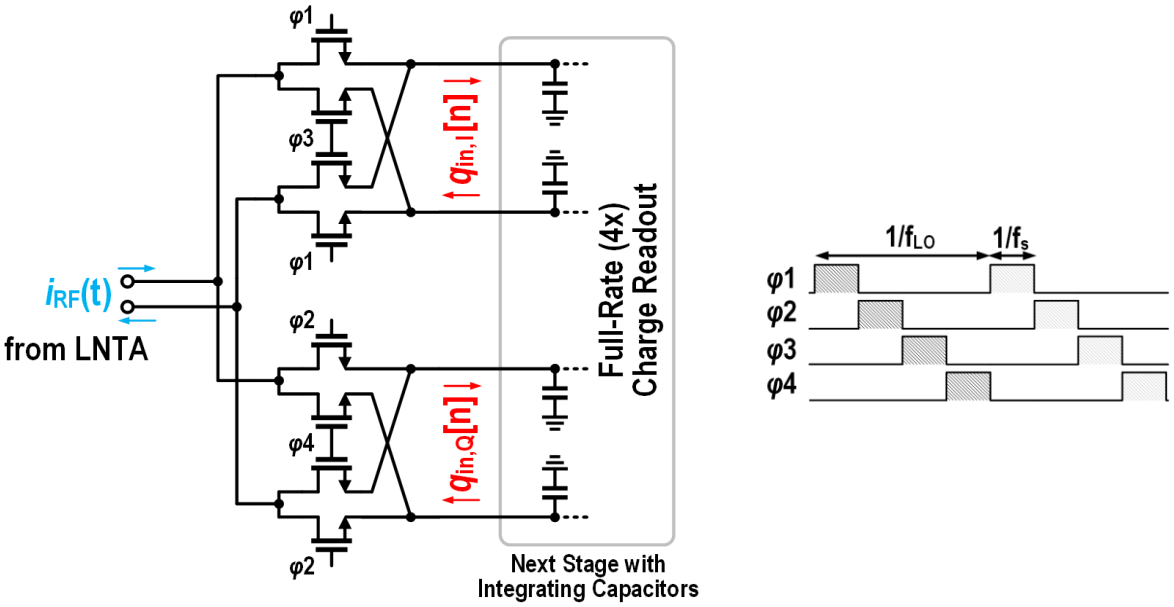
Discrete-time charge packets after windowed integration and sampling are described with the following equation [5], [10], [22], [23]:

$$q_{in}[n] = \int_{(n-1)T_s}^{nT_s} i_{RF} \cdot dt\,, \tag{6.1}$$

where i_{RF} is the result of a voltage at LNTA input (V_{RF}) multiplied by the transconductance $g_{m,LNTA}$. This WI creates a continuous-time *sinc* type filter prior to the sampler in Figure 6-2:

$$H_{WI}(f) = T_s \times \frac{\sin(\pi f T_s)}{\pi f T_s} = T_s \times \mathrm{sinc}\left(\frac{f}{f_s}\right). \tag{6.2}$$

[6] Ref. [25] explains well the difference between CT and DT interpretation of signals in a DT mixing receiver.



(a) *(b)*

Figure 6-3: (a) Implementation of the sampling mixer in Figure 6-2 with passive current commutating mixer, and (b) it driving clock waveforms.

This filter has notches at multiples of f_s.

6.1.1 Sampling Mixer

The clock sequences of DT mixers in Figure 6-2 are $LO_I[n]=\{1\ 0\ -1\ 0\}$ and $LO_Q[n]=\{0\ -1\ 0\ 1\}$, repetitively. They could be written as:

$$\begin{cases} LO_I[n] = \frac{1}{2}e^{j\left(\frac{\pi}{2}n\right)} + \frac{1}{2}e^{-j\left(\frac{\pi}{2}n\right)} \\ LO_Q[n] = \frac{1}{2}e^{j\left(\frac{\pi}{2}n+\frac{\pi}{2}\right)} + \frac{1}{2}e^{-j\left(\frac{\pi}{2}n+\frac{\pi}{2}\right)} \end{cases} \tag{6.3}$$

In frequency domain, they have two tones at $\pm f_s/4$, which is f_{LO}. From (6.3), downconversion (as well as upconversion) gain of each DT mixer becomes $A_{mix,I/Q} = 1/2$. However, output of the mixer in the Q path has a 90º phase shift with respect to the I path.

Implementation of the sampling mixer circuitry is depicted in Figure 6-3(a). It consists of two passive double-balanced mixers for I and Q paths. Each mixer commutates its input current provided by the LNTA. While input of the RF mixer is actually a CT current, their outputs are interpreted as DT charge packets resulting from the windowed integration. Each new coming phase generates a new charge sample. The next block, DT BPF, should read charges also at the 4x rate to maintain the sample rate.

Mixer switches are implemented by NMOS-only. As depicted in Figure 6-3(b), non-overlapped clocks with a 25% duty cycle are used to drive the switches. This avoids charge cross-talk between *I/Q* paths, which would compromise functionality of the subsequent block. Moreover, driving switches with the 25% duty cycle improves IIP3, noise and gain of the mixer, as compared to the 50% duty cycle [15]. In our implementation, the sampling mixer works up to 12 GS/s, limited only by the digital clock generator circuit.

6.1.2 Receiver Chain

Receiver chain from RF input to the end of IF strip is shown in Figure 6-4. Four charge-sharing BPFs are cascaded to increase rejection of out-of-band blockers/interferers. In addition to providing isolation, each of the gm-cells between the BPFs serves as a DT gain stage providing 0–6 dB signal gain. In this way, noise of each subsequent block gets less important. All the CS-BPFs operates with the same 4x sampling rate.

Until this stage, the receiver has had enough out-of-band filtering. Therefore, to save power consumption, signal can be decimated and the baseband circuit is clocked at the lower rate. To do so, an additional gm-cell stage is used at the end of IF strip that again converts voltage to charge. This creates a sinc antialiasing filter before the decimation.

6.2 Frequency Translation

The whole process of frequency translations that happen in the proposed HIF DT receiver is depicted in Figure 6-5. As the continuous-time input signal enters the receiver, whose model is shown in Figure 6-4, it is filtered by the CT sinc filter described in (6.2). Images are then created due to sampling, as indicated in brown in Figure 6-5 (a). In this example, we choose RF signal at $f_{LO}-f_{IF}$, such that sampling images are at $-f_{LO}+f_{IF}+k\cdot(4f_{LO})$ and $f_{LO}-f_{IF}+k\cdot(4f_{LO})$ for k=1, 2, 3, … . From (6.2), sinc filter attenuations of the first two images (k=1) near 3rd and 5th f_{LO} harmonics are 9.5 dB and 14 dB, respectively. These levels are the same as image attenuation of a CT 4-phase mixer. Although these numbers alone might not be adequate, the images are further attenuated in this receiver by the LNTA and a preselect filter.

After sampling, the DT input spectrum is now spread from $-f_s/2$ to $+f_s/2$, where f_s is $4f_{LO}$.

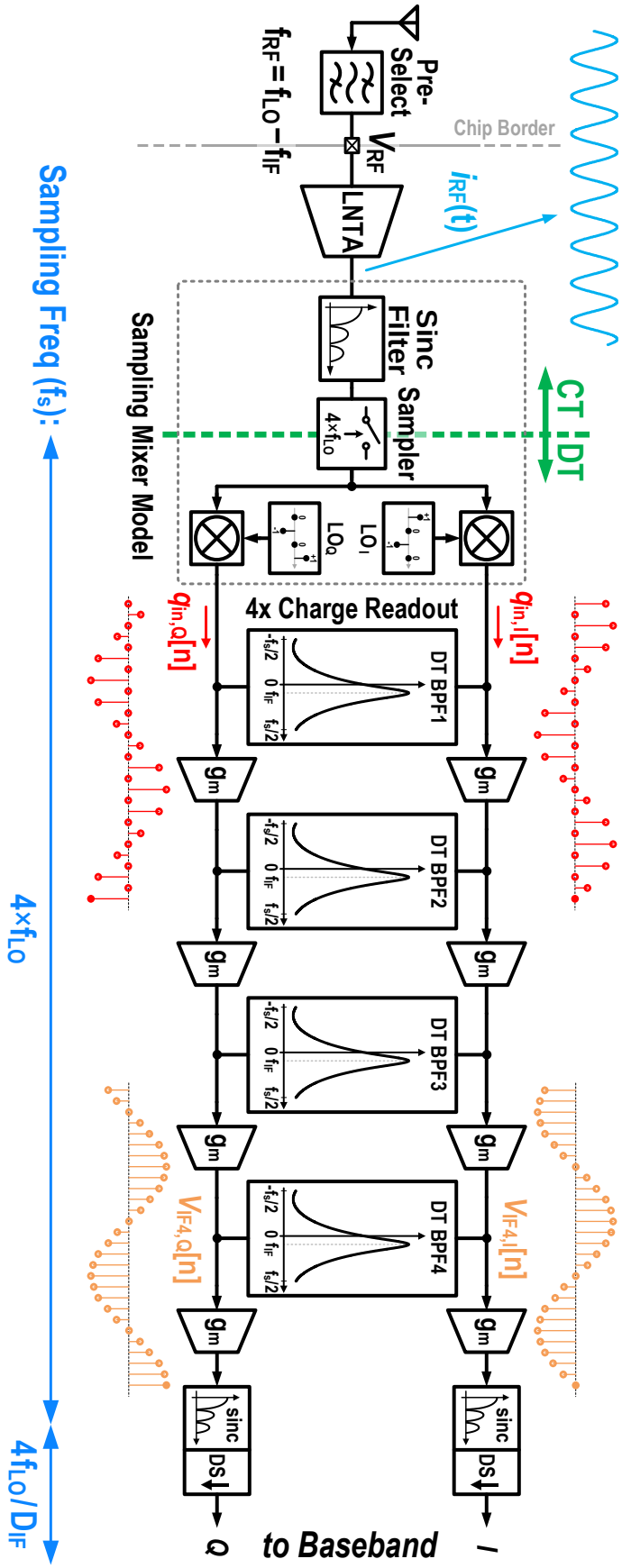


Figure 6-4: The proposed DT superheterodyne receiver using 4x sampling.

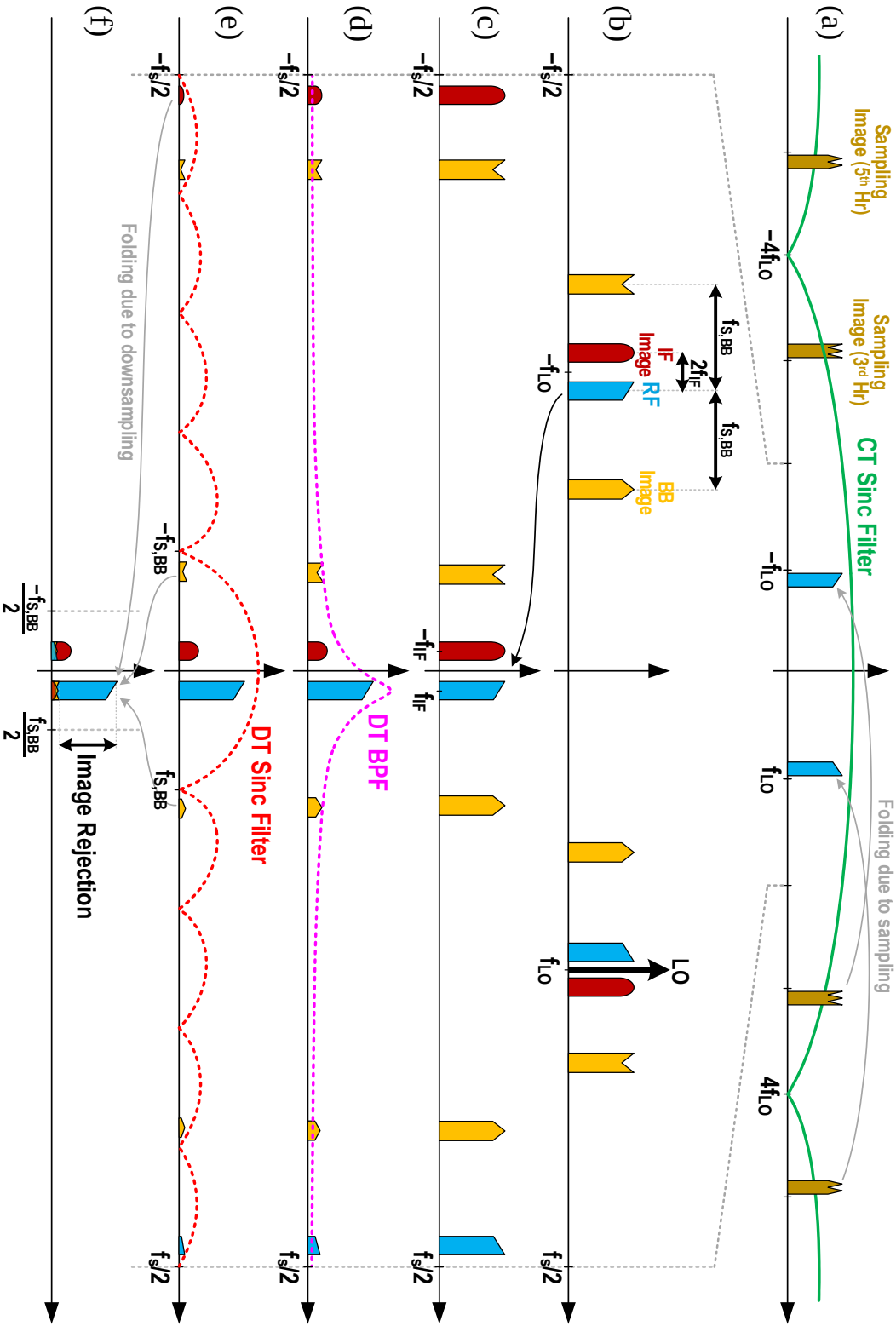


Figure 6-5: Frequency translations in the DT receiver: (a) images caused by sampling of CT signal; (b) input spectrum after the sampling; (c) downconverted spectrum after the DT mixer; (d) signals after IF filter stages; and decimation by (e) applying an antialiasing filter before (f) baseband downsampling.

Figure 6-5(b) shows the wanted RF signal (in blue) and the important images of the receiver[7]. Complex LO signal defined in (6.3) is also displayed as a black single tone. After mixing the entire signal spectrum with this tone, the negative side is downconverted to around dc, while the positive side is upconverted to close to $\pm f_s/2$ (see Figure 6-5(c)). At this point, the wanted signal is located at $+f_{IF}$ while its IF image (in red) at $-f_{IF}$. Because of the quadrature operation of the mixer, these two signals are not aliased and the image can be filtered at IF and later at baseband (BB).

The spectrum of Figure 6-5(c) is then filtered by the complex DT BPFs in the IF strip (see Figure 6-5(d)). The wanted signal is amplified while the rest are attenuated. At this point, out-of-band images and blockers are attenuated enough, such that the signal of interest can be decimated to a lower baseband sample rate, $f_{s,BB}$. This leads to power consumption reduction for the remainder of processing blocks.

The decimation process is being protected by a DT sinc antialiasing filter that is simply achieved by adding up D_{IF} samples (a.k.a., moving average filter), where D_{IF} is a positive integer. Therefore, the images are further filtered out (Figure 6-5(e)) before downsampling and aliasing over the wanted signal (Figure 6-5(f)). The new sample rate becomes $f_{s,BB} = f_s/D_{IF}$. Transfer function of the moving average (MA) filter is:

$$H_{MA,IF}(f) = D_{IF} \times \mathrm{sinc}\left(f / f_{s,BB}\right). \tag{6.4}$$

A small resulting attenuation of the wanted signal at f_{IF} is neglected in the rest of the text. Implementation of the decimation is trivially achieved by lowering the readout rate of the block succeeding the gm-cell. In this way, after several samples are accumulated, they are processed once (temporal decimation [28]).

Considering the frequency translations in Figure 6-5 and the receiver model shown in Figure 6-4, we are now able to calculate gain of signals at different frequencies from the LNTA RF input to the IF strip output. The wanted RF signal experiences the LNTA gain, windowed integration sampling, DT mixer downconversion gain, passband gain of BPFs and gm-cells.

[7] Though blocker and image signals could be at a much higher level than the wanted signal, they are shown at the same level for simplicity.

Using (4.5), (4.8), (6.2), and (6.3) we have:

$$G_{wanted} = V_{IF\,4,I/Q} / V_{RF} = \left[g_{m,LNTA} H_{WI}\left(f_{LO} - f_{IF}\right) A_{mix} A_{BPF}\right] \times \left[A_{gm,IF} A_{BPF}\right]^3 \approx \left[g_{m,LNTA} \mathrm{sinc}(1/4) \times 1/2 \times \frac{1}{f_s C_R}\right] \times \left[\frac{g_{m,IF}}{C_R f_s}\right]^3 . \quad (6.5)$$

In the above equation, the two terms are gain of the stages until the first BPF, and the 2nd to 4th BPFs, respectively. In the approximation, $f_{IF} << f_{LO}$ is considered.

The closest image that could fold onto the wanted RF signal is the IF image at $f_{LO}+f_{IF}$. As shown in Figure 6-5(e), part of the IF image energy after mixing and attenuation resides at $-f_s/2+f_{IF}$. This signal is folded over the wanted signal after downsampling, assuming an even decimation factor, D_{IF}. By neglecting a small gain difference due to the CT sinc filter (H_{WI}), IF image rejection is calculated by adding attenuations of the BPFs and DT moving average filter. Using (4.3), gain of BPF at $-f_s/2+f_{IF}$ can be very well approximated by $1/(2C_H)$ for $C_R << C_H$. So the attenuation of BPF with respect to its passband gain in (4.5) is $2C_H/C_R$, for each of the four stages. Therefore, by adding effect of the moving average filter from (6.4), IF image rejection ratio (IMRR) is:

$$IMRR_{IF} \approx \left(\frac{2C_H}{C_R}\right)^4 \Bigg/ \left|\mathrm{sinc}\left(\frac{-f_s/2 + f_{IF}}{f_{s,BB}}\right)\right| . \quad (6.6)$$

Considering $f_{IF}=f_{LO}/16$ in our implementation, Eq. (4.4) suggests C_H/C_R to be about 10. Consequently, with the D_{IF} decimation factor of 16, the total IF IMRR reaches more than 135 dB. Note than this value assumes perfect quadrature LO signals driving the mixers without any mismatch. However, quadrature inaccuracy of the practical LO signals also aliases a tiny part of IF image right after the mixers, from $f_{LO}+f_{IF}$ to $+f_{IF}$ in Figure 6-5(b) and (c). The latter effect is predominant and limits $IMRR_{IF}$ to 40–80 dB, depending on quadrature accuracy, layout, and mixer mismatch.

The second important class of images are baseband downsampling images. Translated back to the RF input, they are located at $f_{RF} \pm k \cdot f_{s,BB}$. The first two of them (for k=1) are shown in yellow in Figure 6-5(b). After mixing down (Figure 6-5(c)) and passing through the BPFs (Figure 6-5(d)), they are attenuated by the DT moving average filter (Figure 6-5(e)), and then folded over the wanted signal via downsampling (Figure 6-5(f)). By means of (4.3), the exact

attenuation of BPF can be calculated. As a first-order approximation of (4.3) for midrange frequencies ($f_{IF} << f << f_s/2$), Bode plot of a 1st-order lowpass filter with a 3 dB bandwidth of f_{IF} is being considered that is shifted to be centered at f_{IF}. So, BPF rejection at $f_{s,BB}$ offset from the passband is approximated as:

$$R_{BPF}(f) \approx \left. \frac{f - f_{IF}}{f_{IF}} \right|_{f = f_{IF} + f_{s,BB}} = \frac{f_{s,BB}}{f_{IF}}. \tag{6.7}$$

Both sampling images are attenuated by the same amount, due to the symmetry around f_{IF}. The higher $f_{s,BB}$, the higher the attenuation. Then, the images are attenuated by the moving-average filter in (6.4). A higher $f_{s,BB}$, makes the images relatively closer to notches of the sinc filter and improves attenuation. Adding up all these attenuations, baseband downsampling IMRR becomes:

$$IMRR_{BB} \approx \left(\frac{f_{s,BB}}{f_{IF}} \right)^4 \Bigg/ \left| \mathrm{sinc}\left(\frac{f_{IF} \pm f_{s,BB}}{f_{s,BB}} \right) \right|. \tag{6.8}$$

By choosing a proper number of BPF stages and decimation factor to set $f_{s,BB}$, a desired IMRR can be achieved.

6.2.1 Selection of IF Frequency

Based on (6.8), if the ratio of $f_{s,BB}/f_{IF}$ is fixed, changing IF would not have any major impact on the BB IMRR. If improving this rejection is desired, $f_{s,BB}$ had to be increased. In case ADCs are used at the end of IF chain, higher $f_{s,BB}$ means a higher ADC sample rate. On the other hand, if a fixed ratio is considered, lowering f_{IF} results in a narrower bandwidth of BPF's, and hence, higher linearity (IIP2 and IIP3) at a fixed offset frequency. However, f_{IF} should be always higher than the IM2 product and the flicker noise corner.

In this work for the sake of simplicity, a sliding IF approach with $f_{IF} = f_{LO}/16$ is used. With $f_{s,BB}=4f_{IF}$ used in our analog baseband implementation, theoretical BB IMRRs could reach 59 and 63 dB for the images at $f_{RF}+f_{s,BB}$ and $f_{RF}-f_{s,BB}$, respectively. In transistor-level simulations, 46 dB and 51 dB rejections are obtained, respectively. The shortfall is due to lowering of the quality factor of BPFs by the output resistance of IF gm-cells.

6.3 Baseband Signal Processing

The signal at the end of IF strip can be directly sampled and digitized using Nyquist-rate or band-pass ADC [7]. Afterwards, baseband signal processing, including IF mixing and channel select filtering, can be done entirely in digital domain. Among various ADC architectures, especially SAR ADC is attractive for this receiver, due to its process scalability and compatibility with digital CMOS technology. However, this approach might not be always the most power efficient because of the high sample rate and high dynamic range requirement imposed on the ADC and subsequent digital signal processing.

The alternative approach chosen in our 65-nm CMOS implementation is signal processing through the DT analog baseband, as shown in Figure 6-6(a). The main goal of this part of receiver is, by means of filtering and decimation, to reduce the required ADC sample rate and dynamic range. The proposed DT baseband consumes only a few miliwatts, while significantly reducing power consumption of the ADC and digital baseband.

6.3.1 DT Analog Baseband Signal Processing

The first stage of the analog baseband circuitry is a quadrature DT IF mixer. A set of *four* mixers downconvert the signal from IF to zero. Implementation of each mixer is similar to the passive RF mixer shown in Figure 6-3. The baseband sample rate ($f_{s,BB}$) is chosen $4f_{IF}$ to simplify the generation of clocks needed for the IF mixer. As shown in Figure 6-6(b), the IF clock waveforms are very similar to those in the RF mixer, but the period is $1/f_{IF}$. If a higher attenuation of the sampling images would be required (e.g., for a SAW-less application), a higher baseband sample rate combined with harmonic rejection mixing could be implemented. The IF mixer is the only circuitry in this receiver that limits the overall IIP2, even though it is still extremely high. Since the IF mixer is clocked at a much lower rate than the RF mixer, its IIP2 is substantially better [69]. Moreover, the IF filtering considerably improves its IIP2 referred back at the antenna (each 1 dB of a blocker filtering at preceding stages improves IF mixer IIP2 by 2 dB).

The second stage of the analog baseband is a DT 6^{th}-order low-pass filter (hereafter, IIR6), based on the work in [5]. This narrow-bandwidth filter selects the wanted signal and attenuates the rest of in-band and out-of-band interferers and blockers. Thanks to its high filtering order,

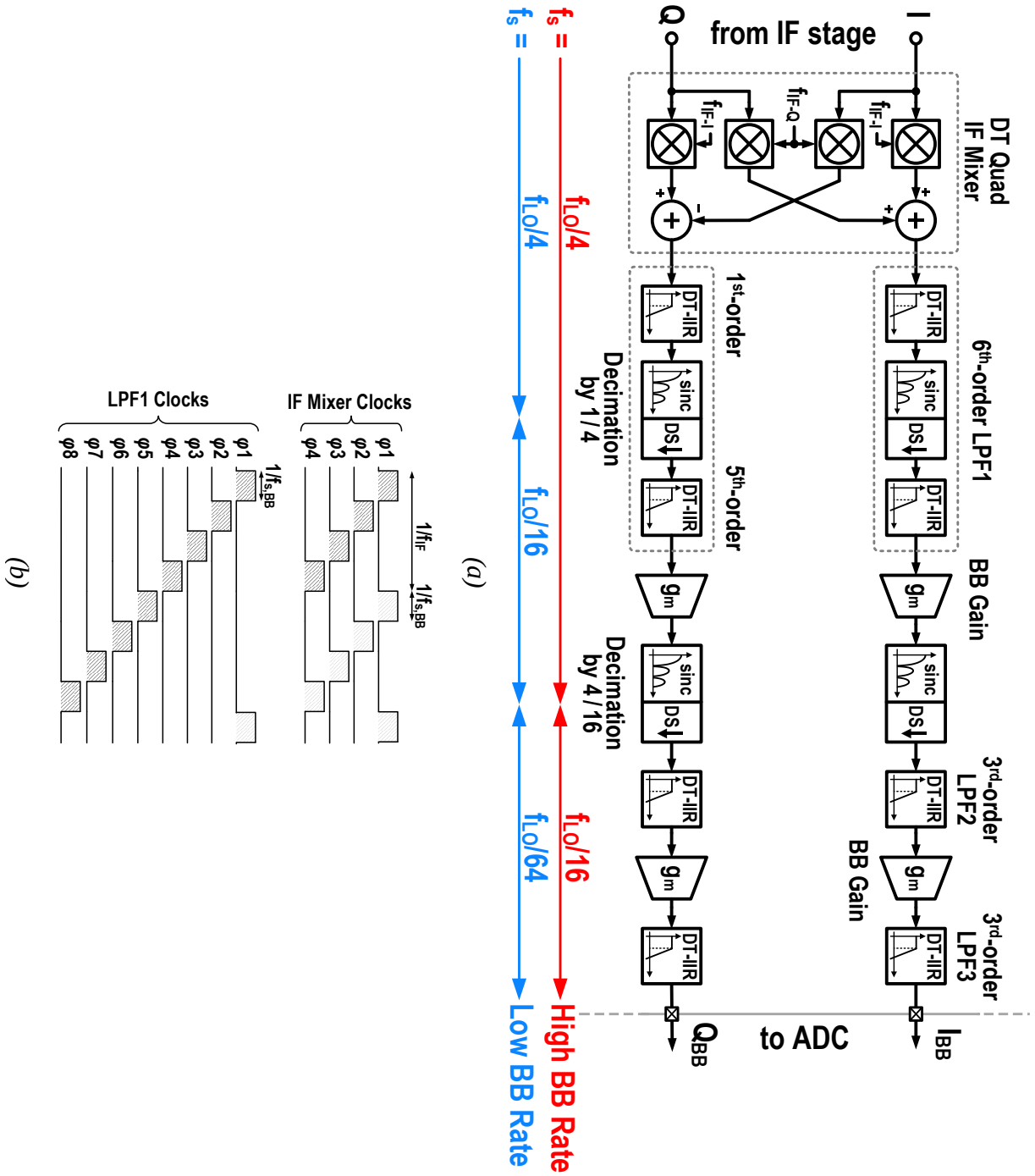


Figure 6-6: (a) Baseband DT signal processing of the receiver. (b) Required clock waveforms for the IF mixer and LPF1.

IIP3 requirements of all the following stages are relaxed. Sample rate of this filter is also the same as $f_{s,BB}$. Figure 6-7 shows a switch-level implementation of this filter. C_{H1} at the input port accumulates the input charge. Through a prearranged switching sequence, each of the C_S capacitors rotates the partial charge of C_{H1} to other history capacitors, C_{H2-6}, and then gets reset.

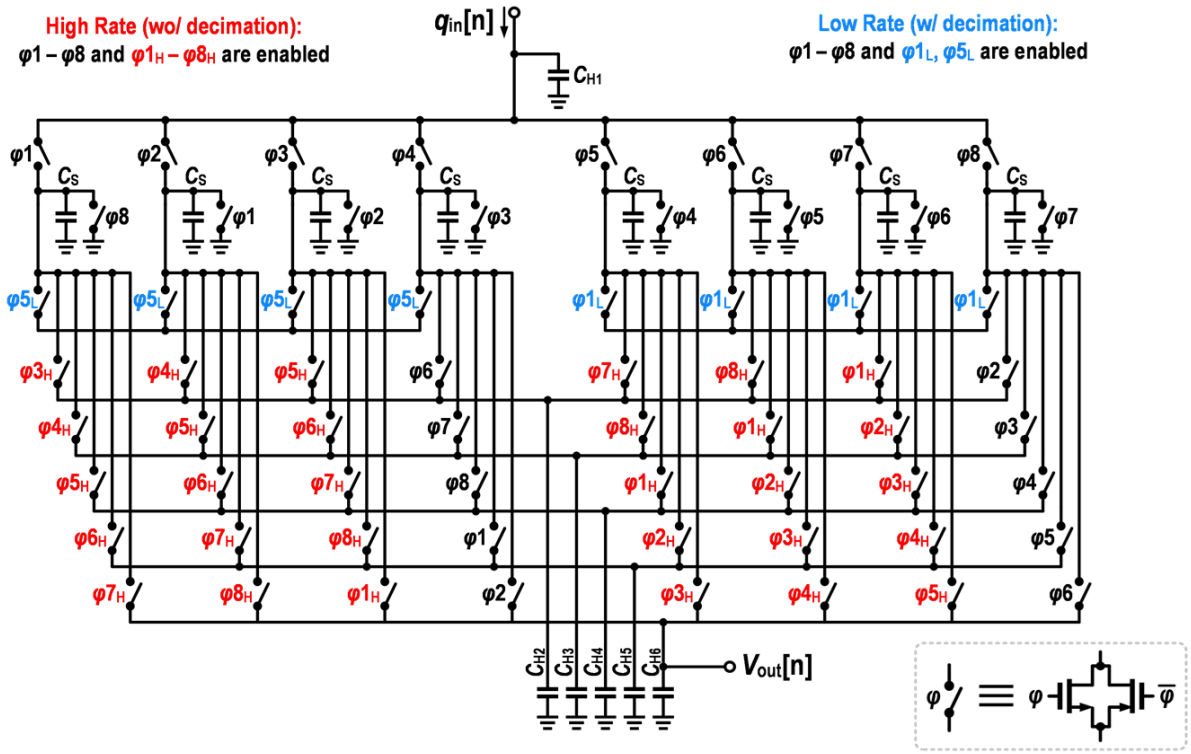


Figure 6-7: Implementation of the DT 6th-order IIR low-pass filter with selectable decimation by 4.

Each charge-sharing operation within the cycle adds one order of filtering. Using 8 sampling capacitors, each with a delay of one phase, increases the filter's sampling rate 8 times while using the same clock signals (parallelized operation). More details and analysis of this filter are described in [5]. In the normal high sample rate mode, black and red switches are clocked and the filter works as described. This mode is used for high bandwidth signals up to about 30 MHz (e.g., for the LTE standard). For narrowband signals (e.g., 200 kHz in GSM standard) the sample rate of $4f_{IF}$ (several 100s of MS/s), would be much higher than necessary. Further decimation should therefore be done to save power consumption. In this low sampling rate mode, only black and blue switches are clocked and the red switches are disengaged to save power. After a set of four succeeding C_S*'s* are charge-shared with C_{H1}, they are shorted together to make a spatial decimation by 4 [28]. Charge sharing of the four C_S*'s* makes a 4-tap moving average (sinc antialiasing filter) prior to the subsequent decimation. Then one of them continues charge-sharing with $C_{H2–6}$. This also reduces the required C_H value to support the narrow bandwidth. In this mode, input sample rate of this filter is $4f_{IF}$ while its output rate is reduced to f_{IF}. Clock waveforms required for driving this filter are shown in Figure 6-6(b).

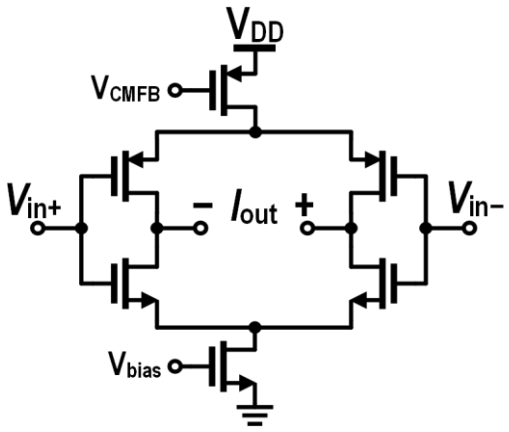


Figure 6-8: Implementation of baseband gm-cells..

The receiver path up to the end of IIR6 already enjoys high gain and high-order of filtering. Hence, noise and IIP3 of the remaining stages would be less of a concern. Due to this reason, the following stages can be implemented at an ultra-low power consumption. After IIR6, two filter stages are cascaded with two gm-cells. Figure 6-8 shows the implementation of baseband gm-cells, in which a fully differential inverter-based structure is used. Note that the baseband gm-cells are dc-coupled to pass the whole signal spectrum. Although putting tail current sources in the gm-cell reduces IIP3, the cell still features good enough linearity (IIP3 = 0 dBm) considering the filtering beforehand. Both stages of the 3rd-order IIR LPFs ("IIR3") are identical and use the same structure as in Figure 6-7, though without spatial decimation [5]. To further save power in these filters, their clocks are reduced by 4x with respect to the IIR6 output rate. This creates a temporal decimation after the first baseband gm-cell. The two baseband gain stages together with LPF2 and LPF3 in *I* and *Q* paths totally consume only 100–700 μW, depending on gain and bandwidth setting.

At the bottom of Figure 6-6(a), sample rate of each block from IF to the end of baseband is displayed. Due to the high total order of filtering (up to the 12th order in this design), ADC sample rate could be reduced to below the receiver output sample rate without any other antialiasing filter.

6.3.2 Digital Equalization

The analog baseband part of the receiver features the total of 12th-order of filtering. However, despite this very high order, only real-poles are used, and so this filter cannot be directly compared with complex-pole filter types (e.g., Butterworth or Chebyshev) of the same order. A

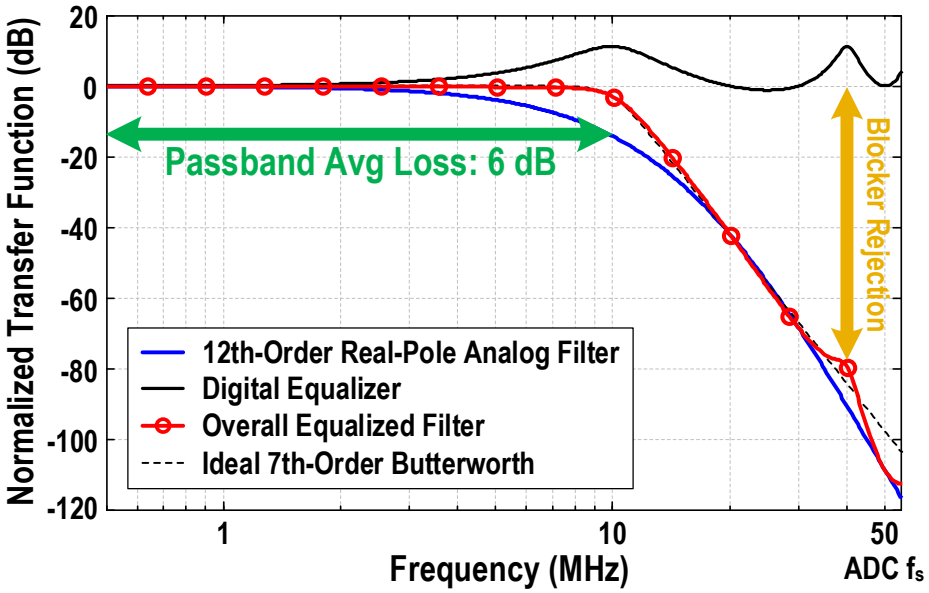
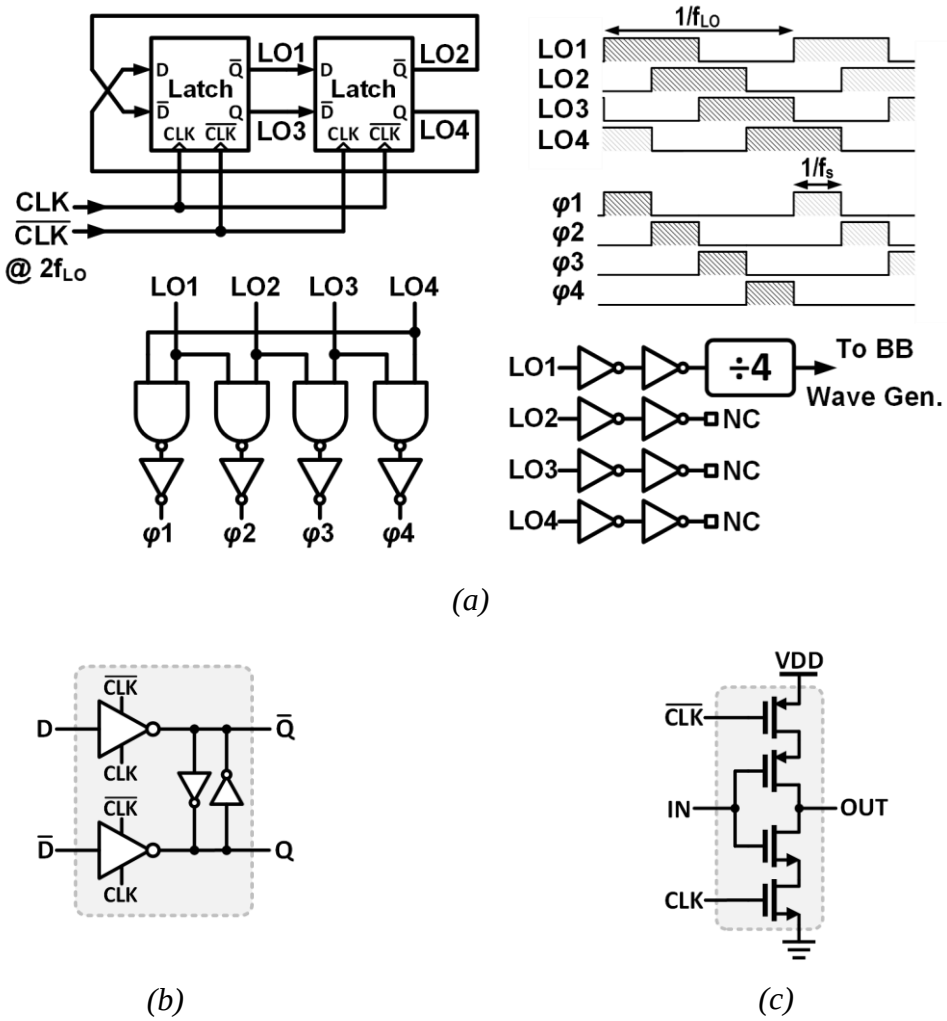


Figure 6-9: Digital equalization of 12th-order real-pole transfer function to better than a 7th-order Butterworth filter. The ADC and digital equalizer are clocked at 50 MHz.

high-order real-pole filter provides a gradual and smooth transition between its passband and its sharp out-of-band roll-off (Figure 6-9). Therefore, [5] has proposed using a low-power digital equalizer after the ADC to map the real-pole transfer function to a sharp complex-pole filter, but with a lower order. In this way, passband of the filter experiences a small average loss. The lower order of the mapped filter, the lower the passband loss [5]. For example, in Figure 6-9, the 12th-order real-pole filter is considered to be mapped to a better than 7th-order Butterworth filter (that should be enough for BB filtering of most wireless standards). As has been calculated, the passband loss is 6 dB that can be compensated by preceding gain stages or 1 additional ENOB in the ADC [5]. Taking into consideration the complete system-level view of the receiver, the proposed baseband processing consumes several times less power (total I/Q baseband: 2.3 mW for 1.96 GHz RF input) than the conventional CT or active switched-capacitor approaches [36], [38], while providing a much lower NF and a very high linearity [5].

6.4 Clock Waveform Generator

All the required clocks for the RF mixer (Figure 6-3) and IF BPF stages (Figure 6-5) are identical 25% duty-cycle clock waveforms at the LO frequency. First, an external clock at $2f_{LO}$ is fed in, then divided by 2 to generate four quadrature 50% clocks ($LO_{1\text{-}4}$ in Figure 6-10(a)). The divider consists of two latches arranged in a loop with a crossed feedback providing an



(a)

(b) *(c)*

Figure 6-10: (a) RF and IF waveform generator. (b) Dynamic latch using (c) gated inverter.

additional 180° phase shift. A similar approach is also used in [7]. As shown in Figure 6-10(b) and (c), two clock-gated (tristate) inverters with weak back-to-back inverters are used as a dynamic latch. This promotes a very high speed of operation at low power. Then, NAND gates are used to make the four 25% clocks ($\varphi_{1\text{-}4}$). Skewed NMOS and PMOS transistors in the NAND gates and their following buffers are used to ensure non-overlapped clocks. Required clocks for baseband are generated in a similar way using standard cells, whose reference clock is provided via a divide-by-4 of LO_1 clock. To keep the phases balanced, two levels of dummy buffers are used for $LO_{2\text{-}4}$. Transistors in the clock generator circuit are sized based on the phase noise requirement and load capacitance.

6.5 Measurement Results

The receiver is implemented in standard TSMC 1P7M 65nm CMOS and occupies an active

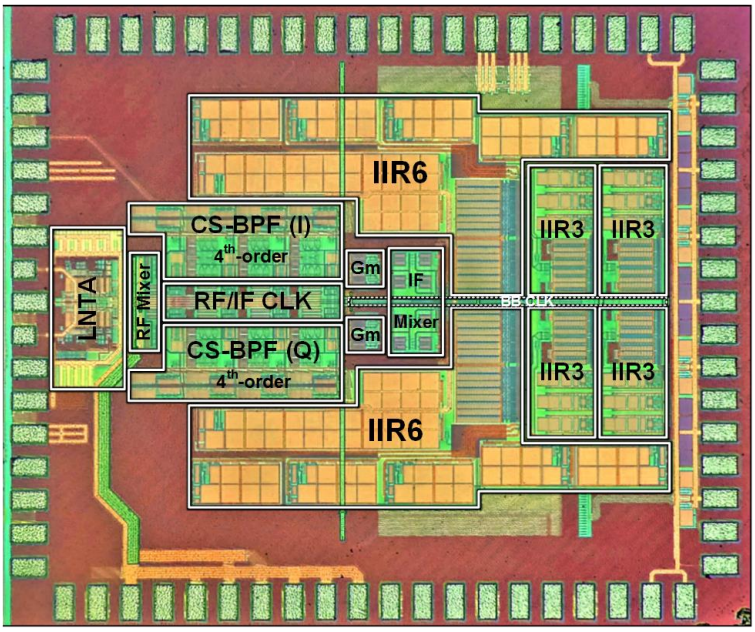


Figure 6-11: The proposed receiver's chip micrograph; 1.9×2.4 mm^2.

area of 1.1 mm^2 (Figure 6-11). It consists mostly of MOS switches, capacitors and inverter-based gm-cells, making it process scalable and amenable to digital nanoscale CMOS. Majority of the chip area is occupied by capacitors used for baseband filtering that supports cutoff frequencies down to 100 kHz. Most of the capacitors are of metal-oxide-metal (MOM) type implemented differentially. Therefore, the chip area scales very well with the CMOS technology advancements.

Measured wideband transfer function of the complete receiver is plotted in Figure 6-12. There are only discrete number of frequency points that can fold into the received band of interest. As analyzed in Section 6.2, major images (shown in yellow) are located at multiples of $4f_{IF}$ away from f_{RF}. The first two major images are rejected by 42 and 46 dB, close to the simulated values. The reminder of images at f_{IF} multiples (in black) are much smaller, and are caused by the baseband decimations. The exception is the image of 37dB rejection (marked in red) that is due to uncalibrated *I/Q* clock mismatch. There, unaccounted parasitics on the mixer clock lines make the *I/Q* unbalanced. Based on simulations, a phase mismatch of about 1^o could lead to the measured degraded rejection. A more carful layout design solves this in future designs (in [64], a 65 dB *I/Q* matching is achieved). Including the preselect filter with a moderate OOB rejection of 35 dB that precedes the receiver, the total image rejection easily improves to better than 72dB.

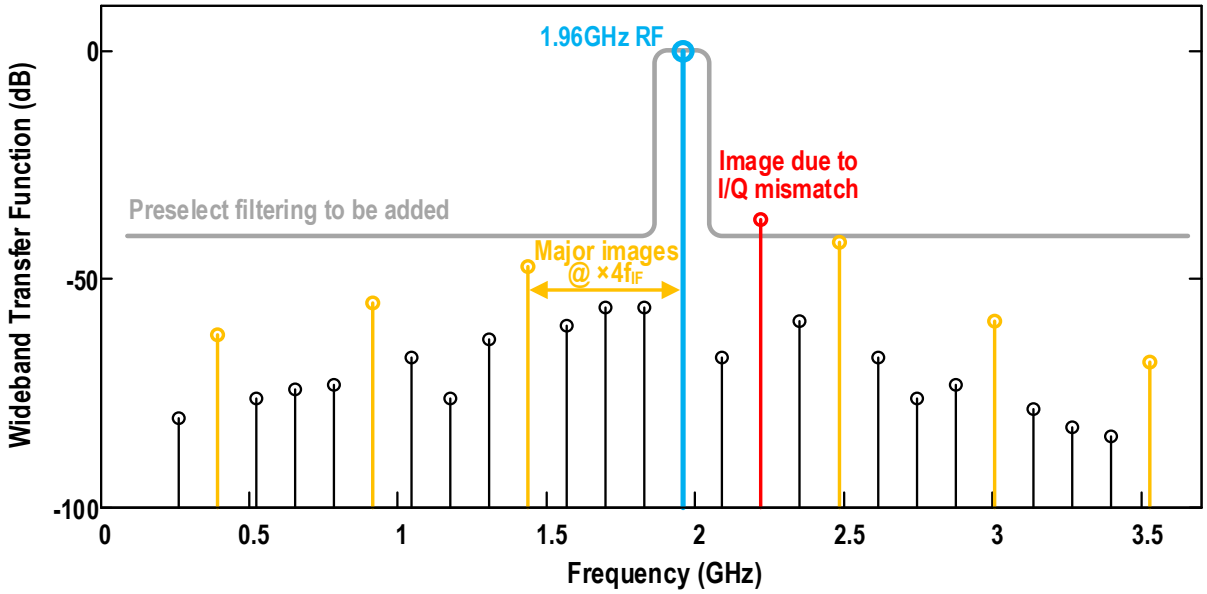


Figure 6-12: Measured wideband transfer function.

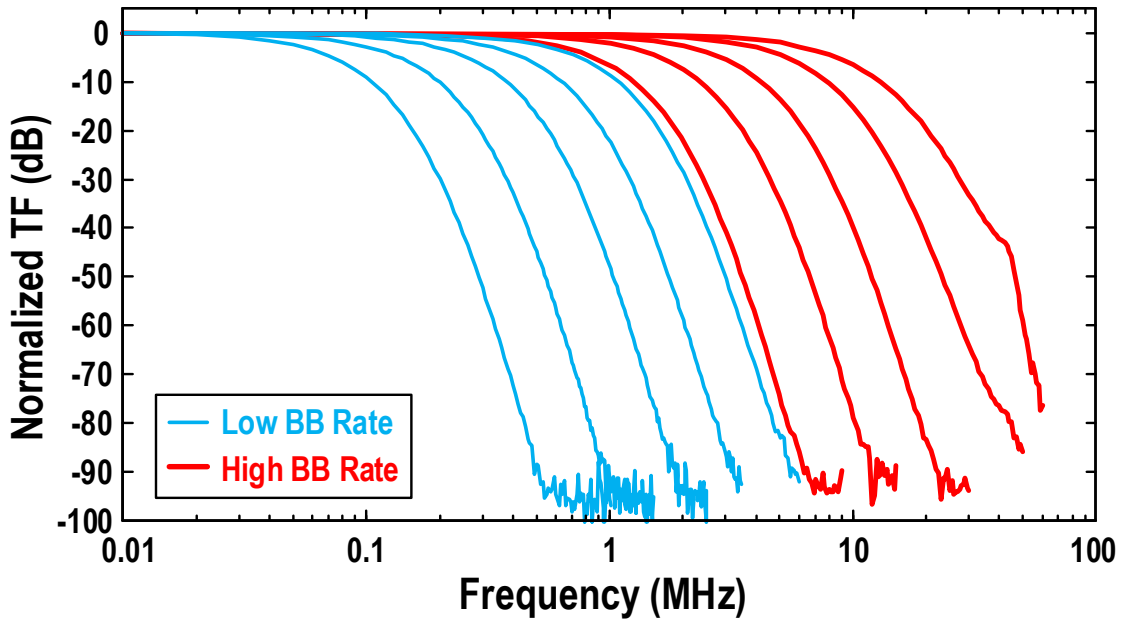


Figure 6-13: Measured close-in transfer function of the receiver.

Measured close-in transfer functions of the receiver for different programmed bandwidths at low/high baseband rates are shown in Figure 6-13. While the IF filters are designed mostly to reject out-of-band blockers/interferers, the close-in TF is created by the baseband filtering to select the desired channel. After converting to digital by the ADC, a digital equalizer will flatten the passband of transfer function, per the mixed-signal scheme of Figure 6-9. As a whole, RF bandwidth of the receiver is programmable from 200 kHz to 30 MHz.

Figure 6-14 shows measured uncalibrated IIP2 and IIP3 of the receiver at medium gain

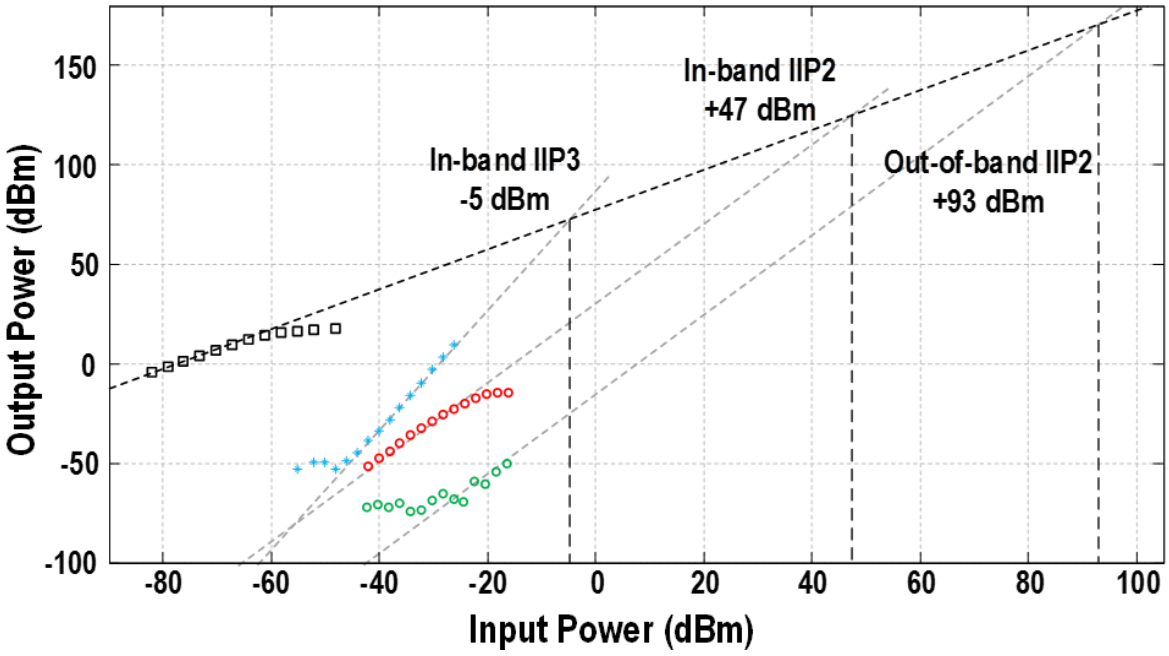


Figure 6-14: Measured IIP2 and IIP3.

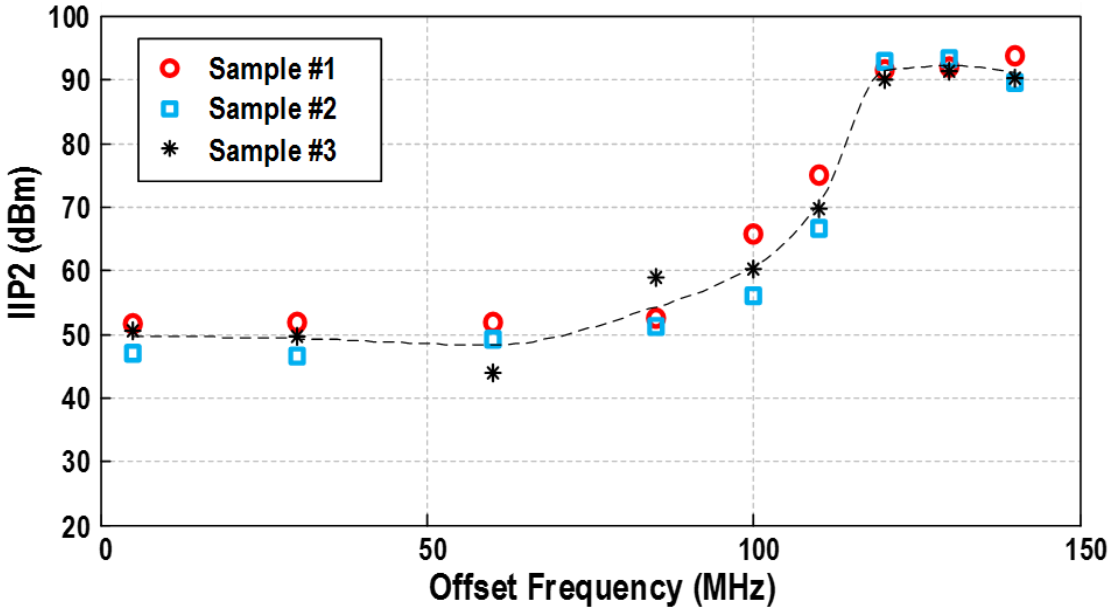


Figure 6-15: Measured IIP2 versus offset frequency.

setting, in which the receiver meets the sensitivity specification in presence of blockers. In-band IIP3 is measured at -5 dBm, which is mainly limited by the linearity of IF gm-cells. While the high-IF front-end has infinite IIP2, the IF mixer limits the receiver's IIP2. The IF filters in this receiver attenuate blockers and, therefore, out-of-band IIP2 increases rapidly at higher frequency offsets (Figure 6-15), from +47 dBm in-band to +93 dBm at 120 MHz offset, all uncalibrated. Though this receiver does not claim to be SAW-less, the superheterodyne architecture appears to be the path to reach such SAW-less operation that could meet most stringent IIP2

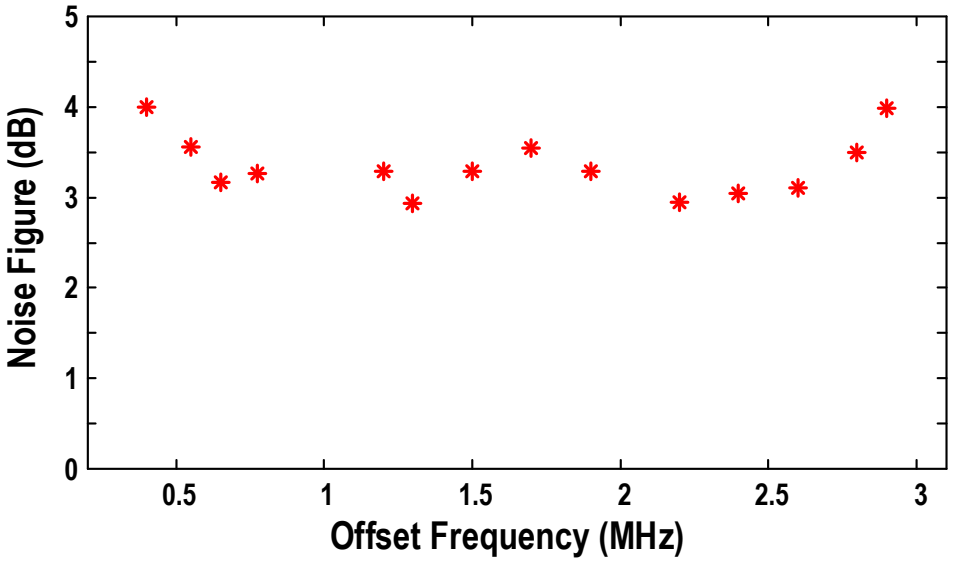


Figure 6-16: Measured noise figure of the complete receiver versus RF frequencies.

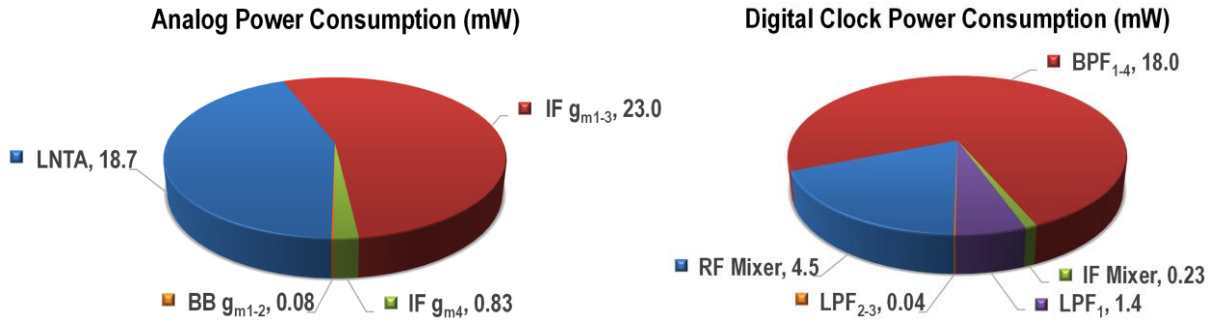


Figure 6-17: Power consumption budget of various blocks for maximum gain setting at 1.96 GHz RF input.

requirements, even in the FDD mode and without any calibrations.

Plotted in Figure 6-16, the noise figure of the complete receiver for different bands from 400 MHz to 2.9 GHz ranges between 2.9–4.0 dB. For each RF frequency, NF is the average value over the BW (anyway it stays constant over up to 3 times BW). At higher frequencies, duty cycle of $\varphi_{1\text{-}4}$ RF clocks is reduced because of a limited rise/fall times. As a consequence, the gain of RF mixer reduces, which directly degrades the RX noise figure.

Table 6-1 summarizes the measured performance of the receiver and compares it with published state-of-the-art. The analog part of the receiver consumes 43 mW in total for the high-gain setting. The clock waveform generator consumes 5–36 mW that linearly scales with f_{LO}. Figure 6-17 shows power consumption budgeting of different blocks. Full chain of the receiver has a maximum gain of 83 dB.

Table 6-1: Performance summary and comparison with state-of-the-art receivers.

	This Work	**[6] RFIC'13**	**[7] JSSC'11**	**[11] JSSC'10**	**[10] JSSC'06**	**[12] JSSC'14**	**[20] JSSC'14**	**[15] JSSC'09**
Technology	65 nm	65 nm	65 nm	90 nm	90 nm	65 nm	28 nm	90 nm
Architecture	Superhet.	Superhet.	Superhet.	Zero-IF	Zero-IF	Zero-IF	Zero-IF	Zero-IF
Description	Full DT	DT / N-Path	N-Path	Full DT	CT / DT	DT / CT	Full CT	Full CT
Analog BB / Order	Yes / 7th[§]	No	No	Yes / 2[¶]	Yes / 3[¶]	Yes / 2[¶]	Yes / 2[&]	Yes / 2[&]
RF Frequency (GHz)	0.4 – 2.9	0.5 – 1.2	1.8 – 2.2	0.5 – 3.8	0.8 – 6	0.5 – 3	0.4 – 6	0.8 – 2.2
Supply Voltage (V)	1.2 / 2	1.2	1.2 / 2.5	1.2	1.0 / 2.5	1.2 / 2.5	0.9	1.5
Power[†] (mW)	48 – 79	24.5	39	67 – 115	45.5 – 65.5	~ 210 – 540[#]	35 – 40	19.5 – 22.6
NF (dB)	2.9 – 4.0	7.5	2.8	5.3 – 6.0	5 – 5.5	5.5 – 8.8	1.8 – 3.1	2.2 – 3.2
Max Gain (dB)	83	35	55	58 / 64	> 47	35	70	61.5
In-band IIP3 (dBm)	-5	+10	-8.5	+1 / +2.5	-3.5	> -12.5	+4	N/A
Out-of-band IIP2 (dBm) / Calibration	+93 / No	–[*]	–[*]	38 – 52 / No	+60 / No	> +46 / No	+80 / Yes	+90 / Yes
Channel BW[‡] (MHz)	0.2 – 30	4.5	4	0.2 – 20	0.2 – 20	~ 26	1 – 100	~ 0.2 – 3.8
Area (mm^2)	1.1	0.45	0.76	0.5	3.8[##]	1.85[#]	0.6	–[*]

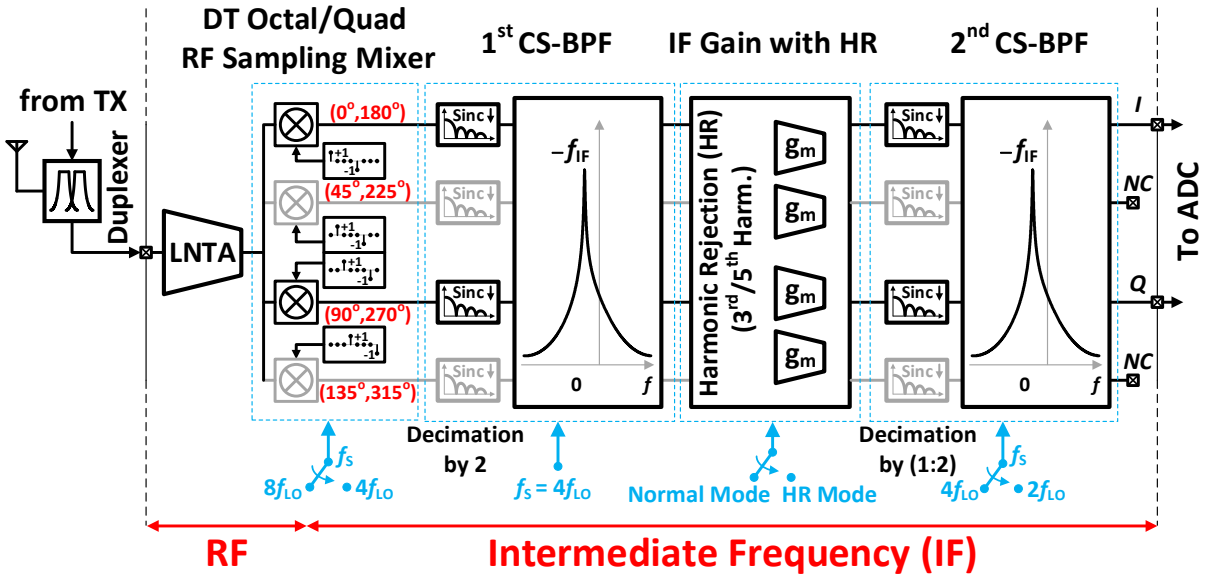
[†] At highest gain setting
[§] 12[th]-order real-pole mapped to a 7[th]-order Butterworth
[#] Synthesizer and bias is excluded
[‡] Two times BB bandwidth
[¶] Real-pole
[##] Including synthesizer
[*] Not reported
[&] Biquad

6.6 Extension to SAW-less Operation

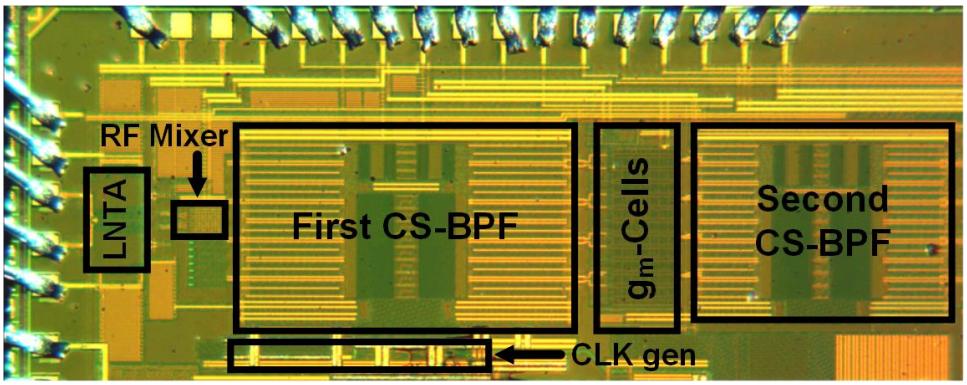
Conventional multi-band, multi-standard receivers require many duplexers, SAW filters, and switches typically one per band. To reduce cost and size, the trend is to eliminate SAW filters and switches by using a high linearity wideband RX [20], [70]–[72]. As a consequence, the isolation of transmitter (TX)-to-RX, and the suppression of TX interferers are worsening, which all further increase RX linearity requirements in FDD mode. The reduced off-chip out-of-band (OB) filtering implies a very tough IIP2 requirement for zero-IF receivers, thus requiring highly sophisticated calibration algorithms to be frequently run due to PVT and channel variations. There are many other issues associated with ZIF, such as time-variant dc offsets, sensitivity to flicker noise, and large in-band LO leakage. As explained in Section 2.1, superheterodyne architectures [21], [73] do not experience the aforementioned problems thanks to their high IF.

The 4x-sampling high-IF RX in [21] operates in discrete-time using a quadrature charge-sharing band-pass filter (CS-BPF) to realize a highly reconfigurable RX solution of small die area and high power efficiency. As in any wideband RX, the linearity and tolerance to out-of-band blockers mainly depends on its first filter's selectivity. Unfortunately, the 4/4-phase CS-BPF has insufficient blocker rejection to support the SAW-less operation. Using 8x-sampling [25] and the novel M/N-phase CS-BPF (described in Section 4.5) that utilizes an octal-phase input signaling and an extra pole to make a sharp filtering (i.e., 8/16-phase CS-BPF), the DT superheterodyne idea [21] is extended to the first-ever high-IF SAW-less RX is thus demonstrated [64], [65].

Figure 6-18 shows top-level block diagram of the SAW-less receiver implemented in CMOS 28nm with its chip micrograph. The RX is digitally programmable to work in either 4x or 8x sampling modes. In the 8x sampling mode, mixers are clocked with 8-phase 12.5% non-overlapped clocks. This enables the 8/16-phase CS-BPF to distinguish between 1^{st} and $3^{rd}/5^{th}$ harmonic after downconversion to IF by the mixer. Using also a harmonic recombination gm-stage in this receiver, provides a total RX $3^{rd}/5^{th}$ harmonic rejection of > 58 dB. Thanks to the sharp filtering at IF, the receiver has a maximum +14 dBm IIP3. Table 6-2 summarizes performances of this receiver and compares with other state-of-the-arts.



(a)



(b)

Figure 6-18: (a) Top-level block diagram of the proposed SAW-less DT superheterodyne receiver, with (b) its chip micrograph.

6.7 Conclusion

A complete chain of a fully-integrated discrete-time (DT) superheterodyne receiver with high reconfigurability for cellular and wireless applications is described. Using the proposed DT band-pass filtering (BPF), IF filters of high center frequency are also integrated on chip. In addition to the insensitivity to flicker noise and time-varying DC offsets, superheterodyne shows an extremely high IIP2 without requiring any calibration. This characteristic makes this architecture a suitable candidate for future SAW-less receivers that work in the toughest FDD mode. DT signal processing using passive switched-capacitor circuits makes this receiver process scalable. It only uses switches, capacitors, and inverter-based gm-cells. The use of a

Table 6-2: Performance summary and comparison with state-of-the-arts.

	[64] This Work	[14] TUDelft	[7] Broadcom	[20] IMEC	[72] Broadcom	[70] UPavia	[71] MediaTek
Technology	28nm	65nm	65nm	28nm	28nm	40nm	40nm
Architecture	**High-IF**	High-IF	High-IF	ZIF	ZIF	ZIF	ZIF
NF (dB)	2.1/2.2/2.6	2.9–4.0	2.8	1.8–3	1.7	3.8/1.9	1.7–2.4
Supply (V)	0.9	1.2/2	1.2/2.5	0.9	1.0	1.2/1.8	1.5
HR (dB)	**> 58***	N/A	N/A	50(70$)	60/60	54/65	N/A
IIP3 (dBm)	14(OB)	-5(IB)	-6.3(OB)	8/5	11.5(OB)	18/16(OB)	0.4(OB)
IIP2 (dBm)	**Infinite**	95¥	N/A	55(88$)	55	64	55
Power (mW)	**24 – 37**	48–79	≈ 39	40/35	36 – 62	32/32	39 – 46.5
Area (mm^2)	**0.52**	1.1	0.76	0.6	5.2	0.84/0.74	0.57

* Worst-case without calibration $ with calibration ¥ Due to an IF Mixer

high-order, but very low-power and low-noise baseband DT filters, reduces the required ADC sample rate and dynamic range thus leading to a lower total power consumption.

In an extension to a SAW-less DT superheterodyne receiver, higher-order and quality CS-BPF are used to reach to a very high IIP3. As experimentally verified, this new receiver shows an infinitely high IIP2.

Part II:
Fully Integrated Oscillator Design in Nano-Scale CMOS

Chapter 7

High-Swing Class-C Oscillator

Today's design and implementation of building blocks for high-frequency communication links in nano-scale CMOS technologies are ever more challenging. One of these challenges is to comply with the imposed low supply voltage of a digital portion of RFICs or RF-SoCs. In a fully integrated transmitter/receiver, at least one oscillator (see Figure 1-3) needs to be integrated to be used in frequency synthesizer. Designed in nano-scale CMOS, phase noise of oscillators degrades due to the reduced supply voltage and output swing.

The aim of this work is to utilize the provided supply voltage as efficiently as possible in order to generate the highest output swing. Based on Leeson's phase noise equation [74], increasing the oscillation amplitude by only 41% reduces the output phase noise by 3 dB. Typically, stacked transistors (i.e., tail current source, cascade amplifier, etc.) consume the precious voltage headroom, which is the reason they are avoided in this work.

In this chapter, after describing the basic operation of a class-C oscillator in light of the low phase noise goal, the proposed low-voltage high-swing class-C (HSCC) oscillator is introduced. Then implementation details of a low-power low-phase-noise test chip in CMOS 90-nm are discussed and measurement results are presented. The same idea of the HSCC oscillator is extended to an ultra-low phase noise dual-core oscillator that, for the first time ever in fully integrated silicon, meets phase noise requirements of the GSM normal BTS receiver standard.

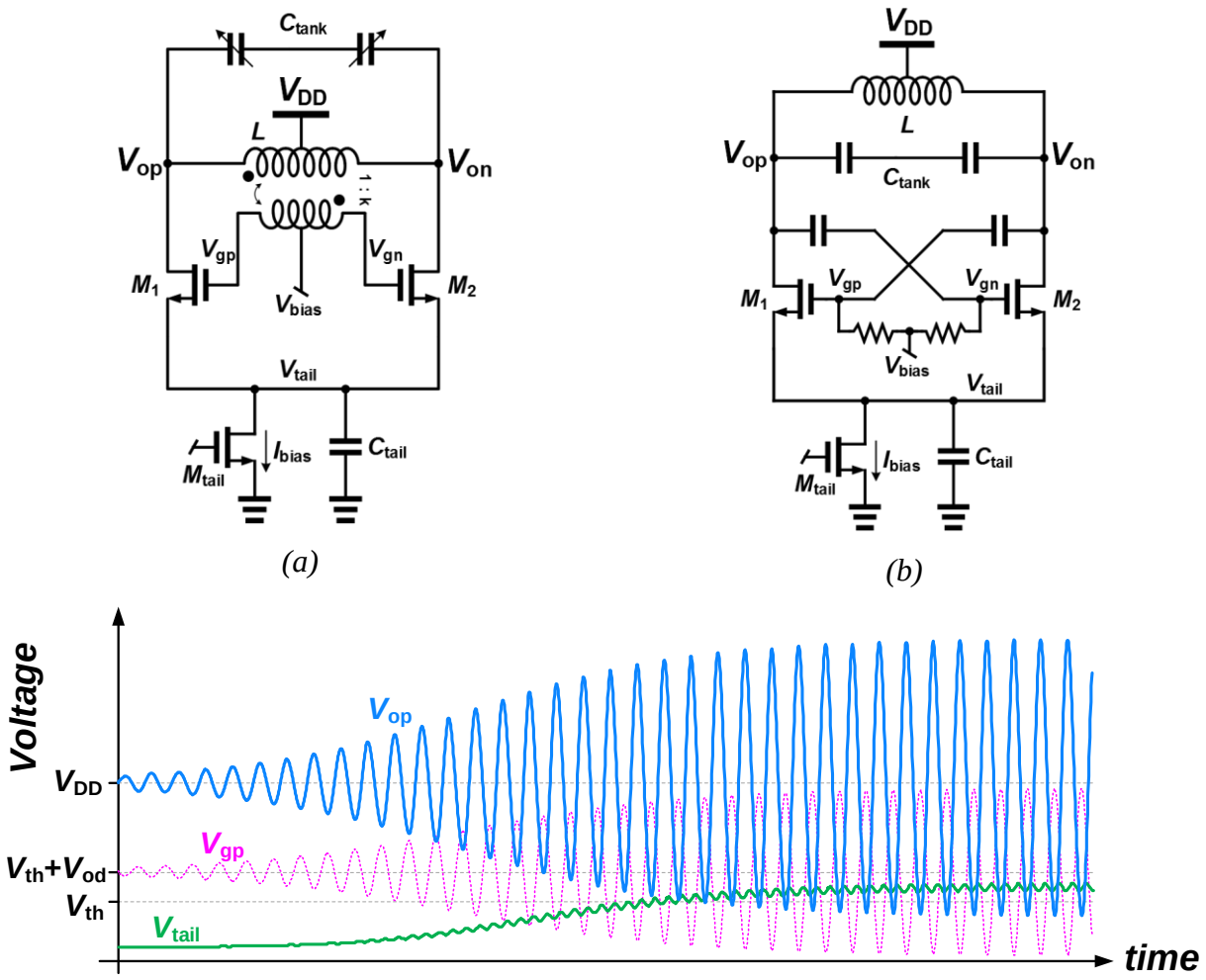


Figure 7-1: Schematic of the original class-C (OCC) oscillator [75] *(a) with transformer bias, and (b) with RC bias. (c) Transient waveforms of the oscillator during startup.*

7.1 Class-C Harmonic Oscillator

A state-of-the-art yet simple class-C oscillator is shown in Figure 7-1(a) and (b) [75]. Here, it is called original class-C (OCC) oscillator. This oscillator is very similar to the conventional cross-coupled LC oscillator, but with a relatively big capacitor (C_{tail}) on the tail node (V_{tail}) and separated DC bias voltage (V_{bias}) of the transistors gates. The tail capacitor is responsible to suppress high frequency fluctuations of V_{tail}. Therefore, V_{tail} is able only to change slowly in presence of C_{tail}. Transformer bias (Figure 7-1(a)) and RC bias (Figure 7-1(b)) are used in two implementations to set the DC bias [75].

Figure 7-1(c) shows transient voltage waveforms of this oscillator. At first, V_{tail} is about zero (or one MOS overdrive voltage, V_{od}) and $V_{gs1,2}$ are equal to V_{bias}. As the oscillation amplitude

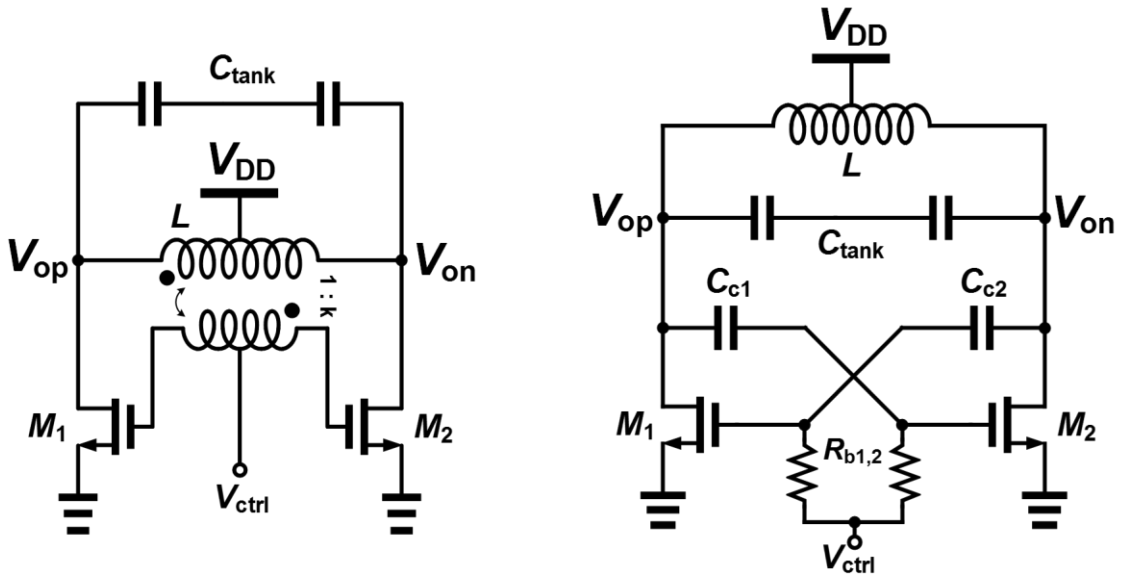
increases, because of non-linear operation of M_1 and M_2, their average currents increase. Therefore, C_{tail} is charged and V_{tail} increases. Consequently, DC bias voltage of $V_{gs1,2}$ gradually reduces. Tail voltage increase continues to a voltage in which $M_{1,2}$ and M_{tail} DC currents are balanced again. Since V_{tail} high frequency variations are damped by C_{tail} (see Figure 7-1), and the oscillation amplitude is determined by the tail bias current, and size of $M_{1,2}$ sets the firing angle at steady-state; the larger transistor width, the lower the firing angle.

In the OCC oscillator, generated noise level of the LC tank loss and switching transistors are the same as in conventional cross-coupled differential oscillator [76]. However, the total output phase noise is reduced due to the higher oscillation amplitude at the same bias current. In class-C oscillators, transistor currents are impulse-like which results in a larger fundamental harmonic compared to cross-coupled configuration in which currents are square-waves shape in time [75]. Moreover, noise contribution of tail current source is suppressed, which is one of substantial noise sources in conventional LC tank oscillators [77].

7.2 Proposed High-Swing Class-C Oscillator

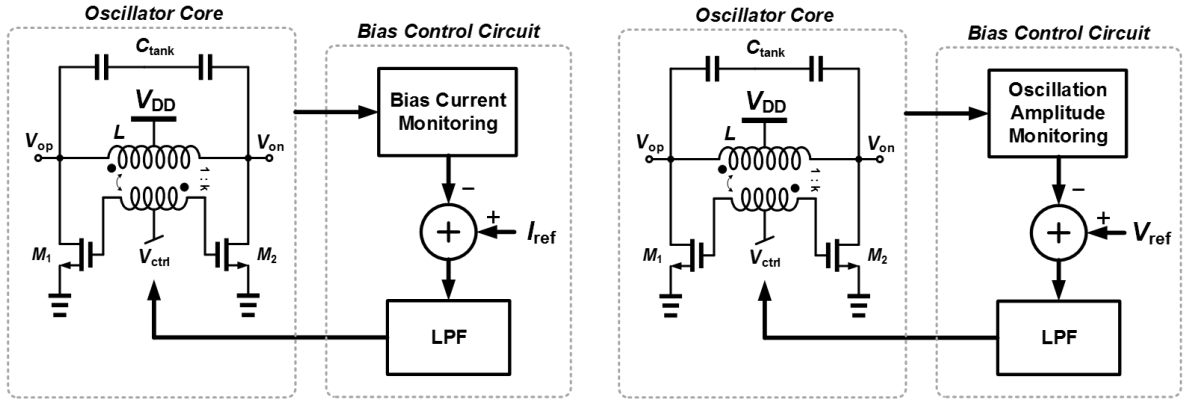
In order to provide the highest voltage headroom for the output swing, the tail current source of OCC oscillator is removed in the present work [78]. The outputs are also fed back to switching transistors, $M_{1,2}$, by means of a transformer or RC bias. In this way, the input DC bias of these transistors is decoupled from the DC of output nodes (V_o), i.e., V_{DD} voltage in conventional LC oscillators. Hence, it allows a higher output swing before transistors enter the triode region. The high-swing class-C (HSCC) oscillator core circuit is depicted in Figure 7-2(a) and (b). The output swing on each side of this circuit can be as high as $V_{DD}-V_{od}$ (peak), where V_{od} is the overdrive voltage of the switching transistors. As a consequence, the minimum output phase noise of this oscillator is reduced, or it can work with lower supply voltages at the same output swing.

The present oscillator requires an additional circuit to work properly, a bias control circuit. This circuit has various tasks: first, it should guarantee a safe startup at the beginning of oscillation. Second, it should be able to set a current consumption of the oscillator core and, accordingly, its oscillation amplitude. In this way, it reduces supply voltage sensitivity as well. At the system level, this circuit can be implemented in two ways: 1) sensing the bias current of the oscillator core, comparing it with a reference (I_{ref}), and then feeding it back to an input control



(a) *(b)*

Figure 7-2: Proposed high-swing class-C (HSCC) core (a) with transformer bias, and (b) with RC bias.



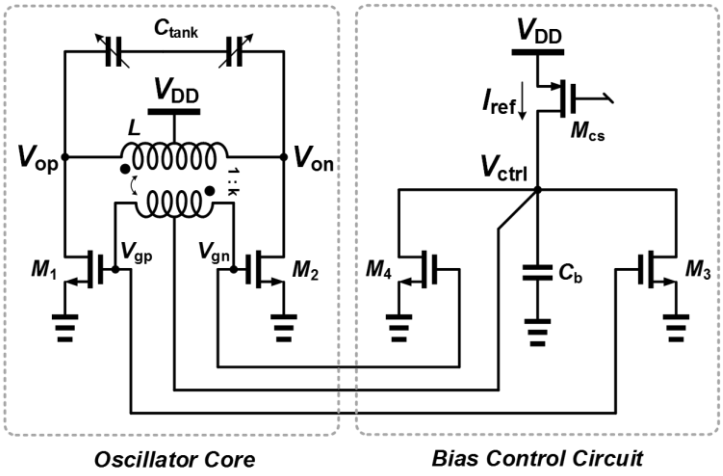
(a) *(b)*

Figure 7-3: Bias control circuit using (a) core bias current, and (b) oscillation amplitude monitoring.

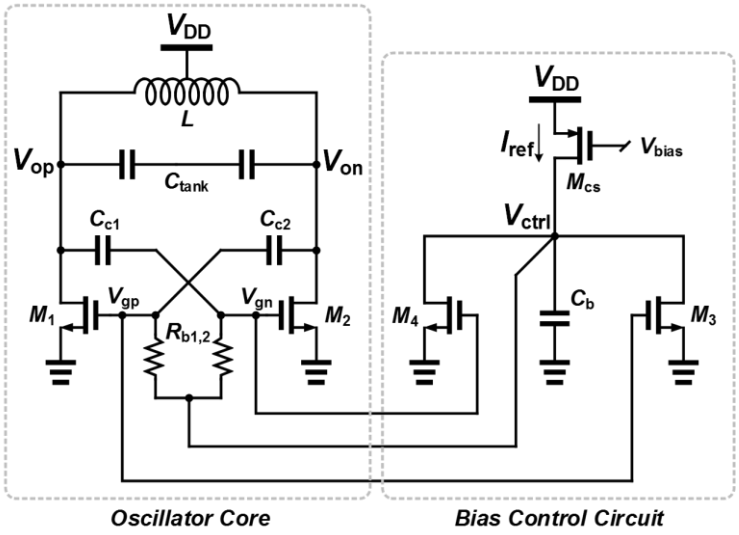
of the core [78], as shown in Figure 7-3(a). 2) Sensing the oscillation amplitude, comparing it with a reference (V_{ref}), and then feeding it back to an input control of the core, as shown Figure 7-3(b). Ref. [79] implements the amplitude monitoring system.

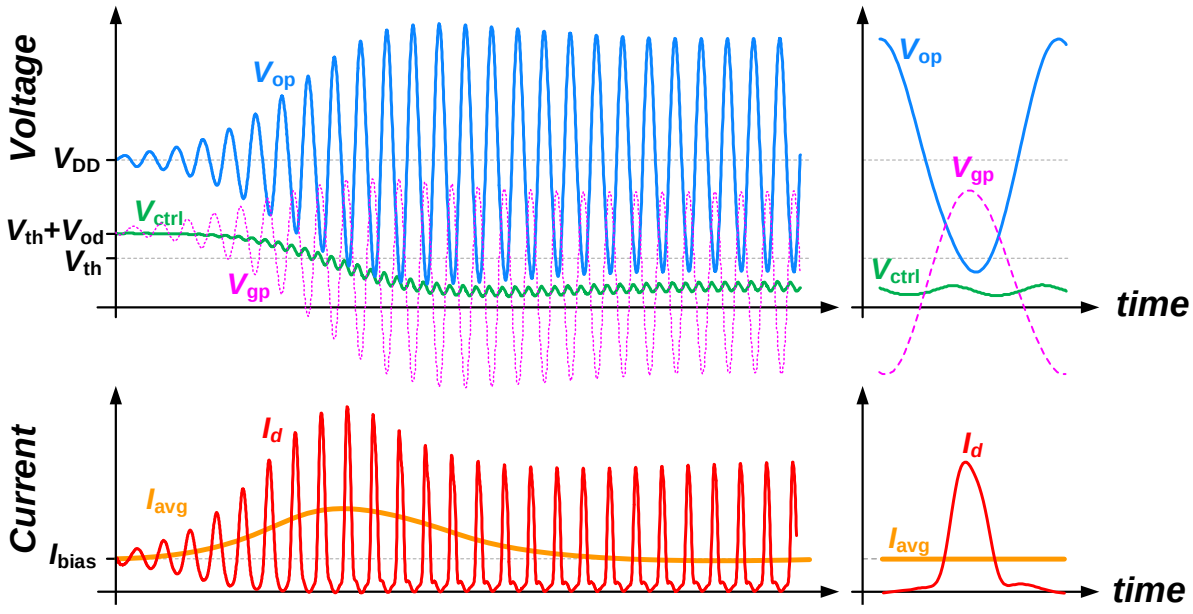
The proposed bias control circuit [78] uses the core bias monitoring scheme. As drawn in Figure 7-4(a) [78] and Figure 7-4(b) [80]–[82], M_3 and M_4 mirror the currents of M_1 and M_2, respectively. These currents are summed at V_{ctrl} node. Their sum is proportional to the current of the oscillator core. It is then compared with a reference current, I_{ref}. The bypass capacitor

(a)



(b)





(c)

Figure 7-4: Complete schematic of the proposed high-swing class-C oscillator with (a) transformer bias, and (b) with RC bias. (c) Transient waveforms during startup.

C_b integrates the current difference and converts it to V_{ctrl}. This integrator acts as a low-pass filter. V_{ctrl} is fed back to the oscillator core. This forms a negative feedback loop. In steady-state, the total DC current of the core is I_{ref} multiplied by the mirror ratio. Hence, the power consumption and the oscillation amplitude can be controlled by adjusting I_{ref}. The proposed control circuit avoids an external bias voltage, V_{bias}, which is necessary for OCC oscillator.

Waveforms of this oscillator are shown in Figure 7-4(c). At the beginning, suppose the oscillation is not started yet. In this condition, the secondary of the transformer is short-circuited in Figure 7-4(a), thus $M_{3,4}$ are diode connected. Since $V_{g1,2}$ are equal to V_{ctrl} (transistor threshold voltage plus overdrive voltage, $V_{th} + V_{od}$), I_{ref} is mirrored into M_1 and M_2. If this current satisfies the oscillation condition, the oscillator core starts to oscillate. As the oscillation amplitude increases, average currents of $M_{1,2,}$ and consequently $M_{3,4,}$ are increased (depicted at the bottom of Figure 7-4(c)). The excess current of $M_{3,4}$ is integrated into C_b which then reduces V_{ctrl}. In steady-state, again the average current of $M_{3,4}$ will decrease to I_{ref}. A larger switching pair width at the same bias current decreases V_{ctrl} and firing angle. By a proper choice of $M_{1,2}$ sizes, V_{ctrl} would be set to a small V_{od} at steady-state, resulting in the maximum possible tank swing. Similar process happens also for the RC bias oscillator in Figure 7-4(b).

7.2.1 Output Swing

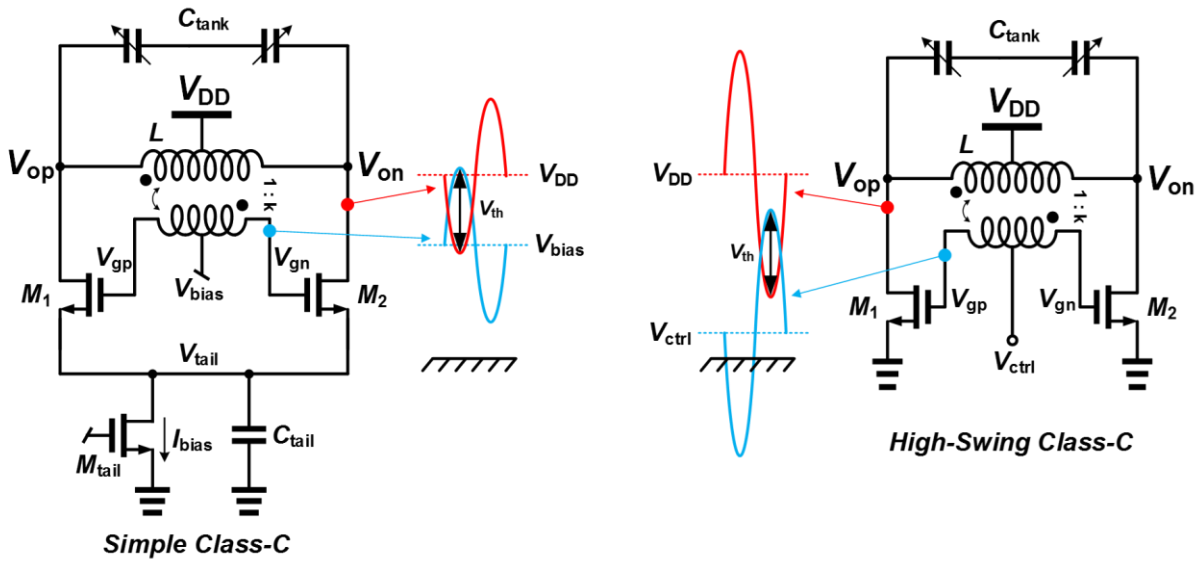
The maximum single-ended peak oscillation swing of OCC oscillator in Figure 7-5(a) is achieved when $M_{1,2}$ are just starting to enter the triode region. Equating $V_{gd1,2}$ with V_{th}, we have:

$$\begin{aligned} V_{gd} &= V_g - V_d = \left(V_{bias} + k \cdot A_{m,SCC}\right) - \left(V_{DD} - A_{m,SCC}\right) = V_{th} \\ &\Rightarrow A_{m,SCC} = \frac{V_{DD} - V_{bias} + V_{th}}{k+1}. \end{aligned} \tag{7.1}$$

in which k is the transformer voltage gain in the transformer biasing configuration, or capacitive voltage ratio from the outputs to the transistor gates. A safe startup condition can be guaranteed with $V_{bias} > V_{th} + V_{od}$ (V_{bias} however, can be reduced shortly afterwards). So the maximum swing is:

$$A_{m,SCC} = \frac{V_{DD} - V_{od}}{k+1}. \tag{7.2}$$

In [83] a feedback loop is used that lowers V_{bias} after the startup. In that design, a higher maximum swing can be achieved.



(a) *(b)*

Figure 7-5: Maximum oscillation swing comparison of (a) original class-C, and (b) high-swing class-C oscillators.

Following the same derivation, the maximum output swing of the proposed HSCC oscillator is:

$$A_{m,HSCC} = \frac{V_{DD} - V_{ctrl} + V_{th}}{k+1}. \tag{7.3}$$

In a well-designed oscillator, V_{ctrl} would be as low as a small V_{od} (although $M_{3,4}$ may barely enter the triode region, this does not affect phase noise performance of the oscillator core). Comparing (7.2) and (7.3), the output swing has been improved by V_{th} / (k+1) which is worthwhile in a low voltage design. Assuming V_{DD} = 0.6 V and k = 0.9 in this design and a low V_{od} in OCC oscillator, the maximum swing predicted by (7.2) is 290 mV. This is for a V_{DD} clipping limitation of 600 mV in this low-voltage example. However, the maximum swing predicted by (7.3) in the HSCC oscillator increases to 470 mV, assuming V_{ctrl} = 150 mV and V_{th} = 450 mV. This swing almost reaches the V_{DD} clipping limitation.

7.2.2 Phase Noise

Since both HSCC and OCC oscillators use the same core structure, the phase noise expression of OCC can be used here. The two class-C oscillators with a bias current I_{bias} at an offset frequency $\Delta\omega$ from the carrier have a phase noise of:

$$L(\Delta\omega) = 10 \cdot \log\left(\frac{k_B T}{2\Delta\omega^2 C^2 I_{bias}^2 R^2} \left(\frac{1}{R} + \frac{\gamma}{k} \frac{1}{R} \right) \right). \quad (7.4)$$

where k_B is Boltzmann's constant, T the absolute temperature, γ the MOS channel noise factor, C the tank capacitance, and R the equivalent parallel tank resistance [75]. All current noises of the bias control circuit are filtered by C_b at V_{ctrl} node. Hence, in (7.4) noise of the tank resistance and $M_{1,2}$ are considered while the other noise sources of the circuit are negligible. Inside the inner parenthesis in (7.4), $1/R$ and $\gamma/(k \cdot R)$ are the noise contributions of tank loss and switching pair, respectively.

Due to the higher maximum swing of the proposed oscillator, I_{bias} would be increased more without forcing $M_{1,2}$ into the triode region. It can be shown that phase noise performance figure-of-merit (FoM) [84] is proportional to I_{bias} for output amplitudes lower than the maximum swing. As a result the minimum output phase noise is reduced. Phase-noise figure-of-merit (FoM) of an oscillator can be written as [80]:

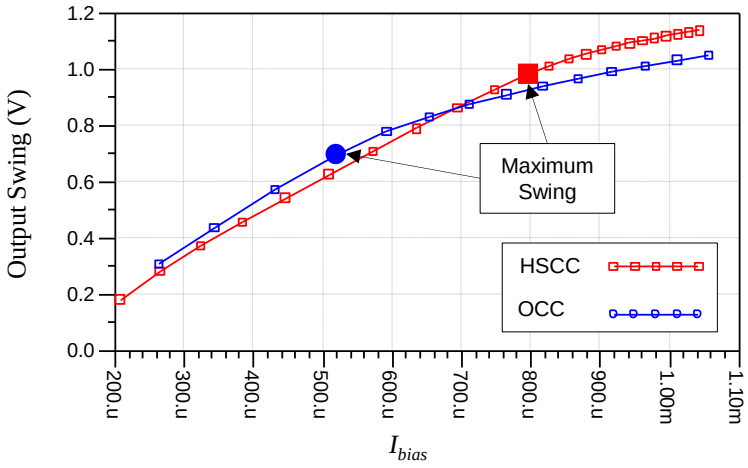
$$\text{FoM} = \frac{4Q^2 \cdot \alpha}{F \cdot 4kT} \times \frac{V_0}{V_{DD}} \times 10^{-3}, \quad (7.5)$$

where, Q is the tank quality factor, α is a bias current conversion factor into the fundamental current harmonic, and V_0 is a differential oscillation amplitude. In this equation, noise factor F is a constant, which depends on oscillator topology and its parameters. This parameter is the same for both OCC and HSCC oscillators. Based on (7.5), a higher swing ($V_0=2A_m$) also leads to a better FoM. Using an example at the end of Section 7.2.1 , HSCC oscillator has a 2 dB better maximum FoM than does the OCC oscillator, with the same circuit elements.

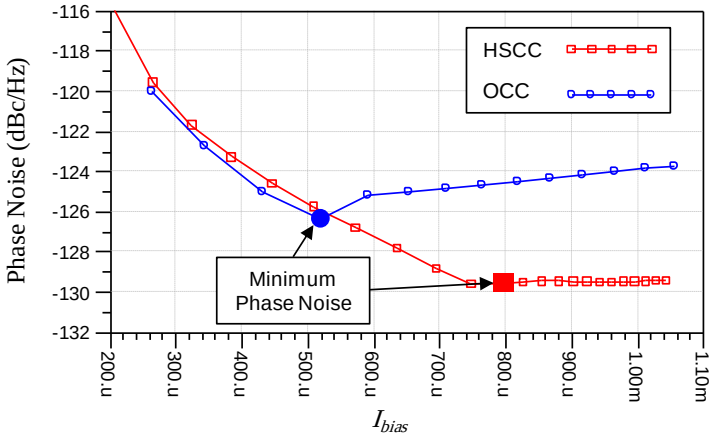
7.2.3 Comparison

The two oscillators, HSCC and OCC, are simulated to compare their output swings and phase noise performances (Figure 7-6). In this simulation, V_{DD}, V_{th} and k are 0.6V, 0.45V and 0.9 respectively.

By increasing bias current of the oscillators, their oscillation amplitudes increase gradually, hence lowering the output phase noise. This trend continues to a point at which the switching pairs are entering the triode region. Since the output phase noise degrades with further increases in the bias current as we enter the triode region, we call the oscillation amplitude of this point



(a)



(b)

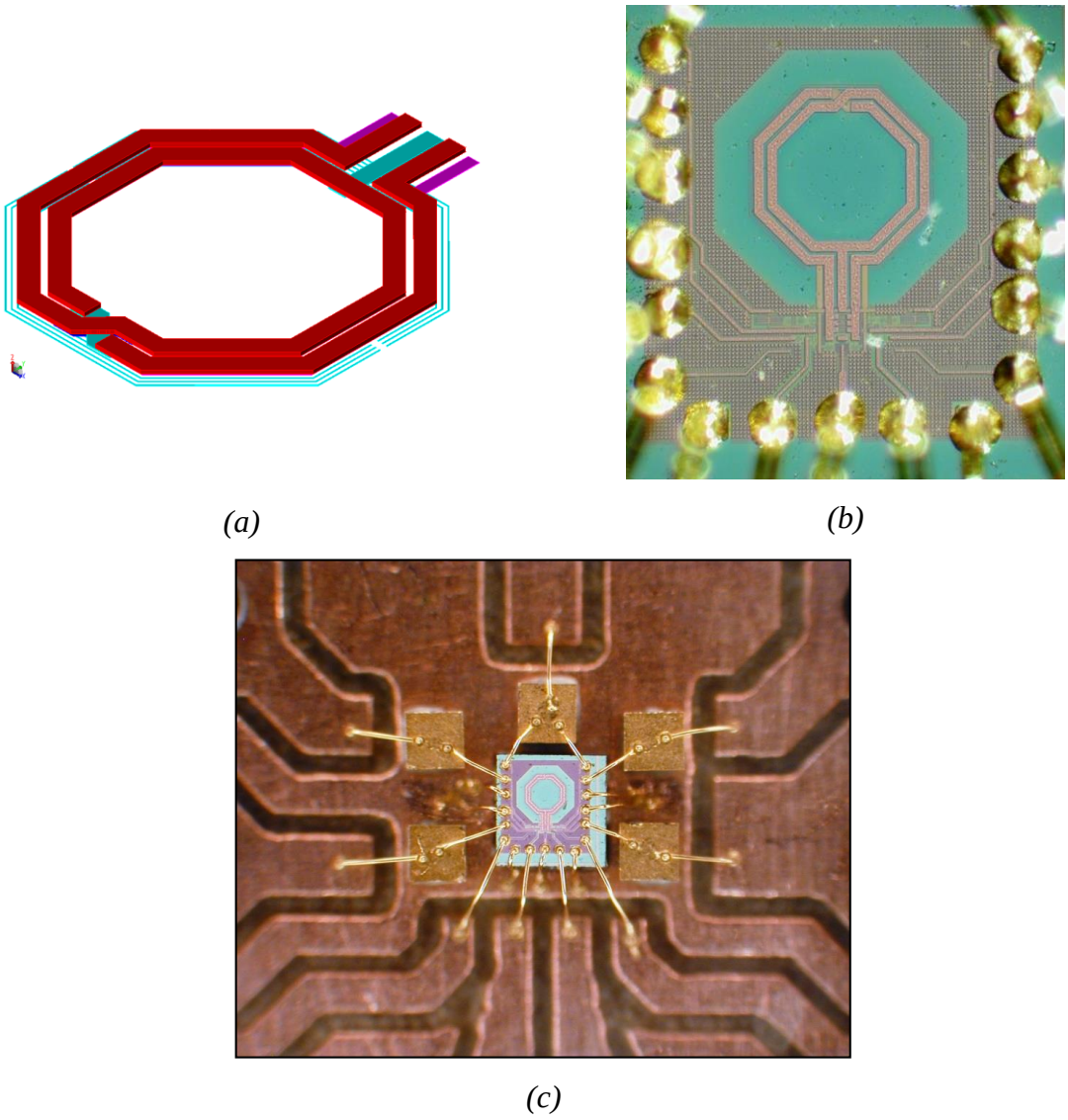
Figure 7-6: (a) Differential peak output swing at V_{DD}=0.6 V and (b) phase noise (at 3MHz offset from 5.5GHz carrier) of HSCC and OCC oscillators versus total current consumption.

"the maximum usable swing" at the region change boundary. Although the oscillation amplitude is still increasing after this point, its slope is decreased due to the region change boundary. As depicted in Figure 7-6, it is clear that the maximum output swing of the HSCC is higher than of the OCC oscillator. Although its output phase noise is a bit more than OCC for low bias currents (due to the overhead current of the control circuit), it has a lower minimum phase noise.

7.3 Implementation

The HSCC oscillator is implemented in 1P9M 90nm CMOS process with ultra-thick metal (UTM) option. In this design, the transformer bias structure in Figure 7-4(a) is implemented.

The transformer used in this oscillator consists of primary and secondary windings, both containing a center tap. The primary winding is a 2-turn coil on Metal9 (UTM) with an average



(a) *(b)*

(c)

Figure 7-7: Chip micrograph of the HSCC oscillator.

radius of 115µm and track width of 15µm. The secondary winding is also a 2-turn, but 10µm width coil on Metal7 with an outer radius is the same as the primary coil. An objective was to maximize magnetic coupling between the two coils while reducing their capacitive coupling. Floating patterned shielding [85] is used beneath this transformer on Metal5 to both isolate it from substrate and to improve its quality factor. Figure 7-7(a) shows a 3D view of the transformer. Electromagnetic simulations show that the voltage gain of the transformer is equal to $k = 0.9$ and differential inductance of the primary coil is 2.4 nH.

Although a lower k in (7.3) increases the output swing, based on (7.4) it increases the phase noise contribution of the switching pair as well. Assuming γ of about 1 for $M_{1,2}$ (at switching times, drain–source voltages of $M_{1,2}$ are small enough and these transistors follow the long-

channel noise regime [1]) the selected *k* balances the phase noise contribution of tank loss and switching pair.

In order to maintain the high quality factor of the primary inductor, tank capacitance is provided by combination of MOM capacitors and A-MOS varactors.

In the proposed oscillator, control circuit mirrors the core current with a 1/5 ratio as to not impose a high overhead on the total power consumption. Going to lower ratios would make the oscillator prone to instability in amplitude (squegging) [86].

7.4 Measurement Results

To isolate the oscillator core from measurement equipment, the outputs of the oscillator are buffered using two common-source amplifiers with 50 Ω resistor loads and a separate supply voltage.

Figure 7-7(b) shows the chip micrograph of HSCC oscillator. The chip is directly wire bonded to a PCB, shown in Figure 7-7(c). For characterizing the oscillator, R&S®FSUP50 Signal Source Analyzer is used. To improve accuracy of the measurements, "PLL Method" with a bandwidth of 30kHz combined with XCorr option is used in this tool.

The oscillator operates at a nominal voltage of 0.6 V oscillating at 5.1 GHz with 131 MHz tuning range. For a bias current of 1.44 mA (including the bias control circuit, but excluding buffers), the oscillation amplitude across the tank almost reaches the maximum swing. The output phase noise spectrum of the oscillator is shown in Figure 7-8. The measured phase noise is as low as -127 dBc/Hz at 3 MHz offset frequency.

Phase noise performance of the HSCC oscillator is now compared with some related works in Table 7-1. HSCC has a performance comparable to [75]. Although the OCC implementation in [75] has a better FoM than the implemented HSCC oscillator, this is due to different circuit components and the process technology. As proved by simulations in Figure 7-6, the HSCC has better maximum FoM than OCC when the same circuit components and process are used. The original class-C oscillator with a feedback [83] has a comparable FoM. In [86] a complementary HSCC is proposed that has also a similar FoM. Ref. [77] reaches an excellent phase noise and FoM because of both noise filtering of the tail current source and a high supply voltage (generally a better phase noise is achievable with a higher supply voltage).

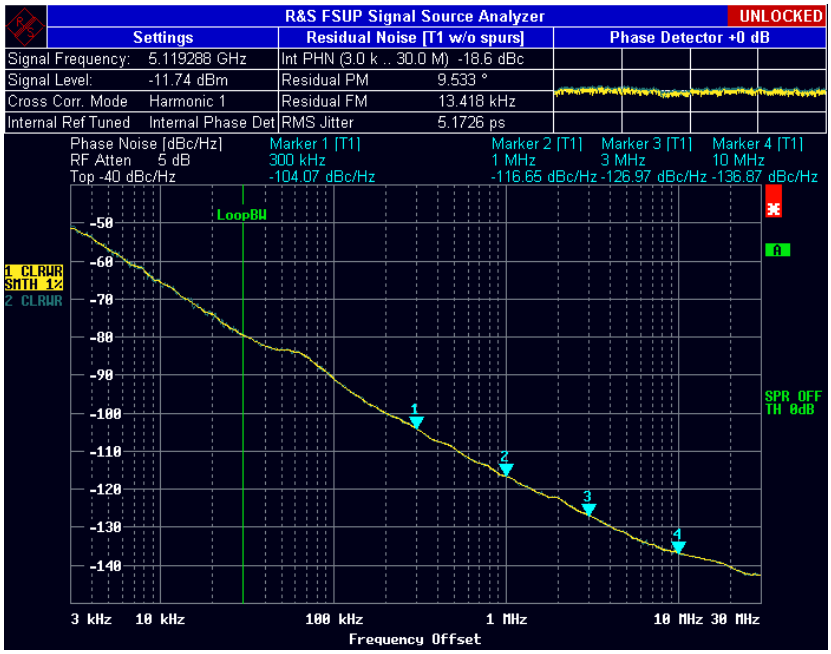


Figure 7-8: Phase noise spectrum of the HSCC oscillator at 5.12GHz.

Table 7-1: Comparison of HSCC with state-of-the-art CMOS oscillators.

Work	Freq. (GHz)	V_{DD} (V)	P_{diss} (mW)	PNosie (dBc/Hz)	Freq. Offset (MHz)	FoM (dB)	Tech.
HSCC [78] ESSCIRC'11	5.1	0.6	0.86	-127	3	192.3	90 nm
OCC [75] JSSC'08	5.2	1.0	1.4	-131.5	3	194.5	0.13 µm
OCC with FB [83] JSSC'13	3.97	1.2	6.6	-147.5	10	191	90 nm
Comp. HSCC [86] ESSCIRC'13	4.4	1.2	2.2	-124	2	191.5	90 nm
[77] JSSC'01	1.2	2.5	9.25	-153	3	195.4	0.35 µm
[79] JSSC'13	4.84	1.2	3.4	-125	1	193	0.18 µm
[87] JSSC'05	3.8	0.5	0.57	-119	1	193	0.18 µm
[88] AICSP'06	1.562	0.6	1.56	-122	1	183.9	90 nm
[89] TMTT'07	5.6	0.6	3	-118	1	189	0.18 µm
[89] TMTT'07	5.6	0.4	1.1	-114	1	189	0.18 µm

7.5 Extension to Ultra-Low Phase-Noise Performance

Certain cellular transmitter/receiver (TX/RX) oscillators require extremely low phase noise for up-/down-conversion of modulating signals. For example, TX oscillator in GSM900 mobile

station (MS) standard should have a phase noise better than -162 dBc/Hz at 20 MHz offset from the 915 MHz carrier. Likewise, the RX oscillator must satisfy the toughest phase noise requirements imposed by the GSM900 normal basestation (BTS) specification, which is better than -147 dBc/Hz at 800 kHz offset from 915 MHz carrier.

Nowadays, this BTS RX phase noise requirement is achieved using expensive SiGe/GaAs ICs or with assistance of high quality discrete components. A fully-integrated oscillator in bulk CMOS meeting this stringent requirement has not been demonstrated before in the literature.

The idea of HSCC oscillator is used here to reach to such a stringent phase noise requirement. To achieve this, the following steps are done [80], [90]:

- Maximum allowed V_{DD} of the process is used. Since thick-oxide devices in a CMOS process tolerates a higher supply voltage, these devices are used in the implementation.
- Oscillation amplitude is maximized by using the maximum bias current just before entering oscillator in voltage limited regime [91]. In this way, the minimum phase noise of a structure is obtained.
- For a given oscillation frequency, inductance value of the LC tank is minimized (by using 1-turn inductor) to reduce equivalent parallel resistance of the tank. Consequently, phase noise is reduced at the cost of spending more current consumption for the same maximum oscillation amplitude. Note that, Q of the tank needs also to be kept high for a good power/phase-noise efficiency.
- The high-swing class-C oscillator structure is used for achieve the maximum possible oscillation amplitude.
- Finally, to further reduce phase noise, we propose use of multi-oscillator cores in parallel [80]. Phase noise is reduced by $1/N$ in an N-core oscillator.

Figure 7-9 shows the proposed dual-core HSCC oscillator. The use of 2 cores in parallel reduces phase noise by 3 dB while increases power consumption 2 times. Therefore, phase noise FoM is remained unchanged. Implementation details of this oscillators is discussed in [80]. Figure 7-10 shows chip micrograph of this oscillator.

Table 7-2 summarizes measured performance of this oscillator and compares it with state-of-the-art ultra-low phase noise oscillators. As measured phase noise is depicted in Figure 7-11, this oscillator is meeting phase noise the toughest standard GSM900 Normal BTS RX requirement for the first time in fully integrated CMOS.

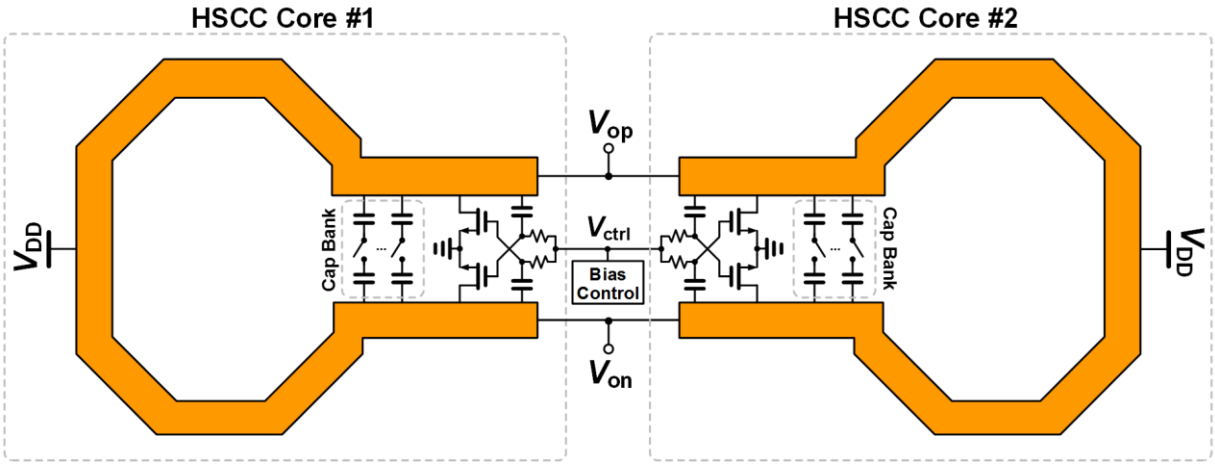


Figure 7-9: Dual-core high-swing class-C oscillator.

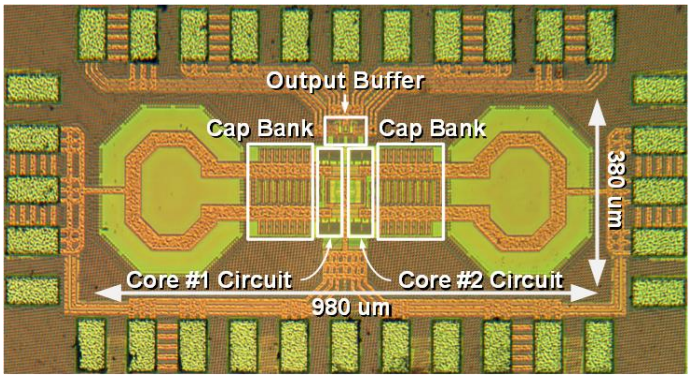


Figure 7-10: Chip micrograph of the dual-core HSCC oscillator.

Table 7-2: Performance summary and comparison with ultra-low phase noise oscillators.

		This Work	JSSC'13 [92]	ISSCC'12 [93]	ISSCC12 [94]	RFIC07 [95]	JSSC06 [96]
Description		**Dual-Core Class-C**	**Class-F**	**Clip & Restore**	**ClassB/C**	**Colpitts**	**ClassB**
Technology		**65nm**	**65nm**	**65nm**	**55nm**	**130nm**	**90nm**
Tuning Range (GHz)		**4.07-4.91 (18.6%)**	**2.94-3.78 (25%)***	**3.64-4.03 (10.2%)***	**3.35-4.6 (31.44%)***	**1.5-1.65 (9.6%)**	**3.21-4.1 (24.3%)**
Frequency (GHz)		**4.07**	**3.7**	**3.92**	**3.35**	**1.56**	**0.915**
Phase Noise (dBc/Hz)	**3MHz**	**-146.7**	**-142.2**	**-141.71**	**-142**	**-150.38**	**-149**
	20MHz	**-163.1**	**-158.6**	**-158.18**	**-158.48**	**-166.85**	**-167**
Phase Noise norm. to a 915MHz carrier (dBc/Hz)	**3MHz**	**-159.7**	**-154.3**	**-154.35**	**-153.3**	**-155.02**	**-149**
	20MHz	**-176.14**	**-170.7**	**-170.8**	**-169.75**	**-171.49**	**-167**
Supply Voltage (V)		**2.15**	**1.25**	**1.2**	**1.5**	**3.3**	**1.4**
Current (mA)		**59**	**12**	**21.5**	**18**	**88**	**18**
FoM @ 3MHz (dB)		**189**	**192.2**	**189.9**	**189**	**180**	**184.6**

**** After division by 2***

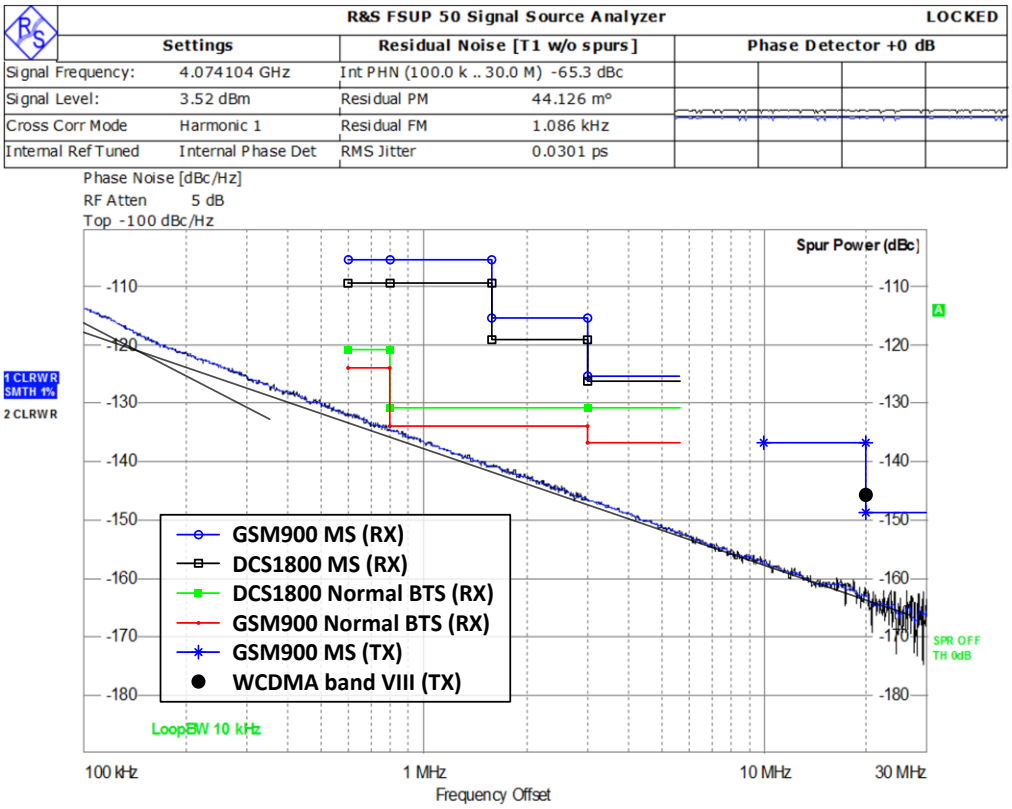


Figure 7-11: Measured phase noises at 4.07 GHz. Mask specifications are normalized to the carrier frequency.

7.6 Conclusion

A modified class-C oscillator which has a higher output swing is proposed. The higher swing is owed to the removed tail current source of the oscillator core and use of a transformer/RC to decuple bias of the switching pair from the output. A bias control circuit guarantees a reliable startup and adjusts bias of the switching pair for the desired power consumption. A low-power/ low-voltage test chip of this oscillator is implemented in 90-nm CMOS. As a whole, it can achieve good phase noise performance with better FoM than the original class-C oscillator, especially at low supply voltages.

The idea of high-swing class-C oscillator is further extended to an ultra-low phase noise dual-core oscillator implemented in CMOS 65nm. This oscillator, for the first time ever, meets the phase noise requirements of GSM normal BTS receiver standard in a fully integrated CMOS chip. This innovation has made possible CMOS implementations of fully integrated BTS receivers.

Chapter 8

Low-Phase-Noise Oscillator Using Series LC Tank

Oscillators are essential building blocks in almost every SoC. For low-cost applications with relaxed performance specifications, conventional inverter-based ring oscillator (RO) structures [97]–[101] have traditionally been used. This is thanks to their small silicon area and a wide frequency tuning range (at least an octave). However, the lack of a resonator causes poor phase noise (PN) and high power consumption. On the other hand, LC-tank oscillators are predominant for high-performance applications. Though providing low PN, they normally occupy a large area and have a limited tuning range.

In this chapter, a novel *quadrature* oscillator with four *series* LC tanks arranged in a ring structure is proposed [102]. By using tiny inductors with a low quality factor (*Q*), it features excellent PN while occupying as little area as the conventional ROs and providing a very wide tuning range of nearly an octave. Simple digital-like inverters are used as amplifiers. In this way, transistor stacking is avoided and the oscillator is able to work in the low supply voltages of nano-scale CMOS.

8.1 Quadrature Series LC Tank Oscillator

8.1.1 Oscillator Core

A series LC tank driven by a voltage source is shown in Figure 8-1(a). As per Bode plot in

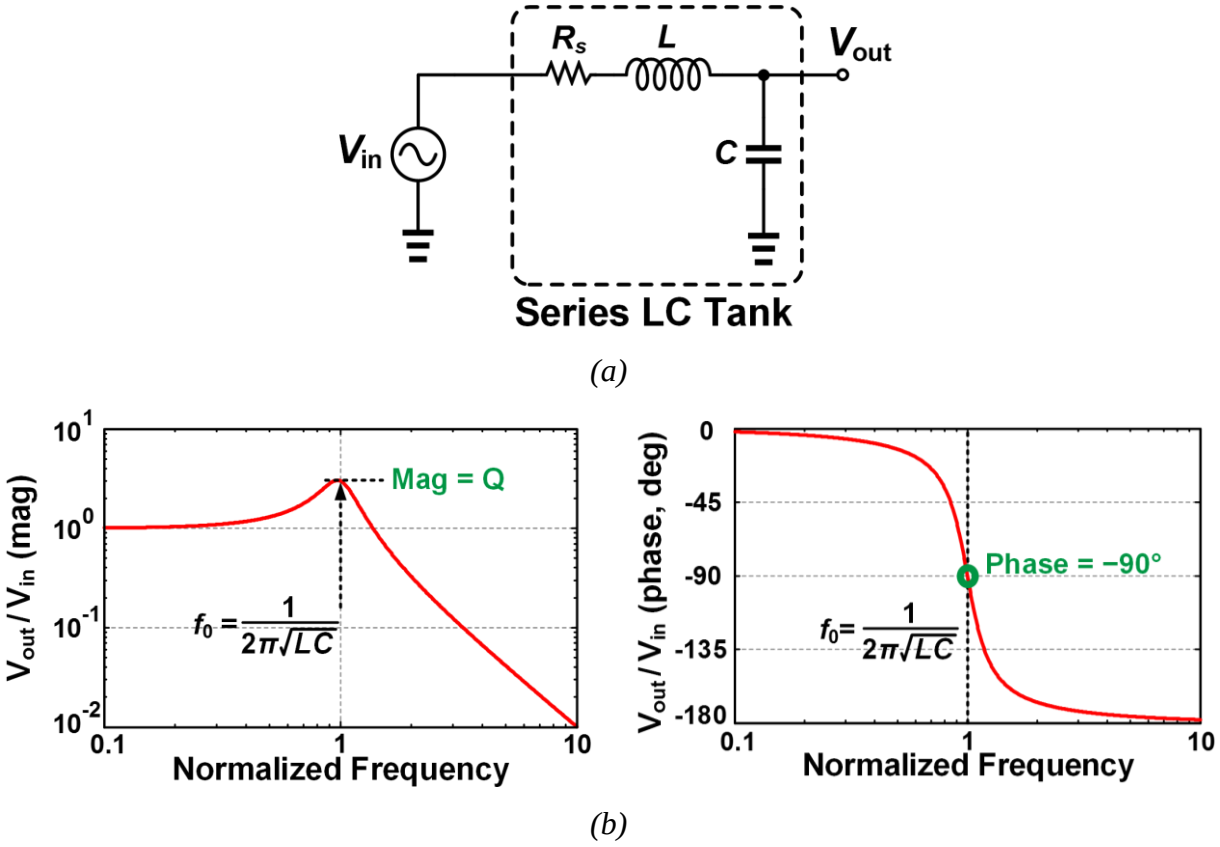


Figure 8-1: (a) Series LC tank as a 90º phase shifter with (b) its frequency response.

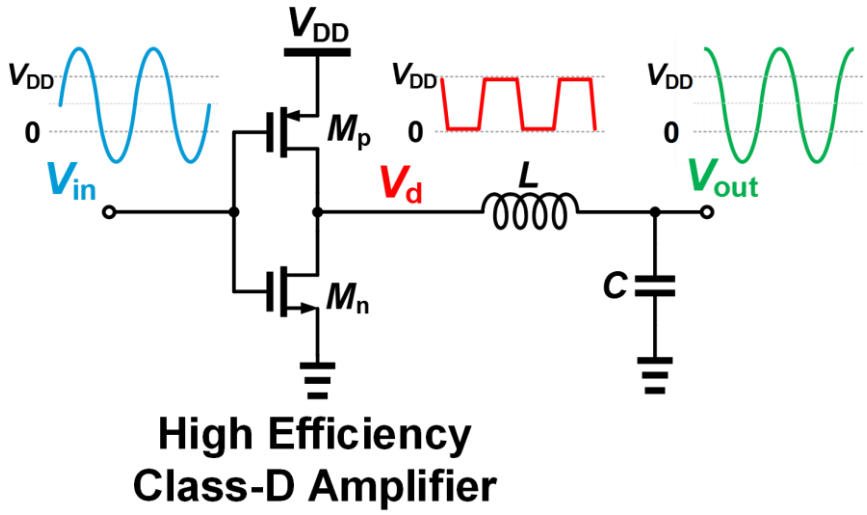


Figure 8-2: Class-D amplifier as a low output impedance driver of series LC tank.

Figure 8-1(b), the tank's output voltage is amplified Q_{LC} times and shifted -90º at the resonant frequency f_0. To work properly, the tank should be driven by a low impedance source and its output should be seen by high impedance.

A simple CMOS inverter, as shown in Figure 8-2, driven by a sufficiently large input signal will provide such low driving impedance while acting as a high-impedance isolator to the

preceding stage.

Since the inverter input is sinusoidal, its output jumps rapidly between two supply rail voltages, 0V and V_{DD}, thus producing a near square wave. The 2nd-order low-pass LC tank filters higher harmonics and recreates a sinusoidal with a total phase shift of +90º with respect to the inverter's input. Four of these stages are placed in a loop to make the 360º phase shift around it, thus forming the oscillator's core (see Figure 8-3(a) top). By also providing enough gain, Barkhausen criteria of oscillation are met. Therefore, if there happens to be an oscillation in the loop, the oscillator core will maintain it while creating 0º, 90º, 180º, and 270º phase outputs. Figure 8-3(b) shows the transient waveforms. Having the inverters sized properly, voltage waveforms are nearly square wave. Each of the transistors conducts only when its drain-source voltage is near zero. This way the inverters are working as high-efficiency class-D amplifiers.

Assuming the inverter delay is negligible compared to the delay of each LC tank, the oscillation frequency turns out to be identical to the tank's resonant frequency:

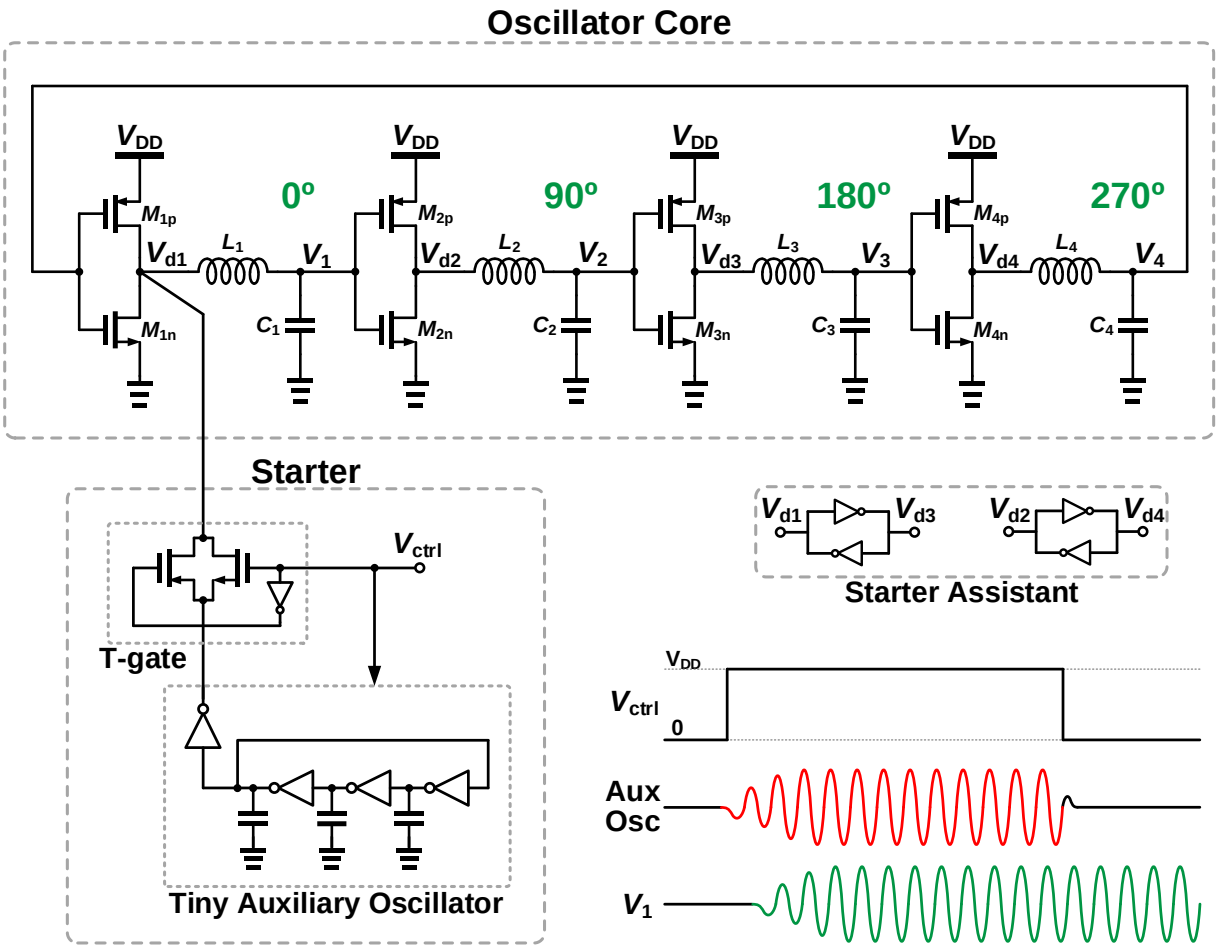
$$f_{osc} = \frac{1}{2\pi\sqrt{LC}}. \tag{8.1}$$

In practice, each of the inverters contributes a few degrees of phase shift (10 ps in this implementation), thus slightly lowering f_{osc}.

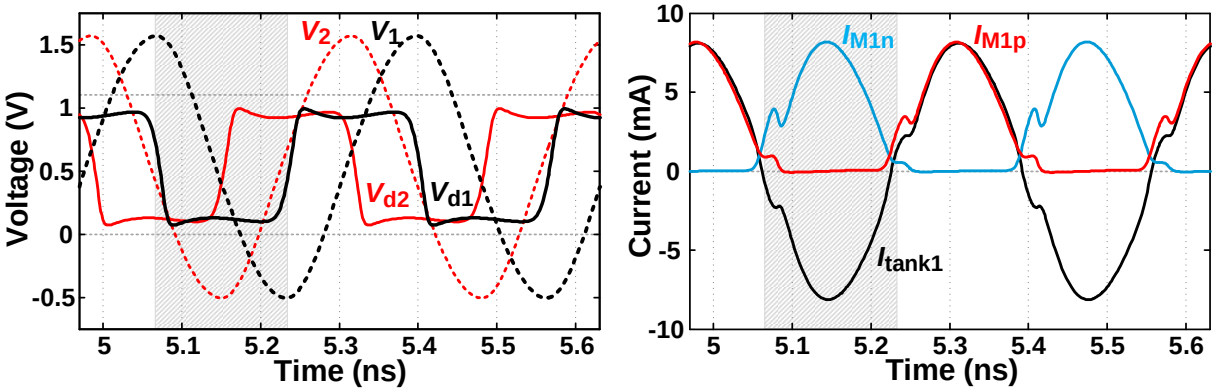
In [103], a multiphase ring structure uses *parallel* LC tanks. Consequently it oscillates at a lower frequency than the tank's resonance with 45º phase shift per LC stage. This reduces Q_{loop} from the maximum possible. A similar structure is also used in [104] with four delay lines in a loop. However, the use of low-efficiency differential amplifiers has resulted in poor PN.

8.1.1.1 Phase Noise Comparison

Superior PN performance of this oscillator topology compared to the conventional ROs is mainly due to its higher total open loop quality factor (Q_{loop}). As calculated in [105], Q_{loop} of a 4-stage inverter RO is ~1.4. Applying the same methodology, Q_{loop} of the proposed oscillator is $4\times Q_{LC}$. Therefore, a very poor quality LC tank, even as low as 1.5 (due to its tiny size) makes the total Q_{loop} ~6, thus substantially improving its phase noise. Due to the low quality of LC tanks, PN sensitivity to mismatches is very low. E.g., even a few percent capacitor mismatch does not degrade PN noticeably and only introduces a few degree of I/Q phase error.



(a)



(b)

Figure 8-3: (a) The proposed oscillator including its core, starter, and starter assistant circuit. (b) Transient voltages and currents of the core at 3 GHz and V_{DD}=1.1 V.

8.1.1.2 Oscillation Amplitude

Oscillation amplitude of the proposed oscillator can be calculated based on the simplified model of one of the stages shown in Figure 8-4(a). The amplifier is modeled as a voltage-

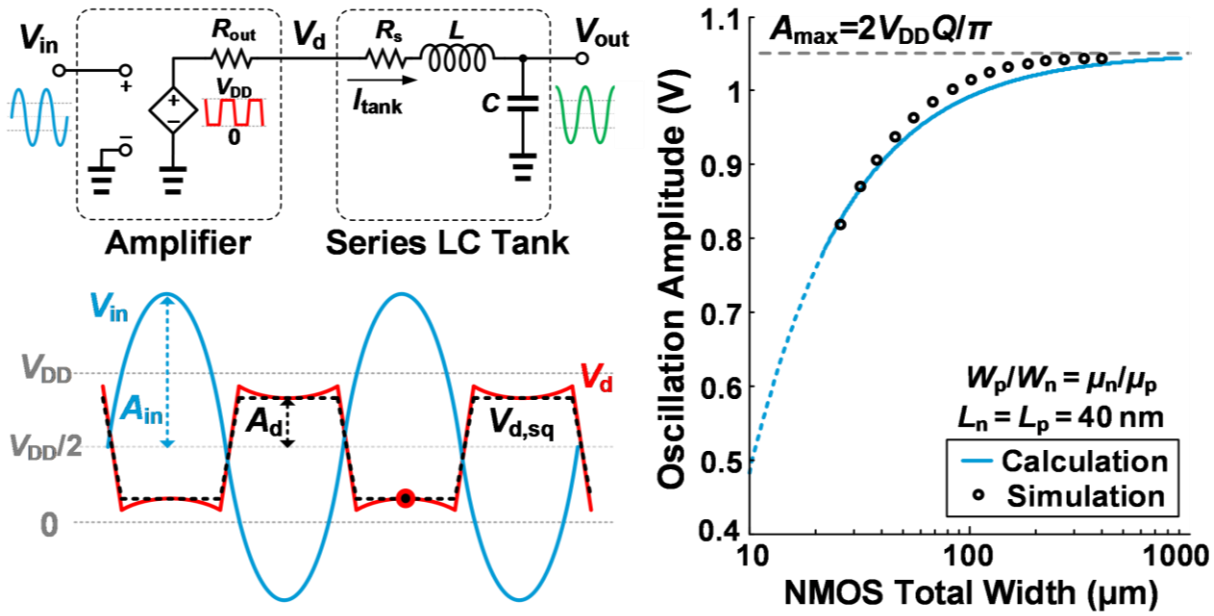


Figure 8-4: (a) Simplified model of one of the stages. (b) Oscillation amplitude versus transistor width (V_{DD} = 1.1 V, f_{osc} = 2.8 GHz, and Q_{LC} = 1.5).

controlled limiting voltage source of output resistance R_{out} switching between the ground (0) and V_{DD}. Signal V_d is then approximated with an ideal square waveform, $V_{d,sq}$, with amplitude A_d. The first harmonic of $V_{d,sq}$ is 4/π times of A_d and so output voltage amplitude becomes:

$$A_{out} = \frac{4}{\pi} A_d Q_{LC} . \tag{8.2}$$

From (8.2), peak current of the tank, that is sinusoidal and out-of-phase with V_{in}, is derived:

$$I_{peak} = \frac{4}{\pi}\frac{A_d}{R_s} = \frac{A_{out}}{Q_{LC} R_s} . \tag{8.3}$$

At the peak of input voltage, where NMOS is in deep triode, V_d reaches $V_{DD}/2$-A_d. Using MOS current equation in triode and (8.2) we have:

$$I_d = k\left(V_{gs} - V_{th}\right)V_{ds} = k\left(A_{in} + \frac{V_{DD}}{2} - V_{th}\right) \times \left(\frac{V_{DD}}{2} - \frac{\pi}{4}\frac{A_{out}}{Q_{LC}}\right), \tag{8.4}$$

where, k is the transistor strength equal to $\mu_n C_{ox} W/L$. At a steady-state oscillation, A_{in} must be equal to A_{out}. Also, considering that NMOS current in (8.4) is the same as tank peak current in (8.3), the oscillation amplitude is found. Figure 8-4(b) shows the calculated oscillation amplitude versus transistor size, which shows a good agreement with simulations. The wider the transistor, the lower output resistance of the inverter and consequently the higher amplitude. For weaker transistors, the drain current deviates from (8.4) towards lower values and the loop might not

even have enough gain for oscillation.

8.1.2 Startup

Before the oscillation could begin, the devices would normally be biased at proper DC operating points. Intrinsic device noise may find a small-signal loop gain higher than unity with 360º phase shift at a certain frequency, so that the oscillation could be build up.

Contrarily, in the proposed oscillator core, even though we could find an oscillation amplitude in which the loop has a large signal gain of unity or more, it will never start the oscillation on its own. Since the core contains four inverting amplifiers, there is a strong positive feedback in the loop at DC (with shorted inductors and opened capacitors) that forces the outputs of inverters to get stuck at 0 and V_{DD} (e.g., V_{d1}=V_{d3}=0 and V_{d2}=V_{d4}=V_{DD}). At this state, the oscillator core is locked and gain of the inverters is almost zero, thus no oscillation.

Consequently, a starter circuit is added (see bottom left of Figure 8-3(a)) to directly put the core in a large-signal mode thus initiating the oscillation. The starter consists of a simple *undersized* auxiliary ring oscillator, and a T-gate switch that connects it to the core. At first, the auxiliary oscillator is turned on and connected to V_{d1}. It makes periodical perturbations to V_{d1} at close to the f_{osc} rate. Large enough perturbations can pull the second stage out of the DC lock state, which is then propagated to all stages. After the oscillation is established in the main core (in few nano-seconds), the auxiliary oscillator is turned off and disconnected. This operation is similar to starting a car engine using its starter. It could be shown that in the large-signal mode the total loop DC gain drops to less than unity and therefore the oscillator cannot fall back into the lock state.

As shown in Figure 8-3(a), adding back-to-back inverters between the complementary outputs (i.e. $V_{d1,3}$ / $V_{d2,4}$) assists with the startup. Three dummy T-gates in “off” state (not shown) connected to outputs of the other core inverters are also used to balance core phases.

8.2 Implementation and Measurement Results

The oscillator is fabricated in TSMC 40-nm CMOS process. To make the total oscillator area as small as the ring oscillators, tiny inductors are used for the oscillator core. Each of them is a 17-turns spiral inductor using two available top thick metals in parallel, all fit in a 34μm×34μm area (Figure 8-5). As per EM simulations, inductance value is ~5.6 nH with self-resonance of ~20 GHz. Tank Q-factor ranges from 2.0 to 3.4, though the effective *Q*, loaded by the output

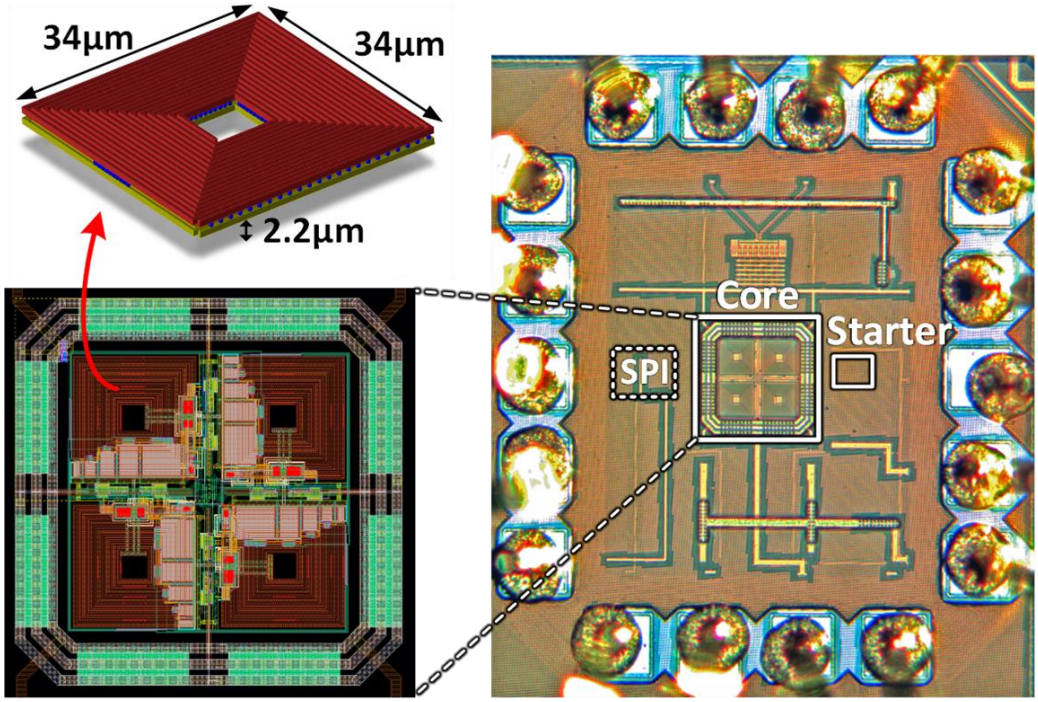


Figure 8-5: Chip micrograph of the proposed oscillator with its symmetric layout.

resistance of the inverters, drops to 1.6–2.8 over the tuning range (TR). The frequency tuning capacitors ($C_{1\text{-}4}$) are implemented as 5-bit binary switched-capacitor banks with a maximum value of 500 fF. Each of them is placed underneath its inductor to save area, at a cost of negligible reduction in tuning range.

The total oscillator core occupies 80 µm × 80 µm. Although the inductors are closely spaced, each adjacent pair has lower than 4% magnetic coupling. As measured, oscillation frequency covers almost an octave, tunable from 2.66 to 4.97 GHz (61%). Worst-case I/Q inaccuracy for 5 samples is between 35 to 45 dB (≈1°) over TR.

The starter circuit is placed out of the core area and occupies 16 µm × 30 µm. Its frequency is tunable via 5-bit binary-weighted switched capacitors. Its TR is from 2 to 6 GHz, designed to cover more than the whole core tuning range to ensure startup at any condition.

Phase noise is measured using R&S® FSW spectrum analyzer. Figure 8-6 shows measured PN of -132 dBc/Hz at 10 MHz offset from 4.97 GHz carrier. Figure 8-7 shows PN and its FoM across the tuning range. At higher frequencies, where the effective Q-factor is higher, the FoM is better. To ensure reliability, V_{DD} is lowered linearly from 1.1 to 0.9 V at higher frequencies. Flicker noise corner is between 600 kHz to 2 MHz over TR.

Table 8-1 summaries the proposed oscillator performance and compares it with state-of-the-

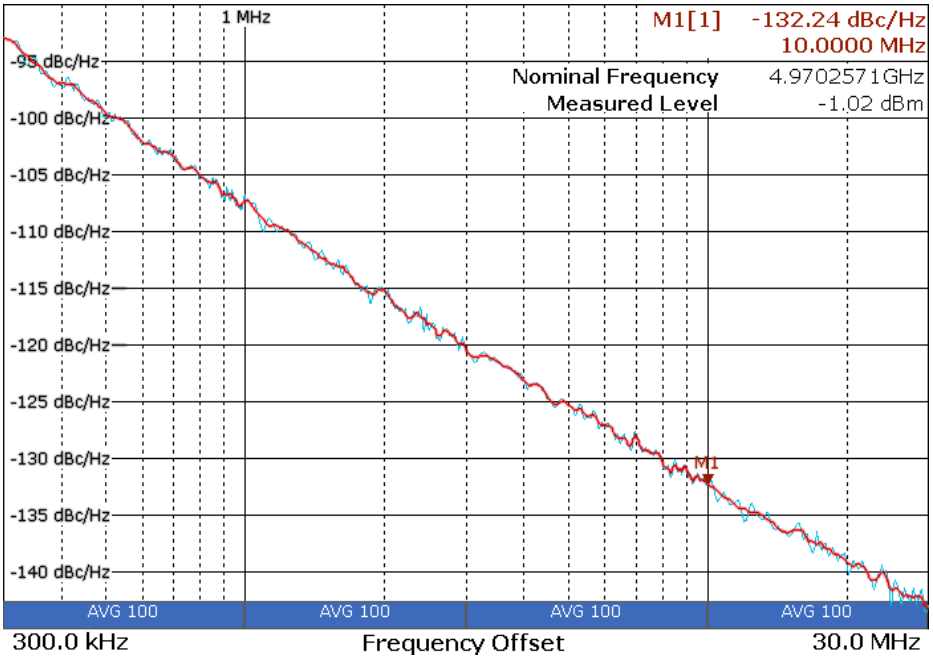


Figure 8-6: Measured phase noise spectrum at 4.97 GHz carrier.

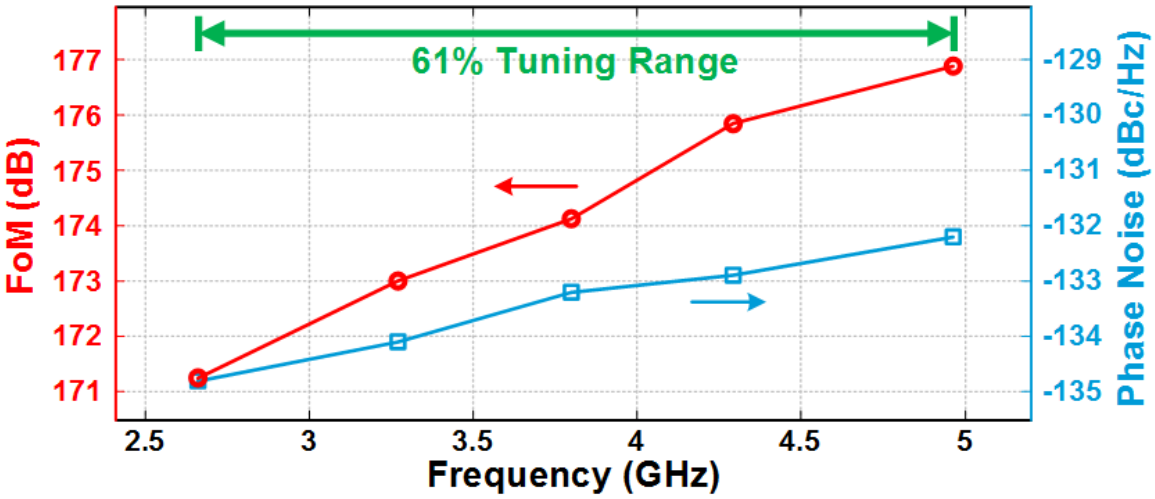


Figure 8-7: Measured phase noise and FoM @ 10MHz offset over tuning range.

art low-area oscillators. Its total area of 0.0069 mm^2 is comparable to a conventional inverter ring oscillator. While maximum phase noise FoM of best ring oscillators ranges 155–170 dB, the proposed oscillator offers 7–20 dB better FoM. In fact, its FoM is the best amongst all other small-size oscillators and almost reaches the FoM of regular large-area LC-tank RF oscillators. Figure 8-8 plots FoM of state-of-the-art ring and LC oscillators versus their active area. The proposed oscillator clearly stands out between the two groups: for low-cost (i.e., area) applications, it has a lower PN or power consumption than ring oscillators; for high performance applications, it saves significant area by consuming somewhat higher power compared to normal LC oscillators.

Table 8-1: Performance summary and comparison with state-of-the-art low-area oscillators.

	This Work	[97] **MWCL'09**	[98] **TMTT'09**	[99] **MWCL'13**	[100] **ISSCC'15**	[101] **ISSCC'15**
Technology	**40 nm**	180 nm	130 nm	65 nm	45 nm	16 nm FF
Description	**Series LC**	Inv. Ring	Inv. Ring	Inv. Ring	Inv. Ring	Inv. Ring
Tuning Range (GHz)	**2.66 – 4.97**	1.7 – 5.5	1.8 – 10.2	2 – 8	2 – 3	0.25 – 4
Supply Voltage (V)	**1.1 – 0.9**	2.9	1.3	1.2	1.0	0.52 – 0.8
Power (mW)	**16 – 8.5**	81	5	1.7-6.8	3.1	4.64
Frequency (GHz)	**4.97**	4.46	5.6	4.2	2.4	3
Phase Noise (dBc/Hz) @ (MHz)	**-132.2 @10**	-120.2 @4	-121.7 @10	-101 @1	-121 @10	-120.2 @10
FoM* **(dB)**	**171.3 – 176.9**	162.2	158.3–169.9	165.4	163.7	163.0
Area (mm^2)	**0.0063**	0.01	0.0144	0.038	NA	~0.004

***FoM = $|PN| + 20\log_{10}(f_{osc}/\Delta f) - 10\log_{10}(P_{DC}/1mW)$**

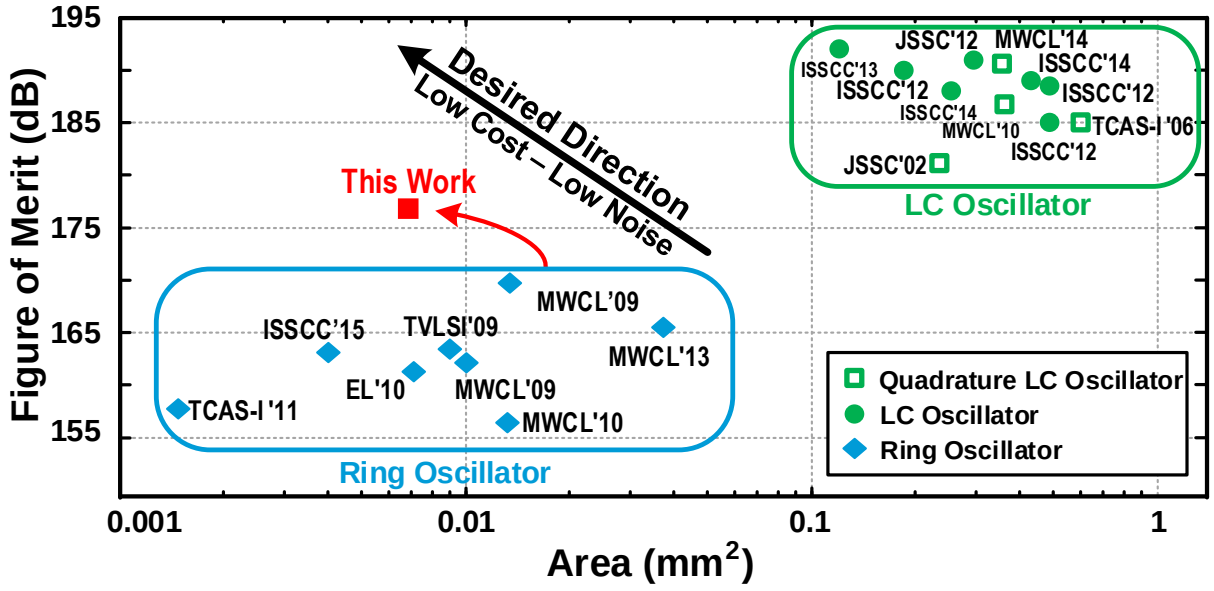


Figure 8-8: FoM of state-of-the art oscillators versus active area.

8.3 Extension to Ultra-Low Phase-Noise Performance

The current proposed structure can be extended to an ultra-low phase-noise oscillator by using normal inductors. For example here, each inductor occupies 190µm × 190µm, to provide a higher quality factor $Q \approx 8$. Since the series LC tank at resonance has a voltage amplification

gain of Q for the first harmonic (see Figure 8-1(b)), its voltage swing can break down the gate oxide of inverters. Therefore, a capacitor is placed before each inverter to make a capacitive voltage divider in combination with parasitic capacitance of the inverter. Then, by choosing a proper capacitor value, voltage swing at the input of inverter can be reduced to a value ensuring reliability of the transistors. Figure 8-10 shows schematic of this version using capacitor dividers.

In this version, gate of the transistors are biased through $R_{1\text{-}4}$ to V_{bias} which comes from a dummy self-biased inverter. In addition to the starter, three dummy switches are placed at the output of other inverters to keep phases balanced.

The main way to tune the frequency of oscillation is changing the capacitances in series with the inductors. Course tuning banks $C_{1\text{-}4}$ are tunable by 4 bits of 20fF steps. It covers a tuning of 26% from 1.85 to 2.4GHz. In addition to these banks, four fine tuning banks are added ($C_{1g\text{-}4g}$).

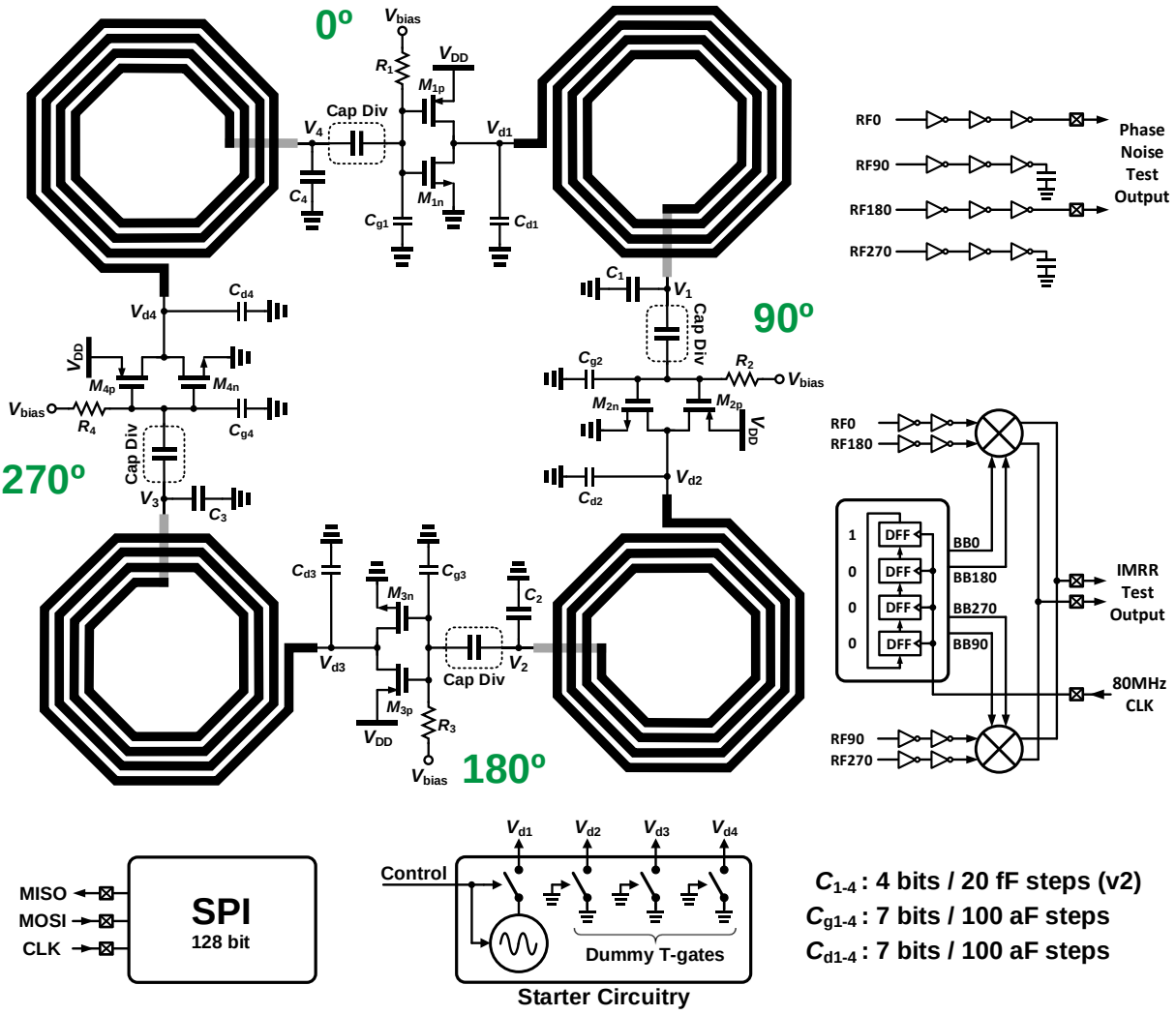


Figure 8-9: Ultra-low phase noise version using normal inductors.

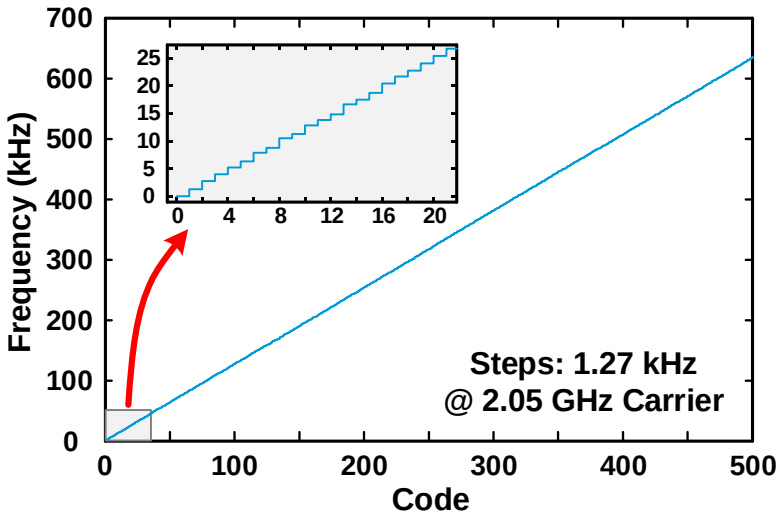


Figure 8-10: Ultra-fine resolution frequency tuning using drain capacitance.

Each of these capacitor banks are 7 bits with an ultra-low step size of 100 aF. This gives a frequency resolution of 20 kHz in 500 steps (≈ 4×27 levels), when fine tuning banks are controlled separately. To achieve further ultra-fine tuning steps, capacitor banks can be placed at the inverter outputs. Any capacitance at the output of each inverter introduces a small delay inversely proportional to the large-signal Gm of the inverter. As the inverters are very strong to be able to drive the LC tanks, the capacitance effect at the output of inverters in much smaller than its effect when it is paralleled with $C_{1\text{-}4}$. Placing the same fine-tuning banks at the output of inverters ($C_{1d\text{-}4d}$) improves the frequency resolution down to 1.27 kHz, that is 16x reduction in this implementation. Figure 8-10 shows frequency change of the ultra-fine tuning bank versus input code. Measured DNL and INL ranges −0.9/+0.95 and −0.86/+1 LSB, respectively. Considering the achieved DNL/INL, the frequency resolution of 1.27 kHz is the best ever reported number as far as our knowledge.

Chip micrograph of this implementation is depicted in Figure 8-11. The oscillator shows an FoM of 186.5 to 187 dB across its tuning range when V_{DD} is 0.8 V. Figure 8-12 shows PN and FoM of the high performance oscillator versus supply voltage. As V goes down, voltage amplitude at the inputs of inverters are reduced and thus output impedance of the inverters are increased. This gradually degrades the tank quality factor and results in a lower FoM. Table 8-2 summaries performance of this implementation and compares it with other state-of-the-art oscillators.

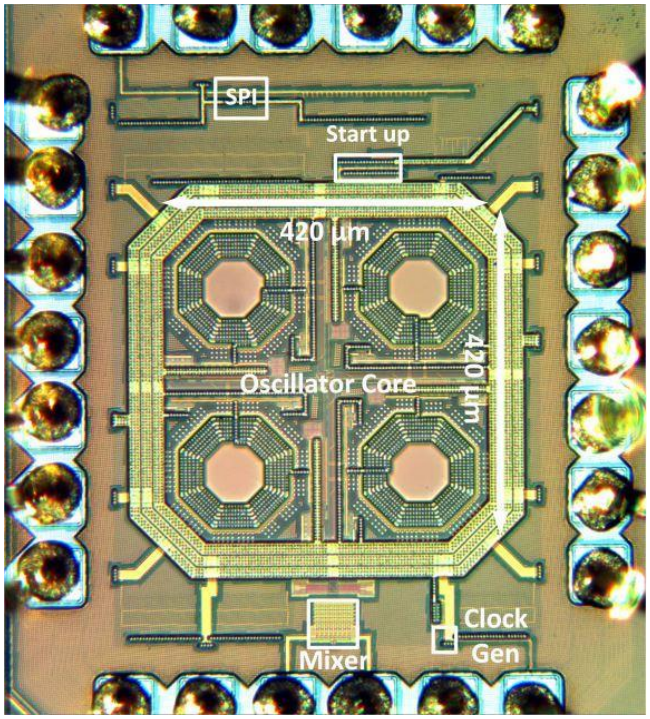


Figure 8-11: Chip micrograph of the ultra-low phase noise version.

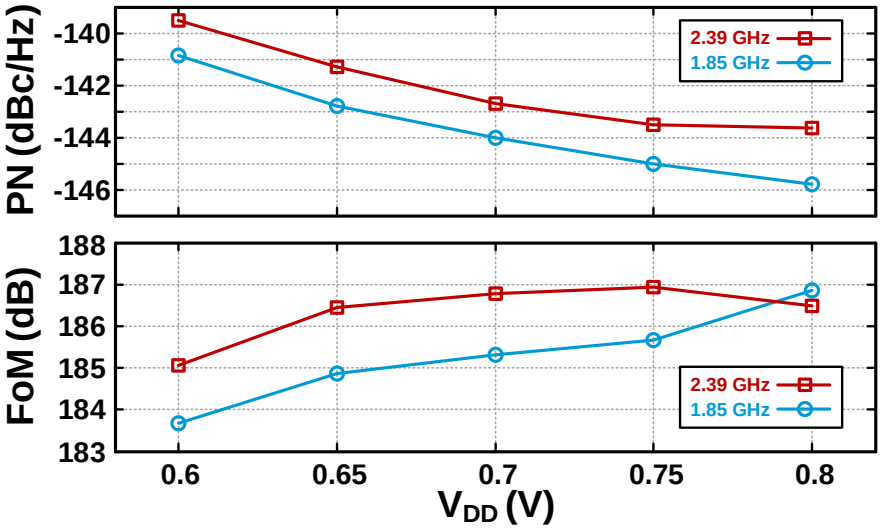


Figure 8-12: Measured phase noise and FoM versus V_{DD}, at 3 MHz offset frequency.

8.4 Conclusion

In this chapter, a new oscillator topology is proposed. It arranges four series LC tanks in a ring structure. In a low-area implementation using low-Q inductors in CMOS 40nm, this oscillator shows 7-20 dB better phase noise than other state-of-the-art ring oscillators, while occupying the same area and maintaining wide tuning range. Later, this idea is extended to an ultra-low phase noise by means of normal inductors in another 40-nm CMOS test chip. In this

Table 8-2: Performance summary and comparison with state-of-the-arts.

	This Work	[106] JSSC'02	[107] TCAS-I'06	[108] JSCC'10	[109] ESSCIRC'12
Technology (nm)	40	350	180	130	65
Architecture	Series LC QDCO	Quadrature VCO	Injection locked QVCO	Multi-phase VCO	ΔΣ-less DCO
Frequency (GHz)	1.85	1.82	1.85	5.12	3.63
Tuning range (GHz)	1.85-2.4 (26%)	1.64-1.97 (18%)	1.7-2.035 (18%)	–	3.1-4.1 (28%)
Supply (V)	0.8	2	1.8	0.5	1.2
Phase noise (dBc/Hz) @offset (MHz)	-145.8 @3	-140 @3	-139 @3	-126.1 @1	-151 @10
Power (mW)	37.6	50	18	4	56.7
FOM	186.9	178-182	185	194.2	185
IMRR (dB) (#Sample)	48-60 (#5)	52 (#7)	46 (#20)	55 (–)	–
Core area (mm²)	0.176	0.24[1]	0.6[2]	0.31	0.329
Frequency-step (kHz) DNL/INL (LSB)	1.27 <1 / <1	–	–	–	9.2 <0.12 / –

[1] **Estimated core area.**

oscillator topology, using switched-capacitor tuning banks at the amplifiers output improves frequency tuning resolution significantly. Moreover, voltage amplification of Q times by the series LC tank facilitates the low voltage operation.

Chapter 9

Conclusion

In this dissertation, design, modeling, and implementation of a fully integrated discrete-time superheterodyne receiver, including the local oscillator, in deep nano-scale CMOS processes are discussed. We have now arrived at the final chapter of this work. Section 9.1 summarizes the thesis and also repeats the accomplishments achieved throughout the thesis. Finally, Section 9.2 proposes some suggestions in order to expand this work.

9.1 The Thesis Outcome

The superheterodyne with resonant band pass filters (BPFs) tuned at a fixed intermediate frequency was the architecture of choice for wireless receivers constructed with external discrete components. With the invention of IC chip, the zero IF architecture has attracted designers to make fully monolithic receivers, mainly for cost reasons. It has been predominant ever since. The main attraction of the zero-IF architecture is that it does not require a BPF, which is needed in a superheterodyne for image rejection, and can instead rely on low-pass filters for channel selection, which are much easier to integrate in CMOS. However, the problems of time-variant DC offset, limited IIP2, and a high devices flicker noise immediately arise. These problems are nowadays mitigated by comprehensive DC offset cancellation and IIP2 calibration loops, combined with slightly shifting the intermediate frequency from zero to low-IF.

However, the historical superheterodyne architecture does not inherently suffer from these problems due to a high IF operation. One of the challenges towards a fully integrated

superheterodyne receiver was the integration of IF bandpass filter, which is now solved in this work.

On the other hand, while transistor cutoff frequency (f_T) has improved dramatically with scaling, conventional RF/analog techniques, which were optimized for the older technology, do not effectively use the ultra-high speed of transistors of scaled CMOS to improve the system performance. In contrast, DT RF/analog building blocks, such as MOS switch, capacitor, gm-cell, and digital clock generator, benefit directly from scaling in terms of speed, power consumption and area. Therefore, an attempt was to use as much as possible the DT RF/analog or digital-like blocks throughout this dissertation. DT implementation also reduces performance sensitivity to the process variations.

In Chapter 2, the 4x sampling scheme required for proper operation of high-IF receiver is proposed. This scheme ensure an image-less operation of the sampling front-end. Basic sampling concepts such as voltage and charge sampling are described in Chapter 3. In addition, a novel 7^{th}-order DT LPF is proposed that is suitable for baseband signal processing of the proposed receiver. The order of this filter is easily extendable to even higher orders. Using pipelining techniques, sample rate of the filter is increased up to 1GS/s. Its state-of-the-art performance includes: very low power consumption, the lowest reported input-referred noise, very wide tuning range and excellent linearity. In Chapter 4, a fully integrated DT I/Q charge-sharing BPF in proposed that fits well as the IF filter of superheterodyne receivers. Unlike N-path filters, this BPF does not have any spectral peak replicas. Passive implementation of this filter allows it to work up to 12 GS/s. The center frequency of the proposed BPF filter as well as cut-off frequency of the LPF are digitally controllable via clock frequency and capacitor ratios and thus insensitive to PVT variations. In Chapter 5, a wideband noise cancelling LNTA is proposed. In this LNTA, in addition to noise of the input matching transistor pair, noise of another transistor pair in is also cancelled. Noise analysis of the proposed LNTA is presented to derive it NF equation that is verified by simulation.

Chapter 6 presented a complete chain of the proposed fully integrated superheterodyne receiver implemented in 65-nm CMOS. In addition to the insensitivity to flicker noise and time-varying DC offsets, this superheterodyne RX shows an extremely high IIP2 without requiring any calibration. This characteristic makes this architecture a suitable candidate for future SAW-

less receivers that work in FDD modes. DT signal processing using passive switched-capacitor circuits makes this receiver process scalable. It only uses switches, capacitors, and inverter-based gm-cells. The use of a high-order, but very low-power and low-noise baseband DT filters, reduces the required ADC sample rate and dynamic range thus leading to a lower total power consumption.

As an essential block of each fully integrated transceiver, two novel low-voltage oscillator topologies are proposed suitable for nano-scale CMOS. Chapter 7 proposes a high-swing class-C oscillator. The higher swing is owed to the removed tail current source of the oscillator core combined with a bias control circuit. A low-power/ low-voltage test chip of this oscillator is implemented in 90-nm CMOS. As a whole, it can achieve good phase noise performance with better FoM than the original class-C oscillator, especially at low supply voltages. Finally, Chapter 8 proposes a new oscillator topology using four series LC tanks in a ring structure. In a low-area implementation using low-Q inductors in 40nm CMOS, this oscillator shows 7-20 dB better phase noise than other state-of-the-art ring oscillators, while occupying the same area and maintaining a wide tuning range. Voltage amplification of Q times by the series LC tank and using a digital inverter as an amplifier make this topology a suitable candidate for a low voltage operation in nano-scale CMOS.

9.2 Suggestions for Future Developments

The findings of this dissertation indicate that the discrete-time (DT) signal processing will be the approach of choice for future development of commercial receivers in nanoscale CMOS.

- As showed in this dissertation, the DT superheterodyne receiver could solve the well-known problems of zero-IF receivers. Since the IIP2 problem is completely solved in the superheterodyne, this approach could be easily extended for SAW-less receivers. In such a receiver, LNTA's 3rd-order nonlinearity will be the dominant problem in the FDD mode. As TX-to-RX leakage is combined with a half-duplex blocker, a high 3rd-order intermodulation product will be created. Immediate solution is to design a highly linear LNTA at a cost of a very high power consumption. However, a wiser solution would be to use the given information that frequency of one of the input blocking signals is known, i.e., the TX leakage. Then, a notch filter at TX frequency made by DT techniques can be placed at the LNTA

output to increase its linearity.

- The proposed DT superheterodyne RX is particularly suitable for high-performance applications, such as cellular handsets. If a low power application is targeted instead, where IIP2 is less troublesome, a DT zero-IF/low-IF could further save power consumption. However, all the state-of-the-art DT receivers up to now have used lower than the 1x sampling, or even decimating the signal just after the 1x sampling. In this way, a high level images are created. If a DT zero-IF receiver is going to be again implemented, it is suggested to use the 2x sampling concept that does not create any images. Right afterwards, a high-order DT charge-rotating LPF with the same rate needs to be used. After a sufficient out-of-band filtering, decimation and more processing can be done. This suggestion could lead to the lowest possible power consumption.
- The idea of the high-order DT charge-rotating LPF can be extended to low-frequency biomedical applications by lowing its sample rate and resizing its capacitors. As noise of this type of filter is exceptionally low, this solution could lead to the lower input-referred noise than in the conventional opamp-based filters, but with an ultra-low power consumption. The limiting parameter for the low frequency implementation is the leakage of MOS switches in "off" state.

Bibliography

[1] T. H. Lee, *The Design of CMOS Radio-Frequency Integrated Circuits*. Cambridge University Press, 2004.

[2] C. P. Yue and S. S. Wong, "Scalability of RF CMOS," in *IEEE Radio Frequency Integrated Circuits (RFIC) Symposium - Digest of Papers*, 2005, pp. 53–56.

[3] C. H. Diaz, D. D. Tang, and J. Y. C. Sun, "CMOS technology for MS/RF SoC," *IEEE Transactions on Electron Devices*, vol. 50, no. 3, pp. 557–566, 2003.

[4] M. Tohidian, I. Madadi, and R. B. Staszewski, "A 2mW 800MS/s 7th-order discrete-time IIR filter with 400kHz-to-30MHz BW and 100dB stop-band rejection in 65nm CMOS," in *IEEE International Solid-State Circuits Conference (ISSCC) - Digest of Technical Papers*, 2013, vol. 56, pp. 174–175.

[5] M. Tohidian, I. Madadi, and R. B. Staszewski, "Analysis and Design of a High-Order Discrete-Time Passive IIR Low-Pass Filter," *IEEE Journal of Solid-State Circuits*, vol. 49, no. 11, pp. 2575 – 2587, 2014.

[6] I. Madadi, M. Tohidian, and R. B. Staszewski, "A 65nm CMOS high-IF superheterodyne receiver with a High-Q complex BPF," in *IEEE Radio Frequency Integrated Circuits Symposium (RFIC)*, 2013, pp. 323–326.

[7] A. Mirzaei, H. Darabi, and D. Murphy, "A low-power process-scalable super-heterodyne receiver with integrated high-Q filters," *IEEE Journal of Solid-State Circuits*, vol. 46, no. 12, pp. 2920–2932, 2011.

[8] R. B. Staszewski, K. Muhammad, D. Leipold, C. M. Hung, Y. C. Ho, J. L. Wallberg, C. Fernando, K. Maggio, R. Staszewski, T. Jung, J. Koh, S. John, I. Y. Deng, V. Sarda, O. Moreira-Tamayo, V. Mayega, R. Katz, O. Friedman, O. E. Eliezer, E. De-Obaldia, and P. T. Balsara, "All-digital TX frequency synthesizer and discrete-time receiver for Bluetooth radio in 130-nm CMOS," *IEEE Journal of Solid-State Circuits*, vol. 39, no. 12, pp. 2278–2291, 2004.

[9] K. Muhammad, Y. Ho, T. L. Mayhugh, C. Hung, T. Jung, I. Elahi, C. Lin, I. Y. Deng, C. Fernando, J. L. Wallberg, S. K. Vemulapalli, S. Larson, T. Murphy, D. Leipold, P. Cruise,

J. Jaehnig, M. Lee, R. B. Staszewski, R. Staszewski, and K. Maggio, "The First Fully Integrated Quad-Band GSM/GPRS Receiver in a 90-nm Digital CMOS Process," *IEEE Journal of Solid-State Circuits*, vol. 41, no. 8, pp. 1772–1783, 2006.

[10] R. Bagheri, A. Mirzaei, S. Chehrazi, M. E. Heidari, M. Lee, M. Mikhemar, W. Tang, and A. A. Abidi, "An 800-MHz-6-GHz software-defined wireless receiver in 90-nm CMOS," *IEEE Journal of Solid-State Circuits*, vol. 41, no. 12, pp. 2860–2875, 2006.

[11] A. Geis, J. Ryckaert, L. Bos, G. Vandersteen, Y. Rolain, and J. Craninckx, "A 0.5 mm2 power-scalable 0.5-3.8-GHz CMOS DT-SDR receiver with second-order RF band-pass sampler," *IEEE Journal of Solid-State Circuits*, vol. 45, no. 11, pp. 2375–2387, 2010.

[12] R. Chen and H. Hashemi, "A 0.5-to-3 GHz software-defined radio receiver using discrete-time RF signal processing," *IEEE Journal of Solid-State Circuits*, vol. 49, no. 5, pp. 1097–1111, 2014.

[13] B. Razavi, *RF Microelectronics*. Englewood Cliffs, NJ, USA: Prentice Hall, 1997.

[14] M. Tohidian, I. Madadi, and R. B. Staszewski, "A Fully Integrated Discrete-Time Superheterodyne Receiver," *under review in IEEE Transactions on Circuits and Systems I: Regular Papers*, 2015.

[15] D. Kaczman, M. Shah, M. Alam, M. Rachedine, D. Cashen, L. Han, and A. Raghavan, "A single-chip 10-band WCDMA/HSDPA 4-band GSM/EDGE SAW-less CMOS receiver with DigRF 3G interface and +90 dBm IIP2," *IEEE Journal of Solid-State Circuits*, vol. 44, no. 3, pp. 718–739, 2009.

[16] Y. Feng, G. Takemura, S. Kawaguchi, N. Itoh, and P. R. Kinget, "Digitally assisted IIP2 calibration for CMOS direct-conversion receivers," *IEEE Journal of Solid-State Circuits*, vol. 46, no. 10, pp. 2253–2267, 2011.

[17] K. Dufrêne, Z. Boos, and R. Weigel, "Digital adaptive IIP2 calibration scheme for CMOS downconversion mixers," *IEEE Journal of Solid-State Circuits*, vol. 43, no. 11, pp. 2434–2445, 2008.

[18] H. Darabi, H. J. K. H. J. Kim, J. Chiu, B. Ibrahim, and L. Serrano, "An IP2 Improvement Technique for Zero-IF Down-Converters," in *2006 IEEE International Solid State Circuits Conference - Digest of Technical Papers*, 2006, vol. 38, pp. 171–174.

[19] M. Chen, Y. Wu, and M. F. Chang, "Active 2nd-order intermodulation calibration for direct-conversion receivers," in *IEEE International Solid State Circuits Conference - Digest of Technical Papers*, 2006, vol. 38, no. 6, pp. 171–174.

[20] B. Van Liempd, J. Borremans, E. Martens, S. Cha, H. Suys, B. Verbruggen, and J. Craninckx, "A 0.9 V 0.4-6 GHz harmonic recombination SDR receiver in 28 nm CMOS with HR3/HR5 and IIP2 calibration," *IEEE Journal of Solid-State Circuits*, vol. 49, no. 8, pp. 1815–1826, 2014.

[21] M. Tohidian, I. Madadi, and R. B. Staszewski, "A fully integrated highly reconfigurable discrete-time superheterodyne receiver," in *IEEE International Solid-State Circuits*

Conference (ISSCC) - Digest of Technical Papers, 2014, pp. 72–73.

[22] A. Mirzaei, S. Chehrazi, R. Bagheri, and A. A. Abidi, "Analysis of first-order anti-aliasing integration sampler," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 55, no. 10, pp. 2994–3005, 2008.

[23] S. Karvonen, T. a D. Riley, and J. Kostamovaara, "A CMOS quadrature charge-domain sampling circuit with 66-dB SFDR up to 100 MHz," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 52, no. 2, pp. 292–304, 2005.

[24] S. Karvonen, T. a D. Riley, S. Kurtti, and J. Kostamovaara, "A quadrature charge-domain sampler with embedded FIR and IIR filtering functions," *IEEE Journal of Solid-State Circuits*, vol. 41, no. 2, pp. 507–515, 2006.

[25] Z. Ru, E. a M. Klumperink, and B. Nauta, "Discrete-time mixing receiver architecture for RF-sampling software-defined radio," *IEEE Journal of Solid-State Circuits*, vol. 45, no. 9, pp. 1732–1745, 2010.

[26] K. Muhammad, D. Leipold, R. B. Staszewski, Y.-C. Ho, C. M. Hung, K. Maggio, C. Fernando, T. Jung, J. Wallberg, J.-S. Koh, S. John, I. Deng, O. Moreira, R. Staszewski, R. Katz, and O. Friedman, "A Discrete-Time Bluetooth Receiver in a 0.13µm Digital CMOS Process," in *IEEE International Solid-State Circuits Conference*, 2004, pp. 268–527.

[27] A. Geis, J. Ryckaert, J. Borremans, G. Vandersteen, Y. Rolain, and J. Craninckx, "A compact low power SDR receiver with 0.5-20MHz baseband sampled filter," in *IEEE Radio Frequency integrated Circuits (RFIC) Symposium - Digest of Papers*, 2009, pp. 285–288.

[28] Y.-C. Ho, R. B. Staszewski, K. Muhammad, C.-M. Hung, D. Leipold, and K. Maggio, "Charge-Domain Signal Processing of Direct RF Sampling Mixer with Discrete-Time Filters in Bluetooth and GSM Receivers," *EURASIP Journal on Wireless Communications and Networking*, vol. 2006, pp. 1–14, 2006.

[29] S. Kiriaki, T. L. Viswanathan, G. Feygin, R. B. Staszewski, R. Pierson, B. Krenik, M. De Wit, and K. Nagaraj, "A 160-MHz analog equalizer for magnetic disk read channels," *IEEE Journal of Solid-State Circuits*, vol. 32, no. 11, pp. 1839–1849, 1997.

[30] G. T. Uehara and P. R. Gray, "100 MHz A/D interface for PRML magnetic disk read channels," *IEEE Journal of Solid-State Circuits*, vol. 29, no. 12, pp. 1606–1613, 1994.

[31] S. S. Lee and C. a. Laber, "A BiCMOS continuous-time filter for video signal processing applications," *IEEE Journal of Solid-State Circuits*, vol. 33, no. 9, pp. 1373–1382, 1998.

[32] F. Yang and C. C. Enz, "A low-distortion BiCMOS seventh-order bessel filter operating at 2.5 V supply," *IEEE Journal of Solid-State Circuits*, vol. 31, no. 3, pp. 321–330, 1996.

[33] S. D'Amico, M. Conta, and A. Baschirotto, "A 4.1-mW 10-MHz fourth-order source-follower-based continuous-time filter with 79-dB DR," *IEEE Journal of Solid-State Circuits*, vol. 41, no. 12, pp. 2713–2719, 2006.

[34] T. Y. Lo and C. C. Hung, "A Wide Tuning Range Gm–C Filter for Multi-Mode CMOS Direct-Conversion Wireless Receivers," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 54, no. 4, pp. 713–722, 2007.

[35] A. Pirola, A. Liscidini, and R. Castello, "Current-mode, WCDMA channel filter with in-band noise shaping," *IEEE Journal of Solid-State Circuits*, vol. 45, no. 9, pp. 1770–1780, 2010.

[36] M. S. Savadi Oskooei, N. Masoumi, M. Kamarei, and H. Sjöland, "A CMOS 4.35-mW +22-dBm IIP3 continuously tunable channel select filter for WLAN/WiMAX receivers," *IEEE Journal of Solid-State Circuits*, vol. 46, no. 6, pp. 1382–1391, 2011.

[37] A. Vasilopoulos, G. Vitzilaios, G. Theodoratos, and Y. Papananos, "A low-power wideband reconfigurable integrated active-RC filter with 73 dB SFDR," *IEEE Journal of Solid-State Circuits*, vol. 41, no. 9, pp. 1997–2008, 2006.

[38] S. Kousai, M. Hamada, R. Ito, and T. Itakura, "A 19.7 MHz, fifth-order active-RC chebyshev LPF for draft IEEE802.11n with automatic quality-factor tuning scheme," *IEEE Journal of Solid-State Circuits*, vol. 42, no. 11, pp. 2326–2337, 2007.

[39] M. Ghaderi, J. Nossek, and G. Temes, "Narrow-band switched-capacitor bandpass filters," *IEEE Transactions on Circuits and Systems*, vol. 29, 1982.

[40] R. Winoto and B. Nikolic, "Discrete Time Processing of RF Signals," in *Multi-Mode/Multi-Band RF Transceivers for Wireless Communications: Advanced Techniques, Architectures, and Trends*, G. Hueber and R. B. Staszewski, Eds. New York, NY, USA: Wiley-IEEE Press, 2011, pp. 219–245.

[41] J. Y. J. Yuan, "A charge sampling mixer with embedded filter function for wireless applications," in *2nd International Conference on Microwave and Millimeter Wave Technology Proceedings*, 2000, pp. 315–318.

[42] Y. S. Poberezhskiy and G. Y. Poberezhskiy, "Sampling and signal reconstruction circuits performing internal antialiasing filtering and their influence on the design of digital receivers and transmitters," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 51, no. 1, pp. 118–129, 2004.

[43] R. Gregorian and G. C. Temes, *Analog MOS Integrated Circuits for Signal Processing*. New York, NY, USA: Wiley, 1986.

[44] B. Nauta, "A CMOS transconductance-C filter technique for very high frequencies," *IEEE Journal of Solid-State Circuits*, vol. 27, no. 2, pp. 142–153, 1992.

[45] B. Razavi, *Design of Analog CMOS Integrated Circuits*. New York, NY, USA: McGraw-Hill, 2001.

[46] Z. Ru, N. a. Moseley, E. a M. Klumperink, and B. Nauta, "Digitally enhanced software-defined radio receiver robust to out-of-band interference," *IEEE Journal of Solid-State Circuits*, vol. 44, no. 12, pp. 3359–3375, 2009.

[47] M. J. Gingell, "Single Sideband Modulation Using Sequence Asymmetric Polyphase Networks," *Electrical Communication*, vol. 48, pp. 21–25, 1973.

[48] J. Crols and M. S. J. Steyaert, "Low-IF topologies for high-performance analog front ends of fully integrated receivers," *IEEE Transactions on Circuits and Systems II: Analog and Digital Signal Processing*, vol. 45, no. 3, pp. 269–282, 1998.

[49] F. Behbahani, Y. Kishigami, J. Leete, and A. a. Abidi, "CMOS mixers and polyphase filters for large image rejection," *IEEE Journal of Solid-State Circuits*, vol. 36, no. 6, pp. 873–887, 2001.

[50] K. K. Parhi, "VLSI Digital Signal Processing Systems: Design and Implementation." John Wiley & Sons, 1999.

[51] L. Wanhammar, *DSP Integrated Circuits*. 1999.

[52] I. Madadi, M. Tohidian, and R. B. Staszewski, "Analysis and Design of I/Q Charge-Sharing Band-Pass-Filter for Superheterodyne Receivers," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 62, no. 8, pp. 2114–2121, Aug. 2015.

[53] A. Mirzaei, H. Darabi, and D. Murphy, "Architectural evolution of integrated M-phase high-Q bandpass filters," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 59, no. 1, pp. 52–65, 2012.

[54] a. Kumar and P. E. Allen, "An 80 MHz noise optimized continuous-time bandpass filter in 0.25 μm BiCMOS," in *IEEE Custom Integrated Circuits Conference (CICC)*, 2007, pp. 679–682.

[55] H. Le-Thai, H.-H. Nguyen, H.-N. Nguyen, H.-S. Cho, J.-S. Lee, and S.-G. Lee, "An IF Bandpass Filter Based on a Low Distortion Transconductor," *IEEE Journal of Solid-State Circuits*, vol. 45, no. 11, pp. 2250–2261, 2010.

[56] L. E. Franks and I. W. Sandberg, "An Alternative Approach to the Realization of Network Transfer Functions: The N -Path Filter," *Bell System Technical Journal*, vol. 39, pp. 1321–1350, 1960.

[57] A. Mirzaei, H. Darabi, A. Yazdi, Z. Zhou, E. Chang, and P. Suri, "A 65 nm CMOS quad-band SAW-less receiver SoC for GSM/GPRS/EDGE," *IEEE Journal of Solid-State Circuits*, vol. 46, no. 4, pp. 950–964, 2011.

[58] A. Ghaffari, E. a M. Klumperink, M. C. M. Soer, and B. Nauta, "Tunable high-q N-Path Band-Pass filters: Modeling and verification," *IEEE Journal of Solid-State Circuits*, vol. 46, no. 5, pp. 998–1010, 2011.

[59] M. Darvishi, R. Van Der Zee, and B. Nauta, "Design of active N-path filters," *IEEE Journal of Solid-State Circuits*, vol. 48, no. 12, pp. 2962–2976, 2013.

[60] A. Mirzaei and H. Darabi, "Analysis of imperfections on performance of 4-phase passive-mixer-based high-Q bandpass filters in SAW-less receivers," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 58, no. 5, pp. 879–892, 2011.

[61] A. V. Oppenheim and R. W. Schafer, *Discrete-Time Signal Processing*, 3rd Editio. Prentice Hall, 2009.

[62] A. Mirzaei, M. Mikhemar, D. Murphy, and H. Darabi, "A 2 dB NF receiver with 10 mA battery current suitable for coexistence applications," *IEEE Journal of Solid-State Circuits*, vol. 49, no. 4, pp. 972–983, 2014.

[63] H. Zhang and E. Sánchez-Sinencio, "Linearization techniques for CMOS low noise amplifiers: A tutorial," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 58, no. 1, pp. 22–36, 2011.

[64] I. Madadi, M. Tohidian, and R. B. Staszewski, "A TDD/FDD SAW-Less Superheterodyne Receiver with Blocker-Resilient Band-Pass Filter and Multi-Stage HR in 28nm CMOS," in *Symposium on VLSI Circuits, Dig. of Tech. Papers*.

[65] I. Madadi, M. Tohidian, and R. B. Staszewski, "A High IIP2 SAW-Less Superheterodyne Receiver with Multi-Stage Harmonic Rejection," *under review in IEEE Journal of Solid-State Circuits*, 2015.

[66] F. Bruccoleri, E. a M. Klumperink, and B. Nauta, "Wide-band CMOS low-noise amplifier exploiting thermal noise canceling," *IEEE Journal of Solid-State Circuits*, vol. 39, no. 2, pp. 275–282, 2004.

[67] W. Zhuo, X. Li, S. Shekhar, S. H. K. Embabi, J. Pineda de Gyvez, D. J. Allstot, and E. Sanchez-Sinencio, "A capacitor cross-coupled common-gate low-noise amplifier," *IEEE Transactions on Circuits and Systems II: Express Briefs*, vol. 52, no. 12, pp. 875–879, 2005.

[68] F. Bruccoleri, E. a M. Klumperink, and B. Nauta, "Generating all two-MOS-transistor amplifiers leads to new wide-band LNAs," *IEEE Journal of Solid-State Circuits*, vol. 36, no. 7, pp. 1032–1040, 2001.

[69] S. Chehrazi, A. Mirzaei, and A. A. Abidi, "Second-Order Intermodulation in Current-Commutating Passive FET Mixers," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 56, no. 12, pp. 2556–2568, 2009.

[70] I. Fabiano, M. Sosio, A. Liscidini, and R. Castello, "SAW-Less Analog Front-End Receivers for TDD and FDD," *IEEE Journal of Solid-State Circuits*, vol. 48, no. 12, pp. 3067–3079, Dec. 2013.

[71] M. Da Tsai, C. F. Liao, C. Y. Wang, Y. Bin Lee, B. Tzeng, and G. K. Dehng, "A multi-band inductor-less SAW-less 2G/3G-TD-SCDMA cellular receiver in 40nm CMOS," in *IEEE International Solid-State Circuits Conference - (ISSCC) Digest of Technical Papers*, 2014, vol. 57, pp. 354–355.

[72] D. Murphy, H. Darabi, and H. Xu, "Noise-cancelling receiver with enhanced resilience to harmonic blockers," *IEEE International Solid-State Circuits Conference - (ISSCC) Digest of Technical Papers*, vol. 57, no. June 2013, pp. 68–69, 2014.

[73] A. Mirzaei, H. Darabi, and D. Murphy, "A low-power process-scalable superheterodyne

receiver with integrated high-Q filters," in *IEEE International Solid-State Circuits Conference*, 2011, pp. 60 – 62.

[74] D. B. Leeson, "A simple model of feedback oscillator noise spectrum," *Proceedings of the IEEE*, vol. 54, no. 2, pp. 329–330, 1966.

[75] A. Mazzanti and P. Andreani, "Class-C harmonic CMOS VCOs, with a general result on phase noise," *IEEE Journal of Solid-State Circuits*, vol. 43, no. 12, pp. 2716–2729, 2008.

[76] P. Andreani, X. Wang, L. Vandi, and A. Fard, "A study of phase noise in colpitts and LC-tank CMOS oscillators," *IEEE Journal of Solid-State Circuits*, vol. 40, no. 5, pp. 1107–1118, 2005.

[77] E. Hegazi, H. Sjoland, and A. A. Abidi, "A filtering technique to lower oscillator phase noise," *IEEE Journal of Solid-State Circuits*, vol. 36, no. 12, pp. 1921–1930, 2001.

[78] M. Tohidian, A. Fotowat-Ahmadi, M. Kamarei, and F. Ndagijimana, "High-swing class-C VCO," in *European Solid-State Circuits Conference (ESSCIRC)*, 2011, pp. 495–498.

[79] W. Deng, K. Okada, and A. Matsuzawa, "Class-C VCO with amplitude feedback loop for robust start-up and enhanced oscillation swing," *IEEE Journal of Solid-State Circuits*, vol. 48, no. 2, pp. 429–440, 2013.

[80] M. Tohidian, S. A.-R. Ahmadi-Mehr, and R. B. Staszewski, "Dual-core high-swing class-C oscillator with ultra-low phase noise," in *IEEE Radio Frequency integrated Circuits (RFIC) Symposium - Digest of Papers*, 2013, pp. 243–246.

[81] S. A.-R. Ahmadi-Mehr, M. Tohidian, and R. B. Staszewski, "Frequency translation through fractional division for a two-channel pulling mitigation," in *European Solid-State Circuits Conference (ESSCIRC)*, 2013, pp. 241–244.

[82] S. A. R. Ahmadi Mehr, M. Tohidian, and R. B. Staszewski, "Toward Solving Multichannel RF-SoC Integration Issues Through Digital Fractional Division," *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, vol. PP, no. 99, pp. 1–1, 2015.

[83] L. Fanori and P. Andreani, "Highly efficient class-C CMOS VCOs, including a comparison with class-B VCOs," *IEEE Journal of Solid-State Circuits*, vol. 48, no. 7, pp. 1730–1740, 2013.

[84] P. Kinget, M. Hill, W. Sansen, J. Huijsing, and R. Plassche, "Integrated GHz Voltage Controlled Oscillator," in *Analog Circuit Design: (X)DSL and Other Communication Systems; RF MOST Models; Integrated Filters and Oscillators*, W. Sansen, J. Huijsing, and R. van de Plassche, Eds. Boston, MA: Kluwer, 1999, pp. 353–381.

[85] T. S. D. Cheung and J. R. Long, "Shielded passive devices for silicon-based monolithic microwave and millimeter-wave integrated circuits," in *IEEE Journal of Solid-State Circuits*, 2006, vol. 41, no. 5, pp. 1183–1200.

[86] L. Fanori and P. Andreani, "A high-swing complementary class-C VCO," in *European*

Solid-State Circuits Conference, 2013, pp. 407–410.

[87] K. Kwok and H. C. Luong, "Ultra-low-voltage high-performance CMOS VCOs using transformer feedback," *IEEE Journal of Solid-State Circuits*, vol. 40, no. 3, pp. 652–660, 2005.

[88] L. Aspemyr and D. Linten, "An ultra low voltage, low power, fully integrated VCO for GPS in 90 nm RF-CMOS," *Analog Integrated Circuits and Signal Processing*, vol. 46, no. 1, pp. 57–63, 2006.

[89] H. H. Hsieh and L. H. Lu, "A high-performance CMOS voltage-controlled oscillator for ultra-low-voltage operations," *IEEE Transactions on Microwave Theory and Techniques*, vol. 55, no. 3, pp. 467–473, 2007.

[90] S. A.-R. Ahmadi-Mehr, M. Tohidian, and R. B. Staszewski, "Breaking the Phase Noise Performance Limits by Coupling Multiple Oscillators," *under review in IEEE Transactions on Circuits and Systems I: Regular Papers*, 2015.

[91] A. Rofougaran, J. Rael, M. Rofougaran, and A. A. Abidi, "A 900 MHz CMOS LC-oscillator with quadrature outputs," *IEEE International Solid-State Circuits Conference (ISSCC) - Digest of Technical Papers*, vol. 14, no. 5, pp. 392–393, 1996.

[92] M. Babaie and R. B. Staszewski, "A class-F CMOS oscillator," *IEEE Journal of Solid-State Circuits*, vol. 48, no. 12, pp. 3120–3133, 2013.

[93] A. Visweswaran, R. B. Staszewski, and J. R. Long, "A clip-and-restore technique for phase desensitization in a 1.2V 65nm CMOS oscillator for cellular mobile and base stations," in *IEEE International Solid-State Circuits Conference - Digest of Technical Papers*, 2012, vol. 55, pp. 350–351.

[94] L. Fanori, A. Liscidini, and P. Andreani, "A 6.7-to-9.2GHz 55nm CMOS hybrid Class-B/Class-C cellular TX VCO," in *IEEE International Solid State Circuits Conference - Digest of Technical Papers*, 2012, vol. 55, no. 3, pp. 354–355.

[95] J. Steinkamp, F. Henkel, P. Waldow, O. Pettersson, C. Hedenäs, and B. Medin, "A Colpitis oscillator design for a GSM base station synthesizer," in *IEEE Radio Frequency integrated Circuits (RFIC) Symposium - Digest of Papers*, 2007, pp. 405–408.

[96] C. M. Hung, R. B. Staszewski, N. Barton, M. C. Lee, and D. Leipold, "A digitally controlled oscillator system for SAW-less transmitters in cellular handsets," *IEEE Journal of Solid-State Circuits*, vol. 41, no. 5, pp. 1160–1169, 2006.

[97] O. Nizhnik, R. K. Pokharel, H. Kanaya, and K. Yoshida, "Low noise wide tuning range quadrature ring oscillator for multi-standard transceiver," *IEEE Microwave and Wireless Components Letters*, vol. 19, no. 7, pp. 470–472, 2009.

[98] B. Fahs, W. Y. Ali-Ahmad, and P. Gamand, "A two-stage ring oscillator in 0.13-µm CMOS for UWB impulse radio," *IEEE Transactions on Microwave Theory and Techniques*, vol. 57, no. 5, pp. 1074–1082, 2009.

[99] S. Yoo, J. J. Kim, and J. Choi, "A 2-8 GHz Wideband Dually Frequency-Tuned Ring-VCO With a Scalable KVCO," *IEEE Microwave and Wireless Components Letters*, vol. 23, no. 11, pp. 602–604, 2013.

[100] L. Kong and B. Razavi, "A 2.4GHz 4mW inductorless RF synthesizer," in *IEEE International Solid-State Circuits Conference (ISSCC) - Digest of Technical Papers(ISSCC) Digest of Technical Papers*, 2015, pp. 450–451.

[101] T.-H. Tsai, M.-S. Yuan, C.-H. Chang, C.-C. Liao, C.-C. Li, and R. B. Staszewski, "A 1.22ps integrated-jitter 0.25-to-4GHz fractional-N ADPLL in 16nm FinFET CM0S," in *IEEE International Solid-State Circuits Conference - (ISSCC) Digest of Technical Papers*, 2015, pp. 260–261.

[102] M. Tohidian, S. A.-R. Ahmadi-Mehr, and R. B. Staszewski, "A Tiny Quadrature Oscillator Using Low-Q Series LC Tanks," *IEEE Microwave and Wireless Components Letters*, vol. 25, no. 8, 2015.

[103] J. Savoj and B. Razavi, "A 10-Gb/s CMOS clock and data recovery circuit with a half-rate binary phase/frequency detector," *IEEE Journal of Solid-State Circuits*, vol. 38, no. 1, pp. 13–21, 2003.

[104] J. E. Rogers and J. R. Long, "A 10-Gb/s CDR/DEMUX with LC delay line VCO in 0.18-μm CMOS," *IEEE Journal of Solid-State Circuits*, vol. 37, no. 12, pp. 1781–1789, 2002.

[105] B. Razavi, "A Study of Phase Noise in CMOS Oscillators," *IEEE Journal of Solid-State Circuits*, vol. 31, no. 3, pp. 331–343, 1996.

[106] P. Andreani, A. Bonfanti, L. Romanò, and C. Samori, "Analysis and design of a 1.8-GHz CMOS LC quadrature VCO," *IEEE Journal of Solid-State Circuits*, vol. 37, no. 12, pp. 1737–1747, 2002.

[107] A. Mazzanti and F. Svelto, "A 1.8-GHz injection-locked quadrature CMOS VCO with low phase noise and high phase accuracy," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 53, no. 3, pp. 554–560, 2006.

[108] G. Li and E. Afshari, "A low-phase-noise multi-phase oscillator based on left-handed LC-ring," *IEEE Journal of Solid-State Circuits*, vol. 45, no. 9, pp. 1822–1833, 2010.

[109] T. Nakamura, T. Norimatsu, T. Uozumi, K. Ueda, and T. Yamawaki, "A ΔΣ-modulator-less digitally-controlled oscillator using fractional capacitors for GSM/EDGE transmitter," in *European Solid-State Circuits Conference (ESSCIRC)*, 2012, pp. 410–413.

Summary

In a radio-frequency (RF) system-on-chip (SoC), a digital baseband/application processor, which occupies most of the silicon area, determines the SoC fabrication process technology and voltage supply. The rest of the circuitry, including RF front-end and frequency synthesizer, must then adopt the chosen process technology, i.e., presently low-voltage deep *nano-scale CMOS*. To design a *fully integrated* power/area efficient *receiver* in this respect, new RF/analog techniques are required to be able to function well at the reduced voltage headroom. In addition, new oscillator structures need to be developed that can work at low supply voltages and in face of poor quality current sources while providing high spectral purity.

On the other hand, conventional RF/analog designs have not benefited significantly from CMOS scaling, which continually reduces transistor cost and improves digital performance. Here in this thesis, traditional continuous-time (CT) analog components, such as opamps, are avoided and, instead, most of signal processing and filtering is done using passive switched-capacitor circuits in *discrete-time* (DT) domain. In this way, the receiver front-end becomes process scalable similar to digital circuits enjoying performance and cost improvements with each process scaling node.

In the first part of this dissertation, principles, design and implementation of a fully integrated DT *superheterodyne* receiver frontend are described. To start with, the optimal sampling scheme in a high-intermediate frequency (IF) receiver architecture is explained. It is followed by sequentially introducing all the constituent circuits. A novel DT high-order low-pass filter is proposed to be used at the receiver baseband. This filter has an exceptionally low noise and high linearity. Deep analysis, verified by test-chip measurements, is presented. Next, a very high

sampling rate DT bandpass filter (BPF) using I/Q charge sharing is proposed and analyzed. Then, a novel wideband noise-cancelling LNTA is proposed with a two-fold noise cancellation technique. Finally, a fully integrated DT superheterodyne receiver is proposed with explanations to its DT model, frequency translations, and image rejection mechanisms. The whole idea, design and analyses are successfully verified by a 65-nm CMOS test chip. The implemented receiver has an exceptional high uncalibrated IIP2 of +90 dBm.

In the second part of this dissertation, design and implementations of low-voltage fully integrated oscillators in nano-scale CMOS are discussed. First, a high-swing class-C oscillator is proposed that efficiently uses the drastically reduced supply voltage in nano-scale CMOS. Measurement results of a low-power low-voltage test chip in 90-nm CMOS shows phase noise figure-of-merit as high as 192 dBc/Hz from a 0.6V power supply. The idea of the high-swing class-C oscillator is extended to an ultra-low phase noise dual-core oscillator implemented in 65nm CMOS. This oscillator is the first-ever fully integrated design that meets phase noise requirements of a GSM basestation standard in a bulk CMOS technology. Next, another novel low-voltage oscillator topology is proposed that uses a series-LC tank ring structure. Its realization in 40-nm CMOS targets low silicon area using low-Q inductors. It exhibits 7–20 dB better phase noise than other state-of-the-art low area oscillators.

Samenvatting

Bij een radio system-on-chip (SoC), bepaalt de digitale baseband/application processor, die het grootste deel van de chip in beslag neemt, het SoC fabricage proces en de voedingsspanning. De rest van het circuit, zowel het front-end als de synthesizer, moeten dan aangepast worden t.b.v het gekozen proces, in dit geval het low-voltage deep nano-scale CMOS. Om vanuit deze benadering een volledig geïntegreerde vermogen/oppervlak efficiente ontvanger te ontwerpen, zijn nieuwe RF/analoge technieken nodig om het goed te laten functioneren in de verkleinde spanningsruimte. Daarvoor moeten nieuwe oscillator structuren worden ontwikkeld die kunnen werken bij lage voedingsspanningen en stroombronnen van slechte kwaliteit waarbij een hoge spectrale zuiverheid wordt geleverd.

Anderzijds, hebben conventionele RF/analoge ontwerpen de voortschrijdende transistor kosten verlaging en digitale prestatie verbetering van CMOS schaling niet erg benut. In dit proefschrift worden traditionele continue tijd (CT) analoge componenten, zoals opamps, vermeden en in plaats daarvan wordt het grootste deel van signaalverwerking en filtering gedaan d.m.v. van passieve switch-capacitor circuits in het discrete tijd (DT) domein. Op deze manier wordt het front-end van de ontvanger naar elk proces schaalbaar vergelijkbaar met digitale schakelingen waarbij prestatie en kosten verbeteren met iedere proces schalingsstap.

In het eerste deel van dit proefschrift worden de principes, het ontwerp en de implementatie van een complete geïntegreerde superheterodyne ontvanger frontend beschreven. Om te beginnen wordt de optimale bemonstering regeling van een hoge middenfrequentie (IF) ontvangerarchitectuur uitgelegd. Daarna worden achtereenvolgens de samenstellende circuit geïntroduceerd. Een nieuw DT hoge orde laagdoorlaatfilter wordt getoond dat wordt gebruikt

bij de ontvanger basisband. Dit filter heeft een uitzonderlijk laag ruis niveau en een grote lineariteit. Uitgebreide analyses, gecontroleerd door Test-chip metingen worden getoond. Vervolgens wordt een banddoorlaatfilter (BPF) met een zeer hoge bemonsteringsfrequentie DT voorgesteld en geanalyseerd, dat gebruik maakt van I/Q lading verdeling. Hierna wordt een nieuwe breedband-noise-cancelling LNTA geïntroduceerd met een twee voudige ruisonderdrukking techniek. Tot slot wordt een volledig geïntegreerde DT superheterodyne ontvanger getoond met uitleg over zijn DT model, de frequentie translatie en het beeld onderdrukkingsmechanisme. Het hele idee, ontwerp en analyses zijn, met succes, geverifieerd d.m.v. een 65-nm CMOS-test chip. De geïmplementeerde ontvanger heeft een uitzonderlijk hoge ongekalibreerd IIP2 van +90 dBm.

In het tweede deel van dit proefschrift, worden ontwerpen en implementaties van compleet geïntegreerde low-voltage oscillatoren in nano-schaal CMOS besproken. Als eerste wordt een grote zwaai klasse-C oscillator beschreven die efficiënt gebruik maakt van de aanzienlijk lagere spanning in nano-schaal CMOS. Meetresultaten van een, laag vermogen en lage spanning, test chip in 90 nm CMOS toont verdienstelijke waarden als 192 dBc/Hz bij een voedingsspanning van 0,6 V. Het idee van de grote zwaai klasse-C oscillator is overgezet naar een ultra-lage fase ruis dual-core-oscillator geïmplementeerd in 65nm CMOS. Deze oscillator is het allereerste volledig geïntegreerd ontwerp dat aan faseruis eisen, van een GSM-basisstation standaard, voldoet in een bulk CMOS-technologie. Verder wordt een nieuwe lage spanning oscillator topologie geïntroduceerd dat gebruik maakt van een LC serie kring. De realisatie ervan in 40-nm CMOS mikt op een laag silicium gebied voor gebruik van lage Q spoelen. Dit geeft 7-20 dB betere fase ruis dan andere nieuwste lage gebied oscillatoren.

List of Publications

Journal Papers

M. Tohidian, I. Madadi, and R. B. Staszewski, "A Fully Integrated Discrete-Time Superheterodyne Receiver," under review in *IEEE Transactions on Circuits and Systems I: Regular Papers*, 2015.

M. Tohidian, S. A.-R. Ahmadi-Mehr, and R. B. Staszewski, "A Tiny Quadrature Oscillator Using Low-Q Series LC Tanks," *IEEE Microwave and Wireless Components Letters*, vol. 25, no. 8, August 2015.

M. Tohidian, I. Madadi, and R. B. Staszewski, "Analysis and Design of a High-Order Discrete-Time Passive IIR Low-Pass Filter," *IEEE Journal of Solid-State Circuits*, vol. 49, no. 11, pp. 2575 – 2587, 2014.

I. Madadi, **M. Tohidian**, and R. B. Staszewski, "A High IIP2 SAW-Less Superheterodyne Receiver with Multi-Stage Harmonic Rejection," under review in *IEEE Journal of Solid-State Circuits*, 2015.

I. Madadi, **M. Tohidian**, and R. B. Staszewski, "Analysis and Design of I/Q Charge-Sharing Band-Pass-Filter for Super-Heterodyne Receivers," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol 62, no. 8, pp. 2114-2121, 2015.

S. A.-R. Ahmadi-Mehr, **M. Tohidian**, and R. B. Staszewski, "Towards Solving Multi-channel RF-SoC Integration Issues Through Digital Fractional Division," *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, vol. PP, no. 99, 2015.

S. A.-R. Ahmadi-Mehr, **M. Tohidian**, and R. B. Staszewski, "Breaking the Phase Noise Performance Limits by Coupling Multiple Oscillators," under review in *IEEE Transactions on Circuits and Systems I: Regular Paper*, 2015.

Conference Proceedings

M. Tohidian, I. Madadi, and R. B. Staszewski, "A fully integrated highly reconfigurable discrete-time superheterodyne receiver," in *IEEE International Solid-State Circuits Conference (ISSCC) -Digest of Technical Papers*, 2014, pp. 72–73.

M. Tohidian, I. Madadi, and R. B. Staszewski, "A 2mW 800MS/s 7th-order discrete-time IIR filter with 400kHz-to-30MHz BW and 100dB stop-band rejection in 65nm CMOS," in *IEEE International Solid-State Circuits Conference (ISSCC) - Digest of Technical Papers*, 2013, vol. 56, pp. 174–175.

M. Tohidian, S. A.-R. Ahmadi-Mehr, and R. B. Staszewski, "Dual-core high-swing class-C oscillator with ultra-low phase noise," in *IEEE Radio Frequency integrated Circuits (RFIC) Symposium - Digest of Papers*, 2013, pp. 243–246.

M. Tohidian, A. Fotowat-Ahmadi, M. Kamarei, and F. Ndagijimana, "High-swing class-C VCO," in *European Solid-State Circuits Conference (ESSCIRC)*, 2011, pp. 495–498.

I. Madadi, **M. Tohidian**, and R. B. Staszewski, "A TDD/FDD SAW-Less Superheterodyne Receiver with Blocker-Resilient Band-Pass Filter and Multi-Stage HR in 28nm CMOS," in *Symposium on VLSI Circuits, Dig. of Tech. Papers*, 2015.

I. Madadi, **M. Tohidian**, and R. B. Staszewski, "A 65nm CMOS high-IF superheterodyne receiver with a High-Q complex BPF," in *IEEE Radio Frequency Integrated Circuits Symposium (RFIC)*, 2013, pp. 323–326.

S. A.-R. Ahmadi-Mehr, **M. Tohidian**, and R. B. Staszewski, "Frequency translation through fractional division for a two-channel pulling mitigation," in *European Solid-State Circuits Conference (ESSCIRC)*, 2013, pp. 241–244.

Patents and Patent Applications

M. Tohidian, I. Madadi, and R. B. Staszewski, "High order discrete time charge rotating passive infinite impulse response filter," US 20140354376 A1, Published Dec. 2014.

M. Tohidian, I. Madadi, and R. B. Staszewski, "Superheterodyne Receiver," US 20140194081 A1, Published Jul. 2014.

M. Tohidian, I. Madadi, and R. B. Staszewski, "Radio Frequency Receiver," US 20140171009 A1, Published Jun. 2014.

M. Tohidian, I. Madadi, and R. B. Staszewski, "DISCRETE-TIME FILTER," US 20150214926 A1, Published July 2015.

M. Tohidian, R. B. Staszewski, A. Fotowat Ahmady, S. A.-R. Ahmadi-Mehr, M. Kamarei, and F. Ndagijimana, "Quadrature LC Tank Digitally Controlled Ring Oscillator," U.S. Patent Application No. 14/547,868, Filed Jul. 2014.

I. Madadi, **M. Tohidian**, and R. B. Staszewski, "High-IF superheterodyne receiver incorporating high-Q complex band pass filter," US9014653 B2, Issued Apr. 2015.

I. Madadi, **M. Tohidian**, and R. B. Staszewski, "A CHARGE SHARING FILTER," Europe Patent Office Application No. PCT/EP2014/068892, Filed Sept. 2014.

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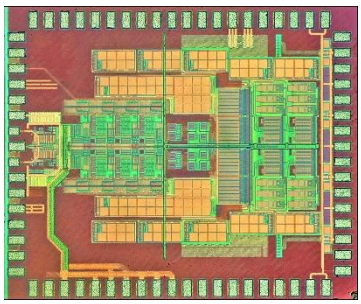
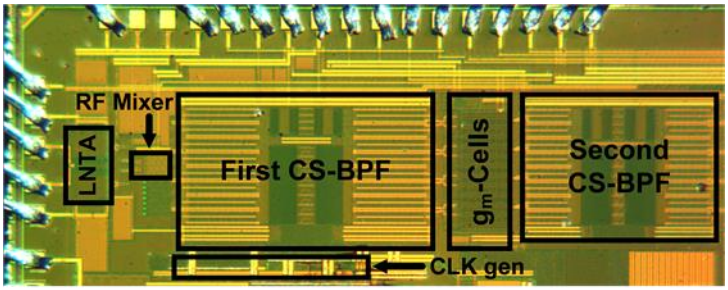
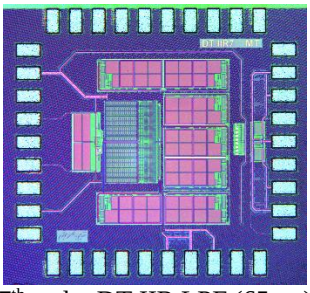


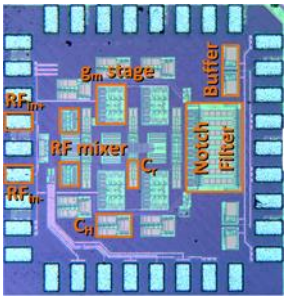
DT Superheterodyne RX (65nm)



SAW-Less DT Superheterodyne RX (28nm)



7^{th}-order DT IIR LPF (65nm)



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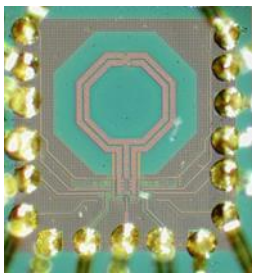
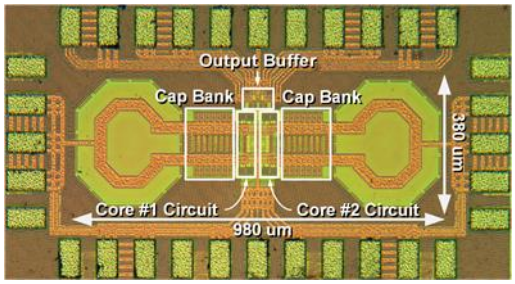
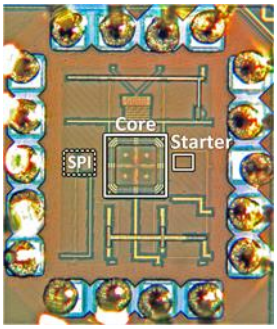


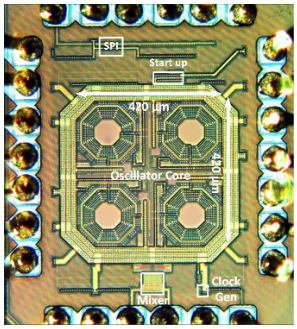
High-Swing Class-C Oscillator (90nm)



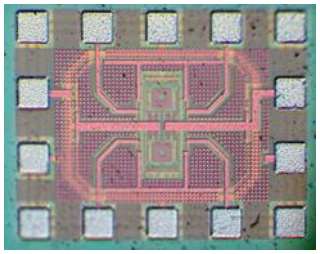
Dual-Core High-Swing Class-C Oscillator (65nm)



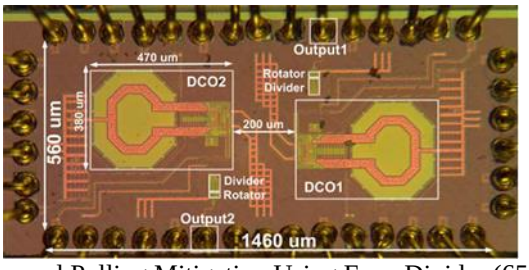
Tiny Quad. Osc. Using Low-Q Series LC (40nm)



Series LC Quad. Oscillator (40nm)



Tiny Quad. Osc. Using Low-Q Series LC (90nm)



2-Channel Pulling Mitigation Using Frac. Divider (65nm)

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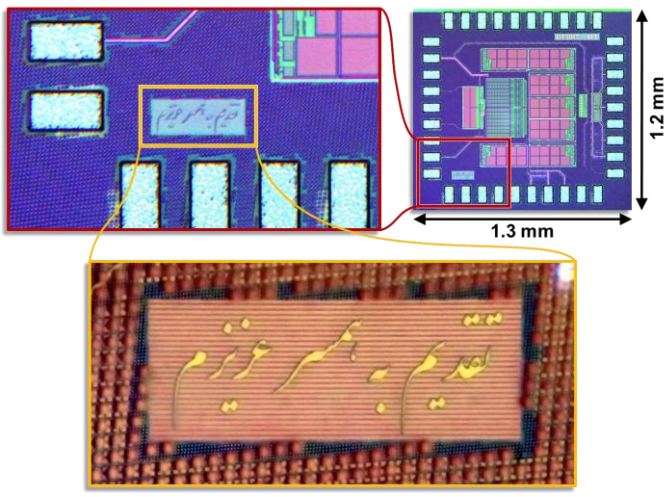

Metal artwork: “To my dear wife”
(in Persian, written in Nastaliq script)

About the Author

Massoud Tohidian received the B.S. and M.S. degrees in electrical engineering (with honors) from Ferdowsi University of Mashhad and University of Tehran, Iran, in 2007 and 2010, respectively. He was a researcher in IMEP-LAHC Laboratory, Grenoble, France, in 2009–2010. In late 2010, he commenced his Ph.D. work in Microelectronics at Delft University of Technology, The Netherlands. He was a consultant at M4S/Huawei, Leuven, Belgium, in 2013–2014, designing a 28-nm SAW-less receiver chip for mobile phones. His research interest includes analog and RF integrated circuits and systems for wireless communications. He holds seven patents and patent applications in the field of RF-CMOS design.