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A Highly Efficient Fully Integrated Active Rectifier for Ultrasonic Wireless Power Transfer

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***Abstract*—Ultrasonic wireless power transfer (WPT) has been proved to be a promising approach to power biomedical implants. To extract the energy generated from the transducer, a rectifier is typically required. Previous inductor-based rectifiers (SSHI and SECE) require a large off-chip inductor to achieve good performance, which is not desired for miniaturization and safety reasons. Synchronized switch harvesting on capacitors (SSHC) rectifiers have been proved to achieve high performance without inductors; however, they are mainly designed for low-frequency kinetic energy harvesting. In this paper, an improved SSHC rectifier is designed to achieve a fully integrated design with all flying capacitors implemented on-chip. The proposed SSHC rectifier can properly operate at ultrasonic excitation frequency ($100\,\mathrm{KHz}$) with precise switching time control and ultrafast voltage flipping techniques. In addition, an on-chip ultralow-power LDO allows the system to be self-sustained. The system is designed in a TSMC 180nm BCD technology and post-layout simulation results are presented.**

***Index Terms*—Biomedical application, energy harvesting, fully integrated, integrated circuit, SSHC rectifier, ultrasonic transducer**

I. Introduction

In recent years, piezoelectric energy harvesting (PEH) has been applied in various applications, especially in wireless sensors, biomedical implantable devices and wearable electronics [1]. For a PEH system, system miniaturization and energy efficiency are the key factors. In order to realize miniaturization, MEMS process is extensively used to fabricate PEHs. The energy efficiency depends on the performance of the used rectifier. A typically used rectifier in a PEH system is the full-bridge rectifier (FBR) for its stability and simplicity. In addition, a FBR does not depend on power supply to operate; therefore, it does not consider cold-startup ability. However, the high voltage threshold for a FBR significantly curtails the output energy efficiency [2]. In order to improve the efficiency, the Synchronized Switch Harvesting on Inductor (SSHI) rectifier was introduced to flip the voltage across the piezoelectric transducer (PT) by employing an inductor [3]–[6].

On one hand, the SSHI can enhance the performance by employing an inductor to form a RLC loop. On the other hand, the inductance is required around $10\,\mathrm{mH}$, which is not benefit for the system miniaturization, hence, the inductor should be replaced without decreasing the performance. Afterwards, the Synchronized Switch Harvesting on Capacitors (SSHC) rectifier was put forward. Several small switch capacitors were employed to replace the inductor for system miniaturization [7]. However, in previous typical SSHC systems, due to large intrinsic capacitance of PT, the required switch capacitors are too large to be put on a chip. Afterwards, the split-electrode (SE) SSHC rectifier was put forward to achieve fully integrated on-chip [8]. While the SE-SSHC requires thick oxide transistors in the CMOS process. Additionally, a typical SSHC rectifier is mainly designed for low-frequency kinetic energy harvesting, because the required operating period for a SSHC demands adequate time.

The system diagram is displayed in Fig. 1. In this work, as shown in Fig. 1, the ultrasonic PT is composed of an AC current I_P and in parallel with a capacitor C_P. A fully integrated SSHC rectifier is proposed in a standard CMOS process. This is the first time for all the flying capacitors to be implemented on-chip thanks to the small inherent capacitance of ultrasonic PTs. The running ultrasonic excitation frequency is $100\,\mathrm{KHz}$ which desires precise switching time control. A low-dropout (LDO) circuit provides a power supply (VDD) for the proposed transistors, so self-powered system is available. Post layout simulation results are presented to verify the system performance.

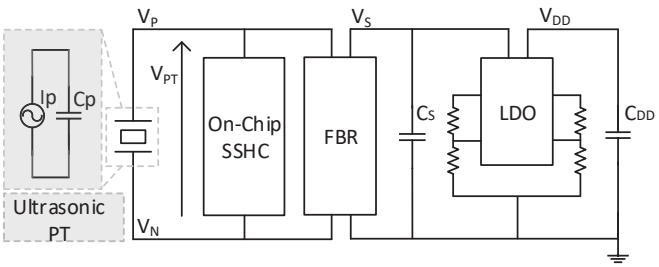

Fig. 1. System Diagram

The structure of this paper is organized as follows: Section II presents the SSHC rectifier in ultrasonic application. Section III shows the circuit implementation. Section IV shows the post-layout simulation results analysis of this proposed system. Finally, a conclusion is given in Section V.

II. SSHC Interface Circuit Analysis

A. Typical SSHC rectifier

The system architecture of the SSHC rectifier is shown in Fig. 2. There are k capacitors and every capacitor is controlled by 4 switches. When the PT voltage flips from positive to negative, the controlled signals are sequenced as

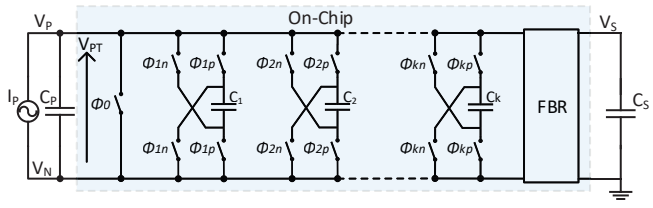

Fig. 2. SSHC Rectifier

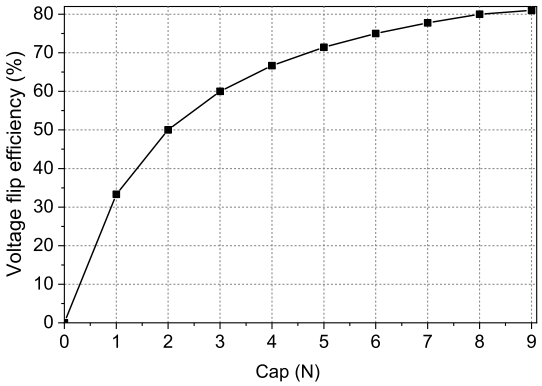

Fig. 3. Voltage flip efficiency related to different number of employed capacitors

$\phi_{1p} \rightarrow \phi_{2p} \rightarrow \ldots \rightarrow \phi_{kp-1} \rightarrow \phi_{kp} \rightarrow \phi_0 \rightarrow \phi_{kn} \rightarrow \phi_{kn-1} \rightarrow \cdots \rightarrow \phi_{2n} \rightarrow \phi_{1n}$. The charge in PT are dumped to the k capacitors when the first k phases are operating. Then, ϕ_0 clears the left charge after dumping. The last k phases are used to transfer the charge in the k capacitors to the PT in an opposite direction.

When we use 8 capacitors (k=8) as the flying capacitors, and every capacitance is the same as the intrinsic capacitance of PT, C_P, the flip efficiency is shown in Fig. 3. Fig. 3 shows that with the increasing numbers of capacitor the flip efficiency is also improved. The efficiency is 33% with one flying capacitor and 80% with 8 flying capacitors.

Generally, as shown in Fig 3, for the purpose of achieving high flipping efficiency, it is required to employ capacitance of C_K as same as C_P at least. However, C_P of typical PT is in nano-Farah level resulting in several tens nano-Farah level in total for the required flying capacitors. These flying capacitors are too large to be fully integrated on-chip which is bad for system miniaturization. Afterwards, SE-SSHC was proposed for the purpose of achieving fully integrated by dividing a monolithic PT into several pieces [8]. Although SE-SSHC provides a good method to put these capacitors on-chip, it has to use the thick oxide process for the switches and this is not preferred for a standard CMOS process.

B. SSHC in ultrasonic wireless power transfer

Despite a typical SSHC rectifier is hard to realize fully integrated on-chip, when PTs are used in ultrasonic wireless power transfer, the ultrasonic PTs usually have very small intrinsic capacitance. The size of the ultrasonic PT is not exceed cubic millimeter level in general. While the resonant frequency is above $100\,\mathrm{KHz}$, and the C_P is around $100\,\mathrm{pF}$. When the flying capacitors, C_K, is equal to C_P, the total capacitance is around $800\,\mathrm{pF}$ for a 8-stage SSHC rectifier, which is accessible to fully integrate on-chip. In the measurement, as long as the effective input C_P is smaller than $100\,\mathrm{pF}$, the system performance would not be affected [9]. The benefit of size and flipping time consideration are given as follows.

a) Size analysis: When the system is designed in a TSMC $180\,\mathrm{nm}$ BCD process, we can use the metal-insulator-metal (MIM) capacitor as the flying capacitor. The density of MIM capacitor is $2\,\mathrm{fF}/\mu\mathrm{m}^2$. Considering that when $C_P = 100\,\mathrm{pF}$, the area for the total capacitance of 8 flying capacitors is around $0.5\,\mathrm{mm}^2$. Area cannot be directly compared between a SSHC rectifier and a SSHI rectifier. The estimated minimum volume of this SSHC rectifier should be smaller than $1\,\mathrm{mm}^3$. While considering the same flip efficiency, when using a SSHI rectifier with a several millihenry inductor, the total occupied volume is at least several hundreds times larger than the proposed SSHC rectifier.

b) Flipping time analysis: On the other hand, due to the resonant frequency of the ultrasonic PT is $100\,\mathrm{KHz}$ which indicates $1000\times$ higher than a typical PT. The vibration period is $10\,\mu\mathrm{s}$. Thus, the flipping cycle for the PT voltage is only $5\,\mu\mathrm{s}$. When PT voltage changes the polarity, it is required to finish flipping in a period which is much less than the flipping cycle to avoid excessive energy wasting. In this design, we propose that the flipping time for the SSHC rectifier is no more than 15% of the flipping period.

III. Circuit Implementations

This section presents the system architecture of the proposed ultrasonic PT receiver and a selection of key functional blocks in the system. The top level architecture of the design is given in Fig. 4, which contains a pulse generation block, a pulse sequencing block, a on-chip SSHC rectifier, a FBR and an on-chip voltage regulator. The FBR rectifies the received energy from AC to DC while generating a synchronized signal, SYN, which indicates the moment to start voltage flipping. This signal is fed into the pulse generator to generate a sequence of pulses. In this implementation, 8 on-chip flying capacitors require 17 pulses generation in total. These 17 pulses are then sequenced in the pulse sequencing block according to current voltage polarity. The sequenced pulses are level shifted to correct voltage levels to fully drive the switch arrays to perform voltage flipping.

A. Full-bridge rectifier

The FBR block plays a key role to rectify the energy and provide the SYN signal. The circuit diagram of the FBR is given by Fig. 5, which includes a FBR consisting of four MOSFETs and an active diode M_0 controlling by a comparator. The output signal of the comparator, SYN, indicates whether the FBR is conducting or not. When the

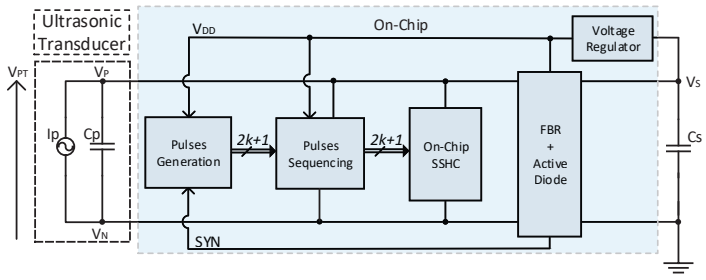

Fig. 4. System Architecture

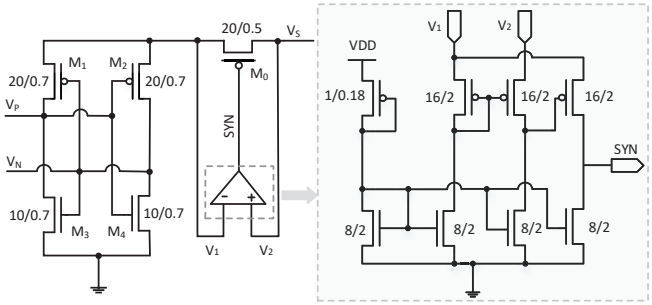

Fig. 5. Full-bridge Rectifier

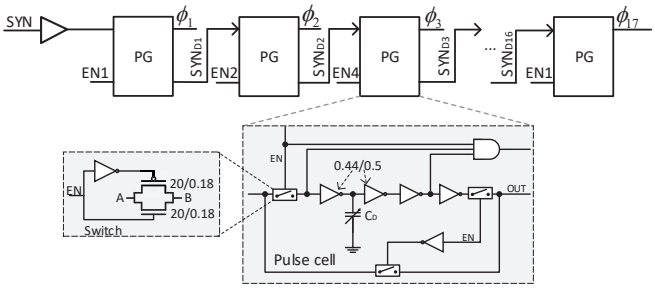

Fig. 6. Pulse Generation Cell

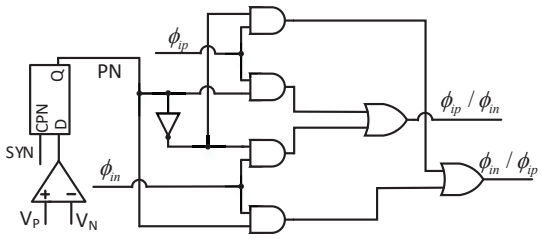

Fig. 7. Sequencing Cell

voltage across the PT needs to be flipped, this is also the moment that the PMOS M_0 is turned OFF to cut off the FBR conduction. At this moment, a rising edge in SYN is generated, which indicates the FBR enters the non-conducting mode and the voltage across the PT needs to be flipped. This rising in SYN is fed into a pulse generation block.

B. Pulse generation

The pulse generation block is shown in Fig. 6, which contains 17 pulse generation cells to generate 17 sequential pulses: ϕ_1 to ϕ_{17}. The first pulse generation cell triggered by a rising edge of SYN. Each pulse generation cell simply ANDs the input with a delayed and inverted version of the input to generate a pulse. The pulse-width can be adjusted by tuning the the variable capacitor C_D to avoid excessive or insufficient flipping time caused by process deviation or parasitic parameter. An enable signal, EN, is added to bypass selected cells if less pulses are required for less enable flying capacitors.

C. Pulse sequencing

The generated 17 pulses are then fed into the pulse sequencing block, which contains 9 pulse sequencing cells. Fig. 7 shows the circuit diagram of one sequencing cell, which takes the i^{th} pulse and the $(17-i)^{th}$ together with a PN signal to sequence the two pulses according to the polarity of PN. The signal PN is generated according to the polarity of the voltage across the PT (V_P and V_N) before flipping is performed, and circuit for generating this signal is also shown at the left of the Figure. After this block, all the 17 pulses are sequenced to drive the switch array (as shown in Fig. 2) for PT voltage flipping by controlling 8 capacitors which are implemented on-chip thanks to the ultra-small inherent capacitance of the ultrasonic PT.

IV. Post-Layout Simulation Analysis

The system is designed in a 180nm BCD process. The piezoelectric ultrasonic transducer used in the simulation has the inherent capacitor, $C_P = 100\,\text{pF}$, and the excitation ultrasonic frequency is set at $100\,\text{KHz}$, which matches the natural frequency of the transducer. Fig. 8 shows that designed layout. The open circuit voltage, V_{OC}, is $2\,\text{V}$. The LDO provides a 1.5-V power supply for the transistors, so the system achieves self-powered sustained. The active area is $0.74\,\text{mm}^2$. Additionally, compared with [8], for the same 8-stage SSHC design with the same technology, the SE-SSHC rectifier takes up $3.9\,\text{mm}^2$, which is above 5.3 $\times$ larger than the proposed design in this work. Different from [8], all transistors used in this design are standard process which means that no thick oxide transistor is employed.

Fig. 9 shows the simulated waveform of V_{PT}. When there are 8 switched capacitors, 17 pulses are required to control

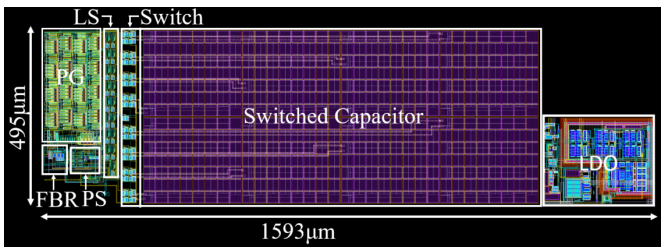

Fig. 8. Layout: PG-Pulse Generation; LS-Level Shifter; PS-Pulse Sequencing

TABLE I
DIFFERENT PERFORMANCE COMPARISON WITH PREVIOUS WORK

Publications	Technique	C_P	$V_{OC}(V)$	F (Hz)	Inductor	On-Chip	Volume (mm^3)	$Power_{Max}$ (μW)	Density($\frac{Power}{Area}$)
ISSCC'16 [12]	SSHI	26nF	2.45	134	3.3mH	No	15.9	160.7	10
TPEL'16 [11]	SECE	52nF	2.35	60	560μH	No	3.5	35	10
ISSCC17 [10]	FCR	78.4pF	1	110K	No	Yes	1.7	50.2	30
JSSC'17 [7]	SSHC	45nF	2.5	92	No	No	1.6	161.8	101
ISSCC'18 [8]	SSHC	1.94nF	2.5	219	No	Yes	5.38	16	2.97
This work	**SSHC**	**100pF**	**2**	**100K**	**No**	**Yes**	**0.74**	**197**	**266**

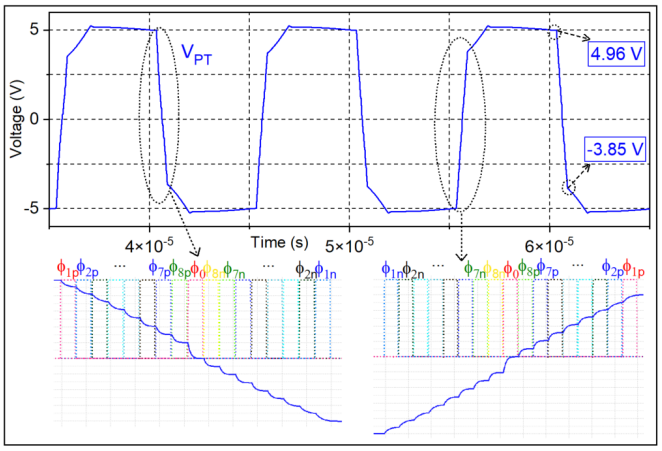

Fig. 9. Waveform of V_{PT} with 80% flip efficiency

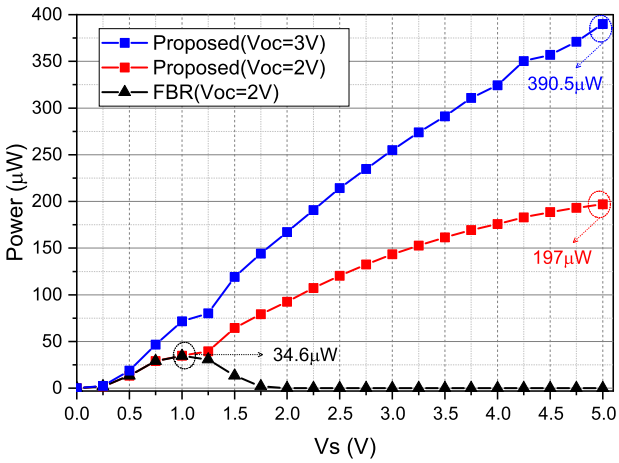

Fig. 10. Different output power comparisons of a FBR and the proposed method

these capacitors. As shown in the Fig. 9, the V_{PT} can be flipped from $4.96\,\mathrm{V}$ to $-3.85\,\mathrm{V}$. The flip efficiency is 78%. The left sub-window shows that When V_{PT} flips from positive to negative, ϕ_{1p}, ϕ_{2p}, ..., ϕ_{8p} are used to dump the charge from PT to the flying capacitors sequentially. ϕ_0 is used to clear the residual charge in PT. ϕ_{8n}, ϕ_{7n}, ..., ϕ_{1n} are employed to dump the charge from switched capacitors to the C_P. When V_{PT} changes from negative to positive, these pulses work in a reverse sequence as shown at the right sub-window. Every phase takes up $35\,\mathrm{ns}$, which is above $800\times$ smaller than the one in a typical PT ($29\,\mu\mathrm{s}$). Thus, it requires a more precision switching control than the typical design. The total flipping time of these phases is $0.6\,\mu\mathrm{s}$ which is 11.9% of the flipping period.

Fig. 10 displays the output power of the FBR and proposed design. When $V_{OC} = 2\,\mathrm{V}$, the maximum output power of the FBR is $34.6\,\mu\mathrm{W}$ and approaches to 0 at $V_S = 2\,\mathrm{V}$. While the maximum output power of the proposed SSHC rectifier is $197\,\mu\mathrm{W}$ at $V_S = 5\,\mathrm{V}$, which is $5.7\times$ larger than the FBR. When increase V_{OC} to $3\,\mathrm{V}$, the maximum output power reach $390.5\,\mathrm{uW}$ at $V_S = 5\,\mathrm{V}$ and it is high enough to power sensors and other wireless devices.

Table I displays the different performance comparisons with previous work. The second left column shows the technique used in different works. The next three columns show the parameters of the used PT model, where the C_P is the inherent capacitance of the PT and V_{OC} is the open circuit voltage of the PT. The output power can be increased with a larger V_{OC}. The resonant frequency, F, of this work is $100\,\mathrm{KHz}$ which is relatively high compared with most papers. There is no inductor employed in this work and eight on-chip capacitors are used to flip PT voltage. The total active area is $0.74\,\mathrm{mm}^2$ which is the smallest fully integrated SSHC rectifier. In order to compare this design with other works in volume, especially with SSHI rectifiers, it is assumed $1\,\mathrm{mm}$ for the height. Thus the volume is $0.74\,\mathrm{mm}^3$. The maximum output power when $V_{OC} = 2\,\mathrm{V}$ is $197\,\mu\mathrm{W}$ which is the highest output among these works although with relatively low V_{OC}. The effective density represents the ration of the maximum power over the active area. This work has the highest output power density at $266\mu W/mm^3$.

V. CONCLUSION

This work investigates a fully integrated active SSHC rectifier with standard CMOS technology in ultrasonic PT application. The resonant frequency of employed ultrasonic PT is $100\,\mathrm{KHz}$ which is $1000\times$ larger than a typical PT. The intrinsic capacitor, C_P, is $100\,\mathrm{pF}$ which provides the possibility to fully integrate the flying capacitors on a chip. 8 flying capacitors are employed to achieve 80% flip efficiency to improve the power efficiency. The simulated maximum output power is $390.5\,\mu\mathrm{W}$ with $V_{OC} = 3\,\mathrm{V}$ and is able to power the biomedical implants.

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