Delft University of Technology

Master Thesis

Transceiver design for reciprocal operation of ultrasonic flow measurement systems

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Transceiver design for reciprocal operation of ultrasonic flow measurement systems

by

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TU Delft

Abstract

In transit-time ultrasonic flow measurement systems, the system's ability to operate reciprocally in the absence of flow is a highly desirable property. If the reciprocity is lacking in the system, any time delay that appears between the upstream and downstream signals at zero-flow conditions will result in false flow measurement. This phenomenon is known as the zero-flow error.
This thesis presents a system in which the reciprocity property has been ensured by matching the electrical impedances of the front-end electronic circuits, namely: the output impedance of the transmitter Z_{out} and the input impedance of the receiver Z_{in}. To achieve this, a circuit has been developed that can be used as both a transmitter and a receiver. This is the main feature that distinguishes the proposed design from those presented in previous work. The transmitter-receiver circuit has been implemented using a three-stage operational amplifier in unity gain feedback configuration. The class AB output stage of the amplifier is equipped with an additional function being used in receive mode for sensing and amplification of the signal. The simulation result obtained by the cross-correlation method yields a zero-flow error value of 30 fs, which is at least by three orders of magnitude smaller than the results achieved in prior work. The input and output impedances are equal to Z_{in}=73.2$\angle$80.7^{o} mΩ and Z_{out}=79.6$\angle$77.3^{o} mΩ respectively. A small mismatch remaining between the impedances prevents perfect reciprocity to be established in the system. A prototype IC has been taped out in TSMC 0.18 µm BCD Gen2 technology.

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Contents

1 Introduction **1**
1.1 Flow measurement system description . . . 1
1.2 Problem definition . . . 2
1.3 Project objective . . . 2
1.4 Thesis organization . . . 2

2 Flow measurement system analysis **3**
2.1 Transducer model . . . 3
2.2 Frequency behavior of the transducer . . . 4
2.3 Flow measurement system model . . . 5
2.4 Reciprocity conditions . . . 8
2.5 Zero-flow error . . . 10

3 Architecture-level analysis and design **13**
3.1 Transmitter topology . . . 13
3.1.1 Pulser as transmitter . . . 13
3.1.2 Buffer as transmitter . . . 17
3.2 Receiver topology . . . 19
3.3 Excitation signal waveform . . . 20

4 Circuit-level analysis and design **23**
4.1 Design of the output stage . . . 23
4.1.1 Class A output stage . . . 23
4.1.2 Class AB output stage . . . 26
4.2 Design of the loop amplifier . . . 28
4.3 Frequency compensation . . . 31
4.4 Receiver design . . . 34
4.5 Noise analysis . . . 36
4.6 Overall performance . . . 38

5 IC design **41**
5.1 Pinout diagram . . . 41
5.2 Layout . . . 41
5.3 Post-layout simulation . . . 43

6 Conclusions **45**

Bibliography **47**

1

Introduction

In many industrial applications, precise measurement of the flow velocity of a fluid running through a pipeline remains a critical issue to address. Obtaining more accurate measurement results would allow industrial plants to better control the amount of material required for a particular process, which would yield an increase of the efficiency and an improvement of the product quality. Given that consumers are billed based on flow meter readings, they can also benefit from precise measurements. Their monthly payment for utility products like water and gas will be reduced, leading to cost savings.

1.1. Flow measurement system description

A widely-used way to determine flow velocity is based on measuring the transit-time difference between an acoustic pulse travelling upstream and a pulse travelling downstream through the fluid. The simple drawing shown in Figure 1.1 explains the working principle of such a transit-time flow measurement system.

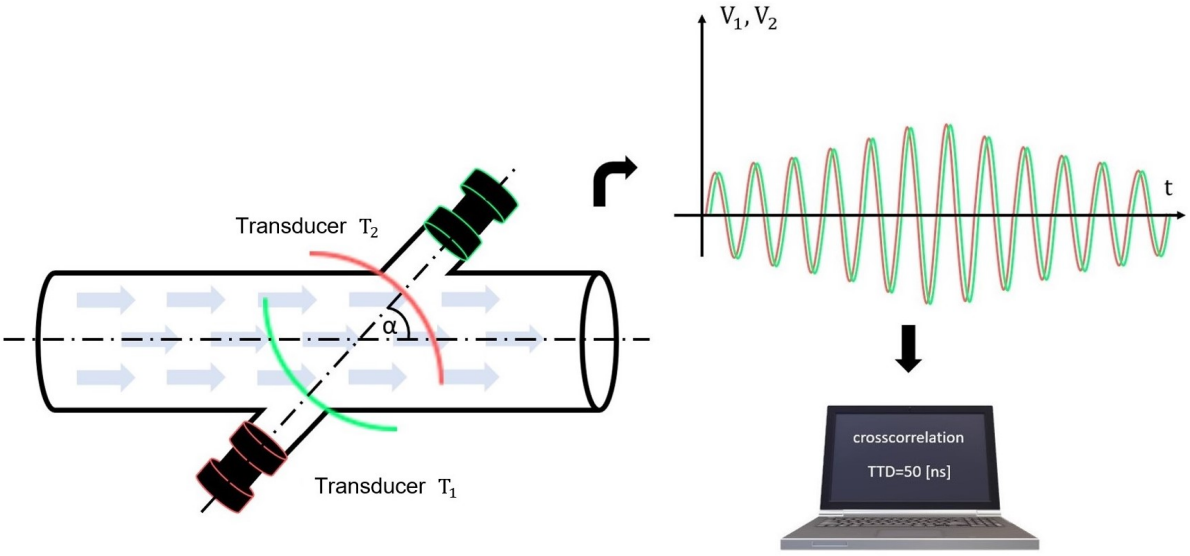


Figure 1.1: Transit-time ultrasonic flow measurement system.

It is assumed that a fluid flows through the pipe. The arrowheads indicate the direction of the flow. At both sides of the pipe two piezoelectric transducers T_1 and T_2 are placed. The sensors are built into the pipe and positioned on opposite sides facing each other under an angle α. To measure the flow rate, the transducers are driven by transmitter circuits, causing two acoustic signals to be sent: the signal from T_1 to T_2 is called the downstream signal, the signal from T_2 to T_1 is called the upstream signal.

The transmitted signals travel through the medium and, having reached the opposite side, are sensed by the same sensors. The received signals are usually first conditioned by means of an amplifier and, after having been digitized, undergo further processing. It is obvious that the signal sent in the flow direction propagates more quickly than the signal sent against the direction of the flow. Therefore, as shown in the figure, there will be a time shift between the received signals V_1 and V_2, which is proportional to the velocity of the flow. One of the methods used to determine this time difference is the cross-correlation method. The algorithm is based on the displacement of one of the signals relative to the other so that the best matching between the signals is found. The obtained result is known as the transit-time difference (TTD). Its value can be converted into the flow rate, which in turn is used to calculate the volume of the transported medium.

1.2. Problem definition

In an ideal situation, when T_1 and T_2 are perfectly matched and the front-end circuits at both sides are identical, the system behaves reciprocally in the absence of flow. In this case, the received signals V_1 and V_2 are equal and the result of the cross-correlation would be a zero TTD value. In the real situation, this is not exactly the case. Since T_1 and T_2 are manufactured in mass production, their parameters are not identical. Moreover, there is a difference in the characteristics of the transmitter and the receiver circuits caused by the design. Due to these reasons, the reciprocity in the system is violated. Having a transducer imbalance and a mismatch between the circuits results in a false flow measurement at zero-flow conditions. This is called the zero-flow error. In fact, the error also appears in the presence of non-zero flow in the pipe, causing measurement error. Using ‘‘dry calibration’’ is one way to get rid of the zero-flow error. However, since its value can be sensitive to process variations (e.g. pressure, fluid properties, temperature), the calibration fails if the system isn’t able to respond immediately to these changes. Re-calibration may require additional effort and time. In order to prevent the zero-flow error from being dominant in low-velocity measurements, a minimum limit is usually specified, at which the accuracy specification can be met for a particular flow meter. As an example, for a flow meter to be able to detect the flow velocity in the interval 0.1-100 m/s with an accuracy of 5%, it is required for the zero-flow error to be less than 0.18 ns [1].
The system designs presented in [2], [3] succeeded in keeping the zero-flow error in a wide range from hundreds of picoseconds to tens of nanoseconds. Obviously, reducing the zero-flow error, let alone removing it completely from the system, is highly desirable.

1.3. Project objective

An analysis of ultrasonic flow measurement system, including the acoustic behavior of the signals and the impact of finite-valued electrical impedances of the transmitter and the receiver, has been carried out in [4]. The obtained results show that for the system to be reciprocal it is sufficient that the output impedance of the transmitter and the input impedance of the receiver are matched. In this case, the zero-flow error can be minimized, regardless of the difference between the transducers. The objective of this master thesis is to investigate how the choice of impedances affects the zero-flow error and to design a system consisting of a transmitter and a receiver, in which the zero-flow error will remain below 100 ps.

1.4. Thesis organization

This thesis report is intended to get familiar with the work done. Starting from a global system analysis, the reader is taken step by step through the design procedure, including investigation aspects aimed at achieving the assigned objective. The thesis is divided into 5 chapters which are organized as follows. Chapter 2 presents a simplified electrical model of the flow measurement system used to derive the conditions for the reciprocal operation of the system. In chapter 3 two different configurations of the transmitter circuit are considered. The configuration of the receiver circuit is completely based on that of the transmitter and is therefore presented in chapter 4 after the implementation of the transmitter at the transistor-level. In chapter 5 the layout of the developed IC and the post-layout simulations are briefly presented. In the concluding chapter, all results achieved are summarized.

2

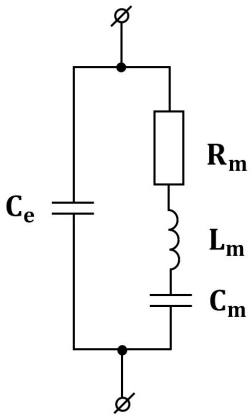
Flow measurement system analysis

This chapter provides an in-depth look at the flow measurement system. The chapter begins with the discussion of the piezoelectric transducer. An equivalent circuit model and the parameters of the transducer are first presented, followed by its frequency behavior. After that, a model of the flow measurement system is introduced and its operation in the non-reciprocal conditions is explored. The chapter concludes with a derivation and an analysis of the conditions that can make the system work in a reciprocal way.

2.1. Transducer model

Figure 2.1a [1] shows a pair of transducers used in the flow measurement system. These are air-backed transducers, which were built by using Pz27 piezo-ceramic discs with a diameter of 10 mm and a thickness of 1 mm. The electrical impedance of the transducers is modelled with a simple Butterworth van-Dyke circuit model, shown in Figure 2.1b [5].

(a) Piezoelectric transducers.



(b) The Butterworth van-Dyke circuit model.

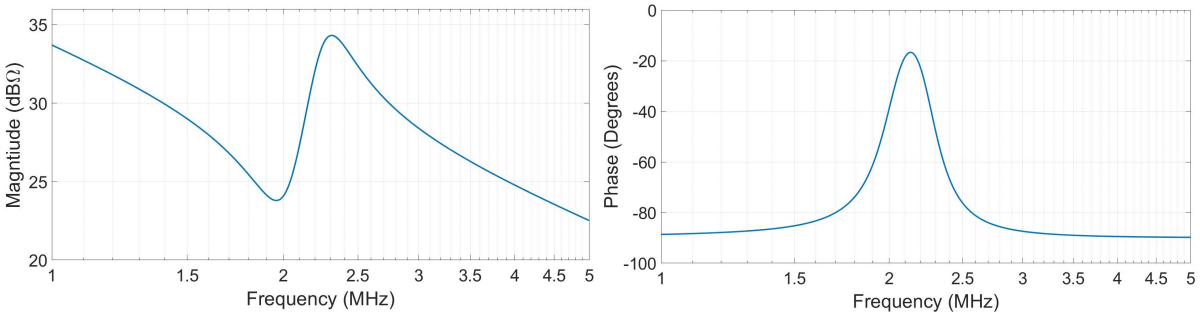
Figure 2.1: Pair of piezoelectric transducers and their equivalent circuit model.

The model comprises a parallel connection of the capacitance C_e and a series branch composed of the resistance R_m, the inductance L_m and the capacitance C_m. The RLC branch describes the dynamic behavior of the energy transfer from the electrical to the mechanical domain. The capacitance C_e represents the capacitance of the dielectric material and any other externally connected device. The model parameters have been obtained from an impedance measurement of a 20 mm diameter Pz27 transducer and they are given in Tab. 2.1 [5].

Table 2.1: Fitted parameters of the Butterworth van-Dyke model.

R_m	L_m	C_m	C_e
20 Ω	10.3 µH	0.6 nF	2.5 nF

As can be seen, the parasitic capacitance C_e is quite big. Therefore it is apparent that when the transducer operates as a transmitter, the voltage source that is used to drive it, will be heavily loaded by this capacitance. The value of R_m is small. Hence, when the transducer is used as a receiver, its thermal noise contribution to the entire system will be also small. A simulated impedance characteristic of the transducer is illustrated in Figure 2.2.



(a) Magnitude. **(b)** Phase.

Figure 2.2: Simulated electrical impedance characteristics of the piezo-electrically resonator targeted in this work..

There are two distinct resonance points in the plot. The first one appears at 2 MHz. It corresponds with series resonance, when the impedances of L_m and C_m cancel each other out, leaving only the purely ohmic impedance R_m. The transducer's impedance at this point is minimal and the resonance frequency is given by [6]:

$$f_s = \frac{1}{2\pi \cdot \sqrt{L_m \cdot C_m}} \tag{2.1}$$

The second point occurs around 2.2 MHz. It indicates parallel resonance, when the equivalent impedance of the series-connected L_m and C_m gets inductive and equal to that of C_e. The transducer's impedance at this point hits its maximum value and the resonance frequency is estimated by [6]:

$$f_p = \frac{1}{2\pi \cdot \sqrt{L_m \cdot \frac{C_m + C_e}{C_m \cdot C_e}}} \tag{2.2}$$

2.2. Frequency behavior of the transducer

The resonance frequency of the transducer is influenced by the resistance of the source that is used to drive it [5]. Figure 2.3 shows a transducer being driven by an excitation source modelled with a Thévenin equivalent circuit consisting of the voltage source V_s and a variable resistance Z_s. The transmitted acoustic signal is represented by the current I_m. Figure 2.4 shows the magnitude and the phase of the transmitted signal for different values of Z_s, which vary from 100 mΩ to 1 kΩ.
There are three clear regions to observe in the frequency plot:

- For small values of Z_s the transducer is in series resonance. This region covers the range from 0 to 10 Ω. The resonance frequency keeps almost constant throughout this region except for the values where Z_s approaches the upper limit of the interval;

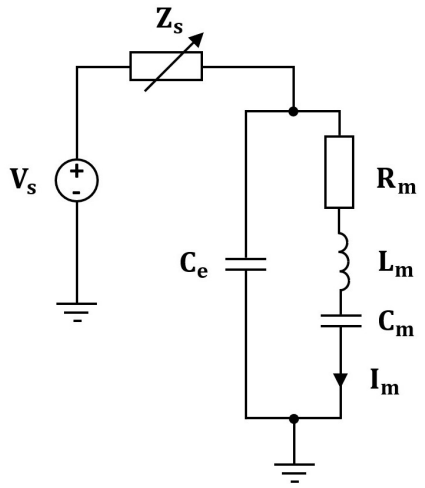
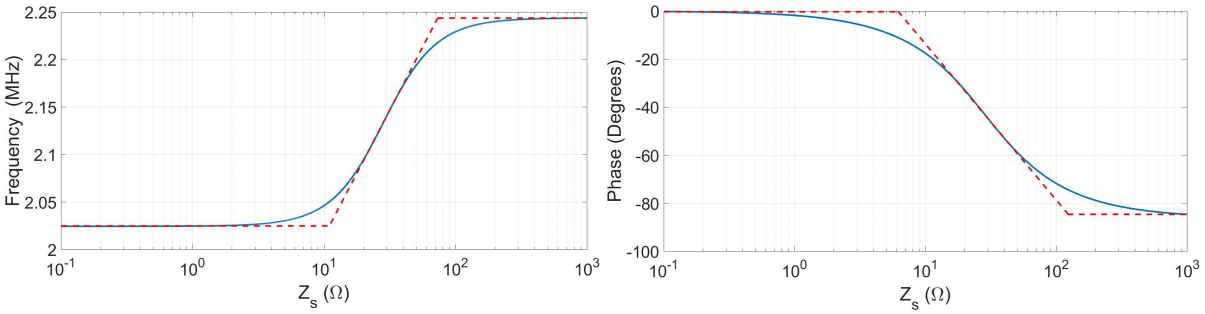


Figure 2.3: Excitation source modeled with a Thévenin equivalent and piezo transducer represented by Butterworth van-Dyke model.



(a) Frequency versus Z_s.

(b) Phase versus Z_s.

Figure 2.4: Resonance frequency and phase of the transmitted signal I_m for different values of the source impedance Z_s.

- For large values of Z_s, starting from 70 Ω, the transducer is in parallel resonance. The resonance frequency also remains unchanged in this region as long as Z_s is at least a factor of 3 larger than the lower interval limit;
- The slope connecting these two regions indicates the transition zone where the values of Z_s stay in proximity of R_m. The resonance frequency in this region is the most sensitive to the change of Z_s. Therefore a small variation of the source impedance results in a visible change of the resonance frequency.

A similar behavior is observed in the phase plot. For small and large values of Z_s the phase is almost constant, while in the transition region it shows the dependency of Z_s. Therefore, if one would want the transducer to oscillate at a fixed frequency, then the output resistance of the excitation source should be significantly smaller or significantly larger than the transducer's impedance itself. In this case, a small variation of the output impedance, commonly present in a non-ideal source, will not result in a significant change of the resonance frequency.

2.3. Flow measurement system model

In order to model the complete measurement system, the two transducers are modelled together. A distinction is made between the upstream and downstream measurements by modeling the signal paths separately. The received signals are processed by a matlab script resulting in a zero-flow error value. The electrical model of the flow measurement system is shown in Figure 2.5.

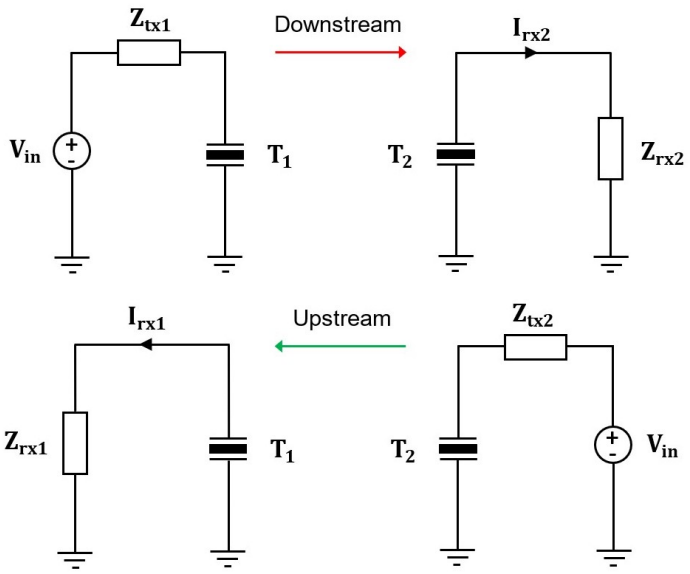


Figure 2.5: Electrical model of the flow measurement system.

Transmitter 1 is presented by a Thévenin equivalent circuit consisting of the voltage V_{in} and a resistance Z_{tx1}. The voltage source V_{in} causes transducer 1 (T1) to oscillate and as a result, the downstream signal is being transmitted. The signal progresses through the medium and it is received by transducer 2 (T2), that develops current I_{rx2}. This current is sensed by receiver 2, which is modelled by the resistance Z_{rx2}. This could be the input resistance of an amplifier that is commonly needed in order to raise the signal magnitude to a desired value. The path of the upstream signal is similar to that of the downstream signal: T2 is driven by transmitter 2 represented by Z_{tx2} and V_{in}, receiver 1 modelled by Z_{rx1} senses the signal I_{rx1} received by T1. The signal transfer between the transducers is modeled as shown in Figure 2.6 [1].

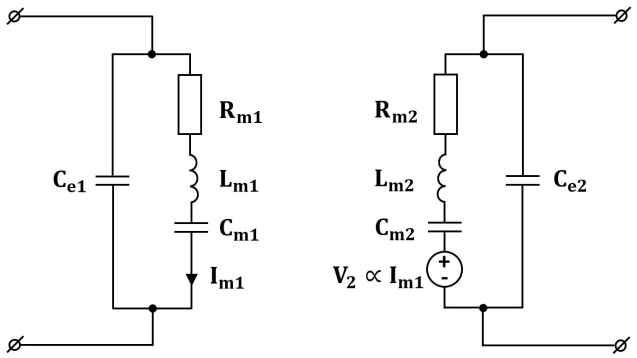
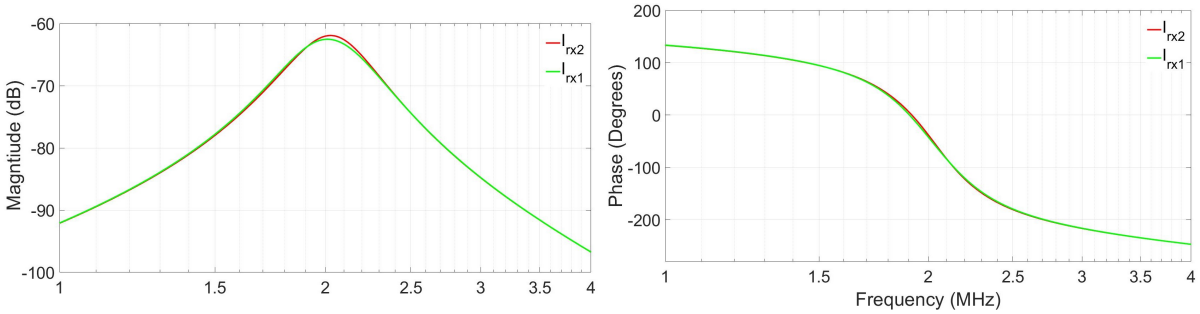


Figure 2.6: Electrical model for the signal transfer between the transducers in the downstream direction.

The current-controlled voltage source (CCVS) V_2 generates a signal in the RLC branch of the receive transducer, whose value is proportional to the current I_{m1} drawn by the RLC branch of the transmit transducer. Since the transducers are manufactured in batch production, they are not identical and thus there is always a mismatch between their parameters. The supplier website states that the standard tolerance of the resonance frequency between the transducers is $\pm 5\%$ [7]. During the simulation the mismatch between T_1 and T_2 is modelled by increasing the value of C_{m2} by 10%.
In addition to the mismatch between the transducers, there is a difference between the values of the output impedance of the transmitter $Z_{tx1,2}$ and the input impedance of the receiver $Z_{rx1,2}$. This is due to the fact that the transmitter and the receiver are implemented by completely different circuits, which are usually made separately, and therefore their parameters generally don't match. To simulate the worst case, $Z_{tx1,2}$ and $Z_{rx1,2}$ are chosen from the transition region in Figure 2.4 to be equal to 10 Ω and

20 Ω respectively. For the sake of the model simplicity they are chosen to be frequency-independent. In a practical system this does not always have to be the case, since the impedances tend to change from the resistive to the capacitive or the inductive behavior at high frequencies such as the resonance frequency of the transducer. Equating Z_{tx1} and Z_{tx2} as well as Z_{rx1} and Z_{rx2} implies that the transducers are driven by the same transmitter and are sensed by the same receiver. The switching circuitry doing that is not shown in the circuit.
Figure 2.7 depicts the bode plot of the transfer functions I_{rx1}/V_{in} and I_{rx2}/V_{in}. As can be seen, both transducers are in series resonance. This is a result of the low values of Z_{tx} and Z_{rx}.



(a) Magnitude.

(b) Phase.

Figure 2.7: Frequency-domain signals of the simulated received upstream and downstream signals I_{rx1} and I_{rx2}, the test conditions: Z_{tx1}=Z_{tx2}=10 Ω and Z_{rx1}=Z_{rx2}=20 Ω.

Moreover, the plot also shows some visible differences between the currents:

- there is a slight shift between the resonance frequencies f_{res} of the signals;
- the values of the gain at f_{res} are different and the shape of the gain plot around f_{res} is not exactly the same;
- there is a mismatch in the phase plot around f_{res}.

This plot reveals that the system operates in nonreciprocal conditions. The reason for that is obvious: the difference between Z_{tx} and Z_{rx} and the mismatch between the transducers themselves. The result of working in nonreciprocal conditions can also be seen in the time-domain in Figure 2.8, where the impulse response of I_{rx1} and I_{rx2} is shown.

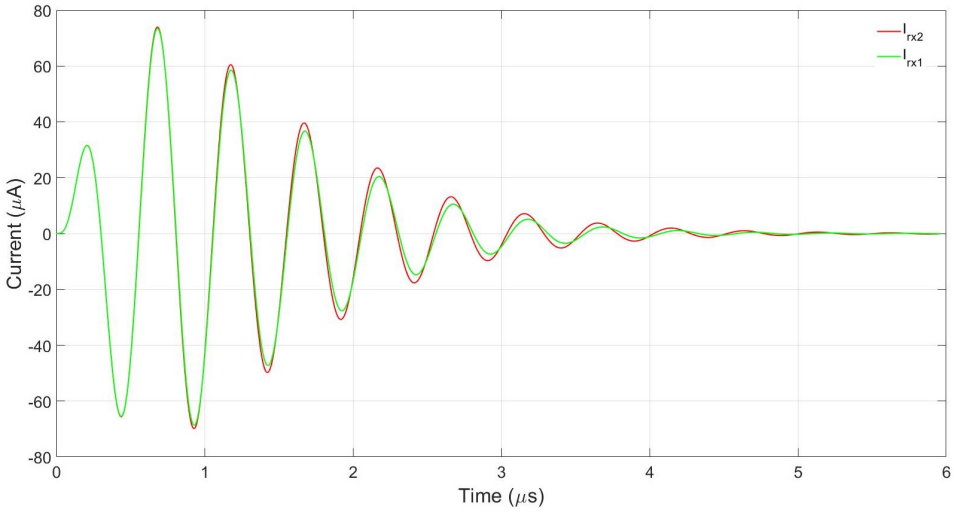


Figure 2.8: Time-domain impulse response of the upstream and downstream signals I_{rx1} and I_{rx2}, the test conditions: Z_{tx1}=Z_{tx2}=10 Ω and Z_{rx1}=Z_{rx2}=20 Ω.

In this plot all observations mentioned in the frequency-domain contribute to the deviation of I_{rx1} from I_{rx2}. At the beginning the signals seem to be matched but after a short time they start to depart from each other. It is remarkable that the longer the signals propagate, the more they differ from each other. It is clear, if one would apply cross-correlation on these two signals, a zero-flow error would be found. A reciprocal operating of the system implies currents I_{rx1} and I_{rx2} to be matched.

2.4. Reciprocity conditions

As has been shown in Section 2.3, any inequality between the parameters of the transmitter and the receiver as well as between T1 and T2 is highly undesired. The prior work [4] shows that if the difference between Z_{tx} and Z_{rx} or the mismatch between T1 and T2 could be eliminated, there would not be any difference between I_{rx1} and I_{rx2} and as a result, the zero-flow would be equal to zero.
There is no simple way to match the transducers. If one would try to do that, then first the difference would have to be measured and second, this difference would have to be compensated. This way of reducing the zero-flow error is not quite suitable for a system in which various transducers are used.
Requiring some conditions to the values of Z_{tx} and Z_{rx} is another way to achieve reciprocity in the flow measurement system. These requirements will be derived from the following analysis.
Figure 2.9 shows the model of the flow measurement system where the transducers have been replaced by the Butterworth van-Dyke circuit model. It is assumed that the coupling coefficient γ is the same in both directions and equal to 1.

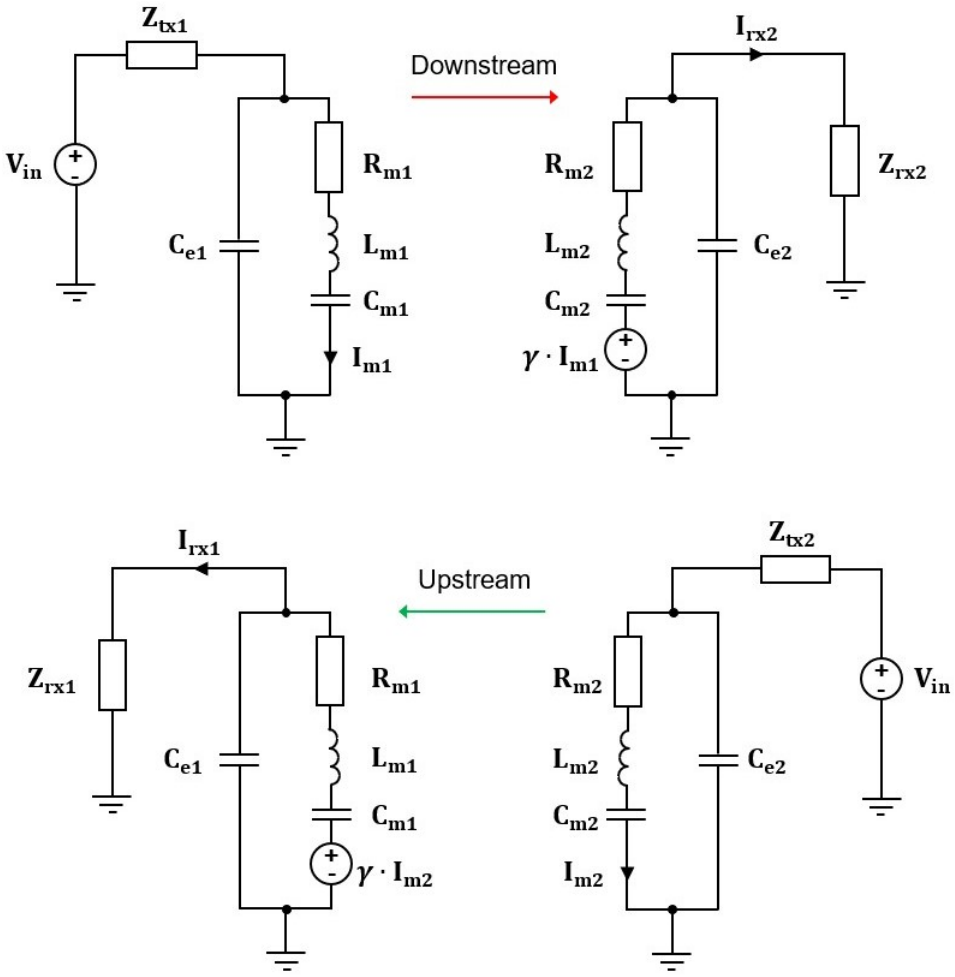


Figure 2.9: Electric model of the flow measurement system where the transducer have been replaced with the Butterworth van-Dyke model.

Using the Laplace transform yields the impedance of the transmit transducer:

$$Z = \frac{Z_e \cdot Z_m}{Z_e + Z_m}, \tag{2.3}$$

where Z_e and Z_m are the impedances of the parasitic capacitance C_e and the series branch RLC, which are given by:

$$Z_e = \frac{1}{s \cdot C_e} \tag{2.4}$$

$$Z_m = R_m + s \cdot L_m + \frac{1}{s \cdot C_m} \tag{2.5}$$

By applying the voltage/current divider formula and the Ohm's law, the transfer functions of the received currents I_{rx1} and I_{rx2} are obtained:

$$I_{rx1} = \frac{k}{(Z_{tx2} + Z_2) \cdot (Z_{rx1} + Z_1)} \cdot V_{in} \tag{2.6}$$

$$I_{rx2} = \frac{k}{(Z_{tx1} + Z_1) \cdot (Z_{rx2} + Z_2)} \cdot V_{in}, \tag{2.7}$$

where k is given by:

$$k = \frac{Z_{e1} \cdot Z_{e2}}{(Z_{m1} + Z_{e1}) \cdot (Z_{m2} + Z_{e2})} \tag{2.8}$$

As mentioned earlier, the currents I_{rx1} and I_{rx2} are always matched when the system operates in reciprocal conditions. This implies that the transfer functions of I_{rx1} and I_{rx2} should be equal. An analysis of Eq. (2.6) and (2.7) shows that this would be the case if the resistances Z_{rx1}, Z_{rx2}, Z_{tx1}, and Z_{tx2} fulfill some conditions:

- The output impedance of the transmitter and the input impedance of the receiver are the same:

$$Z_{tx1} = Z_{tx2} = Z_{rx1} = Z_{rx2} \tag{2.9}$$

- Or, more general, the output impedance of transmitter 1 is equal to the input impedance of receiver 1 while the output impedance of transmitter 2 is equal to the input impedance of receiver 2:

$$Z_{tx1} = Z_{rx1} \quad \text{and} \quad Z_{tx2} = Z_{rx2} \tag{2.10}$$

Though these conditions equate I_{rx1} and I_{rx2}, regardless of the mismatch between T1 and T2, this is not quite easy to achieve in practice. The impedances Z_{tx} and Z_{rx} can always slightly differ from each other as a result of using different topologies for the transmitter and the receiver. Moreover, if the resistance of the former changes in some interval, the resistance of the latter does not generally change in the same manner. Thus, any small deviation between Z_{tx} and Z_{rx} will lead to an increase of the zero-flow error. The conditions can also be worsened by parasitic impedances arising at the places where the chip is mounted to the circuit board. Condition (2.9) implies the use of the same transmitter and the

receiver for the downstream and the upstream signal. To do this an additional switching network is needed.
Unlike (2.9), condition (2.10) does not require the impedances at both sides to be equal. A resistance matching at one side is sufficient and it is independent on the matching at the opposite side. Though this condition does not relieve one from worrying about impedance variations, as mentioned above, this condition allows to treat the one side separately from the opposite one. Moreover, the circuitry and the transducer can be placed in close proximity to each other, or even be integrated together. As a result, the cable may be reduced in length.
According to condition (2.10), it is highly desirable that the transmitter and the receiver are implemented by the same circuit. Beside creating the reciprocal conditions in the flow measurement, the need for switching would disappear altogether.
The matching of Z_{tx} and Z_{rx}, which are obtained from different circuits, remains a challenging part of the design. The need of that can be avoided by ensuring that the output impedances of the transmitters and the input impedances of the receivers are sufficiently smaller or sufficiently larger than the transducer impedances:

$$Z_{tx1}, Z_{rx1} \ll Z_1 \quad \text{and} \quad Z_{tx2}, Z_{rx2} \ll Z_2 \tag{2.11}$$

or

$$Z_{tx1}, Z_{rx1} \gg Z_1 \quad \text{and} \quad Z_{tx2}, Z_{rx2} \gg Z_2 \tag{2.12}$$

As can be seen in Eq. (2.6) and (2.7), by letting Z_{tx1}, Z_{rx1}, Z_{tx2}, and Z_{rx2} be negligibly small or extremely large relative to Z_1 and Z_2, the transfer function of I_{rx1} can be approximated to that of I_{rx2}. These conditions are in close agreement with Figure 2.4, which shows that sufficiently small and sufficiently large values of the impedance keep the resonance frequency of the transducer approximately constant.
In addition to the described conditions for the transmitter and the receiver, there are a couple of conditions for the excitation signal. Making use of these conditions only does not create reciprocity in the flow-measurement system, however contributes to a slight decrease of the zero-flow error. These conditions have been observed in Figure 2.7 and 2.8 and they include:

- Shorting the length of the received signals I_{rx1} and I_{rx2}.

The deviation between I_{rx1} and I_{rx2} increases with their duration in time. Therefore, the shorter the signals, the less value of the zero-flow error can be obtained.

- Using an excitation signal, whose spectrum is bounded around the resonance frequency of the transducer.

The received signals have a different shape in the magnitude and the phase plot. Therefore, the more the signals are limited in the frequency domain around f_{res}, the more undesirable frequency components will be cut off.

2.5. Zero-flow error

The reciprocal conditions, discussed in the previous section, show that the zero-flow error would be ideally zero if the output impedance of the transmitter Z_{tx} and the input impedance of the receiver Z_{rx} would be perfectly matched. It is clear that as soon as these conditions start to be violated, the zero-flow error will still appear in the system. Its value will depend on the mismatch that on its turn will be determined by the system design and the tolerances in the manufacturing process. It has also been shown that keeping Z_{tx} and Z_{rx} much smaller or much larger than the transducer impedances Z_1 and Z_2, relieves one from the matching issue. Beside ensuring a desired value of the zero-flow error in the face of the impedance mismatch, this condition could also tolerate a larger mismatch than it would be allowed in the case of the perfect matching. The choice of Z_{tx} and Z_{rx} is a trade-off between

different parameters like: the power consumption, the amplitude of the received signals I_{rx1} and I_{rx2}, the circuit complexity and reciprocity in the system. Before choosing the right condition, one can ask the questions:

- Is it worth trying to match the impedances? What is the maximum mismatch that can be tolerated to hold the zero-flow error at a desired value?
- When are Z_{tx} and Z_{rx} considered to be sufficiently small and sufficiently large?

To answer these questions it is needed to see how the zero-flow error is related to the values of Z_{tx} and Z_{rx}. The relationship has been obtained by using the electric circuit introduced in Section 2.3 and redrawn in Figure 2.10 for convenience.

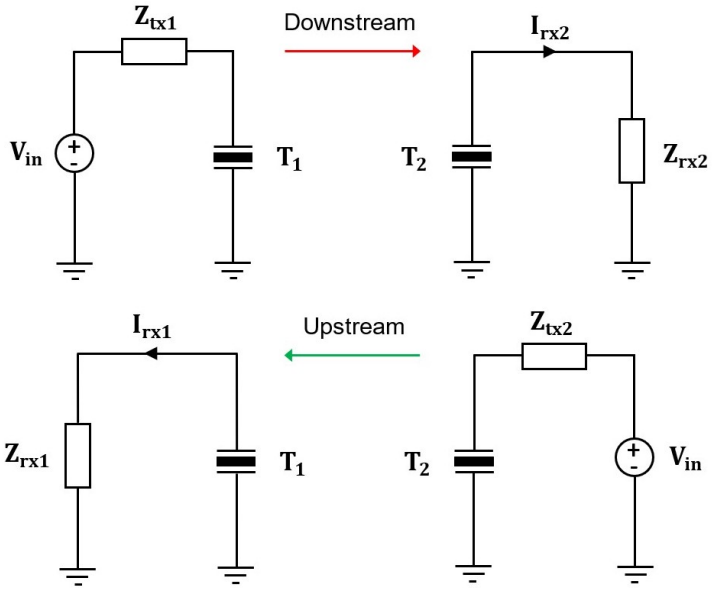


Figure 2.10: Simulation circuit to find the dependency between the zero-flow error and Z_{tx1} and Z_{rx1}, test conditions $Z_{rx1}=(1+\varepsilon)\cdot Z_{tx1}$, $Z_{tx2}=Z_{rx2}=1\ \Omega$.

According to condition (2.10), the value of the zero-flow error will be completely determined by the mismatched impedances located on one side as long as the impedances at the opposites side are perfectly matched. Because this simplifies the simulation considerably, Z_{tx2} and Z_{rx2} are both set to the same values of 1 Ω. The values of Z_{tx1} and Z_{rx1} are given by:

$$Z_{rx1} = (1+\varepsilon)\cdot Z_{tx1}, \tag{2.13}$$

where ε is a mismatch between the impedances. The value of Z_{tx1} has been swept form 100 mΩ to 1 kΩ. The currents I_{rx1} and I_{rx2} for each pair of Z_{tx1} and Z_{rx1} have been processed by the cross-correlation algorithm resulting in the family of the zero-flow error curves, shown in Figure 2.11. The simulation has been performed for different ε: 1%, 2.5%, 5%, 7.5%, and 10%.
The obtained result confirms already familiar observations, namely:

- The zero-flow error hits its maximum value at the point where the values of Z_{tx} and Z_{rx} are chosen to be close to the value of R_m;
- The zero-flow error decreases from its peak value equally as Z_{tx1} and Z_{rx1} are chosen much smaller or much larger than R_m.

The maximum allowable zero-flow error of 100 ps is indicated by the red dashed line. Therefore, the worst-case occurs by trying to match Z_{tx1} and Z_{rx1} with a value which is close to the value of Z_1 and

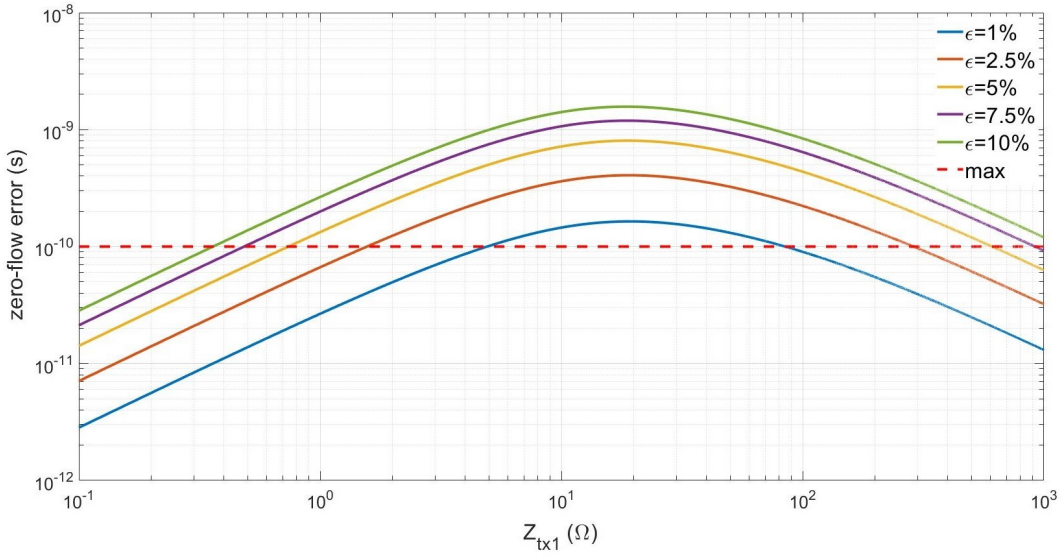


Figure 2.11: Simulated zero-flow error with varying impedances of transmitter 1 and receiver 1 and by introducing different mismatches between the impedances.

Z_2. In order to keep the zero-flow error below 100 ps, the mismatch between Z_{tx1} and Z_{rx1} should be less than 1%, which is highly difficult to be met in practice. This requirement is greatly relaxed if Z_{tx1} and Z_{rx1} are much smaller or larger than Z_1 and Z_2. In these regions, the curves roll off at a rate of approximately 20 dB per decade. Thus, by making Z_{tx1} and Z_{rx1} 100 times smaller than Z_1 and Z_2, the zero-flow error will remain below the maximum value even with a mismatch of 10%.

3

Architecture-level analysis and design

In this chapter two different topologies for the transmitter circuit are discussed. First, the pulser circuit is investigated. After a detailed analysis of the pulser, the buffer circuit is presented. The circuits are compared to each other and the choice is made in favour of a circuit with better performance. At the end, the waveform of the excitation signal is presented.

3.1. Transmitter topology

The zero-flow error is highly dependent on the choice of Z_{tx} and Z_{rx} as well as on the mismatch between them. The relationship has been shown in Section 2.5, Figure 2.11. The simulation circuit used to get this plot is a very simplified model of the flow measurement system. Therefore, the obtained result is considered to be ideal. Several factors which are not captured by the simulation model are: the change of Z_{tx} and Z_{rx} during transmission and reception of the signal, the frequency-dependent behaviour of the impedances, the phase shift in the signal exiting the excitation source, and parasitic impedances of the bond wires on the PCB. When the system will be designed, some of these factors will appear in the simulation. It is obvious that they will cause the zero-flow error value to differ from the ideal curve. A straightforward way to design the real system is step by step replacement of the ideal components with the real ones and to check whether the obtained zero-flow error value stays close to the desired ideal value. It might happen that the design specifications of the individual components will need to be adjusted to push the real zero-flow error value to the ideal value. The system realization begins with the design of the transmitter.

3.1.1. Pulser as transmitter

The most widely used way to bring the transducer into oscillation is using a pulser. Figure 3.1 shows a simple pulser implementation by the complementary inverter.

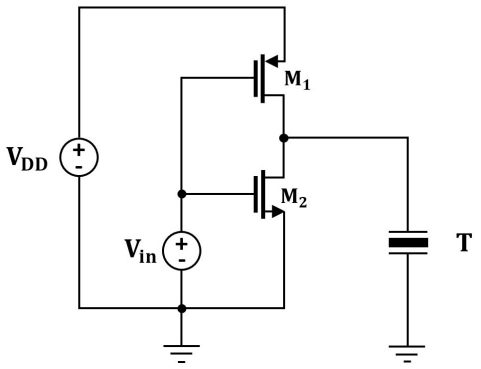


Figure 3.1: Inverter used as the transmitter circuit for excitation of the transducer.

The gates of the PMOS and NMOS devices are tied together and connected to the voltage source V_{in}. The voltage source V_{DD} provides the power supply to the circuit. The transducer **T** is connected to the inverter's output. The circuit operates as follows:

- Once V_{in} is set to 0 V, the circuit is in the precharge phase. The NMOS transistor M_2 is off while the PMOS transistor M_1 is on. The transducer charges up through M_1 to the power supply voltage V_{DD};
- As soon as V_{in} abruptly changes to V_{DD}, the circuit is in the discharge phase. The roles of the transistors are interchanged. M_1 turns off while M_2 turns on. The transducer is discharged through M_2 to zero. This forces the transducer to oscillate and transmit an acoustic signal.

The flow measurement system model, where TX1 has been replaced by the pulser circuit is shown in Figure 3.2.

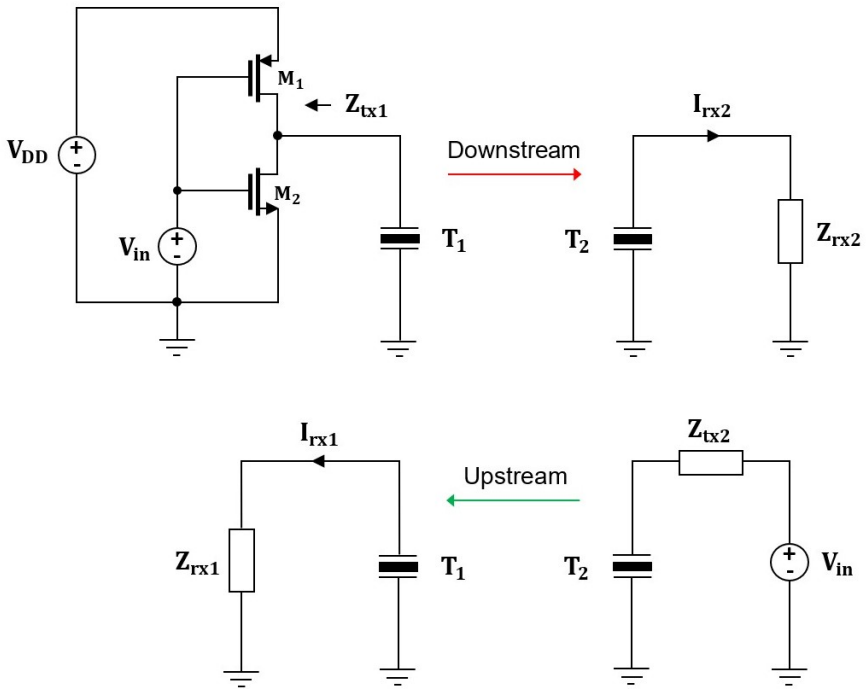


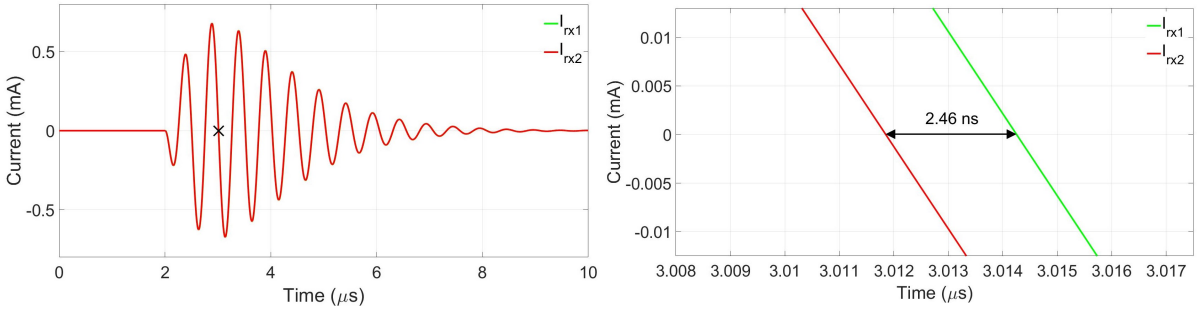
Figure 3.2: Flow measurement system model where TX1 has been replaced with the pulser; the test conditions: Z_{tx1}=Z_{rx1}=0.5 Ω and Z_{tx2}=Z_{rx2}=1 Ω.

To see how the presence of the non-ideal transmitter affects the zero-flow error, the system is tested under conditions Z_{tx1}=Z_{rx1}=0.5 Ω and Z_{tx2}=Z_{rx2}=1 Ω. The impedance seen looking into the inverter's output is equal to Z_{tx} and it is determined by the resistance of M_2. In the discharge phase the transistor M_2 acts like a switch and has a low ohmic resistance, the value of which can be roughly estimated by [8]:

$$\frac{W}{L} = \frac{1}{\mu C_{ox} \cdot Z_{tx} \cdot (V_{gs} - V_{th})} \tag{3.1}$$

Substituting the value of μC_{ox} and V_{th} from Tab.1 along with Z_{tx}=0.5 Ω results in the device size W/L= 2.2mm / 0.6µm.
Once the transducers have been excited, the downstream and the upstream signals are transmitted to the opposite side where they are sensed by the receivers. The obtained time-domain signals I_{rx1} and I_{rx2} are shown in Figure 3.3a. Besides the cross-correlation method, another way for a quick estimation of the zero-flow error is the zero-crossing [1]. In this case, the zero-flow error is determined by the time delay between the signals at the intersection points with the X-axis which appear right after the peak

current values have been passed. A zoom on these points is given in Figure 3.3b. It may be expected that the zero-flow error will not be exactly zero as in the ideal situation, however, the obtained value of 2.46 ns is much larger than expected. To explore what could cause this difference more insight in the circuit operation is needed.

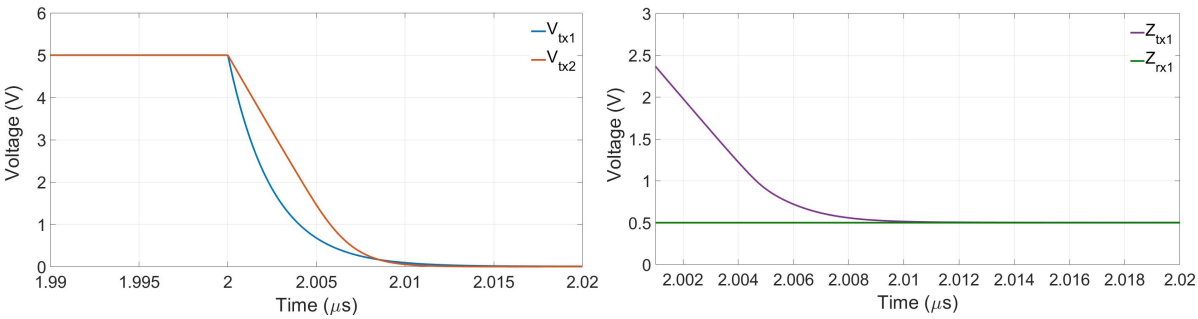


(a) Signals received by RX1 and RX2.

(b) Zero-flow error obtained by zero-crossing measurement.

Figure 3.3: Simulation results of the flow measurement model for obtaining the zero-flow error.

Figure 3.4a depicts the voltages across the transmit transducers T1 and T2 just after the excitation signals have been applied. As can be seen, the voltages decrease in two different ways: V_{tx1} drops according to the exponential decay while V_{tx2} decreases linearly at a constant rate. It is evident that the transistor behaves as a non-ideal voltage source, since its voltage change is limited by the finite current through the transistor itself.



(a) Voltage over the transmit transducers.

(b) Output impedance of TX1 and RX1.

Figure 3.4: Simulation result showing the difference in behavior of TX1 and TX2.

The voltage V_{tx2} corresponds to the drain-source voltage of M_2 during the discharge phase. Once M_2 switches on, it is in the saturation region. The transistor is sinking the current from the transducer at the maximum slew rate until the time that V_{tx1} falls below the saturation voltage. After that point, the transistor is in the triode region. The current decreases and becomes zero as the transducer has been completely discharged. The transducer can be forced to a faster discharge by increasing the discharge current. This makes the slope steeper and yields a behavior closer to the ideal source but at the cost of a large chip area.
Figure 3.4b shows the plot of impedances Z_{tx1} and Z_{rx1} in the time-domain during signal transmission. The impedances are determined as the voltage-current ratio by using the results obtained from the transient simulation. As one can see, the input impedance Z_{rx1} remains at the same constant value, which is in agreement with the ideal resistance of 0.5 Ω. The output impedance Z_{tx1} shows a time-varying behavior. The plot is a zoom on the time interval in which the impedance Z_{tx1} settles to the desired value of 0.5 Ω. Since the transistor starts from the saturation region, it has a very large impedance. Its value is in the order of kΩ's and exceeds by far the expected value. Such large impedance remains throughout most of the discharging phase, until the transistor enters the triode region. After a short decrease, the impedance remains constant in the triode region. Thus, at the very beginning of signal transmission, the impedances are dramatically mismatched. It takes approximately 10 ns for $Z_{tx1}$to reach the finale value of 0.5 Ω. The transducer is in series resonance and oscillates at the resonance

frequency of 2 MHz, implying a period of 0.5 µs. Therefore, the settling time is only 2% of the period, yet it is enough for the signals to get misaligned, resulting in such a large zero-flow error. The time of being in the saturation region can be shortened by reducing the power supply voltage V_{DD}. If its value is lower than the saturation voltage, the transistor will be biased immediately in the triode region. The settling time will be shorter and thus the zero-flow error will be reduced as well. For example, lowering V_{DD} from 5 V to 0.5 V improves the zero-flow error from 2.4 ns to 0.104 ns. However, this has also a drawback. The lower the power supply voltage, the less amount of power can be used to excite the transducer. As a consequence, the received signals will be reduced in amplitude and the system will have a low SNR.
A question arises here: would the zero-flow error be closer to the ideal value of 0 s if transmitter 2 would be replaced by the pulser circuit? This situation is given in Figure 3.5.

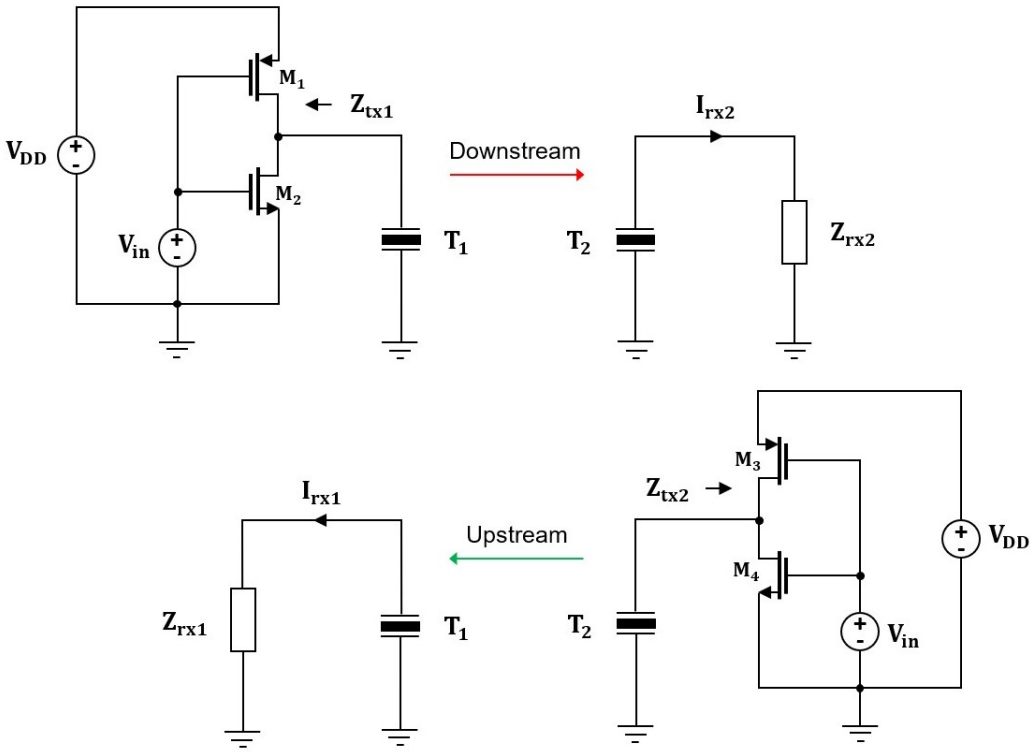


Figure 3.5: Flow measurement system model where TX1 and TX2 have been replaced with the pulser; the test conditions: Z_{tx1}=Z_{rx1}=0.5 Ω and Z_{tx2}=Z_{rx2}=1 Ω.

The zero-flow error for this configuration is 2.43 ns. No wonder that the circuit does not provide any improvement. As one can predict, during the discharge phase the voltages across the transmit transducer are slewing at their maximum rate. When the voltages have dropped down to zero, the impedances Z_{tx1} and Z_{tx2} settle to their final values of 0.5 Ω and 1 Ω. Thus, in addition to the mismatch between Z_{tx1} and Z_{rx1}, there is also mismatch at the opposite side between Z_{tx2} and Z_{rx2}. This being the reason that the significant zero-flow error is still present in the system.
Therefore, despite the simple implementation using, the pulser as the transmitter is a poor solution for achieving the desired zero-flow error, due to several reasons:

- The output impedance of the pulser is not constant. It has a nonlinear time-varying behavior and changes in a wide range from kΩ's to mΩ's;
- In order to compensate the negative effect of the impedance change, Z_{tx1} and Z_{tx2} should be pushed to smaller values. The NMOS devices M_2 and M_4 have to be oversized, which will consume a large chip area;
- The system design is based on the reciprocal condition given by Eq. (2.9). The best solution would be a circuit, which can be used as a transmitter as well as a receiver. This will not happen

when using the pulser as a transmitter, since this requires an additional circuitry for the receiver. Thus, the zero-flow error will still depend on the mismatch between the impedances of the circuits and switching between TX and RX will remain necessary;

- During the simulations discussed above, the input impedances Z_{rx1}, Z_{rx2} have been kept constant and purely active. When a real amplifier circuit is used for the receiver, this assumption likely does not hold anymore. At high frequencies the impedances may show a frequency-dependent behavior. The phase shift between Z_{tx} and Z_{rx} will lead to an increase of the zero-flow error. The situation can be worsened by the parasitic impedances arising in the places where the chip is attached to the PCB;
- To get the transducer oscillating the step function is used. This is a broad spectrum signal. The maximum amount of energy occurs at DC and low frequencies. Since the transducer uses a narrow band around 2 MHz, the power of the transmitted signal is low. Therefore, the choice of the step function as the excitation source is not power efficient and other waveforms are preferable, the spectrum of which is limited around the resonant frequency of the transducer.

This calls for a more advanced transmitter circuit, whose output impedance either remains constant or changes linearly in a very narrow range around the desirable value. To achieve this, the transmitter itself must have a linear behavior. There are different ways to synthesize such circuit, the most straightforward being to apply the two-port network theory.

3.1.2. Buffer as transmitter

The transmitter can be seen as a two-port circuit between the source and the load. It accepts the signal applied to its input and generates the output signal which is delivered to the transducer. The situation is illustrated in Figure 3.6.

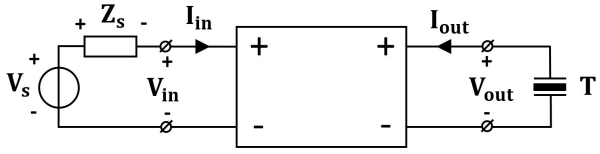


Figure 3.6: Two-port representation of the transmitter.

The impedance looking into the output terminal of the two-port is equal to Z_{out} and it is determined as a ratio of the output parameters V_{out} and I_{out}. The ratio remains constant if these parameters behave linearly relative to each other. For example, when the output voltage rises by some amount, the circuit should be able to measure that and to use this to control the input parameters, thereby forcing itself to increase the output current by the same amount. The linear relation between the input and the output parameters can be described by the chain matrix as [9]:

$$\begin{cases} V_{in} &= A \cdot V_{out} - B \cdot I_{out} \\ I_{in} &= C \cdot V_{out} - D \cdot I_{out} \end{cases} \tag{3.2}$$

The Kirchhoff's voltage law at the input of the two-port yields:

$$V_s = I_{in} \cdot Z_s + V_{in} \tag{3.3}$$

The output impedance of the two-port is determined under the condition that there is no signal at its input. Thus, with V_s set to 0 V, Eq. (3.3) can be rewritten as:

$$V_{in} + I_{in} \cdot Z_s = 0 \tag{3.4}$$

Subtracting Eq. (3.4) from the first equation of the chain matrix results in:

$$\begin{cases} -I_{in} \cdot Z_s &= A \cdot V_{out} - B \cdot I_{out} \\ I_{in} &= C \cdot V_{out} - D \cdot I_{out} \end{cases} \tag{3.5}$$

Solving this equation set for Z_{out} yields:

$$Z_{out} = \frac{C \cdot Z_s + A}{D \cdot Z_s + B} \tag{3.6}$$

As can be seen, the output impedance of the two-port depends on the source impedance Z_s. The value of Z_s is usually not accurately known and it can also vary in some range. Thus, to prevent Z_{out} from change due to Z_s, the values of C and D are both chosen to be 0. The input-output transfer given by (3.2) can be rewritten in the simpler form:

$$\begin{cases} V_{in} = A \cdot V_{out} - B \cdot I_{out} \\ I_{in} = 0 \end{cases} \tag{3.7}$$

The realisation of this system equation implies the circuit to have the following functionality:

- The circuit has to sense the output current and to convert it into the voltage to be provided to the circuit's input;
- The circuit has to measure the output voltage and to feed a fraction of that to the circuit's input;
- The voltages translated from the output to the input have to be summed and set equal to the input voltage;
- There must be no current at the circuit's input.

The graphic representation of such system is shown in Figure 3.7. The system is implemented with the aid of two feedback loops and the nullor [10].

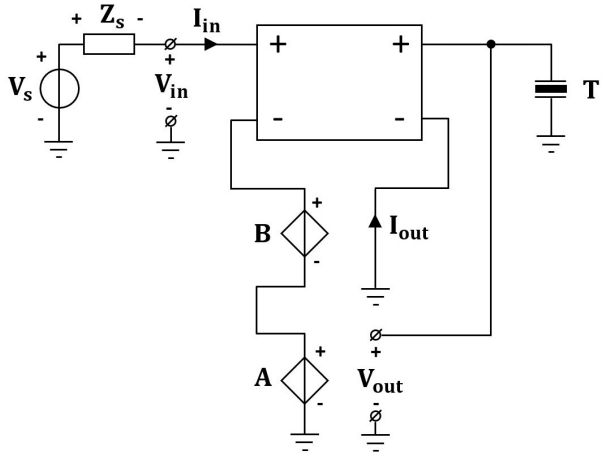


Figure 3.7: Circuit diagram of the transmitter.

Series-series feedback senses the current through the transducer I_{out} and transforms it to the input port as a voltage. Series-shunt feedback samples the voltage across the transducer V_{out} and produces a scaled version of it at the input port. The feedback voltages are summed in series fashion at the input port. The nullor equates the voltages at its input terminals and maintains the zero-current at the input port. The output impedance of the system is entirely determined by the feedback factors A and B. Using linear circuit components to implement the feedback will equip the system with a stable and accurate value of Z_{out}. There are several different realizations of such system in practice, the simplest solution is given in Figure 3.8.

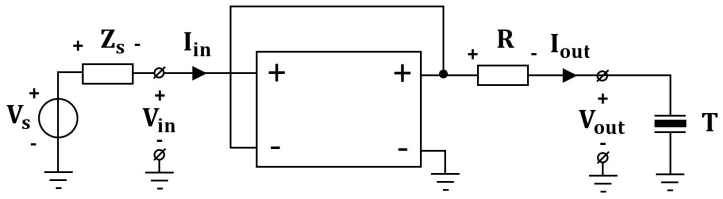


Figure 3.8: Transmitter circuit implementation with the nullor.

In this configuration, the current-to-voltage conversion is performed by means of a resistor with value R. In order to use only one feedback and by this simplifying the circuit, the voltages are first summed at the output and then translated with the unity-gain feedback loop to the input. This implies the value of A to be equal to 1. The nullor nullifies the feedback voltage and the input voltage. It is readily seen that the obtained topology is a simple buffer configuration with an additional resistance connected in series at the nullor's output. The output impedance of this circuit is equal to resistance value R. The resistor is a passive component which can be made very precise. It remains constant and has also frequency independent behavior. So, the output impedance of this ideal circuit will be a stable, predictable, and well defined value.
However, the nullor is an ideal component with infinite gain. During the system design it will have to be replaced with a real circuit, the gain of which will have a finite value. Using the operational amplifier (opamp) offers a suitable solution in this situation. Figure 3.9 shows the transmitter circuit where the nullor has been replaced with the equivalent circuit model of the opamp [11].

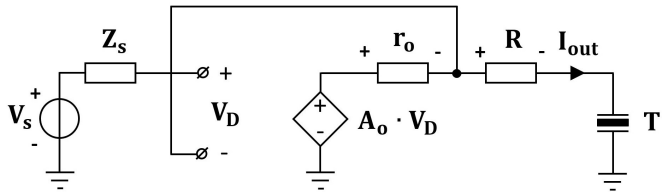


Figure 3.9: Transmitter circuit explicitly showing the opamp with finite A_o and r_o.

Since a real opamp has a finite open-loop gain A_o and non-zero output resistance r_o, it will also provide an additional contribution to the output impedance of the transmitter. In this case, Z_{tx} is given by:

$$Z_{tx} = R + \frac{r_o}{1 + A_o}, \tag{3.8}$$

which can be rewritten as:

$$Z_{tx} = R + Z_{out} \tag{3.9}$$

It is apparent that choosing the buffer amplifier for the transmitter circuit has more advantages in comparison with the pulser. Besides maintaining a stable, predictable output impedance, the buffer can also mitigate the negative effect of the parasitic impedances of the bond wires. By placing resistor R off-chip, the bond wires will appear inside the feedback path so that the magnitude of the parasitic impedances is reduced by the loop gain A_o. In addition to this, the linear amplifier can handle various waveforms rather than only the step function. The power of the transmitted signal can be increased by using a narrowband signal around 2 MHz. Finally, unlike the pulser, the buffer circuit can be also used as a receiver.

3.2. Receiver topology

In the flow measurement systems presented in [2], [3] two different circuits are involved for transmitting and receiving the signal. First, the transducer is connected to the transmitter. Having sent the down-

stream signal, the transducer switches to the receiver to pick up the upstream signal. The easiest way to get rid of switching is simply to use the same circuit for the transmitter and the receiver. Besides that the system complexity is reduced, a better impedance matching can be achieved. This would result in the zero-flow error being minimized. Figure 3.10 shows the buffer amplifier used as a receiver.

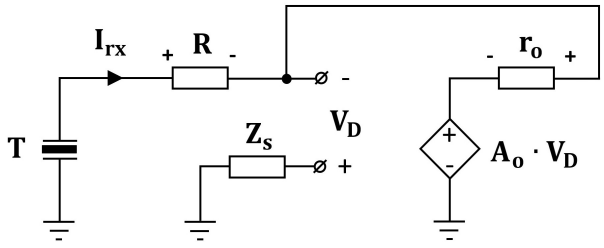


Figure 3.10: Ideal buffer amplifier used in receive mode.

In this case, the input impedance of the receiver is given by:

$$Z_{rx} = R + Z_{in} \tag{3.10}$$

The impedances Z_{in} and Z_{out} from Eq. (3.9), (3.10) are equal and thus the impedances Z_{tx} and Z_{rx} are perfectly matched. This situation has been simulated with the system shown in Figure 3.11, where TX and RX are implemented by an ideal opamp with r_o=2.5 Ω and A_o=40 dB. The system operates reciprocally and the obtained value of the zero-flow error is indeed 0 s.

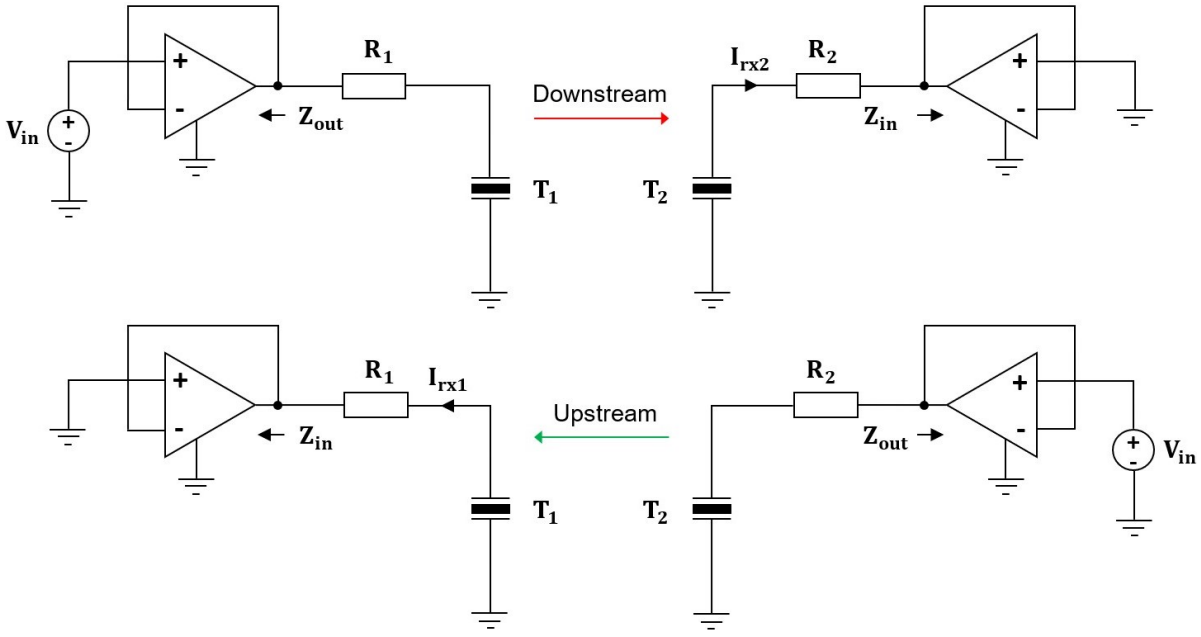
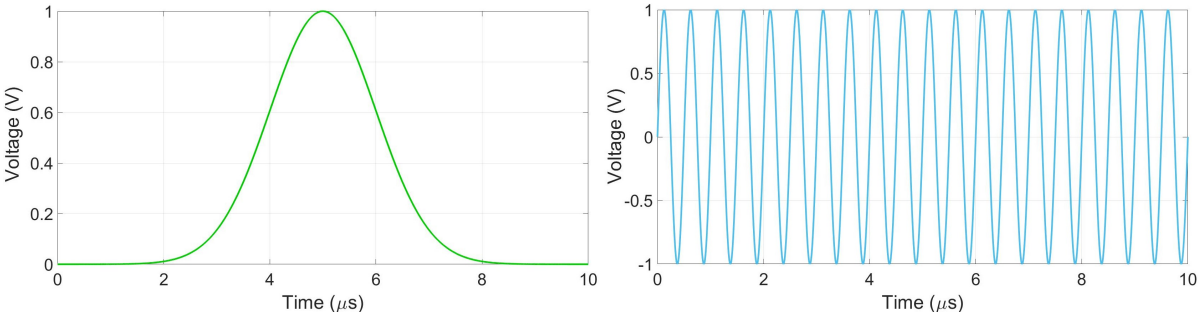


Figure 3.11: Flow measurement system model where TX1, TX2, RX1, and RX2 have been replaced with an ideal opamp; the test conditions: R_1=0.5 Ω and R_2=1 Ω.

3.3. Excitation signal waveform

As has been mentioned earlier, the use of the step function as an excitation signal in the transmitter circuit has a significant drawback. A large amount of signal energy is lost at low frequencies, resulting in poor system efficiency. In order to increase the power of the transmitted signal, the step signal should have a large amplitude. However, since the opamp has a finite current drive capability, its output will

not be able to change rapidly for a large V_{in}. To prevent slew-rate limitation, the opamp must have a high gain bandwidth product, which in turn can consume a lot of power.
Several different signal waveforms have been investigated in [1]. A better alternative to the step signal would be a Gaussian pulse. The signal is obtained by multiplying the Gaussian distribution and a sinusoidal signal shown in Figure 3.12a and 3.12b resulting in the signal given in Fig. 3.13.



(a) Gaussian distribution.

(b) Sine wave with frequency of 2 MHz.

Figure 3.12: Signal used to create a Gaussian pulse.

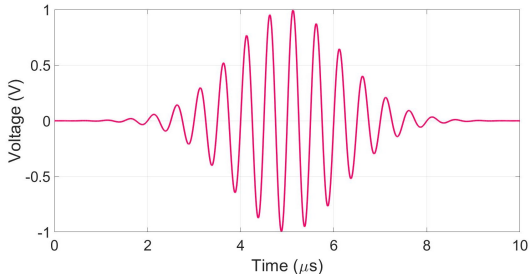
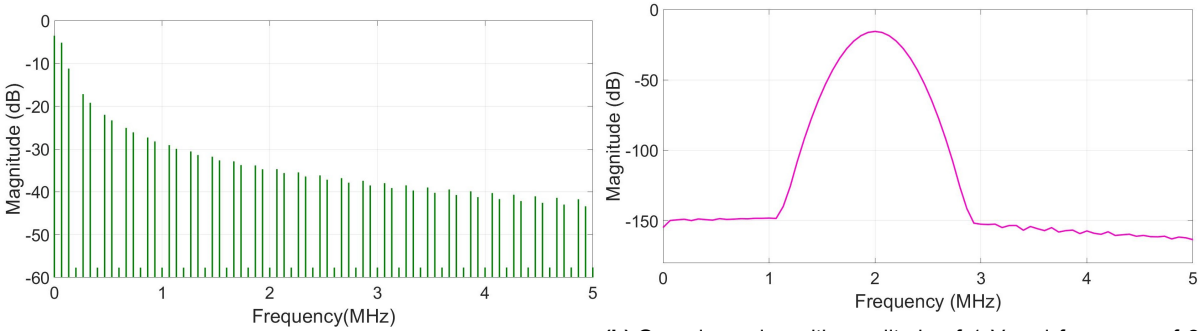


Figure 3.13: Gaussian pulse obtained by multiplying the signals from Fig. 3.12a and 3.12b.

An advantage of such signal is that the maximum power of the step signal can be shifted from the low frequencies to the frequency determined by the sine wave. Choosing the frequency of the sine wave to be 2 MHz, the peak energy will be spent across the bandwidth of the transducer, thereby increasing the system efficiency. Figure 3.14 shows the spectrum of the unity step function and a Gaussian pulse with amplitude of 1 V. In this case, the magnitude of the Gaussian pulse at 2 MHz is 20 dB larger than the magnitude of the step function.



(a) Unit step function.

(b) Gaussian pulse with amplitude of 1 V and frequency of 2 MHz.

Figure 3.14: Magnitude spectrum of two different excitation signals.

Another positive feature of the Gaussian pulse is that by changing the standard deviation of the Gaussian distribution, the duration of the pulse can be adjusted. In case when cross-correlation is used, keeping the Gaussian pulse short will lead to a slight decrease of the zero-flow error.

4

Circuit-level analysis and design

This chapter deals with the realisation of the transceiver at the transistor-level. First, the transmitter circuit design is described, including such steps as: choosing a suitable configuration for the output stage, implementation of the loop amplifier, and ensuring circuit stability by frequency compensation. The chapter continues with the design of the receiver circuit. At the end of the chapter, the circuit performance is evaluated by calculating the zero-flow error remaining in the system.

4.1. Design of the output stage

A practical operational amplifier is usually composed of several stages which are connected in cascade. The first and the second stage are needed to provide a high open-loop gain A_o. These gain stages are followed by the output stage, of which the function is to drive the load and to equip the entire amplifier with a low output impedance r_o. Since r_o is the most important parameter of the transmitter, the opamp design begins with the design of the output stage.

4.1.1. Class A output stage

First a class A output stage is considered. The circuit is shown in Figure 4.1 [12].

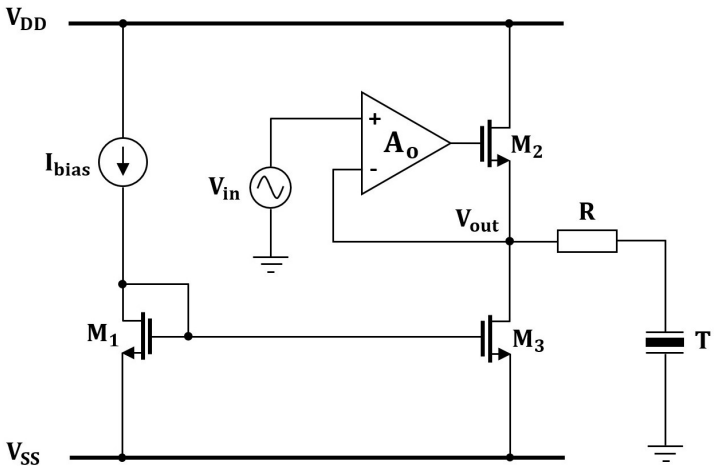


Figure 4.1: Class A output stage with the bias circuit and an ideal opamp used to supply the loop gain.

The circuit utilizes a common-drain configuration with the NMOS transistor M_2, which is actively loaded with the current source M_3. Transistors M_1 and M_3 form a current mirror to supply the output stage with the bias current I_{bias}. The loop gain A_o is provided by an ideal opamp. The input signal V_{in} is a Gaussian pulse with a voltage swing of ± 2 V.
The resistance seen looking into the output node V_{out} is given by:

$$R_{out} = \frac{r_{o2} \cdot r_{o3}}{r_{o2} + r_{o3} + r_{o2} \cdot r_{o3} \cdot g_{m2} \cdot (1 + A_o)}, \tag{4.1}$$

where g_{m2} is the transconductance of M_2, r_{o2} and r_{o3} are the resistances of M_2 and M_3.
Given the third term in the denominator is dominant, Eq. (4.1) can be rewritten in a simplified form as:

$$R_{out} \cong \frac{1}{A_o \cdot g_{m2}} \tag{4.2}$$

By letting R_{out} and A_o be 25 mΩ and 40 dB respectively, the transconductance g_{m2} results in 0.4 S. The transistors operate in the saturation region, thus the transconductance of M_2 is given by:

$$g_m = \sqrt{2 \cdot \mu C_{ox} \cdot \frac{W}{L} \cdot I_{bias}} \tag{4.3}$$

Rearranging Eq. (4.3) slightly yields:

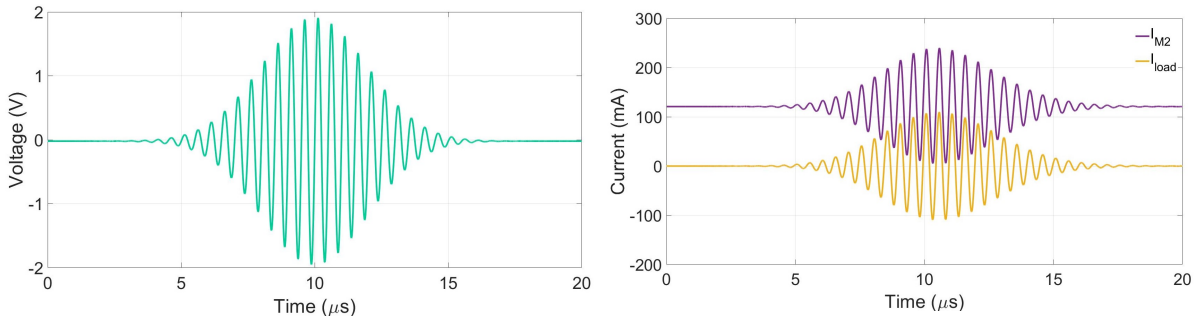
$$\frac{W}{L} = \frac{g_{m2}^2}{2 \cdot \mu C_{ox} \cdot I_{bias}} \tag{4.4}$$

The negative feedback loop forces the input signal V_{in} to appear at the output node, causing the current I_{load} to flow through the transducer. The current swing is ±100 mA. In order to prevent I_{load} from being clipped off during the negative swing of V_{in}, the bias current is chosen to be 110 mA. Substituting the value of μC_{ox} from Tab. 1 along with g_{m2}=0.4 S and I_{bias}=110 mA in Eq. (4.4), provides the required dimensions of the devices M_1-M_3. The devices are chosen with the minimum length L of 0.6 µm in order to minimize the devices capacitance. The obtained results are given in Tab. 4.1.

Table 4.1: Transistor dimensions of the class A output stage in Figure 4.1

Transistor	**M_1**	**M_2**	**M_3**
W/L	35/0.6	35/0.6	35/0.6

Figure 4.2 shows the voltage across the transducer and the currents flowing through the transducer I_{load} and the output stage I_{M2}.



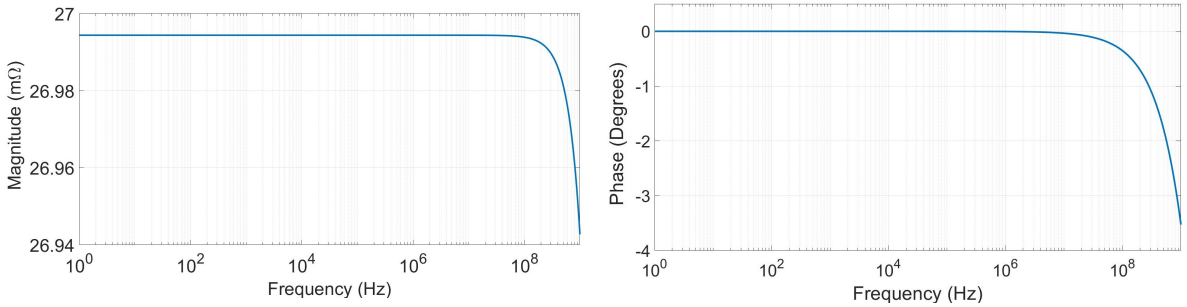
(a) Voltage across the transducer.

(b) Currents I_{M2} and I_{load}.

Figure 4.2: Simulation result of the class A output stage.

For V_{out}=0 V there is no current through the transducer, while the current in the output stage is equal to 110 mA. When V_{out} increases, I_{load} goes up, in turn raising I_{out}. The load current I_{load} flows from V_{DD} through M_2 into the transducer. During the negative voltage swing of V_{in}, the current I_{load} is reversed. It comes out of the transducer and sinks through M_3 down to V_{ss}.

Figure 4.3 shows the bode plot of the output impedance. As can be seen, the impedance has a purely resistive behavior and its magnitude is equal to 27 mΩ.



(a) Magnitude plot.

(b) Phase plot.

Figure 4.3: Frequency response of the output impedance of the class A output stage.

To see what is the value of the zero-flow error after implementation of the output stage, the circuit shown in Figure 4.4 is simulated. The opamp consists of the circuit given in 4.1. The output impedance of TX1 is 0.527 Ω and thus the mismatch between Z_{tx1} and Z_{rx1} is 5.4 %. Applying cross-correlation on I_{rx1} and I_{rx2} results in a zero-flow error of 84.5 ps, which is in close agreement with the ideal value of 73 ps.

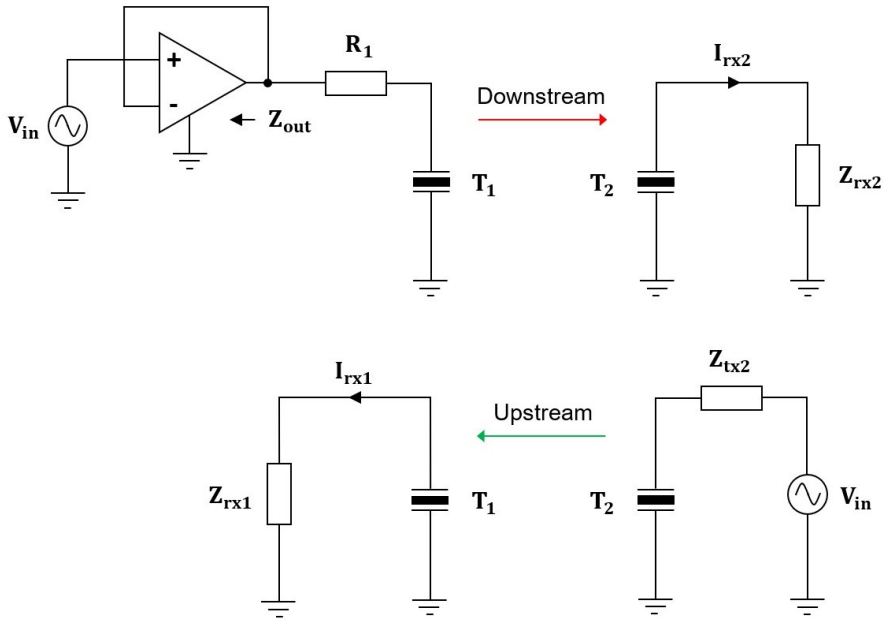


Figure 4.4: Flow measurement system model where TX1 has been replaced with the class A output stage shown in Figure 4.1, the test conditions: R_1=Z_{rx1}=0.5 Ω, Z_{tx2}=Z_{rx2}=1 Ω and Z_{out}=27 mΩ.

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According to Eq. (4.1)-(4.3) the output impedance of the opamp depends on the current through the output stage. An increase of I_{load} causes the transconductance g_{m2} to increase as well, in turn decreasing the output impedance R_{out} and vice versa: a decrease of I_{load} causes a decrease of g_{m2}, in turn increasing R_{out}. The extreme current values of 220 mA and 6 mA correspond with R_{out} of 17.9 mΩ and 115 mΩ respectively. Despite the fact that the zero-flow error is close to the result obtained from the ideal circuit, the class A output stage has a significant disadvantage. There must always be a bias current in the output stage, which depends on the input signal. The higher the voltage V_{in}, the larger the bias current should be. This current is being continuously drawn through the output stage and thus it is a real drain on the power efficiency of the system. So, to make the system power efficient a different type of the output stage is needed. A class AB output stage might be a better choice.

4.1.2. Class AB output stage

Figure 4.5 [12] shows a class AB output stage. Here, the transistors M_7-M_8 connected as source followers form the output stage proper. The biasing is established by the diode-connected pair M_n-M_p. The current mirrors M_1-M_3 and M_2-M_6 along with the current source I_{bias} provide the current to bias the diode pair.

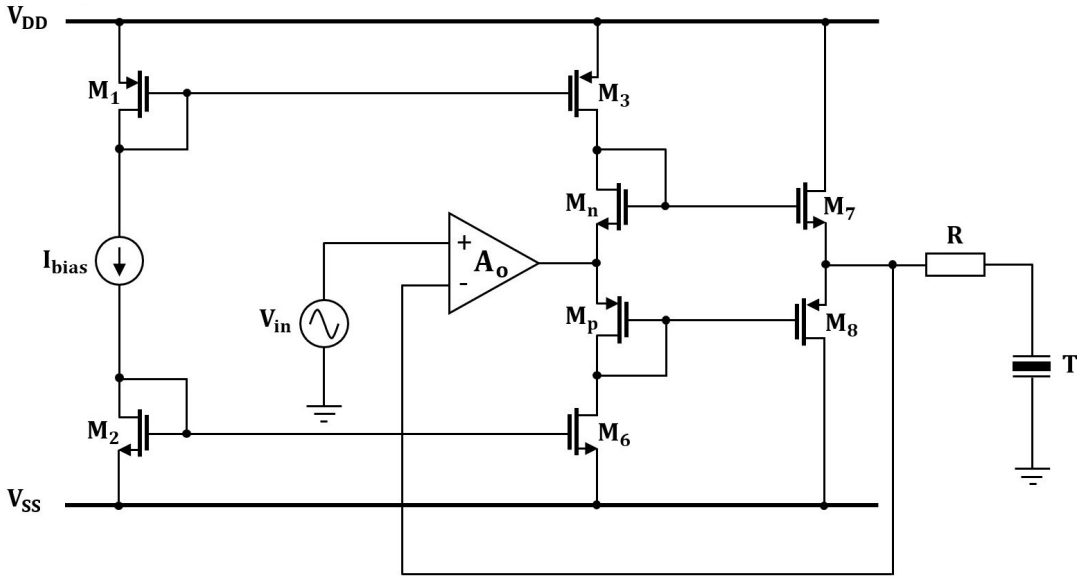


Figure 4.5: Class AB output stage with the bias circuitry and an ideal opamp used to supply the loop gain.

Unlike the class A output stage, this output stage does not require a large bias current in the absence of the input signal V_{in}. The transistors M_7-M_8 should remain conducting to avoid crossover distortion, however, for this the quiescent current is kept at a minimum. The saturation current without considering channel length modulation, is given by [8]:

$$I_{bias} = \frac{1}{2} \cdot \mu C_{ox} \cdot \frac{W}{L} \cdot V_{eff}^2 \tag{4.5}$$

Rearranging Eq. (4.5) slightly provides:

$$\frac{W}{L} = \frac{2 \cdot I_{bias}}{\mu C_{ox} \cdot V_{eff}^2} \tag{4.6}$$

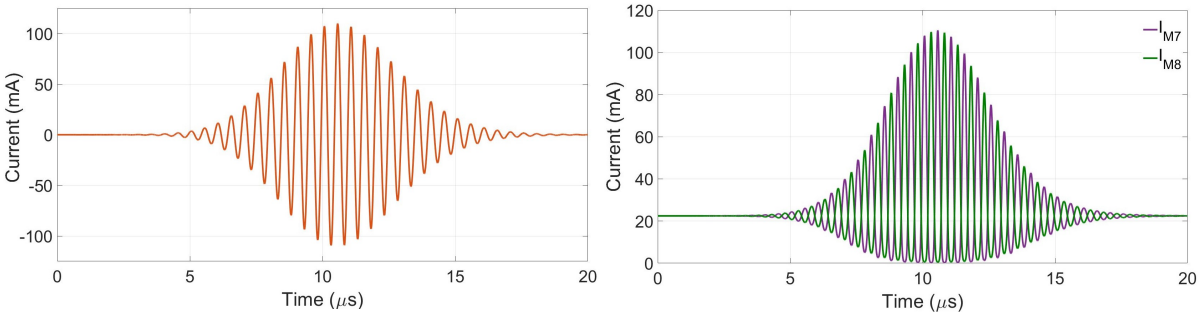
Using the input signal V_{in} with a voltage swing of ±2 V as previously, generates the current swing of ±100 mA. For the sake of power efficiency, the quiescent current is chosen to be 15 % of the maximum load current, thus I_{bias}=15 mA. The overdrive voltage V_{eff} is equal to 0.2 V. Substituting the values in Eq. (4.6) provides the required dimensions of the devices M_1-M_8. The results obtained are displayed in Tab. 4.2.

Table 4.2: Transistor sizes of the class AB output stage in Figure 4.5.

Transistor	M_1	M_2	M_3	M_n	M_p	M_6	M_7	M_8
W/L	125/0.5	35/0.6	125/0.5	35/0.6	125/0.5	35/0.6	35/0.6	125/0.5

Figure 4.6 shows the currents through the transducer and the output stage. Figure 4.7 zooms in on Figure 4.6b. When V_{in}=0, the load current is zero. The transistors M_7-M_8 are both on and they are drawing the small quiescent current. When V_{in} starts to increase, the current through the NMOS M_7 increases as well, while the PMOS M_8 gets less conductive. After some point, when V_{in} is sufficiently

high, M_8 goes off and the load current is completely supplied by M_7. For negative voltage swing, the opposite occurs: for sufficiently low V_{in}, the NMOS goes off and the PMOS takes over the operation. In this case, the transducer is driven by M_8.



(a) Current through the transducer.

(b) Currents through the devices M_7 and M_8.

Figure 4.6: Simulation results of the class AB output stage.

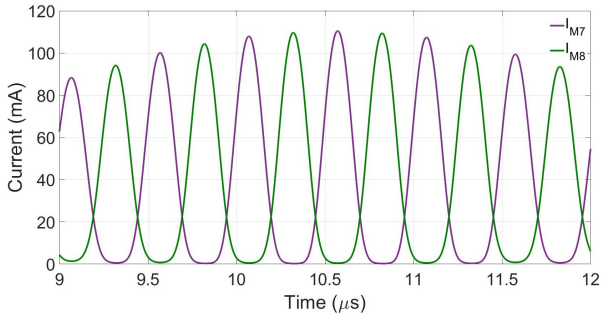
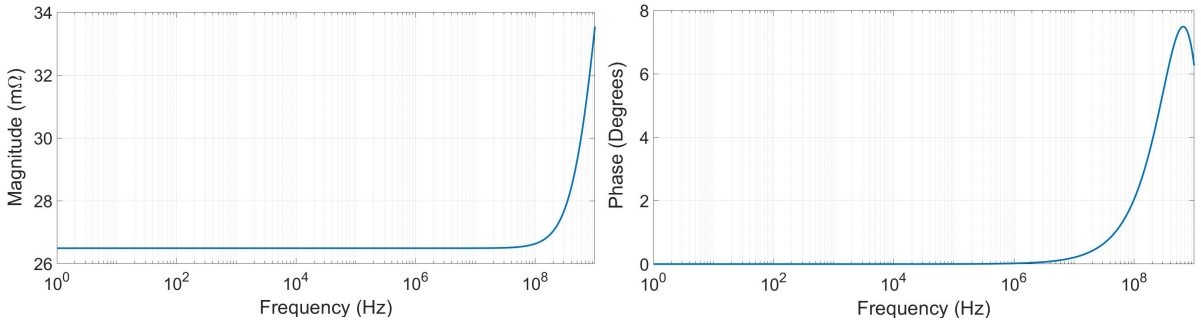


Figure 4.7: Zooming in on Figure 4.6b.

Figure 4.8 shows the bode plot of the output impedance. The magnitude of R_{out} is equal to 26.7 mΩ and since the phase shift at 2 MHz is quite small, it can be considered as a purely resistive impedance.



(a) Magnitude plot.

(b) Phase plot.

Figure 4.8: Frequency response of the output impedance of the class AB output stage.

As one can predict, due to the varied load current, the output impedance will also be changing in some range. When the circuit is in standby, the output impedance has a maximum value R_{max} given by:

$$R_{max} \cong \frac{1}{2 \cdot A_o \cdot g_{min}}, \tag{4.7}$$

where g_{min} corresponds to the quiescent current I_{bias}. When the output stage is in class AB operation, the output impedance reaches its minimum value R_{min}:

$$R_{min} \cong \frac{1}{A_o \cdot g_{max}}, \tag{4.8}$$

where g_{max} corresponds to the maximum load current I_{load}. Using Eq. (4.3), the ratio between Eq. (4.7) and (4.8) is found to be:

$$\frac{R_{max}}{R_{min}} \cong \frac{1}{2} \cdot \sqrt{\frac{I_{load}}{I_{bias}}} \tag{4.9}$$

Substituting the values of I_{bias}=15 mA and I_{load}=110 mA results in:

$$R_{max} \cong 1.17 \cdot R_{min} \tag{4.10}$$

Therefore, the maximum output impedance drops from 26.7 mΩ to 22.76 mΩ. It is evident that in comparison with the class A output stage, the output impedance changes in a much smaller interval. There is no increase of R_{out}, which implies that the maximum mismatch between TX and RX is fixed by the bias current of the output stage and that it is independent of the load current.
The designed class AB output stage is represented by the small-signal equivalent circuit shown in Figure 4.9.

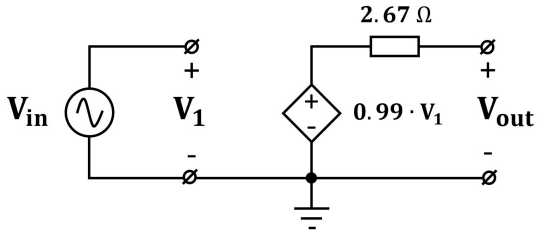


Figure 4.9: Small signal equivalent circuit model the class AB output stage.

The same circuit, which is given in 4.4, has been used to simulate the zero-flow error with the class AB output stage. The obtained result is 79.3 ps and this is fairly close to the ideal value of 73 ps. The next step in the transmitter design is to replace the ideal opamp with a real loop amplifier.

4.2. Design of the loop amplifier

The chosen topology for the loop amplifier is shown in Figure 4.10 [12]. The circuit utilizes two stages. The first stage consists of the n channel differential pair M_1-M_2 and the p channel active load M_3-M_4. The second stage is a common source amplifier M_5 with the active load M_8. In addition to providing gain, the second stage is also used to bias the class AB output stage. It is done by two diode-connected devices M_n-M_p included in the stage. The dual-output current mirror formed by M_8-M_9-M_{10} along with the current source I_{bias} supplies the circuit with the bias current. The value of I_{bias} is chosen to be 1 mA and the overdrive voltage of the transistors is 0.2 V. This allows to immediately determine the device sizes by using Eq. (4.6). The obtained results are given in Table 4.3.

Table 4.3: Transistor dimensions of the loop amplifier in Figure 4.10

Transistor	**$M_{1,2}$**	**$M_{3,4}$**	**M_5**	**M_n**	**M_p**	**M_8**	**M_9**	**M_{10}**
W/L	115/0.6	416/0.5	840/0.5	840/0.5	230/0.6	230/0.6	230/0.6	230/0.6

Figure 4.11 shows a simplified small-signal equivalent circuit model of the loop amplifier, where the two stages are represented as a transconductance amplifier. The transconductance of $M_{1,2}$ and M_5 are

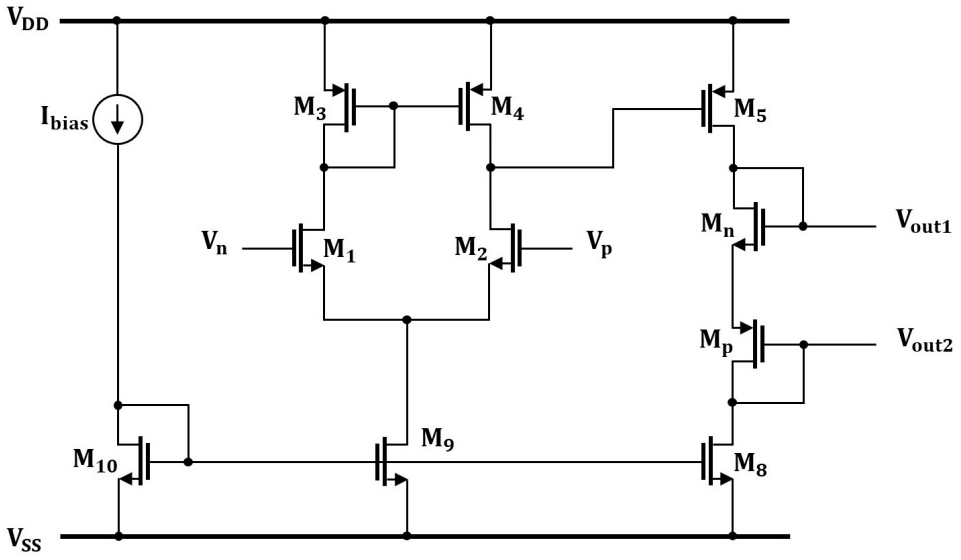


Figure 4.10: Two stage circuit topology of the loop amplifier.

equal to 6.2 mS and 16.3 mS, the output impedance of the first stage R_{out1} and the second stage R_{out2} are 5.6 kΩ and 2.1 kΩ. Each stage contributes gain in the order of 30.6 dB. The output of the circuit corresponds to the node V_{out1}. The capacitance at node V_2 is mainly formed by the Miller capacitance but also includes parasitic capacitances connected to the output of the first stage. The capacitance at node V_3 is the total parasitic capacitance connected to the node V_{out1}. The total DC gain is 61.5 dB. Clearly, the circuit exhibits two poles. The dominant pole established by the first stage appears at 3.4 MHz. The second stage provides a pole at 250 MHz.

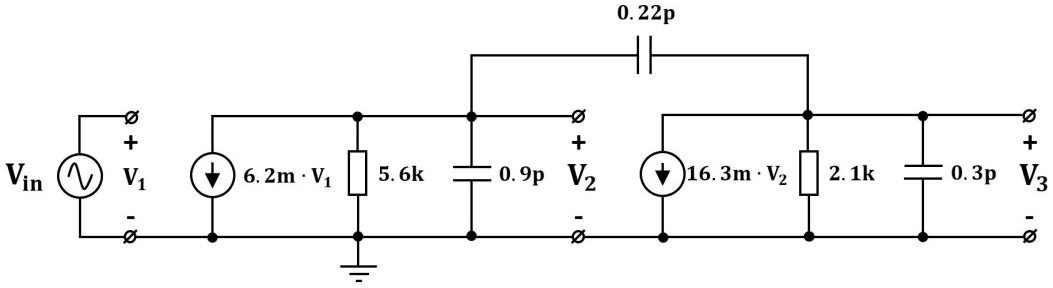
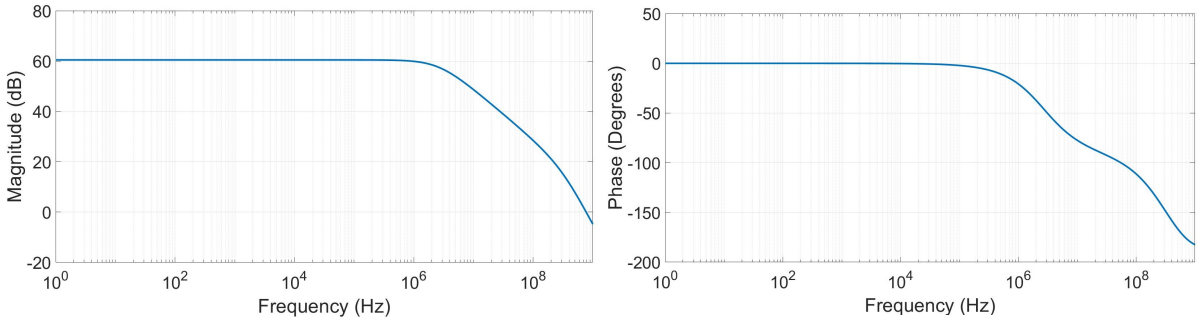


Figure 4.11: Small signal equivalent circuit model of the loop amplifier.

The bode plot of the loop amplifier shown in Figure 4.12 confirms these results. The poles are widely spaced and occur at the above mentioned frequencies, the DC gain is 62 dB.



(a) Magnitude plot.

(b) Phase plot.

Figure 4.12: Frequency response of the loop amplifier.

Figure 4.13 depicts the small-signal equivalent circuit model of the three-stage cascade, where the two stages of the loop amplifier have been combined with the equivalent circuit of the output stage. The output impedance of the third stage is increased by the value of R, resulting in 3.17 Ω. The output stage is loaded by the parasitic capacitance of the transducer C_e equal to 2.5 nF.

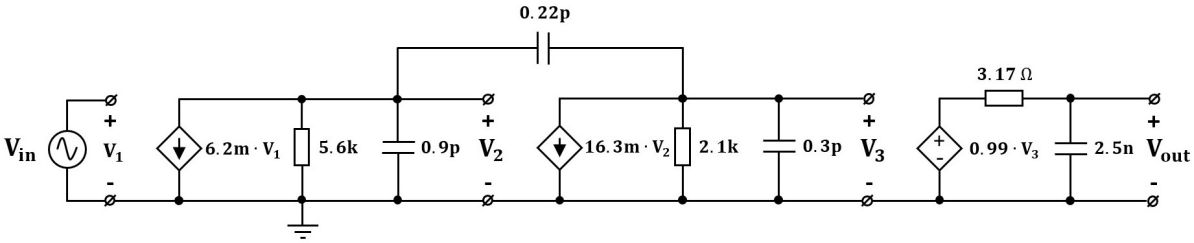


Figure 4.13: Small signal equivalent circuit model of the transmitter circuit.

The presence of the capacitive load at the node V_{out} causes an additional third pole to arise in the system. The pole is located at 20 MHz. Since it lies too close to the pole formed by the first stage, this poses a significant risk for the amplifier to get unstable when negative feedback will be applied around it. In order to investigate the stability of the system, the frequency response of the loop gain has been plotted. The circuit used for this is shown in Figure 4.14. The opamp consists of the circuit given in Figure 4.11, the class AB output stage is shown outside the opamp. After setting the input signal to zero, the test signal V_{test} is injected in the feedback loop. The loop gain is determined as a ratio of the return signal V_r and the feedback signal V_f. The obtained result is given in Figure 4.15.

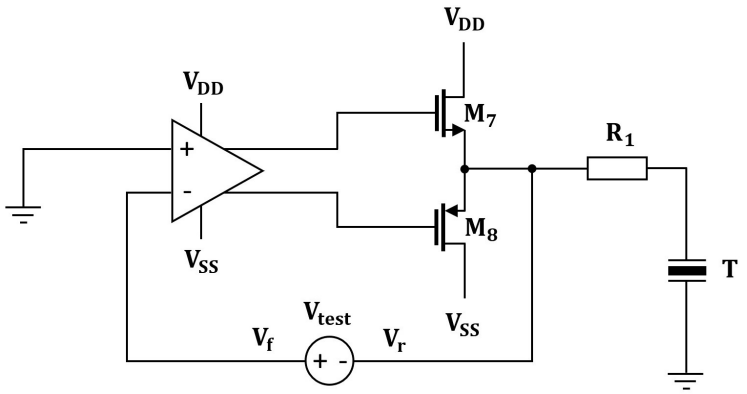
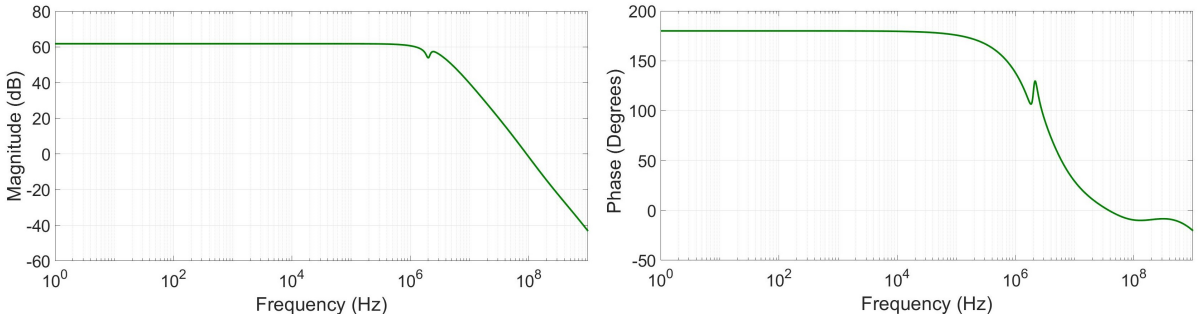


Figure 4.14: Simulation circuit used to plot the frequency response of the loop gain.



(a) Magnitude plot. **(b)** Phase plot.

Figure 4.15: Frequency response of the loop gain the transmitter circuit.

As one can see, the proximity of the two poles causes the magnitude to drop with 40 dB per decade resulting in second-order roll-off behavior. The slope intersects the 0 dB point at 91.6 MHz. In the

phase plot, this frequency corresponds with the negative phase shift of -9.2°. Therefore, there is no phase margin left, indicating that the system is unstable. This is confirmed by Figure 4.16, showing the pole-zero map for the closed-loop configuration.

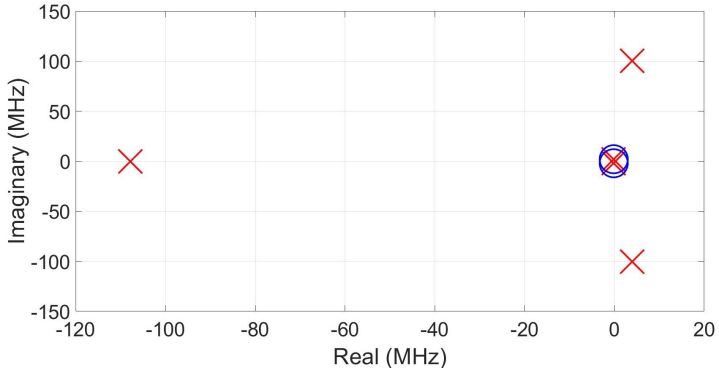


Figure 4.16: Pole-zero map of the transmitter circuit before frequency compensation.

The resonance points of the transducer are represented by a pair of the complex conjugate zeros and poles located near the origin at 2 MHz along the imaginary axis. The poles and the zeros cancel each other and thus they do not pose an instability issue in the system. The pole along the real axis is just beyond the crossover frequency and thus the phase lag associated to this pole erodes the phase margin. The instability is caused by the two complex conjugate poles lying in the right half of the complex plane. It is obvious that these unstable poles will produce an oscillation with a frequency of 100 MHz in the amplifier. This situation is demonstrated in Figure 4.17, showing the response of the amplifier on a step signal.

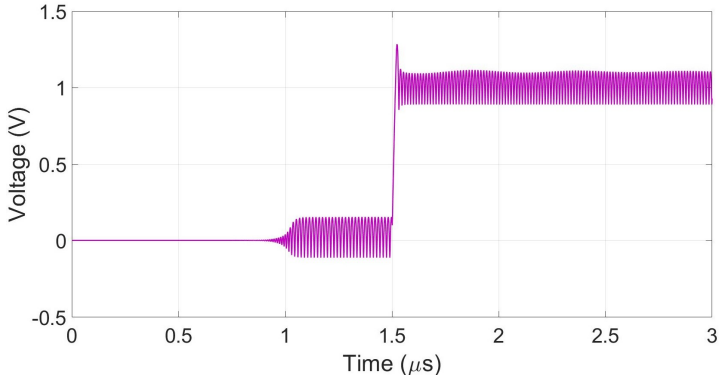


Figure 4.17: Step response of the transmitter circuit before frequency compensation.

As can be seen, the output signal starts to oscillate even before the external signal has been applied. It is evident that the transmitter is unstable and thus the circuit is in dire need of frequency compensation.

4.3. Frequency compensation

The open-loop transfer function of the amplifier consists of three essential poles: a real pole at the crossover frequency and a pair of low-frequency complex conjugate poles. Once the negative feedback loop is closed around the amplifier, the complex conjugate poles are pushed by the high gain of the amplifier into the unstable region, according to the root locus shown in Figure 4.18.
In order to prevent this, the poles have to be moved away from each other. A side effect arising from this solution is a bandwidth reduction resulting in a gain drop at the transducer resonance frequency. Therefore, the phase margin that can be achieved by pole splitting, while maintaining a gain of 40 dB at 2 MHz, is highly limited. For this reason besides pole splitting, the frequency compensation needs additional steps and is implemented as follows:

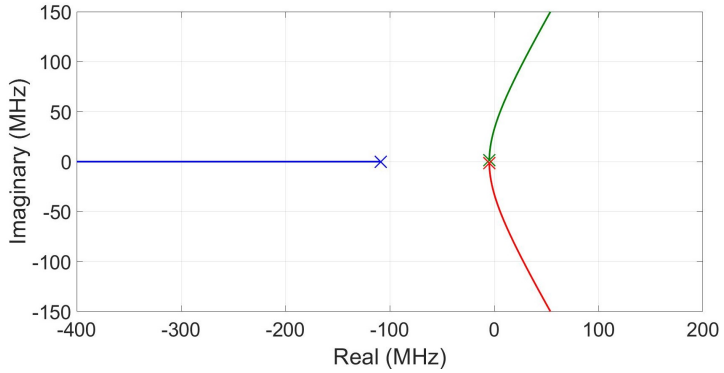


Figure 4.18: Root locus of the transfer function of the transmitter ciruit.

- A compensation capacitor C_c of 2 pF has been inserted between the output of the first and the second stages as shown in Figure 4.19. Due to the Miller effect, the capacitance is multiplied by the gain of the second stage, whereby the pole of the first stage is moved to low frequency, while the pole of the second stage is shifted further away from the crossover frequency. The pole formed by the output stage does not experience any effect and thus it remains at its place. Since there are still two poles before the crossover frequency, they both contribute to the phase lag in the system. The amplifier becomes stable, however, the phase margin is quite small;
- Besides relocating the poles, the capacitance C_c creates a right half plane zero, which has a negative effect on the phase margin. The resistance R_c of 2 kΩ placed in series with C_c causes the zero to move into the left half-plane. The phase lead resulting from this is used to improve the phase margin;
- The value of resistor R has been increased from 0.5 to 2 Ω. By doing this the load capacitance is isolated from the amplifier, which leads to a phase margin boost [13].

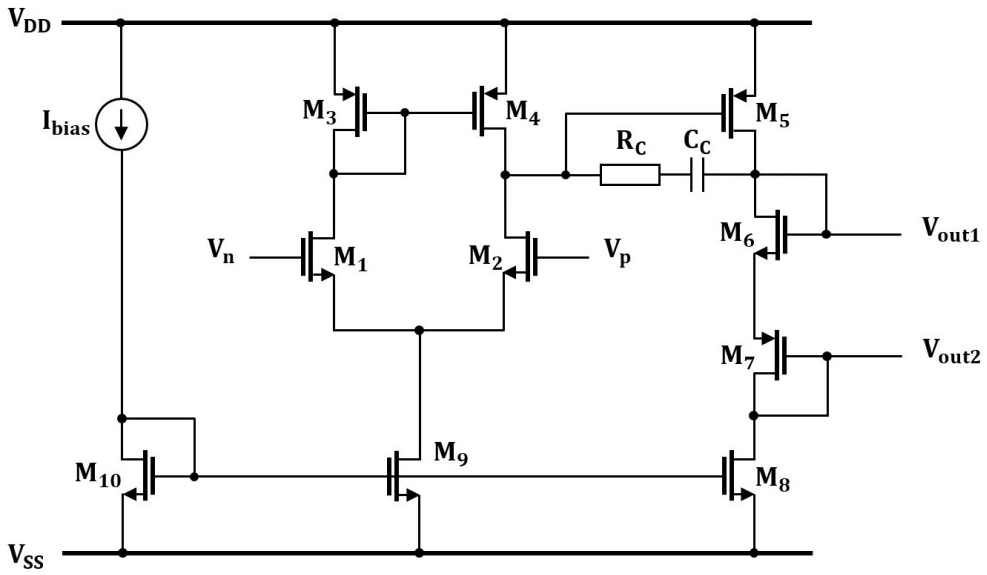


Figure 4.19: Loop amplifier circuit including the Miller frequency compensation.

Figure 4.20 illustrates the pole-zero map of the closed-loop configuration after the frequency compensation. The complex conjugate poles lie in the left half-plane. The pole seen before at 100 MHz has moved to a high frequency. Instead of this, a zero has appeared at low frequency.
Figure 4.21 shows the bode plot of the loop gain before and after frequency compensation. It is clear that due to pole splitting the bandwidth of the amplifier has shrunk. The gain at 2 MHz has dropped

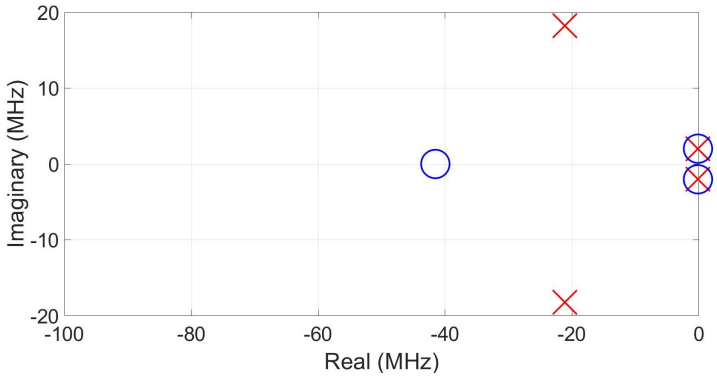
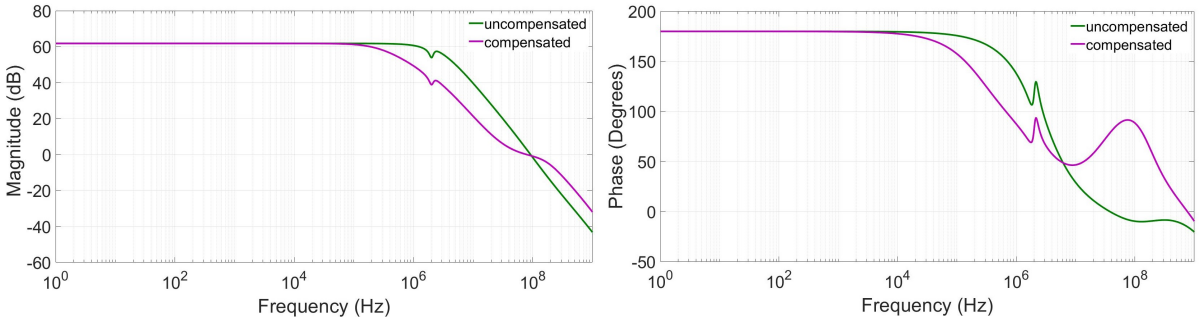


Figure 4.20: Pole-zero map of the transmitter circuit after frequency compensation.

from 60 to 40 dB. The magnitude roll-off slope after passing both poles is -40 dB/decade. The poles are followed by the zero point, which adds 20 dB/decade and lets the plot pass the 0 dB point with the slope of -20 dB/decade. Beyond the crossover frequency, the third pole is approached and the slope returns to -40 dB/decade. The phase plot shows the considerable improvement of the phase margin. The total phase lag of 180^{o} due to two poles is greatly compensated by the phase lead of the zero, resulting in the large phase margin of 83^{o}.

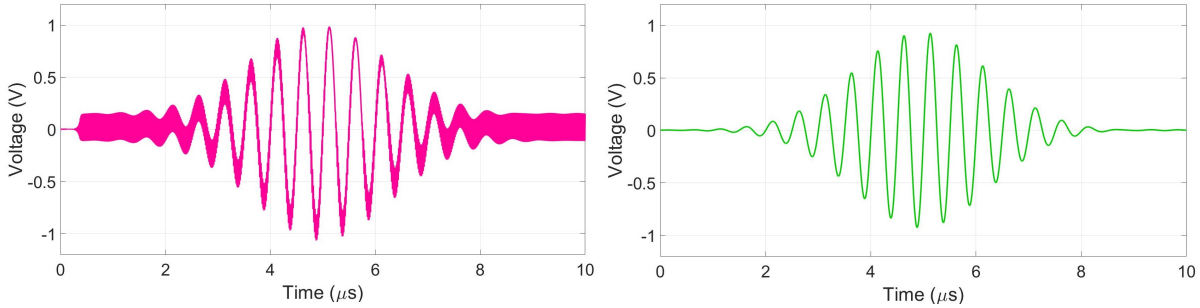


(a) Magnitude plot.

(b) Phase plot.

Figure 4.21: Frequency response of the loop gain the transmitter circuit before and after frequency compensation.

The effect of the frequency compensation in the time-domain is shown in Figure 4.22. The plot represents the voltage over the transducer with the Gaussian pulse as the input signal. There is an obvious difference between the signals. Before the frequency compensation, the signal is heavily corrupted by the high-frequency oscillation. After the frequency compensation, the undesirable oscillation is completely eliminated.

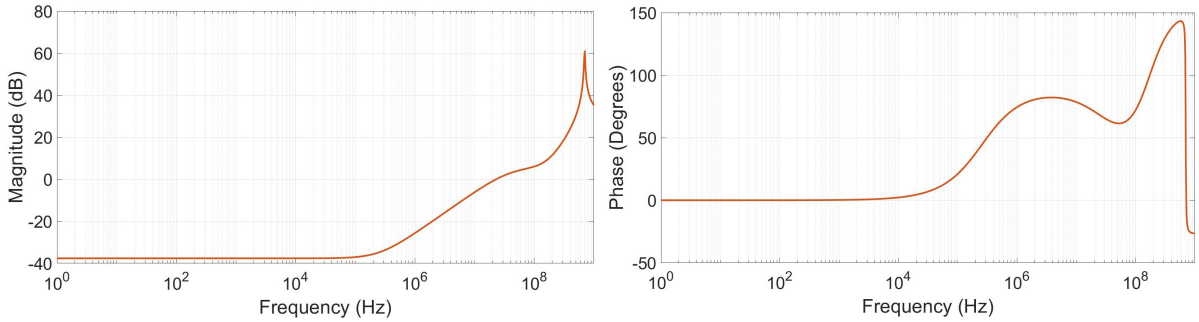


(a) Before frequency compensation.

(b) After frequency compensation.

Figure 4.22: Voltage waveform across the transducer.

The bode plot of the transmitter output impedance is shown in Figure 4.23. As can be seen, the impedance, being a purely ohmic resistance at low frequencies, turns into an impedance with an inductive character at high frequencies. The magnitude and the phase at 2 MHz are equal to 86.34 mΩ and 77.3^{o} respectively.



(a) Magnitude plot. **(b)** Phase plot.

Figure 4.23: Frequency response of the output impedance of the transmitter circuit.

The simulation circuit model of the flow measurement system is given in Figure 4.24 to evaluate the zero-flow error. The buffer in the transmit circuits consists of the three-stage cascaded amplifier. As has been mentioned earlier, the impedances R_1 and Z_{rx1} are set on 2 Ω. The impedances at the opposite side R_2 and Z_{rx2} remain at the same values of 1 Ω.

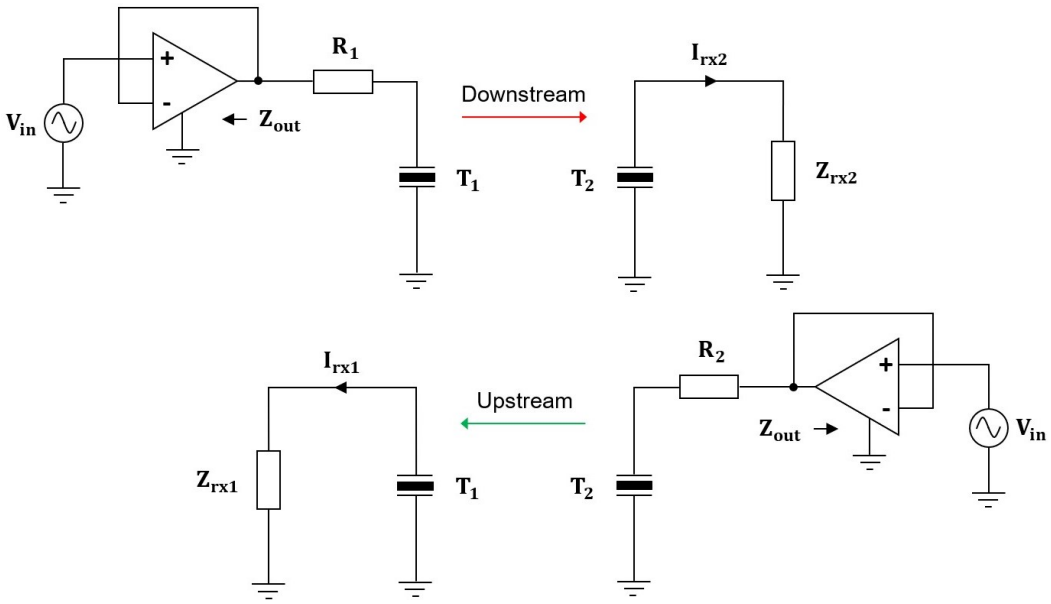


Figure 4.24: Flow measurement system model where TX1 and TX2 have been replaced with the three stage cascaded amplifier, the test conditions: R_1=Z_{rx1}=2 Ω, R_2=Z_{rx2}=1 Ω and Z_{out}=88.24∠77.3^{o} mΩ.

The zero-flow error results in 50.1 ps. The error is mainly caused by the difference in the magnitude and the phase shift between the impedances. The mismatch in this situation appears at both sides of the system. The obtained zero-flow error is below the maximum allowable value of 100 ps. So, the next step is the design of the receiver, of which the input impedance should match the output impedance of the transmitter as close as possible.

4.4. Receiver design

Figure 4.25 shows the transmitter circuit used as a receiver. The main difference between the receiver and the transmitter is that the receiver has to provide amplification of the signal. It is readily seen,

that the designed transmitter circuit is not able to amplify the received signal I_{rx1} and thus, in order to be used as a receiver, it has to be equipped with an additional amplification feature. Such a circuit is shown in Figure 4.26.

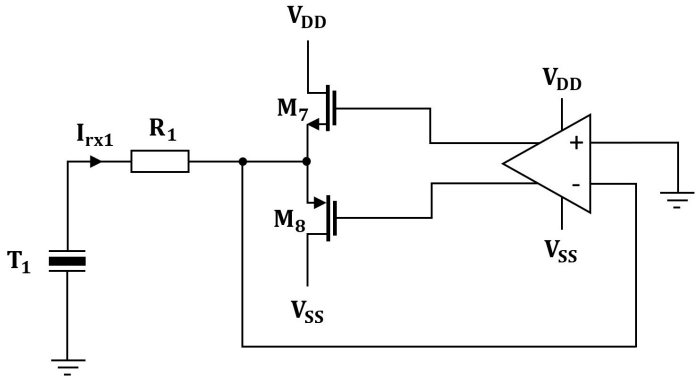


Figure 4.25: Transmitter circuit used in receive mode.

As one can see, there are 4 additional transistors included in the circuit. The devices M_9 and M_{10} appear in series with M_7 and M_8 in the output stage and form a current mirror with M_{11} and M_{12}. The drains of M_{11} and M_{12} are tied together and connected with the resistance R_L. The receive transducer is represented by the current source I_{in} in parallel connection with the resistance R_m and the capacitance C_e.

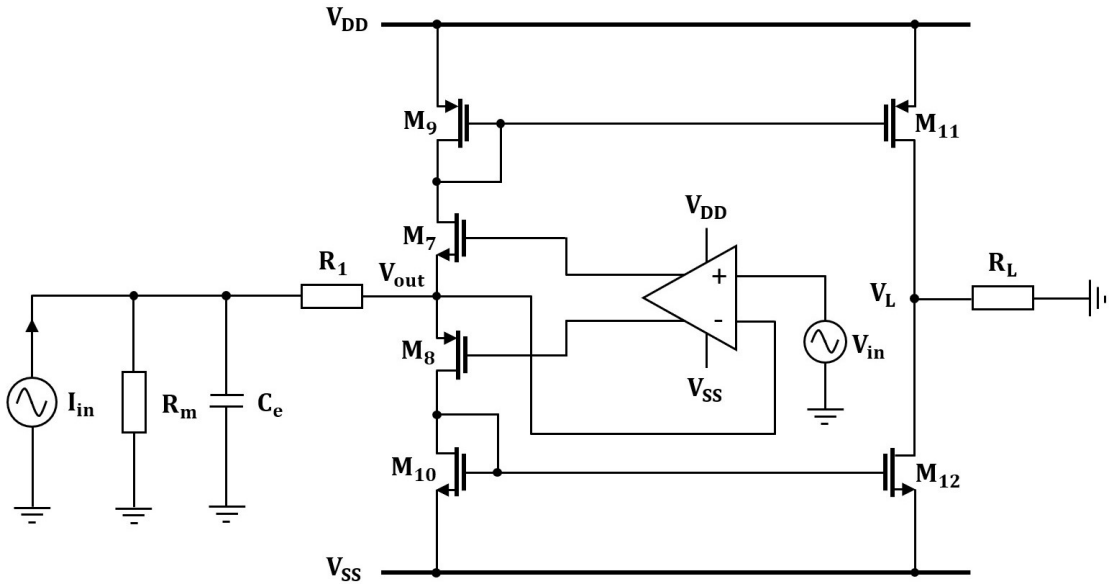
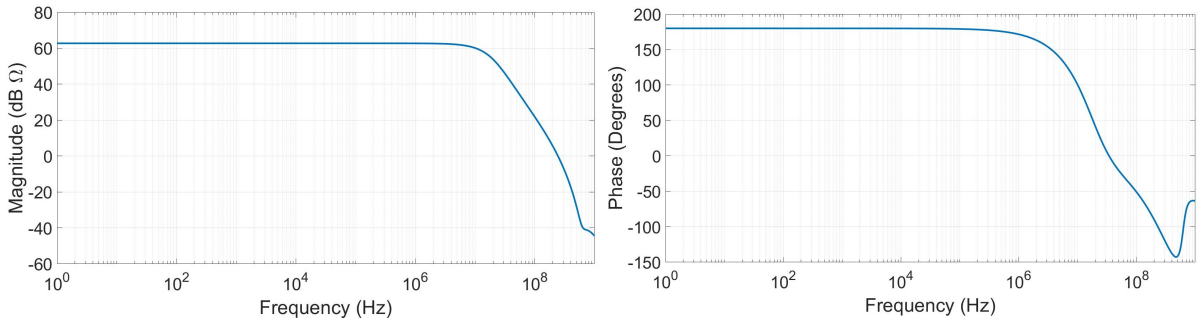


Figure 4.26: Unity-gain feedback amplifier with an additional amplification stage used in transmit/receive mode.

The circuit operates as follows. At the beginning, it is in transmit mode. The input signal V_{in} is applied to the amplifier input. The transducer is driven by the output stage, which is functioning as the class AB stage. The analysis described earlier for the class AB output stage also holds in this situation. The only difference is that the impedance seen by looking up and down from the node V_{out}, is increased by the impedance of diode-connected devices M_9 and M_{10}. These impedances are small and they have a minor effect on the output impedance of the circuit. After V_{in} becomes zero, the circuit stays connected to the transducer and is ready to be used in receive mode. The output impedance of the transmitter Z_{out} turns into the input impedance of the receiver Z_{in}. The value of Z_{in} is smaller than the impedances of R_m and C_e and thus the current almost entirely flows into the output stage. The inverting terminal of the amplifier draws negligible current, hence I_{in} will be flowing through the output stage. This current is sensed by M_9 and M_{10} and fed to the stage composed of M_{11} and M_{12}, where it is converted into the

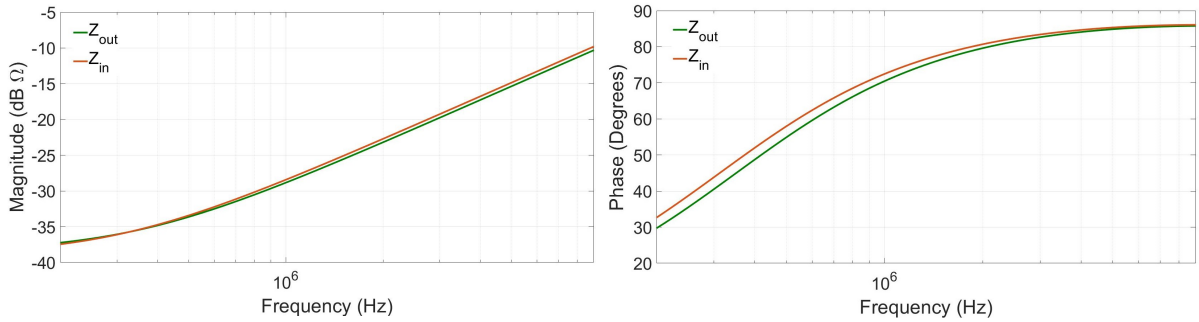
voltage V_L.
Figure 4.27 shows the bode plot of the transfer function V_L/I_{in} of the circuit in receive mode with the value of R_L equal to 2 kΩ.



(a) Magnitude plot. **(b)** Phase plot.

Figure 4.27: Frequency response of the receiver circuit.

The gain at 2 MHz is equal to 62 dBΩ and the phase shift is 30°. In a real flow measurement system, RX1 and RX2 are two separate ICs. Due to the tolerances in the manufacturing process, their transfer functions will not be identical. The differences in the gain and the phase introduce a mismatch between the measured signals and thus this will lead to an increase of the zero-flow error.
Though the transmitter and the receiver are implemented by the same circuit, there is still a mismatch between Z_{in} and Z_{out}. It is caused by the design and imposes the minimum limit on the zero-flow error. The reason for its occurrence is associated with the different operation modes of the output stage. During transmit mode, the output stage behaves as the class AB stage. The current varies, causing the impedance Z_{out} to decrease. In receive mode, the output stage is in standby. There is only a small quiescent current through the stage and thus the impedance Z_{in} remains at its maximum constant value. Since the impedances have an inductive character at 2 MHz, the absolute value and the phase of Z_{in} will slightly differ from that of Z_{out}. This is illustrated in Figure 4.28. The plot indicated as "Z_{out}" demonstrates the situation with a positive voltage swing at the output node V_{out}, when M_7 and M_9 are conducting and M_8 and M_{10} are off. The magnitude change is from 73.2 mΩ to 69.2 mΩ, the phase change is from 80.7° to 79.6°. The presence of the series resistances R_1 and R_2 in the circuit, significantly compensates the difference between Z_{in} and Z_{out}.



(a) Magnitude plot. **(b)** Phase plot.

Figure 4.28: Frequency response of the transmitter output impedance and the receiver input impedance.

4.5. Noise analysis

The magnitude of the received signal depends on several factors, namely: the value as well as the number cycles of the input signal V_{in}, the transducer size, the distance between the transducers, and the losses in the fluid. Two transducers with a diameter of 10 and 20 mm have been tested experimentally in different setups. From the obtained results the amplitude of the received signal I_{in} lies in the range from 100 µm to 5 mA. To be able to sense low amplitude signals, the receiver must have a low noise

level over the bandwidth of the transducer. Table 4.4 displays the simulation results obtained from the noise analysis.

Table 4.4: Dominant noise sources in the receiver before noise reduction.

Device	Parameter	RMS Noise Contribution (V)	% Of Total
M_2	f_n	0.83e-3	40.97
M_1	f_n	0.83e-3	40.93
M_4	i_d	0.27e-3	4.32
M_2	i_d	0.27e-3	4.25
M_1	i_d	0.27e-3	4.24
M_3	i_d	0.26e-3	4.04
R_m	r_n	55.01e-6	0.18
M_{12}	f_n	49.63e-6	0.14
M_{12}	i_d	48.53e-6	0.14
M_{10}	i_d	48.53e-6	0.14

The given values represent the RMS noise voltages over the bandwidth 1-3 MHz referred to the node V_L. As can be seen, the most noise is contributed by the first stage of the amplifier. The flicker noise of the differential pair is the dominant noise source in the circuit. It is followed by the thermal noise produced by the differential pair and the active load. The noise from the transducer is low due to the small value of R_m.
The noise sources shown in Tab. 4.4 generate a total input refereed RMS noise current of 0.83 µA. Using the lowest value of 100 µA for the received signal, results in the SNR of 38.6 dB. In order to boost the SNR value, the first stage and the output stage have been resized as follows:

- The width and the length of the devices M_1 and M_2 have been increased by a factor of 5. By doing this the area of the devices is increased by a factor of 25. Since the flicker noise power is inversely proportional to the area of the devices, the flicker noise from the differential pair is reduced considerably;

- The width of the devices M_1-M_4 and M_9 has been scaled up by a factor of 5. As a result, the bias current through the first stage becomes 5 times larger, which in turn increases the transconductance of $M_{1,2}$. The thermal noise produced by the first stage is inversely proportional to the transconductance $g_{m1,2}$ and thus its value lowers;

- Additionally, the width and the length of the devices M_9-M_{12} have been increased by a factor of 3 to decrease the flicker noise from the output stage.

Figure 4.29 shows the noise spectral density plot before and after the noise reduction.

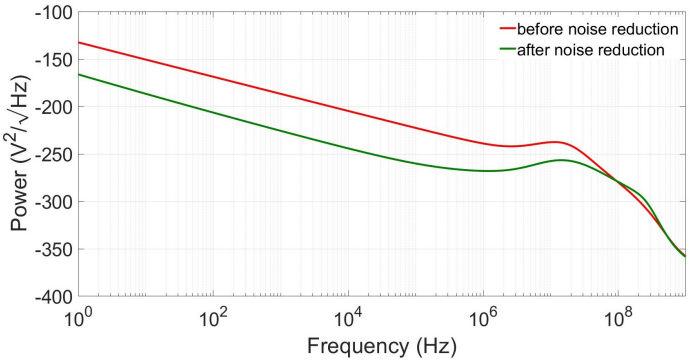
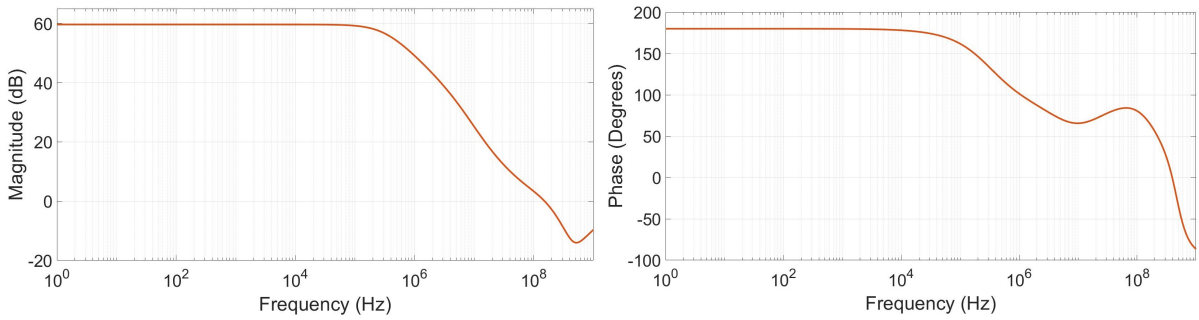


Figure 4.29: Noise spectral density of the receiver circuit before and after noise reduction.

The noise floor has been lowered and the total input referred RMS noise current has dropped to 0.18 µA. Thereby the SNR value is improved up to 51.8 dB.
With the increase of the transistors area, the parasitic capacitances of the transistors have been increased as well. Moreover, the raise of the bias current of the first stage changes its output impedance. An extra phase lag caused by the pole shift in the complex plane, erodes the achieved phase margin. It drops to 16°. The phase margin is recovered by the adjustment of the chosen earlier C_c and R_c to 5 pF and 500 Ω. The bode plot of the loop gain is shown in Figure 4.30. The phase margin of 68.63° ensures the stability of the circuit.



(a) Magnitude plot. **(b)** Phase plot.

Figure 4.30: Frequency response of the loop gain of the receiver circuit.

4.6. Overall performance

So, the transmitter and the receiver that make up the flow measurement system, have been implemented. As in the foregoing sections, the measure of the circuit performance is to determine the zero-flow error in the system. This is done with the simulation model shown in Figure 4.31. As one can predict, all system components TX1, TX2, RX1, and RX2 are identical. Figure 4.32 reveals the voltages across the load resistor R_L while transmitting and receiving the signal.

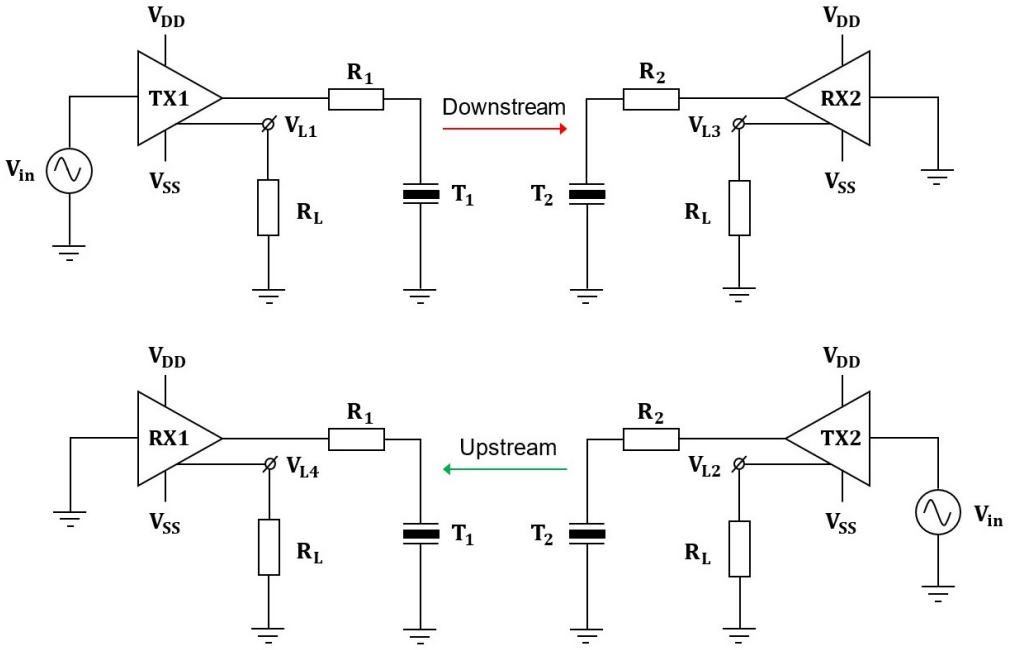
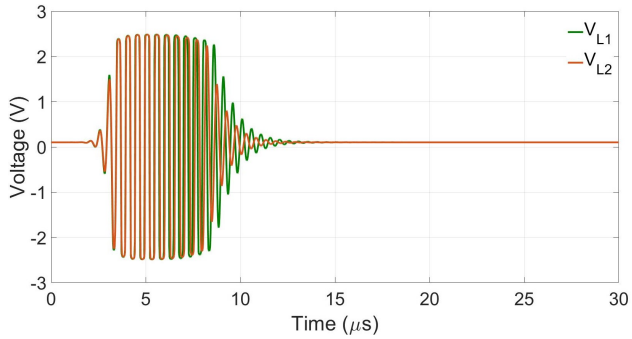
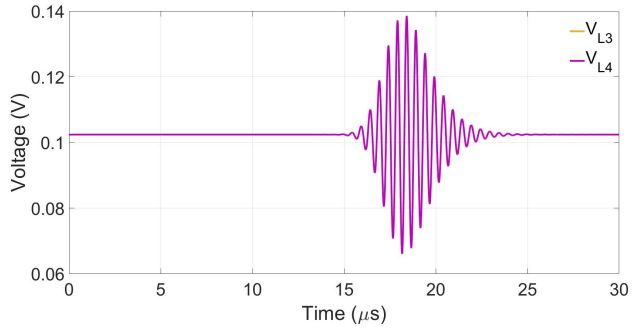


Figure 4.31: Flow measurement system model where TX1, TX2, RX1, and RX2 have been replaced with the circuit shown in Figure 4.24, the test conditions: R_1=2 Ω and R_2=5 Ω.



(a) Output voltage of the amplifier in transmit mode.



(b) Output voltage of the amplifier in receive mode.

Figure 4.32: Voltage measured across the load resistance R_L in (a) transmit and (b) receive mode.

It does not come as a surprise, that there is a signal over the resistance R_L in transmit mode. Due to the presence of the current mirror in the output stage, the current caused by the transmitted signal is fed to R_L, where it is amplified by 60 dBΩ. Keeping the length of the Gaussian pulse short allows this signal to die out before the signal from the opposite side has been received. Applying cross-correlation on the received signals gives a zero-flow error of 30 fs. This is much lower than the maximum allowable value of 100 ps.
The achieved characteristics of the final circuit are summarized in Tab. 4.5.

Table 4.5: Summary of the achieved circuit parameters.

Parameter	Value
Power supply	± 2.5 V
DC supply current	15 mA
Receiver gain	60 dB
Open loop gain	60 dB
Output impedance	70 mΩ
Phase margin	68.6°
RMS noise voltage BW=1-3 MHz at V_L	0.29 mV
Zero-flow error with R_1=2 Ω, R_2=5 Ω	30 fs

In a practical situation TX1 and RX1 as well as TX2 and RX2 represent two different ICs and thus there will be a mismatch between their characteristics. In order to simulate this, the bias current of TX2 and RX2 has been increased by 20% relative to TX1 and RX1. This results in a zero-flow error of 50 fs.
It is obvious that an additional mismatch can arise between the received signals when the measurement equipment or an extra circuit for further signal processing is connected to the node V_L. Therefore, in order to minimize the zero-flow error increase, the test conditions at both sides should be matched as close as possible.

5

IC design

For the designed amplifier an IC has been developed. In this chapter, the chip layout and the results obtained from the post-layout simulation are presented.

5.1. Pinout diagram

The design proposed in this thesis greatly simplifies the flow measurement system. It consists of two identical circuits, each of which is used alternately in the transmit and the receive mode. The design is implemented as an IC and presented by a pinout diagram, as shown in Figure 5.1.

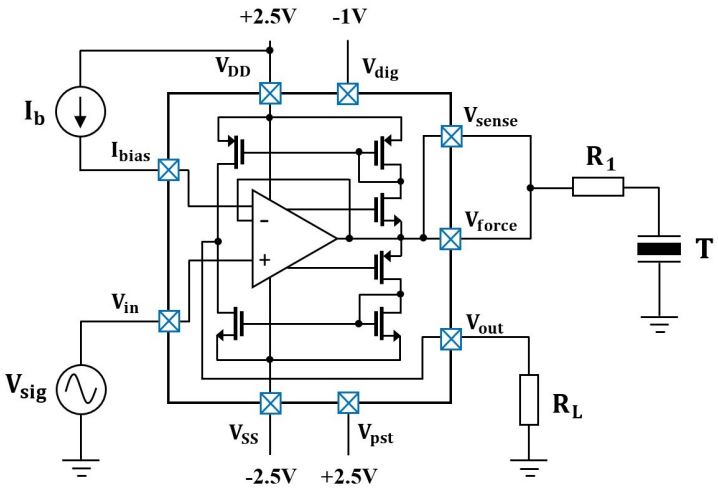


Figure 5.1: Pinout diagram of the IC.

The IC includes the loop amplifier, the output stage, and the additional receive stage. The bias current I_b is generated externally. The resistors R_1 and R_L are placed off-chip. Using a variable resistor for R_L allows adjustment of the amplification of the received signal. The analog pads V_{DD} and V_{SS} provide the power supply for the amplifier. The digital pads V_{dig} and V_{pst} are intended for the padring.

5.2. Layout

Figure 5.2 shows the layout of the overall IC. Two bypass capacitors C_1 and C_2 of 5 pF and 10 pF are connected between V_{DD} en V_{SS} for supply noise suppression. The chip micrograph is shown in Figure 5.3. Figure 5.4 zooms in on the layout of the loop amplifier. In order to avoid cluttering, the routing is not shown. The layout has been drawn in compliance with the following design rules:

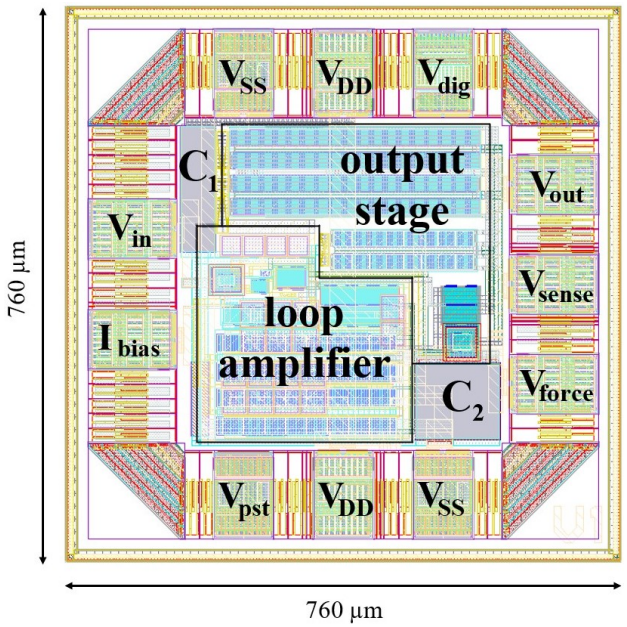


Figure 5.2: Chip layout.

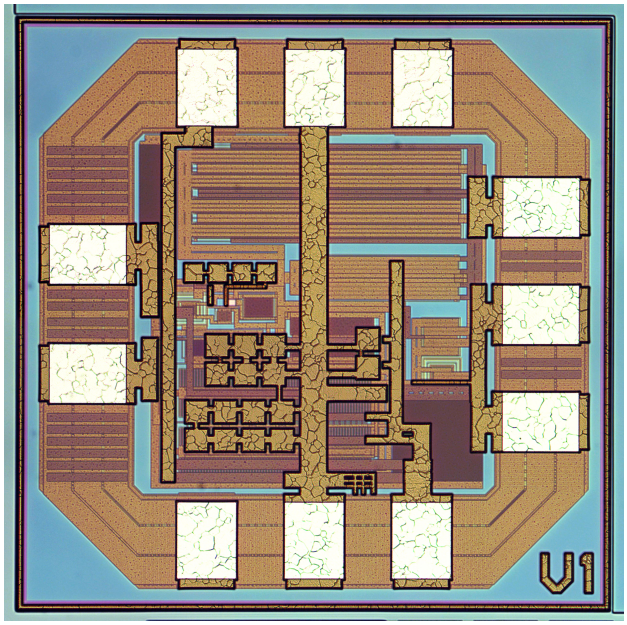


Figure 5.3: Chip micrograph.

- Large size transistors are split into smaller multiple transistors. In order to keep the gate resistance low, the length of the gate is limited to 20 µm;
- To minimize the nonidealities in the circuit caused by linear gradients of the oxide/doping profiles, the devices $M_{1,2}$ and $M_{3,4}$ are arranged in a common-centroid pattern;
- For a better device matching accuracy, dummy fingers are placed along the edges of the transistor arrays.

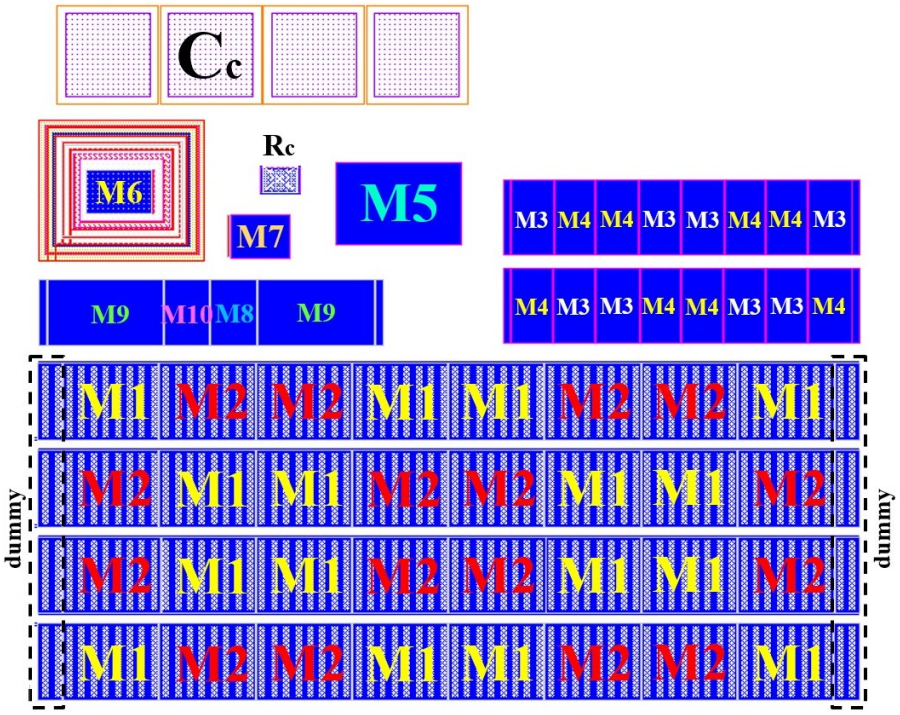
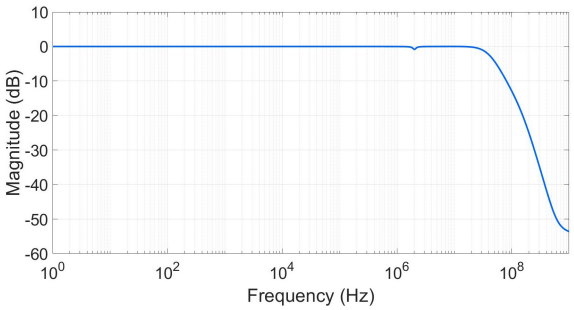


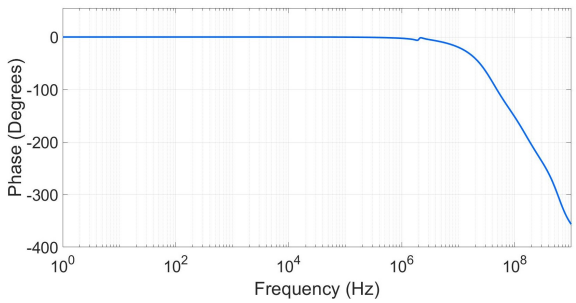
Figure 5.4: Floor plan of the loop amplifier layout.

5.3. Post-layout simulation

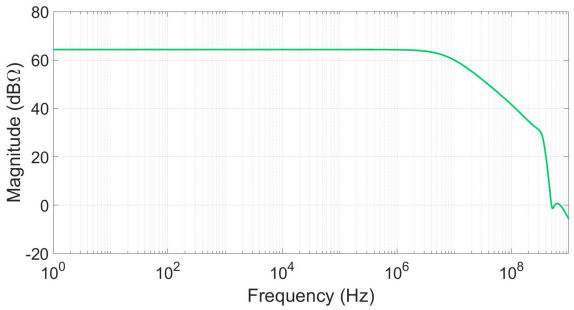
To verify the completed design, final simulations have been run in which extracted parasitic capacitances of the amplifier and the padring are taken into account. The obtained results are shown in Figure 5.5 and 5.6.



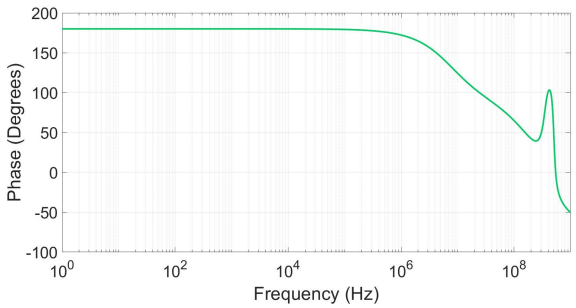
(a) Magnitude frequency response in the transmit mode.



(b) Phase frequency response in the transmit mode.

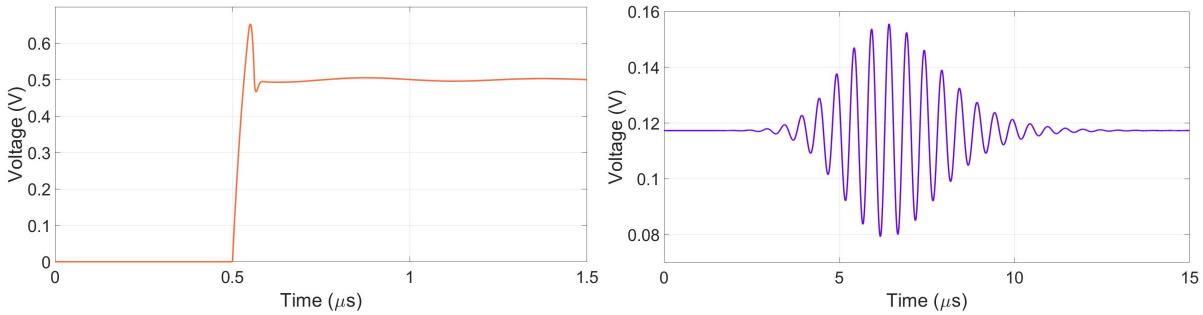


(c) Magnitude frequency response in the receive mode.



(d) Phase frequency response in the receive mode.

Figure 5.5: Post-layout simulation including the extracted parasitic capacitances from the padring and the amplifier.



(a) Step response in the transmit mode.

(b) Gaussian pulse response in the receive mode.

Figure 5.6: Post-layout simulation including the extracted parasitic capacitances from the padring and the amplifier.

There is no performance degradation observed in either transmit or receive mode. With a slight decrease of the bandwidth in the receive mode, the gain remains at the expected value of 60 dBΩ. The time-domain signals confirm the stability of the circuit. There is an increase of the zero-flow error up to 70 fs, but that is still far below the maximum allowable value of 100 ps.

6

Conclusions

The goal of this master thesis was to develop a system consisting of a transmitter and a receiver, in which the reciprocity property is utilized for ultrasonic transit-time flow measurements. This implies that the offset error commonly present at zero-flow condition would be reduced, resulting in an accuracy increase of ultrasonic flow meters.

The preliminary problem investigation and subsequent design steps, have led to the successful achievement of the assigned goal. The simulation result demonstrates a significant decrease of the zero-flow error compared to prior work. The cross-correlation method yields a value of 30 fs, which is also far below the maximum allowable value of 100 ps. The zero-flow error results reported in [2], [3] lie in a wide range of hundreds of picoseconds to tens of nanoseconds, exceeding the result obtained in this thesis at least by three orders of magnitude. The specified result of the zero-flow error is based on simulation and clearly, there might be some increase of its value in real test conditions. Yet, it is expected that there will be an improvement of the result obtained in previous designs. This result has been achieved by using the same circuit for the transmitter and the receiver. This is the main feature, that distinguishes the proposed design from systems provided in prior work. Using one and the same circuit is the simplest and best way to match the output impedance of the transmitter and the input impedance of the receiver. The circuit has been implemented as a three-stage operational amplifier in unity-gain feedback configuration. The class AB output stage of the amplifier has been equipped with an additional function being used in the receive mode for sensing and amplification of the signal. The gain of the receiver can be adjusted by an externally-placed resistance up to a maximal value of 70 dBΩ at 2 MHz. Due to the different operating modes of the output stage in the transmit and the receive phases, a small mismatch still remains between the impedances. The absolute value varies between 73.2 mΩ and 69.2 mΩ, while the phase varies between 80.7^{o} and 79.6^{o}. The difference of the input-output impedance is compensated with a purely active resistance connected in series with the amplifier's output.

In addition to minimizing the zero-flow error, the proposed design also has other advantages. Sharing the same circuit for both operating phases simplifies the flow measurement system. It relieves one from switching between the transmitter and the receiver. As a result, the switching network disappears from the system. This allows the amplifier to be placed closer to the transducer or perhaps even be integrated with it. Furthermore, the size occupied by the entire system is reduced.

It is also worth mentioning, that the proposed design is a low voltage design. Most of the currently used systems utilize a pulser for the transducer excitation, which requires voltages of ~30-40 V. In this system, the power supply voltage is limited to $\pm$ 2.5 V.

The low input-output impedance value prevents signal loss and thus results in a higher power efficiency of the system. Reducing the number of functional blocks in the system also contributes to efficiency increase. Moreover, using a Gaussian pulse instead of the step function as the excitation signal gives rise to a larger amplitude of the received signal and hence, to a higher value of the SNR.

The amplifier is internally compensated. Applied frequency compensation ensures circuit stability with a phase margin of 67^{o}.

An IC prototype has been developed and manufactured. The step following this work is to design a test-setup to be used for the verification of the obtained simulation results in real measurements.

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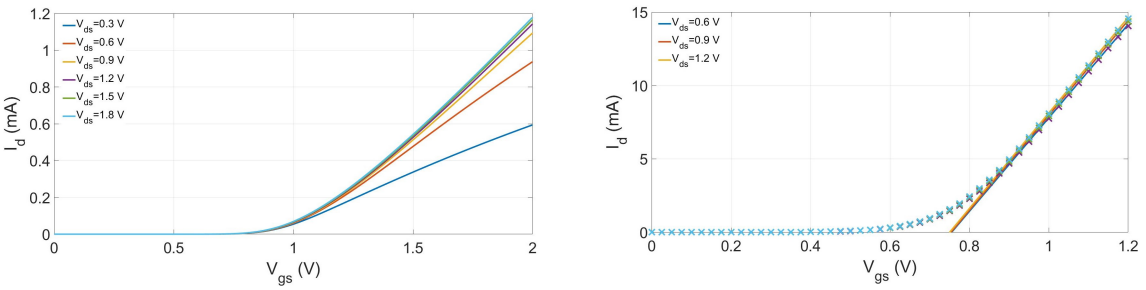
Appendix

The design proposed by this thesis is implemented in TSMC-18 process technology by using low voltage devices *nmos5V* and *pmos5v*. First of all, the basic simulations of the devices have been performed in order to extract a few model parameters, namely: the process parameter μC_{ox}, the threshold voltage V_{th} and the channel length modulation parameter λ. The obtained results are approximate values, however, they are quite suitable for rough estimation of the device sizes during circuit design. The extraction process is described as following for the NMOS device. The values of V_{th} and μC_{ox} are extracted from the input characteristic of the transistor. Figure 1a shows a set of I_d - V_{gs} curves of a single NMOS device. During the simulation V_{gs} is gradually increased from 0 to 2 V, while V_{ds} is incremented with a step of 0.3 V. The device size is W/L=10µm / 0.6µm.



(a) Input characteristics I_d-V_{gs}.

(b) Linear fitting of the input characteristics $\sqrt{I_d}$-V_{gs}.

Figure 1: Simulation result for obtaining V_{th} and μC_{ox} of the NMOS device.

Once $V_{gs} \geq V_{th}$ and $V_{ds} \geq 0.6$ V the device operates in the saturation region. However, as V_{gs} remains increasing, the device turns into the velocity saturation region. This is indicated by a change of the quadratic behaviour of the curves into the linear increase. The saturation current without considering the channel length modulation, can be described by the simple quadratic model given by [8]:

$$I_d = \frac{1}{2} \cdot \mu C_{ox} \cdot \frac{W}{L} \cdot (V_{gs} - V_{th})^2 \tag{1}$$

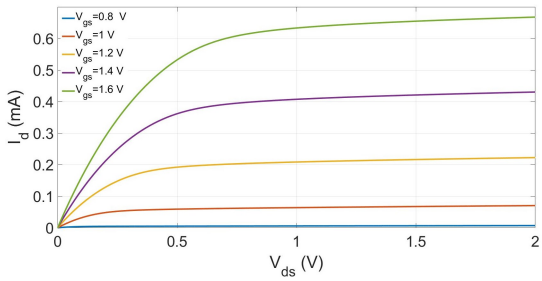
An easy way to get the values of V_{th} and μC_{ox} is first to plot $\sqrt{I_d}$ vs. V_{gs} and then using a linear function to fit resulting curves. This is done in Figure 1b. In order to avoid the triode region as well as the velocity saturation region, the fitting is performed for the limited range of V_{gs} and V_{ds}. The fitted linear functions can be estimated by the expression given by:

$$\sqrt{I_d} = \sqrt{\frac{1}{2} \cdot \mu C_{ox} \cdot \frac{W}{L}} \cdot (V_{gs} - V_{th}) \tag{2}$$

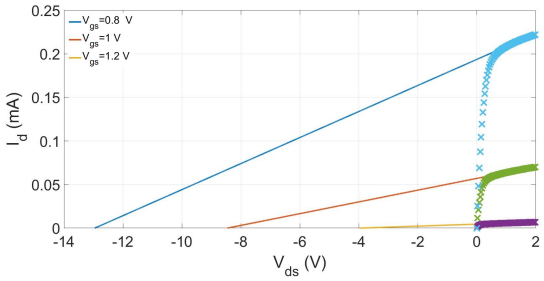
Therefore, the intersection of the fitted line with the V_{gs} axis provides V_{th}, while its slope is directly translated into μC_{ox} according to:

$$\mu C_{ox} = \frac{2 \cdot slope^2}{\frac{W}{L}} \tag{3}$$

The estimated values are found to be: V_{th} =0.74 V and μC_{ox}=130 µA/V^2.
The value of λ is extracted from the output characteristic of the transistor. Figure 2a shows a set of I_d



(a) Output characteristics I_d-V_{ds}.



(b) Linear fitting of the output characteristics

Figure 2: Simulation result for obtaining λ of the NMOS device.

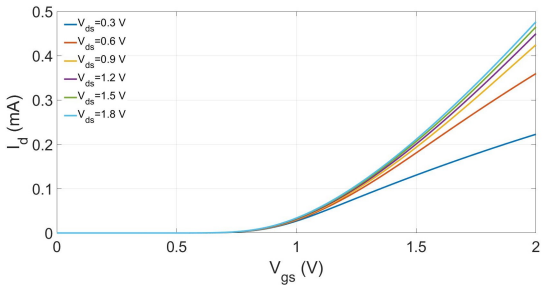
- V_{ds} curves of the NMOS device. During the simulation V_{ds} is gradually increased from 0 to 2 V, while V_{gs} is stepped with an increment of 0.2 V.
As V_{ds} exceeds the overdrive voltage V_{eff}, the device enters the saturation region and the current through it keeps increasing at a roughly constant rate. The saturation current including the channel length modulation into Eq. (1) is given by [8]:

$$I_d = \frac{1}{2} \cdot \mu C_{ox} \cdot \frac{W}{L} \cdot \left(V_{gs} - V_{th}\right)^2 \cdot \left(1 + \lambda \cdot V_{ds}\right) \tag{4}$$

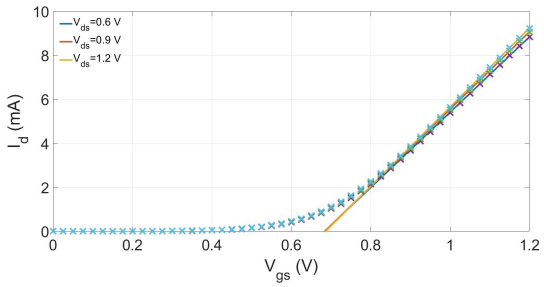
The value of λ is found by extrapolating of the linear fit in the saturation region toward I_d=0 A. This is done in Figure 2b. In order to prevent the result to be influenced by the velocity saturation effect, only the small values of V_{gs} are used. The intersection point of the fitted line and the V_{ds} axis corresponds with zero current and thus, the only solution of Eq. (4) is:

$$\lambda = -\frac{1}{V_{ds}}, \tag{5}$$

which is also known as Early voltage. As can be seen in Figure 2b, there is significant spread in the obtained voltages. This is mainly due to higher order effects which are not included in Eq. (4). These effects cause a non-constant slope in the saturation region leading to a poor fitting result. The average value of λ is found to be 0.14 V^{-1}.
Following the same procedure the parameters of the PMOS device have been extracted. The major steps are shown in Figure 3 and 4. The found results are summarized in Tab. 1



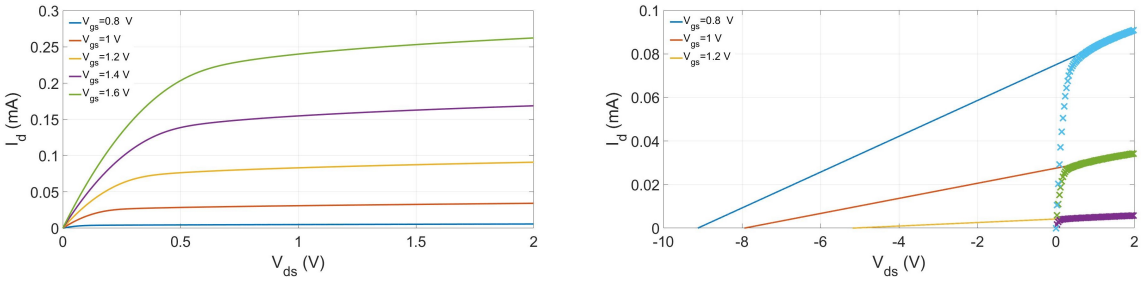
(a) Input characteristics I_d-V_{gs}.



(b) Linear fitting of the input characteristics $\sqrt{I_d}$-V_{gs}.

Figure 3: Simulation result for obtaining V_{th} and μC_{ox} of the PMOS device.

As can be seen, the PMOS transistor suffers from low mobility of the charge carriers and thus has lower current drive capability in comparison with the NMOS transistor. Therefore, if one wants to keep the same current through both devices, the PMOS should be made 4.5 times larger than the NMOS.



(a) Output characteristic I_d-V_{ds} .

(b) Linear fitting of the output characteristics

Figure 4: Simulation result for obtaining λ of the PMOS device.

Table 1: Device model parameters.

Parameter	NMOS W/L=10 µm / 0.6µm	PMOS W/L=10 µm / 0.5 µm
μC_{ox}, ($\mu A/V^2$)	130	30
V_{th}, (mV)	740	680
λ, (V^{-1})	0.14	0.14