A Deep Sub-Electron Temporal Noise CMOS Image Sensor with Adjustable sinc-type Filter to Achieve Photon Counting Capability

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A Deep Sub-Electron Temporal Noise CMOS Image Sensor with Adjustable sinc-type Filter to Achieve Photon Counting Capability

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***Abstract*—This letter introduces a Gm-cell based CMOS Image Sensor (CIS) achieving deep sub-electron noise performance. The CIS presents a new compensation block and low noise current source to improve the performance of Gm pixel. Furthermore, an optional 1st order IIR filter is implemented to improve the output swing. The conversion gain, full well capacity and dynamic range of the CIS can be easily adjusted by the charging time and the filter mode for different applications. The prototype chip is fabricated in a standard 180nm CIS process, and has a deep sub-electron read noise of 0.31e-rms at minimum (of the noise distribution) and 0.42e-rms at peak (of the noise distribution). A smooth and clear photon counting histogram is observed.**

***Index Terms*—CMOS image sensor, ultra-low noise, photon counting, sinc-type filter, noise distribution.**

I. Introduction

In recent years, the noise performance of CMOS image sensors (CIS) has been improved to reach deep sub-electron level (<0.5e-rms) [1-6]. Some of the pixels in a deep sub-electron CIS achieve photon counting capability [1][2][4][5]. A small floating diffusion (FD) node capacitance is necessary for these source-follower (SF) based CIS. Particularly, for the quanta image sensor [1][2], multiple frames are necessary to reconstruct the final image due to its low full well capacity (FWC) and usage of a 1-bit ADC. Recently, two non-SF-based CISs with 0.5e-rms noise have been reported [7][8]. In [7], a reference-shared in-pixel differential common-source amplifier is used to improve the conversion gain (CG) and the read noise. In [8], instead of reducing the FD node capacitance, a Gm amplifier and sampling capacitor constitute a sinc-type low-pass filter to improve the noise. However, the CG is fixed in [1-7] due to the principle of voltage domain sampling, which means the dynamic range and maximum SNR of the single frame are fixed and this solution is only suitable for the particular applications.

The photon counting histogram (PCH) is difficult to be observed in some of the deep sub-electron CISs, the PCH is a direct evidence for a deep sub-electron noise performance. The limitation could be the noise level, the stability of the CISs, the data acquisition system, the accuracy of the noise performance extraction, etc.

This paper presents a Gm-cell based CIS with 0.31e-rms minimum noise (at room temperature). It is fabricated in a standard 180nm CIS process, without special tricks around the FD node [1-4] and without 25V high voltages [4]. The PCH is observed to prove the accuracy of the noise performance extraction by using the photon transfer curve (PTC) method. The CIS has a compensation circuit block for the pixels, which allows for a narrower noise bandwidth of the filter and improves the temperature stability. Furthermore, an optional 1st order IIR filter is implemented to improve the output swing.

II. Image Sensor Design and Operation

Fig. 1 shows the conceptual block diagram of the CIS, including the pixel, low noise column current source, column filter and compensation block for the pixels. The pixel pitch is 10μm for low-light imaging. A thin oxide pMOS transistor M1 (W/L=0.5μm/0.18μm) and a thick oxide pMOS transistor M2 (W/L=0.5μm/0.9μm) constitute a Gm amplifier, which converts the voltage signal to a current signal I_P. For the purpose of fast auto-zero reset, a pMOS reset transistor MRST is used.

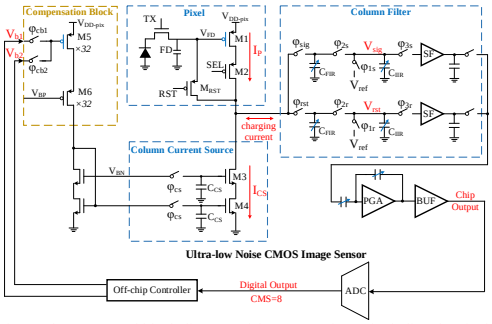

Fig. 1. The conceptual block diagram of the proposed CIS, including the pixel, low noise column current source, column filter and compensation block.

In the compensation block, M5 and M6 are identical to M1 and M2 respectively, which means they have the same temperature coefficient. Without the temperature compensation, the charging current I_P-I_{CS} (DC value) will change with temperature fluctuation due to the different temperature coefficient of M1 and M4. For example, the variation in the range from 20°C to 40°C without compensation is a few tenths of mA in the simulation. In order to minimize the mismatch and to reduce the settling time, multiple M5 & M6 (×32) are used. The area of M4 should be large enough to minimize the mismatch of the column current. The different columns and rows with the same pixel design shares the same compensation block. Furthermore, there are two bias V_{b1} and V_{b2} voltages to compensate for the charge injection effect of M_{RST}. Compared to [8], the charging current (DC value) can be precisely controlled, and the output swing or the maximum allowable charging time is drastically improved. The dominant pole of a sinc-type filter can be adjusted more flexibly.

The additional switches φ_{CS} and capacitors (C_{CS}=1pF) are used in

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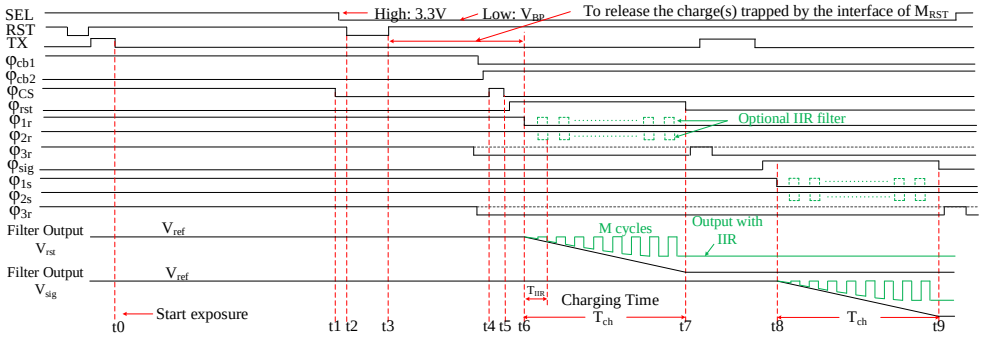

Fig. 2. The conceptual block diagram of the proposed CIS, including the pixel, low noise column current source, column filter and compensation block.

the column current source to block the spikes originated from V_{b1}/V_{b2} transition and the potential noise from other columns. There are two filter chains for the reset signal and light signal respectively. An optional IIR filter stage is implemented after the FIR stage in the analog domain. The gain of the filters can be adjusted both by the charging time and the filter mode.

Fig. 2 shows a simplified timing diagram of the readout phase. The pixel is selected by applying V_{BP}=1V to the gate of M2. At the falling edge of φ_{CS} (t1), the column current I_{CS}(t1), determined by V_{b1}, is locked. The auto-zero transistor M_{RST} is turned on at t2, and I_P will be equal to I_{CS} just before t3. Charge injection, which makes I_P lower, is introduced by the rising edge of RST (t3). To compensate this effect, φ_{cb2} is turned on after t3, and φ_{CS} is on to make I_{CS} lower during t4 to t5. Finally, I_{CS}(t5) determined by V_{b2} is locked after t5. In this work, the DC value of I_P is 1.5μA during the charging phase t6-t7 & t8-t9, and the corresponding DC value of I_{CS} is slightly lower than 1.5μA to guarantee the proper output range of the filter. In order to eliminate the effect of the random trapping-detrapping of the carriers located at Si-SiO_2 interface, the period from t3 to t6 should be longer than 100μs to release the trapped charge(s) of M_{RST} channel.

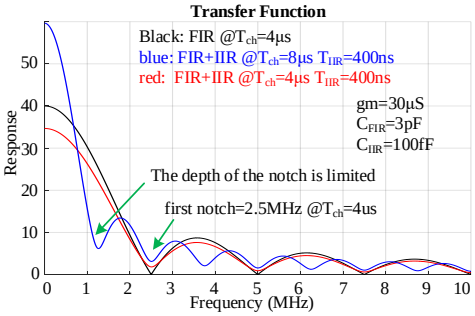

Fig. 3. Transfer function of FIR & FIR+IIR modes.

Equation (1) and (2) show the transfer function of the FIR filter and the FIR+IIR filter respectively [9]:

$$H_{FIR}(s) = \frac{gm \times T_{ch}}{C_{FIR}} \times \frac{1-\exp(-sT_{ch})}{sT_{ch}} \quad (1)$$

$$\begin{cases} H_{FIR+IIR}(s) = \left[\frac{gm \times T_{IIR}}{C_{FIR}} \times \frac{1-\exp(-sT_{IIR})}{sT_{IIR}}\right] \times \left[\frac{1-\alpha^M \exp(-sMT_{IIR})}{1-\alpha \times \exp(-sT_{IIR})}\right] \\ \alpha = \frac{C_{FIR}}{C_{FIR}+C_{IIR}} \end{cases} \quad (2)$$

T_{ch} is the total charging time, T_{IIR} is the time of one cycle at FIR+IIR mode, M is the cycle numbers of the IIR operation, gm is the transconductance of M1, C_{FIR} and C_{IIR} are the capacitance of the FIR stage and the IIR stage respectively. Fig. 3 shows the transfer function curves. With the same charging time T_{ch}, the gain of the FIR mode is larger. For FIR+IIR mode, the DC gain and the notches of the sinc response are limited by the second term in equation (2). If the charging time T_{ch} is long enough (M=T_{ch}/T_{IIR}), equation (2) can be simplified as:

$$H_{FIR+IIR}(s) \approx \left[\frac{gm \times T_{IIR}}{C_{FIR}} \times \frac{1-\exp(-sT_{IIR})}{sT_{IIR}}\right] \times \left[\frac{1}{1-\alpha \times \exp(-sT_{IIR})}\right] \quad (3)$$

In this case, the transfer function is only determined by T_{IIR}.

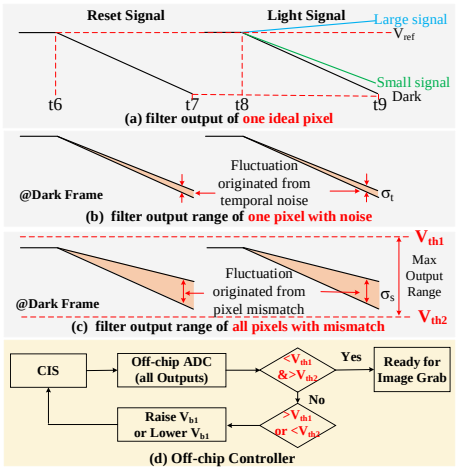

Fig. 4. (a)(b)(c) Filter output range under different conditions; (d) The conceptual diagram of the off-chip controller.

Fig. 4 shows the filter output fluctuation phenomenon before correlated double sampling (CDS) and the basic operation of the off-chip controller. As shown in Fig. 4a, the filters are reset to V_{ref}=1.7V before the charging phase. Ideally, V_{sig}(t9) is equal to V_{rst}(t7) in a dark frame. In a real pixel as shown in Fig. 4b, the outputs are affected by temporal noise and the corresponding fluctuations following a Gaussian distribution (standard deviation σ_t). In the whole pixel array as shown in Fig. 4c, the charging currents (DC value) are slightly different due to the pixel mismatch. And thus, a spatial noise or offset

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is introduced before the CDS operation. The corresponding standard deviation σ_s is much larger than σ_t (×3~4).

To ensure that all the Gm amplifiers of the pixels and all the column current sources can be operated in the saturation region, two threshold voltage V_{th1}=1.9V and V_{th2}=0.4V are set for the feedback control. If any output of the whole pixel array is out of range, V_{b1} will be adjusted to minimize the DC value of the charging current as shown in Fig. 4d. For a different I_P or transconductance value, the bias V_{b1} and V_{b2} should be adjusted first and then they are fixed. The DR and FWC are limited by both $|V_{th1}-V_{th2}|$ and σ_s in this chip.

As a conclusion, a thin oxide transistor M1, a compensation block, a low noise current source and an optional IIR filter stage are implemented to improve the performance compared to [8].

III. Measurement Results

The array size of the prototype sensor is 256×128, and the proposed pixel sub-array is 32×32. In the measurement, the slope of the PTC in the log-log scale must be checked carefully. If the slope in the log-log scale is not equal to 0.5, e.g., $\geqslant 0.505$ or $\leqslant 0.495$ considering measurement error, the timing diagram or the bias has to be adjusted to avoid the leakage, lag, etc., which leads to an inaccurate CG and noise (e-rms) extraction.

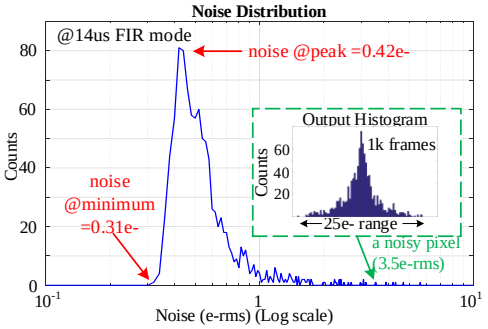

Fig. 5. The noise distribution @ 14 μs FIR mode.

Fig. 5 shows the noise performances of the CIS at room temperature. The best noise performance is measured by using the FIR mode with 14μs charging time. As shown in the noise histogram, the noise value of the peak in the distribution is 0.42e-rms, and the minimum noise in the pixel array is 0.31e-rms. The figure also gives an example of a noisy pixel. Only one peak is observed in the temporal noise histogram, which is very different from the random telegram signal (RTS) noise of a noisy pixel in a traditional SF based pixel.

In Fig. 6, the solid line and dashed line show the noise at the peak and minimum of the distribution respectively. For FIR mode (C_{FIR}=3.4pF), both the noise value at peak and the noise value at minimum are improved with a longer charging time. For FIR+IIR mode (C_{FIR}=3pF, C_{IIR}=100fF, T_{IIR}=400ns), the best noise performance is obtained with 4μs charging time.

Fig. 7 shows the dynamic range and full well capacity performance of the proposed pixels. The FWC can be easily controlled from 240e- to 5700e- by adjusting the charging time, and the corresponding DR is ranged from 55dB to 75.5dB in a single frame. The FIR mode and FIR+IIR mode can be used for different imaging applications. E.g., for the 0.5e-rms noise level imaging, the best DR and FWC are obtained by using FIR+IIR mode @T_{ch}=4μs. Fig. 8 shows the CG and the corresponding standard deviation σ_{CG}, both of them increase with increasing charging time. The variation of the CG is mainly from two sources. One is the mismatch of the pn junction capacitance of the FD node due to process fluctuation. Another source is the mismatch of M1 transconductance.

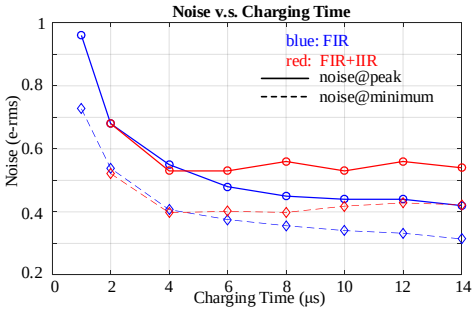

Fig. 6. The noise improvement v.s. charging time.

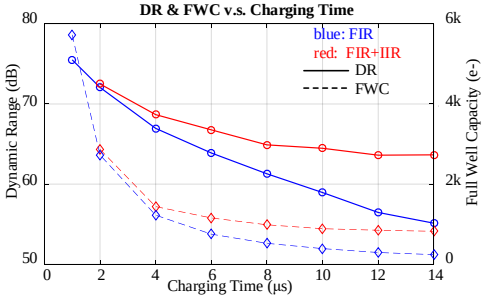

Fig. 7. Dynamic range & full well capacity v.s. charging time.

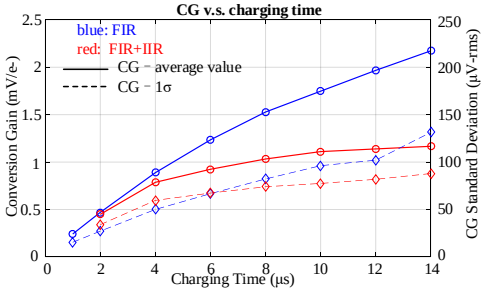

Fig. 8. Conversion gain & CG standard deviation.

Fig. 9(a) shows an example of PCH obtained by 512k frames at the FIR mode. The noise of this pixel is 0.31e-rms, and the main peak of the PCH is located at 16e-. Fig. 9(b) shows an example obtained at FIR+IIR mode. The noise is around 0.42e-rms, which is the threshold for observing discrete peaks in this chip. Thanks to the compensation circuit block, the data from 512k frames are stable at room temperature without any cooling system.

Fig. 10 shows the chip micrograph and 10 dark frames taken by the proposed sub-array (32×32). About 1%-2% of the pixels in the sub-array were observed to be noisy pixels. Table I shows the performance summary and comparison with other work in the same field.

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Table I Comparison of ultra-low noise CISs.

	This work	[2] IISW 2017	[3] ISSCC 2017	[4] EDL 2015	[5] EDL 2020	[7] ISSCC 2020	[8] TED 2017
Process	Standard 180nm CIS	45nm (pixel) 65nm (ASIC)	110nm	110nm	Standard 180nm CIS	90nm (CIS) 55nm (Logic)	Standard 180nm CIS
Noise reduction technique	sinc-type filter	pixel with tapered pump pate	CMS & RG-less pixel	CMS & RG-less pixel & 25V pulse for FD	dual CG & pMOS SF without body effect	in-pixel differential common-source amplifier	sinc-type filter
Pixel pitch (μm)	10	1.1	11.2	11.2(H) 5.6(V)	10	1.45	11
CG (μV/e-)	240~2200	345	172	220	115 / 250	560	90~1600
FWC (e-)	5700~240	*	4100	1500	6500	5800	/
Dynamic range (dB) @single frame	55~75.5	*	72.3	/	/	/	60~68
Noise (e-rms)	minimum: 0.31 peak: 0.42	peak: 0.22	peak: 0.44	peak: 0.27 @-10°C	onlyone pixel was shown: 0.32	peak: 0.5	peak: 0.5
PCH	observed (512k frames)	observed (20k frames)	/	observed (100k frames)	observed (1.5k frames)	/	/

*For this 1-bit quanta image sensor, the FWC and DR @single frame are meaningless.

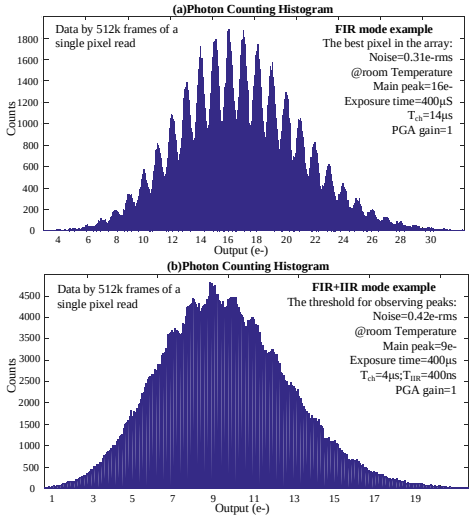

Fig. 9. Photon counting histogram examples.

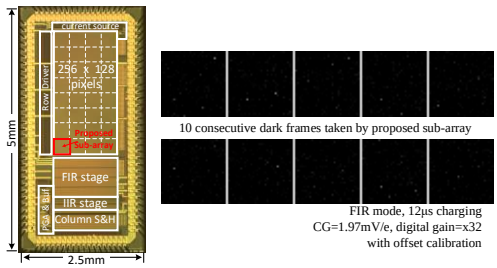

Fig. 10. Chip micrograph & 10 consecutive dark frames.

IV. Conclusion

This chip is fabricated in a standard 180nm CIS process, and has a deep sub-electron read noise of 0.31e-rms at minimum (of the noise distribution) and 0.42e-rms at peak (of the noise distribution). These outstanding noise characteristics are obtained by means of a CIS fabricated in a low-cost CIS process, without extra tricks or limitations in pixel design. A smooth and clear PCH is observed to prove the accuracy of the noise extraction by using the PTC method. For different applications, the CG, FWC and DR of the CIS can be easily adjusted by the charging time and the filter mode.

Acknowledgement

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