Novel Doping Free Metal-oxide Carrier Selective Passivating Contacts for Solar Cells

Yilong Zhou

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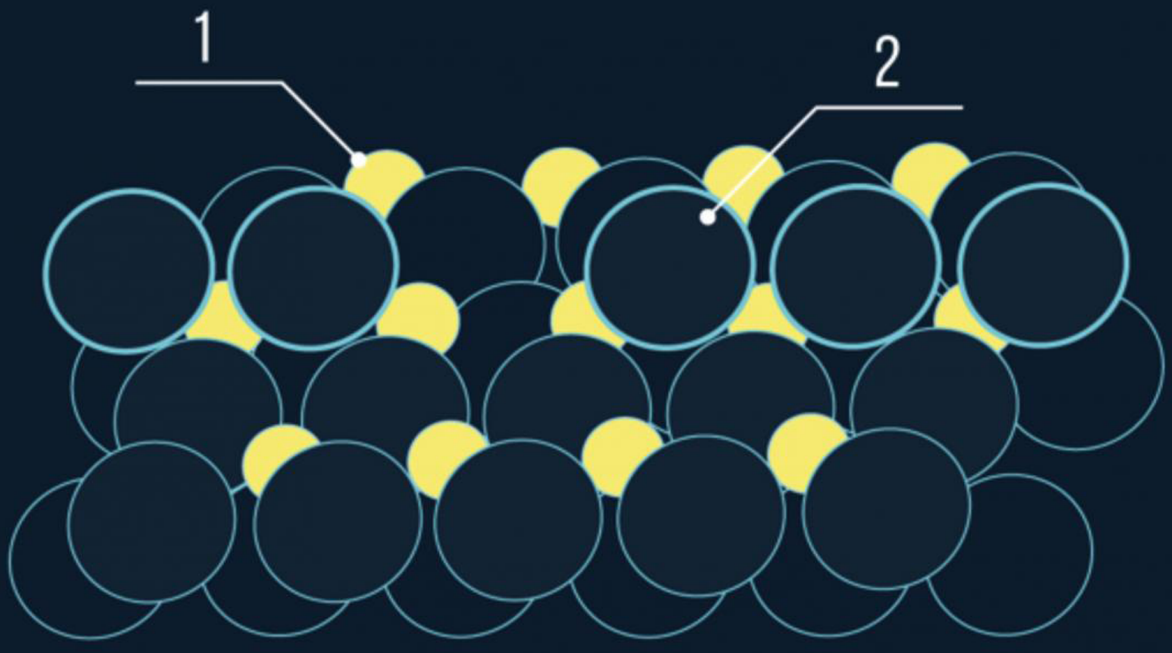
TU Delft



Novel Doping Free Metal-Oxide Carrier Selective Passivating Contacts for Solar Cells

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Yilong Zhou

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PVMD Group, Sustainable Energy Technology
EEMCS Faculty, Delft University of Technology

Graduate

Yilong Zhou

M.Sc. Sustainable Energy Technology

Faculty of Electrical Engineering, Mathematics and Computer Science

musezyl@gmail.com

Supervisors

Assoc. Prof. Dr. Olindo Isabella

Dr. Guangtao Yang

M.Sc. Thesis Committee

Prof. Dr. Miro Zeman, PVMD, ESE, TU Delft

Assoc. Prof. Dr. Olindo Isabella, PVMD, ESE, TU Delft

Assoc. Prof. Dr. Tom J. Savenije, Applied Science, TU Delft

Dr. Guangtao Yang, PVMD, ESE, TU Delft

Delft University of Technology

Department of Electrical Sustainable Technology

Photovoltaic Materials and Devices

Abstract

Carrier selective passivating contact (CSC) is considered to be a promising direction for surface passivation research because it performs passivation for both non-contacted and contacted areas. Conventional heavy doping CSCs are subject to a few drawbacks such as significant Auger recombination, parasitic absorption, complicated processing and relatively high fabrication cost. An alternative approach is by using transition metal oxides (TMO) where nm-thick metal oxides are introduced with easy and cost effective processes to realize the asymmetric conductivity for charge carriers. In this project, we investigated the passivation property and carrier selectivity of two types of TMOs, namely MoO_x as hole transport layer (HTL) and TiO_x as electron transport layer (ETL).

The performance of MoO_x based HTL is characterized at device level. By optimizing the metallization process, interfacial (i)a-Si:H layer thickness, textured surface pre-treatment and annealing conditions, an ultimate PCE of 17.60% is achieved, with Voc being 655 mV, Jsc being 38.36 mA/cm^2 and FF being 70.40%.

The passivation quality of TiO_x based ETL is characterized both by symmetric test for the passivation properties and at device level. First, the passivation property of single TiO_x layer and NAOS-SiO_2/TiO_x stacks are investigated. With the optimization of layer thickness and FGA conditions, a Voc of ~680 mV is obtained in both cases. After which, we investigated the passivation degradation caused by changing a new TiO_2 source material. We conclude that the passivation degradation is mainly attributed to the non-uniform TiO_x coating resulted from the reduced free mean path of evaporated TiO_x due to TiO_2 outgassing during deposition. Meanwhile, we also studied the influence of different interfacial layer between c-Si and TiO_x such as (i)a-Si:H thin layer where a Voc of ~660mV is achieved by using new TiO_2 source. Eventually, all optimized ETL structures are tested in FBC solar cells with p^+ poly-SiO_x at the front side as HTL. The results demonstrate that all cells are showing similar passivation quality (Voc=~575 mV) and the champion cell of 14.21% efficiency is achieved in c-Si/TiO_x stack, with Jsc being 30.53 mA/cm^2 and FF being 74.97%.

Keywords: Carrier selective passivating contact, transition metal oxides, TiO_x, MoO_x, passivation, solar cells

Table of Content

Nomenclature

PCE	Photo Conversion Efficiency
c-Si	Crystalline Silicon
PERL	Passivated Emitter with Rear Locally Diffused
PERT	Passivated Emitter with Rear Totally Diffused
CSC	Carrier Selective Passivating Contact
TMO	Transition Metal Oxides
HTL	Hole Transport Layer
ETL	Electron Transport Layer
FBC	Front Back Contacted
Poly-Si	Poly-crystalline Silicon
a-Si	Amorphous Silicon
iVoc	Implied Open Circuit Voltage
VB	Valence Band
CB	Conduction Band
PECVD	Plasma-Enhanced Chemical Vapor Deposition
ALD	Atomic Layer Deposition
a-Si:H	Hydrogenated Amorphous Silicon
DI Water	Deionized Water
HF	Hydrofluoric Acid
APCVD	Atmospheric Pressure Chemical Vapor Deposition
PVD	Physical Vapor Deposition
ITO	Indium-Doped Tin Oxide
QSSPC	Quasi-Steady-State Photoconductance
MSE	Mean Squared Error
J_0	Saturation Current Density
STC	Standard Test Conditions
Voc	Open Circuit Voltage
Isc	Short Circuit Current
FF	Fill Factor

Impp	Maximum Power Point Current
Vmpp	Maximum Power Point Voltage
XPS	X-ray Photoelectron Spectroscopy
TLM	Transfer Length Measurement
RTP	Rapid Thermal Process
pFF	Pseudo-Fill Factor
FGA	Forming Gas Annealing

1.Introduction

1.1. Background

The fast development of human society is placing insistent and pressing demand for energy. In 2015, the world total final fuel consumption was doubled compared to that in 1973 and it is believing that the number will keep increasing in the future [1]. Coming with which is the exhaustion of the traditional fossil fuels since they cannot be renewed, and the profound negative impact on the global environment. Therefore, it is of urgent task to develop sustainable energies which can both meet the demand of human society development and minimize the damage to the environment [2]. The primary source for sufficient and inexhaustible energy is the sun, which radiates more energy in one hour on earth than all the energy consumed annually by human beings. The idea of harvesting decentralized sunlight is by converting it into various energy forms such as hydro, wind and solar energy for later dispatch and distribution [3][4].

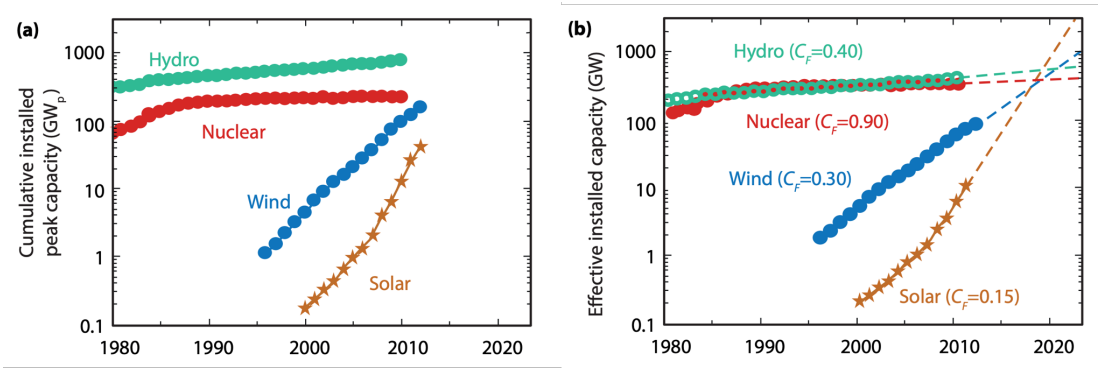

Figure 1.1 a) Development of the installed capacity of a few eco-friendly electricity generation technologies since 1980 [5]. b) After introducing the capacity factor and extrapolated until 2020 [5].

Among all these renewable energy forms, photovoltaic (PV) technology has been justified as the most promising energy carrier in the future due to the abundant sunlight source and its unique advantage of being used in a decentralized way [5]. Figure 1.1 (a) shows the installed capacity of eco-friendly electricity generation since 1980. We can

see that installed hydro and nuclear power are almost saturated, whereas wind and solar are still seeing a significant increase in installed capacity with a growth rate of around 20% and 40% respectively. Figure 1.1 (b) shows the extrapolation until 2020 by taking into account the capacity factors. We can foresee that solar energy will dominate the renewable energy market by 2020.

To achieve this goal, it is very important to increase the photo conversion efficiency (PCE) and reduce the fabrication cost. The rule-of-thumb is to minimize the carrier recombination in the crystalline silicon (c-Si) bulk material, at the cell surfaces and at the contacts. Plenty of research was made in the c-Si bulk material which has successfully increased the bulk carrier lifetime and brought down the fabrication cost [5]. Therefore, the bottleneck in further improving the performance of c-Si solar cells is the minimization of recombination at the cell surfaces and at the contacts. The state-of-the-art industrial solar cells implement single or a stack of dielectric layers (such as SiO_2, SiN_x and Al_2O_3) to realize surface passivation for non-contacted areas, while the contacts are generally passivated by heavy doping at the near surface of the c-Si [6]. However, the approach applied in such passivated emitter with rear locally diffused (PERL) or passivated emitter with rear totally diffused (PERT) cells requires high temperature diffusion and complex patterning process which leads to high cost [7].

Recently, carrier selective passivating contact (CSC) is considered to be a promising direction for surface passivation research. The advantage of CSCs over the traditional passivation technology applied in commercial solar cells is that they perform passivation for both non-contacted and contacted areas; therefore, besides an excellent passivation property for minority carriers is required, it is also expected to provide a good majority carrier conductivity. Current record efficiency of 26.7% for CSC based laboratory solar cell was achieved on thin intrinsic hydrogenated amorphous silicon (a-Si:H) layer with a thicker doped a-Si:H layer on top [8]. However, these heavy doping CSCs are subject to a few drawbacks such as significant Auger recombination, parasitic absorption, complicated processing and relatively high fabrication cost [7].

An alternative approach is by using transition metal oxides (TMO) where nm-thick metal oxides are introduced with easy and cost effective processes to realize the asymmetric conductivity for charge carriers. Figure 1.2 compares the work function as well as the band edges of different TMOs with that of c-Si. In general, TMOs with large work functions (such as VO_x, MoO_x, WO_x) are suitable as hole-selective contacts while

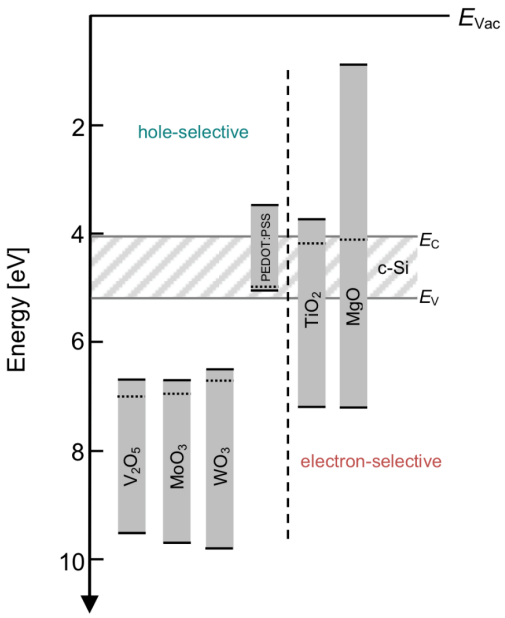

Figure 1.2. Work functions and band edges of a few metal oxides which are suitable as hole-selective contacts (left to dashed line) and electron-selective contacts (right to dashed line) [6].

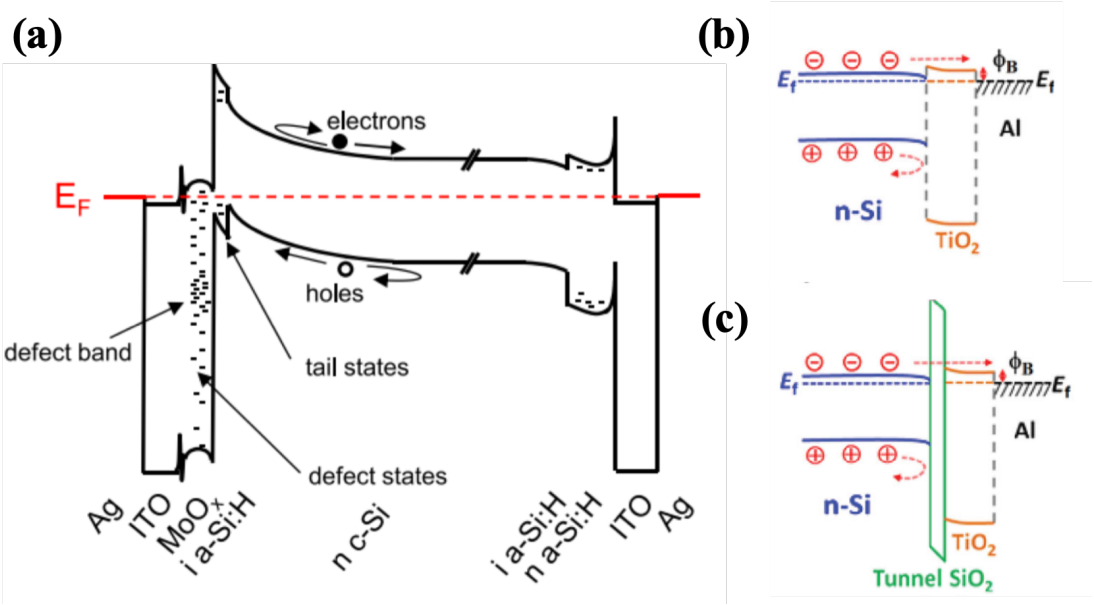

Figure 1.3 Band diagram of a) MoO_x based HIT solar cell [9] b) (n)c-Si/TiO_2/Al junction c) (n)c-Si/SiO_2/TiO_2/Al junction [7] where the material is indicated at the bottom, and the flow direction of electrons and holes is indicated by arrows.

those with low work functions (such as TiO_x and MgO_x) are demonstrated to be able to perform as electron-selective contacts. Impressive PCE of 22.5% has been achieved with MoO_x based silicon heterojunction solar cell [10] and with TiO_x (PCE: 21.6%) [7]. Figure 1.3 (a) shows the band diagrams of MoO_x based HIT solar cell. Due to the high

work function of MoO_x, a remarkable band bending takes place when MoO_x and (n)c-Si are touched which provides an asymmetric conductivity for holes and electrons. When electron-hole pairs are generated within the bulk due to incident photons, the electrons are repelled from the c-Si/MoO_x interface but holes can easily pass through as indicated by the carrier flow direction in Figure 1.3 (a). The holes then tunnel through both interfacial i-layer and MoO_x, and get extracted by the metal grids after being collected by the ITO layer. Figure 1.3 (b) and (c) show the band diagram of (n)c-Si/TiO_x with and without SiO_2 respectively. The band bending at the junction gives a small offset at the conduction band and a large offset at the valence band, which blocks the holes while allows electrons to tunnel through and get collected by metal. As it is still at the very early stage of research, solar cells with metal oxide CSCs are expected to give much higher efficiency in the future.

In this project, the passivation property and carrier selectivity of two types of TMOs are investigated. MoO_x is used as hole transport layer (HTL) to replace the traditional diffused poly-Si; the small valence band offset allows the holes to be collected whereas the large conduction band offset repels the electrons. On the other hand, the performance of TiO_x based electron transport layer (ETL) is also tested in front back contacted (FBC) cells where baron diffused poly-SiO_x is implemented as the front contact.

1.2. Objective

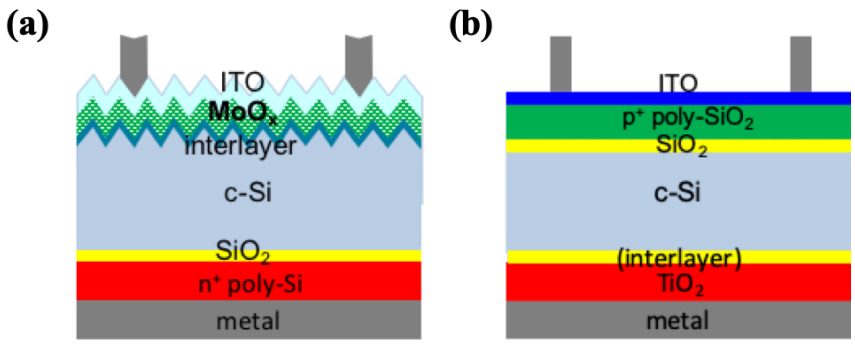

Figure 1.4 Cell architecture of a) MoO_x based FBC solar cell b) TiO_x based FBC solar cell

The main objective of this project is to fabricate FBC solar cells on the basis of MoO_x and/or TiO_x selective contacts respectively. The passivation property of metal oxide

was first optimized by symmetric test, then at the device level. Figure 1.4 (a) schematically shows the cell architecture of MoO_x based FBC solar cell. The rear side is passivated by SiO_2/textured (n^+) poly-Si stack whose excellent passivation (iVoc=721 mV) has already been demonstrated by Yang *et.al* [11]. The front side passivation is achieved by using (i)a-Si:H/MoO_x stack which is coated by ITO for carrier collection and transport. Figure 1.4 (b) schematically shows the architecture of TiO_x based FBC solar cell. The front side is passivated by p^+ poly-SiO_x with a good passivation quality (iVoc=700 mV) reported by Yang *et.al* [12]. The passivation at rear side is achieved by using TiO_x with or without interfacial layer. By using the standard heavy-doping selective contacts with demonstrated excellent carrier selectivity, the passivation quality in device is solely manipulated by the TMO carrier selective passivation layers.

1.3. Outline

This thesis is aiming to optimize the passivation property of MoO_x and TiO_x based HTL and ETL, and integrate these optimized doping-free carrier selective layers in FBC solar cells to characterize their performance at device level.

Chapter 2 gives a review on the fundamental semiconductor physics and working principle of solar cells. It covers the introduction of light property, carrier transport mechanisms and generation and recombination of charge carriers. Meanwhile, the surface passivation techniques for c-Si solar cells are also reviewed in the last section.

Chapter 3 focuses on the necessary processing technologies used for the fabrication of TMO based solar cells, including wet chemical processes (e.g. standard cleaning), various deposition techniques (e.g. LPCVD, PECVD, ALD and PVD) and doping and annealing processes. Their principle and corresponding effect on solar cell fabrication are both addressed in each section.

Chapter 4 reviews various characterization techniques that are required for identifying the passivation quality of TMOs. It covers both electrical and optical characterization methods whose working principle is first introduced, followed by the explanation of their application in this thesis project work.

Chapter 5 deals with the solar cell fabrication processes. A detailed explanation is given, step by step. Meanwhile, the optimized process conditions are also stated.

Chapter 6 presents the results of TMO surface passivation test and performance of

TMO based FBC solar cells. This chapter can be divided into two parts. The first part mainly focuses on the improvement of MoO_x based solar cells where the influences on the passivation property of MoO_x resulted from precursor structures, (i)a-Si:H thickness, texturing surface pre-treatment and annealing are discussed. The second part is mainly dealing with the optimization of TiO_x based solar cells where different ETL stacks (such as c-Si/TiO_x, c-Si/SiO_2/TiO_x, c-Si/(i)a-Si:H/TiO_x and c-Si/Ti/TiO_x) are characterized both on symmetric test level and device level. Meanwhile, the passivation degradation caused by PVD TiO_x source material is also investigated.

Chapter 7 summarizes the findings of this thesis project work, and an outlook is given which explains a few promising improvement methods for TMO based solar cells.

2. Background and Theory

Before diving into the research project, it is important to be equipped with some necessary fundamental theories. Since photovoltaic devices are usually dealing with the interaction between light and semiconductors, therefore, the first subsection gives a brief introduction about the nature of light, followed by basic semiconductor physics. The operation principle of solar cells is then introduced and the limitation factors (i.e. recombination mechanisms) in solar cells are discussed. Finally, a brief discussion about various surface passivation types and methods is given. All information provided in this chapter are based on the following materials: Solar Energy: The Physics and Engineering of Photovoltaic Conversion Technologies and Systems [5], Semiconductor Physics and Devices [13] *and Surface Passivation of Crystalline Silicon Solar Cells: Present and Future [6].*

2.1. The Nature of Light

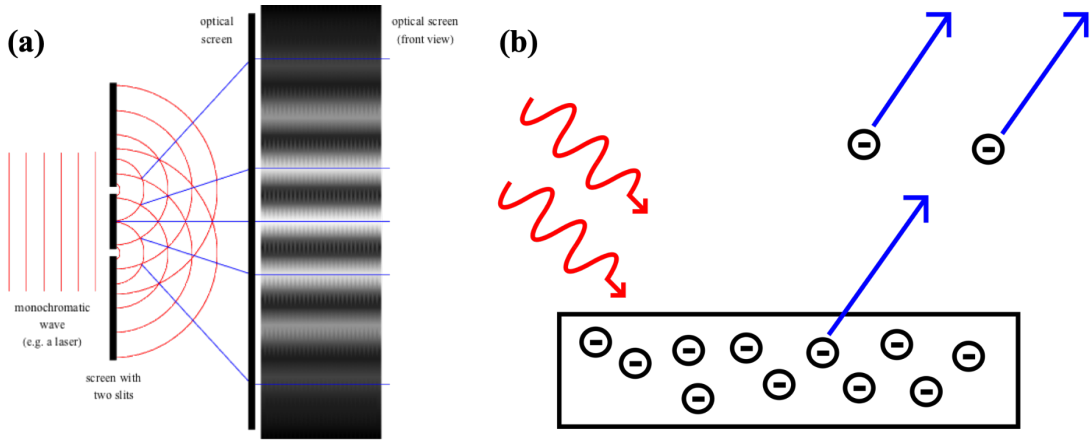

Figure 2.1 a) Double-slit Interference Experiment b) Photoelectric Effect

The nature of light has been debated for centuries and it was not until the beginning of 20th century that the wave-particle duality of light was accepted by the scientific community. This theory describes the light as both wave and particle which can either undergoes interference or diffraction, or transfers energy with other objects. The wave character of light has been demonstrated by many experiments where the most famous one is the double-slit experiment and it was first performed by Thomas Young in 1801.

When the light illuminates two parallel slits, it tends to separate into two waves and interfere with one another. As they reach the screen standing in the front, alternative light and dark stripes are formed as shown in Figure 2.1 (a).

On the other hand, the photoelectric effect observed by Hertz in 1887 demonstrates that light can interact with materials and cause the emission of electrons as shown in Figure 2.1 (b). The first explanation was given by Albert Einstein who published a paper in 1905 stating that the light can be seen as discrete quantized packets instead of continuous wave. These packets are called photons and can be expressed as

$$E = h\nu \tag{1}$$

or

$$E = \frac{h}{\lambda} \tag{2}$$

where h is the Planck constant. When the electron in the material absorbs the photon energy which is greater than the work function of the material, it is ejected. The minimum photon frequency to provide the electron with sufficient energy to effectively escape from the material is called the threshold frequency. Increasing the light intensity only increases the number of photons and can never stimulate electrons out of the material if none of those photons is of the frequency greater than the threshold frequency. Therefore, the successful emission of electrons only depends on the energy (equivalent frequency) of incident photons, and this conclusion plays a main role in the application and development of solar cells.

2.2. Basic Semiconductor Physics

Solar cells are made based on Silicon (Si) which has 4 valence electrons orbiting at the outermost shell. In the crystalline form, Si atoms coalesce and each of them is covalently bonded with 4 neighboring atoms. This interaction results in the overlap of wave functions of Si atoms, and the quantized energy levels split into a range of discrete energy levels that are called energy bands. The allowed energy levels of covalently bonded electrons form the valence band (VB) and those of the liberated electrons form the conduction band (CB). They are separated by a range of forbidden energy levels that are known as the band gap. In the case of 0 K, the covalent bonds are quite stable; thus, no free electrons are present in the lattice and the valence band is fully occupied

by the electrons. As the temperature increases, the thermal energy breaks the bonds and stimulates electrons from the valence band to the conduction band with an equal number of holes left in the valence band. Both situations are schematically shown in Figure 2.2 (a) and (b).

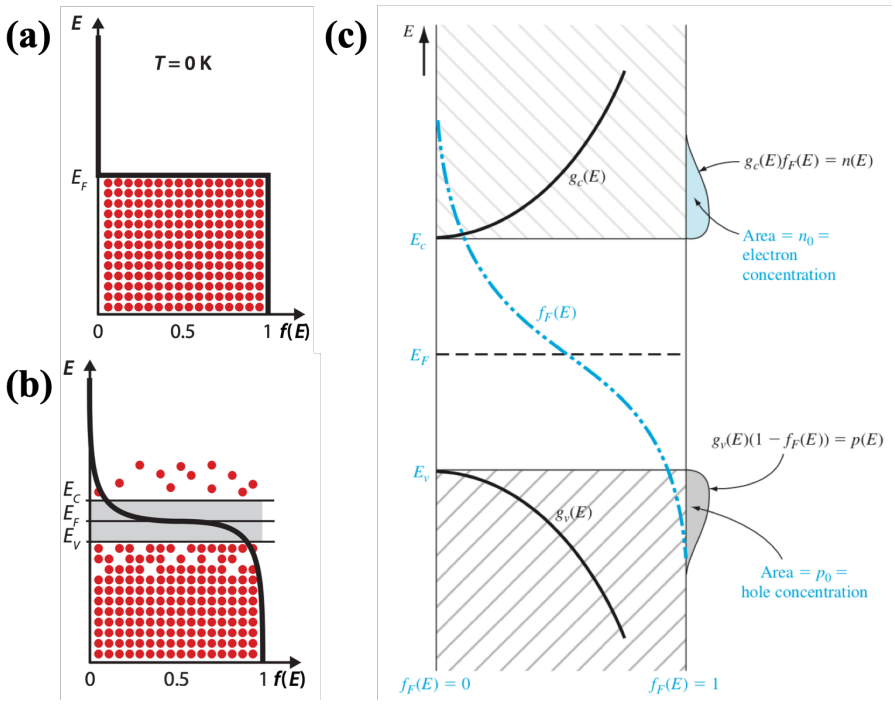

Figure 2.2 a) At T=0K, all electrons are in the valence band. b) At T>0, some electrons are excited to the conduction band by thermal energy. [5] c) Electron and hole concentrations [13].

The operation of solar cells depends on the concentration of charge carriers and it can be analytically determined by the density of energy states function and distribution function (here we are using Fermi-Dirac distribution function as an approximation). The density of energy states function describes the number of quantum states that electrons can occupy. For both conduction band and valence band, we can write their density of energy states as

$$g_C(E) = 4\pi \left(\frac{2m_n^*}{h^2}\right)^{\frac{3}{2}} \sqrt{E - E_C} \tag{3}$$

$$g_V(E) = 4\pi \left(\frac{2m_p^*}{h^2}\right)^{\frac{3}{2}} \sqrt{E - E_V} \tag{4}$$

where m_n^* and m_p^* are the effective masses of electrons and holes; E_C and E_V are the conduction band minimum and valence band maximum respectively. The Fermi-

Dirac distribution function can be expressed as

$$f(E) = \frac{1}{1 + \exp\left(\frac{E - E_F}{k_B T}\right)} \tag{5}$$

where k_B is the Boltzmann's constant and E_F is the Fermi-energy which represents the average energy of electrons in the material. By multiplying the density of energy state functions and the distribution function, we obtained the concentration of electrons in the conduction band and that of holes in the valence band:

$$n(E) = g_C(E) f(E) \tag{6}$$

$$p(E) = g_V(E)[1 - f(E)] \tag{7}$$

The outcome is schematically shown in Figure 2.2 (c). Generally, the concentration of both electrons and holes at 300 K in an intrinsic semiconductor is $1.5 \times 10^{10} cm^{-3}$.

Meanwhile, this concentration can be manipulated by doping where Si atoms are partially replaced with impurity atoms of 3 or 5 valence electrons such as Baron (B) or Phosphorus (P) to create a hole-rich p-type c-Si or an electron-rich n-type c-Si. Besides, doping can introduce additional allowed energy states within the band gap which is denoted by E_D (for n-type) and E_A (for p-type) in Figure 2.3 (b) and (c). The Fermi level is also changed after doping, for example, in n-type c-Si the Fermi level is closer to the conduction band whereas in p-type c-Si the Fermi level is closer to the valence band.

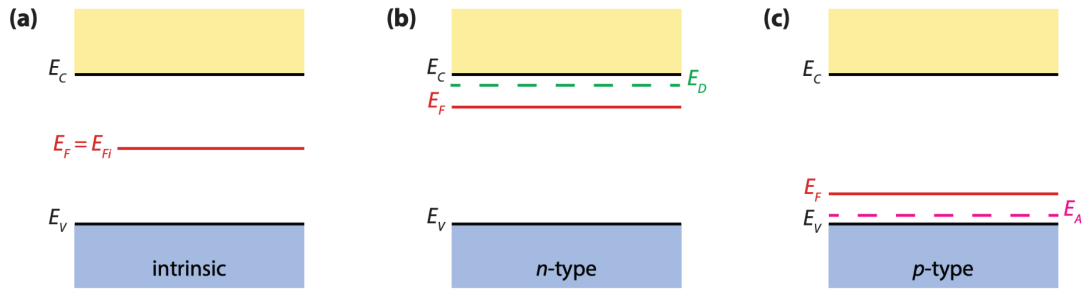

Figure 2.3 Fermi level of a) Intrinsic material. b) n-type material. c) p-type material.

The transport of carriers in semiconductor is mainly dominated by drift or diffusion mechanisms. Drift is the motion of charged particles in response to the electric field whereas diffusion is the movement of particles driven by thermal motion from high density region to low density region. For both electrons and holes, the drift and diffusion current densities can be expressed as

$$J_{n,drift} = qn\mu_n\xi \quad (8)$$

$$J_{p,drift} = qp\mu_p\xi \quad (9)$$

$$J_{n,diff} = qD_n\nabla_n \quad (10)$$

$$J_{p,diff} = -qD_p\nabla_p \quad (11)$$

where μ_n and μ_p stand for the mobility, ξ is the electric field, D_n and D_p are diffusion coefficients. Combining Eqs. (8) to (11) leads to the total current:

$$J_{total} = q(n\mu_n + p\mu_p)\xi + q(D_n\nabla_n - D_p\nabla_p) \quad (12)$$

2.3. Operation of Solar Cells

The working principle of solar cells can be summarized as generation, separation and collection of electrons and holes. As we have already mentioned before, with incident photons whose energy are greater than the band gap of the semiconductor material, electrons are excided from the valence band to the conduction band and leave an equal number of holes in the valence band. These stimulated electrons will first drop to the conduction band minimum by dissipating their excess energy in the form of thermal radiation, then they will stay at this energy level for some time before recombining with holes. This process is called electron-hole pairs generation and for c-Si solar cells it always happens in the bulk material called absorber.

After that, the generated electron-hole pairs need to be separated rapidly before they recombine and dissipate. The most common method to realize the separation is by forming p-n junctions. When n- and p-type materials are brought together, the large difference in electron and hole concentration results in the bidirectional diffusion and leaves positively charged donor atoms and negatively charged acceptor atoms behind, which consequently forms an internal electric field. This internal electric field causes a drift current, and the space charge region reaches an equilibrium when diffusion current is fully compensated by drift current. The band diagram of a p-n junction under thermal equilibrium is schematically shown in Figure 2.4. The Fermi level is constant throughout the junction and the band bending allows the minority carriers to pass while repels the majority carriers. Another common approach is by forming surface field (also known as high-low junction) where a highly doped region is introduced. The interface between the high and low doped regions creates a barrier to the minority carriers but enables the majority carriers to pass through.

Finally, the separated charge carriers need to be collected to contribute to the output current of solar cells. For c-Si, low-resistivity metals such as Aluminum (Al), Silver (Ag) and Copper (Cu) are commonly used to facilitate the collection of charge carriers and further transport them to the external circuit to power the devices.

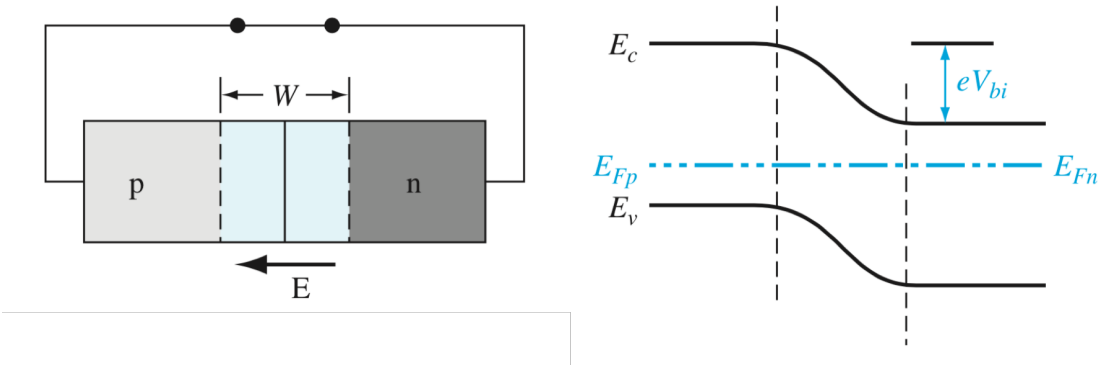

Figure 2.4 Structure and band diagram of a p-n junction [13]

2.4. Recombination in Solar Cells

The performance of solar cells can be highly influenced by the unexpected recombination of electrons and holes. Generally, the recombination occurs both in the bulk and at the surface. In the bulk absorber, there are 3 main recombination mechanisms, namely direct recombination, Shockley-Read-Hall recombination and Auger recombination.

The direct recombination allows the excited electrons to directly recombine with holes without any momentum change, and it always occurs in direct bandgap materials such as gallium arsenide. Coming with which is the emission of photons; thus, it is of great importance for light emitting devices.

The Shockley-Read-Hall (SRH) recombination does not occur directly between bandgaps. It requires the participation of impurity atoms or lattice defects that act as the recombination centers. The trapped electron can recombine with the hole that is attracted by this trapped electron, and the energy is dissipated to the vibrating lattice in the form of heat.

The Auger recombination is a three-particle process where the energy released by the recombination of a pair of electron and hole is transferred to another electron (or hole) to excite it into higher levels in the conduction band (or excite it into deeper levels

in the valence band). When this third particle shifts back to the edge of the bandgap, the energy is dissipated to the vibrating lattice in the form of heat which is schematically shown in Figure 2.5. This recombination mechanism becomes significant when the charge carrier density is high, in other words, the material is heavily doped.

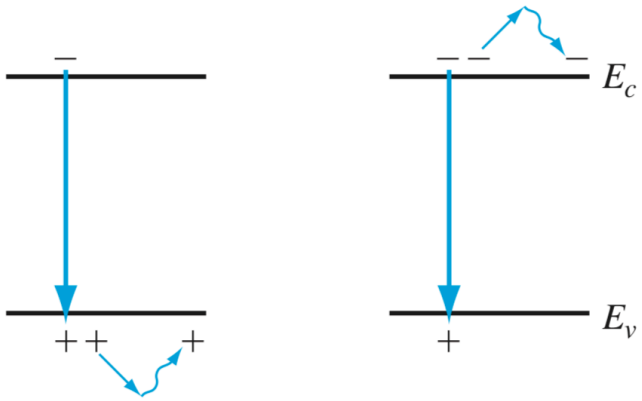

Figure 2.5 Process of Auger recombination [13]

With the developed fabrication technology of bulk c-Si, the bulk carrier lifetimes are dramatically increased. Therefore, surface recombination becomes the dominant recombination mechanism in the operation of solar cells. When the periodic nature of the c-Si ends abruptly at the surface, many valence electrons cannot find a partner to form covalent bonds which results in many defects named dangling bonds. These dangling bonds create additional discrete energy states within the bandgap and induces SRH recombination. The surface recombination can be approximated with:

$$R_s \approx v_{th}\sigma_p N_{sT}(p_s - p_0) \tag{13}$$

where v_{th} is the thermal velocity [cm/s], N_{sT} is the surface trap density [cm^{-2}], σ_p is the capture cross-section for holes [cm^2], p_s is the hole concentration at the surface and p_0 is hole concentration in the n-type semiconductor in equilibrium. The surface recombination velocity can be expressed as:

$$S_r = v_{th}\sigma_p N_{sT} \tag{14}$$

Apparently, the surface recombination is mainly determined by the surface recombination velocity and the minority carrier concentration at the surface. Therefore, surface recombination can be reduced in the following two ways: 1) Reduce the surface recombination velocity by reducing the surface trap density. This is generally realized by depositing a thin layer of suitable material which forms covalent bonds with the surface electrons; 2) Reduce the minority carrier concentration at the surface by heavy

doping at the region underneath the surface. This highly-doped region creates a barrier that minority carriers can barely pass, hence the surface recombination is reduced.

2.5. Surface Passivation of c-Si Solar Cells

The surface passivation includes the passivation at the cell surface and at the contacts. The overall passivation quality is characterized by the saturation current density J_0 [fA/cm^2] which includes both recombination in the bulk and at the surface. Based on the wonderful work done by Jan Schmidt *et.al.* [6], a brief review of various surface passivation technologies is given in this section.

2.5.1. Cell Surface Passivation

The state-of-the-art surface passivation for non-contacted area is mainly realized by dielectric layers such as SiO_2, SiN_x and Al_2O_3. The surface of diffused n^+ emitters can be effectively passivated with SiO_2 grown under high temperature, but it is subject to a couple of drawbacks such as too high production cost and potential damage to the c-Si bulk material. An alternative is by using SiN_x which is deposited at low-temperature with plasma-enhanced chemical vapor deposition (PECVD). This dielectric layer can perform not only as a good passivation layer, but also as an excellent antireflection coating due to its tunable refractive index. It is reported that the stack of SiO_2/SiN_x can provide an outstanding passivation with J_0 of 12-25 fA/cm^2. This is attributed to the rich atomic hydrogen content in the PECVD-SiN_x layer which diffuses to the SiO_2/c-Si interface and passivates the silicon dangling bonds.

However, neither SiO_2 nor SiO_2/SiN_x stack is suitable for the surface passivation of boron diffused p^+ emitters. This is due to the fact that single SiO_2 passivation layer tends to form a moisture barrier when it is stored at atmosphere, and the high positive fixed charge density in SiN_x and the SiO_2/SiN_x stack increases the minority carrier concentration at the surface; both degrade the passivation quality. An alternative is by using Al_2O_3 deposited by atomic layer deposition (ALD). The high negative fixed charge density reduces the J_0 to only 10 fA/cm^2. Further improvement on thermal stability can be achieved by combing Al_2O_3 with SiN_x but at the price of a relatively higher J_0 of around 40 fA/cm^2.

2.5.2. Passivation of Contacts

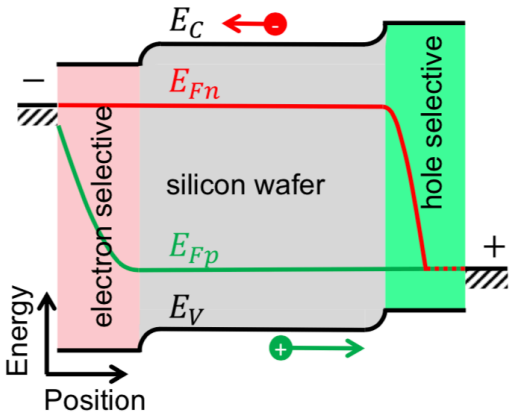

Figure 2.6 Band diagram of c-Si wafer where contacts are passivated by n^+ and p^+ selective regions [6]

Metal/Semiconductor contacts are generally subject to high recombination velocity. Traditional way to passivate the contact interface is by heavy doping at the region underneath the metal. Figure 2.6 shows the band diagram of a c-Si wafer where contacts are passivated by n^+ and p^+ selective regions. Apparently, an asymmetric conductivity for both holes and electrons is formed at each selective region, where n^+ region allows electrons to pass but shows high resistivity to holes. By contrast, p^+ region facilitates the collection of holes while blocks the electrons, hence a low recombination velocity is achieved at both regions.

2.5.3. Definition of Selectivity

Carrier selective contacts should provide an asymmetric conductivity to the carriers, i.e. allowing one type of carrier to easily pass but block the other. Therefore, the selectivity S is proportional to the resistance seen by the majority carriers and minority carriers. Assume that the total recombination rate at the carrier selective contact is R(V) where $V = (E_{Fn} - E_{Fp})/q$ is caused by the splitting of quasi-Fermi levels, then the resistance for minority carriers is

$$\rho_m = \frac{V}{qR(V)} \tag{15}$$

and the resistance for majority carriers is

$$\rho_M = \rho_C \tag{16}$$

Taking the ratio of two resistances, we get

$$\frac{\rho_m}{\rho_M} = \frac{V}{qR(V)\rho_C} \tag{17}$$

By transforming Equation 17 to

$$\frac{V}{qR(V)\rho_C} = \frac{V_{th}}{\rho_C\left[\frac{qR(V)}{\exp\left(\frac{V}{V_{th}}\right)-1}\right]} \quad \frac{V}{V_{th}\left[\exp\left(\frac{V}{V_{th}}\right)-1\right]} = S(V)g(V) \tag{18}$$

where V_{th} it the thermal voltage, and g(V) is a voltage-dependent factor, the selectivity is defined as

$$S(V) = \frac{V_{th}}{\rho_C\left[\frac{qR(V)}{\exp\left(\frac{V}{V_{th}}\right)-1}\right]} \tag{19}$$

Under low injection, the total recombination rate can be written as

$$R(V) = \frac{J_0\left[\exp\left(\frac{V}{V_{th}}-1\right)\right]}{q} \tag{20}$$

By combing Eqs. (19) and (20), the selectivity becomes voltage-independent:

$$S = \frac{V_{th}}{\rho_C J_0} \tag{21}$$

In case of a p^+ carrier selective region, the selectivity is calculated to be

$$S = \frac{p_0\mu_p}{n_0\mu_n} \propto \frac{p_0}{n_0} \tag{22}$$

where p_0 and n_0 are the equilibrium carrier concentration, μ_p and μ_n are the hole and electron mobility respectively. Obviously, a higher selectivity can be achieved by increasing the majority carrier concentration at the region underneath the contact, i.e. increasing p_0 while decreasing n_0 for the case illustrated above. The overall selectivity can be expressed as

$$S_{overall} = \frac{1}{\left(\frac{1}{\sqrt{S_e}} + \frac{1}{\sqrt{S_h}}\right)^2} \tag{23}$$

where S_e and S_h stand for the selectivity at both electron and hole selective regions.

2.5.4. Carrier Selective Passivation Contacts

Qualified carrier selective contacts should provide excellent passivation for both contacted and non-contacted areas, and also enable effective extraction of one polarity of carrier but block the other. Typical material such as hydrogenated amorphous silicon (a-Si:H) has been widely reported to be an excellent candidate for carrier selective passivation contact. It is based on a stack of intrinsic a-Si:H with n^+ or p^+ a-Si:H where the doped layer is relatively thicker. A record efficiency of 26.7% for c-Si solar cells has been achieved by using this type of carrier selective passivation contact.

Polycrystalline Silicon (poly-Si) also has a large potential to be integrated in the solar cells as a remarkable carrier selective passivation contact. The idea is based on an ultrathin interfacial SiO_2 layer (grown either thermally or wet chemically) plus a thicker n^+ or p^+ poly-Si on top. An extremely low J_0 (1 fA/cm^2) has already been reported with this passivation structure [14].

However, both a-Si:H and poly-Si carrier selective passivation contacts are subject to a couple of intrinsic drawbacks. First, these Si layers can more or less induce the parasitic absorption which limits the carrier generation ability in the bulk absorber; second, the heavy doping can lead to significant Auger recombination which is unexpected for high-efficiency solar cells; third, the high-temperature post treatment also raises the fabrication cost.

A promising alternative is by using TMOs whose work functions and band gaps are schematically shown in Figure 1.2. Compared to traditional Si CSCs, the larger bandgap of TMOs reduces the optical losses; the doping-free nature eradicates the potential Auger recombination; and relatively easy processing enables it to cut down the capital cost. In general, materials with high work function such as molybdenum oxide (MoO_x) and tungstate oxide (WO_x) are suitable as hole-selective contacts, whereas those with low work function such as titanium oxide (TiO_x) and magnesium oxide (MgO_x) have potential to work as the electron-selective contacts. When MoO_x and c-Si are brought together, the Fermi level becomes horizontal throughout the junction under thermal equilibrium, and the band bending occurs which is shown in Figure 2.7 (b). The large offset at the conduction band repels the electrons while the holes are still capable of tunneling through. On the other hand, the band diagram of

TiO_x/(n)c-Si junction shows another way around where a small conduction band offset and a large valence band offset facilitate the transport of electrons while block the holes.

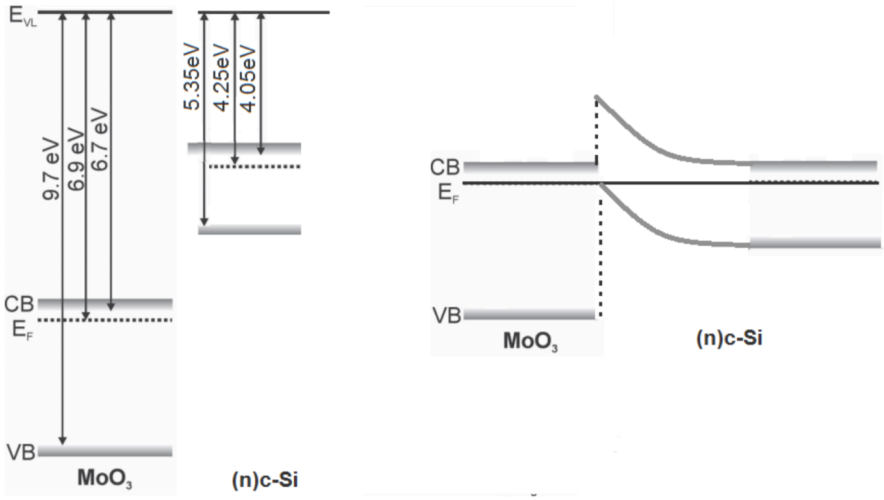

Figure 2.7 a) Band diagram of both MoO_3 and (n) c-Si when they are separated b) Band diagram of MoO_3/(n) c-Si junction where band bending occurs

The interface between TMOs and c-Si is generally passivated by either intrinsic a-Si:H [15] or SiO_2 [16] because the chemical passivation quality of TMOs is not satisfactory. Besides, due to the fact that TMOs are insulators, the thickness of both TMO layer and additional interfacial passivation layer must be ultrathin (i.e. a few nm) so that the transport of majority carriers is not hindered. In this project, both MoO_x based hole selective contact and TiO_x based electron selective contact are investigated.

3. Processing Techniques

In this chapter, various processing techniques that were used for solar cell fabrication are briefly introduced. The cleaning of c-Si wafers and growth of SiO_2 passivation layer are carried out by using Nitride Acid Oxidation of Si (NAOS) method; poly-Si and amorphous Si are deposited by means of Low Pressure Chemical Vapor Deposition (LPCVD) and Plasma Enhanced Chemical Vapor Deposition (PECVD) respectively; doping is done by either Ion Implantation or Thermal Diffusion and the activation of dopants is realized by high temperature annealing; the passivation of dangling bonds at the interfaces are further improved by Forming Gas annealing; MoO_x and TiO_x are deposited by thermal evaporation and E-beam evaporation respectively; Al_2O_3 is deposited by Atomic Layer Deposition.

3.1. Standard Cleaning

The standard cleaning of wafers aims to remove any organic or inorganic residues from the c-Si surface. The basic idea it to oxide the silicon surface to form a thin layer of silicon dioxide, then etch it away along with the residues. In this project, the standard cleaning is carried out by means of Nitride Acid Oxidation Cycles (NAOC).

The wafers are first immersed in a 99% HNO_3 solution and stay there for 10 minutes to remove the organic residues, then the wafers are rinsed in deionized water (DI Water) for 5 minutes. After which, the wafers are transferred to a 68% HNO_3 solution whose temperature is constantly kept at 110 ^oC. The wafers stay in the solution for another 10 minutes to remove the inorganic residues, and again are rinsed in DI water for 5 minutes. To expose the c-Si surface for further processing, the oxidized thin layer can be removed by dipping the wafer in 0.55% Hydrofluoric acid (HF) for 4 minute, followed by 5 minute of DI water rinsing. Due to the fact that unexpected native oxide can be formed when the wafers are kept in air, it is very important to do HF etching right before the next step of process.

3.2. Nitric Acid Oxidation of Si (NAOS)

The ultrathin SiO_2 passivation layer is grown wet-chemically in which the cleaned wafers are soaked in the 69.5% HNO_3 solution at room temperature for 60 minutes [17]. The growth rate of SiO_2 is saturated after 60 minutes and the obtained thickness can be precisely kept at around 1.5 nm [18]. The advantage of this method is that the layer is more conformal and requires much less energy consumption compared to the thermal growth method, but it is subject to some drawbacks such as lower thermal stability.

3.3. Low-pressure Chemical Vapor Deposition

Low Pressure Chemical Vapor Deposition (LPCVD) is a commonly used method for deposition of thin films on semiconductors ranging from a few nanometers to micrometers [19]. Similar to other CVD processes, in LPCVD a gaseous species reacts on a solid surface or wafer and a solid phase material is formed. Generally, the deposition in LPCVD includes four steps [20]: 1) The gaseous reactants must be transported to the wafer surface; 2) The gaseous species must adsorb onto the surface of the wafer; 3) The heterogeneous surface reaction produces products; 4) The gaseous reactants must be removed from the surface.

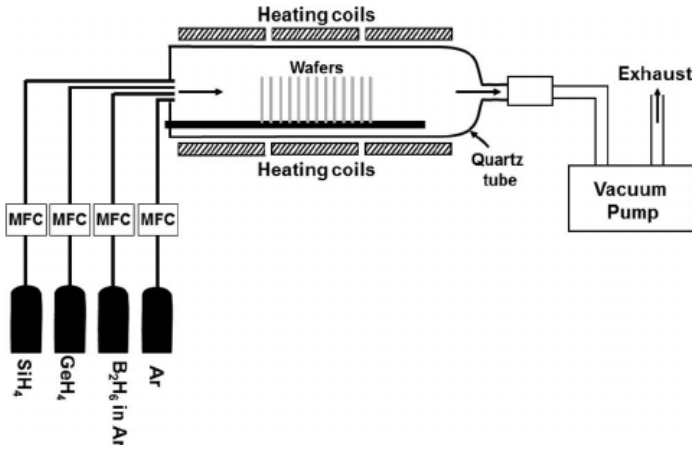

Figure 3.1 Schematic diagram of LPCVD system [21]

Figure 3.1 schematically shows an overview of LPCVD system. The deposition occurs in a quartz tube which is placed within a spiral heating coils, and connected to a

vacuum pump. When the desired vacuum level and temperature are both reached, the gaseous species is inserted from the inlet into the tube and diffuses to the hot substrates. The reaction then takes place and the solid phase material is formed on the substrate. The excess material and by-products are pumped out from the tube.

Compared to Atmospheric Pressure Chemical Vapor Deposition (APCVD), the advantage of LPCVD is that the ratio between the mass transport velocity and the velocity of reaction on the surface is much lower. It has been demonstrated that the diffusion of gaseous species decreases proportionally with pressure. During LPCVD process, the low pressure results in a low mass transport velocity, meaning that reactants are more likely to uniformly distributed at the surface which leads to a more homogeneous and conformal thin film on the substrate [22]. In this project, LPCVD is mainly used for poly-silicon thin film deposition where SiH_4 is used as the precursor gas and the deposition occurs at a temperature of 580 ^oC.

3.4. Plasma Enhanced Chemical Vapor Deposition

Plasma Enhanced Chemical Vapor Deposition (PECVD) is another widely adopted thin film deposition method where plasma is created in the deposition chamber to provide energy to the reaction [23]. Plasma is seen as the fourth state of matter, and it is a hot ionized gas where high free electron content is present [24].

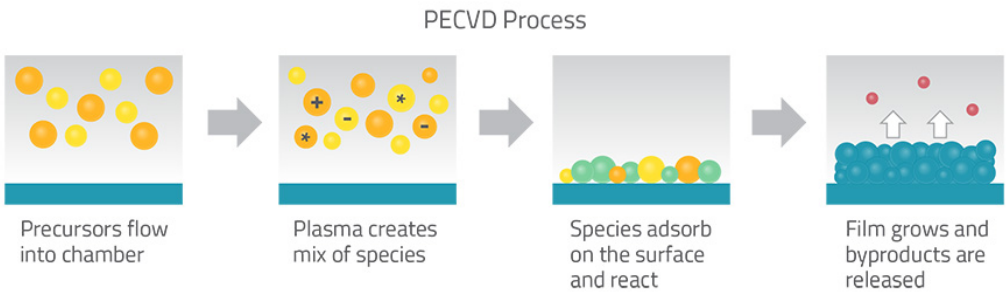

Figure 3.2 Plasma Enhanced Chemical Vapor Deposition Process [25]

Figure 3.2 schematically shows the PECVD process. During deposition, precursor gases are introduced and mixed between two parallel electrodes. The RF electric field excites the reactant gases into a plasma where high energy electrons dissociate precursor gases into free radicals. These radicals subsequently adsorb on the substrate

surface and the chemical reaction results in the formation of solid film [26]. Compared to LPCVD, PECVD enables the deposition at low temperature because the major energy source for the reaction comes from plasma. In this project, PECVD is mainly used for the deposition of amorphous silicon.

3.5. Doping - Ion Implantation & Diffusion

Ion implantation is a process whereby a beam of ions are focused and bombard the target sample to achieve doping [27]. This idea was first introduced in 1950s, and adopted in semiconductor manufacturing in mid-1970s. Figure 3.3 gives a schematic overview of ion implanter system.

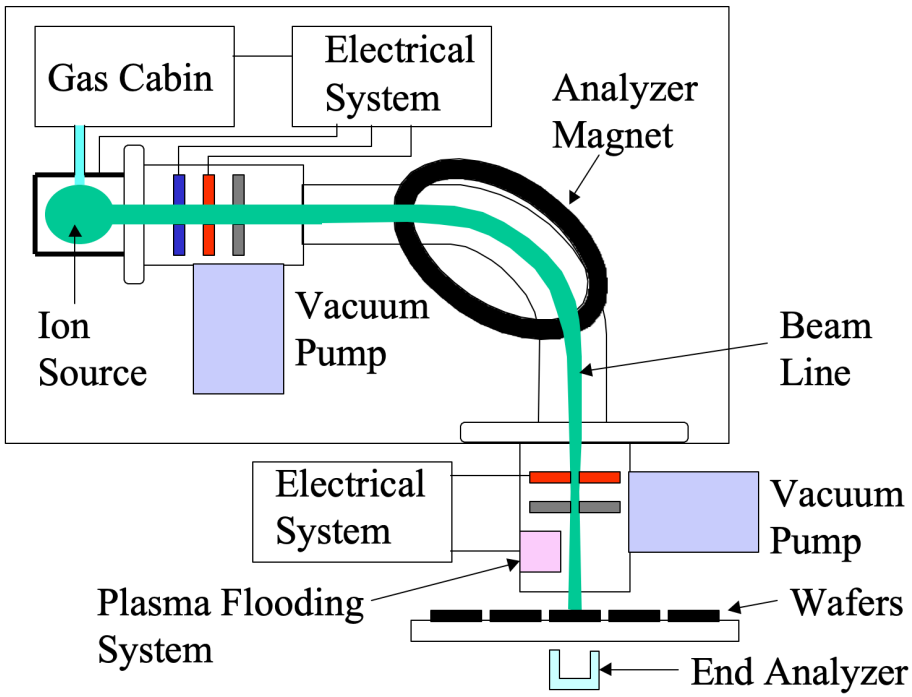

Figure 3.3 Schematic overview of an Ion Implanter system [28]

Generally, an ion implanter consists of 4 parts, i.e. gas system, vacuum system, electrical system and control system [28]. The gas system is responsible for delivering hazardous gaseous reactants where Argon is used for purge and beam calibration; the vacuum system includes Turbo pump and Cryo pump. A high vacuum level is necessary during implantation so that ions can be properly accelerated and unexpected collision with particles can be reduced; the electrical system generates required electric field and

magnetic field to accelerate and separate ions; the control system controls the implantation parameters such as ion energy, beam current and ion species.

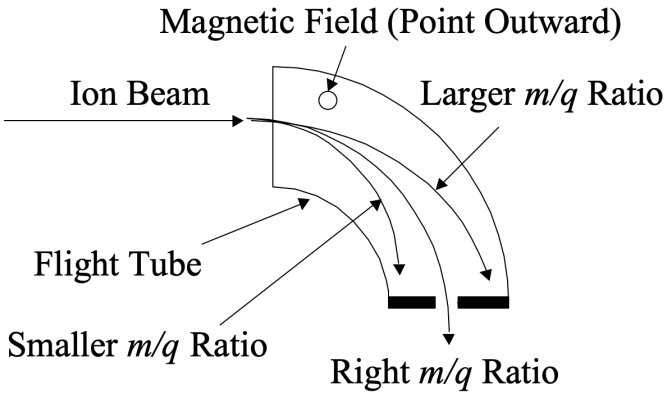

Figure 3.4 Analyzer magnet which only allows the ions of the right mass to charge ratio to pass [28]

During process, the thermal electrons are emitted from a hot tungsten filament and collide with dopant gas molecules to generate dopant ions. These ions are extracted and accelerated by the extraction electrode to a beamline. To obtain a high-purity ion beam of dopant species, an analyzer magnet is used. Due to the fact that the gyro radius of charged particles in magnetic field is related to B-field and the mass to charge ratio [29]:

$$r_g = \frac{m \cdot v_p}{|q| \cdot B} \tag{24}$$

where m is the mass of the particle, v_p is the velocity perpendicular to the magnetic field, q is the particle charge and B is the magnetic field, thus, by adjusting the magnetic field, the ions with desired mass to charge ratio can pass the slit as shown in Figure 3.4. After being selected by the analyzer magnet, the purified ion beam is accelerated or decelerated again to reach the desired ion energy. During implantation, ions cause a charged wafer, leading to non-uniform doping and arcing defects. An additional plasma flooding system is required to keep charge neutralization of wafers [30].

Diffusion is another commonly used doping technique where a n- or p-doped layer is deposited on the substrate, followed by a high temperature post-treatment in furnace to activate and drive in the dopant atoms [31]. In this project, ion implantation is the first priority for doping due to its anisotropic dopant profile, and independent control of the dopant concentration and junction depth.

3.6. Annealing and Oxidation

For both doping with diffusion and ion implantation, a subsequent high temperature annealing is required to activate the dopants. During ion implantation, the energetic ions bombard the substrate surface and knock the atoms out from the lattice grid, leading to the amorphous structure as shown in Figure 3.5.

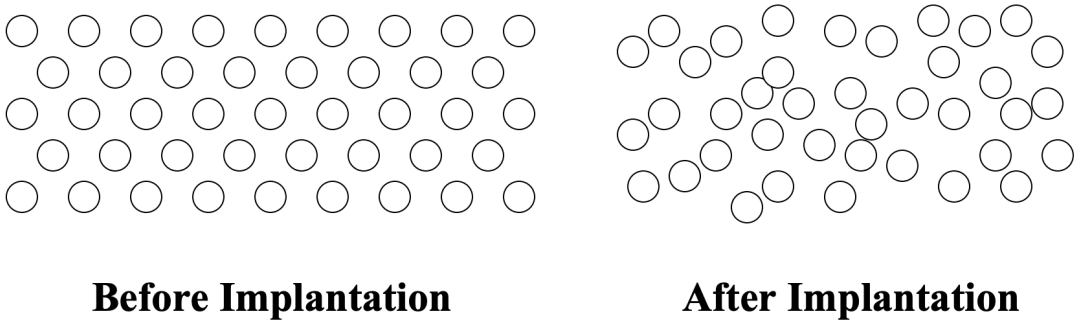

Figure 3.5 c-Si structure change after ion implantation where amorphous state is present [28]

These implanted atoms distribute randomly in the material and the majority of them are not bonded with silicon atoms. In order to activate the dopants, high temperature annealing is adopted which transforms the amorphous atoms back to single crystal structure. Dopants are covalently bonded with 4 silicon atoms and can properly act as donors or acceptors. A schematic illustration is shown in Figure 3.6.

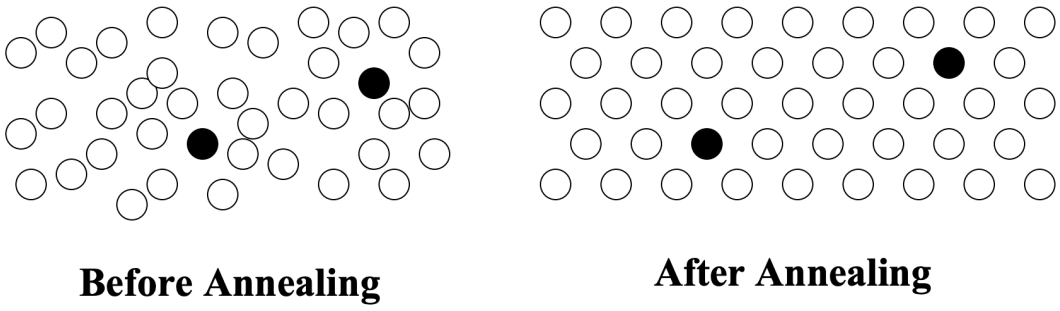

Figure 3.6 c-Si structure changes after annealing where dopants are activated and crystal structure recovers [28]

3.7. Hydrogenation

One of the challenges of thin film deposition during the fabrication of solar cells is to maintain a good surface passivation quality. It has been studied that the passivation degradation at the surface after high-temperature annealing is mainly caused by the loss of hydrogen from the Si/Oxide interface, which generates additional dangling bonds as recombination centers [32]. Therefore, a subsequent forming gas (5% H_2 in N_2) annealing is introduced where the hydrogen atoms penetrate the thin films and reach the interface to re-passivate the defects [33].

3.8. Physical Vapor Deposition (PVD)

Physical Vapor Deposition (PVD) is a thin film deposition process where the target material is vaporized from solid or liquid phase and transported in a high vacuum environment to reach the substrate and condense into films [34]. The main PVD processing methods are vacuum evaporation, sputtering, arc vapor deposition and ion plating [35]. In this project, sputtering and vacuum evaporation methods are used where the latter can be further categorized into thermal evaporation and E-beam evaporation.

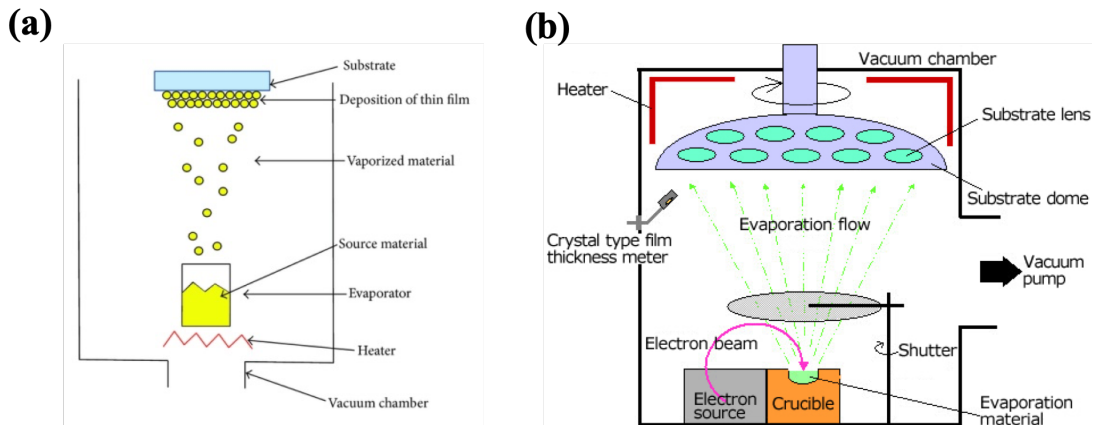

Figure 3.7 Physical Vapor Deposition a) Thermal Evaporation [36] b) E-beam Evaporation [37]

In thermal evaporation, target materials are melted directly by heating up the containers such as tungsten wire coils in a low pressure atmosphere. The high vacuum level ensures the long free mean path for the evaporated material so that these material

atoms can transport to the substrate without colliding with gas molecules. This technique is commonly used for the materials with a melting temperature lower than 1500 °C [35]. Figure 3.7 (a) schematically shows the thermal evaporation process.

In E-beam evaporation technique, a focused high energy electron beam is redirected to the target material which causes the local melting of the material. The evaporated material transports to the substrate surface and cause the deposition. This technique is suitable for the material whose melting temperature is higher than 1500 °C. A schematic overview of the system is shown in Figure 3.7 (b).

During deposition, the sample stage is rotating continuously to ensure a relatively uniform thin film growth, and the thickness of the deposition is monitored by a crystal. In this project, MoO_x thin film is deposited by thermal evaporation, and TiO_x thin film is deposited by E-beam evaporation. The metallization is realized by first thermally evaporating 300 nm Aluminum, followed by E-beam evaporation to complete the layer.

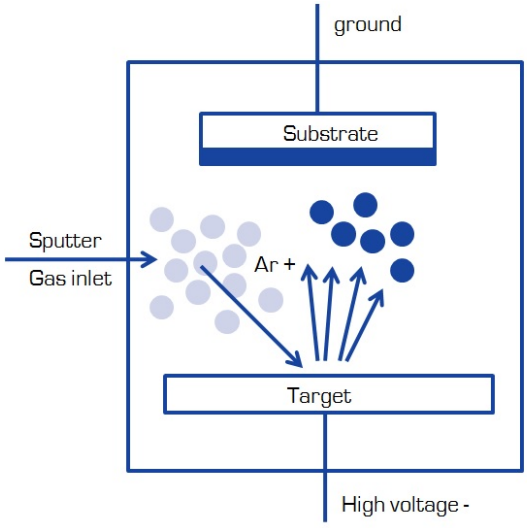

Figure 3.8 PVD sputtering process where Ar ions cause the ejection of target material atoms [38]

Sputtering is another PVD thin film deposition technique whereby atoms are ejected from target material due to the momentum transfer from bombarding atomic-sized particles [35]. Figure 3.8 shows the working principle of PVD sputtering. During deposition, inert gas such as Argon is introduced to the vacuum chamber. When a sufficiently large DC voltage is applied, the discharge is generated and the sputter gas is partially ionized where the ions are accelerated and directed to the target material. The high-energy ions bombard the target surface and transfer the momentum to eject

target atoms which subsequently reach the substrate and coat the surface. In this project, PVD sputtering technique is used for ITO deposition.

3.9. Atomic Layer Deposition (ALD)

Atomic Layer Deposition (ALD) is a self-limiting film growth method which splits the chemical reaction by alternatively exposing the growing film to the chemical precursors, enabling the growth of monolayers [39]. Generally, ALD process involves four steps which are schematically shown in Figure 3.9.

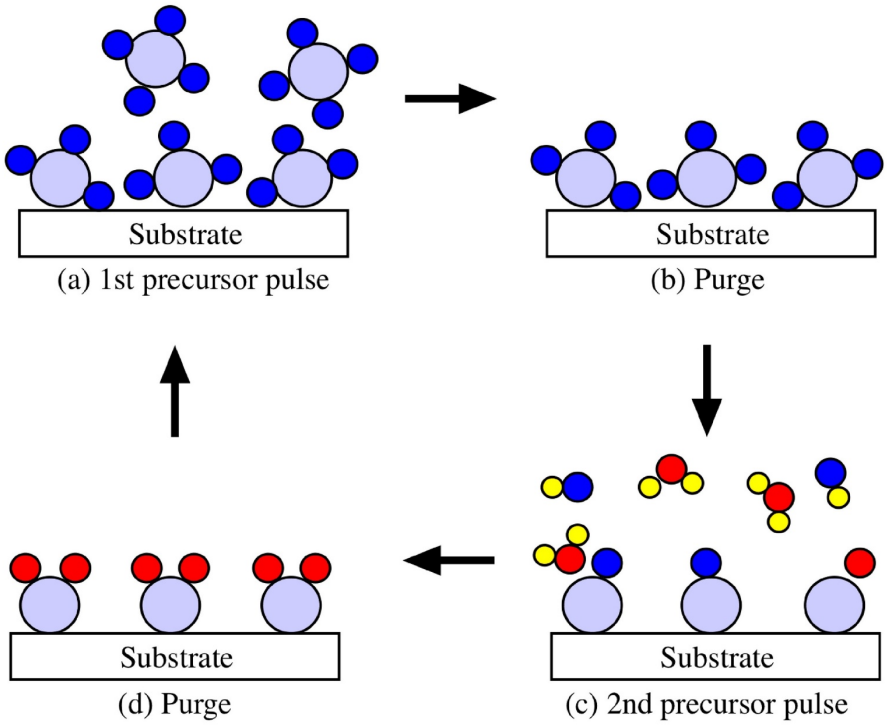

Figure 3.9 Typical Atomic Layer Deposition process

1) The first precursor is introduced to the vacuum chamber and chemisorbed onto the substrate surface until saturation.
2) Chamber is purged with N_2 to remove the unreacted precursor.
3) The second precursor is introduced to the vacuum chamber and reacts with the surface groups of precursor-1, leading to desired film and by-products.
4) Chamber is purged with N_2 to remove the unreacted precursor and by-products.

These four steps complete one cycle. Based on the surface self-limiting mechanism,

the amount of adsorbed molecules in each reaction step is constant, meaning that the final deposition thickness only relies on the number of running cycles. Therefore, the thickness of as-deposited thin films can be precisely and simply controlled by adjusting the deposition cycles. Meanwhile, the alternative dosing of precursors prevents the gas-phase reaction which ensures a uniform and conformal growth of thin film [40].

4. Characterization Methods

This chapter gives a brief introduction of different characterization methods that were used to analyze the performance of the solar cells. The surface passivation quality of cell precursors is measured by Quasi-Steady-State Photoconductance; the thickness of thin layers is determined by means of Ellipsometry; the external parameters of fabricated solar cells are characterized by illuminated I-V measurement system; the open circuit voltage of solar cells is measured by SunsVoc measurement; the chemical composition and the oxidation state are determined by using X-ray Photoelectron Spectroscopy; the contact resistance of is measured by Transfer Length Measurement.

4.1. Quasi-steady-state Photoconductance (QSSPC)

The effective minority carrier lifetime is an important parameter to characterize the passivation property of a solar cell. In this project, the measurement is carried out by using contact-less Quasi-steady-state Photoconductance (QSSPC) where the sample is illuminated with a light flash that either slowly or rapidly decays [41]. The measurement system is schematically shown in Figure 4.1.

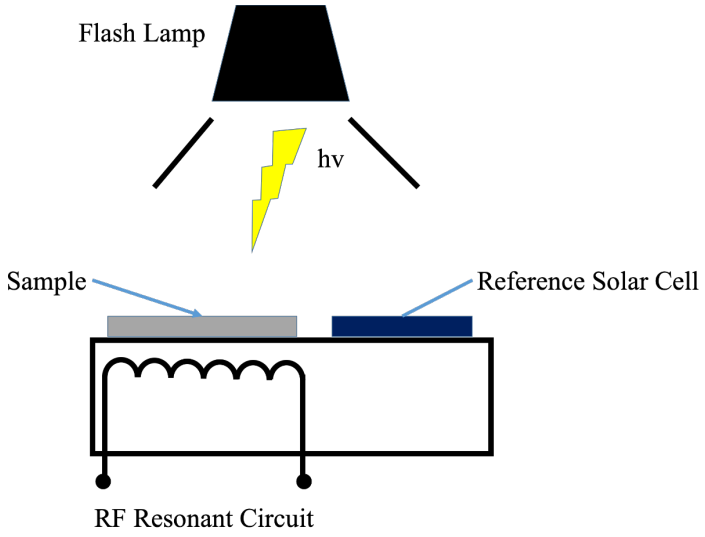

Figure 4.1 Quasi-steady-state Photoconductance (QSSPC) measurement system

The to-be-measured sample is placed on a stage whose temperature is kept

constantly at 300 K. As the light flashes, excess electron-hole pairs are generated in the sample due to the absorption of photon energy. This carrier concentration difference compared to the case of thermal equilibrium results in the change in sample conductivity which is inductively detected by the RF resonant circuit integrated in the stage. The absolute illuminance intensity is measured by the reference solar cell. As is already discussed in Chapter 2, the bulk and surface recombination are the two dominant recombination mechanisms during the operation of a solar cell. Generally, the recombination is characterized by effective minority carrier lifetime:

$$\frac{1}{\tau_{eff}} = \frac{1}{\tau_{bulk}} + \frac{1}{\tau_{surface}} \tag{25}$$

where

$$\frac{1}{\tau_{bulk}} = \frac{1}{\tau_{SRH}} + \frac{1}{\tau_{Auger}} + \frac{1}{\tau_{Radiative}} \tag{26}$$

The basic continuity equation gives a relation between the effective minority carrier lifetime and the excess minority carrier density. For p-type c-Si, the equation can be expressed as:

$$\frac{\partial[\Delta n(t)]}{\partial t} = G - R = G(t) - \frac{\Delta n(t)}{\tau_{eff}} \tag{27}$$

For slowing decaying light flash, the equation is transformed to:

$$\tau_{eff} = \frac{\Delta n(t)}{G(t) - \frac{\partial[\Delta n(t)]}{\partial t}} \tag{28}$$

It is know that the generation and recombination of excess carriers can cause the change in sample conductivity. Assuming $\Delta n = \Delta p$ and identical mobility for excess carriers, then the excess minority carrier density can be calculated by:

$$\Delta n = \frac{\Delta \sigma}{q(\mu_n + \mu_p)} \tag{29}$$

where μ_n and μ_p are the mobility of minority and majority carriers. The generation rate G(t) is measured by a reference solar cell according to equation:

$$G(t) = \frac{I(t) f_{abs} N_{ph}(t)}{W} \tag{30}$$

where f_{abs} is the optical absorption fraction, N_{ph} is the density of photons whose energy is greater than the band gap, W is the thickness of the reference solar cell. Therefore, by measuring the conductivity change over time, one can determine the

effective minority carrier lifetime.

Two different measurement modes are available, i.e. the quasi-steady-state mode and the transient mode. Generally, for the case that lifetime is lower than $200\,\mu s$, quasi-steady-state is applied where the light decay time constant is larger than the effective lifetime [42]. The transient mode is only suitable for the case that lifetime is larger than $200\,\mu s$. In this mode, the light flash decays rapidly, hence, the generation rate is negligible and the effective lifetime is only related to the decreasing of excess carrier density due to recombination. Equation 27 can be simplified to:

$$\tau_{eff} = \frac{\Delta n(t)}{-\frac{\partial[\Delta n(t)]}{\partial t}} \tag{31}$$

In order to have a standard parameter to compare the solar cells with different doping concentration and thickness, the effective lifetime can be converted to the implied open circuit voltage (iVoc) by:

$$iVoc = E_{Fn} - E_{fp} = \frac{k_B T}{q} \ln\left[\frac{(p_0 + \Delta n)(n_0 + \Delta n)}{{n_i}^2}\right] \tag{32}$$

where q is the elementary electron charge, k_B is the Boltzmann constant, n_i is the intrinsic carrier concentration.

4.2. Ellipsometry

The measurement of thickness and optical constants of thin layers is carried out by ellipsometry. This is a non-destructive method where the thickness is obtained by measuring the change of polarization as light reflects or transmits from a material [43]. The measurement system is schematically shown in Figure 4.2.

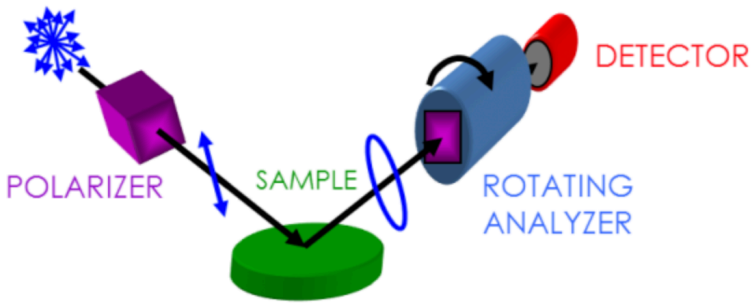

Figure 4.2 Ellipsometry measurement system where the thin film thickness and optical constants are obtained by measuring the change of light polarization [44]

As is mentioned in Chapter 2, light can be seen as an electromagnetic wave where the electric field is always orthogonal to the propagation direction. Generally, the polarization of light is determined by its phase and amplitude. For the light whose orthogonal electromagnetic waves are in phase, the light is linearly polarized and its orientation is dependent on the amplitude; if they are 90 degrees out of phase and share the same amplitude, the light is circularly polarized; if they are combined in arbitrary phase and amplitude, the light is elliptically polarized. When light interacts with material, the electric fields that are parallel and perpendicular to the incident plane can be seen as p- and s- polarized respectively, and these two components can be calculated separately by Fresnel Equations [45]:

$$r_p = \frac{E_{rp}}{E_{ip}} = \frac{n_t cos\theta_i - n_i cos\theta_t}{n_t cos\theta_i + n_i cos\theta_t} \quad (33)$$

$$t_p = \frac{E_{tp}}{E_{ip}} = \frac{2n_i cos\theta_i}{n_t cos\theta_i + n_i cos\theta_t} \quad (34)$$

$$r_s = \frac{E_{rs}}{E_{is}} = \frac{n_i cos\theta_i - n_t cos\theta_t}{n_i cos\theta_i + n_t cos\theta_t} \quad (35)$$

$$t_s = \frac{E_{ts}}{E_{is}} = \frac{2n_i cos\theta_i}{n_i cos\theta_i + n_t cos\theta_t} \quad (36)$$

When measuring the thickness, an unpolarized light produced from the light source first goes through the polarizer where a preferred electric field orientation is allowed to pass. This linearly polarized light interacts with the sample and undergoes phase and amplitude delay, resulting in a elliptically polarized light which is reflected from the sample to a continuously rotating polarizer. The amount of light that is allowed to pass through is detected and the complex reflection ratio can be calculated as:

$$\rho = \tan(\varphi) \exp(i\Delta) \quad (37)$$

where φ is the amplitude ratio which compares the reflected and incident electric field magnitudes, and Δ is the phase change. The experimental data is then fitted with the model where the lowest Mean Squared Error (MSE) represents the best answer.

4.3. Illuminated I-V Measurement

I-V curve is one of the most fundamental characteristics for solar cells, and it is the superposition of the dark I-V curve of solar cell and photo-generated current. When no

voltage is applied, the generation current and recombination current are balanced which leads to zero external net current. When a moderate forward-biased voltage is applied, the current change follows the Shockely Equation:

$$J = J_0 \exp\left(\frac{qV_a}{k_B T}\right) \tag{38}$$

where J_0 is known as the saturation current density. The generation current is nearly independent of the applied voltage and is determined by the thermally-generated minority carriers in the doped region. Therefore, the net current density becomes

$$J = J_{rec} - J_{gen} = J_0 \left[\exp\left(\frac{qV_a}{k_B T}\right) - 1\right] \tag{39}$$

Under illumination, the p-n junction can be seen as being applied with a forward bias voltage. By including the photo-generated current, the external net current density can be expressed as

$$J = J_{rec} - J_{gen} - J_{photo} = J_0 \left[\exp\left(\frac{qV_a}{k_B T}\right) - 1\right] - J_{photo} \tag{40}$$

where J_{photo} stands for the photo-generated current density. Figure 4.3 compares the I-V curves under dark and illuminated cases. It is clear that the illuminated I-V curve resembles the dark I-V curve but it shifts down by the photogenerated current density.

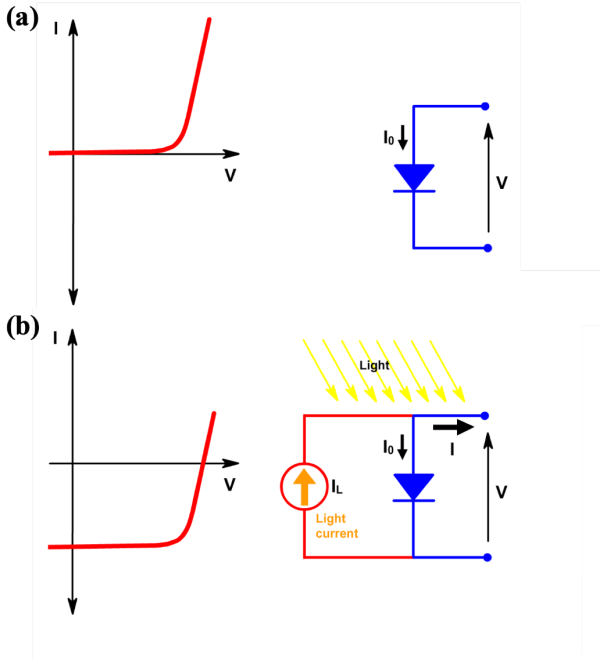

Figure 4.3 a) I-V curve under no illumination b) I-V curve under illumination [46]

In this project, the illuminated I-V measurement is carried out by Wacom WXS-156S-L2 system under standard test conditions (STC) where AM 1.5 spectrum, 1000 W/m^2 irradiation intensity and measuring temperature (25^{o}C) are used. The spectrum is simulated by using both Halogen lamp and Xenon lamp, and the temperature of the stage is maintained by a temperature controller. Typical I-V curve is shown in Figure 4.4 where the open-circuit voltage (Voc), short-circuit current (Isc), maximum power point (Pmpp) can be directly obtained therefrom.

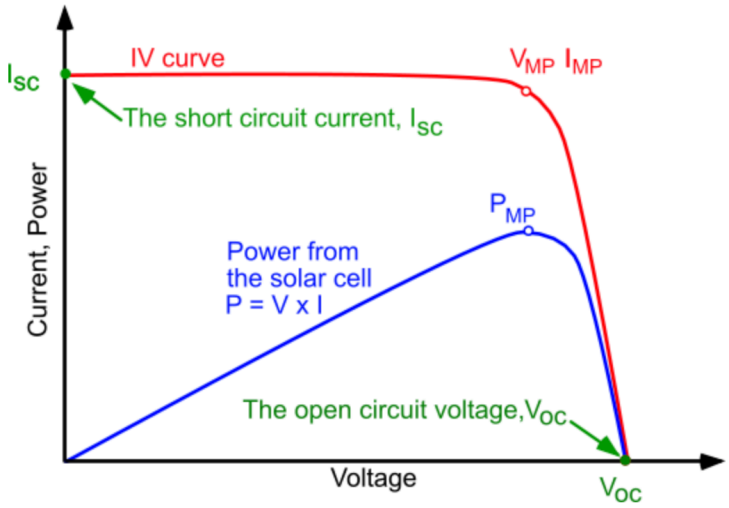

Figure 4.4 Classic I-V curve of a solar cell where V_{oc}, I_{sc} and P_{mpp} can be obtained [46]

Voc and Isc are measured when the solar cell is under open-circuit and short-circuit condition respectively. Pmpp is the maximum power that a solar cell can deliver. The Fill Factor is defined as the ratio between the maximum power and the product of Jsc and Voc as expressed as follows:

$$FF = \frac{P_{mpp}}{J_{sc}V_{oc}} = \frac{J_{mpp}V_{mpp}}{J_{sc}V_{oc}} \tag{41}$$

and the photo-conversion efficiency (PCE) can be expressed as

$$\eta = \frac{P_{mpp}}{P_{in}} = \frac{J_{sc}V_{oc}FF}{P_{in}} \tag{42}$$

where P_{in} is the total incident power, and J_{sc} is the short-circuit current density. The result gives a first approach to analyze the performance of solar cell, for instance, the open-circuit voltage is mainly influenced by recombination and a greater open-circuit voltage indicates a better passivation quality, while the fill factor is dominated by series resistance and shunt resistance.

4.4. SunsVoc Measurement

SunsVoc measurement can be used to determine the open-circuit voltage of solar cell without measuring the current [47]. The measurement setup is similar to that for QSSPC where a slowly decaying light is generated by Xenon flash lamp and shone on the sample. The sample is electrically contacted by the front probe and back stage and the voltage is directly measured as the light decays. The light intensity is measured simultaneously by a reference solar cell. The entire measurement is performed under open circuit, therefore, it is free from any series resistance effect [48]. By comparing it to the I-V curve obtained from Wacom, one can precisely determine the series resistance of a solar cell with the equation below:

$$Rs = \frac{V_{mpp,SunsVoc} - V_{mpp,I-V}}{J_{mpp,I-V}} \tag{43}$$

where $V_{mpp,SunsVoc}$ is the maximum power point voltage from SunsV_{oc} measurement, $V_{mpp,I-V}$ and $J_{mpp,I-V}$ are the maximum power point voltage and current extracted from the I-V curve respectively.

4.5. X-Ray Photoelectron Spectroscopy (XPS)

X-ray Photoelectron Spectroscopy (XPS) is based on photoelectric effect where electrons are emitted from the surface after irradiation with photons. When an electron within a material absorbs the energy from the photon and acquires the energy that is higher than its work function, this electron is ejected. The work function is also known as the binding energy which describes the minimum energy to disassemble an object into separate parts.

Figure 4.5 shows a ball model of an oxygen atom where one electron in 1s energy level is emitted by X-ray photon. Generally, electrons in the inner shells have higher binding energy and any photon with an energy lower than the work function is not able to eject the electrons. After the emission of photoelectrons, a vacancy is created which is subsequently filled by an electron from a higher energy level, leading to the release of energy. In most cases, the energy is released in the form of photons, but sometimes this energy can also be absorbed by another electron and cause additional electron

emission which is named as Auger electrons [49].

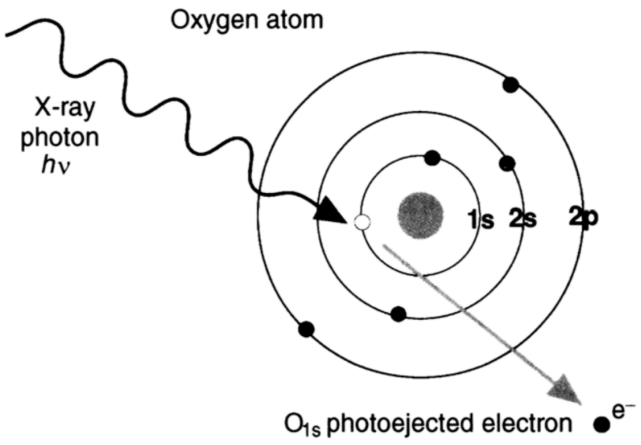

Figure 4.5 Ball model of an oxygen atom where one electron in 1s energy level is emitted

XPS was first developed by Swedish scientist Kai Siegbahn in 1960s for chemical analysis and surface sensitive measurements. Figure 4.6 shows a schematic diagram of a XPS system. During measurement, the surface of a material is irradiated with a beam of X-rays and the photons cause the emission of electrons. The emitted electrons are filtered by a set of electrostatic or magnetic lens and then get focused onto the analyzer entrance slit. The hemispheric analyzer generates an electrostatic field which only collects the electrons of a given energy (known as Pass Energy) and allows them to reach the detector [50]. Therefore, the binding energy of electrons can be calculated as

$$E_{binding} = h\upsilon - E_{kinetic} \tag{44}$$

where $h\upsilon$ is defined as the energy of the photon.

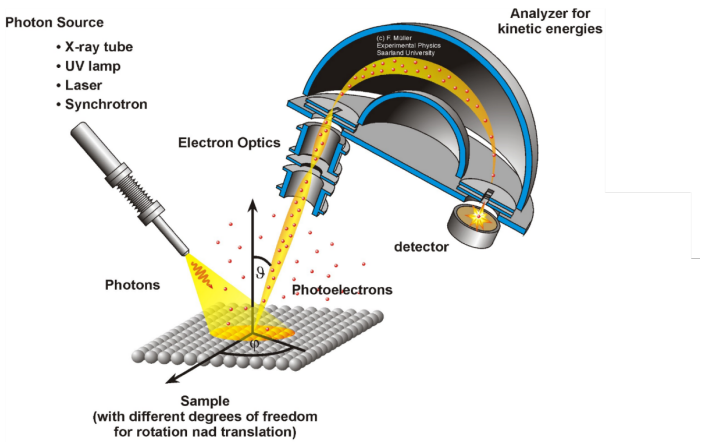

Figure 4.6 X-ray Photoelectron Spectroscopy (XPS) Measurement System [51]

By knowing the binding energy, one can determine the orbital energy of the atom and identify certain elements because every element gives its own unique set of binding energy levels. Moreover, the binding energy profile for compounds is slightly different from that of pure elements which is known as the chemical shift. By observing the shift in binding energies, one can determine the chemical oxidation state and composition.

4.6. Transfer Length Measurement (TLM)

Transfer Length Measurement (TLM) is commonly used for determining the contact resistance [52]. In the TiO_2-based solar cell structure, the metal is directly contacted with TiO_2, indicating that the dominant transport mechanism for electrons is tunneling. Therefore, it is important to measure the contact resistance so that one can have some idea of how good the contact between metal and semiconductor is, also determine the selectivity of metal oxide.

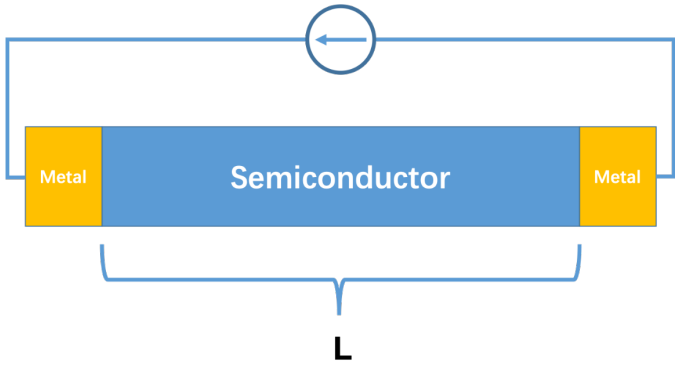

Figure 4.7 Schematic diagram of contact resistance measurement

Figure 4.7 shows a simple resistor diagram where two metal contacts are made at the end of the semiconductor. The semiconductor has a length of L and each metal contact has an area of A_c. The total resistance can be expressed as

$$R_T = 2R_C + 2R_M + R_{Semi} \tag{45}$$

where R_C is the contact resistance, R_M is the metal resistance and R_{Semi} is the semiconductor resistance. In most cases, R_M is very low and can be neglected; therefore, the equation becomes

$$R_T = 2R_C + R_{Semi} \tag{46}$$

The semiconductor resistance can be expressed as

$$R_{semi} = R_S \frac{L}{W} \tag{47}$$

where R_S is known as the sheet resistance. In order to have a standard comparison of different metal/semiconductor contacts, the contact resistivity is used which ignores the contact size related effect, and can be expressed as

$$\rho_C = R_C A_C \tag{48}$$

Due to the fact that the current flow in the contact is not uniform, thus, the physical length and width of the contact cannot be used to determine the contact area [53]. Generally, the density of current flow is the highest at the edge of the contact, and it drops exponentially as it moves away from the edge. This effect is known as Current Crowding and the effective length of the contact is defined as transfer length which can be expressed as

$$L_T = \sqrt{\frac{\rho_C}{R_S}} \tag{49}$$

The transfer length is the average distance that the carrier travels in the semiconductor before it flows into the contact . Therefore, the contact resistance becomes

$$R_C = \frac{\rho_C}{L_T W} = \frac{R_S L_T}{W} \tag{50}$$

The total resistance then becomes

$$R_T = \frac{R_S}{W}(L + 2L_T) \tag{51}$$

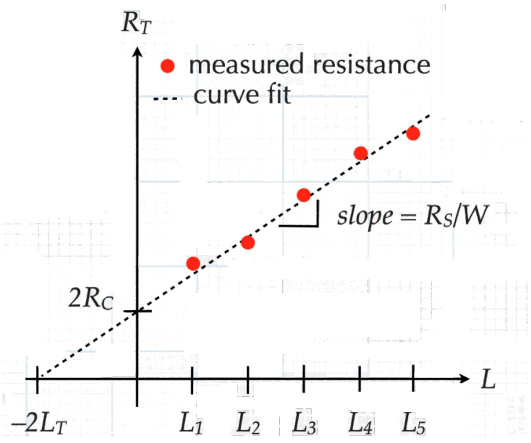

Figure 4.8 Total resistance as a function of resistor length [53]

Figure 4.8 shows the plot of total resistance versus resistor length. By extrapolating the curve back to Y-axis and X-axis, one can get both the contact resistance and the transfer length where the intercepts represent $2R_C$ and $2L_T$ respectively.

5. Experimental Section

This chapter gives a detailed illustration for processing, including the fabrication of MoO_x based FBC solar cells, TiO_x symmetric test and the fabrication of TiO_x based FBC solar cells.

5.1. Fabrication of MoO_x Based FBC Solar Cells

Polished n-type c-Si wafers are used as starting materials with the specifications shown in Table 5.1.

Table 5.1 Specification of starting c-Si wafers

Wafer Brand	Diameter [mm]	Doping Type	Thickness [μm]	Crystal Orientation	Resistivity [$\Omega \cdot cm$]
Topsil	99.7-100.3	n-type	255-305	100	1-5

The c-Si wafers are first cleaned with standard cleaning method, then they are transferred to the Marangoni HF (0.55%) bath and soaked for 4 minutes followed by 4-minute DI water rinsing to remove the surface oxide. The cleaned c-Si wafers are soaked in HNO_3 solution (69.5%) at room temperature for 60 minutes, followed by 5-minute DI water rinsing and drying to obtain a wet-chemically grown SiO_2 film. After that, the samples are loaded into the LPCVD furnace to grow poly-Si layers with a deposition temperature of 580 ^oC and deposition time of 1 hour and 53 minutes. The rear side is then covered with SiO_2 protection layer (200 nm) by means of PECVD with the standard deposition recipe. Texturing is done by TMAH bath at 80 ^oC for 15 minutes where random pyramids are grown on the unprotected front side. The wafers are then cleaned and dipped in BHF 1:7 solution to remove the SiO_2 protection layer. After that, Phosphorus are implanted into the rear side with an ion energy of 20 keV and dose of 6E15. The wafers are cleaned again before being transferred to the furnace to do oxidation and hydrogenation. 2 cycles of standard cleaning are performed to remove the contaminations and nanoscale roughness introduced during texturing, followed by

4 minutes of HF (0.55%) dip and DI water rinsing. After that, intrinsic a-Si:H of optimized thickness is deposited on the substrate by means of PECVD, followed by 10 nm PVD thermal evaporation of MoO_x (0.01 nm/s) and 75 nm ITO coating. Finally, $1\mu m$ metallization is done by E-Beam evaporation with full-area at rear side and hard mask at the front side.

5.2. Symmetric Test for TiO_x

Polished n-type c-Si wafers are used as starting materials with the specifications shown in Table 5.1. The c-Si wafers are first cleaned with standard cleaning method, then they are transferred to the Marangoni HF (0.55%) bath and soaked for 4 minutes followed by 4-minute DI water rinsing to remove the surface oxide. In the case without any interfacial layers, the cleaned wafers are immediately loaded into PVD and TiO_x of various thickness is deposited (0.02 nm/s) on both sides of the samples. In the cases with interfacial layers, the cleaned wafers are first immediately transferred to the corresponding chambers to deposit interfacial layers (for instance, PECVD for intrinsic a-Si:H deposition, PVD for Ti deposition and HNO_3 (69.5%) for SiO_2 growth). After that, TiO_x of different thickness is deposited (0.02 nm/s) on both sides of the samples. The prepared samples are cut into quarter wafers and annealed in forming gas with Rapid Thermal Process (RTP) equipment under different annealing conditions.

5.3. Fabrication of TiO_x Based FBC Solar Cells

Polished n-type c-Si wafers are used as starting materials with the specifications shown in Table 5.1. The c-Si wafers are first cleaned with standard cleaning method, then they are transferred to the Marangoni HF (0.55%) bath and soaked for 4 minutes followed by 4-minute DI water rinsing to remove the surface oxide. The cleaned c-Si wafers are soaked in HNO_3 solution (69.5%) at room temperature for 60 minutes, followed by 5-minute DI water rinsing and drying to obtain a wet-chemically grown SiO_2 film. After that, samples are transferred to PECVD and 10 nm intrinsic a-Si:H and 10 nm p-type a-SiO_x are deposited in sequence, followed by high-temperature (850°C) annealing for 45 minutes. To improve passivation of poly-SiO_x, 10 nm AlO_x is coated with ALD at the temperature of 300 °C, followed by 30-minute of forming gas annealing at 400 °C.

Then the samples are etched in HF (0.55%) solution for 3 minutes to remove the AlO_x as well as the surface oxides. In the case without interfacial layers, the etched samples are immediately transferred to the PVD and the rear side is coated with TiO_x (0.02 nm/s) by E-beam evaporation. In the case with interfacial layers, the etched samples are immediately transferred to the corresponding chambers to deposit interfacial layer (for instance, PECVD for intrinsic a-Si:H deposition, PVD for Ti deposition and HNO_3 (69.5%) for SiO_2 growth). Then, 4 nm TiO_x is deposited (0.02 nm/s) on the rear side of the samples followed by $1\mu m$ of metallization where the first 300 nm is evaporated thermally and the rest is completed by E-beam. After that, the samples are annealed in forming gas at optimized temperatures for 4 minutes. To facilitate the collection of holes at the front side, 75 nm ITO is sputtered on top of the surface, followed by 2 μm of metallization with hard mask where the first 300 nm is evaporated thermally and the rest is completed by E-beam.

6. Results and Discussion

In this chapter, the implementation of transition metal oxides (i.e. MoO_x and TiO_x) as HTL and ETL are discussed respectively. First, the MoO_x based heterojunction solar cell is investigated based on the following research questions: 1) The influence of processes on the passivation level of precursors; 2) The influence of (i)a-Si:H thickness on the device performance; 3) The influence of c-Si surface pre-treatment; 4) The influence of annealing on the passivation quality. The investigation in TiO_x is carried out by first looking into the surface passivation of c-Si/TiO_x and c-Si/SiO_2/TiO_x stacks where symmetric test is performed. Then the influence of TiO_x source material on the passivation performance is also discussed, and the optimal processing conditions are determined. After that, the passivation quality of c-Si/(i)a-Si:H/TiO_x is investigated based on the new TiO_x source material. Finally, optimized TiO_x is integrated into the FBC solar cells where various rear side structures (i.e. c-Si/TiO_x, c-Si/SiO_2/TiO_x, c-Si/(i)a-Si:H/TiO_x and c-Si/Ti/TiO_x) are tested.

6.1. MoO_x Integrated Heterojunction Solar Cell

As it is already mentioned before, MoO_x is a suitable material to form the hole selective contact in a solar cell. In order to investigate the passivation property of MoO_x based hole selective contact, the rear side of the heterojunction solar cell is passivated by the standard SiO_2/n^+ poly-Si stack whose excellent electron selective passivation quality has already been demonstrated [11]. At the front side, a stack of (i)a-Si:H/MoO_x is used where the i-layer is working as the interfacial chemical passivation layer.

In this subsection, the performance of (i)a-Si:H/MoO_x working as a hole selective contact is investigated based on the following aspects: 1) Influence of processes on the passivation level of cell precursor; 2) Influence of the thickness of intrinsic a-Si:H on the cell performance; 3) Influence of cell pretreatment on the passivation quality; 4) Influence of post annealing on open-circuit voltage (Voc).

6.1.1. Influence of Processes on the Passivation Level of Cell Precursors

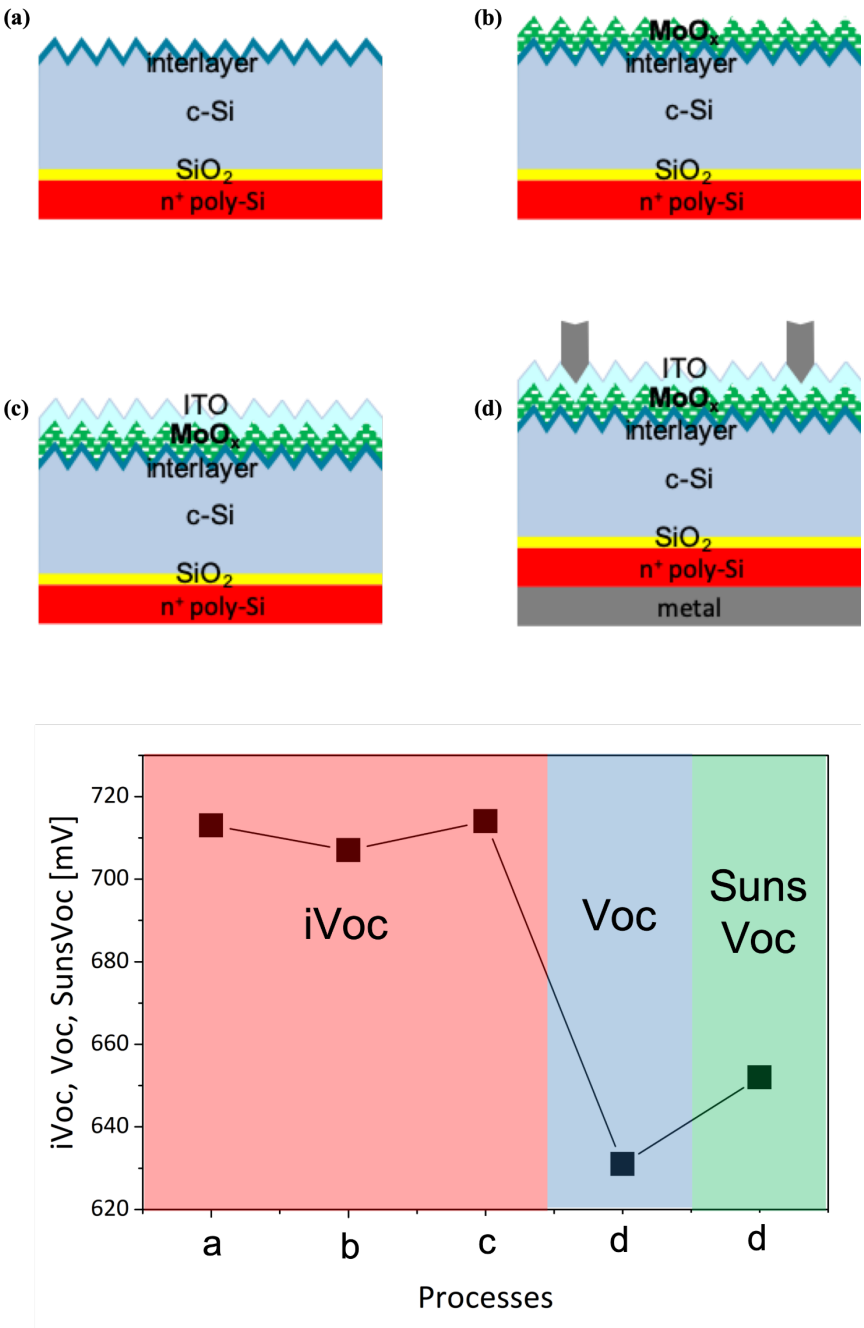

Figure 6.1 Influence of precursor steps on the passivation quality characterized by iVoc, Voc and SunsVoc where the precursors are denoted by a, b, c and d on X-axis, and the corresponding device structures are schematically shown above

The influence of processes on the passivation property of cell precursors is investigated by measuring the Voc (including iVoc and SunsVoc) after each step of process. In this

part, the thickness of i-layer and MoO_x are chosen as 9 nm and 5 nm respectively. The iVoc and Voc results as well as the corresponding precursor structures are shown in Figure 6.1.

It is obvious that the intrinsic a-Si:H layer can provide an excellent surface passivation quality at the front side which sees an iVoc of 713 mV. After the deposition of MoO_x and ITO layer, the iVoc first goes down slightly to 709 mV then recovers back to 714 mV which indicates that the surface passivation quality is not degraded. The small voltage difference could be resulted from the measurement error. However, after the metal grids are formed, the complete solar cell shows a much lower Voc which drops dramatically to 632 mV. This degradation can be mainly attributed to both the damage of surface passivation quality during E-beam metallization process and the non-ideal carrier extraction ability of MoO_x.

First, the surface passivation quality is limited by the E-beam metallization [54]. The deposition of materials by using electron beam evaporation generates energetic radiation which increases the trap states at the layers and their interfaces. The thickness of as-deposited (i)a-Si:H/MoO_x/ITO stack is around 85 nm; covering on top of the c-Si bulk with such a thin layer of passivation stack is not able to prevent the penetration of high energetic radiation. As the covalent bonds receive the radiation energy, they tend to break and additional dangling bonds are created at the interfaces which gives rise to the recombination rate. Another potential E-beam induced damage is caused by the bombardment of charged particles on the sample surface. During evaporation, electrons are scattered by the evaporating metal atoms where part of them are redirected to the sample surface. This large flux of electrons is of high kinetic energy; thus, it bombards the surface layers and their interfaces. This process generates unexpected defects which significantly degrades the properties of the thin film material and therefore, their passivation property. Potential solution is by thermally evaporating a few hundred nanometers of metal layer which is able to protect the layers underneath from the damage caused by E-beam metallization. Therefore, it is suggested to first thermally evaporate 100 nm metal as a protection layer, then use E-beam evaporation to complete the metal grids.

Besides, the non-ideal carrier selectivity of (i)a-Si:H/MoO_x stack also plays an important role in the drop of open circuit voltage. As it is already mentioned in Chapter 4, iVoc is the maximum achievable open-circuit voltage if the surface passivation

quality is the only limit factor; whereas SunsVoc is measured directly from the external voltage, thus, it eliminates the series resistance related effect and can be used to characterize the carrier selectivity. Here, SunsVoc is measured and the result is plotted in Figure 6.1. It can be seen that the SunsVoc (652 mV) is a bit higher than the Voc achieved from I-V measurement, but it is still significantly lower than the iVoc before metal contacts are made. This large difference between SunsVoc and iVoc indicates that our (i)a-Si:H/MoO_x stack does not offer an ideal selectivity for the carriers, therefore, besides the efficient hole transport, the electrons can also pass the i-layer and then recombine at the MoO_x/metal interfaces, which dramatically reduces the cell Voc. According to Equation 21, the selectivity is inversely proportional to the saturation current density and the contact resistance. The latter can be calculated by [55]

$$Rs = \frac{V_{mpp,SunsVoc} - V_{mpp,I-V}}{J_{mpp,I-V}} \tag{52}$$

where $V_{mpp,SunsVoc}$ is the maximum power point voltage from SunsVoc measurement, $V_{mpp,I-V}$ and $J_{mpp,I-V}$ are the maximum power point voltage and current extracted from the I-V curve respectively. The corresponding results are shown in Table 6.1.

Table 6.1 Series resistance of the solar cell based on (i)a-Si:H/MoOx stack under illumination

$V_{mpp,SunsVoc}$ [mV]	$V_{mpp,I-V}$ [mV]	$J_{mpp,I-V}$ [mA/cm^2]	Rs [Ohm·cm^2]
605	464	31.10	4.53

The current density is calculated based on the effective area with a correction factor of 1.12. It is obvious from the table that the (i)a-Si:H/MoO_x stack does not provide the majority holes with good conductivity, leading to a non-ideal selectivity. Such high series resistance on one hand, can be resulted from the thick intrinsic a-Si layer and MoO_x which lowers the tunneling possibility of holes; on the other hand, the surface field that formed at the c-Si/(i)a-Si:H/MoO_x junction is reduced by ITO deposition whose work function is close to that of c-Si. Therefore, the band bending is not powerful enough to generate strong surface field at the interface to facilitate the transport of holes while block the electrons, leading to the degradation of passivation quality.

In conclusion, the passivation quality of cell precursors can be evaluated by measuring iVoc after each step of process and SunsVoc after metal contact is formed.

The large iVoc (~715 mV) after individual deposition of (i)a-Si:H, MoO_x and ITO indicates an excellent surface passivation property, and the fabrication of as-deposited stack structure do not influence the passivation performance. By contrast, a low SunsVoc (652 mV) indicates an non-ideal carrier selectivity of MoO_x which is not able to effectively extract holes from the bulk while block the electrons, leading to a significant degradation in the overall passivation quality. Moreover, the additional interface or layer defects induced by E-beam metallization further reduce the Voc to 631 mV. Therefore, it is suggested to thermally evaporate a 100 nm metal protection layer at the first metallization stage [54].

6.1.2. Influence of (i)a-Si:H Thickness on Device Performance

In the previous section, it is concluded that the carrier selectivity of as-deposited (i)a-Si:H/MoO_x stack is not ideal which leads to a significant degradation in the overall cell passivation quality. In this section, the thickness of i-layer is varied (here we chose 6 nm, 8 nm and 10 nm), and the corresponding external parameters of the solar cells are characterized by measuring their I-V curve.

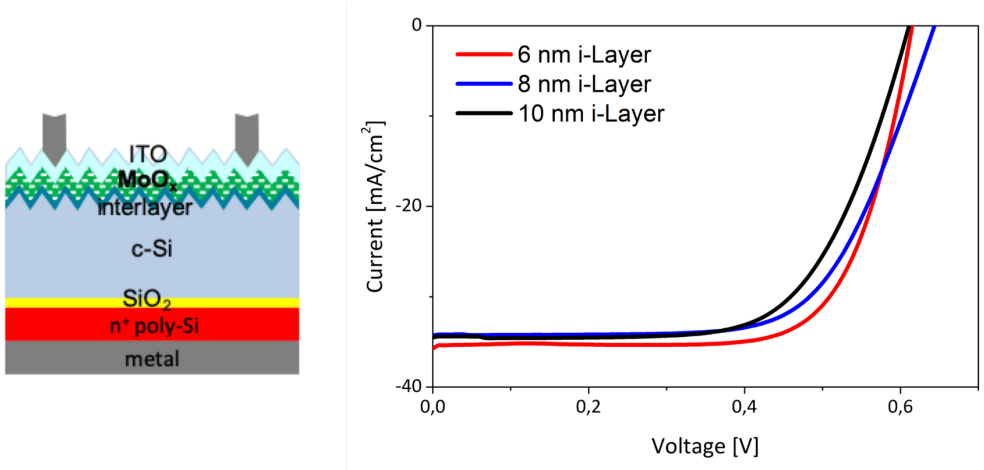

Figure 6.2 Cell architecture and I-V curves where the thickness of i-layer is 6, 8, 10 nm respectively

Figure 6.2 shows the architecture and I-V curves of the MoO_x based FBC solar cells where the thickness of i-layer is 6, 8 and 10 nm respectively. First, the value for shunt resistance and series resistance can be estimated from the I-V curves. By looking at the region that is close to the short-circuit current point, it is clear that the curves are

quite horizontal which indicates a high shunt resistance among all three solar cells. Generally, a high shunt resistance is expected during the fabrication of solar cells due to the fact that low shunt resistance can reduce the utilization of photo-generated current by directing it to an alternate path [56]. This shunted current does not contribute to the current output of the solar cell which leads to a power loss of the device especially at low irradiance levels. The effect of a low shunt resistance on I-V curve is schematically shown in Figure 6.3 (a). In order to numerically compare the shunt resistance of these three solar cells, the measurement results are also plotted in Figure 6.3 (b).

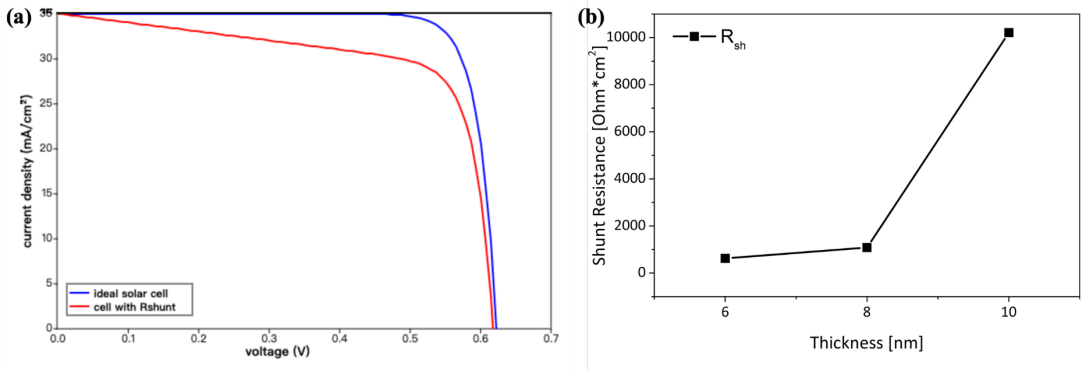

Figure 6.3 a) Effect of shunt resistance on I-V curve when R_{sh}=100 [Ohm·cm^2] [57] b) Shunt resistance of solar cell with different thickness of i-layer (623, 1083 and 10210 [Ohm·cm^2] for 6, 8, 10 nm thick i-layer respectively).

The shunt resistance is mainly associated with highly conductive paths which connect directly the front and back contacts. They can be found within the solar cells or at the cell edges. Crystal scratches, impurities or voids introduced during fabrication processes can give rise to those potential shunt current [56]. The shunt paths at the cell edges can be effectively eliminated by proper cutting of the solar cells before measurement, while those within the bulk can be minimized by optimizing process conditions. In Figure 6.3 (b), all solar cells are featured with high shunt resistance, which represents that high quality p-n junctions are fabricated by using current deposition conditions. Besides, one can also see that R_{sh} goes up with the increase of i-layer thickness, indicating less shunt paths are present in large i-layer thickness cases. This can be mainly attributed to the high surface roughness that introduced by texturing [58]. In order to enhance the light trapping ability, the front side of FBC solar cell is usually textured where random pyramids are generated. Those pyramids not only

increase the surface area, but they also allow the light to be reflected for multiple times. However, the high roughness of textured surface increases the risk of connecting the two opposite contacts directly by the ITO, especially when the carrier selective region is ultrathin (i.e. in the range of nm). In our case, the thickness of passivation stack is less than 20 nm. With such a thin layer, unexpected pinholes or voids can be present and are subsequently filled during the ITO deposition. As a highly conductive material, ITO creates easy paths for carrier transport which lowers the shunt resistance. Therefore, larger i-layer thickness has higher chance to uniformly cover the textured surface and minimize the density of pinholes, which in turn increases the shunt resistance.

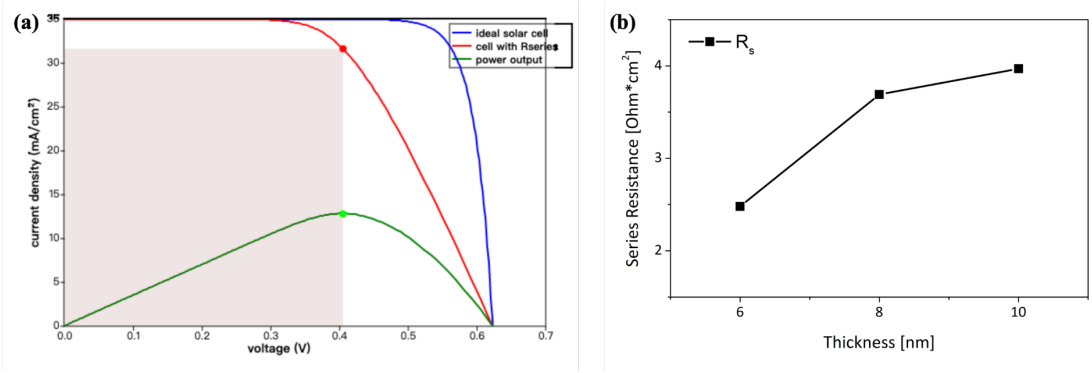

Figure 6.4 a) Effect of high series resistance (Rs=5 [Ohm • cm^2]) on I-V curve [59] b) Series resistance of solar cells where i-layer thickness is 6, 8, 10 nm respectively

Table 6.2 MPP voltage and current and SunsVmpp of solar cells with different i-layer thickness

Thickness [nm]	**V_{mpp} [mV]**	**J_{mpp} [mA/cm²]**	**$SunsV_{mpp}$ [mV]**	**R_s [Ohm·cm²]**
6	466	36.29	556	2.48
8	472	34.72	600	3.69
10	447	31.80	573	3.97

On the other hand, the slope of curves in the vicinity of open-circuit voltage is not vertical which indicates a high series resistance. Opposite to shunt resistance, a low series resistance is expected in the solar cell due to the fact that high series resistance can cause more energy dissipation within the solar cell. Therefore, the output performance is deteriorated and less power is able to be extracted and supplied to the external circuit. The effect of high series resistance is schematically shown in Figure

6.4 (a). According to Section 6.1, the series resistance can be calculated by Equation 24. Important external parameters are listed in Table 6.2 and calculated series resistances are plotted in Figure 6.4 (b).

It can be seen that the series resistance increases as the i-layer thickness is increased. This is in accordance with the I-V curves shown in Figure 6.2 where 6 nm case shows the largest slope, while 8 nm and 10 nm cases are sharing similar and smaller slope at the region close to the open-circuit voltage point. This higher series resistance is mainly resulted from the increase of i-layer thickness. In the work done by M. Leilaeioun *et.al.* [60], they reported that the varied intrinsic a-Si:H layer thickness in silicon heterojunction solar cells is the main contribution to the change of series resistance. Figure 6.5 (a) shows the architecture of the solar cell and Figure 6.5 (b) plots the series resistance of solar cell and the contact resistance of the hole contact region as a function of the i-layer thickness. One can see that both resistances are increased as the increase of i-layer thickness and they are following similar trend. The difference between series resistance and contact resistance is nearly constant which indicates that the major contribution to the series resistance increase is the larger contact resistance between the metal and c-Si induced by the increase of the i-layer thickness. Therefore, it can be concluded that in our case, the series resistance increase is mainly associated with the larger thickness of i-layer.

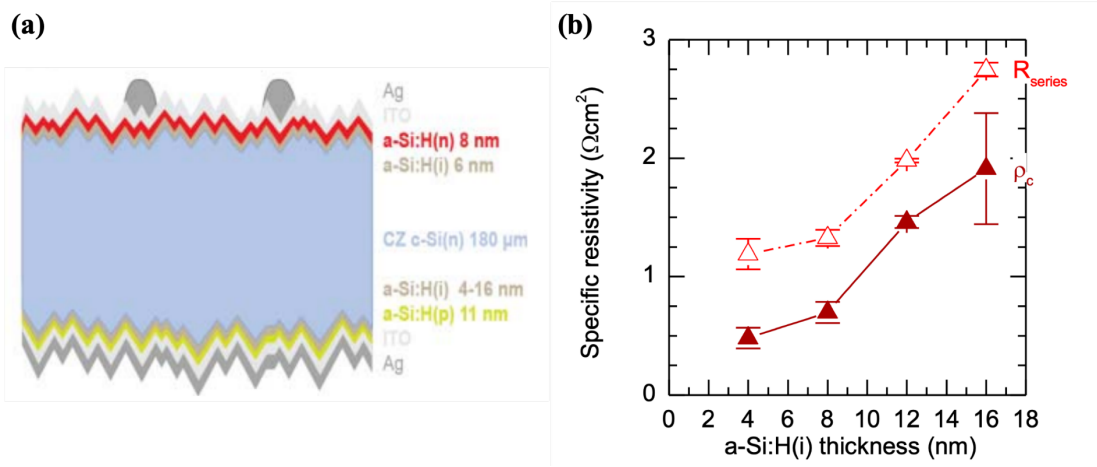

Figure 6.5 a) Heterojunction solar cell architecture b) Series resistance of solar cell and contact resistance of hole contact region as a function of i-layer thickness [60]

Both shunt resistance and series resistance can have impact on the performance of

solar cell and it is mainly reflected by FF. The equations for FF as a function of both series resistance and shunt resistance are expressed as follows [57][59]:

$$FF_{series} = FF_0(1 - r_s) \tag{53}$$

$$FF_{shunt} = FF_0(1 - \frac{1}{r_{sh}}) \tag{54}$$

where FF_0 denotes the fill factor that is neither affected by series resistance nor shunt resistance, r_s and r_{sh} are the normalized series and shunt resistance. An empirical equation that combines both the impact of series resistance and shunt resistance on FF is given as [61]:

$$FF = FF_0\left\{(1 - 1.1r_s) + \frac{{r_s}^2}{5.4}\right\}\left\{1 - \frac{V_{oc} + 0.7}{V_{oc}}\frac{FF_0}{r_{sh}}\left[(1 - 1.1r_s) + \frac{{r_s}^2}{5.4}\right]\right\} \tag{55}$$

Apparently, the fill factor can be enhanced by either increasing the shunt resistance or reducing the series resistance. Figure 6.6 (a) compares the pseudo-fill factor (pFF) obtained from SunsVoc measurement and the FF extracted from I-V measurement.

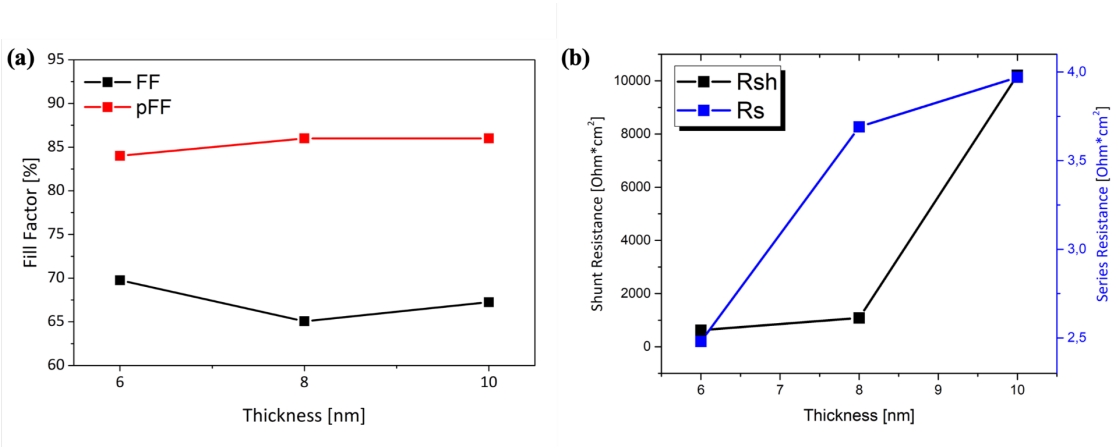

Figure 6.6 a) pFF and FF of solar cell as a function of varying thickness of i-layer b) Series resistance and shunt resistance of solar cells as a function of i-layer thickness

One can see from Figure 6.6 that pFF remains nearly constant at 85% and increases slightly in the case of thicker i-layer because of an improved surface passivation quality. By contrast, the FF for each i-layer thickness is much lower than the corresponding pFF due to the fact that pFF measurement does not take into account the effect of series resistance. Besides, it is also clear that the FF decreases first from 69.76% to 65.60% then recovers back to 69.99%. This phenomenon can be mainly attributed to the trade-off between the impacts caused by series resistance and shunt resistance. Figure 6.6 (b)

shows both the series resistance and shunt resistance as a function of i-layer thickness. Obviously, as the i-layer thickness varies from 6 to 10 nm, the series resistance sees a large increase from 2.48 to 3.69 [Ohm·cm^2], and ends up with 3.97 [Ohm·cm^2]. Meanwhile, the shunt resistance shows another way around which first increases slightly from 623 to 1083 [Ohm·cm^2], then it jumps to 10210 [Ohm·cm^2]. As it is already demonstrated before, the FF is simultaneously influenced by series resistance and shunt resistance. Therefore, the FF is first dominated by the increase of series resistance which results in the decrease in FF; then the jump in shunt resistance effectively compensates the small increase of series resistance and brings up the FF.

To determine the passivation quality of the i-layer with different thickness, Voc (I-V) and SunsVoc are plotted in Figure 6.7. It can be seen from the figure that as the i-layer thickness increases from 6 nm to 10 nm, the SunsVoc first increases from 627 mV to 657 mV then it drops to 629 mV.

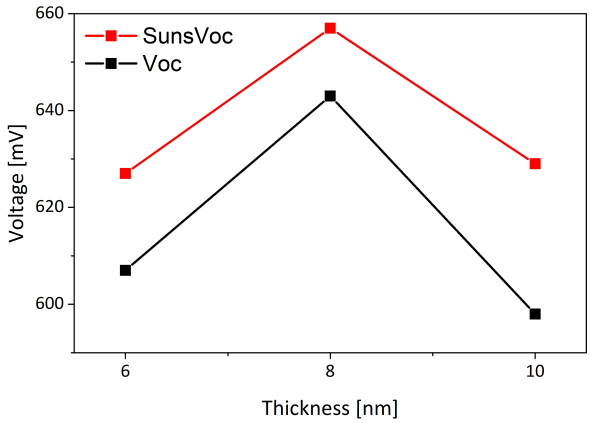

Figure 6.7 SunsVoc and Voc (I-V) of solar cells with varying i-layer thickness

The degraded passivation at 6 nm i-layer case can be mainly attributed to the non-ideal surface passivation that provided by such thin i-layer which is unable to cover the substrate uniformly. The surface nanometer scale roughness, introduced during texturing partially shades the substrate during i-layer deposition, leading to an inhomogeneous passivation layer. Larger thickness such as 8 nm is thought to be able to compensate the surface roughness which results in a more conformal i-layer and a better passivation quality. When the surface passivation quality induced by i-layer is saturated, further increase in i-layer thickness does not improve the surface passivation

property, but introduces higher series resistance for majority holes to be collected. This is in accordance with the fact that the difference between Voc and SunsVoc in 10 nm i-layer case is the largest, indicating the highest series resistance among these three cells. Therefore, 8 nm is chosen to be the thickness of interfacial passivation layer for further investigation because it effectively provides the interface with a conformal surface passivation layer and minimizes the negative influence caused by the series resistance.

Table 6.3 External parameters of MoO_x based solar cells where i-layer is 6, 8, 10 nm thick respectively

Thickness [nm]	**V_{oc} [mV]**	**J_{sc} [mA/cm^2]**	**V_{mpp} [mV]**	**I_{mpp} [mA]**	**FF [%]**	**PCE [%]**
6	607	40.10	466	36.29	69.76	16.90
8	643	38.73	467	34.72	65.06	16.18
10	598	34.75	447	31.80	69.99	14.51

The external parameters of MoO_x based solar cells with intrinsic a-Si:H of various thickness are listed in Table 6.3. Apparently, the case of 8 nm i-layer provides the best passivation quality which is represented by the highest Voc. However, it is still subject to a low shunt resistance, leading to a relatively low FF. A PCE of 16.18% is achieved with this MoO_x based heterojunction solar cell where the c-Si/MoO_x interface is passivated with 8 nm intrinsic a-Si:H layer.

6.1.3. Influence of Si Surface Pre-treatment

In the previous section, we demonstrated that 8 nm intrinsic a-Si:H interfacial layer can provide with the best surface passivation quality, and has the least negative influence on the carrier selectivity of (i)a-Si:H/MoO_x stack. However, the performance is still limited by the low shunt resistance and relatively low open-circuit voltage.

In the report written by D. Deligiannis *et.al.* [62], they find out that surface texturing can lead to poor interface quality of the a-Si:H/c-Si junction. The unavoidable contamination and nano-roughness (i.e. structural irregularities) introduced during surface texturing act as defect centers which significantly increases the recombination rate and brings down the open-circuit voltage. Therefore, they proposed a widely-used wet-chemical cleaning procedure to perform oxidation and stripping of the oxide for

multiple runs. This chemical treatment before layer growth is able to remove those texturing-introduced defects and minimize the density of recombination centers.

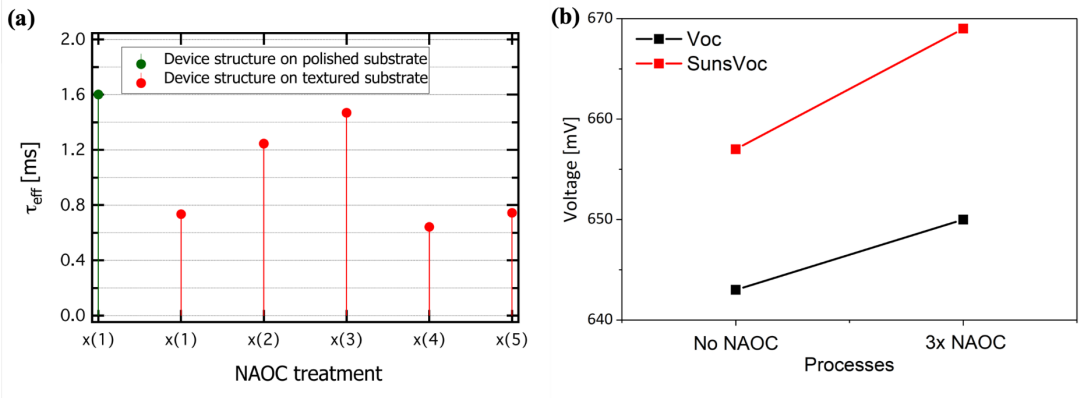

Figure 6.8 a) Effective lifetime measured after various cycles of NAOC treatment [62] b) FF and pFF of MoO_x based solar cells before and after performing 3 times of NAOC

It is demonstrated that 3 cycles of NAOC treatment can best improve the surface passivation quality as shown in Figure 6.8 (a). More cycles of NAOC treatment will again create similar roughness and bring down the effective lifetime. Figure 6.8 (b) shows the performance of Voc and SunsVoc before and after performing NAOC. It is clear that after 3 cycles of NAOC treatment, the SunsVoc increases from 657 mV to 669 mV. This can be mainly attributed to the removal of contaminations and surface roughness which reduces the defect density and improves the passivation quality. The Voc also sees a small increase from 643 mV to 650 mV, but interestingly, the difference between Voc and SunsVoc for NAOC case is larger than that for non-NAOC case, indicating a larger series resistance.

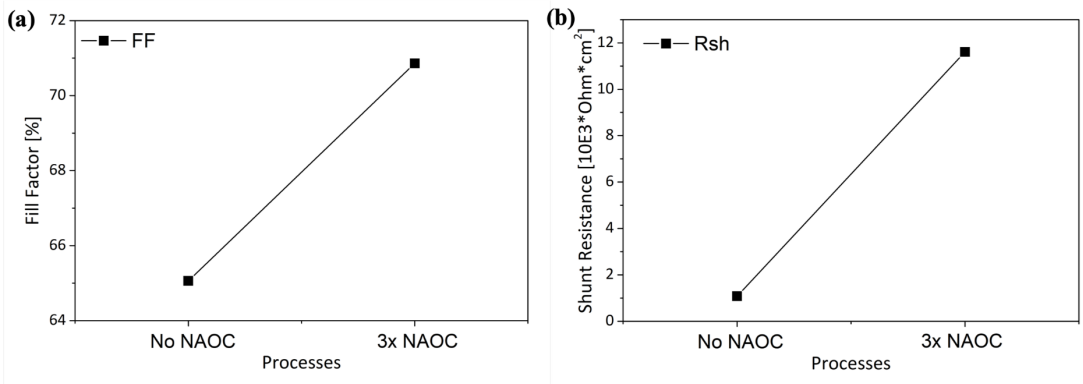

Figure 6.9 a) FF of solar cell before and after NAOC treatment b) Shunt resistance of solar cells before and after NAOC treatment

Figure 6.9 (a) shows the change of fill factor before and after NAOC treatment. One can see that the FF increases from 65% to 71% after NAOC treatment, which can be mainly attributed to a higher shunt resistance. As is already mentioned before, the surface roughness induced by texturing can form pinholes. Those pinholes might be filled with ITO and create direct connection between opposite contacts, leading to a low shunt resistance. By performing NAOC pre-treatment, the surface roughness is effectively reduced and pinholes are less likely to form during the deposition. Therefore, the homogeneous layer prevents the shunt paths from evolving, resulting in a jump in the shunt resistance (from 1000 to 10000 [Ohm·cm^2]) as shown in Figure 6.9 (b). The photo-conversion efficiency for this batch of solar cell is enhanced to 17.31%.

6.1.4. Influence of Annealing on Passivation Quality

To further improve the performance of MoO_x based heterojunction solar cells, post-annealing of the samples is applied which is believed to be able to enhance the passivation quality by relaxing the film when there is an abrupt transition from c-Si to the (i)a-Si:H [63]. In this section, both annealing time and temperature are varied to investigate their influence on the passivation quality and cell performance.

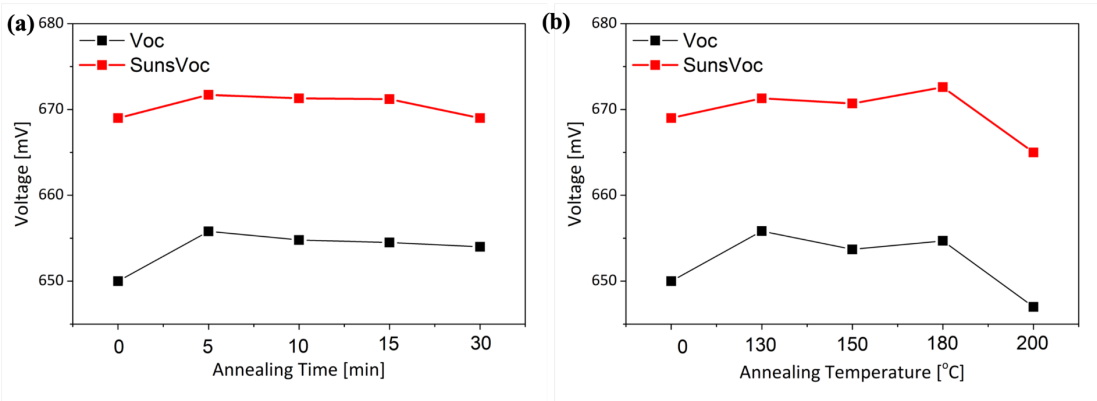

Figure 6.10 a) Voc and SunsVoc after annealing at 130°C for different time b) Voc and SunsVoc after annealing for 10 mins at different temperatures

According to the work done by J. Geissbühler *et.al.* [10], they evidence that 130 °C annealing under N_2 atmosphere can improve the device performance while further increased temperature will detrimentally impact the hole collection ability. Figure 6.10

(a) shows the Voc and SunsVoc of the device under 130 °C atmospheric annealing for different durations. One can see that both Voc and SunsVoc see an increase after 5-minute annealing, which can be mainly attributed to an improved passivation quality of the relaxed (i)a-Si:H/c-Si interface. Under low temperature annealing, film relaxation is taking place without creating additional dangling bonds. A more gentle transition at the interface is capable of removing potential defects which consequently improves the passivation quality. However, longer annealing period does not lead to better device performance because both Voc and SunsVoc remain nearly constant even after 30-minute of annealing. The tiny difference might be resulted from experimental errors.

To further investigate the temperature influence on the passivation property, the annealing time is kept at 10 minutes. Figure 6.10 (b) shows the Voc and SunsVoc as a function of annealing temperature. As expected, both Voc and SunsVoc show an increase after 10-minute atmospheric annealing under 130 °C, and it is clear that further increasing the temperature to 180 °C does not enhance the passivation quality. Therefore, low temperature atmospheric annealing is able to efficiently relax the (i)a-Si:H/c-Si interface. However, when the temperature reaches 200 °C, one can see a significant drop in both Voc and SunsVoc. Such passivation degradation can be mainly attributed to the effusion of H atoms which used to be in the i-layer to passivate dangling bonds [64]. Higher temperature provides larger energy to the H atoms, and allows them easier to de-bond from Si and escape from the film. The vacancy of H atoms generates additional dangling bonds in i-layer and the c-Si/i-layer interface which brings down the Voc. It can be foreseen that further increasing the annealing temperature to above 200 °C will cause more damage to the i-layer passivation quality.

Based on the above discussion, it is clear that the device should undergo a 10-minute atmospheric annealing under 130 °C to further improve the passivation quality by relaxing the (i)a-Si:H/c-Si interface. The final photo-conversion efficiency after annealing is enhanced to 17.60%.

6.2. TiO_x Based Electron Selective Layer

Ultrathin TiO_x layer has been demonstrated to form an electron-selective contact due to its small conduction band offset and large valence band offset which facilitates the collection of electrons but repels the holes [7].

In this subsection, the passivation quality of various TiO_x architecture (c-Si/TiO_x, c-Si/SiO_2/TiO_x, c-Si/(i)a-Si/TiO_x and c-Si/Ti/TiO_x) is investigated by means of symmetric test in the following aspects: 1) Influence of stack thickness combination on the passivation quality; 2) Influence of annealing temperature and time on the passivation quality; 3) Influence of PVD TiO_x source on the passivation quality. After optimizing the passivation of TiO_x stack, the TiO_x based FBC solar cells are fabricated where p^+ poly-SiO_2 is adopted as the hole transport layer.

6.2.1. Surface Passivation Quality of c-Si/TiO_x Stack

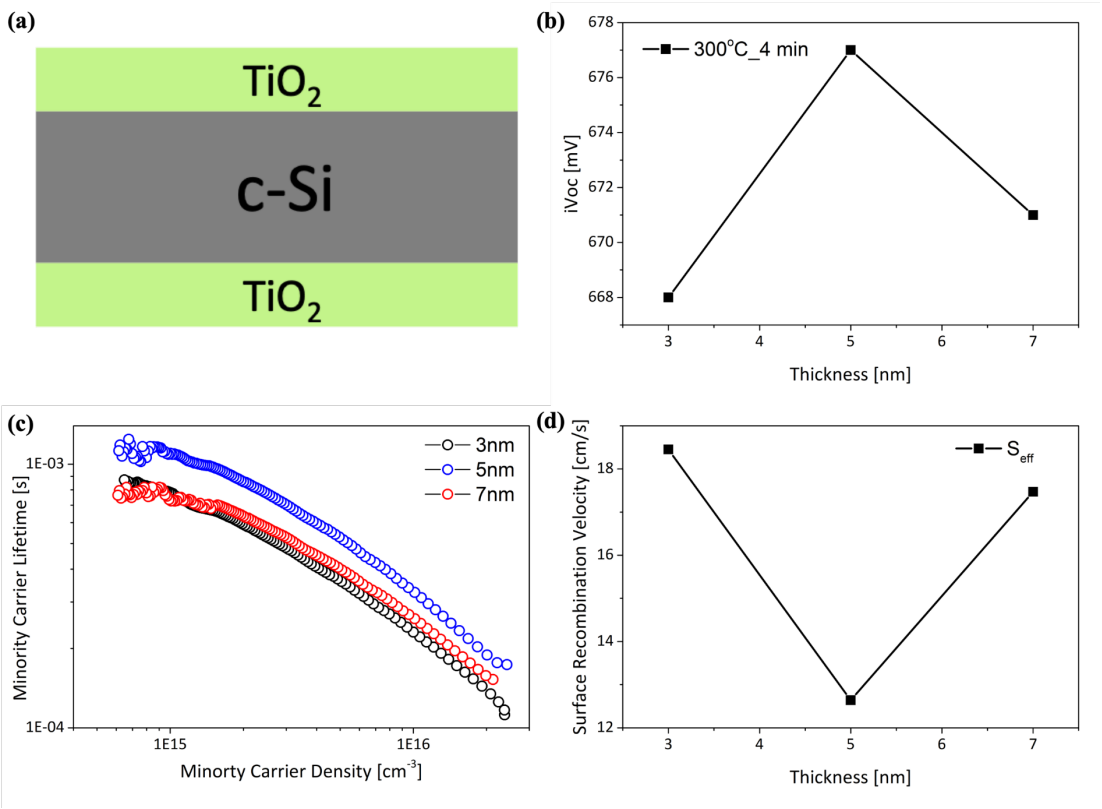

Figure 6.11 Passivation quality of different thickness of TiO_x in a) Symmetric test structure of c-Si/TiO_x stack; b) iVoc of different thickness of TiO_x after 300°C FGA for 4 minutes; c) Injection level dependent effective lifetime of different thickness of TiO_x after 300°C FGA for 4 minutes; d) Surface recombination velocity of different thickness of TiO_x after 300°C FGA for 4 minutes.

The passivation quality of TiO_x was first investigated on bare c-Si wafer without any interfacial passivation layer. TiO_x of various thickness (3 nm, 5 nm and 7 nm) was

deposited by PVD E-beam evaporation on c-Si wafer and underwent forming gas annealing (FGA) with different temperature and time. Figure 6.11 schematically shows the symmetric test architecture of c-Si/TiO_x stack, and the passivation quality of different thickness of TiO_x.

It can be seen from Figure 6.11 (b) that ultrathin TiO_x can properly passivate the n-type c-Si surface. As the thickness increases from 3 to 7 nm, the iVoc first increases from 668 mV, then it sees a decrease and ends up with 671 mV. The maximum iVoc of 677 mV is obtained in the case of 5 nm TiO_x film. Figure 6.11 (c) shows the injection level dependent effective lifetime of the samples passivated by 3, 5 and 7 nm TiO_x. One can see that as the thickness of TiO_x increases from 3 to 5 nm, the effective lifetime (at the injection level of $1 \times 10^{15} cm^{-3}$) is improved from 759 to 1107 μs. Further increasing the thickness to 7 nm brings down the effective lifetime to 801 μs. The effective surface recombination velocity S_{eff} can be calculated by [65]

$$\frac{1}{\tau_{eff}} = \frac{1}{\tau_{bulk}} + \frac{2S_{eff}}{W} \tag{56}$$

where τ_{eff} is the effective lifetime, τ_{bulk} is the bulk lifetime and W is the wafer thickness. As is already mentioned before, the bulk lifetime can be assumed to be infinite due to the developed c-Si bulk fabrication technology. Therefore, Equation 56 can be simplified to

$$S_{eff} = \frac{W}{2\tau_{eff}} \tag{57}$$

Knowing that the wafer thickness is 0.028 cm, thus, the surface recombination velocity of TiO_x samples with different thickness is obtained and plotted in Figure 6.11 (d). It is clear that 5 nm case gives the lowest surface recombination velocity of around 13 cm/s.

The results demonstrate that ultrathin TiO_x can provide excellent surface passivation quality on n-type c-Si surface. This can be attributed to the formation of Ti-O-Si bonding after proper FGA treatment [66]. When thin layer TiO_x is deposited on c-Si, the abrupt transition results in a non-ideal interface where defects such as dangling bonds trap the holes which then recombine with electrons. This is in accordance with the truth that a large surface recombination velocity (700 cm/s) is measured in the as-deposited TiO_x/c-Si structure. After adequate forming gas annealing, the TiO_x/c-Si interface experienced rebinding where Ti-O-Si bonding is formed. This bonding reduces the c-Si surface defect states at the interface, leading to a significant

improvement in the minority carrier effective lifetime. Meanwhile, TiO_x deposited by PVD at room temperature tends to give defective layer because the Ti-O bonding are not properly equilibrated within the layer due to the low diffusion coefficient at the surface. Therefore, such PVD-grown TiO_x is of larger void density, porosity and unbalanced bonding profile which results in higher defect densities and poorer passivation quality. FGA mobiles the atoms where rebinding and relaxation of the film occurs which reduces the defect densities, and in turn gives rise to the passivation quality.

Besides, it is also seen that the champion thickness of TiO_x is 5 nm which gives the best surface passivation quality with a surface recombination velocity of 13 cm/s, while in the case of 3 and 7 nm, a lower minority carrier effective lifetime is obtained. The non-ideal passivation quality in 3 nm case can be attributed to the inhomogeneous layer deposited by PVD. Although the deposition rate has been kept at extremely low (0.02 nm/s), 3 nm layer is still too thin for PVD to deposit uniformly. The nonuniform coating of TiO_x thin layer leads to an incomplete formation of Ti-O-Si bonding at part of the surface areas which brings down the passivation quality. On the other hand, when the thickness is increased to 7 nm, the surface passivation sees a decrease. The mechanism behind has been reported by I. Yu *et.al.*[67], who found out that as the thickness of film increases, the tensile stress in the film decreases while the compressive stress starts to play a role. The higher compressive stress facilitates the crystallization of TiO_x during FGA, and anatase phase forms. It is known that as-deposited TiO_x at room temperature is of amorphous phase [68], and amorphous TiO_x film is preferred for the surface passivation of c-Si because more Ti-O-Si bonding can be formed and fewer defect states are present at the interface. Therefore, the easier transformation to anatase phase in thicker TiO_x case after FGA due to larger compressive stress causes the degradation of surface passivation quality. Moreover, thicker TiO_x film tends to have higher surface roughness. This strain-induced surface roughness introduces additional defects at the interface, leading to a lower effective lifetime.

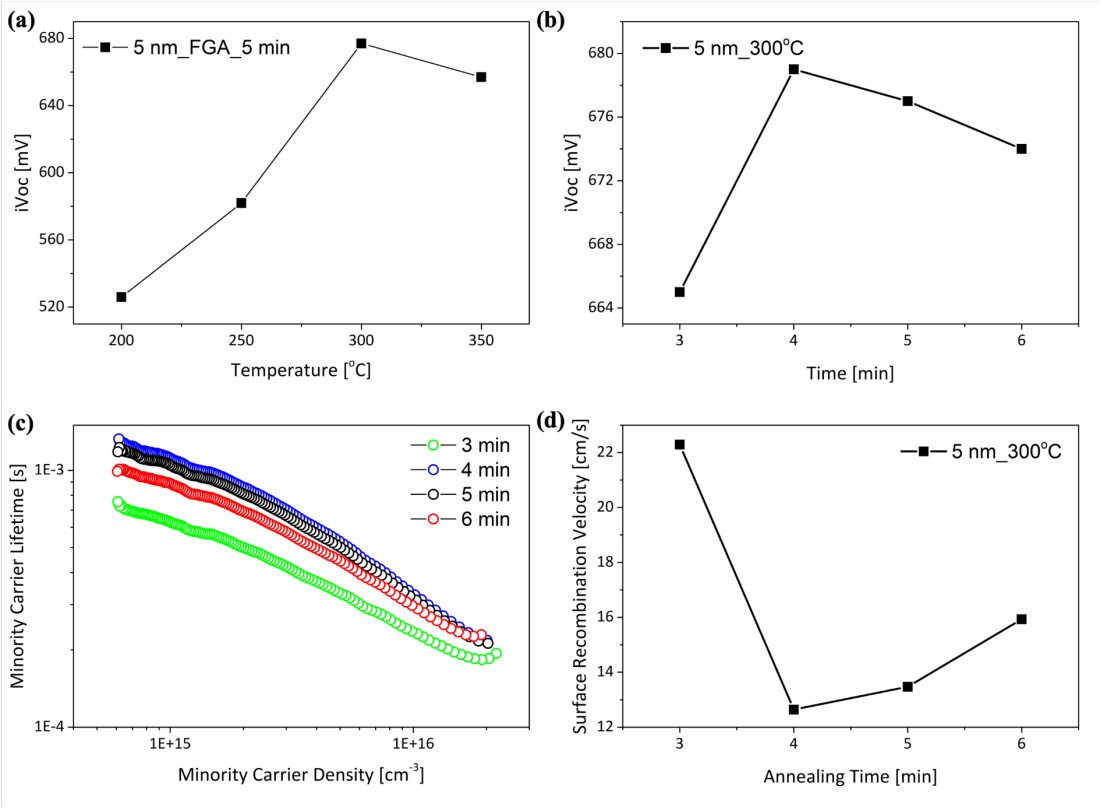

Figure 6.12 Thermal stability of 5 nm TiO_x a) iVoc as a function of temperature b) iVoc as a function of FGA time c) Effective lifetime as a function of minority carrier density when TiO_x is annealed at 300°C for 3, 4, 5 and 6 mins d) Surface recombination velocity as a function of annealing time.

The thermal stability of the as-deposited TiO_x thin film is also investigated where 5 nm TiO_x was chosen to characterize its performance under various annealing temperature and time. Figure 6.12 (a) shows the iVoc of 5 nm TiO_x after annealing at 200, 250, 300 and 350 °C for 5 minutes. One can see that as the temperature increases from 200 °C to 300 °C, the iVoc representing the surface passivation quality is improved from 526 mV to 677 mV. Further increasing the temperature to 350 °C brings down the iVoc to 657 mV. Figure 6.12 (b) shows the surface passivation quality of TiO_x where iVoc is plotted as a function of annealing time at the optimized 300 °C. A large jump in iVoc (from 665 mV to 679 mV) can be observed when the annealing period is extended from 3 minutes to 4 minutes. Further extending the annealing period gradually brings down the surface passivation quality where an iVoc of 674 mV is achieved in the case of 6-minute FGA. Figure 6.12 (c) shows the injection level dependent effective lifetime under various annealing time conditions. It is clear that 4-minute FGA results in the best effective lifetime (at the injection level of $1 \times 10^{15} cm^{-3}$) of 1107 μs which is in accordance

with Figure 6.12 (d) where the lowest surface recombination velocity of 13 cm/s is observed in the 4-minute FGA case.

The non-ideal surface passivation quality at low temperatures (200 and 250 ºC) can be attributed to the incomplete formation of Ti-O-Si bonding at the interface. Generally, the formation of Ti-O-Si bonding involves the decomposition of Ti-O bond and rebinding of Si-O bond [66]. When the temperature is not high enough, the thermal energy is not able to break the original bonding; therefore, fewer Ti-O-Si bonding are formed, leading to the degradation of surface passivation. On the other hand, when the temperature goes beyond 300 ºC and reaches 350 ºC, the decrease in iVoc can be mainly attributed to the phase transformation from amorphous to anatase. It is reported that the pure TiO_2 thin film crystalizes into anatase phase at temperatures of around 350 ºC [69]. Therefore, the formation of anatase phase under 350 ºC annealing violates the Ti-O-Si bonding and creates additional interface defects which leads to the degradation of surface passivation. Besides, the high temperature might also directly break the Ti-O-Si bonding. The same mechanism also applies to the different annealing time cases where 3-minute forming gas annealing at 300 ºC is not long enough for a complete formation of Ti-O-Si bonding at the interface, while longer FGA time (>4 mins) induces the phase transformation to anatase of part of the amorphous TiO_x, leading to the degradation of surface passivation quality.

In conclusion, for c-Si/TiO_x stack, the best passivation quality (iVoc of 677mV) is obtained with 5 nm TiO_x which was annealed in forming gas at 300 ºC for 4 minutes.

6.2.2. Surface Passivation Quality of c-Si/SiO_2/TiO_x Stack

Excellent passivation quality and thermal stability of SiO_2/doped poly-Si carrier selective stack has been widely reported [7]. Inspired by this, an ultrathin wet chemically grown SiO_2 (~1.5 nm) tunnel layer is introduced between c-Si and TiO_x thin film to enhance the thermal stability of TiO_x passivation layer. The results are shown in Figure 6.13.

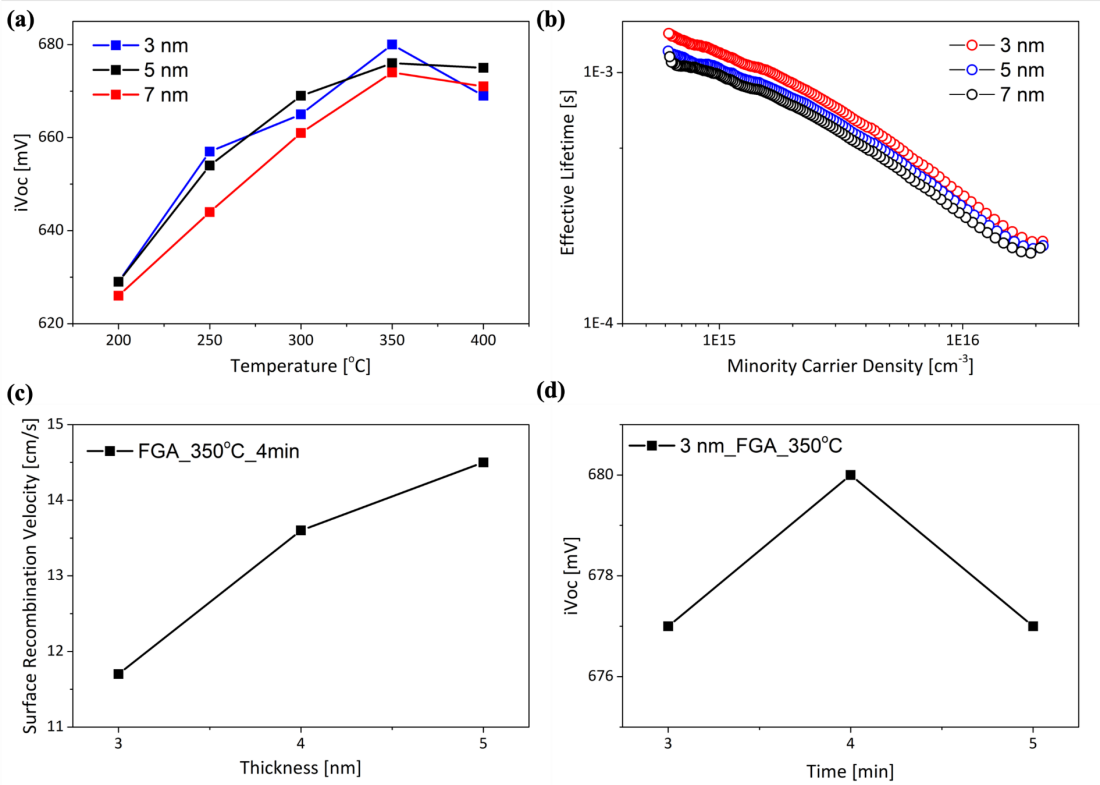

Figure 6.13 a) iVoc of SiO_2/TiO_x stack with various thickness of TiO_x capped layer after 4 minute of FGA at different temperatures b) Effective lifetime of SiO_2/TiO_x stack after 350 °C FGA where the thickness of TiO_x varies c) Surface recombination velocity of SiO_2/TiO_x stack after 350 °C FGA where the thickness of TiO_x varies d) iVoc of 3 nm TiO_x after 350 °C FGA for 3, 4, and 5 mins.

It can be seen in Figure 6.13 (a) that as the FGA temperature increases from 200 °C to 350 °C, the passivation is improved significantly in all cases of TiO_x thickness. Further increasing the annealing temperature to 400 °C leads to a degradation in surface passivation quality. The best surface passivation quality (represented by the highest iVoc) is achieved when c-Si is capped with 3 nm TiO_x layer. This result is also in accordance with Figure 6.13 (b) and (c) where the highest effective lifetime ($1195\mu s$) and lowest surface recombination velocity (12 cm/s) are both obtained in the case of 3 nm TiO_x. Figure 6.13 (d) shows the influence of annealing time on the iVoc on this champion case. It is clear that 4 minutes of FGA gives the best surface passivation quality. These results demonstrate that SiO_2/TiO_x stack can provide a good surface passivation quality on n-type c-Si. Meanwhile, the thermal stability is also improved compared to the case when c-Si surface is directly capped with TiO_x.

The difference between the passivation outcome as well as thermal stability of c-

Si/TiO_x and c-Si/SiO_2/TiO_x stack is mainly due to the different passivation mechanisms. It is already concluded that c-Si/TiO_x structure passivates the c-Si surface by the formation of Ti-O-Si bonding during FGA, while the surface passivation of SiO_2/TiO_x stack is achieved mainly by the combination of chemical passivation of SiO_2 and field effect passivation of TiO_x [7]. During FGA, the atomic hydrogen diffuses to the c-Si/SiO_2 interface to terminate the dangling bonds which enhances the chemical passivation of SiO_2; meanwhile, as-deposited TiO_x thin film is also activated by thermal energy which leads to a better field effect. It is reported that higher FGA temperature results in lower surface recombination velocity at the c-Si/SiO_2 interface [70]. Therefore, the improved surface passivation at 350 °C can be mainly attributed to the enhanced chemical passivation of SiO_2. The degradation in passivation at 400 °C can be resulted from the phase transformation of TiO_x from amorphous to anatase which reduces the field effect. The trade-off between chemical passivation of SiO_2 and field effect of TiO_x as a function of FGA temperature determines the final overall passivation quality. On the other hand, thicker TiO_2 tends to transform to anatase phase under the same annealing condition due to the higher compressive stress within the thin film. Therefore, the degradation in surface passivation of SiO_2 with thicker TiO_x layer can be attributed to the easier phase transformation induced field effect loss of TiO_x. The same mechanism applies to the passivation difference under various annealing time where 3-minute annealing is not long enough to fully activate the field effect of TiO_x while 5-minute annealing causes the phase transformation of TiO_x.

In conclusion, SiO_2/TiO_2 can provide good surface passivation and better thermal stability due to the cooperation of chemical passivation and field effect provided by SiO_2 and TiO_x respectively. The best passivation outcome is found in the case with 3 nm capped TiO_x after 350 °C for 4 minutes.

6.2.3. Influence of TiO_2 Source on the Passivation of c-Si/TiO_x Structure

E-beam evaporation is a popular method to deposit many dielectric thin films. However, the reproducibility and stability of E-beam prepared samples are sometimes unsatisfactory especially for the materials that can exist in a number of different stoichiometric forms such as TiO_x. It has been reported that the critical deposition parameters for obtaining a high quality of TiO_x film are the stoichiometry of the source

material, oxygen partial pressure during deposition, substrate temperature and deposition rate [71].

A number of source materials (TiO, Ti_2O_3, TiO_2) can be used to deposit TiO_x. In general, the material with higher O/Ti ratio results in greater packing density, which enables the film to be more thermally and humidly stable and gives better film quality. In this project, only TiO_x source (labelled TiO_2) was used. The oxidation degree of source material can be estimated with naked eyes because fully oxidized TiO_2 is white while the source being used shows greyish color due to the reduction of oxygen [72].

Oxygen partial pressure also plays an important role in the deposition of TiO_x films. The direct E-beam evaporation of TiO_x under vacuum will cause the decomposition and thermal dissociation of source material which affects the stoichiometry of the as-deposited layer [71][73]. Introducing controlled amount of oxygen during deposition can more or less prevent the film from non-stoichiometry.

Another important parameter is the substrate temperature. It has been found that depositing at higher substrate temperature tends to give higher thin film density and enhanced electrical properties. Besides, the phase of the as-deposited TiO_x is also determined by the substrate temperature where depositing at room temperature results in amorphous structure while increasing the substrate temperature causes the phase transformation to anatase [68].

Deposition rate also determines the quality of E-beam deposited TiO_x. When the deposition rate is too high, a porous film is more likely to be deposited. In this subsection, due to the limited function of PVD equipment, only the influence of PVD TiO_2 source on the passivation quality of its resulted film is investigated. Therefore, for each round of deposition, the substrate temperature is kept at room temperature, and the TiO_x layer is deposited at a deposition rate of 0.02 nm/s without oxygen partial pressure supply.

The TiO_x source material investigated in this project can be classified into 3 groups: 1) The original source which has been kept in the chamber for a couple of years and experienced a few E-beam evaporations; 2) The refilled source which is composed of equal proportion of original source and new TiO_x flakes; 3) The new source which is made up of fresh pure TiO_x flakes. Meanwhile, sources from class 2 and 3 also experienced a calibration process which is referred to a complete melting process by E-beam evaporation at a deposition rate of 0.2 nm/s.

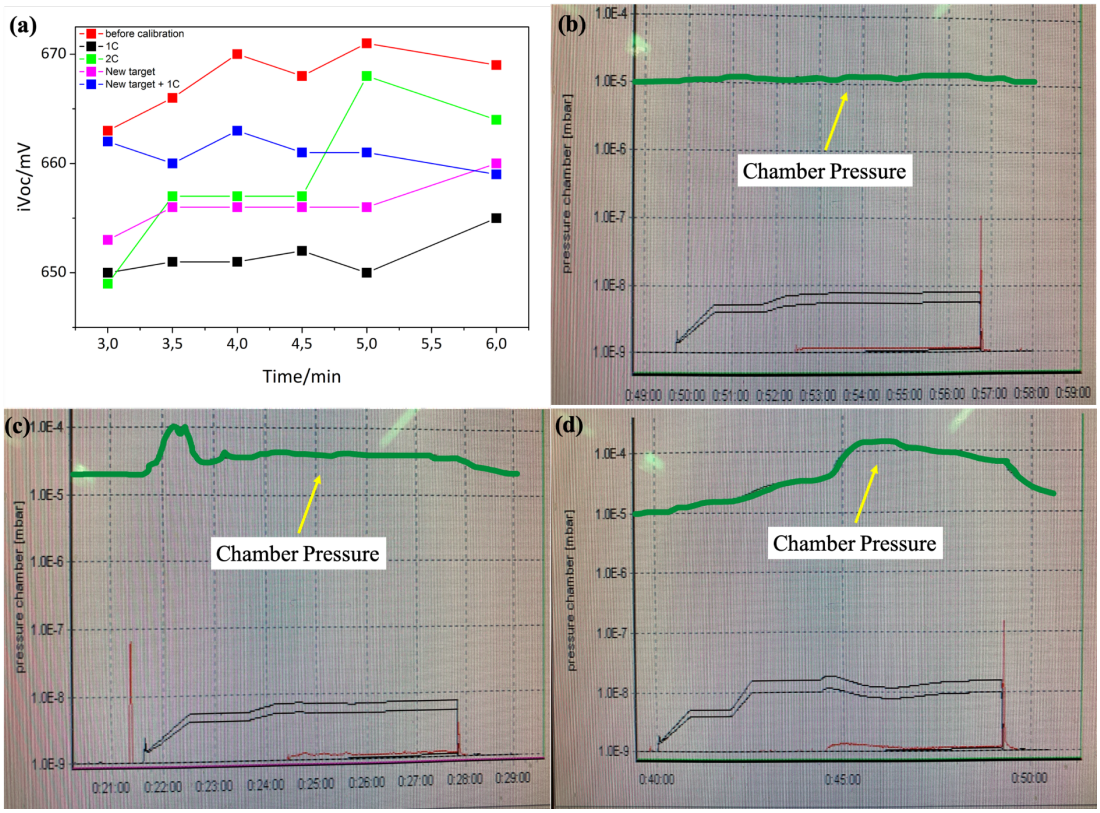

Figure 6.14 Electrical and optical performance of TiO_x layer a) iVoc of old and new TiO_2 source after 300 °C FGA for different period where 1C/2C represents once/twice calibration respectively. b) Chamber pressure during deposition when using the original source c) Chamber pressure during deposition when using the refilled source d) Chamber pressure during deposition when using the new source.

The excellent passivation quality provided by the original TiO_2 source is already discussed in the previous sections. The original half-full crucible was refilled with fresh TiO_2 material, and the same symmetric test on c-Si/TiO_x structure was performed. In Figure 6.14 (a), the red curve represents the iVoc of TiO_x which was directly evaporated by E-beam on the substrate after source refilling. One can notice that the iVoc sees an decrease by 10 mV compared to the original case, and its variation as a function of annealing time also differs. The black and green curves represent the iVoc of TiO_x after one and two times of source calibration respectively. It is interesting to see that after the first source calibration, the iVoc drops dramatically by ~30 mV compared to the original case. After the second source calibration, the iVoc is increased but the passivation quality is very unstable and the curve resembles neither the original case nor other calibration cases. The plum curve shows the iVoc of a completely new TiO_x pocket source and the blue curve represents the case when the new source was

calibrated. One can see that the passivation quality of the new TiO_x source is still non-ideal but it is relatively more stable.

The degradation in surface passivation quality by using different TiO_x sources can be mainly attributed to the non-stable vacuum pressure during deposition due to the outgassing of fresh TiO_x source which results in a non-uniform as-deposited layer with high roughness. When depositing TiO_x with E-beam evaporation method, the source material reaches an equilibrium with the background after some rounds of evaporation or being melted for some time [74]. The source with high Ti/O ratio such as TiO needs to take up oxygen from the ambient, while TiO_2 must release oxygen until they reach Ti_3O_5 which is reported to be the equilibrium state [75]. Figure 6.14 (b), (c) and (d) show the vacuum pressure during deposition of original source, refilled source and new source respectively. It is obvious that in the case of original source, the vacuum pressure is nearly constant throughout the deposition. This indicates that the TiO_x source is in equilibrium and nearly no outgassing occurs during deposition. Thus, the long mean free path for evaporated TiO_x leads to a uniform coating on the substrate. By contrast, one can see a significant vacuum pressure change in both refilled source case and new source case. Such high fluctuation in pressure indicates that significant outgassing is taking place during deposition due to the decomposition of source material. The liberated oxygen atoms collide with TiO_x vapor and reduces its free mean path, resulting in an inhomogeneous coating on the substrate. The non-ideal film uniformity generates additional defects and nucleation after FGA and degrades the passivation quality.

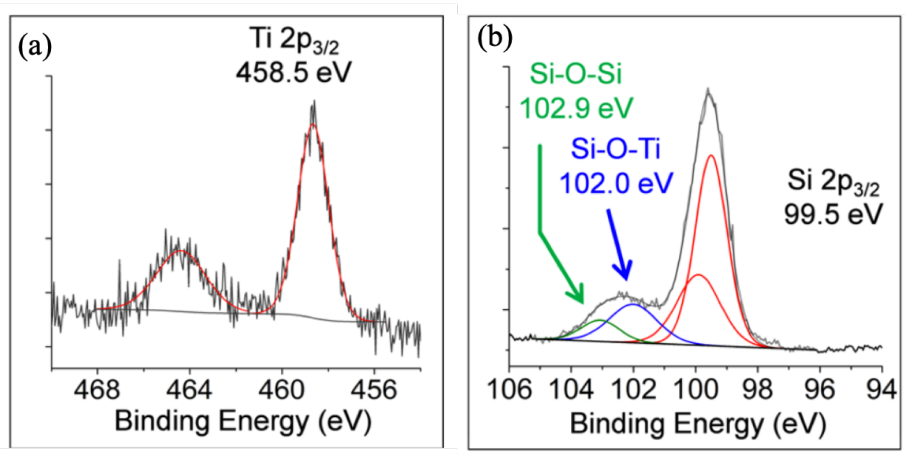

Figure 6.15 Standard XPS results for TiO_2/c-Si interface after 250ºC atmospheric annealing [66]

To investigate the stoichiometry and optical performance of the TiO_x layer deposited from different source materials, the chemical compositions and the optical constants are also characterized by means of XPS and Ellipsometry respectively. Figure 6.15 shows the standard XPS results for TiO_2, Si-O-Si and Si-O-Ti bonds. The standard binding energy for Ti^{4+} is found at 458.5 eV, and that for Si-O-Si and Si-O-Ti bonds are marked at 102.9 eV and 102.0 eV respectively. By locating these binding energies, one can readily analyze the bonding scenario at the TiO_x/c-Si interface.

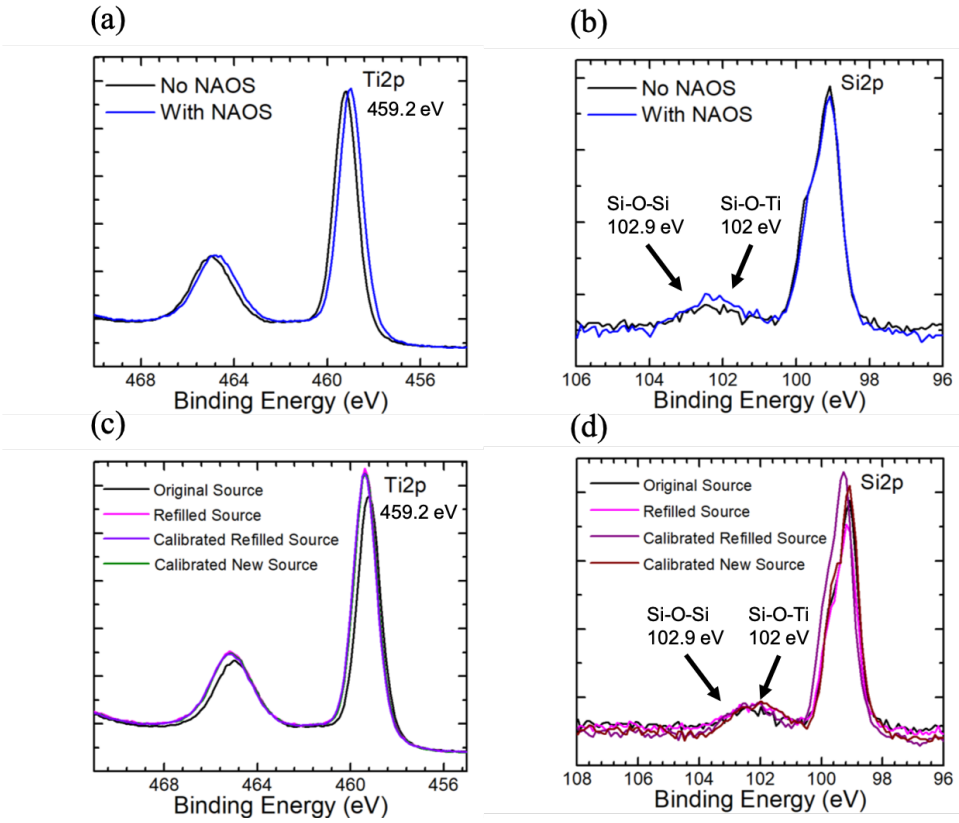

Figure 6.16 a,b) XPS results of c-Si/TiO_x (indicated by black curve) and c-Si/NAOS-SiO_2/TiO_x (indicated by blue curve) stack after 300 ºC and 350 ºC FGA for 4 minutes respectively; c,d) XPS result of c-Si/TiO_x stack with different TiO_x sources after 300 ºC FGA for 4 minutes

Figure 6.16 (a) and (b) show the XPS result of c-Si/TiO_x and c-Si/SiO_2/TiO_x under optimized FGA conditions. It can be seen from Figure 6.16 (a) that both cases see a peak at around 458.5 eV, indicating the successful deposition of TiO_x layer by E-beam evaporation on the substrate. Figure 6.16 (b) demonstrates that both Si-O-Si (peaks at 102.9 eV) and Si-O-Ti (peaks at 102 eV) bonds are present at the c-Si/TiO_x interface. It is interesting to notice that the location and intensity of those two peaks are nearly

the same, indicating a similar bonding scenario at the c-Si/TiO_x interface after FGA.

Figure 6.16 (c) and (d) show the XPS result of c-Si/TiO_x stack after 300 °C FGA for 4 minutes where different TiO_x sources are used. Apparently, the stoichiometry of TiO_x deposited from different source materials is nearly the same which can be demonstrated by Figure 6.16 (c) where all curves peak at around 459.2 eV. Meanwhile, it is also worth noting that all cases are seeing both Si-O-Si and Si-O-Ti peaks in Figure 6.16 (d), and the shapes resemble one another. This means that the bonding scenario at c-Si/TiO_x interface is independent with the source material. This result is also in accordance with the optical constants where all TiO_x layers are showing identical n, k and absorption coefficient values. Therefore, it can be concluded that the stoichiometry of TiO_x layer deposited from different sources is constant, and the bonding scenario at c-Si/TiO_x is independent from SiO_2 interlayer and source material.

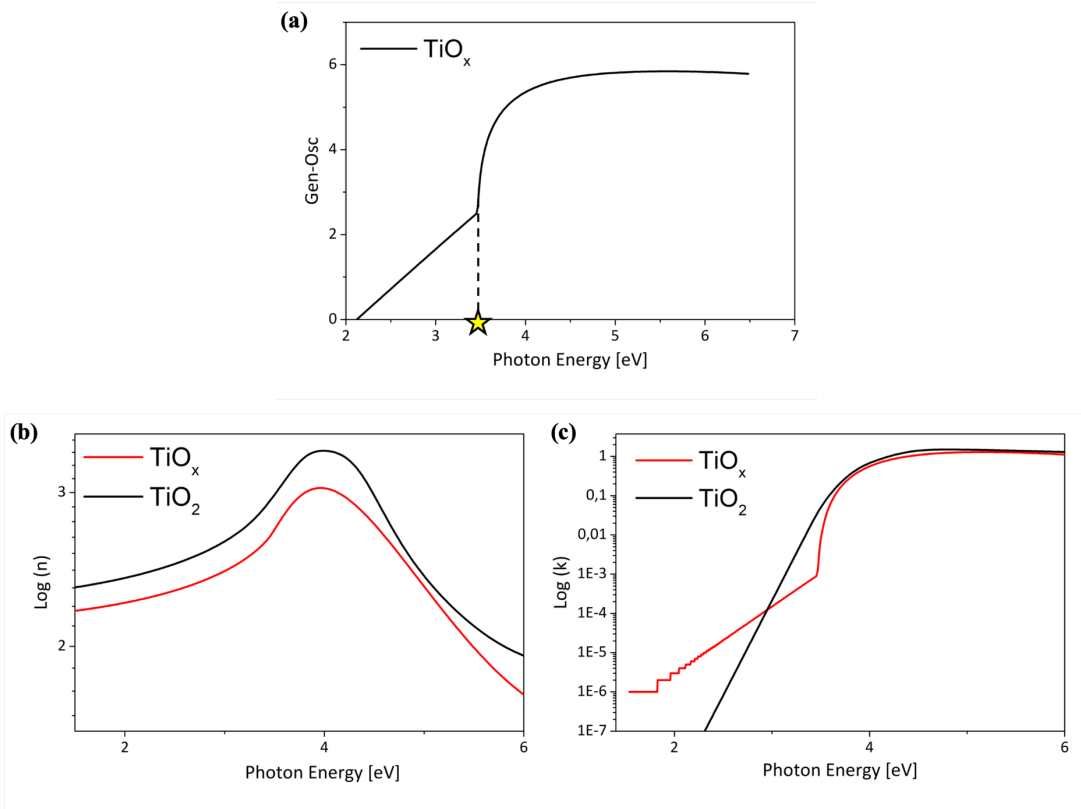

Figure 6.17 a) Absorption coefficients of TiO_x layer b) Refractive index of TiO_x layer c) Extinction coefficient of TiO_x layer after 350 °C FGA for 4 minute.

Figure 6.17 (a) shows the absorption coefficient of TiO_x layer after 300 °C FGA for 4 minutes. The absorption coefficient represents the penetration depth of the light with

a particular wavelength before it is absorbed by the material. Semiconductor materials are featured with a step in the absorption coefficient because the photons with energy smaller than the band gap are not able to stimulate the electrons from valence band to the conduction band. Therefore, by extrapolating the 'step' region to the X-axis, one can determine the optical band gap of the semiconductor material [76]. In Figure 6.17 (a), the intercept is denoted by the star and the optical band gap of TiO_x layer is estimated to be 3.45 eV which is larger than the standard TiO_2 band gap of 3.2 eV [77]. This band gap shift might be caused by the non-stoichiometry of the TiO_x layer. Figure 6.17 (b) shows the n values of TiO_x layer. It is obvious that the refractive index of TiO_x is constantly lower than the standard TiO_2 thin film which can be mainly attributed to the oxygen deficiency in TiO_x layer [68]. As is mentioned before, FGA enables the formation of Ti-O-Si bonds at the c-Si/TiO_x interface. This consumption of oxygen results in a oxygen deficient TiO_x layer, and the absence of oxygen causes the optical loss. Figure 6.17 (c) shows the k values of TiO_x layer where a greater absorption at small wavelength is observed compared to that of the standard TiO_2. This result demonstrates that defect states exist within the band gap which enables the electrons to be excited to the conduction band by receiving the photon energy that is lower than the band gap. These defect states are mainly associated with the reduction in O/Ti ratio in the sub-surface region [78]. Here, the formation of Ti-O-Si bonds is responsible for the deficiency of oxygen in TiO_x layer.

Due to the passivation degradation caused by TiO_x source material, symmetric test based on c-Si/TiO_x and c-Si/SiO_2/TiO_x structures are performed again to determine the optimal processing conditions.

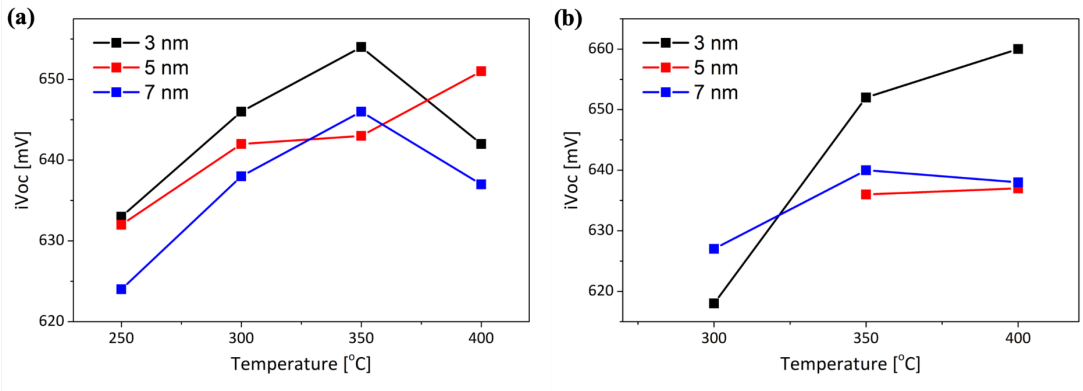

Figure 6.18 Symmetric test of new TiO_x source showing iVoc of a) c-Si/TiO_x b) c-Si/SiO_2/TiO_x stack

It can be seen from Figure 6.18 that for both c-Si/TiO_x and c-Si/SiO_2/TiO_x stacks, the optimal TiO_x thickness is 3 nm, and the optimal annealing temperatures are 350 °C and 400 °C respectively. Therefore, the following experiments are performed based on these optimal processing conditions.

6.2.4. Surface Passivation Quality of c-Si/(i)a-Si:H/TiO_x Stack

Inspired by the excellent surface passivation provided by (i)a-Si:H [79], a thin layer of (i)a-Si:H is introduced as the interfacial passivation layer between c-Si and TiO_x. The influence of such i-layer on the passivation quality is investigated by symmetric test where i-layer of different thickness (2, 4, 6, 8 nm) is capped with 4 nm of TiO_x, and the results are shown below. Here, 4 nm of TiO_x is used because this symmetric test was performed after the TiO_x thickness test on the cell level (discussed in Section 6.2.6) where FBC solar cell based on 4 nm of TiO_x is showing the best performance.

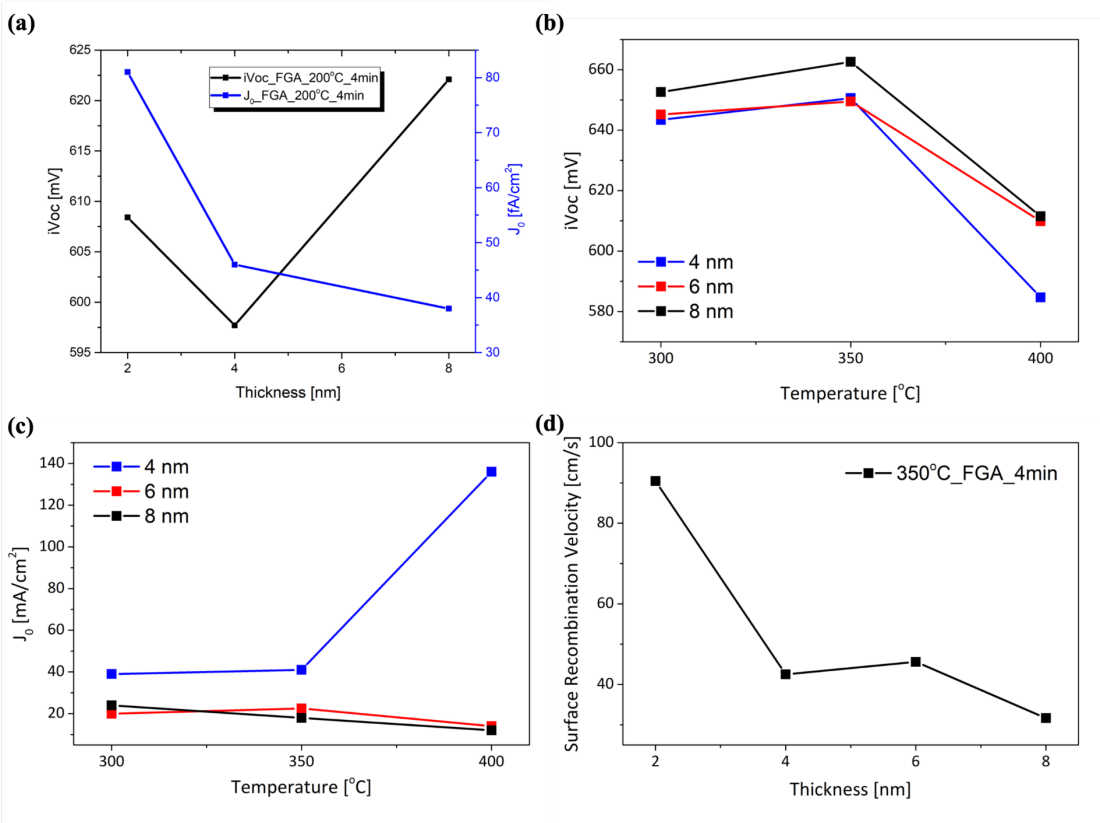

Figure 6.19 Symmetric test results of c-Si/(i)a-Si:H/TiO_2 stack a) iVoc and J_0 of 2, 4 and 8 nm interface i-layer after 200°C FGA for 4 mins; b) iVoc of 2, 4, 6 and 8 nm interface i-layer after 300, 350, and 400°C FGA for 4 mins c) J_0 of 2, 4, 6 and 8 nm interface i-layer after 350°C FGA for 4 mins d) Surface recombination velocity of 2, 4, 6 and 8 nm i-layer after 350°C FGA for 4 mins

It is already mentioned that the higher annealing temperature will cause the effusion of H atoms from the (i)a-Si:H layer and degrade the passivation quality. Therefore, the threshold FGA temperature of 200 °C for i-layer is first performed and the passivation outcome is shown in Figure 6.19 (a). One can see that the overall passivation quality under 200 °C FGA for various i-layer thickness is not excellent. As the thickness increases from 2 to 8 nm, the iVoc decreases first then jumps to 622 mV while the saturation current density J_0 sees a continuous decrease and ends up with 38 fA/cm^2 in the case of 8 nm interfacial i-layer. The improved passivation quality as the i-layer thickness increases can be attributed to the better dangling bonds deactivation at the c-Si/i-layer interface. During FGA, part of the (i)a-Si:H reacts with TiO_x. The consumption of i-layer causes the out-diffusion of hydrogen atoms and violates the Si-H bonding at the c-Si/i-layer interface. Therefore, additional dangling bonds are created which degrades the surface passivation quality. As the thickness of i-layer increases, the effect of hydrogen out-diffusion is less critical and the Si-H bonds are mostly preserved, leading to a better surface passivation quality. It is also interesting to notice that J_0 is nearly stable when i-layer thickness increases over 4 nm. This phenomenon indicates that the amount of i-layer consumed by TiO_x under specific annealing condition is almost constant, thus, further increasing i-layer thickness does not proportionally improve the passivation quality. The drop of iVoc at 4 nm case might be an experimental error. Moreover, the overall degradation in iVoc can be mainly resulted from the non-ideal field effect formation of TiO_x under low temperature FGA.

To investigate the thermal stability of as-deposited i-layer, the passivation quality under higher FGA temperature is also tested. Figure 6.19 (b) shows the iVoc of such structure under various FGA temperatures (300, 350, 400 °C) for 4 minutes with the thickness of i-layer being 4, 6, and 8 nm. It is clear that all cases are following the same trend: iVoc first sees an increase when the FGA temperature is raised to 350 °C while further increasing the temperature to 400 °C brings down the iVoc. Figure 6.19 (c) correspondingly shows the J_0 in each case. One can see that the J_0 for 6 and 8 nm cases stabilizes at ~20 fA/cm^2 within the chosen temperature range. The iVoc for 4 nm case starts at ~40 fA/cm^2 and jumps to 136 fA/cm^2 when the FGA temperature reaches 400 °C. These results demonstrate that 6 and 8 nm interfacial i-layers are thermally stable during FGA and the effusion of H atoms under high temperature barely happens. 4 nm case, by contrast, is only thermally stable below 350 °C and the effusion of H atoms at

the interface cannot be balanced by the hydrogen in forming gas when the FGA temperature reaches 400 °C. On the other hand, the improvement in surface passivation at 350 °C can be mainly attributed to the enhanced field effect of TiO_x layer which is in accordance with the previous discussion. However, further increasing the FGA temperature to 400 °C results in the phase transformation of TiO_x which damages the field effect, and in turn reduces the passivation quality. It can be concluded that such degradation is mainly caused by the phase-transformation induced field effect reduction because J_0 remains almost unchanged under 400 °C FGA.

Figure 6.19 (d) shows the surface recombination velocity of various thickness of i-layer cases after 350 °C FGA for 4 minutes. Apparently, 2 nm case shows the highest surface recombination velocity due to additional dangling bonds introduced by broken Ti-H bonds, while 8 nm case offers the best surface passivation quality with the lowest of surface recombination velocity of 32 cm/s.

6.2.5. Influence of Metallization on TiO_x Based FBC Solar Cells

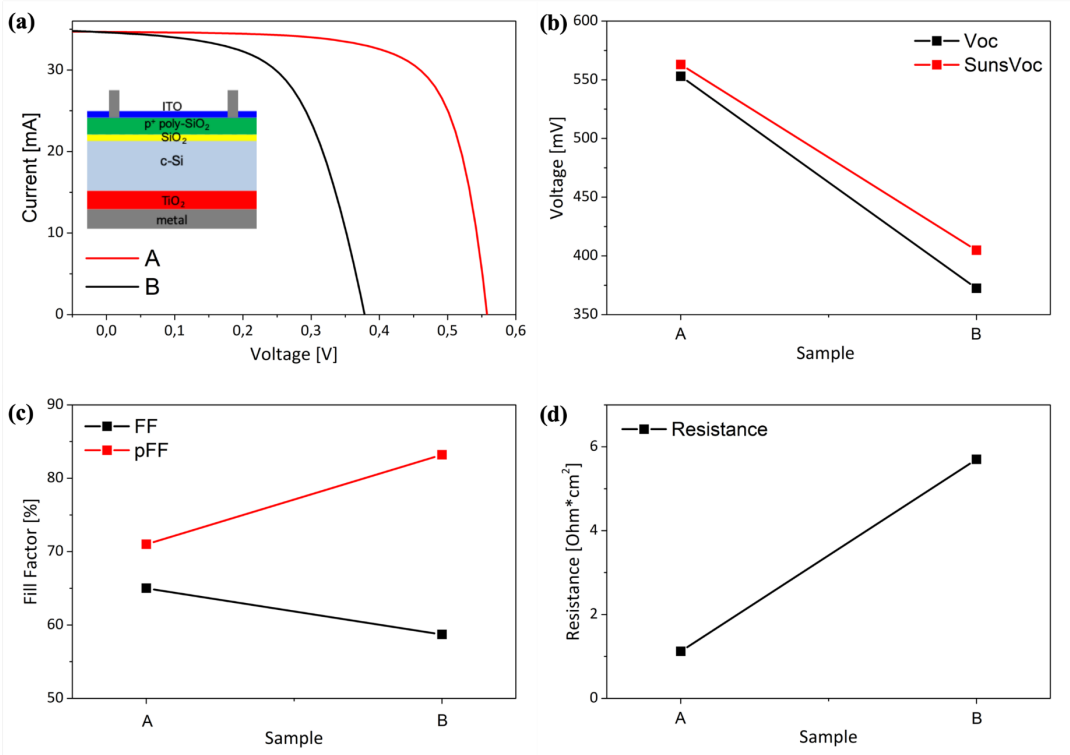

Figure 6.20 a) I-V curves of FBC solar cells with inserted cell structure where metallization was performed before (curve denoted by A) and after FGA (curve denoted by B) respectively b) Voc and SunsVoc of FBC solar cells c) FF and pFF of FBC solar cells d) Resistance of FBC solar cells

To investigate the carrier selectivity of TiO_x, FBC solar cells were fabricated with p^+ poly-silicon as the front side and 3 nm of TiO_x as the electron selective layer. First, the influence of metallization on the performance of solar cell was tested, where the TiO_x rear side was deposited with Aluminum either before or after FGA. Detailed process steps are explicitly listed in Table 6.4, and the measurement results are plotted and shown in Figure 6.20.

Table 6.4 Precursor and process steps of TiOx based electron selective region

Process Steps	TiO_x Layer	Al Layer	FGA	Al Layer
Sample A	X	X	X	
Sample B	X		X	X

Figure 6.20 (a) shows the I-V curves of FBC solar cells where metallization was performed before and after FGA respectively. Obviously, sample A gives much higher open circuit voltage (553 mV) than sample B (372 mV). By looking at the slope in the vicinity of both Voc and Isc, one can surmise that sample A shows lower series resistance and higher shunt resistance. Figure 6.20 (b) compares the Voc and SunsVoc of both Cell A and B, and it is clear that for both cases, SunsVoc is slightly higher than Voc which is due to the fact that the measurement of SunsVoc is free of series resistance related effects. Meanwhile, the voltage difference in Cell B is larger than that in Cell A, indicating a larger series resistance in Cell B. This is also consistent with the results shown in Figure 6.20 (c) where Cell B sees a larger difference between FF and pFF. According to Equation (52), the series resistance for both Cell A and B is calculated and plotted in Figure 6.20 (d). As expected, Cell B is subject to a much higher series resistance (5.12 $[\Omega \cdot cm^2]$) than Cell A (1.31 $[\Omega \cdot cm^2]$).

The much lower open-circuit voltage seen by Cell A can be mainly attributed to the non-ideal contact at the TiO_x/Al interface. The abrupt transition at the interface significantly increases the contact resistance, therefore, electrons cannot easily be collected. Instead, they recombine rapidly with the holes trapped in the defect states of TiO_x. Such poor carrier selectivity results in the degradation in Voc. On the other hand, the reduction in series resistance when coating the TiO_x with Al before FGA can be mainly attributed to two aspects. First, the post-FGA after TiO_x/Al junction formation relaxes both the TiO_x and Al films, thus, the abrupt transition at the TiO_x/Al interface

is minimized and a better contact results in a higher conductivity. Second, it has been widely reported that TiO_x shows higher conductivity when the concentration of oxygen deficiencies increases [80]. Due to the high oxygen affinity of Al, the oxygen atoms in the TiO_x film tend to diffuse to the TiO_x/Al interface and an ultrathin layer of AlO_x is formed during the FGA process. Such AlO_x layer is supposed to be highly conductive because of the low resistance obtained in Cell A. The formation of AlO_x leaves high concentration of oxygen vacancies in TiO_x which increases the conductivity. Therefore, the reduced contact resistance enables a better collection of electrons which significantly improves the Voc. The higher FF and smaller difference between FF and pFF in cell A can also be attributed to the reduced series resistance after the formation of highly oxygen-deficient TiO_x layer. Based on this conclusion, the following FBC solar cells were all fabricated with FGA after metallization.

6.2.6. Influence of TiO_x thickness on the TiO_x based FBC Solar Cells

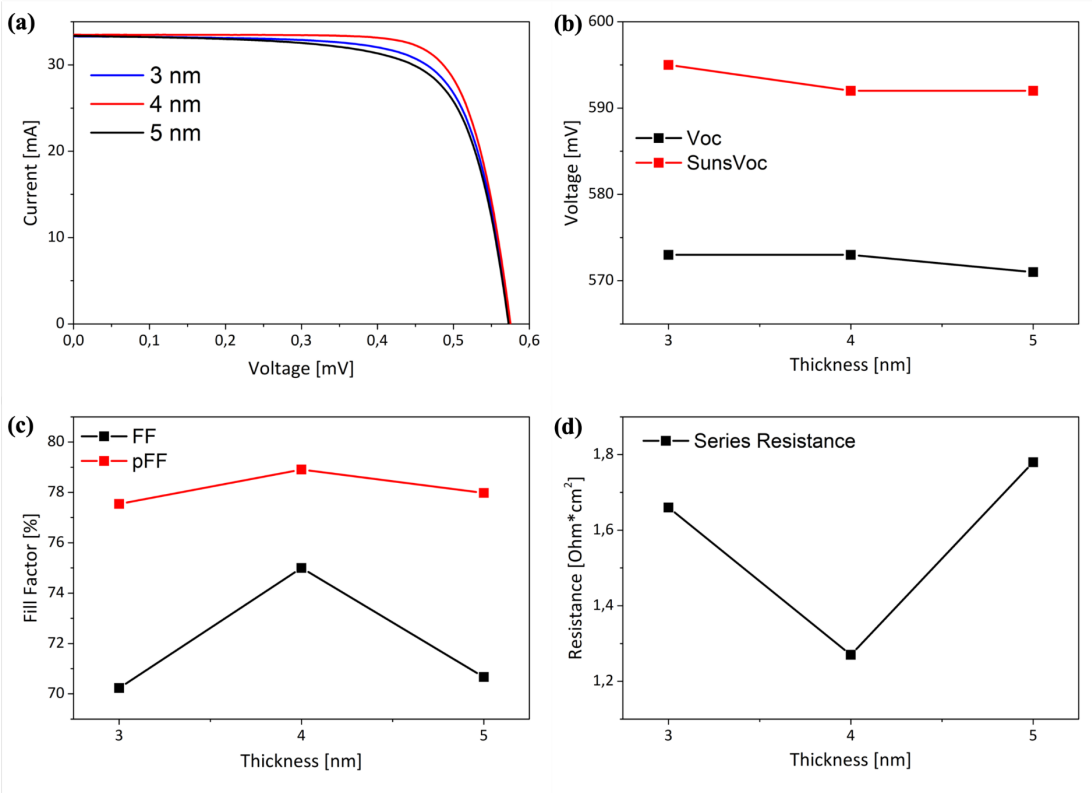

Figure 6.21 Results of FBC solar cells where the rear side is based on TiO_x with different thickness (3, 4 and 5 nm respectively) and the front side is featured with p^+ poly-SiO_x a) I-V curves b) Voc and SunsVoc c) FF and pFF d) Series Resistance

Since FGA after metallization consumes oxygen in TiO_x layer, and this oxygen deficient layer might have changed its field effect. Therefore, the optimal thickness of TiO_x at cell level might have slight difference with the outcome from symmetric test. In this section, the optimal TiO_x thickness in FBC solar cell is determined.

From Figure 6.21 (a), one can see that the thickness of TiO_x has almost no influence on the passivation quality since the Voc for all cells are nearly the same. To be more specific, it is shown in Figure 6.21 (b) that the Voc for all TiO_x thickness cases remains in the vicinity of ~573 mV but the SunsVoc sees a difference of ~20 mV. Figure 6.21 (c) compares the FF and pFF and it is clear that 4 nm TiO_x case shows the smallest series resistance. This result is consistent with the calculation plotted in Figure 6.21 (d) where 3 nm and 5 nm cases are subject to similar series resistance (~1.7 $[\Omega \cdot cm^2]$) while in the case of 4 nm, the series resistance is reduced to 1.2 $[\Omega \cdot cm^2]$.

The high series resistance found in 3 nm and 5 nm cases can be mainly attributed to the trade-off between field effect and series resistance associated with TiO_x thickness. It is known that thinner TiO_x layer is bound to give lower tunneling resistance due to its insulating nature. However, TiO_x of small thickness is also subject to weaker field effect. In the case of 3 nm TiO_x, the out-diffusion of oxygen during FGA to both c-Si/TiO_x and TiO_x/Al interfaces reduces the effective region of TiO_x, which in turn lowers the field effect. Therefore, the impaired field effect is not able to offer enough energy for electrons to tunnel through, leading to the increase of series resistance. On the other hand, the field effect in the case of 5 nm is better preserved but the increase in TiO_x thickness significantly brings up the tunneling resistance, leading to the increase of series resistance. It can be concluded that when the TiO_x thickness is lower than 4 nm, the field effect plays a dominate role in determining the series resistance of ETL region. As the thickness goes beyond 4 nm, the tunneling resistance starts to take over the determination of overall series resistance of ETL region. Therefore, 4 nm TiO_x is selected as the optimal thickness for the flowing experiments.

6.2.7. Influence of Interfacial Layers on TiO_x based FBC Solar Cells

In order to investigate the passivation improvement of interfacial layers on the cell level, the rear side was fabricated in a number of structures as listed in Table 6.5.

Table 6.5 Rear side structure and film thickness

Number	Structure and Thickness
1	Ti (1 nm) / TiO_2 (4 nm)
2	SiO_2 (1.5 nm) / TiO_2 (4 nm)
3	(i) a-Si:H (6 nm) / TiO_2 (4 nm)
4	(i) a-Si:H (8 nm) / TiO_2 (4 nm)

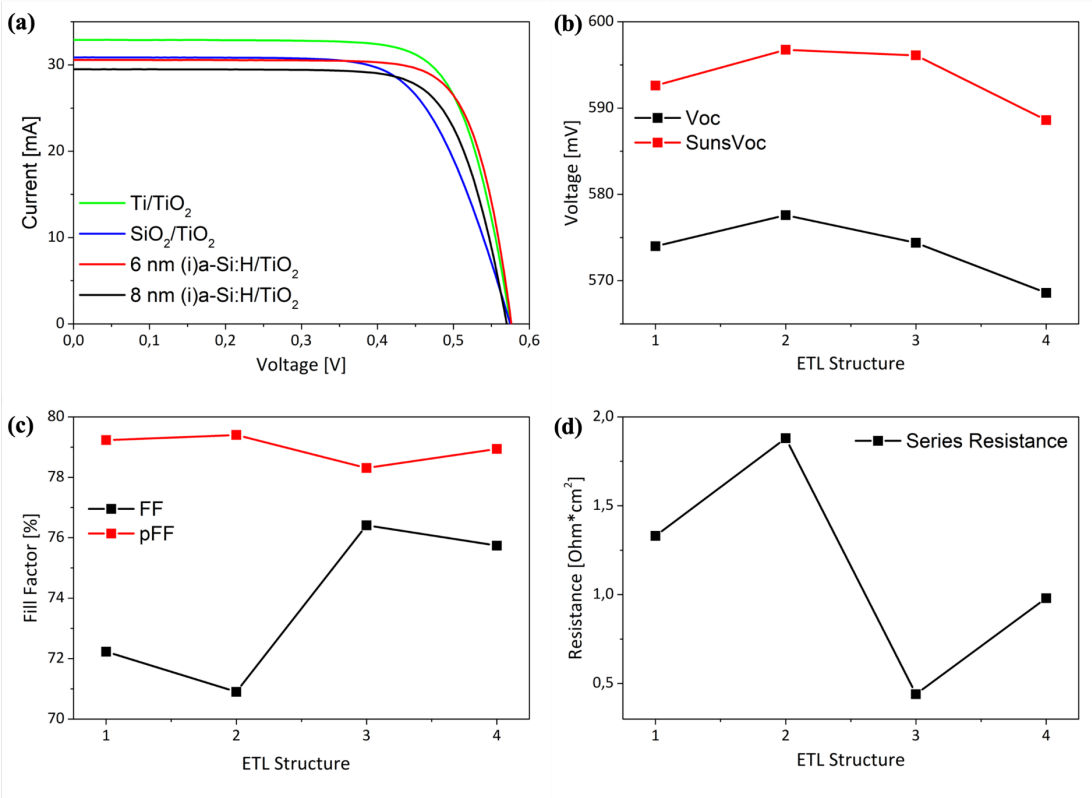

Figure 6.22 a) I-V curves of FBC cells b) Voc and SunsVoc of FBC cells c) FF and pFF of FBC cells d) Series resistance of FBC cells where the rear side is fabricated with different structures

Figure 6.22 (a) shows the I-V curves of the FBC solar cells whose rear side is fabricated with different structures. One can see that all cells show a high shunt resistance but also a high series resistance, and the open-circuit voltages are nearly the same. Figure 6.22 (b) compares the Voc and SunsVoc of all cells. Obviously, SiO_2/TiO_x stack shows the best passivation quality and there is a constant ~20 mV difference between Voc and SunsVoc for all cells. Figure 6.22 (c) compares the FF and pFF, and it can be seen that sample 2 and 3 show the largest and smallest difference between FF and pFF respectively. This indicates that the series resistance in sample 2 is the highest

while that in sample 3 is the lowest which is consistent with the series resistance calculations plotted in Figure 6.22 (d).

The highest Voc in sample 2 can be mainly attributed to the better surface passivation quality provided by wet-chemically grown SiO_2. However, the insulating nature of SiO_2 also introduces high series resistance, leading to the highest series resistance of ~1.9 [$\Omega \cdot cm^2$]. By contrast, sample 2 shows a similar Voc but lower series resistance. This can be mainly resulted from the thinner SiO_x formed during FGA. It has been reported that an ultrathin layer of SiO_x (~1.2 nm) is generated at the c-Si/TiO_x interface during FGA [7]. The formation of Ti-O-Si bonds deactivate the dangling bonds at the c-Si surface and significantly reduces the surface recombination velocity. When 1 nm Ti layer is introduced at the interface, the diffused oxygen from TiO_x during FGA is partially consumed by the ultrathin Ti layer, forming a highly oxygen-deficient TiO_x. The residual oxygen diffuses to the c-Si surface and generates Ti-O-Si bonds, but in this case, the thickness of SiO_x layer is much thinner due to the consumption of oxygen in Ti layer. The results shown in Figure 6.22 demonstrate that this structure can still provide similar surface passivation compared to SiO_2/TiO_x stack but the series resistance is reduced due to the thinner SiO_x. Interestingly, the introduction of intrinsic a-Si:H layer significantly brings down the series resistance. The reason behind might because there is few SiO_x formed at the (i)a-Si:H/TiO_x interface, therefore, no additional series resistance is introduced. However, as a semiconductor, increasing the thickness of i-layer will also raise the series resistance which is consistent with the results shown in Figure 6.22 where 8 nm i-layer shows higher series resistance than 6 nm i-layer case. Besides, it is also observed that Voc is slightly reduced in i-layer cases. This might be resulted from the thick i-layer which impairs the field effect offered by TiO_x. The electric field responsible for selectively collect the carriers cannot penetrates the i-layer, thus, the band bending at the c-Si surface is significantly lowered which damages the carrier selectivity. Thicker i-layer causes stronger degradation on the field effect which is consistent with the results that 8 nm i-layer shows lower Voc than 6 nm i-layer case. However, sample 1 and 2 with better field effect do not show significant Voc improvement. This can be mainly attributed to two aspects. On one hand, the work function of Al is close to that of c-Si, thus, the band bending caused by TiO_x at c-Si/TiO_x interface is more or less reduced after metallization, leading to degraded carrier selectivity. The holes cannot be effectively repelled from the c-Si surface, therefore,

significant recombination of electron-hole pairs occurs which results in low Voc. On the other hand, the oxygen out-diffusion during FGA generates a number of defect states within the band gap. These defect states facilitate the recombination of electron-hole pairs, leading to a non-ideal overall passivation quality.

In summary, the external parameters of FBC solar cells based on various rear side architectures are listed in Table 6.6. It is obvious that the passivation quality (represented by Voc) for each structure is almost unchanged, and the difference in other external parameters is mainly caused by the series resistance featured in each structure. It can be concluded that the E-beam evaporated TiO_x is not favorable for working as ETL due to the substantial defect densities within the band gap which significantly degrades the passivation quality when Al metal contact is made.

Table 6.6 External parameters of FBC cells where rear side is based on various TiO_x structures

Structure	**V_{oc} [mV]**	**J_{sc} [mA/cm^2]**	**FF [%]**	**PCE [%]**
c-Si/TiO_x	573	30.53	74.97	14.21
c-Si/SiO_2/TiO_x	577	30.78	70.09	12.48
c-Si/Ti/TiO_x	574	33.17	72.23	13.64
c-Si/(i)a-Si:H (6nm) /TiO_x	574	30.11	76.41	13.22
c-Si/(i)a-Si:H (8nm) /TiO_x	568	27.61	75.74	11.88

7. Conclusion and Outlook

In this chapter, the core achievements of this master thesis project are summarized. Also, an outlook for future improvement on transition metal oxides (MoO_x and TiO_x) integrated solar cells is given.

7.1. MoO_x Based Heterojunction Solar Cells

This project deals with the optimization of passivation property of MoO_x based HTL and TiO_x based ETL and demonstrates their performance on device level.The performance of (i)a-Si:H/MoO_x working as a hole selective contact can be concluded as follows:

1) The large iVoc (~715 mV) after individual deposition of (i)a-Si:H, MoO_x and ITO indicates an excellent surface passivation property, and the fabrication of as-deposited stack structure do not influence the passivation quality. By contrast, the low Voc (632 mV) and SunsVoc (652 mV) measured after metallization indicate an non-ideal carrier selectivity of MoO_x. This can by mainly attributed to the reduced surface field induced by ITO which has a similar work function to c-Si. Therefore, the reduced field effect cannot effectively extract the holes from the bulk and simultaneously block the electrons, leading to a significant degradation in the overall passivation quality. Moreover, the additional interface or layer defects induced by E-beam metallization also plays a role in the degradation of passivation quality. Therefore, it is suggested to thermally evaporate a 100 nm metal protection layer in the first metallization stage.

2) The thickness of interfacial (i)a-Si:H can influence the performance of MoO_x based FBC solar cells. First, all cells (imbedded with 6, 8 and 10 nm i-layer) are featured with high shunt resistance, and increasing the i-layer thickness causes the increase in shunt resistance. This is mainly because thicker i-layer is more likely to cover the textured surface uniformly and reduce the unexpected pinholes and voids resulted from the potential shadings during deposition.

Meanwhile, the series resistance of solar cell is also increased mainly due to the increase of i-layer thickness. Second, 8 nm case shows the lowest FF because it sees a relatively low shunt resistance and high series resistance. Third, 8 nm case shows the best passivation quality (with Voc=643 mV) because it provides a more uniform surface coating than 6 nm case and simultaneously is subject to lower series resistance than 10 nm case. A PCE of 16.18% is achieved in 8 nm i-layer case, with Voc being 643 mV, Jsc being 38.73 mA/cm^2, and FF being 65.06%.

3) The surface roughness and nano-scale contaminations introduced during texturing are effectively reduced after performing 3 cycles of NAOC. This improved textured surface increases the Voc by 7 mV and significantly raises the shunt resistance, which in turn increases the FF to 71%. The PCE is improved to 17.31%.

4) After atmospheric annealing at 130^{o}C for 10 minutes, the interfaces are effectively relaxed and a better junction contact is achieved. Lower temperature (<130^{o}C) is not able to fully relax the interface, while higher temperature (>200^{o}C) will cause the effusion of H atoms from i-layer, leading to additional dangling bonds and degrade the passivation quality. Therefore, 130^{o}C atmospheric annealing for 10 minutes is preferred which slightly enhances Voc and a PCE of 17.60% is achieved.

7.2. TiO_x Based Heterojunction Solar Cells

The performance of TiO_x based electron selective contact can be concluded as follows:

1) The improvement in surface passivation of c-Si/TiO_x stack after FGA is mainly due to the formation of Ti-O-Si bonding, which effectively deactivates the dangling bonds at the c-Si surface. Meanwhile, the PVD evaporated TiO_x at room temperature is of larger void density, porosity and unbalanced bonding profile which results in higher defect densities and poorer passivation quality. FGA mobiles the atoms where rebinding and relaxation of the film occurs which reduces the defect densities, and in turn gives rise to the passivation quality.

2) In c-Si/TiO_x configuration, 5 nm TiO_x capping layer after FGA provides with the best passivation quality (iVoc=677 mV). The non-ideal passivation quality in 3 nm case can be attributed to the inhomogeneous layer deposited by PVD. The nonuniform coating of TiO_x thin layer leads to an incomplete formation of Ti-O-Si bonding at part of the surface areas which brings down the passivation quality. On the other hand, 7 nm TiO_x is subject to higher compressive stress which facilitates its transformation to anatase phase during FGA. This phase transform degrades the passivation due to the fact that amorphous TiO_x is preferred for c-Si surface passivation.

3) In c-Si/TiO_x configuration, the optimal FGA condition is found at 300 ^oC for 4 minutes. Lower temperature (<300 ^oC) is not able to break the original bonding; therefore, fewer Ti-O-Si bonding are formed, leading to the degradation of surface passivation. On the other hand, when the temperature goes beyond 300 ^oC, the decrease in iVoc can be mainly attributed to the phase transformation from amorphous to anatase. The same mechanism also applies to the different annealing time cases where 3-minute forming gas annealing at 300 ^oC is not long enough for a complete formation of Ti-O-Si bonding at the interface, while longer FGA time (>4 mins) induces the phase transformation to anatase of part of the amorphous TiO_x, leading to the degradation of surface passivation quality.

4) In c-Si/SiO_2/TiO_x configuration, the highest iVoc (680 mV) is achieved in the case of 3 nm TiO_x after 350 ^oC FGA for 4 minutes. The difference in TiO_x thickness and FGA temperature can be attributed to the different passivation mechanisms. The surface passivation of SiO_2/TiO_x stack is achieved mainly by the combination of chemical passivation of SiO_2 and field effect passivation of TiO_x. Higher FGA temperature can improve the chemical passivation of SiO_2 due to in-diffusion of H atoms, but it degrades the field effect of TiO_x due to phase transformation. The trade-off between chemical passivation of SiO_2 and field effect of TiO_x as a function of FGA temperature determines the final overall passivation quality.

5) The degradation in surface passivation quality by using different TiO_x sources can

be mainly attributed to the non-stable vacuum pressure during deposition due to the outgassing of fresh TiO_x source. Such outgassing reduces the free mean path of evaporated TiO_x and forms a non-uniform as-deposited layer with high roughness, which leads to additional defects and nucleation after FGA and degrades the passivation quality. The XPS results reveal that the stoichiometry of TiO_x layer deposited from different sources is constant, and the bonding scenario at c-Si/TiO_x is independent from SiO_2 interlayer and source material.

Meanwhile, the ellipsometry measurement demonstrates that the optical constants of TiO_x layers deposited from different source materials are showing identical n, k and absorption coefficient values. The optical band gap of TiO_x is obtained at 3.45 eV and the refractive index of TiO_x is constantly lower than the standard TiO_2 thin film which can be mainly attributed to the optical loss induced by oxygen deficiency in TiO_x layer. The k values of TiO_x layer show a greater absorption at small wavelength compared to that of the standard TiO_2. This result demonstrates that defect states exist within the band gap which is mainly associated with the reduction in O/Ti ratio in the sub-surface region.

6) In c-Si/(i)a-Si:H/TiO_x configuration, 8 nm i-layer gives the best passivation performance. This is mainly because thicker i-layer can better withstand the consumption of i-layer during FGA which violates the Si-H bonds at c-Si surface. Also, the amount of i-layer consumed by TiO_x under specific annealing condition is almost constant, thus, further increasing i-layer thickness does not proportionally improve the passivation quality.

   Meanwhile, the thermal stability test found out that the optimized FGA condition is 350 ^oC for 4 minutes. 6 and 8 nm interfacial i-layers are thermally stable during FGA and the effusion of H atoms under high temperature barely happens. 4 nm case, by contrast, is only thermally stable below 350 ^oC and the effusion of H atoms at the interface cannot be balanced by the hydrogen in forming gas when the FGA temperature reaches 400 ^oC. The improvement in surface passivation at 350 ^oC can be mainly attributed to the enhanced field effect of TiO_x layer, further increasing the FGA temperature to 400 ^oC results in the phase transformation of TiO_x which

damages the field effect, and in turn reduces the passivation quality.

7) In TiO_x based FBC solar cells, metallization must be performed before FGA. This is mainly because the post-FGA after TiO_x/Al junction formation relaxes both the TiO_x and Al films, thus, the abrupt transition at the TiO_x/Al interface is minimized and a better contact results in a higher conductivity. Meanwhile, the formation of AlO_x at TiO_x/Al interface during FGA leads to highly oxygen-deficient TiO_x which is reported to have higher conductivity.

8) The optimal TiO_x thickness at cell level is found at 4 nm. The trade-off between thickness dependent field effect and tunneling resistance determines the overall series resistance of the ETL region. When the TiO_x thickness is lower than 4 nm, the field effect plays a dominate role in determining the series resistance of ETL region. As the thickness goes beyond 4 nm, the tunneling resistance starts to take over the influence of overall series resistance of ETL region.

9) The passivation quality of various rear side structures (e.g. c-Si/TiO_x, c-Si/SiO_2/TiO_x, c-Si/Ti/TiO_x, c-Si/(i)a-Si:H/TiO_x) is nearly the same, and the difference in other external parameters is mainly caused by the series resistance featured in each structure. The highest PCE is achieved in c-Si/TiO_x stack, with Voc being 573 mV, Jsc being 30.53 mA/cm^2, and FF being 74.97%. It can be concluded that the E-beam evaporated TiO_x is not favorable for working as ETL due to the substantial defect densities within the band gap which significantly degrades the passivation quality when Al metal contact is made.

7.3. Outlook

The theoretical efficiency limit of c-Si solar cells has been assessed to be 29.43%, with Voc being 761.3 mV, Jsc being 43.31 mA/cm^2 and FF being 89.26% [81]. Therefore, there is still a large gap between the efficiency obtained in this project and the theoretical limit. Here, a couple of suggestions are made for the future improvement in transition metal oxide based c-Si solar cells.

- **Optimization of ITO layer**

Due to the low work function of ITO layer (~4.5 to 4.7 eV) [82], the band bending formed by MoO_x is reduced by the ITO coating. This impaired field effect damages not only the electron blocking ability, but also the selective transport of holes. It is reported that chlorinated ITO can provide a very high work function of ~6 eV [83], which well matches the work function of MoO_x. Therefore, the field effect is properly preserved by coating with such high work function ITO layer, and the carrier selectivity can be strongly improved.

- **Implementation of ALD for TiO_2 deposition instead of E-beam evaporation**

It has been mentioned before that the property of E-beam evaporated TiO_x is dominated by the source material stoichiometry, substrate temperature, oxygen partial pressure and deposition rate. Due to the function limitation of equipment, TiO_x deposition cannot be optimized which leads to nonconformal coating and a number of defect states within the band gap. This non-ideal TiO_x quality reduces the carrier selectivity and degrades the device performance. Due to its unique advantage of self-limiting process, ALD can provide with uniform stoichiometric TiO_2 layer and the thickness of as-deposited layer can be precisely controlled. It is reported that the stack of SiO_2/TiO_2(ALD)/Al rear side stack achieves an efficiency of 21.6%, with Voc being 676 mV, Jsc being 39.6 mA/cm^2 and FF being 80.7% [7].

- **Growing TiO_2 by oxidation of E-beam evaporated Ti**

Another alternative for growing high quality of TiO_2 has been reported by Ling *et.al.* [84], in which the TiO_2 thin film is obtained by thermally oxidizing E-beam pre-deposited Ti layer in O_2 environment. The best passivation quality is achieved in the case of 3.5 nm of TiO_2 which reaches an effective lifetime of 1.5 ms and a corresponding surface recombination velocity of 16 cm/s. By using this TiO_2 growth method, one might achieve better device performance.

- **Implementation of Mg/Al or Ca/Al contact**

The work function of Al (4.06 eV to 4.26 eV) [85] is similar to that of n-type c-Si, therefore, the TiO_x/Al contact reduces the field effect that formed at c-Si/TiO_x interface,

leading to non-ideal carrier selectivity. By embedding a metal with low work function, such as Mg (3.66 eV) or Ca (2.87 eV) [85], the field effect can be better protected. It has already been reported that Mg/Al contact can serve as good electron-conductive contact, where a low ohmic contact resistivity of ~0.22 Ω/cm^2 and a PCE of 19% is achieved [86].

- **Integration of MoO_x and TiO_x in FBC/IBC solar cells**

After optimizing both MoO_x based HTL and TiO_x based ETL, one can integrate these two TMO carrier selective passivation contacts within one FBC solar cell to truely realize the doping-free passivation for both front and back contacts. Finally, IBC structure based on MoO_x and TiO_x can be properly designed to eliminate metal grid shading and enhance the current density.

- **Other promising TMO materials for carrier selective contacts**

Besides MoO_x and TiO_x, there is still a couple of TMOs that can serve as HTL (e.g. V_2O_5) or ETL (e.g. MgO). It has been reported that V_2O_5 based multilayer back contact (MLBC) solar cell demonstrates an efficiency of 19.02% [87], while MgO based FBC solar cell is also reported to manage to achieve an efficiency of 20% with Voc being 630 mV, FF being 80% and Jsc being 39.5 mA/cm^2 [88].

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