Operational Amplifier with 1-V Rail-to-Rail Multipath-Driven Output Stage

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Abstract—**A bipolar operational amplifier (op amp) with a rail-to-rail multipath-driven output stage that operates at supply voltages down to 1 V is presented. The bandwidth of this output stage is as high as possible, viz. equal to that of one of the output transistors, loaded by the output capacitance. The output voltage can reach both supply rails within 100 mV and the output current is ±15 mA. The op amp is designed to be loaded by a 100-pF capacitor and the unity-gain bandwidth is 3.4 MHz at a 60° phase margin. The voltage gain is 117 dB and the CMRR is 100 dB. The frequency behavior of the multipath-driven (MPD) topology has an improved performance when compared to that of previously presented low-voltage output stages. A figure of merit F_M for low-voltage op amps has been defined as the bandwidth–power ratio.**

I. Introduction

THE TREND towards very low supply voltages forces new demands on the design of accurate analog building blocks. An important building block is the operational amplifier (op amp). Op amps that run on a supply voltage of 1 V have already been in existence for over a decade [1], but until now, the bandwidth of these circuits has been in the kilohertz range rather than in the megahertz range. The bandwidth that can be obtained is mainly limited by the output stage of the low-voltage op amp. To be universally applicable, the output stage has to meet the following requirements.

1) Usually, base–emitter voltages prevent the output from reaching either one of the supply rails. However, to be able to deliver an output voltage signal that is as large as possible, preferably from rail to rail, the actual output transistors have to be connected in a common-emitter (CE) configuration.

2) The minimum supply voltage should preferably be as low as 1 V. This enhances the applicability of the op amp, such as operation on a one-cell battery, but it hampers the design of the op amp because only one base–emitter voltage fits in the supply-voltage range.

3) The maximum bandwidth of the op amp is determined by the current flowing through the output transistors, which determines their transconductance, and by the capacitive load it has to drive. Any transistors preceding the actual CE output transistors more or less reduce the obtainable bandwidth. This reduction should be kept as small as possible.

4) The output stage should be able to push and pull output currents in the order of 10 mA, which means that its current gain should be in the order of 10^3. One output transistor in CE configuration does not meet this condition and therefore emitter followers are normally placed in front of it.

5) Finally, the power consumption must be kept low, so the quiescent current, which is drawn from the supplies by the output stage, must be as small as possible. Also, the output stage must be realized with few and small transistors in order to keep the chip size limited.

The op amp presented here has a complementary class-AB output stage that very well meets the demands listed above. It further contains a complementary input stage with a rail-to-rail common-mode input range and an intermediate stage that is insensitive to the Early effect if the supply voltage is much higher than the minimum value of 1 V.

To be able to compare the output stage presented here with the prior art, both are discussed with respect to the requirements mentioned above. In Section II, two previously presented output stages are examined, and Section III deals with the output stage presented here. To verify the theory of Sections II and III, three op amps with three different output stages have been integrated. The circuit implementation is discussed in Section IV. Section V covers the measurement results and in Section VI conclusions are drawn.

II. Darlington and Widlar Output Stage

The circuit shown in Fig. 1 is the well-known Darlington output stage. For simplicity, only the n-p-n or pull side is shown, but the theory presented in this and the following section also applies to the complementary p-n-p side. The driver transistor Q_2 precedes the output transistor Q_1 and the intermediate stage consists of transistors Q_{11}–Q_{14}. Miller capacitor C_{m1} splits the pole at the output of the intermediate stage and the one at the output of the output stage. A difficult condition, where the frequency compensation is concerned, is that the

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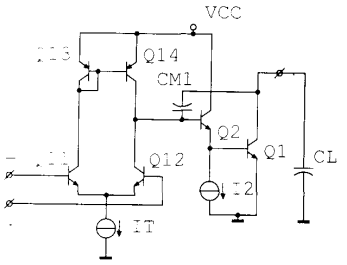

Fig. 1. The n-p-n Darlington output stage.

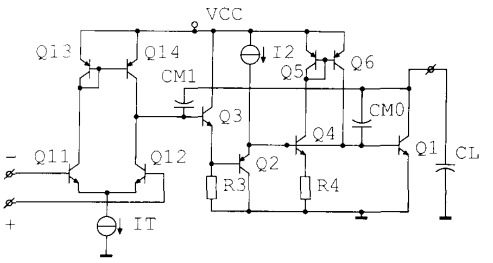

Fig. 2. The n-p-n Widlar output stage.

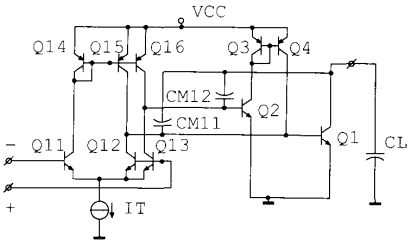

Fig. 3. The n-p-n MPD output stage.

circuit can be loaded by a relatively large output capacitor C_L.

With respect to the specifications summed up in the Introduction, the following analysis of the Darlington output stage can be made.

1) Since the output transistor has a CE configuration, the output-voltage range is large; depending on the output current, Q_1 is able to reach the supply rail within about 100 mV.

2) The minimum value of the supply voltage is not 1 V but 1.8 V, because the two base–emitter voltages of Q_1 and Q_2 are stacked.

3) As in all CE output stages, the bandwidth of the Darlington output stage is determined by the quiescent current through Q_1 and by C_L, but, unfortunately, it is limited by the internal pole of the output stage, located at the base of Q_1. If the output current increases, the output bump in the frequency response is likely to occur [2]. This bump becomes even more likely in the design of op amps employing lateral p-n-p transistors, where the bandwidth is limited by the transit frequency of the transistors, as well as by the load capacitor. Unfortunately, the use of p-n-p's in the CE configuration is inevitable in low-voltage op amps.

4) The current gain of the Darlington output stage is equal to $\beta_1\beta_2$, if β is the current gain of the transistors Q_1 and Q_2, respectively. Even if the output stage consists of lateral p-n-p transistors with a moderate current gain of 30, the total current gain of the output stage is large enough to push output currents in the order of milliamperes.

5) The Darlington output stage consists of only two transistors and the transistor Q_2 consumes only $1/\beta$ of the current through Q_1, which makes this output stage very efficient. However, to avoid the output bump, the quiescent current through Q_2 should be substantially increased.

Another previously presented output stage is the Widlar output stage, shown in Fig. 2 [1]. Widlar used the output stage in National Semiconductor's 1-V op amp LM10. Output transistor Q_1 is preceded by the emitter followers Q_2 and Q_3. To be able to pull large output currents, a boost circuit Q_4–Q_6 is added. The intermediate stage comprises transistors Q_{11}–Q_{14} and the circuit is Miller compensated by C_{m1}.

If the Widlar output stage is also investigated regarding the previously stated requirements, the following results are found.

1) Transistor Q_1 has a CE configuration, so the output-voltage range is again from rail to rail.

2) The emitter followers Q_2 and Q_3 are folded, yielding a minimum supply voltage of only 1 V.

3) The input signal has to pass through emitter followers Q_2 and Q_3, which lowers the obtainable bandwidth and makes the occurrence of the output bump even more likely. We found that the positive loop gain around Q_4–Q_6 and the presence of Q_2 and Q_3 necessitates the insertion of an additional compensation capacitor C_{m0} [3], to keep the output bump within bounds at high current levels; this further reduces the bandwidth.

4) The current gain of the Widlar output stage is potentially very high. If the boost circuit Q_4–Q_6 is configured appropriately, a current gain of more than 10^4 is possible.

5) When designed for optimal bandwidth, the current through Q_2–Q_4 can easily be half that flowing through Q_1, giving a rather high total current consumption. The output stage consists of seven transistors, of which Q_2 and Q_3 must have a rather large emitter area, and an additional capacitor. Because of this, the chip size is larger than that of the Darlington output stage.

III. Multipath-Driven Output Stage

Fig. 3 shows the n-p-n multipath-driven (MPD) output stage [4]. Output transistor Q_1 is driven by Q_2–Q_4. Because this signal path provides the necessary gain, it is referred to as the "gain path." Parallel to the gain path, the so-called "feedforward path" directly drives output

transistor Q_1. This feedforward path gives the circuit the maximal obtainable bandwidth and bypasses the bandwidth reduction caused by Q_2–Q_4. The clue to this success is that the intermediate stage, with transistors Q_{11}–Q_{16}, supplies the output stage with two identical, but decoupled signals. The pole at the output of Q_1 and the two poles at the two outputs of the intermediate stage are being split by the Miller capacitors C_{m11} and C_{m12}, respectively.

With respect to the demands on low-voltage op amps as summarized in the Introduction, the following is claimed about the op amp with MPD output stage.

1) The MPD output stage has a rail-to-rail output-voltage range.

2) Since none of the base–emitter voltages of the transistors are stacked, the output stage operates at a supply voltage of 1 V.

3) The frequency behavior of the MPD output stage equals that of the capacitively loaded output transistor Q_1. The gain path through Q_2–Q_4 does not influence the frequency behavior because of the feedforward path to Q_1. The bandwidth is now entirely determined by the current through Q_1 and by C_L.

4) The current gain of the MPD output stage is of the same order as that of the Darlington output stage.

5) The MPD output stage consists of four transistors, but also two additional transistors are needed in the intermediate stage; it therefore occupies more chip area than the Darlington but less than the Widlar output stage. The output stage is economical; driver transistors Q_2–Q_4 only consume $2/\beta$ of the current flowing through Q_1.

To confirm these claims, the behavior of the MPD output stage is further analyzed. The first claim speaks for itself, and the second can be verified directly from Fig. 3. To investigate the third claim about the frequency behavior of the MPD output stage, the transfer from the input voltage of the intermediate stage to the output voltage is analyzed. To calculate this transfer, the current equations of the small-signal equivalent circuit are solved. The resulting voltage gain of the circuit is

$$\frac{U_o}{U_i} = \frac{1}{sr_{e13}C_{m12}} \cdot \frac{1 + s\dfrac{r_{e13}}{r_{e12}} r_{e2}C_{m12}}{1 + sr_{e2}C_{m11} + s^2 r_{e2}C_{m11}r_{e1}C_L} \quad (1)$$

where r_e are the emitter resistances of the transistors and s is the complex frequency, and the Miller capacitors C_{m11} and C_{m12} are assumed large compared to the diffusion capacities of the transistors. Since

$$r_{e2} \approx \beta_1 r_{e1} \quad (2)$$

it can be assumed that

$$r_{e2}C_{m11} = r_{e1}\beta_1 C_{m11} \gg r_{e1}C_L. \quad (3)$$

If, further, the Miller capacitors C_{m11} and C_{m12} as well as the current through the intermediate transistors Q_{12} and Q_{13} are equal:

$$r_{e13}C_{m12} = r_{e12}C_{m11} \quad (4)$$

and the voltage gain becomes

$$\frac{U_o}{U_i} = \frac{1}{sr_{e13}C_{m12}} \cdot \frac{1}{1 + sr_{e1}C_L}. \quad (5)$$

The pole–zero cancellation depends on the matching of the Miller capacitors and of intermediate stage transistors. This can be done very accurately, which is important, because a pole–zero doublet gives a slow settling time of the transient response [5]. Fig. 4 shows the frequency response of the intermediate and output stage. The dashed and dotted lines represent the response of the gain and feedforward paths, respectively; the gain path has a large gain, but a smaller bandwidth, and the feedforward path has a small gain, but larger bandwidth. As can be seen from Fig. 4, no pole–zero doublet occurs. The bandwidth is, thus, only limited by the current flowing through Q_1 and by the load capacitor C_L.

The current gain of the MPD output stage can be calculated as $\frac{1}{2}\beta_1(\beta_2 + 1) \approx \frac{1}{2}\beta_1\beta_2$. If necessary, it could be further increased by scaling the current mirror Q_3, Q_4. Note that Q_4 supplies just the current needed to drive output transistor Q_1; in particular, this implies that, at small output currents, only a very small current flows through Q_2–Q_4.

The fifth assertion, regarding the number of transistors and their current consumption, can again be verified directly from Fig. 3.

IV. Circuit Implementation

The MPD output stage shown in Fig. 5 embodies two complementary parts, Q_{110}–Q_{140} and Q_{210}–Q_{240}. Both parts are identical to the output stage shown in Fig. 3, except that the current mirrors Q_{130}–Q_{140} and Q_{230}–Q_{240} are scaled 1:4 to increase the gain. The small emitter resistors R_{110} and R_{210} prevent breakthrough of the output transistors at high current and voltage levels, but they do not limit the output-voltage range in normal operation; when driving light loads, the output voltage is able to reach within 100 mV of the supply rails. The output transistors Q_{110} and Q_{210} are able to sink or source a maximum output current of 15 mA. Transistors Q_{150} and Q_{250} are part of the class-AB current control loop. The quiescent current through the output transistors is kept at 320 μA, and the minimum current through either one of these transistors is 160 μA.

Fig. 6 shows the input stage, the intermediate stage, and the class-AB current control. The intermediate stage consists of two parts, each with its own tail current source of 22 μA, and it has four outputs to drive the four inputs of the output stage. The differential stage Q_{410}–Q_{420} supplies the n-p-n output stage and has n-p-n current mirrors Q_{450}–Q_{460} that are connected to the negative supply rail, just as the n-p-n output transistors are. The other differential stage Q_{430}–Q_{440} is connected to the p-n-p output stage and has p-n-p current mirrors Q_{470}–Q_{480} that are connected to the positive supply rail. Thus, the voltages on all matching transistors of the

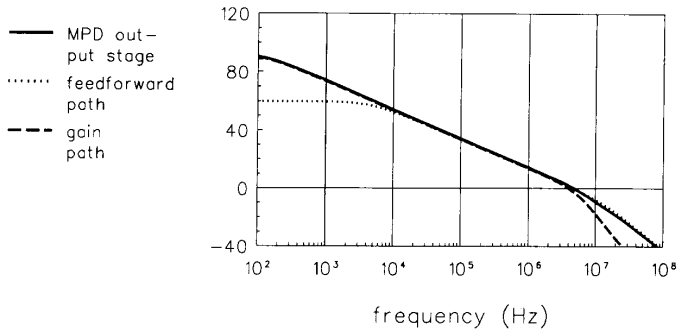

Fig. 4. Frequency response of the MPD output stage. The dashed line gives the response of the gain path, with a large gain but smaller bandwidth, and the dotted line marks the response of the feedforward path, which has a small gain but larger bandwidth.

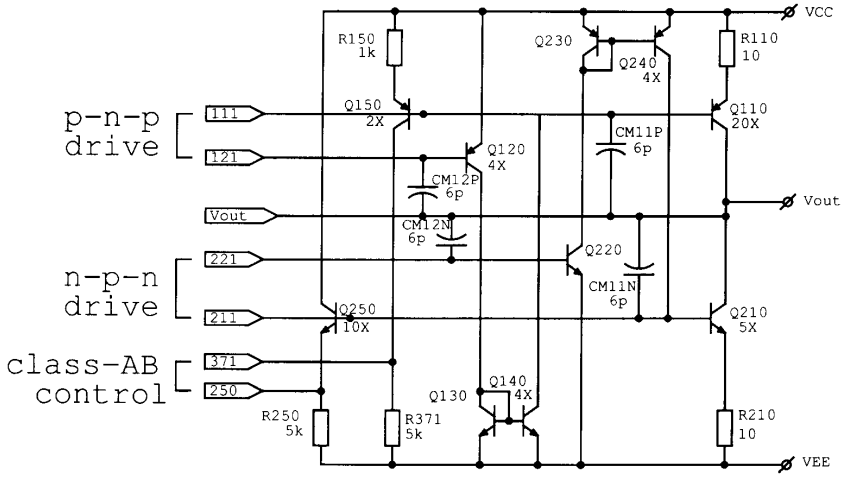

Fig. 5. Circuit implementation of the complementary MPD output stage.

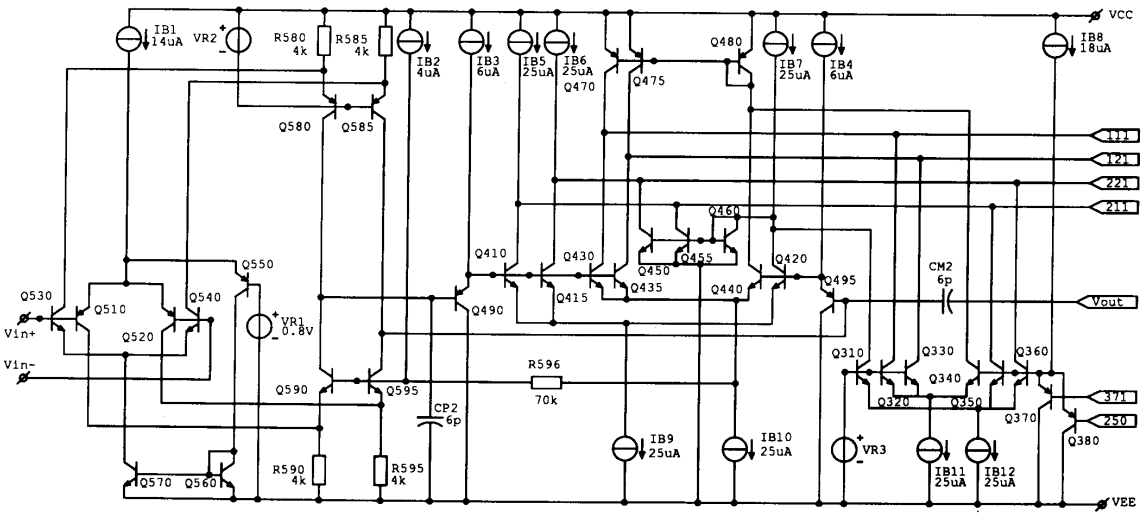

Fig. 6. Circuit implementation of the input stage, intermediate stage, and class-AB current control.

intermediate stage are equal and the Early effect is compensated. This guarantees operation also when the supply voltage is much higher than the 1 V minimum.

The feedback class-AB current control embodies transistors Q_{150} and Q_{250}, shown in Fig. 5, and Q_{310} through Q_{380}, shown in Fig. 6. The differential amplifier $Q_{310}-Q_{360}$ consists of two parts, each connected to the matching part of the intermediate stage, again to compensate for the Early effect. The currents through the output transistors Q_{110} and Q_{210} are converted into voltages at the bases of Q_{370} and Q_{380} by Q_{150} and Q_{250}, respectively. These voltages are compared to the reference voltage V_{R3} by the feedback amplifier $Q_{310}-Q_{360}$ and thus the quiescent current through Q_{110} and Q_{210} is kept at a constant value. If one of the output transistors is supplying an output current, the matching transistor of the pair Q_{370}, Q_{380} is cut off, and the current through the other, nonactive, output transistor is regulated at half the quiescent current by the feedback amplifier $Q_{310}-Q_{360}$ [6], [7].

At supply voltages of 1.7 V and more, the input stage $Q_{510}-Q_{540}$ has a rail-to-rail input-voltage range. For supply voltages below that level, only the p-n-p input pair operates in the common-mode range from the negative supply rail to 0.8 V below the positive supply. However, if desired, an input stage with a fully rail-to-rail common-mode input range at a supply voltage of 1 V could also be incorporated [3]. Current switch Q_{550} keeps constant the sum of the currents through both input pairs over the full common-mode input range. The transconductance of the input stage therefore has a constant value of 0.25 mmho. The input-offset voltage changes between that of the n-p-n and p-n-p transistor pair when the common-mode input voltage crosses the turnover range of Q_{550}. This limits the CMRR, as is described in Section V. The circuit $Q_{580}-Q_{595}$ adds the currents of the differential input stages.

The current sources and reference voltages included in the op amp are realized with the bias circuit shown in Fig. 7. It comprises a PTAT current source $Q_{10}-Q_{60}$ and a start-up circuit $Q_{70}-Q_{80}$ [8].

The output is assumed to be loaded by a maximum output capacitor C_L of 100 pF. At a quiescent current through the output transistors of 320 μA, the output transconductance g_{out} is 12 mmho, and the base–emitter capacitance C_{be} is 0.6 and 2 pF for the n-p-n and p-n-p transistors, respectively. The Miller capacitors C_{m11P}, C_{m12P}, C_{m11N}, and C_{m12N}, with a value of 6 pF each, are connected between the output of the output stage and each of its four inputs. The output pole then has a value:

$$\frac{g_{out}}{2\pi C_L(1+C_{be1}/C_{m11})} \approx 15 \text{ MHz}. \quad (6)$$

The bandwidth of the output and intermediate stage should be chosen at a factor of 2 lower than the output pole [7], which is realized with an intermediate-stage transconductance g_{int} of 0.28 mmho:

$$\frac{g_{int}}{2\pi C_{m11}} = \frac{1}{2}\frac{g_{out}}{2\pi C_L(1+C_{be1}/C_{m11})} \approx 7.5 \text{ MHz}. \quad (7)$$

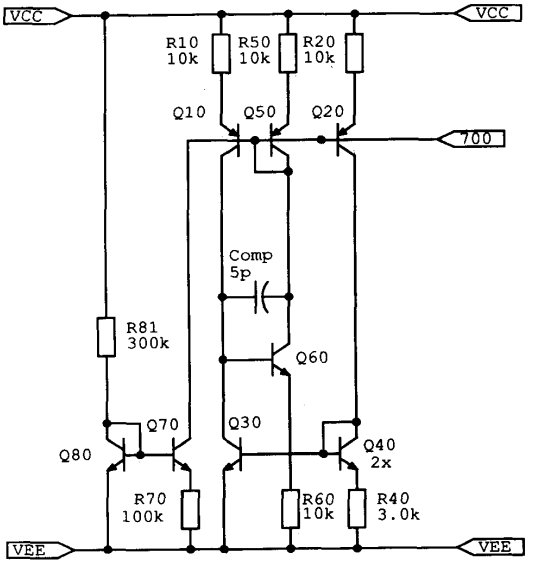

Fig. 7. The PTAT current source.

The overall bandwidth should again be half this value, which is achieved with a Miller capacitor C_{m2} of 6 pF, connected between the output of the output stage and the output of the input stage, and an input-stage transconductance g_{inp} of 0.25 mmho:

$$\frac{g_{inp}}{4\pi C_{m2}} = \frac{1}{2}\frac{g_{int}}{2\pi C_{m11}} = \frac{1}{4}\frac{g_{out}}{2\pi C_L(1+C_{be1}/C_{m11})} = 3.4 \text{ MHz}. \quad (8)$$

The op amp now has a straight 6-dB/octave frequency rolloff from 3 Hz to 6 dB below the unity-gain frequency of 3.4 MHz. Any pole–zero doublet, which would remain in the MPD output stage, is effectively suppressed by this second nest.

V. Measurements

Besides the MPD output stage, a Darlington and Widlar output stage have also been integrated with the same input and intermediate stages shown in Fig. 5. Fig. 8 shows a micrograph of the op amps with MPD and Darlington output stages. On the right-hand side of the micrograph the output stages can be distinguished; in the middle, the intermediate stage and class-AB current control are situated. The input stage, with quad layout, can be seen to the left of the micrograph. The total capacity used in each of these op amps is 41 pF. The chip area that is occupied by the output stages is 0.26 mm^2 for the MPD output stage and 0.20 mm^2 for the Darlington output stage. A micrograph of the op amp with the Widlar output stage is shown in Fig. 9. Because of the additional compensation capacitors, the total capacity is 51 pF for the Widlar output stage and the chip area is 0.30 mm^2. The op amps have been made in a 12-V

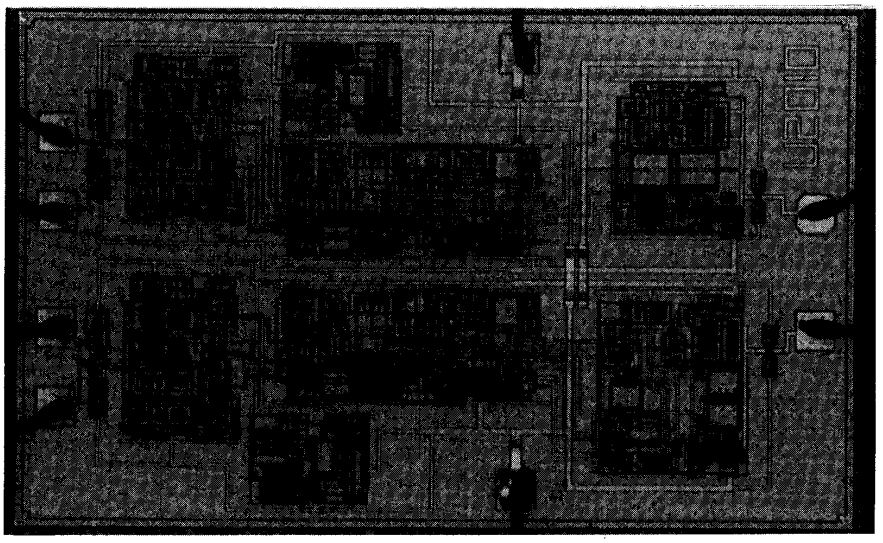

Fig. 8. Micrograph of the op amp with MPD output stage (bottom) and the op amp with Darlington output stage (top).

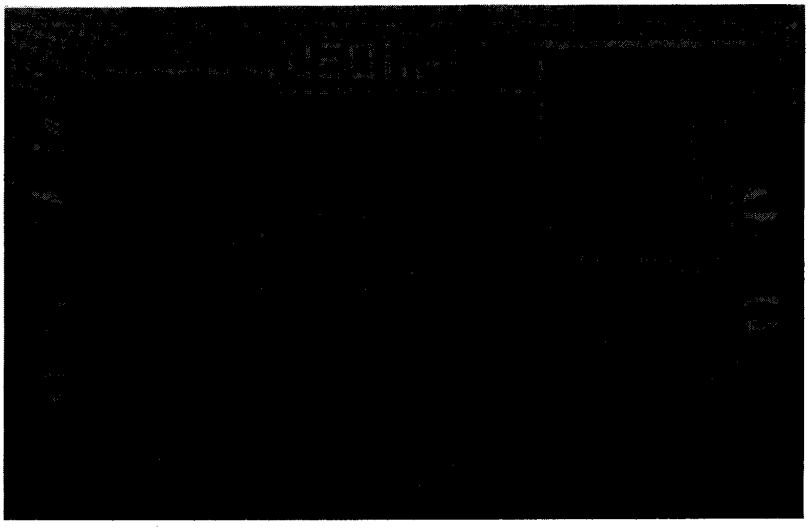

Fig. 9. Micrograph of the op amp with Widlar output stage (bottom). The circuit shown on top of the micrograph is not discussed here.

BiCMOS process with 3-GHz n-p-n transistors and 1-GHz p-n-p transistors.

The measured open-loop frequency response of the op amp with MPD output is shown in Fig. 10. The supply voltage is 1 V and the op amp is loaded by a 100-pF capacitor and a 10-kΩ resistor in parallel. The unity-gain frequency is 3.4 MHz at a phase margin of 61°, and the dc gain is 117 dB. If the op amp drives a light load, the phase margin increases to 70°.

Since all op amps have been designed with an equal quiescent current of 320 μA flowing through the output transistors, the bandwidth of all three, following from (8), is roughly the same. The supply power needed to achieve this differs, however. To compare the performance of the op amps, a figure of merit F_M is therefore defined as the bandwidth–power ratio of the output stages:

$$F_M = \frac{B_W}{V_{\mathrm{sup}_{\min}} \cdot I_{\mathrm{sup}}}. \tag{9}$$

The dimension of this figure of merit F_M is inverse to the well-known power–delay product P_d in digital circuits. Table I shows the values of F_M of the three output stages together with the characteristics from which they are derived. The MPD output stage has a substantially higher

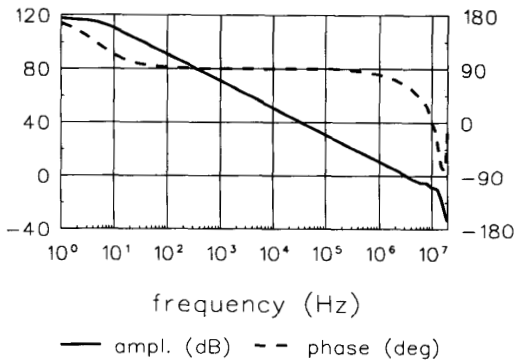

Fig. 10. Measured frequency response of the op amp with MPD output stage. The unity-gain frequency is 3.4 MHz, and the unity-gain phase margin is 61°.

TABLE I
FIGURE OF MERIT, $F_M = B_w / V_{sup_{min}} I_{sup}$, FOR THE THREE OUTPUT STAGES

Parameter	MPD	Darlington	Widlar	Unit
Figure of merit F_M	18	11	9.6	MHz/mW
Bandwidth Output Stage	7.5	7.5	6.7	MHz
Minimum Supply Voltage	1.0	1.8	1.0	V
Supply Current Output Stage	420	395	695	μA

TABLE II
SPECIFICATIONS OF THE COMPLETE OP AMPS

MPD: Op Amp with Multipath-Driven Output Stage, 1.0-V Supply
Darlington: Op Amp with Darlington Output Stage, 2.0-V Supply
Widlar: Op Amp with Widlar Output Stage, 1.0-V Supply
All Op Amps: $R_L = 10$ kΩ, $C_L = 100$ pF, Temp = 27° C

Parameter	MPD	Darlington	Widlar	Unit
Input-Offset Voltage	0.6	0.6	0.6	mV
Input-Noise Voltage	23	23	23	nV/$\sqrt{}$Hz
Input-Bias Current	140	140	140	nA
Supply-Voltage Range	1–7.5	1.8–7.5	1–7.5	V
Total Supply Current	700	670	980	μA
CMRR	100	100	100	dB
Open-Loop Gain	117	110	115	dB
Output-Voltage Range	$V_{CC}-0.1/V_{EE}+0.1$	$V_{CC}-0.1/V_{EE}+0.1$	$V_{CC}-0.1/V_{EE}+0.1$	V
Output Current	±15	±15	±15	mA
Slew Rate	1.1	1.1	0.9	V/μs
Unity-Gain Frequency	3.4	3.5	2.7	MHz
Unity-Gain Phase Margin	61	63	63	degree

figure of merit F_M than that the Darlington output and compared to the Widlar output, an improvement of almost a factor of 2 is achieved.

Table II lists typical overall specifications of the three op amps. The total supply current of the MPD op amp is 700 μA and it is constant within 5% over the supply-voltage range from 1 to 7.5 V. The average input-offset voltage is ±0.6 mV, and the CMRR is 100 dB in the common-mode range where either the n-p-n or the p-n-p input pair is active and 62 dB in the turnover range of Q_{550}. If desired, this value can be enlarged at the cost of a proportional enlargement of the turnover range by placing a resistor in series with the emitter of Q_{550}. The maximum output current is ±15 mA. The slew rate of the op amp with MPD output is 1.1 V/μs.

VI. Conclusions and Discussion

The operational amplifier that has been presented operates at supply voltages down to 1 V, and it has rail-to-rail input and output ranges. A multipath-driven output stage is introduced with a feedforward path directly from the intermediate stage to the output transistor. It gives the op amp a bandwidth that is determined exclusively by the load capacitor and by the amount of current through the output transistors.

The op amp with multipath-driven output, as well as the op amps with Darlington and Widlar outputs, have been implemented in a BiCMOS process with 3-GHz n-p-n's and 1-GHz vertical p-n-p's. A figure of merit F_M is established which is the ratio of bandwidth and power consumption of the output stages. The figures of merit for these three output stages are 18, 11, and 9.6 MHz/mW, respectively. The difference between the three op amps is now mainly apparent at high-current levels. If lateral p-n-p's are used, the difference between the multipath-driven output stage and the Darlington and Widlar output stages is even more distinct. Even at low output-current levels, the output bump then occurs as a result of the internal poles of these latter output stages. The multipath-driven output stage directly addresses the output transistor and there is no output bump. Presently, a 1-V 10-MHz op amp, loaded by 10 pF and using only 100-μA quiescent current in the output stage with 100-MHz lateral p-n-p's, is being developed. The figure of merit F_M of this op amp is 120 MHz/mW.

Acknowledgment

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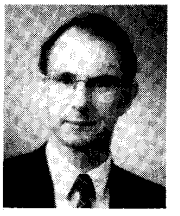

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