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A Single-Stage Regulating Voltage-Doubling Rectifier for Wireless Power Transfer

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***Abstract*—In this letter, a 6.78-MHz single-stage regulating voltage-doubling rectifier is presented for biomedical wireless power transfer (WPT) applications. Derived from a full-wave voltage doubler, a theoretical voltage conversion ratio (VCR) of 2 can be achieved, which benefits the end-to-end voltage gain of a biomedical WPT system with varying link conditions. As a result, a wider WPT operational range and less coil-link loss can be achieved. To avoid efficiency loss due to cascading, the rectifier output is in-situ regulated in a sub-50-mV hysteresis window by pulse-skipping control. To ensure a high power conversion efficiency (PCE), adaptive delay-compensated active diodes are adopted with an offset locking technique. The input/output capacitors of the rectifier are fabricated on-chip, achieving a fully integrated design. The rectifier was fabricated in a 180-nm BCD process, occupying a silicon area of 0.3/2.7 mm^2 without/with on-chip capacitors. The measurements show that the rectifier can realize a peak PCE at 90.6% when the output power is 79.8 mW. The PCE and VCR are achieved higher than 86.4% and 1.6, respectively, over a large loading range (from 1 to 40 mA). The rectifier can output a maximum power of 159.2 mW, satisfying most biomedical implants.**

***Index Terms*—Adaptive delay compensation, biomedical implants, hysteresis output regulation, regulating rectifier, voltage conversion ratio (VCR), voltage doubler (VD), wireless power transfer (WPT).**

I. Introduction

Wireless power transfer (WPT) is widely used for powering biomedical implantable devices. In a typical biomedical WPT system, a high power conversion efficiency (PCE) is critical to reduce heat generation that can be absorbed by human tissue. On the other hand, a compact system is always desired for bioimplants. Thus, the regulating rectifier becomes a promising solution as a single-stage wireless power receiver performing voltage rectification and regulation simultaneously. It avoids cascaded power losses and reduces the use of bulky power components [1], [2], [3], [4], [5], [6].

In practice, the transmitter (TX) and receiver (RX) coils in a biomedical WPT system are usually loosely coupled [Fig. 1(a)], and the voltage gain of the inductive link may unpredictably drop due to a large coil separation or misalignment [7], [8], [9]. When the wireless link is too weak to power the implants with the minimum required supply voltage, the WPT will fail. Typically, a regulating rectifier derived from a full-bridge rectifier (FBR) ensures a full-wave operation and a high PCE [2] [Fig. 1(b)]. However, the FBR-based topology requires the amplitude of the ac input V_{AC} to be higher than the dc output V_{DC}. Therefore, it only provides a voltage conversion ratio (VCR) lower than 1, limiting the receiver operation in loosely coupled conditions. Recently, some works have been reported to cope with the low-voltage gain, without increasing the TX power demand [Fig. 1(c)]. Lu et al. [4] and Li et al. [5] proposed a reconfigurable 1X/2X rectifier working as a voltage doubler (VD) in weak coupling cases; however, the output regulation is achieved by 1X/2X mode switching that may become unstable due to the varying VCR ratio between the 1X and 2X modes [8]. In [3] and [10], resonant current-mode (CM) rectifiers are presented, in a working fashion similar to a boost converter. Thus, a high VCR can be easily obtained. However, since the ON resistance of a power switch is in the resonance loop and the output charging is always with a switch hard turn-on, the PCE is lower than that in a voltage-mode rectifier. The resonance-and-charging operation also indicates a low load-driving frequency, thus a low output power.

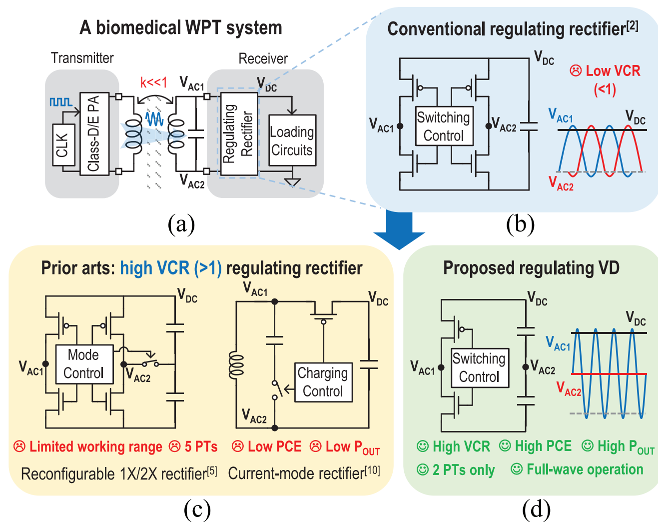

Fig. 1. (a) Biomedical WPT system. (b) FBR-based regulating rectifier [2]. (c) Prior high-VCR regulating rectifiers [5], [10]. (d) Proposed rectifier.

In this letter, a single-stage regulating voltage-doubling rectifier is presented to enhance the WPT voltage gain without sacrificing other performances [Fig. 1(d)], employing only two power transistors and a fully integrated implementation. Derived from a full-wave VD, it has a theoretical VCR of 2 and a full-wave operation leading to high output power. A pulse skipping control is used to regulate the output in a 50-mV hysteresis window to eliminate cascading dc–dc conversion. Adaptive delay-compensated active diodes in the proposed design ensure a high PCE. The on-chip capacitors further decrease the system form factor.

II. System Architecture

Fig. 2 shows the system architecture of the proposed regulating voltage-doubling rectifier, which includes three major parts: 1) a power stage; 2) a hysteresis output controller; and 3) a self-start-up block.

In the power stage, two power switches, S_P and S_N, are driven by the buffered outputs of two delay-compensated comparators, CMP$_P$ and CMP$_N$, respectively. When the rectifier is enabled (2X mode), both switches operate as active diodes. The output capacitor C_{L1} is charged in the positive half-period of V_{AC}, and C_{L2}

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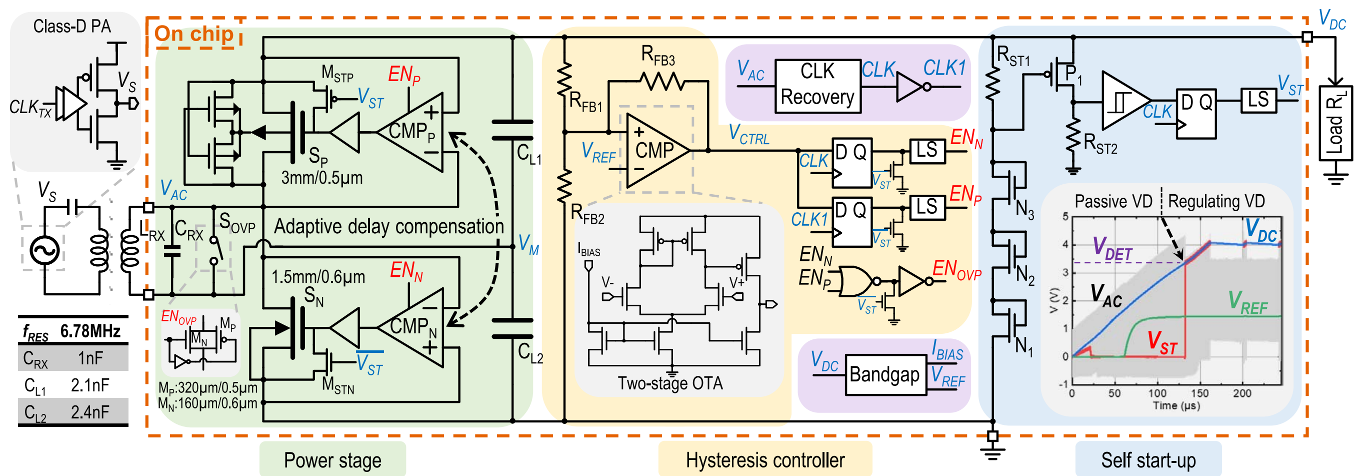
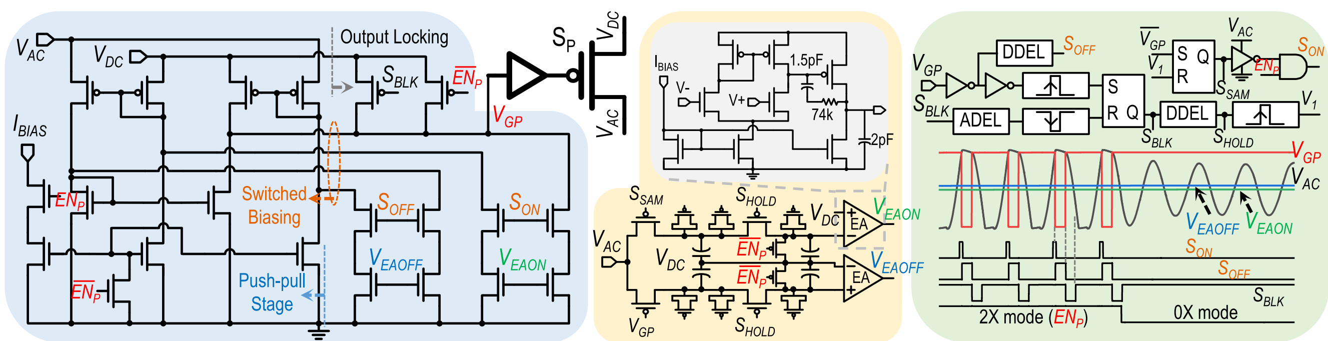


Fig. 2. System architecture of the proposed regulating voltage-doubling rectifier.



(a) (b) (c)

Fig. 3. Circuit implementation of CMP_P: (a) push–pull stage; (b) delay-to-voltage converter; and (c) logic timing generator (DDEL: digital delay cell).

is charged in the negative half-period, forming a full-wave operation. C_{L1} and C_{L2} are stacked to achieve a doubled output voltage ($V_{DC} = 2V_M$). A transmission-gate switch, S_{OVP}, for overvoltage protection is employed between the two ac input nodes to short the $L_{RX}C_{RX}$ tank when the rectifier is disabled (0X mode). S_{OVP} can also be used as a short-circuit load-shift-keying switch to realize uplink data telemetry to the WPT transmitter.

The output voltage, V_{DC}, is regulated at 4 V in this design by a hysteresis-based pulse-skipping controller. The divided version of V_{DC} is compared with a reference voltage V_{REF}, which is generated at 1.45 V by an on-chip bandgap reference. The comparator, CMP, is a two-stage OTA with a positive feedback resistor, R_{FB3}. The hysteresis window is thus defined as

$$\mathrm{Hyst} = V_{\mathrm{REF}}\left(\frac{R_{FB1} + R_{FB2}||R_{FB3}}{R_{FB2}||R_{FB3}} - \frac{R_{FB1}||R_{FB3} + R_{FB2}}{R_{FB2}}\right) \quad (1)$$

which is less than 50 mV in this work. When V_{DC} reaches the upper hysteresis threshold, the output of CMP, V_{CTRL}, goes high. The rectifier will be disabled (0X mode) by setting S_P and S_N at V_{DC} and V_{SS}, respectively, and S_{OVP} is turned on to limit the amplitude of V_{AC}. When V_{DC} reaches the lower hysteresis threshold, V_{CTRL} goes low to enable the rectifier (2X mode); S_P and S_N work as active diodes, and S_{OVP} is turned off. In order to realize a smooth mode switching between 2X and 0X, a synchronized clock signal, *CLK*, is recovered from V_{AC} to synchronize EN_P, EN_N, and EN_{OVP} by the moment when V_{AC} equals V_M. Therefore, the mode switching happens when no conduction path exists between V_{AC} and V_{DC}, so V_{AC} is not distorted and the resonance power can be saved.

The self-start-up of the rectifier is achieved by biasing S_P and S_N as diode-connected MOSFETs. As a result, the rectifier works as a passive VD till V_{DC} attains a certain voltage V_{DET}. V_{DET} is around 3.4 V in this work, which is defined by the threshold voltages of MOSFETs

$$V_{\mathrm{DET}} = V_{TH,N1} + V_{TH,N2} + V_{TH,N3} + V_{TH,P1} \quad (2)$$

where N_1 is a 2-V device, and N_2, N_3, and P_1 are 5-V devices. R_{ST1} and R_{ST2} are current-limiting resistors to reduce the quiescent power consumption of the start-up block. A Schmitt trigger is employed to avoid potential multistartup issues caused by the slight drop in V_{DC} when the rectifier just becomes active.

III. Adaptive Delay Compensation

When the rectifier works at industrial, scientific, and medical (ISM) band frequencies such as 6.78/13.56 MHz or even higher ones, the propagation delay in active diodes (CMP_P/CMP_N and gate drivers) should be carefully compensated. Otherwise, the power switches S_P and S_N can hardly be turned on or off at proper moments, inducing conduction delays and reverse currents. Techniques, such as current injection [11], [12], voltage offset [13], etc., were reported to adaptively compensate for the delay in active rectifiers. However, these works do not consider output regulation. In this work, the adaptive current injection technique is adopted in CMP_P and CMP_N with an offset-locking technique, achieving regulation-compatible delay compensation (Fig. 3).

When the rectifier is in 2X mode, the propagation delay in the active diode can be detected by a delay-to-voltage converter formed

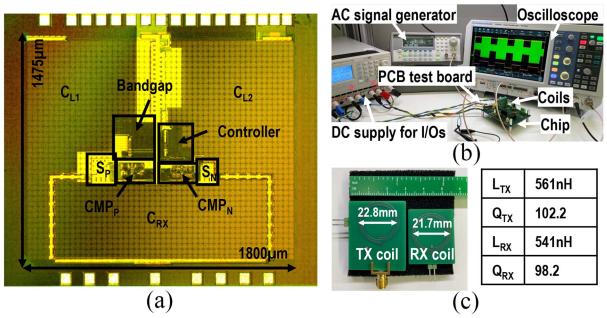


Fig. 4. (a) Chip micrograph of the proposed rectifier. (b) Measurement setup during steady state. (c) Measured coil sizes and parameters.

by a sample-and-hold circuit and an error amplifier (EA) [Fig. 3(b)]. The delay-converted voltages, V_{EAON} and V_{EAOFF}, are then fed into the push–pull stage by switched voltage-controlled biasing to compensate for the delay [Fig. 3(a)]. When the proper offset is given by V_{EAON} and V_{EAOFF}, the delay can be near-optimally compensated regardless of coupling/loading/PVT variations [11]. The offset-current injection moment is controlled by S_{ON} and S_{OFF} generated by the logic timing generator [Fig. 3(c)]. To avoid energy waste by giving turn-on offset too early, S_{ON} is designed as a short pulse to enable switched biasing solely at the moment when V_{AC} is in its rising (or falling) edge and close to V_{DC} (or V_{SS}) in CMP_P (or CMP_N). This is done by 1) designing the duration of S_{BLK} to be no shorter than 30 ns by an analog delay cell (ADEL) to freeze S_{ON}, when V_{AC} is in its falling (or rising) edge in CMP_P (or CMP_N) and 2) using the V_{AC}-supplied inverters.

When the rectifier is in 0X mode, CMP_P and CMP_N are off, and the outputs of CMP_P and CMP_N are locked to turn off S_P and S_N. Due to unavoidable leakage, the held voltages floating in the delay-to-voltage converters can vary from their initial levels (e.g., around V_{DC} in CMP_P), and the offsets given by the continuous-time EAs (V_{EAON} and V_{EAOFF}) will shift as well. This will cause a long settle time or even malfunctions when the rectifier is enabled again. Therefore, an offset-locking technique is proposed in the delay-to-voltage converters. In 0X mode, the held voltages are designed to be short-connected to V_{DC} and V_{SS} in CMP_P and CMP_N, respectively. The outputs of EAs will thus stay around their common-mode voltages, which are close to those in the near-optimal compensation cases. The input pair of EAs is further designed to have a large device size to reduce the effect of mismatch. Thus, when the rectifier enters 2X mode again, CMP_P and CMP_N can still provide mostly proper offset and have a short settle time.

IV. Measurement Results

The proposed rectifier was fabricated in a 180-nm BCD process with standard 1.8-V/5-V devices, occupying a silicon area of 0.3/2.7 mm^2 without/with on-chip capacitors, as shown in Fig. 4(a). C_{RX} (1 nF) was implemented using MIM capacitors, while C_{L1} (2.1 nF) and C_{L2} (2.4 nF) were implemented using MOS capacitors stacked by MIM capacitors. Fig. 4(b) shows the measurement setup when the rectifier is in the steady state. Fig. 4(c) shows the measured coil sizes and parameters. The inductance, L_{TX} and L_{RX}, and quality factors, Q_{TX} and Q_{RX}, were measured by an impedance analyzer at 6.78 MHz. To achieve cleaner signals and better high-frequency noise filtering, two additional off-chip capacitors (100 nF and 2.2 μF) were added at the dc output nodes in the test board.

Fig. 5 shows the measured steady-state waveforms of the rectifier when R_L is 2 kΩ (equivalent to $I_L = 2$ mA). The rectifier regulates V_{DC} at 4 V by pulse-skipping control [Fig. 5(a)]. When it is in 2X mode, the proper operation of CMP_P and CMP_N can be observed

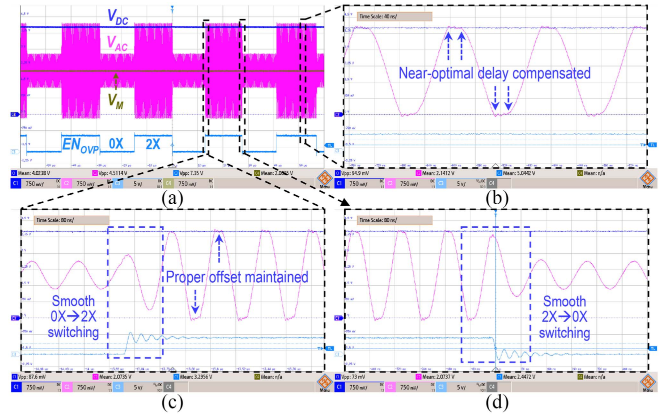


Fig. 5. (a) Measured steady-state waveforms of the rectifier when R_L is 2 kΩ; zoomed-in waveforms (b) in 2X mode; (c) 0X to 2X; and (d) 2X to 0X.

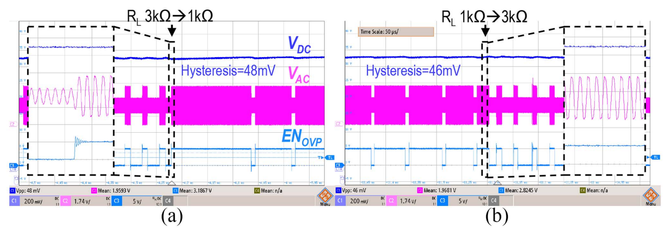


Fig. 6. Measured load-transient waveforms of the rectifier when R_L changes (a) from 3 to 1 kΩ and (b) from 1 to 3 kΩ.

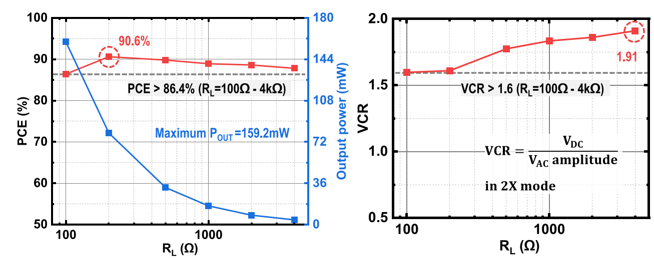


Fig. 7. Measured PCE, P_{OUT}, and VCR of the rectifier versus R_L.

[Fig. 5(b)], where V_{AC} has no obvious ringing/spark at the turn-on/off moments of S_P and S_N. As seen from Fig. 5(c) and (d), V_{AC} is not distorted at the mode-changing moments and the previously generated offsets are maintained in CMP_P and CMP_N after 0X mode.

Fig. 6 shows the measured load-transient waveforms of the rectifier when R_L changes between 1 kΩ ($I_L = 4$ mA) and 3 kΩ ($I_L = 1.33$ mA) in both directions. The duty ratio of 2X/0X mode changes, as seen from the signal EN_{OVP}; however, the hysteresis window of V_{DC} keeps less than 50 mV in both transient cases, indicating that the output regulation is robust despite loading variations [6].

Fig. 7 shows the measured PCE, output power (P_{OUT}), and VCR of the rectifier in different loading conditions. The WPT transmitter is tuned to ensure that enough power can be provided. The peak PCE is achieved at 90.6% when P_{OUT} is 79.8 mW. The PCE keeps higher than 86.4% and the VCR keeps higher than 1.6 over the entire measured R_L range from 100 Ω ($I_L = 40$ mA) to 4 kΩ ($I_L = 1$ mA). The maximum P_{OUT} reaches 159.2 mW. The proposed rectifier is further compared with state-of-the-art designs in Table I.

V. Conclusion

A 6.78-MHz single-stage regulating voltage-doubling rectifier is proposed. Based on a full-wave VD, a VCR up to 1.91 is obtained to enhance the WPT system voltage gain. Thanks to the only two

TABLE I
COMPARISON WITH STATE-OF-THE-ART DESIGNS

	This work	TBCAS'20 [2]	SSCL'20 [13]	JSSC'19 [3]	JSSC'15 [5]
Technology	**180nm BCD**	180nm CMOS	180nm CMOS	350nm CMOS	350nm CMOS
Working frequency	**6.78MHz**	1-10MHz	13.56MHz	1MHz	13.56MHz
Chip area	**0.3mm^2 (w/o caps); 2.7mm^2 (w/ caps)**	6mm^2	0.2mm^2	2.4mm^2	3.1mm^2
Topology	**Full-wave VD**	FBR	FBR	CM rectifier/HBR	1X/2X rectifier
Number of PTs	**2**	4	4	5	5
Active diode delay compensation	**Adaptive switched biasing + offset locking**	Adaptive switched biasing	Adaptive input voltage offset	No compensation	Fixed switched biasing
Output regulation	**Hysteresis-based pulse skipping**	PFM+PWM	No regulation	Conduction reverse current	1X/2X mode switching
Output voltage	**4V**	2.5V	1.9V*	3V	3.6V
Output ripple	**48mV (Hyst. defined)**	19.6mV	N/A	100mV*	150mV*
Load regulation	**0.17%**	0.46%	N/A	0.8%	3.1%
Line regulation	**0.37%**	0.48%	N/A	1.8%	N/A
ΔV in load-transient	**Unobservable**	80mV*	N/A	1V	112mV
Maximum P_{OUT}	**159.2mW(R_L=100Ω)**	65mW	7.2mW*	18mW	102mW
VCR	**1.60-1.91 (R_L=100Ω-4kΩ)**	0.86*	0.91	1.4*	1.3*
Peak PCE	**90.6% @79.8mW**	90.7% @32.5mW	90.7% @7.2mW	75% @18mW	92.6% @60mW

*Estimated from the reference

power transistors, the adaptive delay-compensated comparators, the regulation-compatible offset locking technique, and the zero-voltage mode switching, a high PCE is achieved over a large loading range with a peak PCE at 90.6%. The maximum output power is 159.2 mW, which meets the power requirements for most bioimplants. The loading-insensitive sub-50-mV hysteresis output control regulates V_{DC} at 4 V and eliminates the voltage undershoot/overshoot during load transients.

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