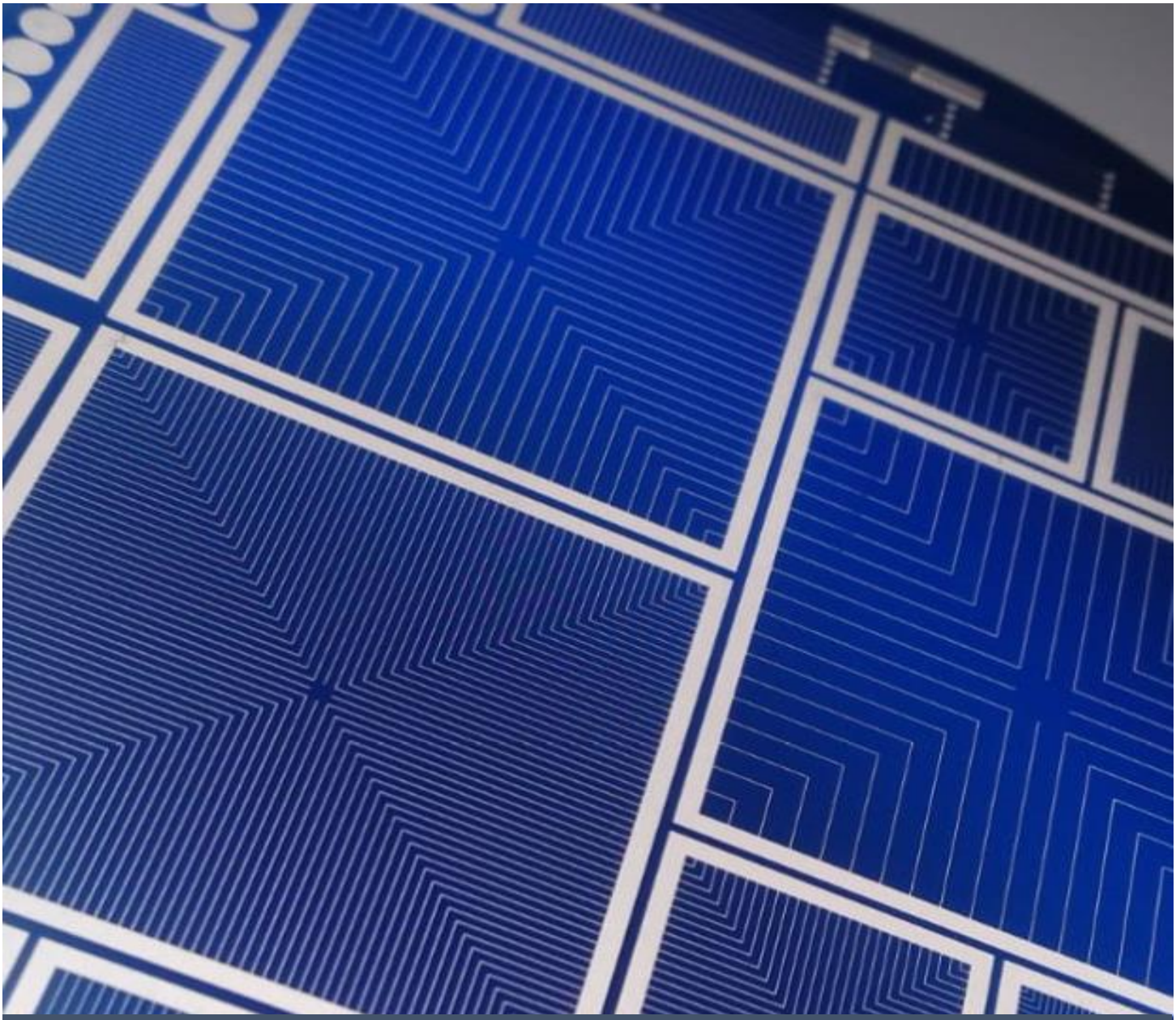

Ultra-thin thermal SiO_x enabled poly-Si carrier selective passivating contacts for IBC solar cell application

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TU Delft 26/08/2020 Master Thesis

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By

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PVMD

Conference Abstract

Development of poly-Si passivating contacts on textured Si surface for bottom c-Si solar cell application - Guangtao Yang, Saravana Kumar Senthil Kumar, Paul Procel, YiFeng Zhao, Can Han, Manvika Singh, Gianluca Limodio, Luana Mazzarella, Arthur Weeber, Miro Zeman, Olindo Isabella – *EUPVSEC 2020 September*

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Abstract

Crystalline silicon solar cells based on poly-Si Tunneling Oxide Passivating Contacts (TOPCon) is becoming one of the most promising solar cell structures that enable both high efficiency and low cost. The record efficiency for the Front-Back contacted (FBC) cell with TOPCon structure is 25.7 %. By moving both the metal contacts to the back side, the so-called interdigitated back contact (IBC) approach, the solar cell efficiency can be improved significantly due to the absence of optical shading from the front metal contact. Further, by narrowing the width of the metal fingers present on the rear side of an IBC solar cell, light illumination can also be made possible from the rear side. This makes the IBC solar cell a bi-facial IBC solar cell. The objective of this thesis work is to optimize the Carrier Selective Passivating Contacts (CSPCs) with an ultra-thin thermal SiO_X.

From the optimization of CSPCs the best passivation effect was achieved for both the p^+ and n^+ CSPCs with the oxide growth condition of 675°C, 3 min. Also, the post-implantation annealing conditions plays an important role in influencing the field-effect passivation provided by the CSPCs. The n^+ poly-Si CSPCs (both flat and textured) and flat p^+ poly-Si CSPC showed better passivation effects when annealed for 2.2 min. The textured p^+ poly-Si CSPC showed better passivation when annealed for 30 s. The influence of the oxidation condition and post-implantation annealing condition on the contact resistivity of the CSPCs were studied by Transfer Length Measurements (TLM).

The study on different hydrogenation processes showed that the performance of the p^+ poly-Si CSPCs can be significantly improved by using a triple capping layer – $AlO_X/SiN_X/AlO_X$ followed by annealing at 650°C for 10 min in Forming Gas atmosphere by RTP (Rapid Thermal processing). By this hydrogenation process the iV_{OC} achieved for the flat and textured p^+ poly-Si CSPCs were 725.3 mV and 711.3 mV respectively, the highest so far achieved in the PVMD group.

Testing the optimized CSPCs in a FBC solar cell structure, the maximum V_{OC} and FF obtained by screen printing of silver are 699.7 mV and 72.2 % respectively. In the future works, these CSPCs are to be tested in IBC and bi-facial IBC solar cell structures.

Contents

Nomenclature

τ_{eff}	Minority Carrier Lifetime
η	Conversion efficiency
ρ_C	Specific Contact resistance
σ_e	Electron Conductivity
σ_h	Hole Conductivity
a-Si	Amorphous Silicon
Ag	Silver
Al	Aluminium
AlO_X	Aluminium Oxide
AM	Air Mass
ALD	Atomic Layer Deposition
ARC	Anti-reflection Coating
B	Boron
BHF	Buffer Hydrofluoric Acid
c-Si	Crystalline Silicon
CSPC	Carrier Selective Passivating Contacts
E_g	Bandgap
E_C	Conduction Band
E_V	Valance Band
ECV	Electrochemical Capacitance Voltage
FBC	Front and Back Contacted
FF	Fill Factor
FG	Forming Gas
FGA	Forming Gas Annealing
FZ	Float Zone
HF	Hydrofluoric Acid
HNO_3	Nitric Acid
iV_{OC}	Implied open-circuit voltage
IBC	Interdigitated Back Contact

IPA	Isopropyl Alcohol
ITO	Indium Tin Oxide
J_0	Recombination Current Density
J_{SC}	Short-circuit Current density
LPCVD	Low Pressure Chemical Vapour Deposition
NAOS	Nitric Acid Oxidation of Silicon
N_2	Nitrogen
O_2	Oxygen
P	Phosphorous
Poly-Si	Polycrystalline Silicon
PECVD	Plasma Enhanced Chemical Layer Deposition
PVD	Physical Vapour Deposition
PV	Photovoltaics
QSS	Quasi-steady state
RTP	Rapid Thermal Processing
R_s	Series Resistance
R_{shunt}	Shunt Resistance
S_{10}	Logarithmic Selectivity
SEM	Scanning Electron Microscopy
SP	Screen Printing
SQ	Shockley-Queisser
SRH	Shockley-Read-Hall
STC	Standard Test Conditions
SiH_4	Silane
SiN_X	Silicon Nitride
SiO_X	Silicon Oxide
t-SiO_X	Thermal Silicon Oxide
TCO	Transparent Conducting Oxide
TEM	Transmission Electron Microscopy
TEOS	Tetraethyl orthosilicate
TLM	Transfer Length Measurements

TMAH	Tetramethylammonium Hydroxide
TMA	Trimethyl Aluminium
V_{OC}	Open-Circuit Voltage

1 Introduction

"We are like tenant farmers chopping down the fence around our house for fuel when we should be using Natures inexhaustible sources of energy – sun, wind and tide. … I'd put my money on the sun and solar energy. What a source of power! I hope we don't have to wait until oil and coal run out before we tackle that."

-THOMAS EDISON

The need for clean energy has become one of the prime importance in the recent years. The International Energy Agency (IEA) foresees a sustainable development scenario in which the global electricity demand increases at a rate of 2.1 % till the year 2040. This rate is twice the rate at which the primary energy demand increases [1]. The increase in clean energy needs have accelerated the use of solar energy in the recent year both in large and small scale systems. Fraunhofer Institute for Solar Energy Systems, ISE has come up with the trend in Global Annual Production (GWp) from the global photovoltaic (PV) installations. As of 2019, this value is at 140 GWp and has seen an increasing trend in the last decade [2].

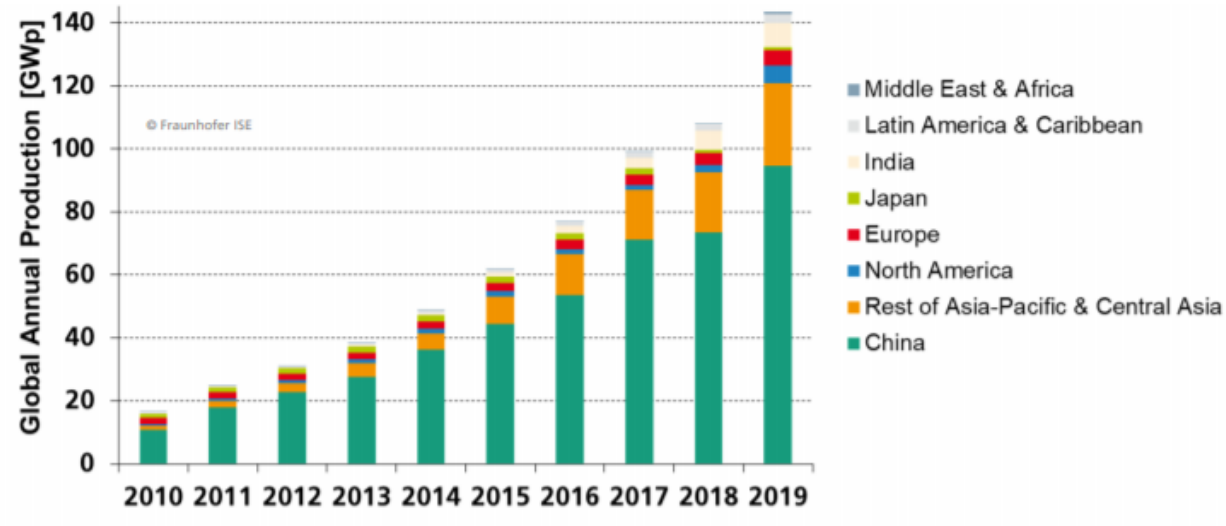


Figure 1.1 Global Annual Production (GWp) with regional contribution [2].

In the year 1839, Alexandre Edmond Becquerel discovered the photovoltaic effect. As per photovoltaic effect, when a photovoltaic cell is exposed to sun light it generates voltage or electric current within it. In 1954, Daryl Chapin, Calvin Fuller, and Gerald Pearson developed the first silicon PV cell, with an efficiency of 4 % at Bell Labs [3]. Right from its discovery the silicon based solar cells have ruled the solar energy market. The silicon solar cell market in the beginning years was dominated by multi crystalline solar cells and in the recent years the mono-crystalline silicon solar cells dominates the market and it can be clearly seen in the Figure 1.2. This change in trend has taking place in the recent 3 years.

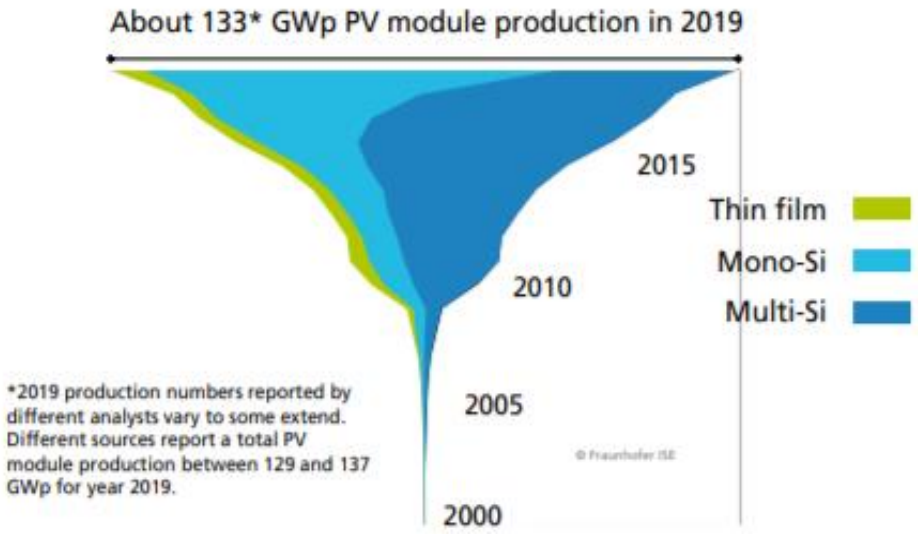


Figure 1.2 Annual PV Production by Technology [2].

In the current situation, the mono-crystalline PV technology dominated the PV market with an annual production of 89.7 GWp. This is followed by the multi-crystalline PV technology with an annual production of 39.6 GWp. The thin film technologies contribute to an annual production of 7.5 GWp. At present the highest efficiency achieved by mono-crystalline base PV technology is at 26.3 % by Photovoltaic & Thin Film Device Research Laboratories, Kaneka corporation [4]. The type of solar cells is a silicon heterojunction with interdigitated back contacts (IBC). One such similar mono-crystalline technology is with poly-Si (multi-crystalline Silicon) based carrier selective passivating contacts with interdigitated back contacts. The main goal of the thesis work is to optimise the poly-Si based carrier selective contacts enabled by ultra-thin thermal silicon oxide, which can be deployed in IBC and bi-facial IBC solar cell applications.

1.1 Working principle of a solar cell

The working of the solar cell is based on the photovoltaic effect. The energy of the photon, E = hv is converted into chemical energy when absorbed by a semiconductor material, by the formation of an electron-hole pair. The working principle is better understood in three steps as follows

Generation of charge carriers – When a photon of desired energy is absorbed in a semiconductor material, the electron in the valance band gets excited to the conduction band. This leaves a positive void in the valance band known as holes. Thus, an electron-hole pair is generated within the material. The difference between the valance band (E_V) and conduction band (E_C) gives the band gap (E_g) of the material. For instance, the E_g for crystalline silicon is 1.12 eV.

Separation of charge carriers – The generated charge carriers tend to recombine if not separated. The separation of the electron-hole pair is done with the help of a p-n junction in a solar cell. Such a junction is formed when a p-type and n-type semiconductors are brought into contact.

Collection of charge carriers – To perform electric work in the external circuit, these separated charge carriers has to be extracted from the semiconductor material. The electrons are collected at the n-side, passes through the external circuit to perform electric work and then recombines with the holes at the metal and p-side interface.

The simple working of a solar cell is depicted in Figure 1.3

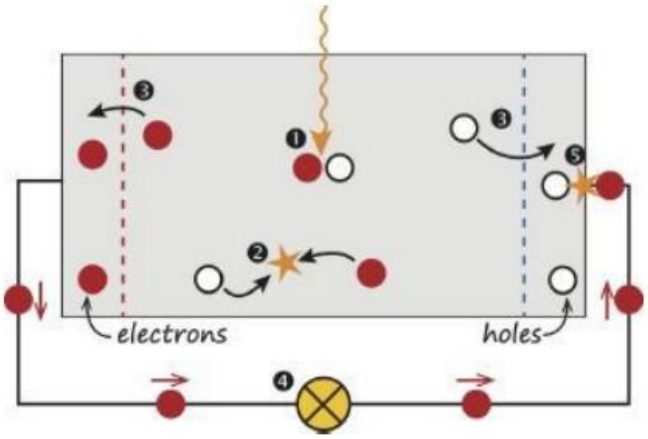


Figure 1.3 Solar cell model. 1. Generation of charge carriers 2. Recombination of charge carriers 3. Separation of charge carriers 4. Electrons passing through the external circuit 5. Recombination of electron-hole pair [5].

1.2 Loss Mechanisms

Not all the photons reaching the solar cell helps in the creation of electron-hole pair and not all the electron-hole pair generated are collected in the solar cells. These losses can be classified as optical and losses. Apart from these losses, there is spectral mismatch in case of a single junction solar cell.

1.2.1 Spectral Mismatch

The spectral mismatch takes into account of two important losses that pulls down the efficiency of a single junction solar cell. They are non-absorption of low energy photons and thermalisation by high energy photons

Non-absorption – The photons with energy less than the band gap of semiconductor are not absorbed and henceforth do not contribute to charge carrier generation. Such low energy photons just traverse the absorber material.

Thermalization – On the other hand, photons with energy greater than the band gap of semiconductor, do produce electron-hole pair and the excess remaining energy of the photon is released within the semiconductor material as heat.

1.2.2 Optical Losses

Different forms of optical losses take places within the solar cells. The main optical losses are refection loss, shading loss and parasitic absorption.

Reflection losses – Crystalline silicon, when polished is highly reflective. The reflection losses can be reduced to a great extent by texturing the surface. An insight of texturing is given in section 2.1.2. Also, the reflection losses can be reduced by using anti-reflection coating (ARC) layers such as Silicon nitride or by using a transparent conducting oxide (TCO) layer.

Shading losses – The front metallisation of the solar cell shades the absorber from the incident radiation. Therefore, the design of the front metal is so crucial that the width has to be as low as possible to reduce shading . This loss can be completely eliminated by the IBC solar cell architecture, in which both the metal contacts are on the rear side of the solar cell.

Parasitic absorption – Any undesirable absorption of photon in layers other than the photo-absorber layer, do not contribute in charge carrier generation. This leads to the so called

parasitic absorption. As a result, the layers such as the TCO and ARC has to be kept as thin as possible.

1.2.3 Electrical Losses

Electrical losses are experienced within the absorber material, even before the electrons flow in the external circuit. This can be attributed to the recombination of the generated charge carriers before being collected at the metal electrode. These losses due to recombination are classified into three main forms namely, radiative recombination, Shockley-Read-Hall (SRH) recombination and Auger recombination. The defect states on the surface of the bulk also leads to surface recombination losses. Also, there is resistive losses experienced by charge carriers within the device along its flow.

Radiative recombination – This can be realised as the inverse process of charge carrier generation. The generated electron-hole pairs recombine by giving out energy in the form of a photon This type of recombination is dominant is a direct band gap material. In case of an indirect band gap material like silicon, an additional photon is required for such recombination to occur. So, silicon based solar cells are not prone to radiative recombination.

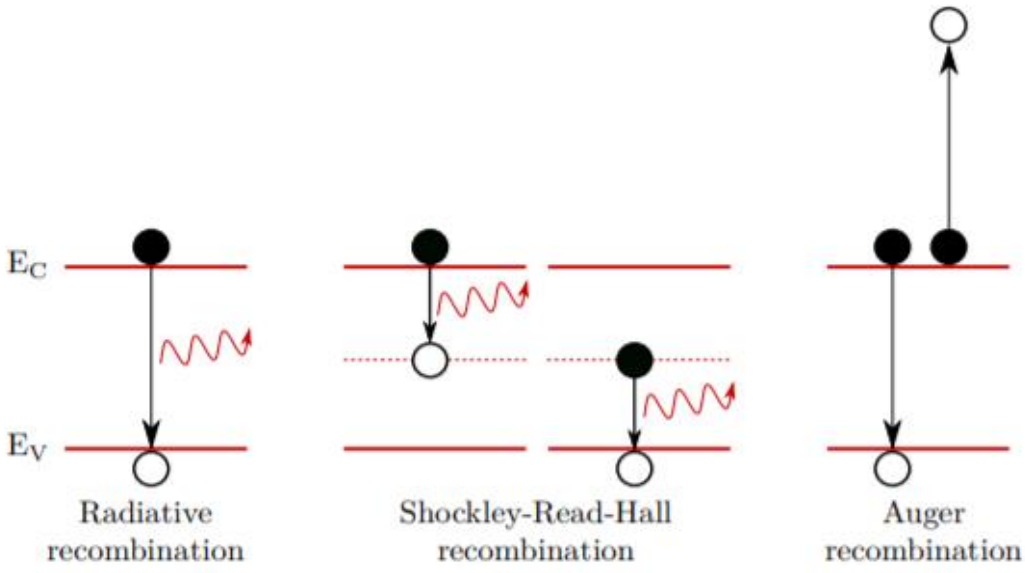


Figure 1.4 Schematic of recombination mechanism [6].

SRH recombination – This occurs due to the relaxation of charge carried via intermediate energy states between the valance band and conduction band. These intermediate energy states arise dur to the defects within the crystal lattice. The charge carrier gets trapped within

these defect states and easily undergo recombination. Poly-crystalline silicon suffers much from SRH recombination compared to mono-crystalline silicon, because of the increased defect states at the grain boundary.

Auger recombination – This type of recombination is dominant in an indirect bandgap material such as silicon. An electron-hole pair recombine by giving its energy to a third charge carrier. This third charge particle is thus excited to a higher energy state and later relaxes back to the band edge by thermalisation. This type of recombination increased with the increase in doping concentrations.

Surface recombination – The dangling bond on the surface of the material can act as defect states. These defect states then trap the charge carriers and later facilitates recombination. It can be reduced by means of chemical passivation of surfaces.

Resistive losses – Different layers within the solar cells exerts different resistance to the charge carriers on its way to the metal electrodes. This can be understood as the series resistance experienced by the charge carriers. This value has to be as low as possible for the better charge carrier collection at the electrodes. On the other hand, the shunt resistance has to be as high as possible, to minimise the leakage currents.

1.3 Shockley-Queisser (SQ) limit

The theoretical maximum limit of a single junction solar cell can be realised as the Shockley-Queisser limit. The maximum efficiency that can be achieved in AM1.5 spectrum is 33.1% for a band gap of 1.43 eV [5]. Figure 1.5 shows the loss mechanisms which pulls the efficiency down to the SQ limit as a function of increasing the band gap. The major losses include the non-absorption of photons below the band gap of the material, thermalisation losses, voltage losses and so on. These limits are overcome with the advent of multi-junction solar cells with better bandgap utilisation and spectral utilisation.

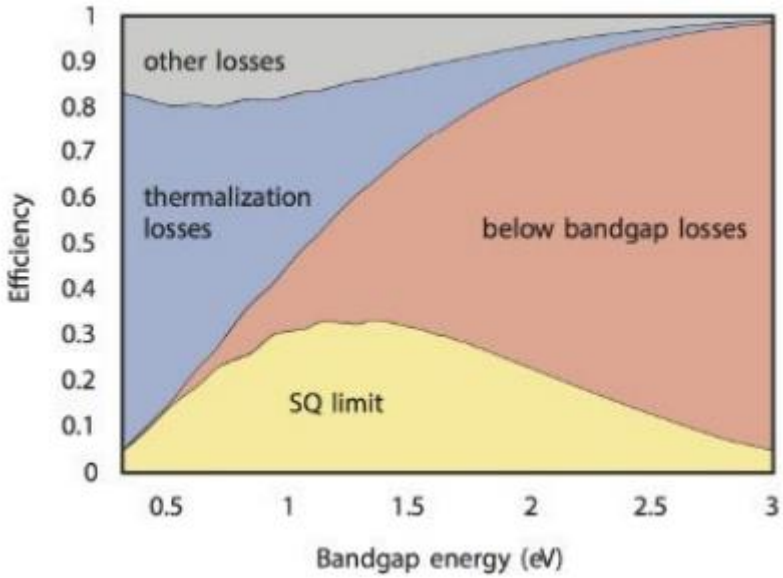


Figure 1.5 SQ limit along with the major losses for AM1.5 spectrum [5].

1.4 External solar cell parameters

The external solar cell parameters help in characterising the performance of the solar cell. Such parameters namely open-circuit voltage (V_{OC}), short circuit current density (J_{SC}), fill factor (FF) and conversion efficiency (η) are explained in this section.

1.4.1 Standard test conditions

To have a standard in measuring the solar cell performance throughout the world the Standard Test Conditions (STC) are followed. The STC conditions are as follows, the total irradiance on the solar cell has to be 1000 W/m^2 with the irradiation spectrum same as that of AM1.5 spectrum. The temperature of the solar cell during measurement has to be at 25°C.

1.4.2 Short circuit Current density

It is the maximum current density that is delivered by the solar cells. The short circuit current, I_{SC} is the maximum current given by the device at zero voltage. To eliminate the dependence of the area in measurement, Short circuit current density, J_{SC} is used. It depends directly on the photon flux incident on the solar cell and the optical properties of the solar cell.

1.4.3 Open circuit voltage

It is the maximum voltage that can be delivered by the solar cell, when no current flows through the external circuit. It depends on the photo generated current density, J_{ph}. The open circuit voltage (V_{OC}) is calculated from Equation 1.1.

$$V_{OC} = \frac{k_B.T}{q} \ln\left(\frac{J_{ph}}{J_0}\right) \quad 1.1$$

1.4.4 Fill factor

Fill factor (FF) can be defined as the ratio of maximum power generated by the solar cell, P_{max} to the product of open circuit voltage and short circuit current. It can be calculated by the Equation 1.2.

$$FF = \frac{P_{max}}{J_{SC}.V_{OC}} \quad 1.2$$

1.4.5 Conversion efficiency

The conversion efficiency of the solar cell can be defined as the ration of maximum power generated by the solar cell to the incident power, P_{in} . Since, the solar cells are measured under STC conditions, P_{in} value equals to 1000 W/m^2. The efficiency of the solar cell can thus be calculated by Equation 1.3.

$$\eta = \frac{P_{max}}{P_{in}} = \frac{J_{SC}.V_{OC}.FF}{P_{in}} \quad 1.2$$

1.5 Surface passivation

As mentioned in section 1.2.3, Surface recombination is one of the main losses experience by the c-Si solar cells. This can be overcome by two techniques namely chemical passivation and field-effect passivation. A combination of these two techniques helps in creating a carrier selective passivating contact – CSPC. The working behind these two techniques are discussed in the following sub-sections.

1.5.1 Chemical Passivation

As discussed earlier, the surface defects arising due to the presence of dangling bonds behave as centres for SRH recombination to occur. The defect densities can be reduced by have a thin layer of suitable material which forms covalent bonds with the surface atoms. The most commonly used passivating layer is SiO_X. It can be seen from the Figure 1.6, that the SiO_X layer do not completely passivate all the trap states. Thus, an addition step helps in increasing the surface passivation. This can be done by the process of hydrogenation.

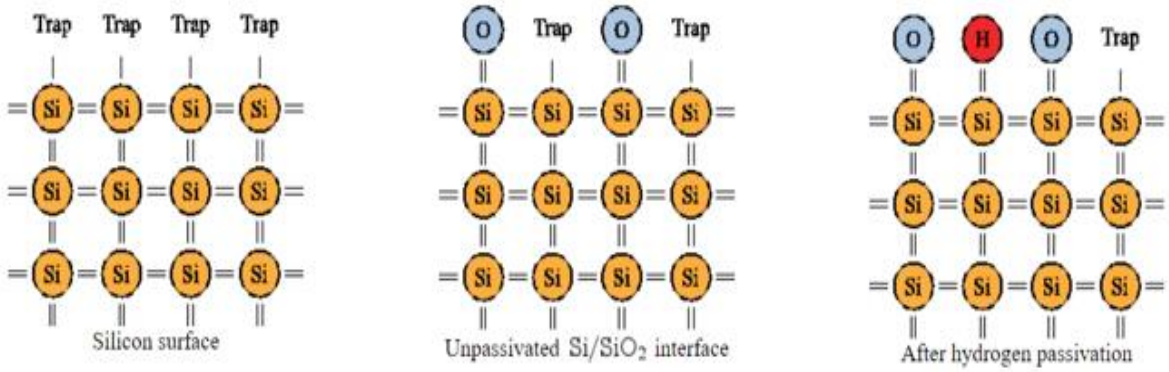


Figure 1.6 Chemical passivation by silicon oxide and hydrogen atoms [7].

Hydrogenation – The process of saturating the dangling bonds with the help of hydrogen atoms is called hydrogenation. When annealed in a hydrogen rich atmosphere, the defects states which were not passivated by the SiO_X layer is passivated with the help of hydrogen atoms. This process is explained and studied in detail in Chapter 4 of this thesis work.

1.5.2 Field-effect passivation

Field-effect passivation is done by introducing a heavily doped region above the base. This creates an electric field suitable to collect the particular charge carrier and repel the other, thus minising the recombination at the surface. This concept is same as that applied in a back surface field of a solar cell. The band diagram of s back surface field is as shown in Figure 1.7. The p / p^+ interface behaves like a p-n junction repeling the electrons and leading to high hole densities in the p-doped region.

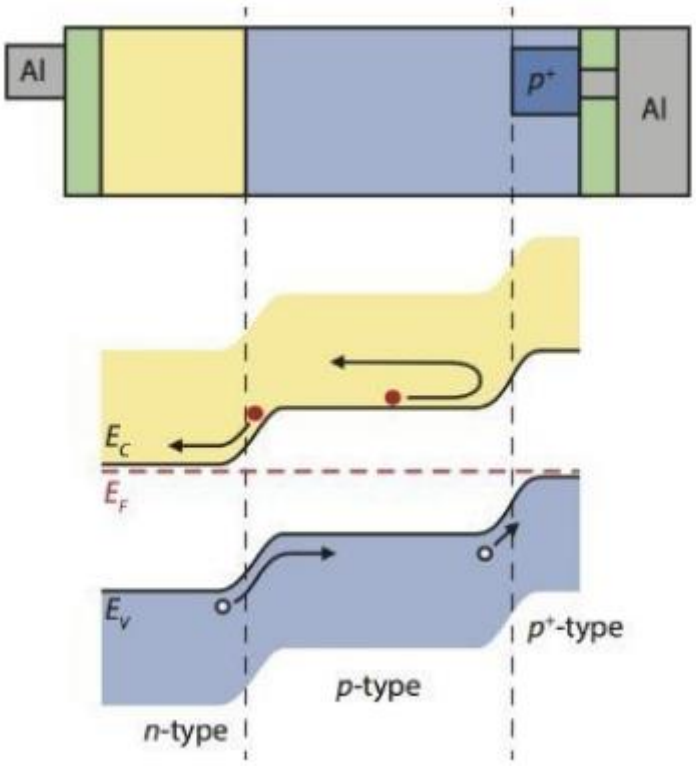


Figure 1.7 Band diagram of a back surface field [5].

1.6 IBC solar cells

The prime importance of using an IBC structure is because of its no shading loss by metallisation on the front side. In such a sell architecture there is no one complete p-n junction. Rather there are many localized junctions. Figure 1.8 shows the architecture of an IBC solar cells with an n-type bulk. The holes are separated at the p^+ / n-bulk junction and the electrons are collected at the n^+ / n-bulk interface. Two metal grids are used to collect the hole and electrons. The contact of the metal with the heavily doped interface is kept as small as possible to minimise recombination. The metal contacts can be made wider than used in FBC structure because of no metal shading losses in the front. Thus, the resistivity of the metal decreases. The wide of the metal is also kept at the optimal, for applications such as a bi-facial IBC solar cell, which can receive illumination from both the sides of the cell.

For the n-type bulk, a heavily doped n^+ layer is deposited on the front side, which acts a front-surface field, repelling the minority holes back towards the bulk. Refection losses are reduced with the help of an anti-reflection coating.

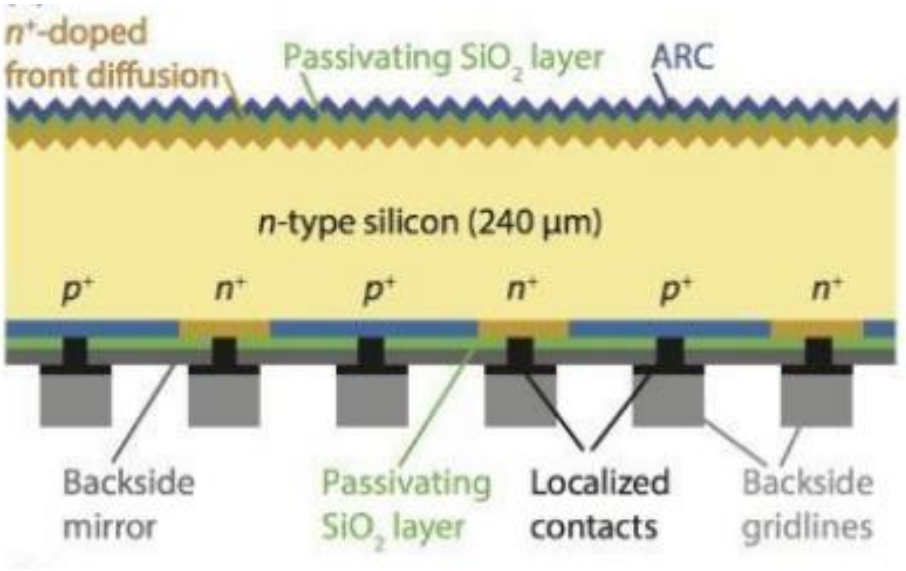
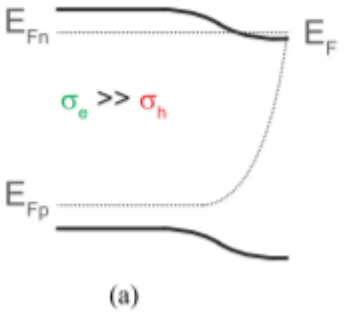


Figure 1.8 IBC solar cell architecture [5].

1.7 Carrier selective passivating contacts

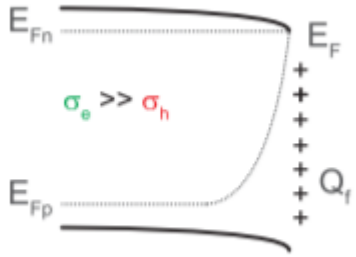
Carrier selective passivating contacts (CSPC) has two functionalities. As the name suggests, they behave both as a contact and serves as a passivation layer [8]. In such a layer, the conductivity of one of the charge carriers is larger than that of the other. If there is a similar conductivity for both the charge carriers then the probability of recombination increases. Two main parameters which are helpful in studying the carrier selectivity are the recombination current density, J_0 and contact resistivity, ρ_C [8]. These values have to be as low as possible to get better passivation and carrier selectivity. These two parameters are interrelated to each other because of their mutual dependence on the conductivity of the charge carriers. In order to maintain a low J_0 and ρ_C values , the conductivity of the majority carriers should be high compared to that of the minority charge carriers. The difference in conductivity between the charge carriers makes it selective to a particular charge carrier. The effect of these parameters is studied in detail in Chapter 3 of this thesis.

The carrier selectivity can be achieved by many ways and an overview study is carried out by Jimmy Melskens et al. The summery of the review on electron selectivity is presented in this section.



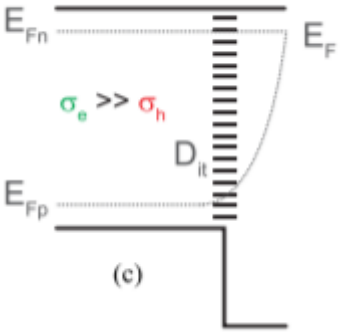
(a)

Here, the electron selectivity is achieved by introducing heavy n^+ doping adjacent to the n-layer. The working is the same as front surface field introduced in Figure 1.8. Similar effect can also be achieved for hole selectivity as shown in Figure 1.7



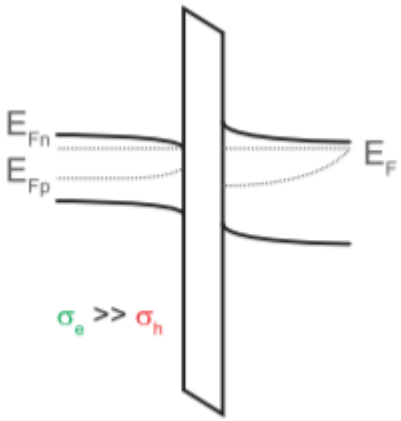
(b)

An external potential source or a layer with a large fixed charge capacity (Q_f) is introduced to change the surface carrier concentration. Here a high surface charge concentration of electrons is achieved by having a layer with high fixed positive charges.



(c)

A heterojunction is formed between c-Si and a wider bandgap material. Here there is a proper alignment of the conduction bands to facilitate electron selectivity. In reality, this is not the case and we have to try keeping the off-set between the conduction band (in case of electron selectivity) sufficiently small, with fermi level alignment.



(d)

A tunnel layer, ultra-thin SiO_X layer is introduced between the n and a heavily doped n^+ layer, which has an asymmetric probability of the electrons and holes to tunnel through. The SiO_X layer provides better tunnelling for electrons compared to that of holes. This type of CSPCs are used in this thesis work with thermal SiO_X enabled by poly-Si.

1.8 Tunnelling oxide deposition

The tunnelling oxide layer is an important layer in a CSPC. It has to be at its right thickness to let the charge carrier tunnel through it. Thin tunnelling SiOx layers also finds application in the field of micro-electronics such as CMOS (Complementary metal–oxide–semiconductor) and MOSFET (metal-oxide-semiconductor field effect transistor). There are various methods through which such thin tunnelling oxides are grown or deposited. Some of the methods are explained below.

NAOS – Nitric acid oxidation of silicon, it a wet chemical process in which the silicon wafer is immersed in nitric acid. Nitric acid reacts with Si to from silicon oxide. This can also be carried out with vapour of nitric acid [9]. Usually, the reaction rate can be controlled by changing the temperature. In PVMD group, NAOS is carried out under room temperature.

PECVD with TEOS – TEOS is Tetraethyl orthosilicate, which is used as the precursor along with water to deposit SiO_X layer by means of plasma enhanced chemical vapour deposition.

Thermal Oxidation – It takes place in a furnace in an oxygen atmosphere with or without the presence of water. The reaction which takes place in the absence of water vapour is called dry oxidation and gives a high quality oxide compared to the other. The thermal oxidation is explained in detail in Section 2.1.5.

In this thesis work, dry thermal oxidation is used to grow the tunnelling oxide layer for the carrier selective contacts. The main advantage is that oxide from dry thermal oxidation is more uniform and we can have better control over the oxidation rate by changing the oxygen flow rate, oxidation temperature and time. Also, there is no need for any wet chemical process, which making the fabrication step simplified.

1.9 Research goals

There are three main objectives in this thesis work,

- Optimising the poly-Si based carrier selective passivating contacts assisted by ultra-thin oxide layer grown by dry thermal oxidation for four different types of contacts namely flat and textured n^+ poly-Si CSPCs , and flat and textured p^+ poly-Si CSPCs.
- Finding suitable hydrogenation step for increasing the chemical passivation of all the four different CSPCs.

- Testing the optimised CSPCs in a Front Back Contacted solar cell structure.

These findings will be helpful for the future research work in achieving high efficiency IBC solar cells enabled by poly-Si CSPCs.

1.10 Outline

The thesis repost consists of 6 main chapters. Chapter 2 deals with the different experimental and characterisation set-ups and their working principle. In Chapter 3, the experimental results on optimising the carrier selective passivating contacts are presented. In Chapter 4, results of different hydrogenation processes for the CSPCs are presented. These optimised results are tested in a FBC solar cell structure in Chapter 5. Finally, the report concludes with Chapter 6 summarising the results and finds with outlook for the future research.

2 Experimentation

This chapter consists of two main sections namely, fabrication and measurement. Firstly, in the fabrication steps all the equipment and its working principle behind its functioning are explained in detail. Also, the fixed parameters that are used during the time of experiments are mentioned. Secondly, how the measurements are done with the help of the characterisation equipment are discussed.

2.1 Fabrication

In this section the different fabrication processes involved in the fabrication of the solar cells are explained in a sequential order starting from the wafer texturing and clean to the metallisation processes. These methods are also applicable for the fabrication of the symmetric samples which are used in studying the carrier selectivity and the passivation quality during the hydrogenation processes.

2.1.1 Wafer specifications

In this thesis work both the n and p doped c-Si (crystalline-Silicon) wafers were used. The properties of the wafers are as mentioned in Table 2.1. The n-type wafers are used in optimising the Carrier Selective Passivating Contacts (CSPCs), hydrogenation process and in making the solar cells. The only place where a p-type wafer was used is during the measurement of the contact resistivity of the p^+ poly-Si CSPCs to avoid the formation of a p-n junction [10].

Table 2.1 Specification of the silicon wafers used in the thesis work

Specifications	**n-type**	**p-type**
Diameter (mm)	99.8 - 100.2	99.7 – 100.3
Method	Float Zone	Float Zone
Dopant	Phosphorous	Boron
Thickness (µm)	260 - 300	255 - 305
Orientation	<100> ± 1°	<100> ± 1°
Resistivity (Ω.cm)	1 - 5	1 - 5

Also, the two main reasons for choosing a n-type bulk for the experimentation are as follows. Firstly, the n-type wafers are less susceptible to the light induced degradation compared to the p-type wafers. Secondly, the n-type wafers are less sensitive to the Fe (iron) impurities, which leads to low cost wafers in terms of purification [5], [11].

2.1.2 Texturing

Texturing helps in increasing the light absorption of the solar device [5], . This done by etching in a strong alkaline solution. When the silicon surface comes in contact with the alkaline solution the crystal lattice orientation <100> experiences etching rate 50 times higher than that of <111> plane [12]. The etching rate of the <100> plane on the surface of the bulk is removed at a higher etching rate leaving behind the <111> facets . These facets on inspection under a Scanning Electron Microscope (SEM) appears as tiny pyramids as shown in Figure 2.1. The alkaline solution used in this thesis work is prepared by a mixture of water and Tetramethylammonium hydroxide (TMAH) in the ratio 4:1 and an addition solution ALKA_TEX of 120 ml is added and maintained at 80°C. Texturing is carried out until the is no reflection from the surface for about 10 min. This process gives pyramids with height ranging between 2 – 6 µm.

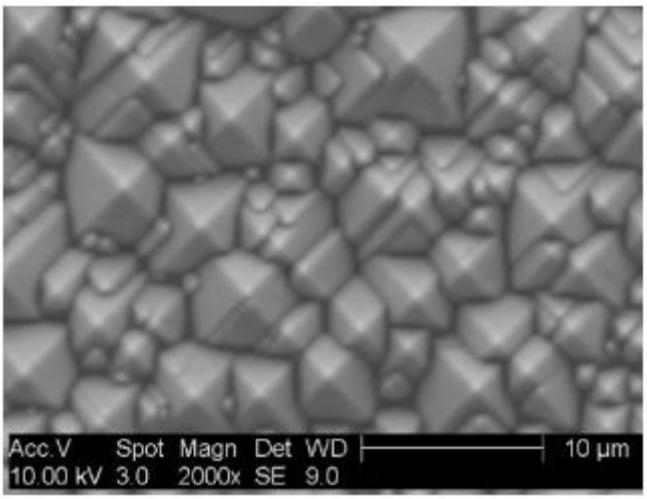


Figure 2.1 Textured c-Si surface under SEM *[13]*.

Also, the textured surfaces consist of shape pyramidal tips which acts as the defect states. To reduce the defect states chemical smoothening of the pyramids is carried out. In most research groups it is done in a solution mixture of HF: HNO_3:CH_3COOH = 1:3:3 [14]. In this

thesis, the chemical smoothening is performed by etching in a mixture of HNO_3 / 40% HF, for 2 min. A constant circulation of the solution is maintained to make the reaction uniform.

2.1.3 Standard Cleaning

The cleaning is done in during the fabrication processes whenever necessary. The standard cleaning procedure followed by the Else Kooi Laboratory (EKL) consist of two rounds of acid cleaning steps. Initially, the wafers are immersed in fuming HNO_3 – 99% for 10 min. Then the wafers are rinsed thoroughly in DI water (deionised water). Next, the wafers are immersed in boiling HNO_3 – 69.5% at 110°C for 10 min. Finally, the wafers are rinsed thoroughly in DI wafer and dried in a Spin Rinse Dryer (SRD).

2.1.4 Marangoni cleaning and drying

A native oxide is always formed on the surface of the wafer even when kept in the clean room atmosphere. A very porous native oxide of 2 nm thick is always encountered in the EKL. This native oxide has to be removed before the deposition of the t-SiO_X and is done by Marangoni cleaning and drying step. This is done by immersing the samples in a bath containing 0.55% HF for 4 min. The thorough removal of the sample can be visually inspected as the pure Si surface is hydrophobic. Then the HF bath is flushed with DI wafer to remove the acid. Then the immersed wafers are pulled out from water slowly and dried with jets of IPA (Isopropyl Alcohol). The name Marangoni comes from the principle behind drying. A feeble force acts between the upper and lower meniscus of the liquid due to the difference in the surface tension. This force is called the Marangoni force, which helps in drying the wafers. The schematic of the process is as shown in Figure 2.2

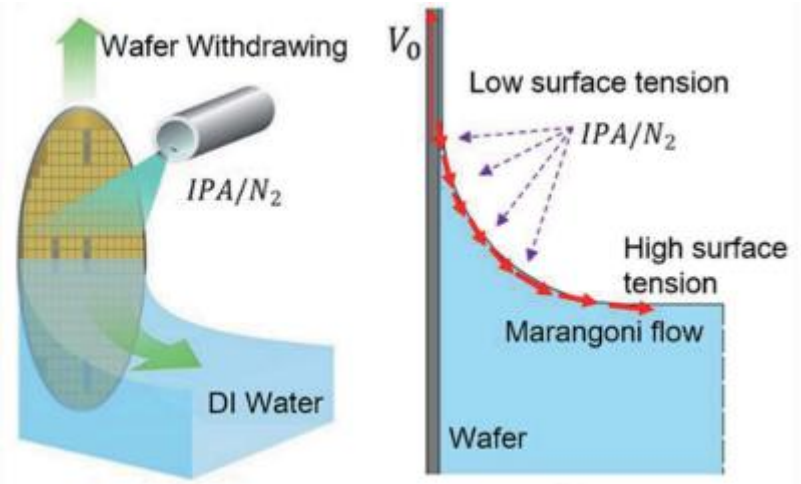


Figure 2.2 Marangoni Drying of the wafers and its working mechanism *[15]*.

2.1.5 Thermal Oxide Growth

The tunnel oxide layer needed for the formation of the carrier selective layer is carried out by dry thermal oxidation of silicon. The silicon layer when comes in contact with an oxygen atmosphere at a temperatures between 750 – 1100°C forms Silicon Oxide [16], [17]. This reaction happens as shown in equation 2.1. The temperature and time of the process plays an important role in determining the thickness of the silicon layer formed. There is an increase in the volume of the silicon surface as it gets oxidised due to the incorporation of oxygen within the surface. The electrical resistivity and the band gap of a dry thermal silicon oxide is around 1 e20 Ω.cm and 9 eV respectively [16].

$$Si\ (s) + O_2\ (g) \rightarrow SiO_2\ (s) \qquad 2.1$$

In this thesis work the thermal oxidation of silicon is carried out in a Tempress Systems furnace as follows. Initially, the chamber is filled with N_2 gas with a constant flow of 6 SLM. This helps in removing undesired gases within the reaction zone such as water vapour. The required oxidation time and temperature is given as an input. Then the temperature of the reaction zone is ramped up at a rate of 10°C/min. When the set temperature is reached along with the nitrogen flow 0.6 SLM of oxygen is added, which starts reacting with the silicon surface. Once the oxidation is done, the oxygen flow is cut, and the temperature is ramped down. This process is immediately proceeded with the next step of a-Si deposition by LPCVD to prevent any addition growth of any oxide layer.

2.1.6 Low Pressure Chemical Vapour Deposition

The a-Si deposition is carried out by LPCVD in a horizontal reactor by Tempress Systems. The schematic of the furnace is as shown in figure 2.3. The wafers are placed in a low pressure chamber. Then the reaction gases are fed into the chamber at a constant flow rate. After the end of the reaction the product gases are purged out.

For a-Si deposition the precursor gas used in silane (SiH_4). The pressure of the chamber is maintained at 150 mTorr. The flow rate of silane is kept constant at 45 sccm during the a-Si deposition under low pressure. The temperature of the chamber is kept at 580°C. By these set parameters the deposition rate of a-Si takes place at 2.2 nm/min. The thickness of the a-

Si deposited is controlled by the processing time. For instance, on a flat surface to deposit 250 nm of a-Si a deposition time of 113 min is required.

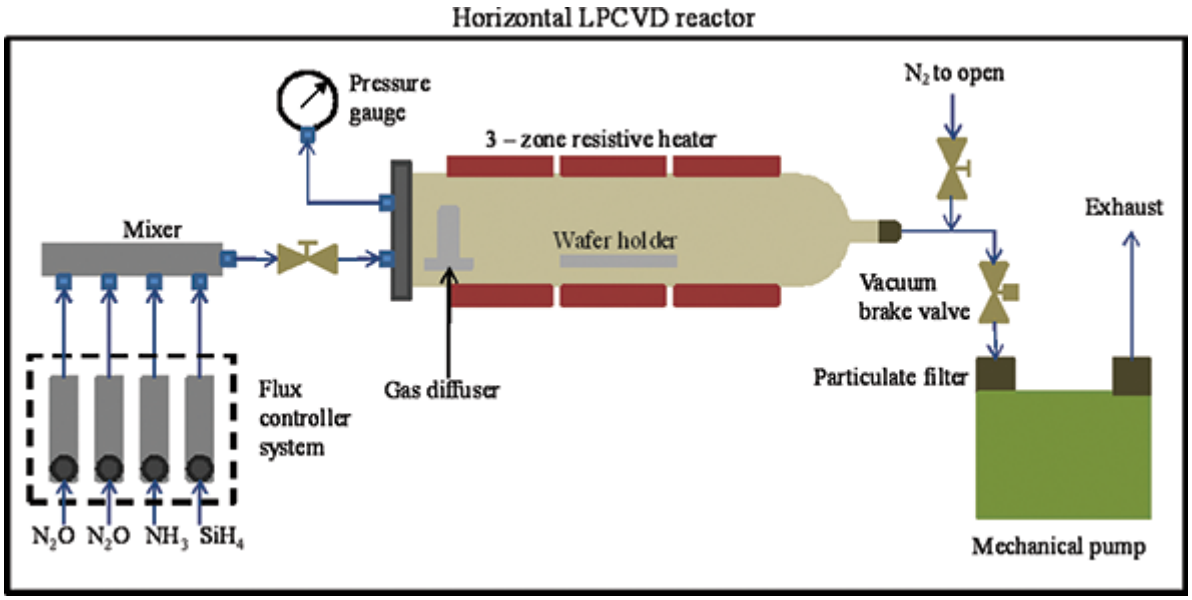


Figure 2.3 Schematic of a LPCVD reactor [18].

A post-deposition annealing is done within the furnace at a temperature of 600°C for 60 min to relieve the thermal stress incurred within the sample. After the deposition of the intrinsic amorphous layer, ion implantation is done as a means of doping.

2.1.7 Ion Implantation

The dopants used for creating the n^+ and p^+ poly-Si layer in this thesis are Phosphorous and Boron respectively. The a-Si layer is doped by using the Varian ion implanter. The schematic of such an implanter is shown in Figure 2.4. The dopant ions are created with the help of a plasma and are guided towards the accelerator with the help of a magnetic field. Before entering into the acceleration column, the ions are filtered by using a mass separation slot, which allows only the desired doping ion to pass through. Then the ion beams are focussed onto the target with the help of magnetic lenses. The depth to which the ions has to reach within the substrate can be changed by adjusting the implantation energy and ion dosage. This implantation process has to be followed by an annealing step within the temperature range 600 – 1100°C to activate the dopants. In our case, this annealing process also helps in the phase transition of a-Si to poly-Si. The influence of the post-implantation annealing conditions is explained in detail in Section 3.1.5.

The ion dosage and energy used in the thesis work are mention in Table 2.2. For the textured samples different ion dosages are studied within the thesis work.

Table 2.1 Ion implantation parameters.

Specifications	n-type	p-type
Dopant gas	PH_3	BF_3
Dopant	Phosphorous	Boron
Dosage (ions/cm^2) - flat	6 e15	5 e15
Energy (keV)	20	5
Pressure (Torr)	3.10	2.30

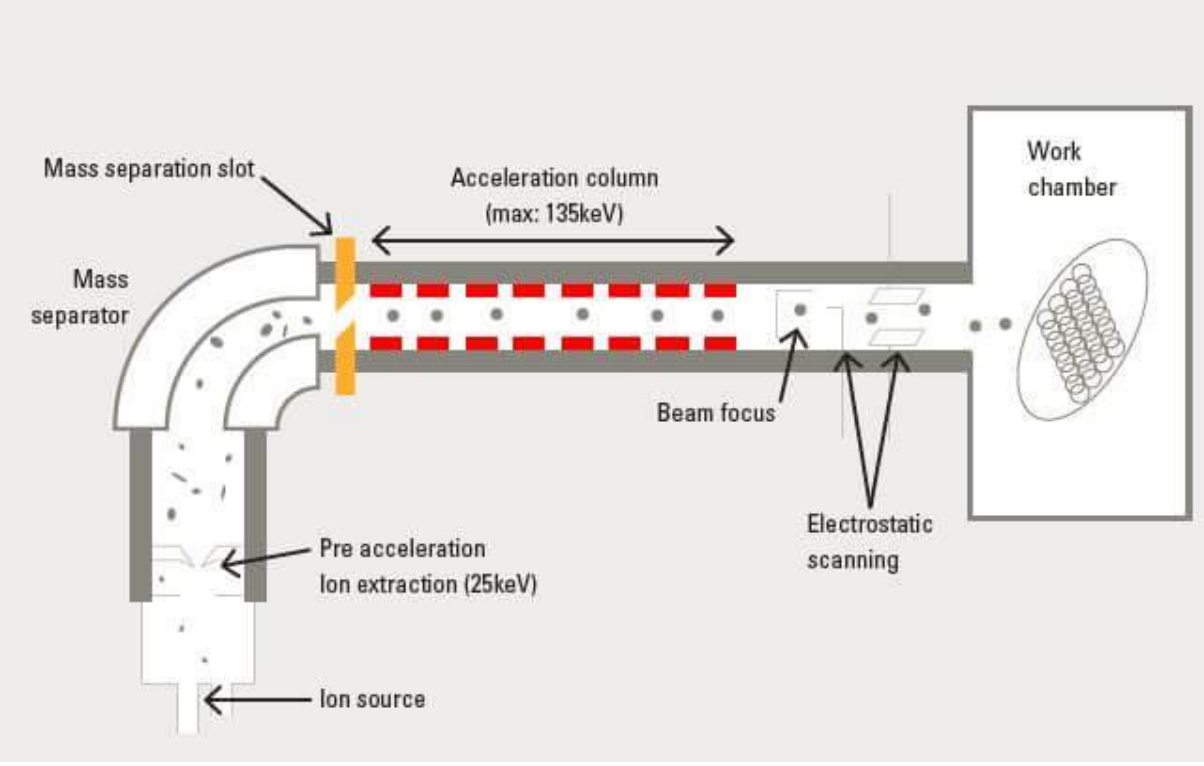


Figure 2.4 Schematic of a Varian ion implanter [19].

2.1.8 Annealing

Annealing is an important step used in a wide variety of application in the field of solar cell fabrication. In this thesis work is annealing is carried out at many stages throughout the fabrication of the solar cell.

Firstly, annealing is performed after ion implantation for the purpose of activating the dopants and converting a-Si into poly-Si [20], [21], [22]. This annealing is carried out in a Tempress furnace. The implanted samples are placed inside the furnace and annealing is carried out in high temperatures between 900 – 950°C for different time intervals. The annealing atmosphere is a mixture of nitrogen and oxygen with flow rates 6 and 1 SLM respectively. After annealing is done the gases are purged out and the samples are allowed to cool.

Secondly, annealing is carried out in Forming Gas, mixture of Nitrogen and Hydrogen in the ratio 10:1, atmosphere. The purpose of this annealing is to increase the chemical passivation of the CSPCs and is explained in detail in Chapter 4. This annealing process is called hydrogenation. It is also carried out in a Tempress furnace. The forming gas atmosphere is achieved by maintaining a constant flow rate of hydrogen and nitrogen at 0.3 and 3 SLM respectively. The temperature of the furnace during annealing is kept at 400°C and carried out for a duration of 1 hour.

Thirdly, annealing is also carried out in a different experimental set-up in Solaris 100 Rapid Thermal Process System. The main difference in annealing by RTP compared to annealing in furnace is in the temperature profile during the process. In the Furnace annealing takes place once the chamber reaches the stable set temperature. In RTP within the first few minutes or seconds of the process the temperature is increased at a drastic rate, which induces thermal shocking to the sample [23]. Figure 2.5 shows the schematic of a RTP system and the temperature profile. A comparison of the temperature profile in RTP annealing and furnace annealing is also shown in Figure 4.4.

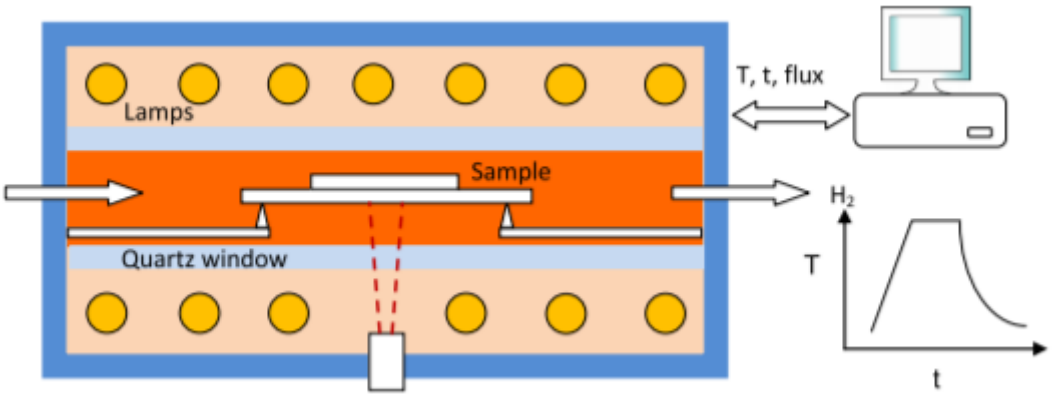


Figure 2.5 Schematic of Rapid Thermal Processing [23].

Lastly, annealing is also carried out by mean of hot plate. Hot plate annealing is done after the metallisation process through screen printing. In the process, the sample is placed on the hot plate for the desired time once the set temperature is stabilised. This is done to ensure the proper contact between the metal and TCO layer (Transparent Conducting Oxide) or poly-Si layer.

2.1.9 Plasma Enhanced Chemical Vapour Deposition

Plasma Enhanced Chemical Vapour Deposition (PECVD) is used in the deposition of Silicon Nitride (SiN_X), which acts as a capping layer during hydrogenation and as anti-reflection coating (ARC). The main advantage of using PECVD compared to that of Chemical Vapour Deposition (CVD) is the low deposition temperature required when a plasma is used [24]. The chamber consists of two electrodes parallel to each other. The plasma is created when the RF (Radio Frequency) power is ON, as a result of the reaction between the gaseous reactants. This is also supported by a DC (Direct Current) if required. The plasma helps in closing the circuit in the process. For the SiN_X layer deposition the reactant gases used are silane and ammonia. The reaction to from a non-stoichiometric SiN_X layer is shown in equation 2.2 [25].

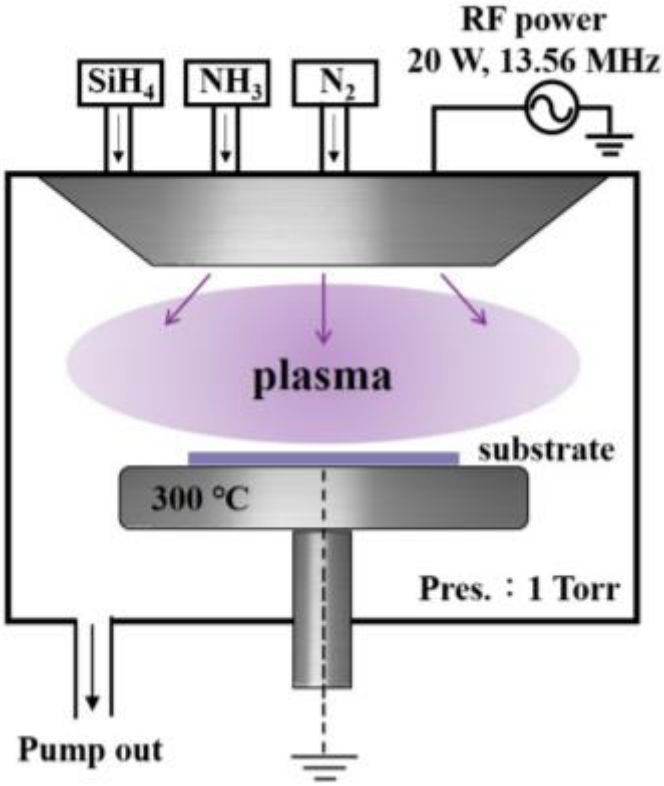


Figure 2.5 Schematic of Plasma Enhanced Chemical Vapour Deposition [26].

$$SiH_x + NH_x \longrightarrow SiN_x + xH_2 \qquad 2.2$$

The product SiN_x is deposited on the sample placed on the top of the electrode and H_2 is purged out. The SiN_X deposition in this thesis is carried out with the help of OXFORD PlasmaLab80Plus. The flow rate of silane and ammonia are maintained at 20 sccm. Different deposition temperatures were tested in this thesis.

2.1.10 Atomic Layer Deposition

Atomic Layer Deposition (ALD) is the technique used in the deposition of the Aluminium oxide layer (AlO_X). AlO_X is used as a capping layer during hydrogenation. The advantages of ALD over other deposition techniques are high quality, high uniformity, high conformity and most importantly the self-limiting nature of precursor adsorption on the substrate [27]. The precursors used in the AlO_X growth are water and trimethylaluminum (TMA). The mechanism behind the growth of AlO_X is shown in Figure 2.6.

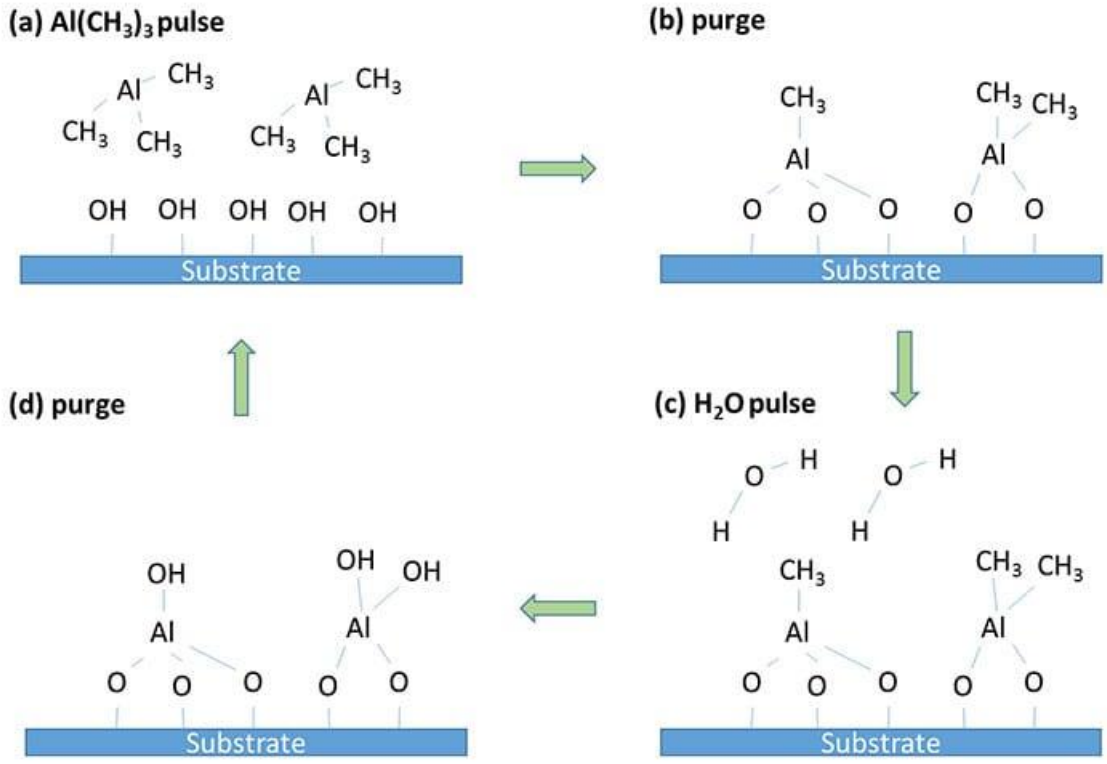


Figure 2.6 Aluminium Oxide growth mechanism by Atomic Layer Deposition [28].

Initially, a pulse of $Al(CH_3)_3$ is fed inside the reaction chamber. TMA reacts with the hydroxyl (OH) groups to form an intermediate layer as shown in Figure 2.6 b. Next, the excess TMA precursor and the by-products are purged. Then, the second precursor water is fed in, which

reacts with the intermediate to form the first AlO_X layer with hydroxyl groups. These hydroxyl groups serve as the active centres for the second cycle to start. Before the commencement of the next cycle again excess water and by-products are purged. The cycle is repeated as required. The number of cycles used in this thesis is 100 to get an AlO_X thickness of around 6 nm on a flat surface. The process is carried out at 105°C in Oxford Instruments OpAL™ reactor.

2.1.11 Physical Vapour Deposition

Physical Vapour Deposition comprises a wide variety of vacuum coating processes in which the metal is physically removed from the source or the target by evaporation or sputtering at very low pressure [29]. In this thesis work PVD is deployed in the metallisation process and in TCO deposition. Aluminium metal is evaporated thermally and deposited on the sample with the suitable hard mask placed on the surface of the rotating chuck in the top of the chamber, as shown in Figure 2.7. The devise used for thermal evaporation is PROVAC PRO500S.

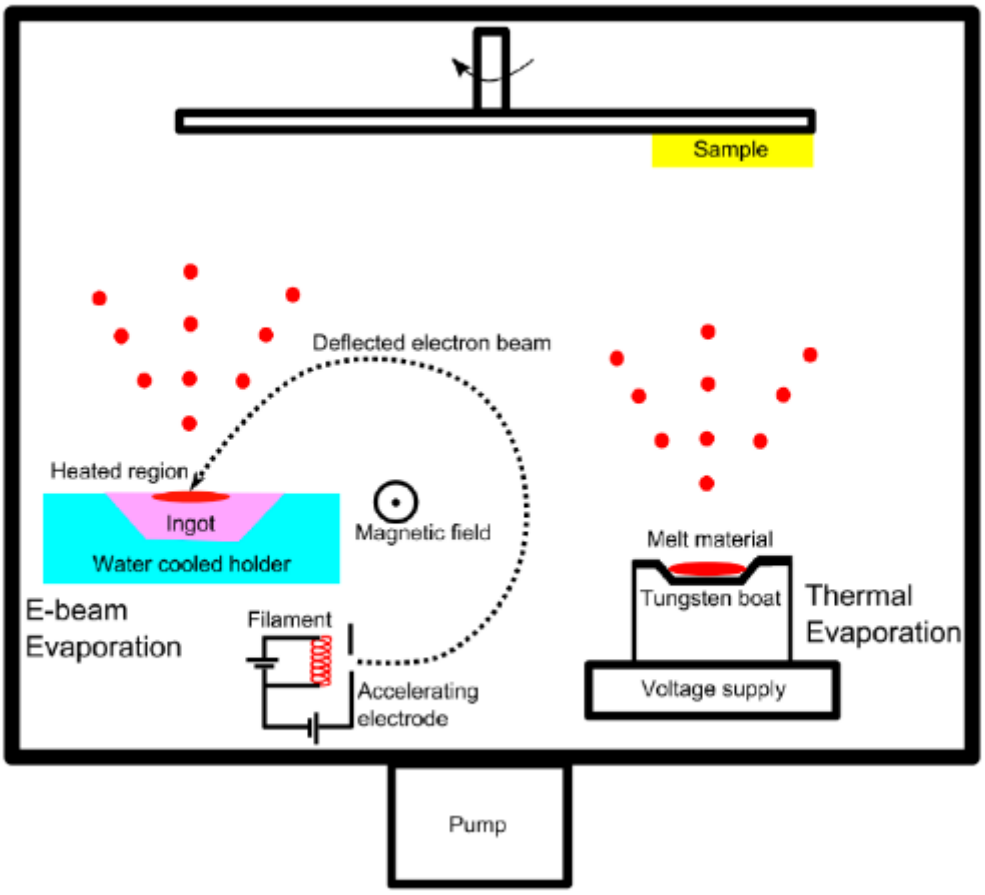


Figure 2.7 Thermal and e-beam evaporation of metal – Physical Vapour Deposition [30].

Magneton sputtering was used in the deposition of TCO layer. In this process inert atoms such as Argon (Ar) are accelerated towards the target. Ar transfers its momentum and energy to the target [30]. The consecutive bombardment of Ar (striking atom) on to the target atom (struck atom) makes it into vapour. The target vapour is then directed toward the sample on which it is be deposited. The deposition pattern is controlled with the help of hard mask. The TCO material used is Indium Tin Oxide (ITO), which is sputtered at a temperature and pressure of 110°C and 2.2 e-5 bar.

2.1.12 Photolithography and Lift-off

Photolithography is the process which helps in the deposition of a photoresist layer on a surface such that the rest of the area can be selectively etched or deposited with the required layer (in our case the metal) [31]. The photoresist material is deposited onto the surface of the cell-precursor. Suitable baking step is performed before the exposure of the photoresist. Exposure is done with the guidance of the mask with ultra-violet light (UV). The exposed photoresist layer undergoes chemical changes such that they remain or gets dissolved during development. In case of a positive photoresist the exposed area gets dissolved in the developer and in case of a negative photoresist the exposed area remains on development. The schematic of photolithography is depicted in Figure 2.8. Then the metal is deposited either with thermal evaporation or sputtering.

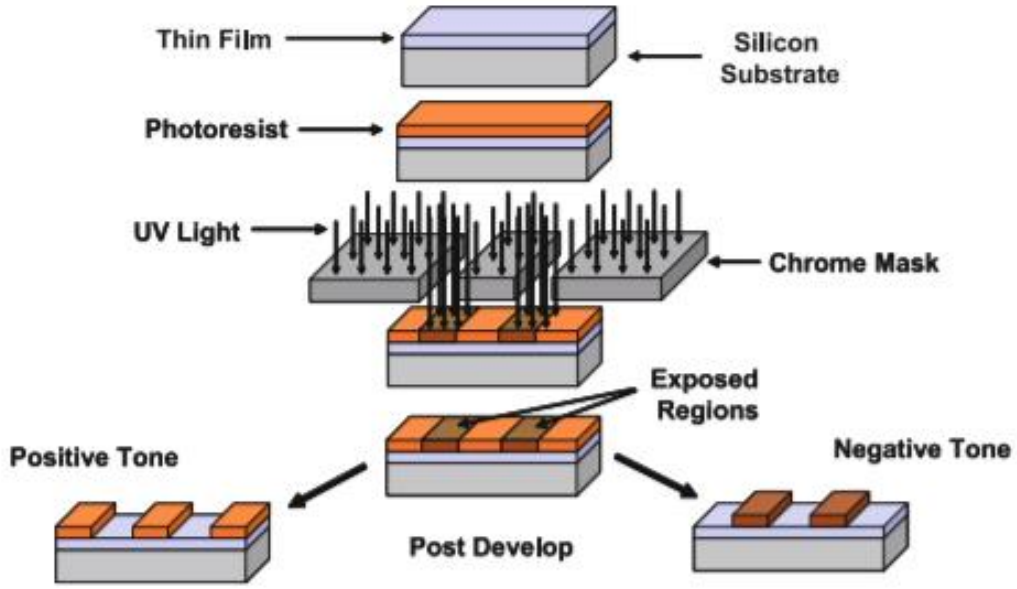


Figure 2.8 Photolithography steps [31].

A maximum metal thickness of 2 µm can be deposited with the help of thermal evaporation. After metallisation lift off is performed to remove the photoresist, which leaves behind the active area of the solar cell, without any metal. Lift-off is performed by ultrasonic dip in acetone [32]. Acetone dissolves the photoresist beneath the metal layer covering the active area of the cell causing the metal to lift-off.

2.1.13 Screen Printing

Screen printing is the widely used metallisation technique in the solar cell manufacturing industry due to the simplicity followed by a firing step [33]. The metal paste is squeezed through the pores in the screen as the squeegee advances. Snap distance is the distance between the screen and the wafer. Snap distance plays an important role in determining the sharpness of the finger geometry. The schematic of screen printing is shown in Figure 2.8.

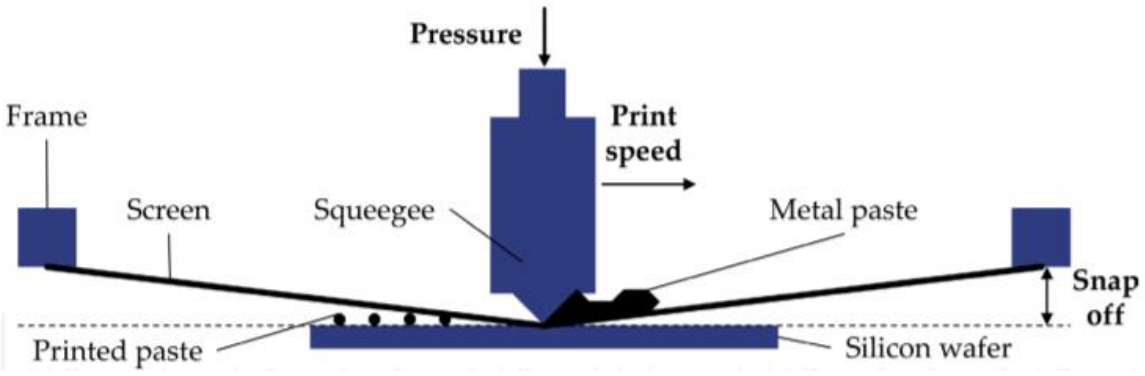


Figure 2.8 Schematic of metal screen printing [33].

The screen printing paste used is a low temperature silver paste. The viscosity of the paste used is 114.4 Pa.s. After the printing the cells are annealed in an oven at 170°C for 40 min. Also, further annealing is carried out at higher temperatures by means of hot plate annealing to check for improvement in the cell performance. The silver paste consists of three main ingredients namely silver powder, solvent and organic binders. During annealing the binders and solvent are burnt away leaving behind the silver metal [33]. The thickness of the silver metal obtained in this set-up in the PVMD group is around 10 – 15 µm.

2.2 Characterisation

Now, that we have understood the working principle of different processing steps it is important to know about the characterisations done on the samples which helps in analysing the performance of the solar cells or half fabricates or cell precursors. The methodology behind the characterisation used are explained in detail in this section.

2.2.1 Spectroscopic Ellipsometry

Spectroscopic Ellipsometry in this thesis work is used to determine the thickness of the layers deposited. It works on the principle of light polarisation. When the vibration of the light wave occurs only in a single plane then the light is said to be polarized. The material which filters the wave vibrating in a single plane is called as a polariser. When the incident light falls on the sample two polarisation states appear orthogonal to each other. The wave with its electric field parallel to the plane of incidence is p-polarised and gets transmitted through the sample. The wave with its electric field perpendicular to the plane of incidence is s-polarised and gets reflected by the sample.

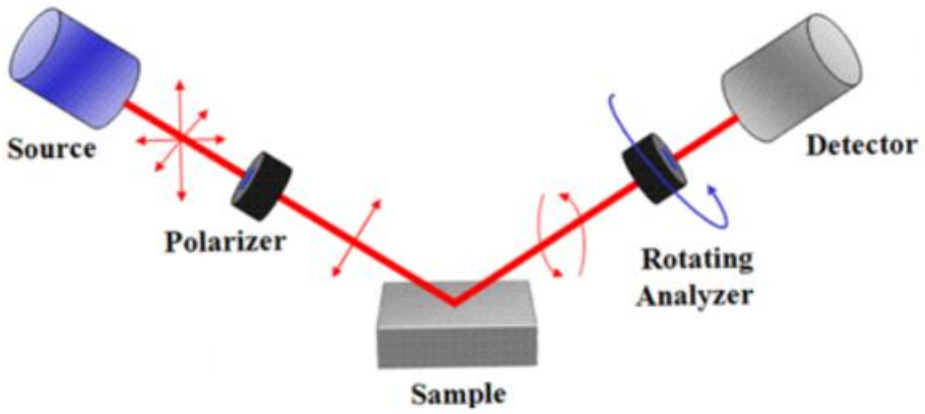


Figure 2.9 Working principle of Ellipsometry [34].

The detector and analyser help in finding the reflectance of the s and p-polarised light from which the n (refractive index) and k (extinction coefficient) values for the materials can be calculated. Since these values are wavelength dependant, they have to be determined for all the wavelengths simultaneously. From these n and k values the thickness of the layer under examination can be deduced by using a suitable fit [34]. The schematic is as shown in Figure 2.9. This measurement was carried out in M-2000DI from J.A. Woollam Co.

2.2.2 Photoconductance Lifetime measurement

The lifetime of the minority charge carriers (τ_{eff}) can be calculated with the help of this measurement. On light illumination excess charge carriers are injected in the bulk (Δn and Δp). From these excess carrier concentrations, the lifetime of the charge carriers can be calculated. Two important modes used in this measurement are the transient mode and Quasi-steady state (QSS) mode. Transient mode is suitable for lifetime greater than 100 µs. The QSS mode is suitable for lifetime less than 100 µs. From the minority carrier densities and the lifetime, the recombination current density (J_0) of the samples can also be deduced [34]. These measurements are carried out in Sinton WCT-120 and its schematic is represented in figure 2.10.

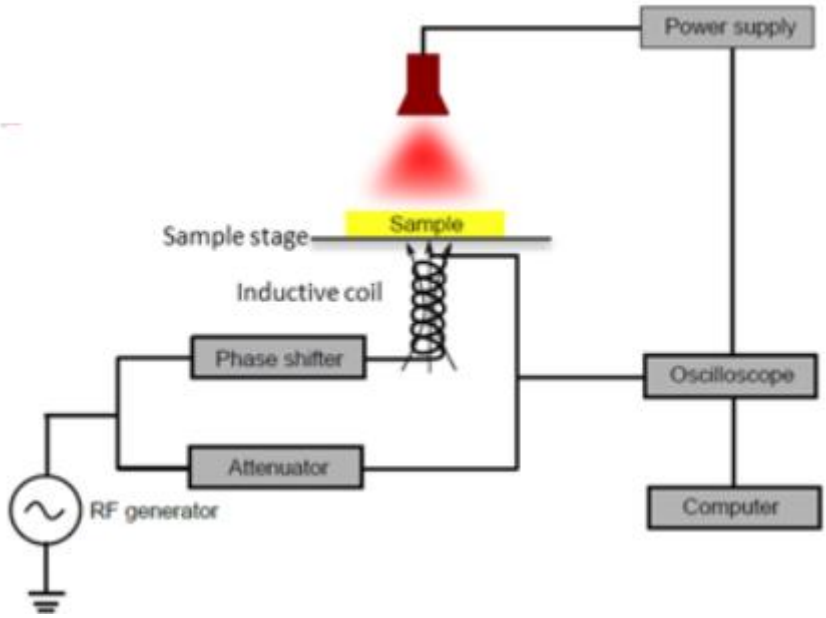


Figure 2.10 Schematic of Sinton lifetime measurement set-up [34]

With this measurement we can also determine two imparted parameters used in analysing the performance of the cell-precursors and the cells, namely Implied V_{OC} (iV_{OC}) and Suns-V_{OC}. The iV_{OC} helps in predicting the final V_{OC} of the device during the course of the fabrication process. It is calculated by using the following equation 2.3.

$$iV_{OC} = \frac{k_B.T}{q}\left[\ln\left(\frac{\Delta n.(N_D + \Delta n)}{n_i^2}\right)\right] \qquad 2.3$$

Suns-V_{OC} helps in finding the open circuit voltage under different light intensities. Suns-V_{OC} under one sun illumination helps in finding the solar cell V_{OC}. At open circuit condition, the

effect of the series resistance is excluded, which helps in analysing the information such as shunting and Pseudo-FF (pFF) [34]. The suns-V_{OC} can be determined by the following equation 2.4.

$$suns\ .J_{SC} = J_0\ exp\left(\frac{q.V_{OC}}{n\ .k_B.T}\right) + \frac{V}{R_{shunt}} \qquad 2.4$$

In the above two equations, J_0 is the recombination current density, q is the elementary charge (1.602 e-19 C), k_B is Boltzmann constant (1.38 e-23 JK^{-1}) and T is room temperature (300 K), n is the ideality factor, R_{shunt} is the shunt resistance, N_D is the concentration of the donor and n_i is intrinsic concentration of carriers.

2.2.3 Transfer Length Measurement

The transfer length measurement helps in calculating the contact resistivity and the sheet resistance of the carrier selective contacts. The sample used in the measurement of the contact resistivity is shown in Figure 3.11. The intercept of the y-axis gives twice the contact resistance (R_C) from which the contact resistivity can be calculated. The slope of the fit helps in finding the sheet resistance (Rs) where W is the length of the metal contact. A sample plot is as shown in Figure 2.10.

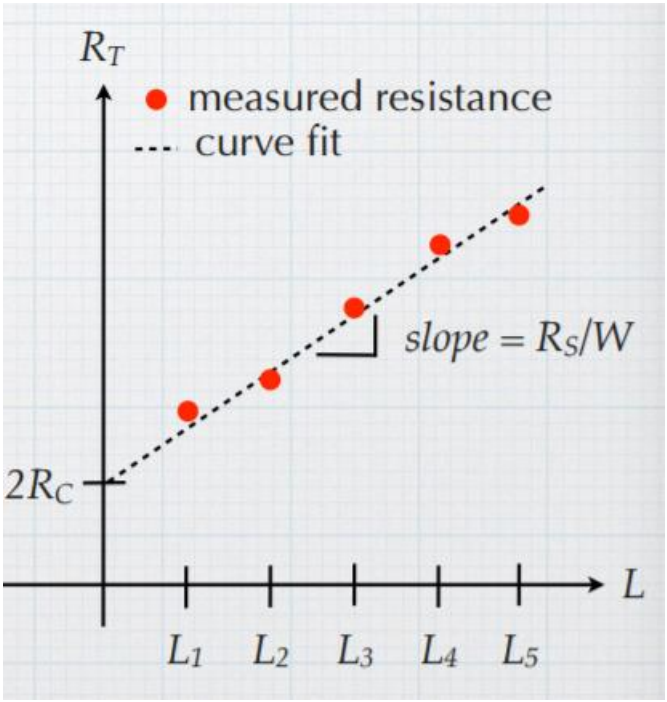


Figure 2.10 TLM – Resistance as a function of the distance between metals [35].

2.2.4 Current-Voltage Measurement

The current-voltage measurement is done in Wacom WXS-156SL2 solar simulator set-up. By using a combination of xenon and halogen lamps this device mimics the Standard Test Conditions (STC) – AM1.5 spectrum, 1000 W/m^2 irradiation. The ambient temperature of 25°C is maintained by means of a cooling system. The schematic of such a set-up is as shown in Figure 2.11.

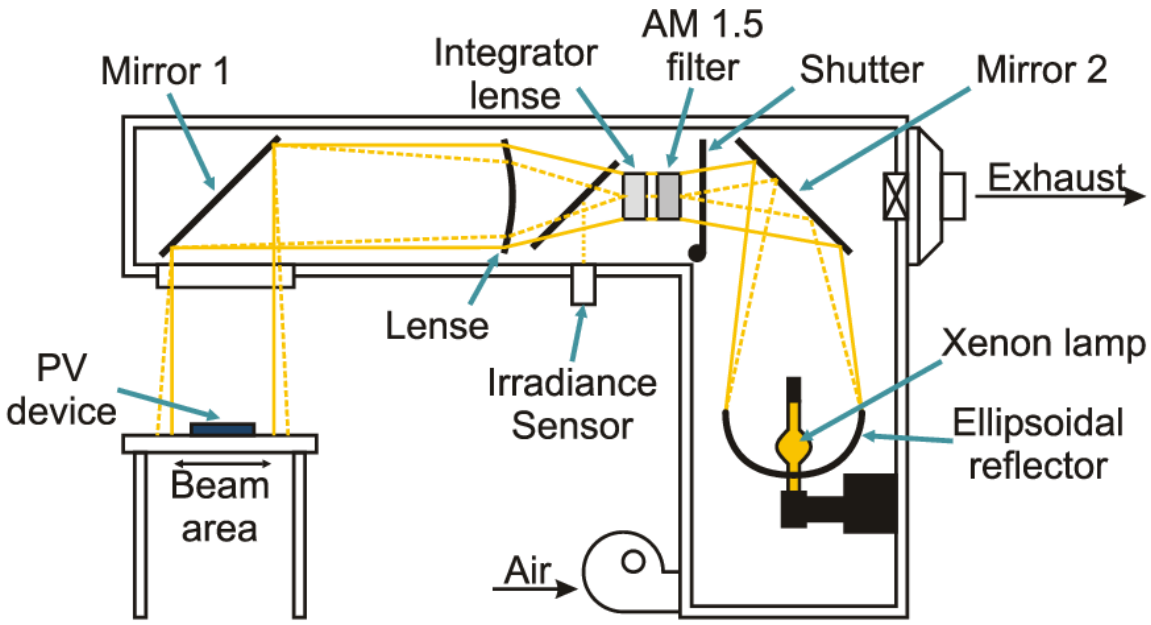


Figure 2.11 Current-Voltage measurement set-up [36].

2.2.5 Electrochemical Capacitance-Voltage Measurement

Electrochemical Capacitance Voltage (ECV) measurement helps in finding the dopant profile within a semiconductor. A depletion region is created within the sample which is free of any charge carriers leaving behind the ionised dopants. This depletion region comprising of the ionised dopants behaves like a capacitor. The capacitance of this depletion region gives the concentration of the dopant in that region. Profiling of the dopant concentration is done by electrochemically etching the sample between the capacitance measurements [37].

3 Carrier Selective Passivating Contact

In this chapter how carrier selectivity is achieved by using an ultra-thin thermal Silicon oxide (t-SiO_X) and poly-Si heavy doped layer is analysed by optimising the different parameters influencing the Carrier Selectivity, by measuring the passivation qualities and contact resistivities of symmetric passivation test samples. Firstly, Tests are carried out with four different poly-poly symmetric samples namely flat and textured n^+-poly, and flat and textured p^+-poly. Secondly, the optimisation of the different parameter is carried out by varying the particular parameter and keeping the rest constant. For instance, if the Oxide growth condition is optimised the other factors such the doping concentration, poly-Si layer thickness, post-implantation annealing time and temperature are kept constant. Also, contact resistivity of the CSPC layers are studied with the help of TLM (Transfer Length Measurements). Finally, the carrier selectivity of the different layers is quantified numerically for better comparison of process conditions.

3.1 Factors influencing carrier selectivity

The carrier selective contact is formed by the overlap of an ultra-thin t-SiO_x layer over a relatively thicker doped poly-Si layer. The carrier selectivity of this combined layers can be influenced by various factors such as the thickness and the uniformity of t-SiO_x , thickness and doping concentration of the poly-Si layer, the post-implantation annealing time which influences the crystallinity of the poly-Si layer and the penetration depth of the dopant atoms (doping profile); and the specific contact resistance (ρ_C) between the Carrier Selective Passivating Contact (CSPC) and the bulk. In this section a literature study on the influence of these parameters on passivation quality and carrier selectivity will be presented.

3.1.1 Silicon Oxide thickness

For the better performance of the CSPC the thickness of the silicon oxide layer plays a vital role. It must be at its right thickness to allow the required charge carrier to pass through it reaching the heavily doped poly-Si layer by tunnelling, in other words providing field effect

passivation and passivating the surface defects by bonding with the dangling bonds, in other words providing chemical passivation. Previous research in our group claims that a tunnel oxide thickness of 1.5 nm shows sufficient passivation effects [38]. It is to be noted that the tunnel oxide was grown by NAOS – Nitric Acid Oxidation of Silicon. A wide range of thicknesses used for the SiO_x are found in literature ranging from 1.4 nm to 3.6 nm [8]. Glunz et al. suggest that a tunnel oxide thickness of 1.1 – 1.2 nm works good for an effective charge carrier transport [39]. Michael et al. from ISFH have documented their usage of ~2.1 nm thick thermal oxide on poly-Si for their POLO (**poly**-silicon on **Oxide**) junction [40]. Even thicker oxide layer of 2.4 – 3.6 nm is reported to perform good by Udo et al. [41].

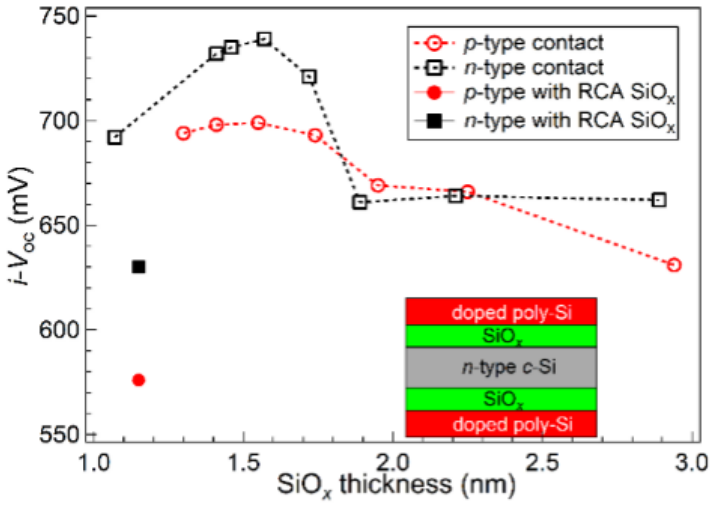


Figure 3.1 Effect of t-SiO_x on the iV_{OC} of n^+ and p^+-polySi symmetric samples *[42]*

Note: The dotted lines in the above plot is just to guide the reader's eyes

From Figure 3.1, it can be seen that the iV_{OC} for both the p^+ and n^+-polySi symmetric samples peak at an oxide thickness of 1.5 nm. The passivation drop below the oxide thickness of 1.5nm can be attributed to the poor chemical passivation of the oxide on the c-Si bulk and on the other hand the drop in passivation at higher oxide thicknesses can be attributed to the deterioration in the field effect passivation, as the barrier for dopant diffusion increases as the t-SiO_x thickness increases [42]. Another issue which has to be kept in mind is that the t-SiO_x growth is followed by a high temperature process at ~ 1000°C for the activation of the dopants and for the conversion of a-Si to poly-Si. This high temperature process might induce thermal stress, leading to formation of voids in in the t-SiO_X layer if it is very thin (< 1.2 nm).

These voids are addressed as pinholes and plays an important role in analysing the charge transport mechanism from the bulk to the poly-Si layer [43].

3.1.2 Silicon Oxide Uniformity

The uniformity of the SiO_X layer depends on the method of deposition. For instance, the t-SiO_X grown with dry oxidation in less porous than the one grown with wet oxidation [17]. This is due to the fact that the wet thermal oxide has water inclusions which decreases the dielectric strength of the oxide layer. As explained in section 3.1.1, the high temperature annealing process following the oxide growth might create local pin holes and the density of the pin holes in the oxide layer increases with the increase in the temperature and the duration of the annealing process [43]. Figure 3.2 shows the increase in pine hole density as the post-annealing time increases.

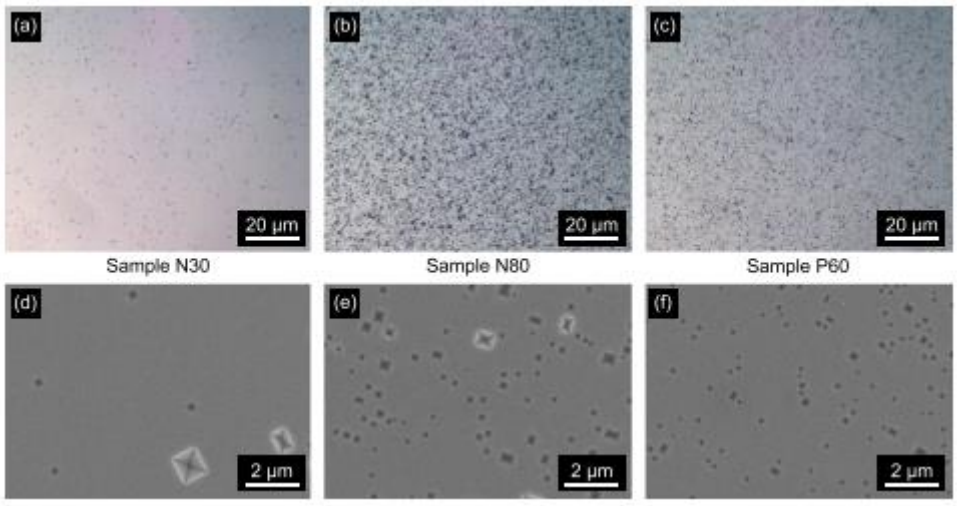


Figure 3.2 [a-c] OM and [d-f] SEM images of the pin hole for three different samples *[43]*.

Note: Samples N30 and N80 are n^+-poly-Si symmetric samples annealed at 1050°C for 30- and 80-mins resp. P60 is p^+-poly-Si symmetric samples annealed at 1050°C for 60 mins

Wietler et al. concluded that with the increase in the pin hole densities the contact resistivity (ρ_C) of the CSPC decreases which results in better carrier collection and on the other hand there is a slight increase in the recombination current density (J_0) arising due to the defect states introduced by the pin holes. When n-type symmetric samples were annealed at 1050°C for 80 mins, the density of the pin hole rises by an order of magnitude. Apart from the pin holes, the local reduction in the thickness of the t-SiO_X layer also results in better charge

carrier collection [44]. Henceforth, some research group claims that the charge carrier collection in SiO_X enabled poly-Si CSPC is due to the combination of the direct tunnelling and pin hole assisted transport [8].

3.1.3 Poly-Si layer thickness

The thickness of the poly-Si can influence the electrical and the optical properties of the carrier selective layers. The electrical quality of the CSPC can be optimised for different poly-Si thicknesses by choosing the right doping concentration and post-implantation annealing conditions. The optical quality of the carrier selective layer can be optimised by thinning the poly-Si layer which decreases the parasitic absorption when deployed in a solar cell. In certain applications a thicker poly-Si of about 250 nm can still be used with almost negligible parasitic absorption. For instance, when used in an Interdigitated Back Contact (IBC) solar cell structure, both the n^+ and p^+-polySi layers are on the rear side of the cell, which enables us to have a very low probability of parasitic absorption of high energy photons. Also, when a 250nm thick poly-Si layers are used in Front Back Contact (FBC) solar cell configuration as bottom cell for a perovskite – c-Si tandem cell applications, the loss due to parasitic absorption is found to be around 1% of the photo-generated current of the bottom cell [22], [20]. Choosing different thickness for a specific doping concentration affects the doping profile throughout the poly-Si layer and the bulk. Also, the post-implantation annealing conditions has to be altered because the thermal flux that lead to an optimal distribution of the dopants in a thinner poly-Si layer may not be sufficient to obtain an optimal distribution of the dopants in a thicker poly-Si layer.

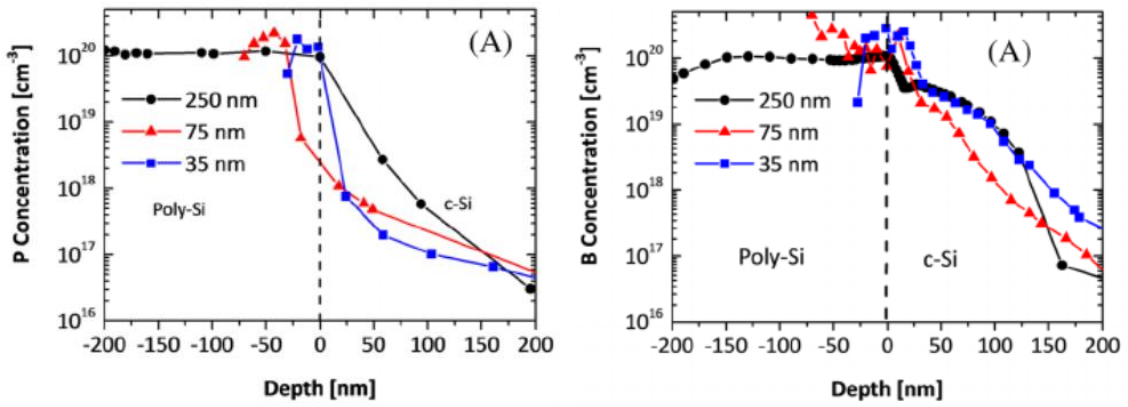


Figure 3.3 Electrochemical capacitance-voltage (ECV) profiling for the CSPC layers. Left: Doping profile of three different textured n^+ poly-Si samples of thicknesses 250, 75 and 35 nm. Right: Similar plot for flat p^+ poly-Si samples. *[20]* Note: The dotted line in the middle of the plot indicated the presence of a thin SiOX layer of 1.5nm

The analysis in this paragraph is based on the research carried out in the PVMD group. Figure 3.3 shows the doping profile of the textured n^+ and flat p^+ poly-Si layers of different thicknesses. It can be clearly seen that the doping profile for both the n^+ and p^+ poly-Si layers vary significantly in the bulk. As mentioned above, the thermal flux from the post-implantation annealing condition has to be low for the thinner poly-Si layers. Hence, its viable to choose a low thermal budget for post-implantation annealing when working on a thinner CSPC layers. Minority carrier lifetime of 4.5 ms was achieved for the textured n^+ poly-Si samples of thicknesses 35 nm and 250 nm; and 2.2 ms was achieved for the sample with 75 nm [20]. The lower lifetime in sample with 75 nm can be attributed to the fact that there is no sufficient phosphorous concentration at the junction of n^+ poly-Si layer and the bulk, as seen in Figure 3.3. On the other hand, high lifetime of 5 ms was recorded for the p^+ flat poly-Si layer only for the 250 nm thick passivation layer [20]. Optimising the CSPC layer with a thinner p^+ poly-Si layer becomes more challenging because of the diffusion of boron atoms is much higher than that of phosphorous atoms [45], [46].

The doping concentration of the poly-Si layers has a significant effect on the absorption coefficient (α) of the layers. As the doping concentration increases, the absorption coefficient of the poly-Si layer, irrespective of the type of dopants, increases at higher wavelengths (λ) > 800 nm. Irrespective of the doping concentrations the absorption coefficient follows the same trend as that of the c-Si in the interval 300 nm to 800 nm [47]. Figure 3.4 clearly shows the increase in absorption at longer wavelengths as the doping concentration of the poly-Si layer increases due to free carrier absorption.

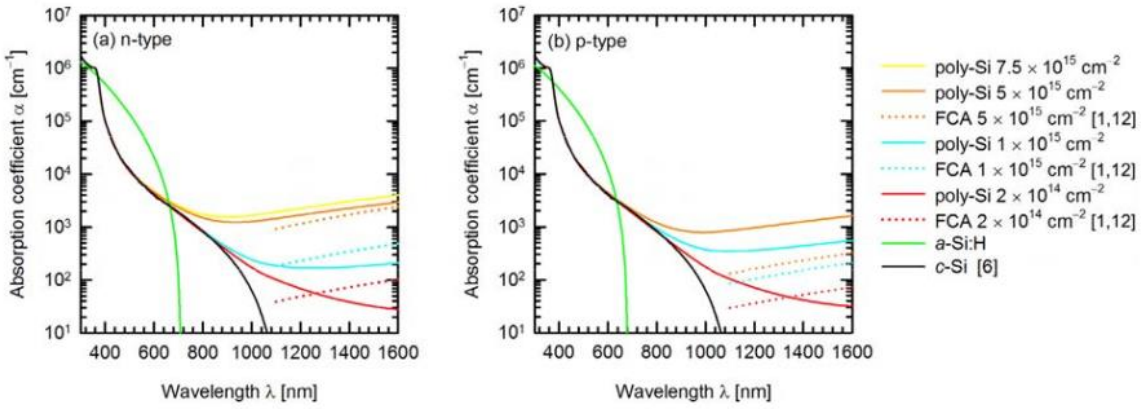


Figure 3.4 The absorption coefficient as a function of the Wavelengths. (a) For n+ poly-Si layer (b) for p+ poly-Si layer *[47]*.

3.1.4 Doping concentration of poly-Si layer

Along with the thickness of the poly-Si layer, the spatial variation of the doping concentration along the CSPC layer affects the passivation quality of the layer. An optimal doping concentration is the one which is sufficient enough to induce band bending to provide the required field effect passivation and insufficient enough to make Auger recombination dominant. Increasing the doping concentration increases the in-diffusion area of the dopants in the bulk during the post-implantation annealing process [48]. This can lead to the deterioration of field effect passivation of the contacts. Higher doping concentrations can also lead to the formation of inactive precipitates of dopants on cooling after post-implantation annealing as the dopant concertation approaches its solubility limit in poly-Si. This can induce defect states, that can serve as an active sight for Shockley Read Hall (SRH) recombination centres [48]. For instance, at around 900°C the solubility of Phosphorous atoms in silicon is 2e20 atoms/cm^3 and the solubility of Boron atoms in silicon is 8e19 atoms/cm^3 [49], [50] as shown in Figure 3.5 . Henceforth, the selection of the doping concentration should be less than the maximum solubility of the dopants at the post-implantation annealing temperature. An increase in the doping concentration of phosphorous atoms from 8e19 cm^{-3} to 2e20 cm^{-3} results in a significant increase in the electron tunnelling current [48]. Thus, an optimal doping concentration is required to achieve the desired passivation effect.

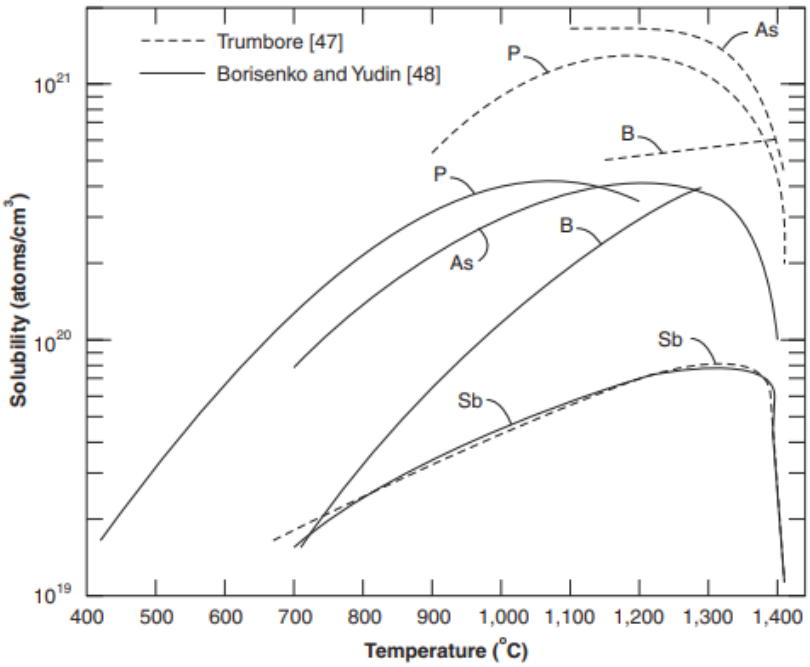


Figure 3.5 Solubility of dopants in silicon as a function of temperature *[49]*.

The concentration of the dopants in the poly-Si layer can be controlled by changing the ion dosage (ions/cm^2) and the energy of implantation (keV). There is a high range of window to select the ion dosage level, but the energy of implantation depends on the type of implanter used during the experimentation. In this thesis, using Varian ImplanterE500HP, the optimal energy used for implanting Phosphorous and Boron is 20 keV and 5 keV respectively. The low implantation energy used for Boron is due to the high diffusivity compared to that of Phosphorous in silicon. This is explained in detail in section 3.1.5.

3.1.5 Post-implantation Annealing Conditions

There are two main happenings during the post-implantation process. Firstly, the dopants get activated during the high temperature annealing process and gets spatially distributed along the poly-Si layer and the silicon bulk (in-diffused region of the bulk) as shown in Figure 3.3. Secondly, the amorphous silicon (a-Si) deposited on the t-SiO_X phase changes to poly-Si at this high temperature due to thermal crystallisation. The crystallinity of the poly-Si formed on annealing of a-Si depends on the thermal budget used in the annealing process.

Diffusion of Boron and Phosphorous atoms in the silicon substrate exhibits an Arrhenius behaviour when solved by using Fick's equation. Christensen et al. calculated the activation

energy required for the diffusivity of Boron and Phosphorous to be 3.12±0.04 eV and 2.74±0.07 eV respectively [46]. Hence, the thermal budget needed for the activation of Boron atoms in a silicon substrate has to be slightly higher than that required for Phosphorous atoms. This analogy complies with the suggestions made to carry out post-implantation annealing at temperatures greater than 950°C for p^+ poly-Si carrier selective layers in Gianluca et al. [20]. The size of Phosphorous and Boron atoms is 195 pm (Atomic number: 15) and 180 pm (Atomic number: 5) respectively. Thus, Boron diffusion in more agile compared to that of phosphorous in silicon substrate. The diffusivity of Boron (6±2 e-2 cm^2/s) is higher than that of Phosphorous (8±5 e-4 cm^2/s) by two orders of magnitude [46]. Thus, higher temperature annealing for p^+ poly-Si CSPC layers on one hand, helps activating the dopants and on the other hand, increases the in-diffused bulk region due to high diffusivity leading to poor field effect passivation. Thus, the optimisation window for the p^+ poly-Si CSPC layers becomes narrow and tricky to optimise.

Bellanger et al. studied the crystallisation of a-Si under different thermal budgets. It was concluded that the crystallinity of 6 µm thick poly-Si increases as the thermal budget increases. A crystalline fraction of 68% was recorded at thermal annealing for 1 h at 490°C and 90% crystallinity at thermal annealing for 1 h at 550°C [51]. This low temperature annealing is not sufficient for the dopant activation to take place. ThanhNga et al. have also documented that there is complete crystallisation of a-Si to poly-Si while annealing at 650° C for 5 hrs [52]. Higher temperature and short duration annealing results in both high crystallinity and dopant activation. Hence, research works in the PVMD Group were carried out at high temperatures ranging from 850 – 950°C in time intervals ranging from 5 – 90 min [20], [22].

Figure 3.6 shows the Raman spectra for both a-Si samples before and after thermal annealing. The upward shift in the arbitrary units (y-axis) at the wave number 520 cm^{-1} after annealing shows the increase in the crystallinity of the a-Si layer. Henceforth, in this thesis, the post-implantation annealing temperature was set to be 900°C and 950°C, and different annealing times were tested.

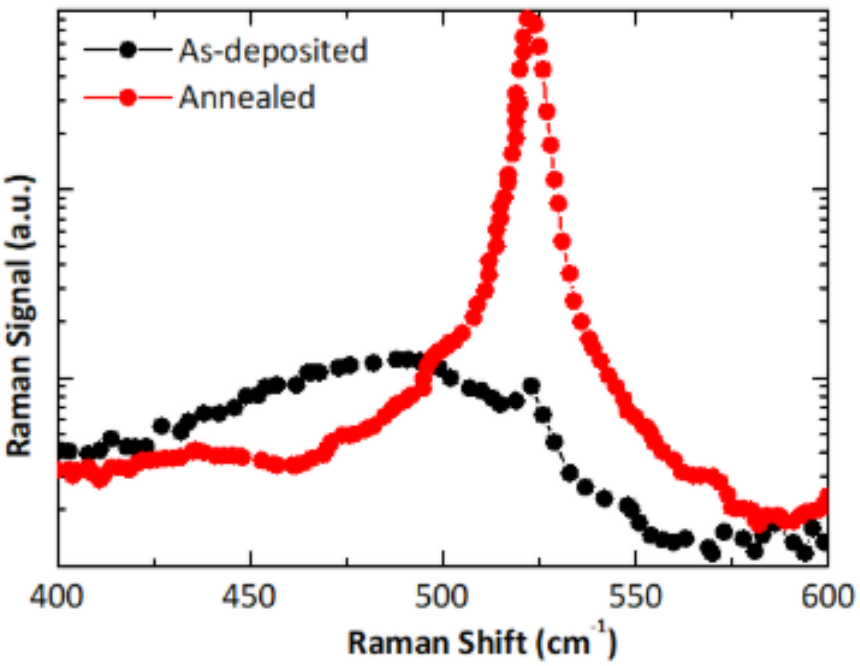


Figure 3.6 Raman spectra of a-Si (black) and poly-Si (orange) after annealing at 950°C *[20]*.

3.1.6 Specific Contact Resistance of the CSPC layer

Specific contact resistance or Contact resistivity (ρ_C) of the CSPC layer helps in analysing the resistive losses induced by the carrier selective layers on the working device. This value has to be as low as possible for the better required charge collection. Also, the Contact resistivity varies inversely with the sum of the conductivities of both the majority and minority charge carriers [8]. This can be expressed in the form of Equation 3.1, where σ_m and σ_M are the conductivity of the majority and the minority carriers respectively. Hence, we can infer that to have a low contact resistivity the conductivity of the required charge carrier should be as high as possible. The ratio of the conductivity or the resistivity of the charge carriers can be thus helpful in analysing the carrier selectivity [8], [53].

$$\rho_C \; \alpha \; \frac{1}{\sigma_m + \sigma_M} \qquad 3.1$$

In this thesis work the contact resistivity of the CSPC layers were measured with the help of Transfer Length Measurements (TLM). Research by ECN/Tempress have documented contact

resistivity of 5 mΩ.cm^2 and 30 mΩ.cm^2 for p$^+$ poly-Si and n$^+$ poly-Si [54]. P.Stradins et al. have also reported contact resistivity of ~20 mΩ.cm^2 for n$^+$ poly-Si CSPC with oxide grown thermally at 700°C followed by post-implantation annealing at 850°C [55].

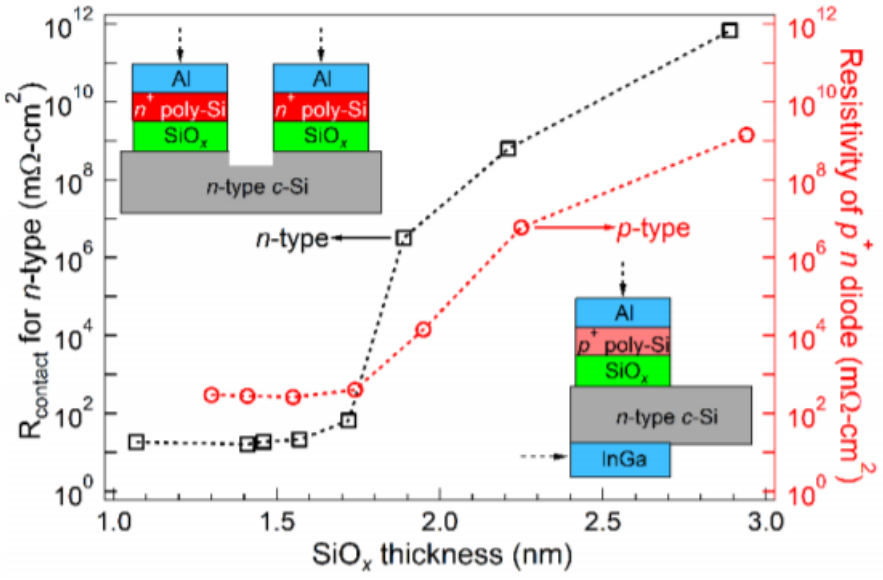


Figure 3.7 Contact resistivity of the n+ poly-Si (Black Squares) and p+ poly-Si layers (Red Circles) as a function of the thermal oxide thickness ranging from 1 nm to 3 nm [42].

Figure 3.7 shows the specific contact resistance of the CSPC layers (both n and p type) depends on the thickness of the SiO_X layer. It is well known that SiO_X is dielectric in nature known for its good electrical insulating nature. It can be seen that the contact resistivity increases drastically in orders of magnitude, when the thickness of the oxide layer is greater than 1.7 nm. When an oxide thickness of 1.5 nm is used with a n$^+$ poly-Si layer contact resistivity of ~ 20 mΩ.cm^2 is recorded. This measurement is carried out easily with the help of Transfer Length Measurement (TLM) as shown in the figure insert on top left of Figure 3.7. On the other hand, TLM measurements don't ease the measurement of contact resistivity of p$^+$ poly-Si layer on n-type bulk. Hence, a diode setup is used for this measurement. For a proper measurement of the contact resistivity of such a layer, an ohmic contact has to be ensured between the layer and the substrate in order to facilitate the flow of current from the contact to the layer and through the bulk and back to the contact. For instance, if a p$^+$ poly-Si layer along with a thin t-SiO_X is grown on a n-type bulk, it forms a p-n junction leading to rectification or a diode behaviour [42], [10]. Through, the diode set-up on the bottom right of Figure 3.7, contact resistivity of p$^+$ poly-Si CSPC layer is found to be higher than that of n$^+$

poly-Si CSPC layer. In this thesis work, a novel method for the measurement of the contact resistivity of p^+ poly-Si carrier selective layer is introduced as follows.

To avoid the formation of p-n junction and to measure the contact resistivity of the p^+ poly-Si CSPC layer, t-SiO_X and p^+ poly-Si layers were grown on a p-type bulk. If such as structure is used, two critical questions arise. Firstly, Will the conductivity of the p^+ poly-Si layer CSPC on a n-type bulk be same as that of the conductivity on a p-type bulk? The resistivity of both the n and p type wafers used in this thesis are identical (1 – 5 Ω.cm). Hence, the conductivity of the p^+ poly-Si CSPC layer on p-type bulk will be similar to that of the conductivity of the p^+ poly-Si CSPC layer on n-type bulk. Secondly, Will the same oxidation condition lead to similar t-SiO_X thickness on both n-type and p-type bulk? There is no significant literature which studies the effect of doping on the oxidation rate of the silicon bulk on nano scale. Hence, some approximations are made to answer the question. For a wafer resistivity of 2.5 Ω.cm, the doping concentration for n-type and p-type bulk were calculated to be 1.87 e15 cm^{-3} and 5.67 e15 cm^{-3} respectively (using online calculator) [56]. These values fall in the moderate doping concentration range between 10^{14} to 10^{16} cm^{-3} for silicon [5]. Deal and Sklar studied the thickness of wet and dry thermal oxide of heavily doped silicon and concluded that during dry oxidation, the oxidation rate of the p-type and n-type silicon substrate varies significantly only at higher doping concentration and higher oxidation temperature [57].

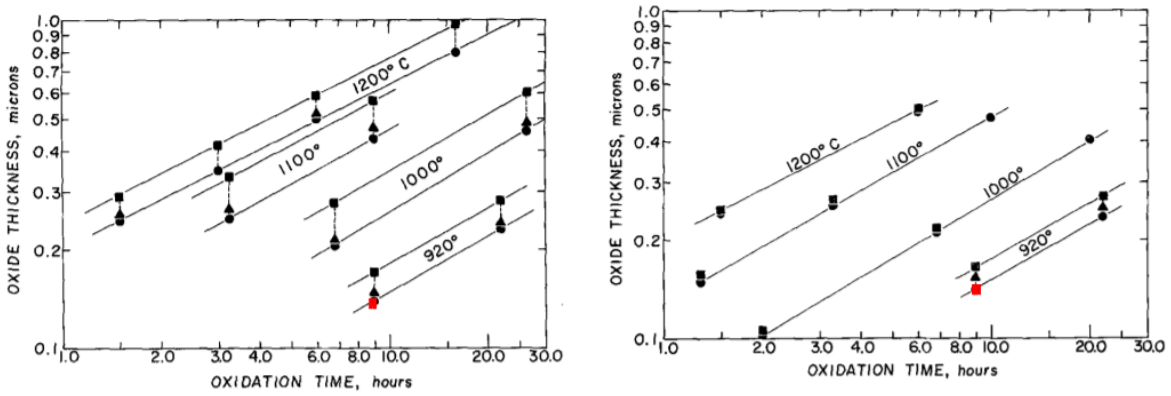


Figure 3.8 Left: The thermal Silicon Oxide thickness for different doping concentration of Boron with respect to the oxidation time during dry oxidation. Right: Similar for different doping concentration of Phosphorous [57]. Note: The line with the red square represents boron doping concentration of 1 e16 cm^{-3} (Left) and phosphorous doping concentration of 4 e15 cm^{-3} (Right).

For instance, at the oxidation condition of 9 hours at 920°C, represented as red square in Figure 3.8, the thickness for the thermal oxide in both the cases are approximately 130 nm. Henceforth, it is inferred that at same oxidation conditions a n-type wafer of 4 e15 cm^{-3} phosphorous concentration and a p-type wafer of 1 e16 cm^{-3} boron concentration leads to similar oxide thickness. As mentioned above, the doping concentrations of the wafers used are slightly lesser than the values used in this analysis. So, it can be concluded that similar oxidation conditions will give rise to similar oxide thicknesses on both n-type and p-type silicon wafers.

3.2 Quantifying Carrier selectivity

From the above section it is obvious that there are many factors that determine the selectivity of the layer. All the above discussed factors either leads to recombination losses (SRH recombination or Auger recombination), which affects the recombination current density (J_0) or changes in contact resistivity (ρ_C) of the CSPC layer. Contact resistivity and recombination current density helps in analysing the carrier selectivity od the CSPCs. Also, these two parameters, by instinct has to be as low as possible for having a better carrier selectivity as expressed in Equation 3.2. Hence, quantifying carrier selectivity is possible with simple derivation.

$$\text{Carrier Selectivity } \alpha \frac{1}{\rho_C \cdot J_0} \qquad 3.2$$

The derivation as follows is done with the help of work by Brendel et al.

As mentioned in section 3.1.6, the carrier selectivity of the carrier selective contact can be delineated by comparing the contact resistivity of the desired charge carrier that has to be collected to that of the other. So, the carrier selectivity (S) can be defined as the ratio of the contact resistivity of the minority charge carrier (ρ_m) to the contact resistivity of the majority charge carrier (ρ_M). As a result, carrier selectivity, S is just an arbitrary number with no units.

$$\text{Carrier Selectivity, } S = \frac{\rho_m}{\rho_M} \qquad 3.3$$

By knowing the current-voltage characteristics of both the minority and majority charge carrier, their contact resistivity can be easily defined.

Firstly, Shockley equation establishes the relation between the external net current density due to the minority charge carriers (J_m) and the external voltage (V_a) applied across the p-n junction as depicted in Equation 3.4.

$$J_m = J_0 \left[exp\left(\frac{q.V_a}{k_B.T}\right) - 1 \right] \qquad 3.4$$

Where J_0 is the recombination current density, q is the elementary charge (1.602 e-19 C), k_B is Boltzmann constant (1.38 e-23 JK^{-1}) and T is room temperature (300 K).

The above equation can also be rewritten in terms of thermal voltage (V_{th}) as follows

$$J_m = J_0 \left[exp\left(\frac{V_a}{V_{th}}\right) - 1 \right] \quad 3.5$$

Since, the thermal voltage, $V_{th} = \frac{k_B.T}{q}$

We know that, the specific contact resistance (ρ) imposed to the charge carrier can be calculate by the inverse of the first derivative of the current density (J) with respect to the applied voltage (V) at V = 0. So,

$$\text{Specific contact resistance, } \rho = \left(\frac{\partial J}{\partial V}\right)^{-1}_{V=0} \quad 3.6$$

Hence the specific contact resistance of the minority carriers (ρ_m) can be expressed as follows,

$$\rho_m = \left(\frac{\partial J_m}{\partial V_a}\right)^{-1}_{V_a=0} \quad 3.7$$

By differentiating the minority carrier current density (J_m) with respect to the applied voltage (V_a), we get,

$$\frac{\partial J_m}{\partial V_a} = J_0 \left(\frac{\partial \left(\left[\exp\left(\frac{V_a}{V_{th}}\right) - 1 \right] \right)}{\partial V_a} \right) \quad 3.8$$

$$\frac{\partial J_m}{\partial V_a} = J_0 \left(exp\left(\frac{V_a}{V_{th}}\right) \cdot \frac{1}{V_{th}} \right) \quad 3.9$$

$$At\ \ V_a = 0, \ \ \frac{\partial J_m}{\partial V_a} = \frac{J_0}{V_{th}} \quad 3.10$$

Henceforth Equation 3.7 can be rewritten as follows,

$$\rho_m = \frac{V_{th}}{J_0} \quad 3.11$$

Secondly, we can assume that the majority charge carriers experience ohmic behaviour across the carrier selective contact. In other words, the majority charge carriers experience a linear current-voltage characteristic at the carrier selective contacts.

Hence the majority charge carrier current density (J_M) can be expressed as in Equation 3.12

$$J_M = \frac{V_a}{\rho_C} \tag{3.12}$$

Where ρ_C is the contact resistivity of the CSPC layer.

As per Equation 3.6, the specific contact resistance of the majority charge carriers (ρ_M) can be expressed as follows,

$$\rho_M = \left(\frac{\partial J_M}{\partial V_a}\right)^{-1}_{V_a=0} \tag{3.13}$$

By differentiating the majority carrier current density (J_M) with respect to the applied voltage (V_a), we get,

$$\frac{\partial J_M}{\partial V_a} = \frac{1}{\rho_C} \tag{3.14}$$

Henceforth, Equation 3.13 can be re-written as,

$$\rho_M = \rho_C \tag{3.15}$$

Now Equation 3.3 becomes,

$$Carrier\ Selectivity,\ S = \frac{\mathrm{V_{th}}}{J_0 \cdot \rho_C} \tag{3.16}$$

The recombination current density, J_0 is expresses in $fA.cm^{-2}$ and the contact resistivity, ρ_C is expressed in $m\Omega.cm^2$. So, it becomes obvious that Equation 3.16 will lead to a very large number which becomes cumbersome to handle. This problem can be dodged by simply expressing carrier selectivity, S in logarithmic scale. Thus, we can define logarithmic selectivity, S_{10} as follows,

$$\text{Logarithmic Selectivity},\ S_{10} = \log\left(\frac{\mathrm{V_{th}}}{J_0 \cdot \rho_C}\right) \tag{3.17}$$

Hence, from Equation 3.17 it is possible for us to quantify the carrier selectivity of the contact. As mentioned earlier for the best performance of the carrier selective contact, the contact resistivity and the recombination current density has to be as low as possible. So, higher the S_{10} value better is the carrier selectivity of the contact.

3.3 Optimal Conditions for CSPC by NAOS

Extensive research in the PVMD group has been made in optimising the optimal SiO_x thickness and using them for the carrier selective passivating contact applications by using NAOS – **N**itric **A**cid **O**xidation of **S**ilicon. Hence, the results from such an optimisation will serve good as a base line for the optimisation of CSPC with ultra-thin dry thermal oxide (t-SiO_X).

Table 3.1 The Passivation quality of the n-type and p-type poly-Si with NAOS SiOX with different poly-Si thicknesses, ion implantation energy and dosage, and post-implantation annealing temperature, time and atmospheric condition *[58]*.

Poly-Si			Implantation		Annealing/Oxidation			Passivation		
n-/p-type	Sample number	Thickness [nm]	Energy [keV]	Dose [$\times 10^{15}$ cm^{-2}]	Temperature [°C]	Time [min]	N_2/O_2	τ^b [ms]	J_0 [fA/cm^2]	iV_{OC} [mV]
n-type	1	70	~	~	850	90	N_2	0.03	1000	560
	2	75	20	2	850	90	N_2	5.5	9.5	706
	3	75	20	3.5	850	90	N_2	3	21.5	694
	4	75	20	4	850	90	N_2	1.5	51	684
	5	75	20	6	850	90	N_2	0.3	228	637
	6	250	20	2	950	5	N_2	1.2	48	679
	7	250	20	6	950	5	N_2	8	9	721
	8	**250**	**20**	**6**	**950**	**5**	**O_2^c**	**11.8**	**6**	**723**
p-type	12	200	5	5	950	5	N_2	1.8	25	695
	13	200	5	5	950	15	N_2	1.6	33	690
	14	200	5	5	950	30	N_2	1.1	65	677
	15	250	5	5	950	5	N_2	1.9	30	692
	16	**250**	**5**	**5**	**950**	**5**	**O_2^c**	**3.8**	**19**	**704**

Note: Samples 8 and 16 (in bold) have the best passivation effect and carrier selectivity. The samples are flat.

From Table 3.1, taken from G. Yang et al. the following conclusions can be drawn. Firstly, the optimal thickness of the poly-Si layer for a better passivation is observed at a thickness of 250 nm for both n^+ and p^+ poly-Si CSPC layers. Secondly, the optimal implantation energy use for phosphorous and boron implantation is 20 keV and 5 keV respectively. The most favourable ion dosage on the flat samples are 6 e15 ions/cm^2 and 5 e15 ions/cm^2 for phosphorous and boron implantation. Lastly, the prime condition for both n^+ and p^+ poly-Si layers during post-implantation annealing is with oxygen atmosphere at 950°C for 5 min. Meanwhile, as post-implantation annealing takes place in oxygen atmosphere and at high temperature the poly-Si layer tends to oxidise to form poly-$Si(O)_x$. As a result, this layer has to be chemically etched away before proceeding with further processing steps. Now, with these inferences, the ballpark values can be set, to fix the optimisation window for the CSPC with t-SiO_X.

3.4 Sample Preparation

3.4.1 Symmetric Sample Preparation

Symmetric samples aka half-fabricates are used in the study of the passivation quality and carrier selectivity of the contacts. The flow chart of their fabrication process is represented pictorially in the following Figure 3.9. The schematic of the textured and flat n^+ and p^+ poly-Si symmetric samples are shown in Figure 3.10.

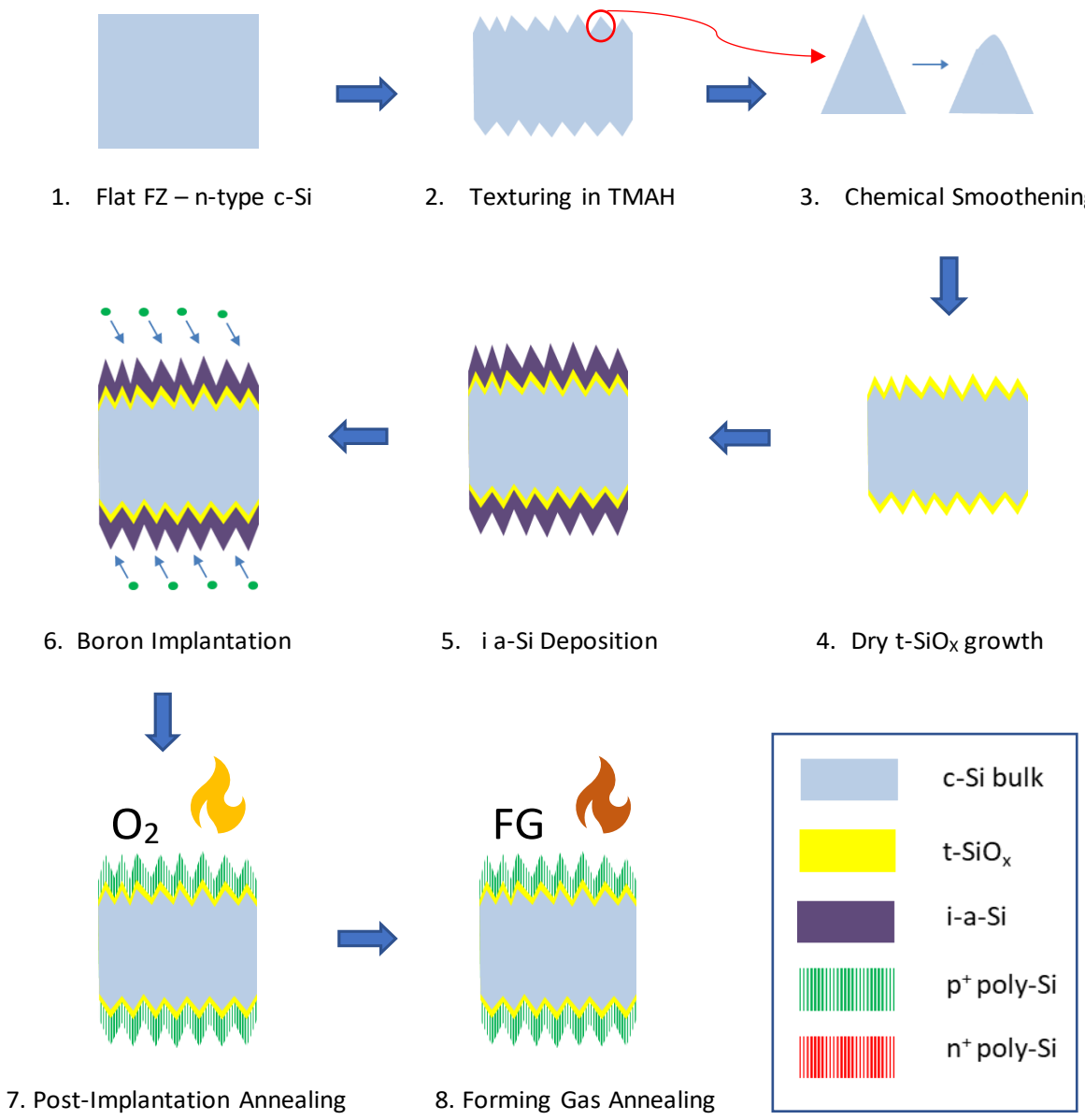


Figure 3.9 Flow chart for the fabrication of textured p^+ poly-Si symmetric sample.

Note: Only the most important steps are presented in this flow chart. Standard cleaning when necessary is performed between the steps.

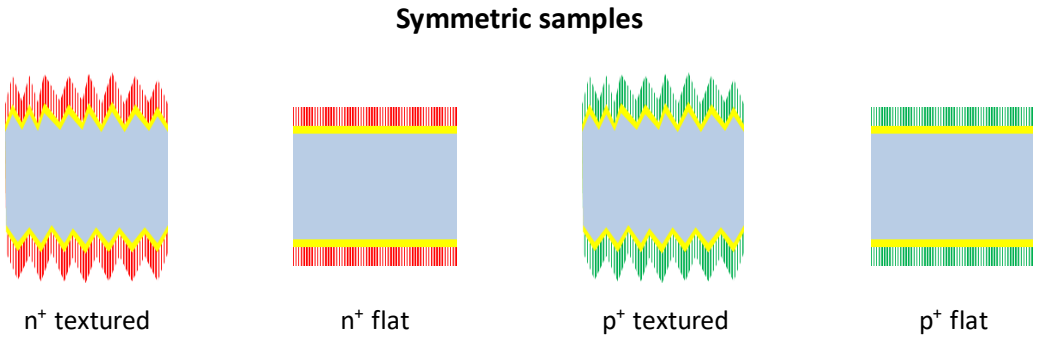


Figure 3.10 Symmetric sample structures used in the optimisation of the symmetric samples.

The fabrication process starts with the fully polishes <100> crystal-oriented n-type c-Si Float Zone wafers. The thickness of the wafers is around 280 µm. Texturing of the wafers is done by selective etching in TMAH solution with some proportion of ALKA_TEX solution at 80°C and with constant stirring at 160 rpm for 15 min until there is no reflection from the surface. The solution is initially activated with the help of a dummy wafer. Then Standard cleaning is performed on the wafers to get rid of any residues from texturing. This is following by etching in HNO_3 / 40% HF, for 2 min with constant circulation of the etchant to smoothen out the sharp pyramids to reduce the defect centres. Again, standard cleaning is performed before the removal of native oxide grown on the silicon surface by HF, 0.55% dip in Marangoni drying process for 4 min. This is followed immediately by the growth of thermal oxide (t-SiO_x) by dry oxidation. Then intrinsic a-Si is grown on the oxide layer with the help of Low-Pressure Chemical Vapour Deposition (LPCVD) technique. This is followed by ion implantation by Varian ion implanter E500HP. Boron and Phosphorous ions are used to make the p^+ and n^+ layers with suitable implantation energy and ion dosage. Then a last round of standard cleaning is performed to remove the impurities on the surface formed during implantation. Post-implantation annealing is then performed at high temperature to activate the dopants and to make the ion-implanted a-Si layer undergo thermal-crystallisation to doped poly-Si. Before the measurements of the samples Forming Gas Annealing (FGA) is performed to slightly improve the chemical passivation of the contacts.

3.4.2 TLM Sample Preparation

The Transfer Length Measurement (TLM) samples are made in the same way as that of the symmetric samples, but implantation one single side is sufficient to study the contact resistivity of the carrier selective layers. Also, metallisation is done to allow the external current to pass through the contact. Metallisation is done through Physical Vapour Deposition (PVD) – [Type: e-beam evaporation] of Aluminium, by using hard mask. The thickness of the metal deposited is 2 µm. Figure 3.11 shows the schematic and the picture of a flat n^+ poly-Si sample used for the TLM measurement. As mentioned in section 3.1.6, for measuring the carrier selectivity of the p^+ poly-Si layer, a p-type bulk is used in this thesis work.

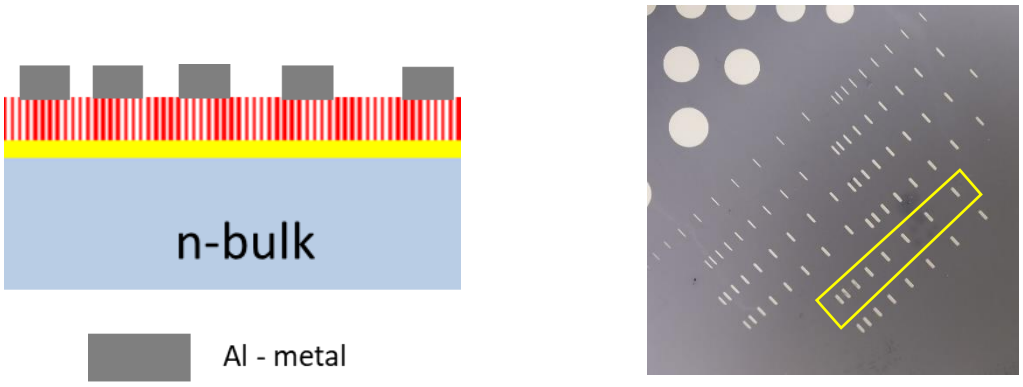


Figure 3.11 Left: Schematic of the TLM sample for n^+ - CSPC. Right: Prepared sample for TLM measurements. Note: The yellow box on the right picture encloses the line of measurement used to measure the resistance.

Table 3.2 Spacing between the metal contacts

Label	Spacing (µm)
L12	625
L23	1050
L34	1475
L45	1900
L56	2325
L67	2750
L78	3175

Table 3.2 shows the distance between each metal contacts in the measurement line highlighted in Figure 3.11. The resistances experienced by a small current ~ 8 mA across the metal contacts are measures and plotted against the metal spacing to find the contact resistance (R_C) from which the contact resistivity (ρ_C) of the contact can be calculated.

3.5 Experimental results and inferences

In this section the results from the experiments are presented and analysed in comparison with the literature findings. *Firstly*, the thermal budget used for the thermal oxide growth and post-implantation annealing are optimised. The p^+ textured poly-Si layer is found to be the one with the lowest passivation quality and the reason for such behaviour is analysed with the help of ECV measurements. *Secondly*, study on the thickness of the poly-Si layers are performed. *Thirdly*, the effect of the thermal budget of oxide growth and post-implantation annealing on contact resistivity is studied with the help of TLM measurements. Lastly, the carrier selectivity of the layers is quantified with the logarithmic selectivity (S_{10}). The main objective is to find in optimal set of parameters for all the four different symmetric samples.

NOTE: The iV_{OC} used in the plots are after Forming Gas Annealing (FGA)

3.5.1 Thermal Budget of Oxide Growth and Post-implantation Annealing

The optimisation of the parameters is done in two stages. In the first stage (Section 3.5.1.1 – 3.5.1.3), the thermal budgets used for the thermal SiO_X growth are 600°C, 6 min; 675°C, 6 min and 675°C, 8 min and the thermal budget used for post-implantation annealing are 900°C -10 min; 20 min; 30 min and 950°C, 2 min; 5 min; 15 min. Temperature range of 600 – 675 °C is chosen for the oxide growth because at temperatures greater 700°C, the thickness of the oxide grown are greater than 2 nm [56]. But our target thickness of the thermal oxide is in the range 1 – 2 nm for the optimal tunnelling of charge carriers. Temperature range of 900 – 950 °C is chosen for post-implantation annealing as a result of the previous research explained in Section 3.3. In the second stage (Section 3.5.1.4), the oxide growth condition is fixed at 675°C, 3 min and the post-implantation annealing temperature is fixed at 950°C and four different annealing time intervals 0.5, 2.2, 5 and 15 min are tested.

During these two stages of optimisation the other parameters are fixed constant. The poly-Si layer thickness is fixed to be 250 nm (on flat layer), which is achieved by using a-Si deposition time of 113 min with a deposition rate of 2.2 nm/min. The ion dosage for the flat n^+ and p^+ layers are fixed to be 6 e15 ion/cm^2 and 5 e15 ion/cm^2 respectively. The ion dosage for the textured n^+ and p^+ layers are fixed to be 1 e16 ion/cm^2 and 7.5 e15 ion/cm^2 respectively. These values are 1.7 time greater than the values mentioned for flat surfaces to compensate the increased surface area in the textured wafers caused due to the pyramidal structures.

3.5.1.1 t-SiO_x grown at 600°C, 6 min

The results discussed in this section are based on Figure 3.12 Top (n^+ layer) & Bottom (p^+ layer).

Flat n^+ CSPC –The maximum iV_{OC} achieved when annealed at 900°C is 695 mV. This shows that there is enough chemical passivation by the t-SiO_X layer and there is still room for increasing the field-effect passivation. There is no significant improvement in the passivation quality when the annealing time is increased from 20 min to 30 min. Implied V_{OC} as high as 734 mV is achieved by using this oxide growth condition when annealed at 950°C for 5 min. Annealing time lower and higher than 5 min leads to the loss in passivation, which arises due to insufficient and excess in-diffusion in the bulk [20], [58].

Textured n^+ CSPC – The passivation trend is similar to that of the flat n^+ CSPC layers. The decrease in iV_{OC} compared to that of the of the flat wafers can be attributed to the extra defect started that are created on the surface of the silicon bulk when texturing. In thermal budgets at 900°C the difference with the corresponding flat samples are only few mV. On the other hand, in thermal budgets at 950°C there is at least 10 mV difference between the corresponding samples. It is trusted that with hydrogenation the passivation can be further increased.

Flat p^+ CSPC – An increasing trend is seen along the thermal budget from 900°C, 10 min to 950°C, 5 min; after which there is a drop in iV_{OC} at 950°C, 15 min. The maximum iV_{OC} obtained is 700 mV and an increase in iV_{OC} of more than 20 mV is experience in hydrogenation, which is explained In Chapter 4. Hence it can be concluded that, for oxide growth condition of 600°C, 6 min irrespective of the type of doping, 950°C, 5 min post-implantation annealing performs the best for flat samples.

Textured p^+ CSPC – That main inference is that as the annealing time increases, the passivation quality of the textured p^+ CSPC layer decreases irrespective of the annealing temperature. Similar passivation of about 656 mV is achieved for the annealing conditions 900°C, 10 min and 950°C, 2 min. Hence, without any further study it can be concluded that the annealing temperature of 950°C is suitable for all the four different poly-Si passivating contacts

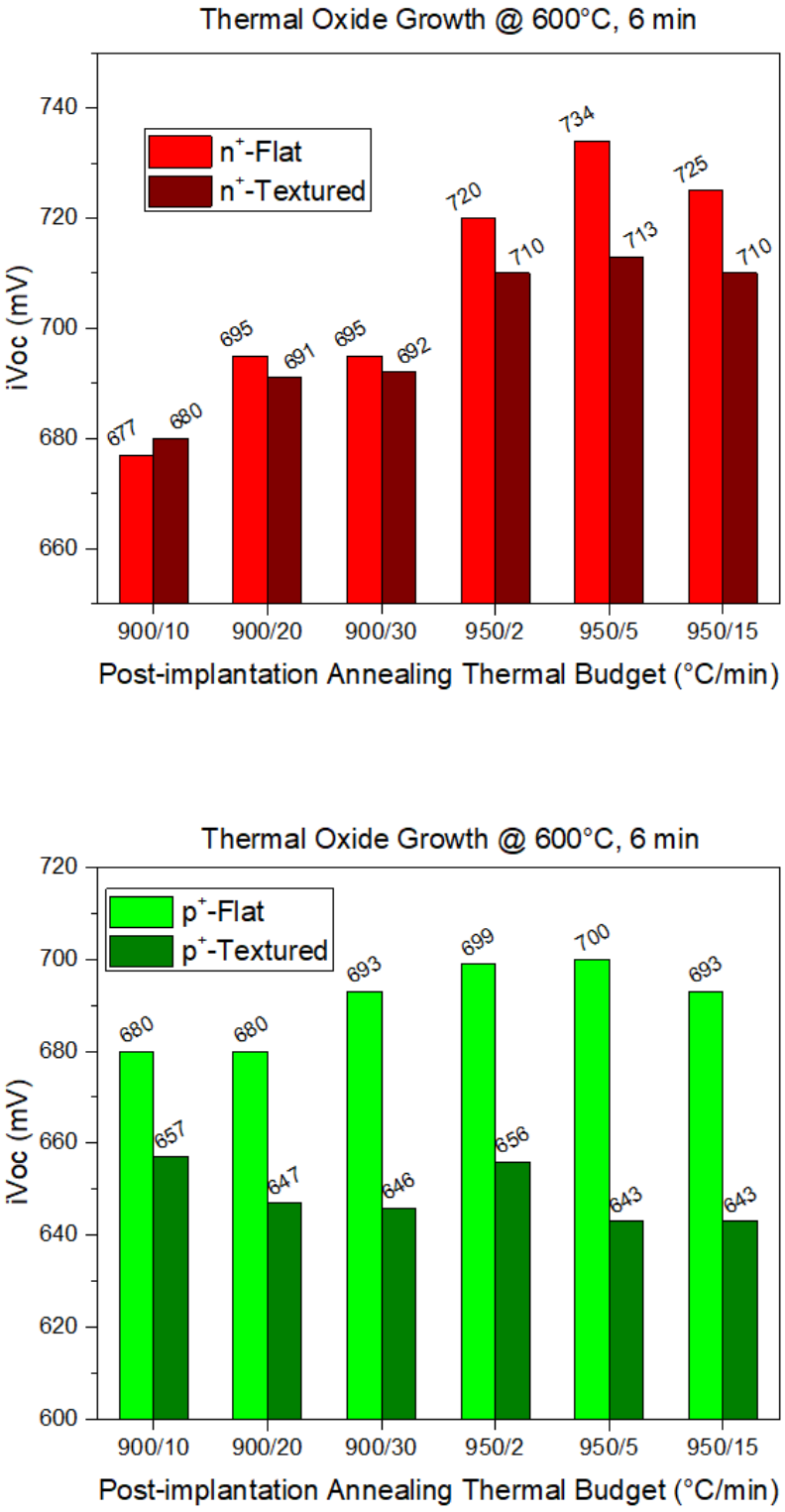


Figure 3.12 Passivation quality of thermal oxide grown at 600°C, 6 min with respect to the increase in post-implantation annealing thermal budget. Top: For textured(wine) and flat(red) n^+ poly-Si CSPC. Bottom: For textured (olive) and flat (green) p^+ poly-Si CSPC. NOTE: Along x-axis the values are expressed in (Temperature/Time) and it's not the rate of change of temperature.

3.5.1.2 t-SiO_x grown at 675°C, 6 min

The results discussed in this section are based on Figure 3.13 Top (n^+ layer) & Bottom (p^+ layer).

Flat n^+ CSPC – The maximum iV_{OC} achieved using this oxide conditions is 636 mV when annealed at 950°C for 5 min, which is about 100 mV smaller than value achieved using the previous oxide condition. The passivation at 900°C is still lower compared to that of passivation at 950°C. The inference is that at this oxide growth condition the thickness of the t-SiO_X should have exceeded 2 nm, which makes the dopant diffusion of atoms harder than before.

Textured n^+ CSPC – On the other hand, the passivation when annealed at 950°C for 15 min is similar to that of the sample annealed at 950°C for 5 min (t-SiO_X at 600°C, 6 min) since the extra annealing time has helped reduce the barrier for the in-diffusion in the bulk to have a shallow doping profile as mentioned in section 3.1.3. A significant low passivation effect is observed in the samples annealed at 900°C.

Flat p^+ CSPC – An increasing trend is seen along the increase in thermal budget for annealing. An iV_{OC} of 708 mV higher than the one achieved from the previous oxide layer is obtained when annealed at 950°C for 15 min. The increased annealing time to get better passivation gives an additional proof that the thermal oxide thickness is slightly higher than the former. An overall increase in performance is observed compared to the corresponding n^+ flat layers except at the last annealing condition.

Textured p^+ CSPC – An increase of 15 mV is notices compared to the previous oxide condition with the passivation of 672 mV at 950°C, 5 min annealing condition. The overall performance of the textured p^+ layers is better than the previous thermal oxide.

It is obvious that this oxide growth condition is not well suitable for the flat samples, but still works good for n^+ textured CSPC and way better for p^+ textured CSPC. It is due to the fact that the thickness of the oxide grown on the flat surface is slightly higher than the thickness of the oxide grown on the textured surface at same conditions. But in the event of making an Interdigitated Back Contact (IBC) solar cell with textured n^+ and p^+ poly-Si carrier selective layers, this oxide condition with post-implantation annealing at 950°C, 15 min can be used for the better performance.

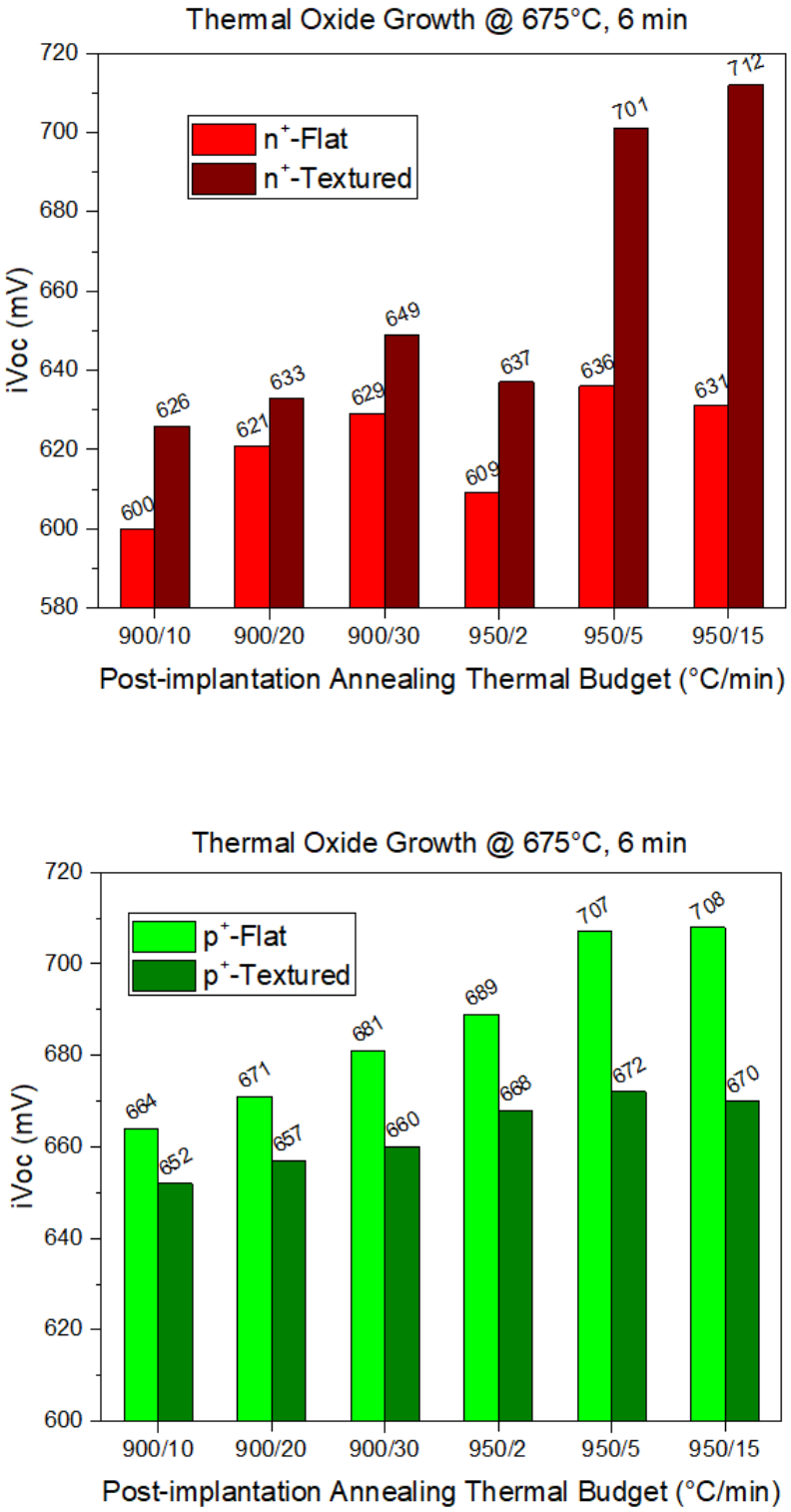


Figure 3.13 Passivation quality of thermal oxide grown at 675°C, 6 min with respect to the increase in post-implantation annealing thermal budget. Top: For textured(wine) and flat(red) n^+ poly-Si CSPC. Bottom: For textured (olive) and flat (green) p^+ poly-Si CSPC. NOTE: Along x-axis the values are expressed in (Temperature/Time) and it's not the rate of change of temperature.

3.5.1.3 t-SiO_x grown at 675°C, 8 min

The results discussed in this section are based on Figure 3.14 Top (n^+ layer) & Bottom (p^+ layer). This Oxide growth condition is tested to check if there is any significant rise in passivation for the textured samples.

Flat n^+ CSPC – All the samples show a poor passivation irrespective of the annealing condition. This is due to the formation of even thicker oxide layer at 675°C, 8 min. This shows that there is significant chemical passivation in all the samples and a weak field-effect passivation due to the confinement of all the phosphorous atoms in the poly-Si layer and a high barrier for tunnelling of charge carriers.

Textured n^+ CSPC – Similar behaviour is observed as that of flat samples. But there is a meagre field-effect passivation unlike the flat sampled due to the comparatively thinner oxide formed on the textured layer.

Flat p^+ CSPC – Unlike the n^+ samples the passivation of samples annealed at 950°C have similar behaviour as that of the samples with t-SiO_X grown at 675°C, 6 min. This owes to the facts that the diffusion of boron is much faster than that of phosphorous under same conditions [46].

Textured p^+ CSPC – The passivation at 950°C, 5 min is similar to the previous oxide condition but there is no significant improvement in the passivation quality.

The main summeries drawn based on this stage of optimisation are as follows,

- Irrespective of the oxide growth condition both flat and textured n^+ poly-Si CSPC have better passivation when annealed at 950°C, 5 min. The best passivation is shown with the oxide growth condition of 600°C, 6 min – 734 mV for n^+ flat and 713 mV for n^+ textured.
- For flat p^+ poly-Si CSPC the best passivation (708 mV) is achieved with oxide growth at 675°C, 6 min and the annealing conditions 950°C, 5 min and 15 min. For textured p^+ poly-Si CSPC the best passivation (672 mV) is achieved with both oxide growth conditions at 675°C, 6 min and 8 min and annealing conditions 950°C, 5 min.

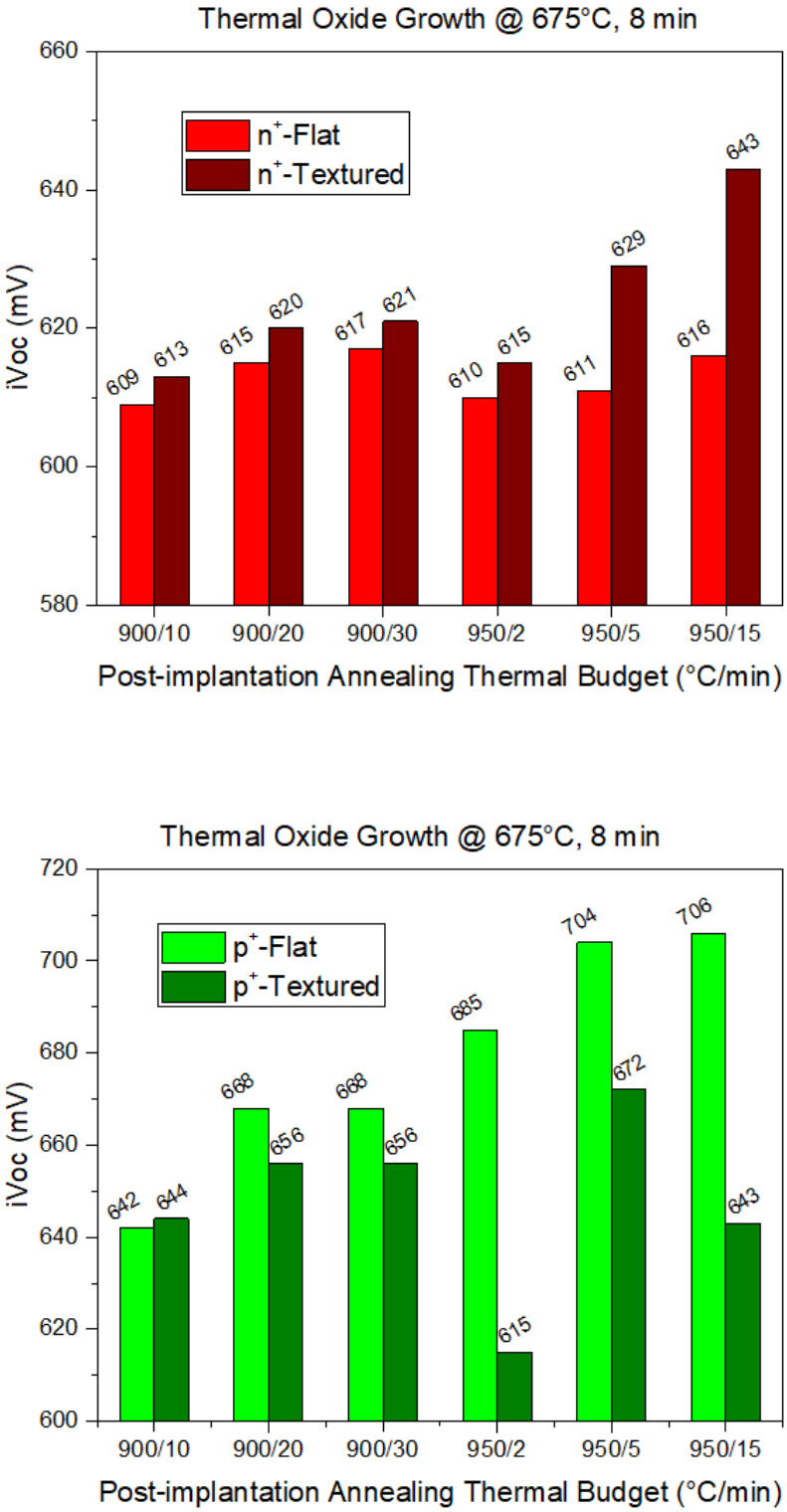


Figure 3.14 Passivation quality of thermal oxide grown at 675°C, 8 min with respect to the increase in post-implantation annealing thermal budget. Top: For textured(wine) and flat(red) n^+ poly-Si CSPC. Bottom: For textured (olive) and flat (green) p^+ poly-Si CSPC. NOTE: Along x-axis the values are expressed in (Temperature/Time) and it's not the rate of change of temperature.

3.5.1.4 t-SiO_x grown at 675°C, 3 min

From the previous round of optimisation, it is clear that a post-implantation annealing condition of 950°C, 5 min is suitable for all the four different kinds of samples. But this annealing condition cannot be fixed, since changing the oxide growth conditions have significant influence on the post-annealing conditions. Hence, only the annealing temperature is fixed at 950°C and further two lower annealing time of 0.5 and 2.2 min are decided to be studied. A low oxide growth thermal budget (600°C, 6 min) is suitable for n^+ poly-Si CSPC and a higher thermal budget (675°C, 6 min) is suitable for p^+ poly-Si CSPC. As a single optimal condition is needed for both the n^+ and p^+ CSPCs a thermal budget between these two conditions is decided to be tested. Hence, a second round of optimisation is carried out at an oxide growth condition of 675°C, 3 min.

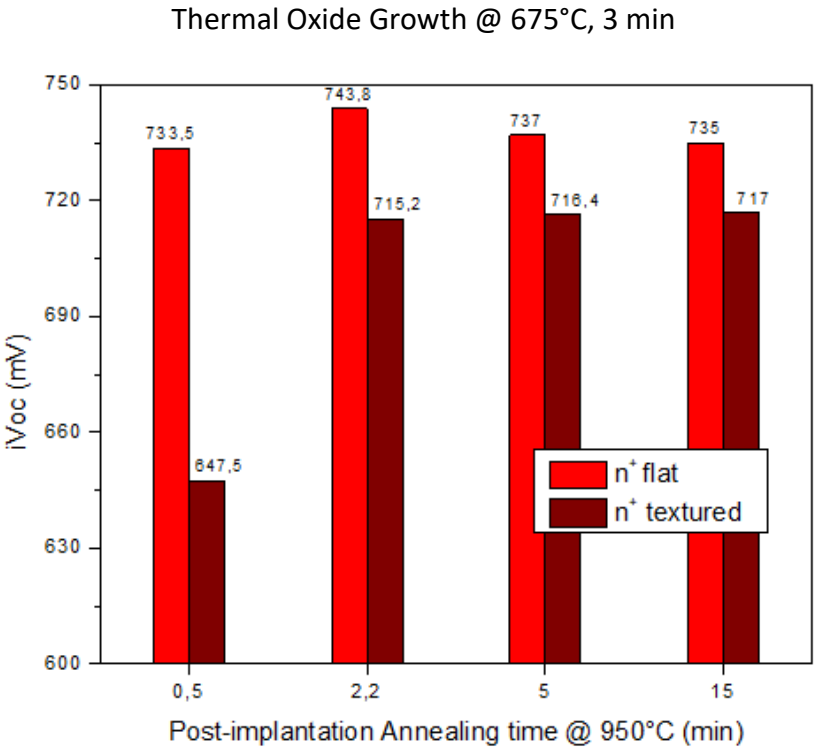
The results discussed in this section are based on Figure 3.15 Top (n^+ layer) & Bottom (p^+ layer).

n^+ CSPC - The best passivation so far is achieved for both the flat and textured samples with this thermal oxide. When annealed at 950°C for 2.2 min, a passivation quality as high as 743,8 mV is observed for the flat samples. Higher passivation effects at annealing times 2.2, 5 and 15 mins (715.2, 716,4 and 717 mV) are experienced compared to the best result (713 mV) of the previous optimisation for textured samples. But, the increase in passivation quality is very feeble.

p^+ CSPC – The best passivation achieved for flat sample is 706 mV (2 mV less than pervious optimum) when annealed for 2,2 min and there is a decreasing trend in the iV_{OC} as the annealing time increases. Whereas, the best passivation achieved for textured sample is 674 mV (2 mV higher than pervious optimum) when annealed for 0.5 min and there is a decreasing trend in the iV_{OC} as the annealing time increases.

In conclusion, except for the textured p^+ poly-Si CSPC the best passivation is achieved at annealing time of 2,2 min at 950°C. A lower annealing time of 0.5 min is need for the textured p^+ poly-Si CSPC for the optimum.

A comparison of different thermal budget for oxide growth at same post-implantation annealing condition is made in the following section.



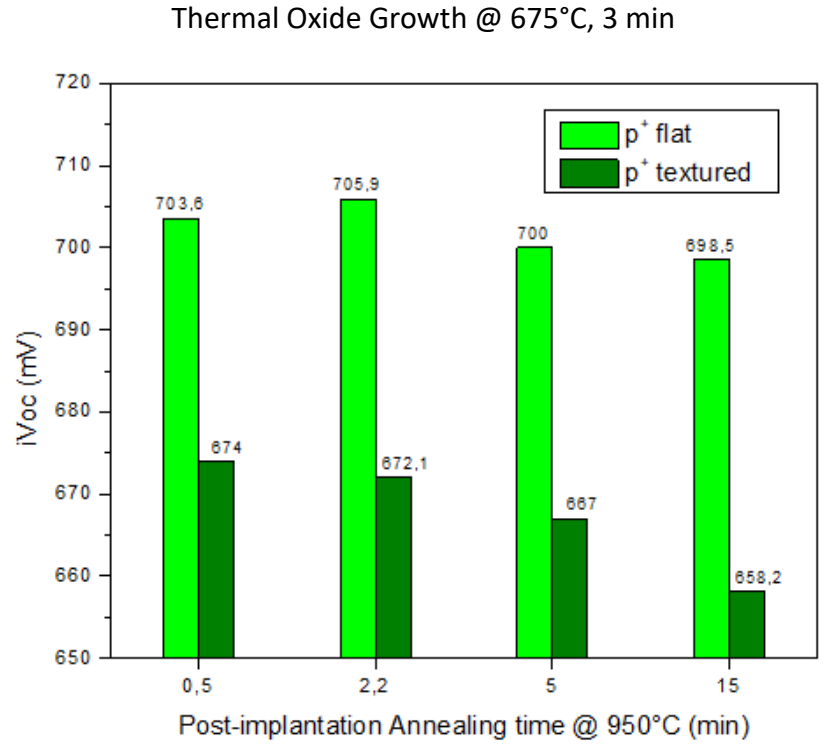


Figure 3.15 Passivation quality of thermal oxide grown at 675°C, 3 min with respect to the increase in post-implantation time at 950°C. Top: For textured(wine) and flat(red) n+ poly-Si CSPC. Bottom: For textured (olive) and flat (green) p+ poly-Si CSPC.

3.5.1.5 Thermal Oxide comparison at same annealing conditions (950°C, 5 min)

As mentioned in section 3.1, the oxidation condition influences the silicon oxide thickness and the uniformity. In this section the comparison is made between the different thermal oxidation conditions used to analyse the quality and thickness of the t-SiO_X. The results and inferences are based on Figure 3.16. From Figure 3.1, an oxide thickness between 1.2 - 1.8 nm showed better optimisation for both n^+ and p^+ CSPC [42]. With the passivation quality at respective oxide growth condition the approximate oxide thickness can be expected.

n^+ CSPC - It is inferred that both the textured and flat samples performs best at lower thermal budgets, showing a proper balance between the chemical passivation and field-effect passivation. At higher thermal budget (675°C, 8 min), the thickness of the oxide becomes too thick, thus hindering the ease at which the charge carrier can tunnel though. It is interesting to note that at oxidation condition of 675°C, 6 min the textured sample still shows better field-effect passivation compared to that of the flat sample. It can be understood in two ways. Firstly, the thickness of the oxide grown on the flat surface is thicker compared to the one grown on the textured surface at same oxide growth conditions due to the increased area of reaction arising due to texturing. Secondly, the defects in the textured surface lead to non-uniform layer of SiO_X on oxidation leading to pinhole like structures on high temperature annealing, enabling direct charge carrier collection.

p^+ CSPC – For the flat and textured samples the best performance is at higher thermal budget. As mentioned in section 3.1.5 the diffusion of boron is two orders of magnitude higher than that of phosphorous in silicon substrate. So, when thinner oxide is used most of the boron should easily diffuse through and reach the bulk giving rise to loss in field-effect passivation. On the other hand, when a thicker thermal oxide is used, the barrier for the boron atoms to reach the bulk increases giving rise to less in-diffusion area leading to better field-effect passivation.

But, still the textured p^+ poly-Si CSPC shows poor passivation quality as compared to the rest. To further optimise this layer, it is decided to understand in depth the effect of annealing time and oxide growth condition on the dopant profile with the help of Electrochemical capacitance-voltage (ECV) measurements.

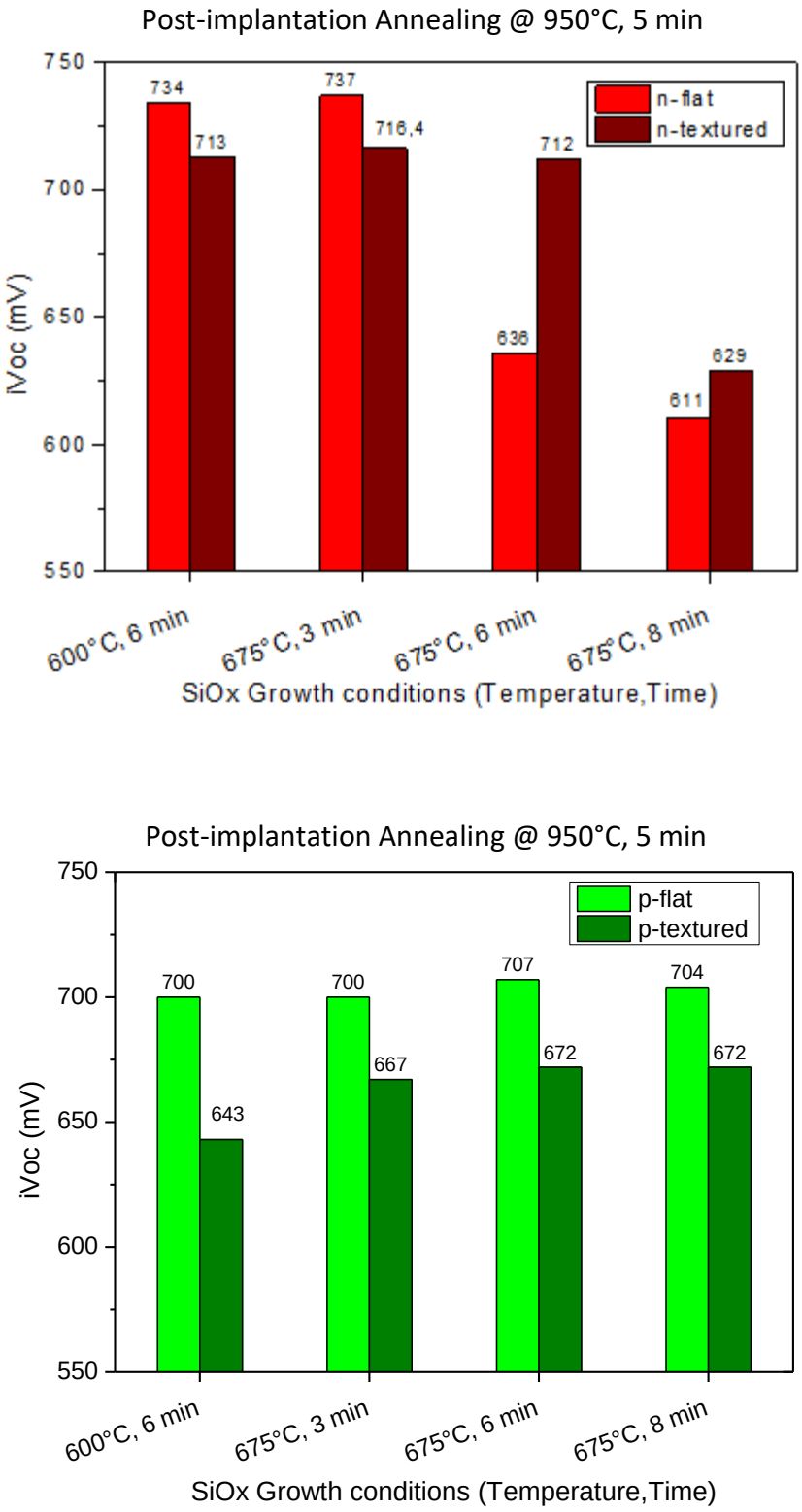


Figure 3.16 Passivation quality with respect to different thermal oxide conditions when annealed at 950°C, 5min. Top: For textured(wine) and flat(red) n+ poly-Si CSPC. Bottom: For textured (olive) and flat (green) p+ poly-Si CSPC.

3.5.2 ECV measurements of textured p^+ poly-Si CSPC

The ECV measurement helps us analyse the carrier distribution in the poly-Si/SiO_X/c-Si interface. The influence of the post-annealing time and oxide growth condition are studied in this section with the help of Figure 3.17.

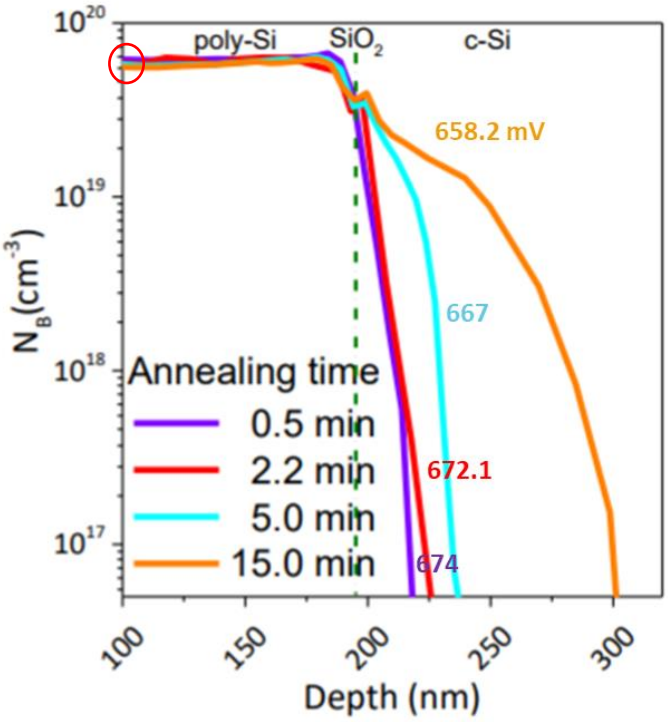
3.5.2.1 Influence of Post-implantation annealing time

It can be seen that, the in-diffusion area increases as the annealing time increases. But in all the conditions there is a uniform dopant profile in the poly-Si region. The passivation quality of the CSPC decreases as the in-diffusion area increases, which is explained by the decrease in iV_{OC}. As, the annealing time increases the thermal stress experienced by the boron atoms is prolonged giving rise to a higher in-diffused area. When annealed at 950°C, 15 min the in-diffused area extends to 100 nm down the bulk. On the other hand, when annealed only for 2.2 min the in-diffused area is reduced to one-fourth (~ 25 nm). When the in-diffused area is reduced one-fourth there is a 14 mV rise in $iV_{OC.}$ Also, at the interface of the bulk and poly-SI layer there should be a significant change in the doping concentration to achieve better field-effect passion. This trend is difficult to observe in this plot (Figure 3.17 Top)

3.5.2.2 Influence of Oxide Growth conditions

Similar trend is observed with increase in the thermal budget for oxidation. As the thermal budget increases the in-diffusion area decreases. The least thermal budget (600°C, 6 min) creates an in-diffusion area of around 70 nm and the highest thermal budget (675°C, 8 min) leaves an in-diffusion area of around 40 nm. A 30 nm decrease in the in-diffused area has given rise to an increase in iV_{OC} of about 30 mV. The dopant distribution in the poly-Si layer is again uniform irrespective of the oxidation conditions. Also, at the interface in the Figure 3.17 bottom (green dotted line), it is clear that as the thermal budget increases there is a notable decrease in boron concentration. The highest thermal budget (675°C, 8 min) has a boron concentration of 10^{19} cm^{-3} at the interface which performs the best. Whereas the least thermal budget (600°C, 6 min) has a boron concentration of 5 e19 cm^{-3} at the interface. So, it can be concluded that higher the difference in doping concentration at the poly-Si/c-Si interface better id the field-effect passivation.

Thermal Oxide Growth @ 675°C, 3 min



Post-implantation Annealing @ 950°C, 5 min

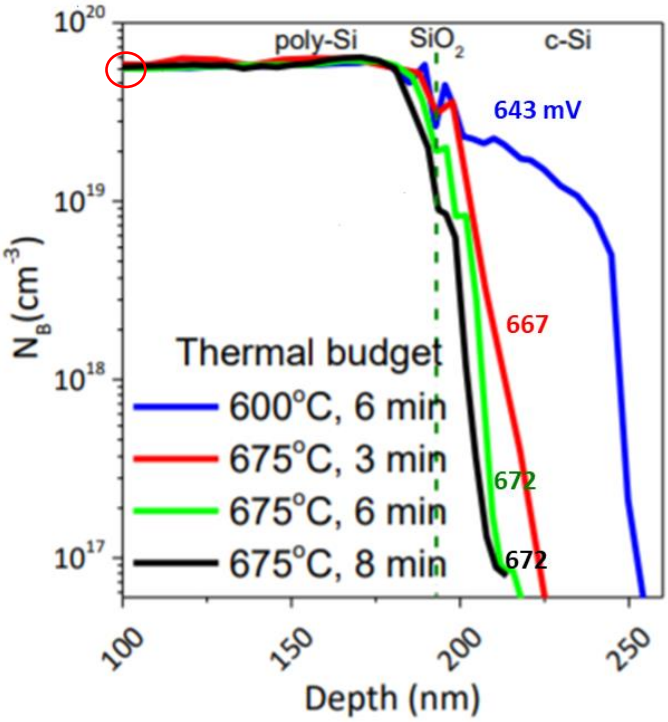


Figure 3.17 Electrochemical Capacitance-Voltage (ECV) measurement for the p^+ poly-Si CSPC. The plot shows the Boron concentration along the course of poly-Si/SiOX/c-Si. Top: Variation of the doping profile with change in post-implantation annealing time at 950°C. Bottom: Variation of the doping profile with change in Oxide Growth conditions. NOTE: The samples used for ECV are same as the samples used in Figure 3.15. The red circle on the x-axis of both the plots shows a doing concentration of ~6 e19 cm^{-3}.

One of the main findings from both the plots of Figure 3.17 is that in the poly-Si layer the concentration of boron is around 6 e19 cm^{-3} (red circle) when an ion-implantation dosage of 7.5 e15 ion/cm^2. Experimentation and simulation result shows that for a poly-Si layer of around 250 nm, the best passivation effect is observed when the doping concentration is above 1 e 20 cm^{-3} in the poly-Si region [59], [58]. Hence, it is decided to increase the doping concentration by varying the ion dosage used during the implantation process. The effect of increasing the doping concentration is explained in the following section.

3.5.3 Doping Concentration of textured p^+ poly-Si CSPC

Section 3.1.4 studies the solubility of the dopants in silicon substrate. The same applies for the analysis of the influence of the boron concentration in textured p^+ poly-Si CSPC. The conductivity of the charge carrier increases as the doping concentration increases [60]. On the other hand, excessive doping can lead to saturation of the dopants leading to inactivated dopants behaving as recombination centres [48]. Previously, the ion dosage used for the textured p^+ poly-Si samples is 7.5 e15 ion/cm^2. Two increased ion dosage of 1 e16 and 1.5 e16 ion/cm^2 were tested to check if an increase in doping concentration leads to better passivation effects. Figure 3.18 shows the effect of increasing the boron concentration on passivation quality of the contacts.

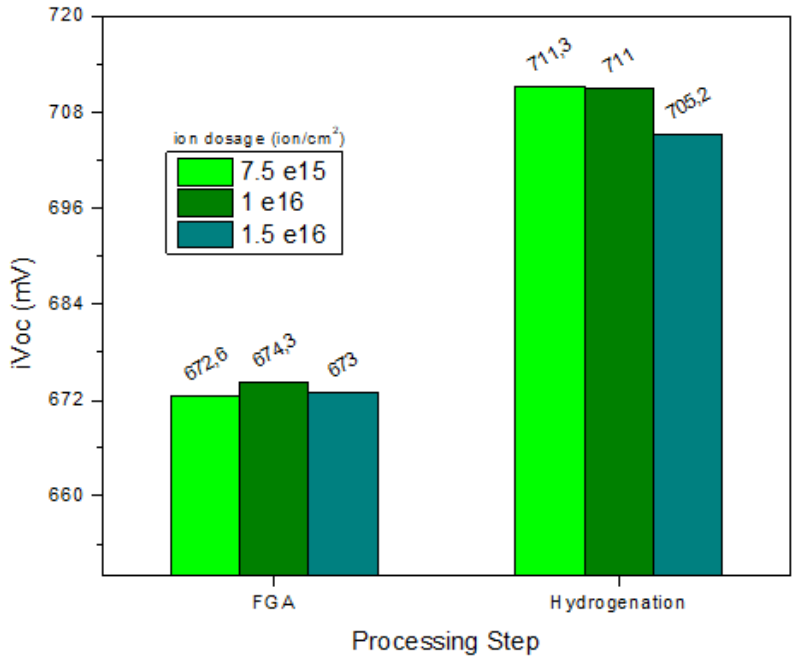


Figure 3.18 Passivation quality of textured p^+ poly-Si CSPC with increase in doping concentrations before and after hydrogenation.

It is clear from the plot that after post-implantation annealing followed by FGA there is no significant change in the passivation quality. This might due to the fact that the chemical passivation of the different samples is not uniform. Hydrogenation helps in increasing the chemical passivation of the samples (Explained in detail in CHAPTER 4). After hydrogenation, it is found that both the ion dosage 7.5 e15 and 1 e16 ion/cm^2 have same passivation effects of 711 mV. Whereas, the sample with an ion dosage of 1.5 e16 ion/cm^2 showed a 6 mV drop in the passivation quality of the contact. An high doping level, the recombination at the metal-semiconductor interface is also lowered, which in turn leads to the reduction in the contact resistivity of the interface [5].

The minority carrier lifetime (τ_{eff}) at minority carrier density (Δn) 1 e15 cm^{-3} for the all the three different samples after FGA were 0.7 ms. After hydrogenation the lifetime increased to 1.8 ms for the sample with 7.5 e15 ion/cm^2 ion dosage and to 1.7 ms for the sample with 1 e16 ion/cm^2 ion dosage. The lifetime of the heavily doped samples showed a little declivity in the lifetime (1.54 ms) which might have occurred due to Auger recombination becoming dominant. Hence, the Front Back contacted solar cells and the contact resistivity (ρ_C) measurement in this thesis were fabricated with a textured p^+ poly-Si CSPC with an ion dosage of 1 e16 ions/cm^2.

3.5.4 Thickness of poly-Si layer

In this section the influence of the passivation quality of the CSPC by the thickness of the poly-Si layer is studied. As discussed in section 3.1.3, using the optimal thickness for the chosen doping concertation and annealing time will improve the optical and electrical properties of the device. In Figure 3.19, the top x-axis shows the corresponding thickness of the a-Si layer (later annealed to poly-Si) for the deposition time on the bottom x-axis. It can be seen that the thickness of the textured a-Si layer is less than the corresponding flat a-Si layer by a factor of 1.25 due to the increase in surface area due to the pyramidal structures. Note: The thickness values are calculated from the a-Si deposition rate, which is 2,2 nm/min.

n^+ CSPC – Thinner poly-Si layers shows poor passivation qualities compared to the thicker ones. It arises due to the inadequate field-effect passivation. In thinner poly-Si these is an expected non uniform distribution of dopants within the poly-Si layer and excess in-diffusion in the bulk. This affects the charge carrier collection at the contacts. The maximum passivation (743 mV) is achieved for the flat samples with a poly-Si thickness of 125 nm. When the thickness is doubled there is a 6 mV drop in the passivation raised due to deterioration in field-effect passivation. The best passivation of the textured sample (716.4 mV) is achieved at a thickness of 200 nm.

p^+ CSPC - Similar passivation is observed when 250 or 125 nm thick poly-Si is used in the CSPC for the flat sample (700 mV). In textured samples, there is a significant 11 mV rise in the iV_{OC} when the poly-Si layer thickness of 100 nm is doubled. Thinner layers can still be optimised to show better passivation effects by optimising the doping concentration and the post-implantation annealing time.

When an IBC solar cells is decided to have textured p^+ and n^+ poly-Si layers, then a deposition time of 113 min has to be used for the better performance for the confirmed doping concentration and annealing conditions. On the other hand, for an IBC solar cell with flat carrier selective layers a deposition time of 57 mins still gives a better passivation, which will lead to parasitic absorption.

Now it is also important to analyse the influence of these above discussed parameters in the contact resistivity of the CSPC layers, which is discussed in the following section.

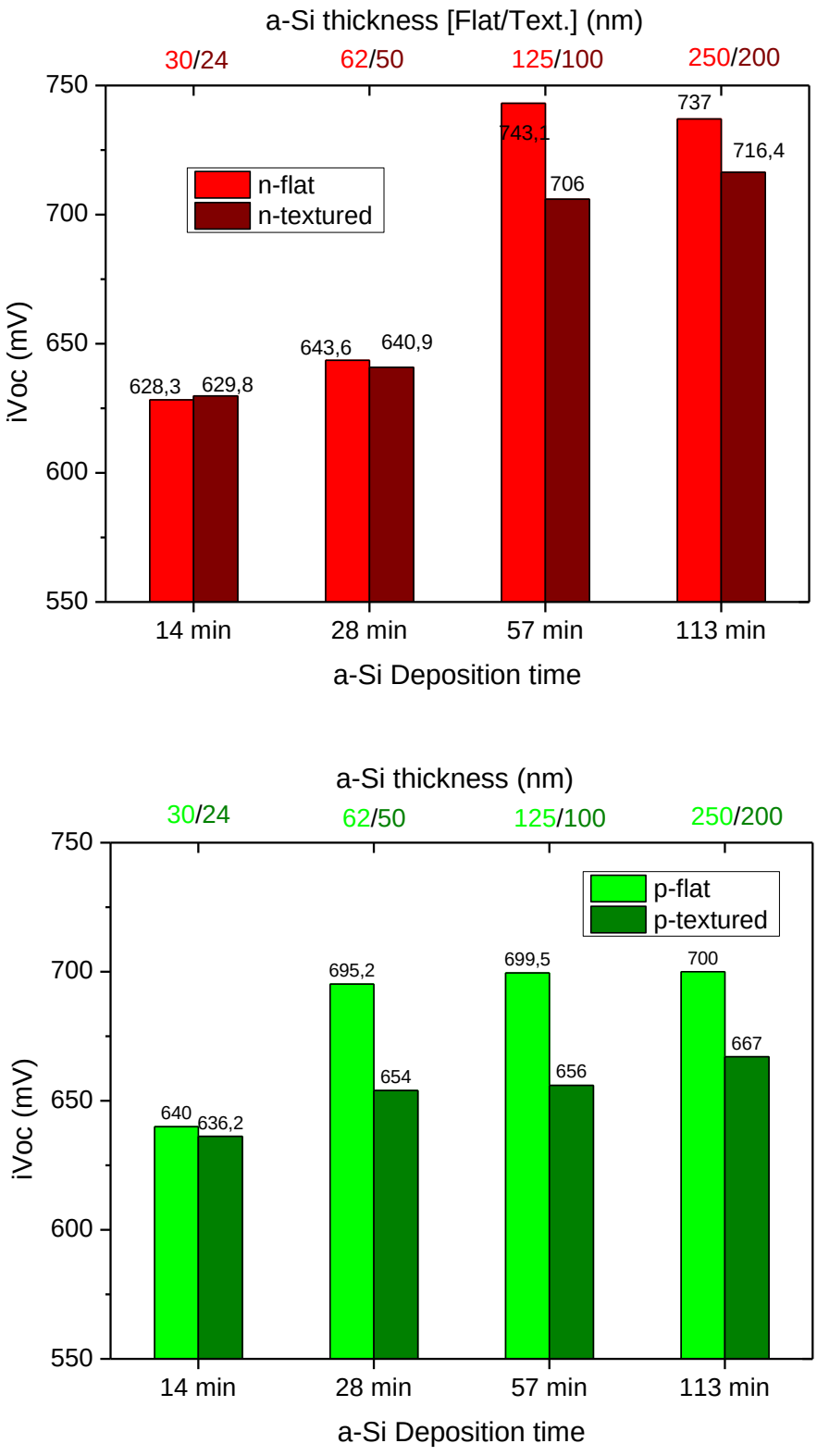


Figure 3.19 Passivation quality of poly-Si CSPC with respect to change in the thickness of the poly-Si layer (top x-axis) or with respect to the a-Si deposition time (bottom x-axis). Top: For textured(wine) and flat(red) n+ poly-Si CSPC. Bottom: For textured (olive) and flat (green) p+ poly-Si CSPC. NOTE: Thermal oxide growth condition is 675°C, 3 min and Post-implantation Annealing is done at 950°C, 5 min

3.5.5 Contact resistivity of CSPC

In this section the effect of the different annealing conditions and oxide growth conditions on the contact resistivity (ρ_C) of the CSPC is studied. For the n^+ poly-SI CSPC analyses are done for both the changes in post-implantation annealing time and thermal budget of oxidation. For the p^+ poly-Si CSPC only the effect of different annealing time at the oxidation condition of 675°C, 3 min is studied because it is just to check if measuring a p^+ poly-SI layer on a p-type bulk will give a reasonable contact resistivity in accordance with the literature. The contact resistivities are measured with the help of TLM measurements and samples are prepared as explained in section 3.4.2. **Note:** Thickness of poly-Si used is 250 nm (flat) [a-Si deposition time is 113 min]

3.5.5.1 Influence of post-implantation annealing time

n^+ CSPC – As the annealing time increases, the recombination current density (J_0) increases and the specific contact resistance (ρ_C) decreases [61]. This is due to the increase in pinhole densities deteriorating the quality of the t-SiO_X layer, which leads to loss in surface passivation. On the other hand, these pin holes results in more dopants diffusion into the c-Si surface, which leads to better field-effect passivation and low contact resistivity. The decreasing trend in the contact resistivity is seen in both the flat and textured samples when the annealing time is varied from 5 min to 10 min. Also, in all the cases the contact resistance of the n^+ CSPC are within the range 14.5 – 19 mΩ.cm^2 which is a couple of units less than the values found in the literature.

p^+ CSPC – As the annealing time increases, the solubility of the boron atoms in the poly-Si layer increases. In other words, more boron atoms get activated and the resistivity of the layer should decrease. In the last three cases, for the flat samples there is significant decrease in the contact resistivity as the annealing time increases. But for the textured samples an increasing trend is seen, which might have resulted due to the undesired current flow paths in the sample during measurement. Also, the values of contact resistivity for the p^+ CSPCs are in the range 15.5 – 31 mΩ.cm^2 which is slightly higher than the values found in literature. A critical reasoning of such a behaviour is done in section 3.5.5.3.

The influence of the thermal budget on the contact resistivity of the n^+ CSPC layers are analysed in the following section.

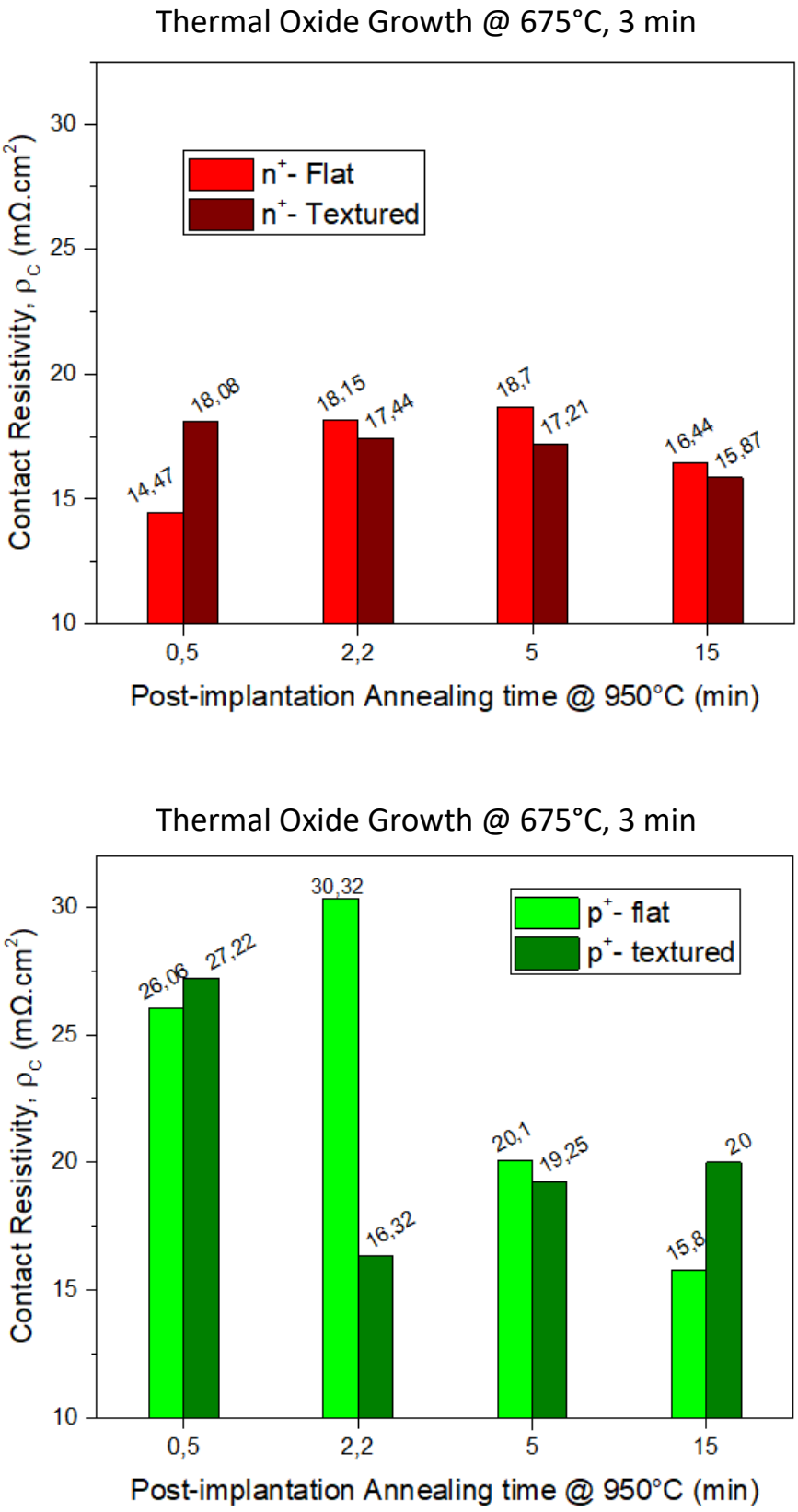


Figure 3.20 The contact resistivity of the CSPCs as a function of increasing post-implantation annealing time. Top: For textured(wine) and flat(red) n+ poly-Si CSPC. Bottom: For textured (olive) and flat (green) p+ poly-Si CSPC. NOTE: Thermal oxide growth condition is 675°C, 3 min and Post-implantation Annealing is done at 950°

3.5.5.2 Influence of Oxide Growth conditions

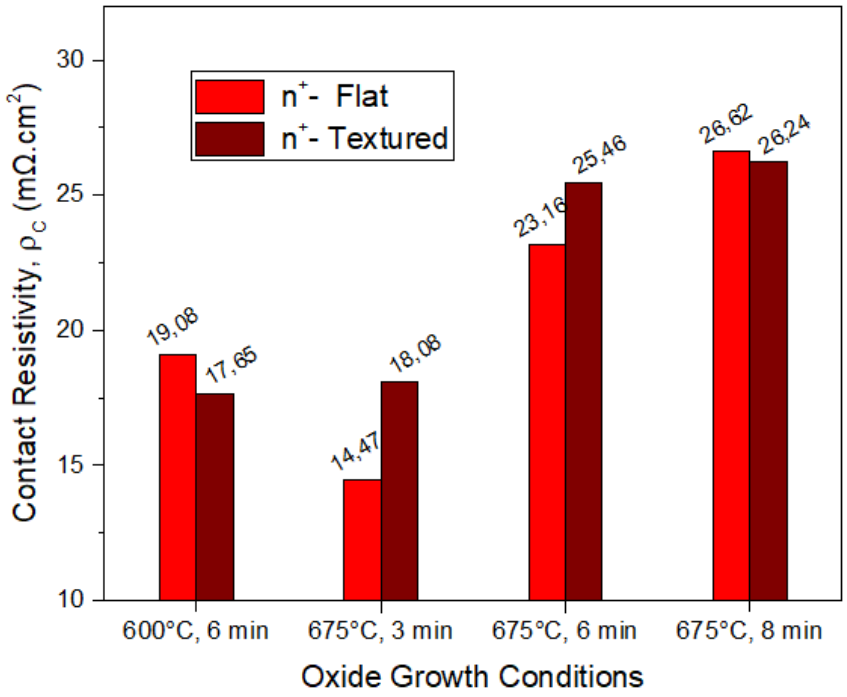
The thickness of the oxide layer greatly affects the contact resistivity of the carrier selective contact. As the thickness of the t-SiO_X increases the resistance for the charge carrier to be collected is increases. In other words, the barrier for tunnelling of charge carriers to pass through the oxide increases [42]. In this section the impact of the oxide growth condition on different annealing time is analysed only for the n^+ CSPC layers. Form Figure 3.21 it can be concluded that the thermal oxide growth condition 675°C, 3 min give the thinner thermal oxide (showing least contact resistivity). The best passivation shown by this t-SiO_X in Section 3.5.1.5 is in concordance with this analogy.

Similar trend in the contact resistivity is followed in all the annealing conditions. Considering all the cases, the contact resistivity for the highest two thermal budgets ranges between 20 – 29 mΩ.cm^2 (flat) and 20 – 27 mΩ.cm^2 (textured). The very meagre decrease in the upper limit of the range might be attributed to the fact that the thickness of thermal oxide is relatively thinner on the textured surface compared to that on the flat surface at same oxidation conditions. For the lowest two thermal budgets the range of the contact resistivity is between 14.5 – 19 mΩ.cm^2 (flat) and 16.5 – 18 mΩ.cm^2 (textured). These values at lower thermal budgets for oxidation are similar to the values found in the literature. There is almost 10 mΩ.cm^2 difference between the lower and higher thermal budgets used for oxidation.

Comparing the effects of both thermal budget for oxidation and annealing time it can be concluded that as the annealing time increases the contact resistivity decreases due to the better activation of the dopants and if the thermal budget used in oxidation is high the contact resistivity increases. So, to have the least contact resistance as possible higher annealing time and lower thermal budget for oxidation has to be used. As discussed in section 3.5.2.1 using higher annealing time increases the in-diffusion area of the bulk leading to loss in field-effect passivation. Hence a moderate annealing time has to be chosen as a trade-off between low contact resistivity and better passivation quality. As a result, an annealing time of 5 min at 950°C is chosen while processing the solar cells.

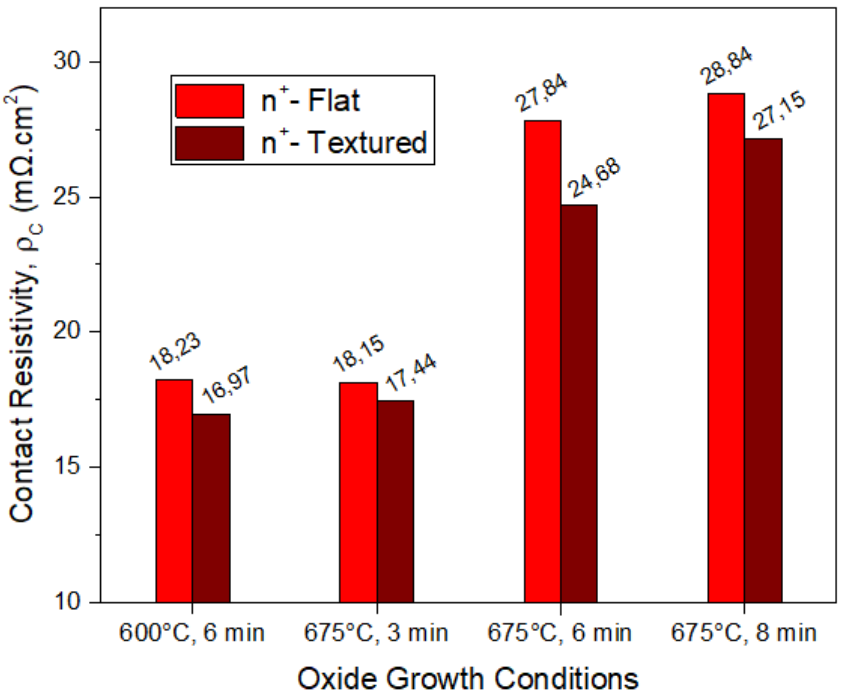
The drawbacks in the sample structure and the suspected error in the contact resistivity readings are discussed in the following section.

Post-implantation Annealing @ 950°C, 0.5 min

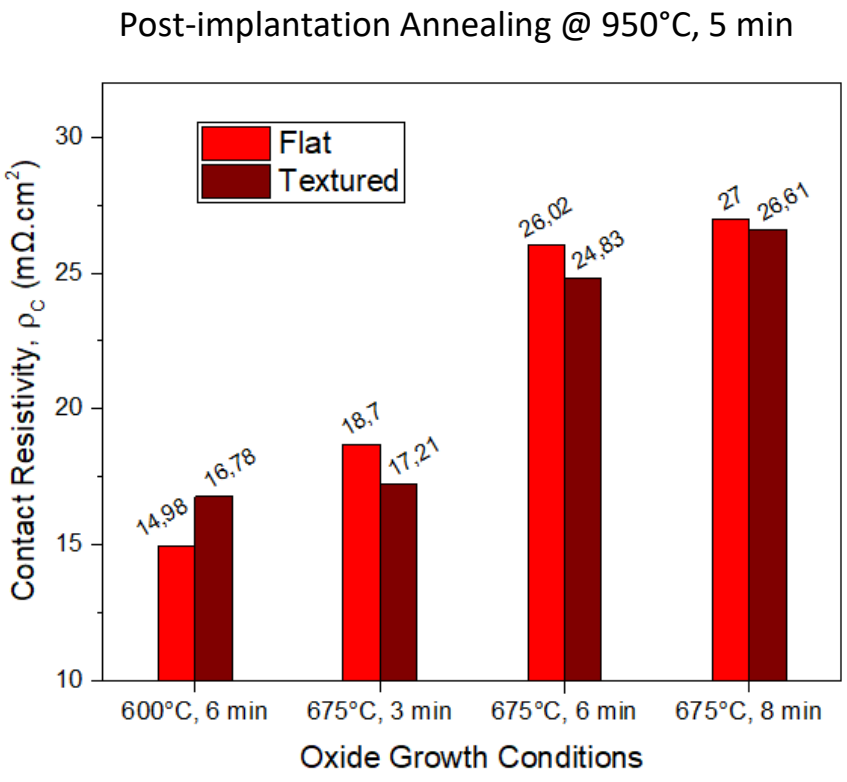


(A)

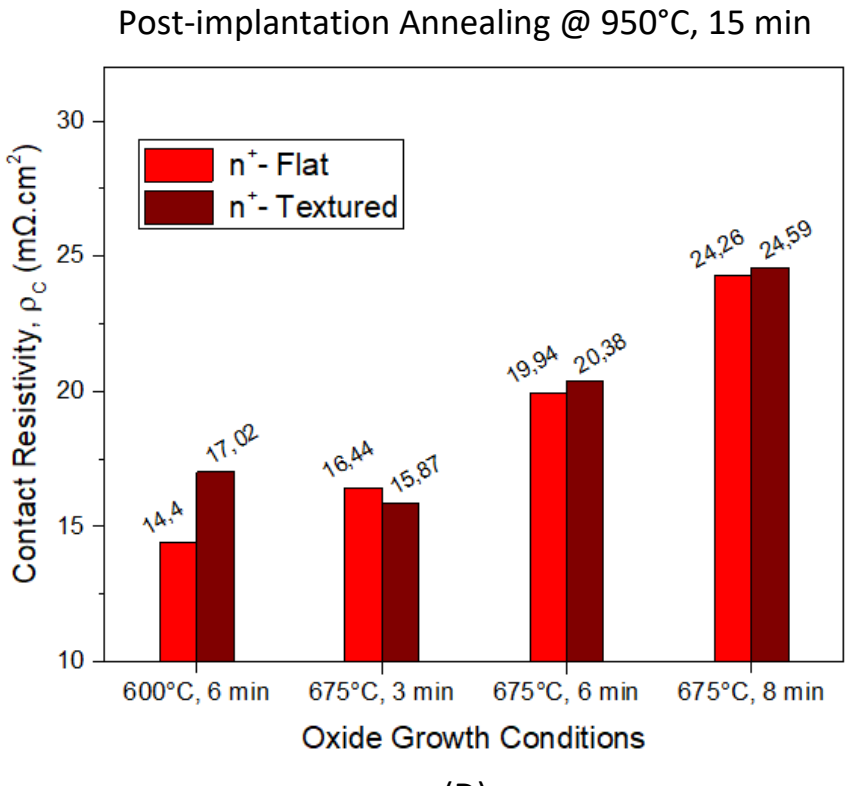
Post-implantation Annealing @ 950°C, 2.2 min



(B)



(C)



(D)

Figure 3.21 The contact resistivity of the CSPCs as a function of different thermal budget used for oxidation. Plots A, B, C and D represents the data when post-implantation annealing is carried out at 950°C for 0.5, 2.2, 5 and 15 min respectively.

3.5.5.3 Critical interpretation on Contact Resistivity measurement

The Contact resistivities measured from the TLM (Transfer Length Measurement) for the n^+ poly-Si CSPC are in the same range as found in the literature. Previous measurements in the PVMD group resulted in a contact resistivity of 0.1 mΩ.cm^2 [20], which is not accurate. In this section, few suggestions are made to improve the accuracy of the contact resistivity measurement via TLM for the n^+ poly-Si CSPC.

The measurements made using the samples as mention in section 3.4.2 have two drawbacks. Firstly, since the poly-Si is quite conductive there will be lateral conductivity of current within and the surface of poly-Si layer as shown in the sample (1) of Figure 3.22. Hence the measured resistance values will be less than the resistance across the carrier selective contact and the bulk as not all current pass through the contact. The solution to this behaviour, is to direct the current toward the t-SiO_X layer and the bulk. This can be done by etching the poly-Si layer between the metal contacts. Such a TLM sample is as shown in the schematic (2). Gamze et al have also suggested similar etching technique to improve the accuracy of the Transfer Length Measurements [62].

Secondly, the measured contact resistivity (ρ_C) of the sample does not represent the contact resistivity of the CSPC and the bulk. It also includes the resistivity between the metal and the poly-Si layer. Equation 3.18 shows the contact resistivity (ρ_C) measured by the using the sample structure (2).

$$\rho_C = \rho_{C1} + \rho_{m-c} \qquad 3.18$$

Where, ρ_{C1} is the actual contact resistivity between the CSPC and the bulk and $\rho_{m\text{-}c}$ is the contact resistivity between the metal and poly-Si layer. If the value of $\rho_{m\text{-}c}$ is found out, then it becomes easy to predict the actual contact resistivity (ρ_{C1}). The resistivity $\rho_{m\text{-}c}$ can be easily found by using the sample structure (3). In this sample a relatively thicker SiO_X layer is used. Being a good dielectric insulator, thicker SiO_X does not allow the current to cross the poly-Si layer. Hence from this set-up the contact resistivity between metal and poly-Si layer ($\rho_{m\text{-}c}$) can be found out. Then the actual contact resistivity (ρ_{C1}) can be deduced with the help of Equation 3.18.

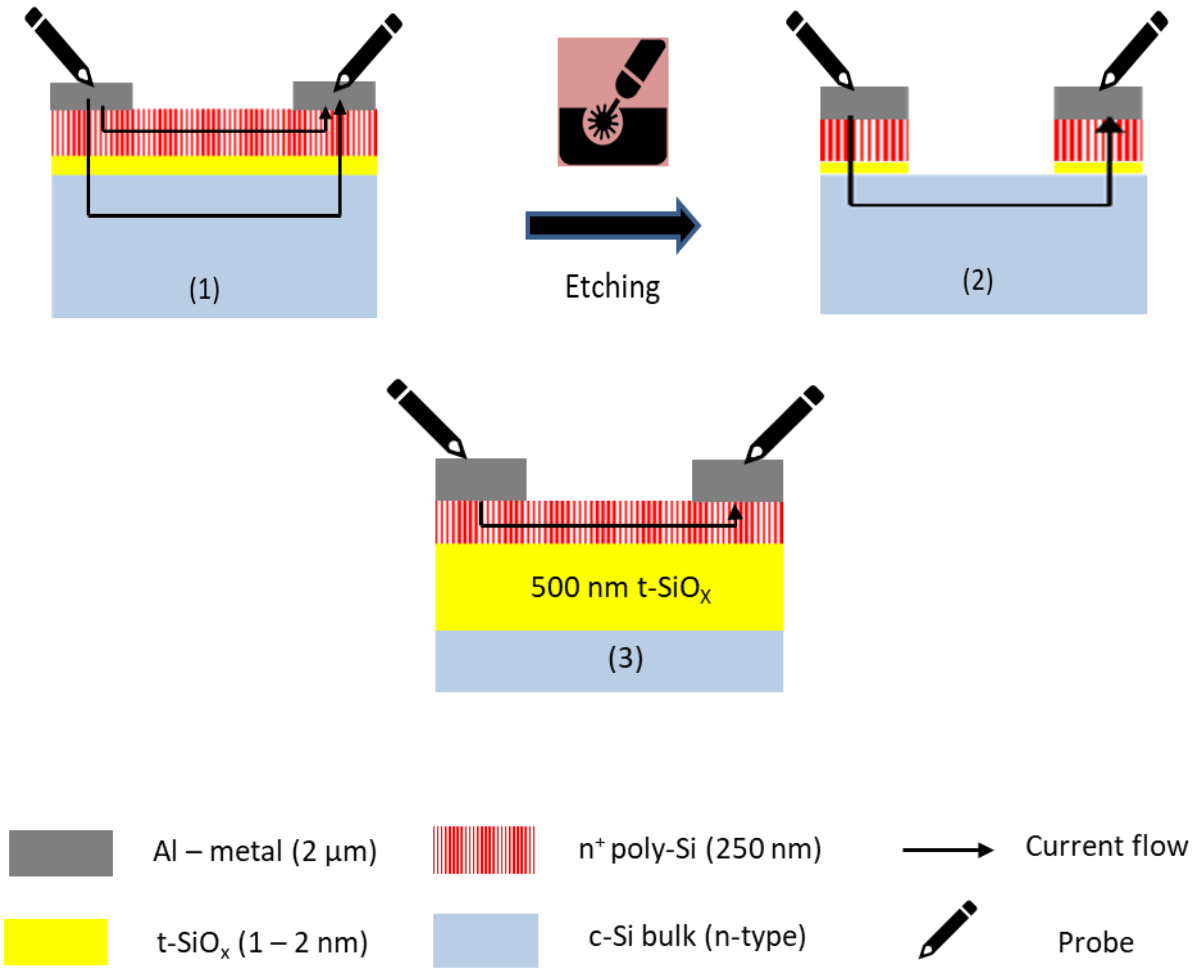


Figure 3.21 Schematic of the proposed sample structure for accurate measurement for the contact resistivity of the n^+ CSPC. Sample (1)- Continuous poly-Si layer leading to lateral conductivity. Sample (2)- Etched sample to avoid lateral conductivity. Sample (3)- With thicker oxide to find the contact resistivity between metal and poly-Si layer.

From the above two suggestions more accurate value of the contact resistivity of the contacts can be found out. Hence, the values of the contact resistivity used in this thesis have a few units deviation from the actual values due to the resistivity between the metal and poly-Si and due to the lateral conductivity of the poly-Si. The quantification of the carrier selectivity with the measured values is done in the next section.

3.5.6 Logarithmic Selectivity (S_{10}) for n^+ poly-Si CSPC

With the help of Equation 3.17 derived in section 3.2, the Logarithmic selectivity values are calculated for the n^+ poly-Si CSPC. It is to be noted that the values of contact resistivity (ρ_C) and recombination current density (J_0) used in the calculation of Logarithmic Selectivity (S_{10}) are from the different samples processed with the same operational conditions. The measurements are taken from different samples because the TLM samples are single side doped and its lifetime measurement does not yield an accurate J_0 value.

From Figure 3.22 it is clear that the S_{10} values for the flat n^+ poly-Si CSPC layers are in the range 14 – 14.5. These values are close to the ones found in the literature summarised by Schmidt et al. [63]. D. Yan et al have documented a S_{10} value of 14.5, with J_0 and ρ_C values of 5 fA/cm^2 and 16 mΩ.cm^2 respectively [64]. The best value of S_{10} achieved by is 14.33, with J_0 and ρ_C values of 6.5 fA/cm^2 and 18.7 mΩ.cm^2 respectively. In this sample, the relatively low J_0 value achieved during 5 min post implantation annealing is the driving factor the best selectivity compared to the rest, although the sample has the highest contact resistivity. The S_{10} values for the textured n^+ poly-Si are in the range 13.7 – 13.9. The contact resistivities are still in the range close to that of the flat samples. But the recombination current densities in the textured samples are almost thrice than those of the flat samples, due the defects induced on the surfaces during texturing. Hence there is a slight drop in the selectivity for the textured samples

The recombination current density values used in the Figure 3.22 are the ones without any hydrogenation process. So, after suitable hydrogenation processes, there is a considerable decrease in J_0. For instance, after hydrogenation of the flat (textured) sample annealed at 950°C for 5 min, the J_0 drops from 6.6 to 2 fA/cm^2. This rises the selectivity from 14.33 to 14.84. Similarly, for the similarly processed textured sample, the J_0 drops from 22.7 to 7.5 fA/cm^2. This reduction in J_0 increases the S_{10} value from 13.82 to 14.84.

Hence, it is obvious that the logarithmic selectivity (S_{10}) is more convenient in analysing the effect of both J_0 and ρ_C on the quality of carrier selectivity of the contacts. In the following section the main results and finding of this chapter are concluded.

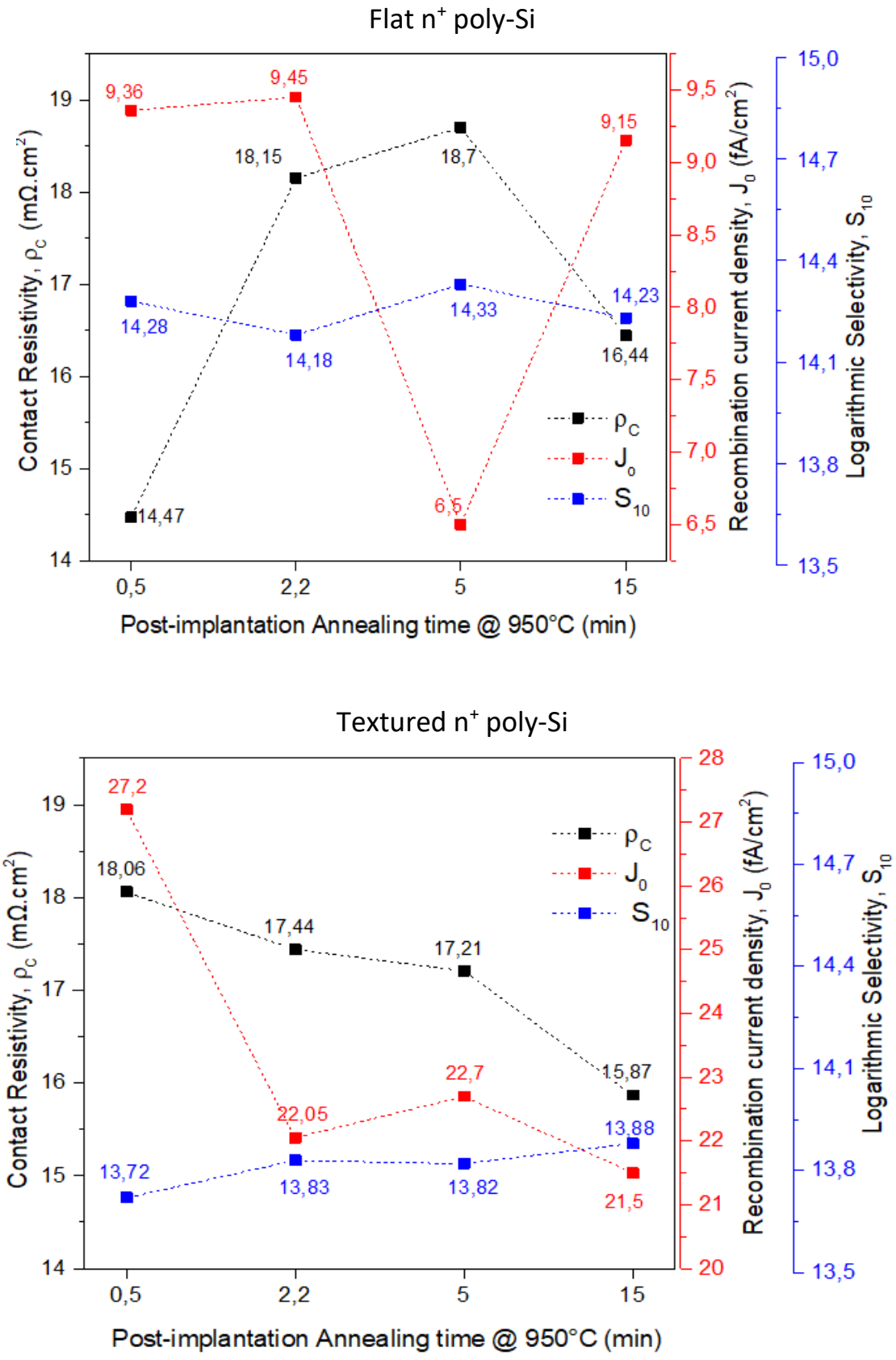


Figure 3.22 The change in contact resistivity (ρ_C), recombination current density (J_0) and logarithmic Selectivity (S_{10}) with change in post-implantation annealing time at 950°C. NOTE: Top- Flat n^+ poly-Si CSPC, Bottom: Textured n^+ poly-Si CSPC. Thermal oxide growth condition - 675°C, 3 min. poly-Si thickness – 250 nm (flat). The data points are connected with dashed lines only for the purpose of guiding the eyes.

3.6 Conclusions

Initially, the experimentation stated with optimising the post-implantation annealing time and the thermal oxide growth conditions. The other conditions such as poly-Si thickness, ion dosage, were fixed constant. In the first stage of optimisation it was found that for the flat and textured n-type poly-Si CSPC the best passivation was achieved with an oxide grown at 600°C, 6 min and annealed at 950°C, 5 min. The p^+ poly-Si flat CSPC had the best passivation with an oxide grown at 675°C, 6 min and annealed at 950°C, both 5 min and 15 min. The p^+ poly-Si textured CSPC had the best passivation with an oxide grown at 675°C, both 6 min and 8 min and annealed at 950°C, 5 min. With these findings the post-implantation annealing temperature was fixed at 950°C. In the second round of optimisation the new thermal budget of 675°C, 3 min is tested with lower annealing time. For both the textured and flat n^+ poly-Si CSPC and flat p^+ poly-Si CSPC an annealing time of 2.2 min was found to give the best passivation and for the textured p^+ sample the best annealing time was even lower at 0.5 min. But an annealing time of 5 min is decided to be used while fabricating the solar cells since at higher annealing time there is better solubility of the dopants in the bulk and because of low contact resistivity as annealing time increases.

Secondly, ECV measurements were done to find the reason for the poor passivation of the textured p^+ poly-Si CSPC and was found that there was no sufficient doping concentration within the poly-Si layer as per simulation studies. So, passivation effects with increased ion dosages were studied and was concluded to use an ion dosage of 1 e16 ion/cm^2, same as that used for textured n^+ poly-Si CSPC.

Thirdly, study on the different thicknesses of poly-Si layer was performed and was concluded that all the four different samples performed the bets at a-Si deposition time of 113 min. Also, only a slight degradation in the passivation quality was found out with the deposition time of 57 min.

Finally, Contact Resistivity measurements were performed, and suggestions were made to improve the accuracy of the contact resistivity measurement. Then based on the measured J_0 and ρ_C values the logarithmic selectivity values, S_{10} were defined and compared with the ones found in literature.

4 Hydrogenation

In this chapter, different hydrogenation approaches to improve the chemical passivation of the CSPC interface and the bulk are discussed. Firstly, the behaviour of hydrogen atoms in the silicon substrate is studied followed by analysing the different parameters that influence the hydrogenation process. Secondly, the different hydrogen containing dielectric layers and their combinations in the form of stacks to serve as a capping layer for hydrogen are studied. Thirdly, the hydrogenation processes done on four different symmetrical samples (flat and textured n^+ and p^+-polySi) are explained schematically. Fourthly, the results from the experiments are presented and inferred to increases the chemical passivation in the successive experimental trails. Triple capping layer technique is introduced in this section for bring the passivation quality of the p^+-polySi layers closer to that of the n^+-polySi layers. Lastly, the chapter is concluded with the optimal results achieved for all the four different types of symmetric samples.

4.1 Hydrogen in Silicon substrate

Hydrogen, the smallest element known plays an important role in increasing the chemical passivation of the silicon surface, interface and the bulk in a solar cell device [38], [20], [58], [5]. Van Wieringen and Warmoltz studied the permeability of hydrogen in the silicon substrate and concluded that the diffusion coefficient (D) increases from 1.7 e4 to 2.17 e4 $cm^2\ s^{-1}$ when the temperature is increased from 1092°C to 1200°C [65]. This makes it suitable for the hydrogen atoms to diffuse through the poly-Si layer and passivate the interface with the bulk, giving an addition boost to the chemical passivation provided by the ultra-thin t-SiO_X layer on the bulk.

Hence, we can define hydrogenation as the process of reducing the defect states on the surface, interfaces and the silicon bulk by making covalent bond with the surface dangling bonds and forming neutral vacancies in the bulk [5], [66]. Figure 4.1 shows the presence of hydrogen atoms in the poly-Si/SiO_x/c-Si layers. Without the use of any capping layer (black line) the concentration of hydrogen in the poly-Si layer varies between 10^{19} – 10^{20} cm^{-3}. At

the SiO_X interface a small spike in the profile shows the excess concentration of hydrogen compared to the vicinity owing to the boost in chemical passivation by t-SiO_X.

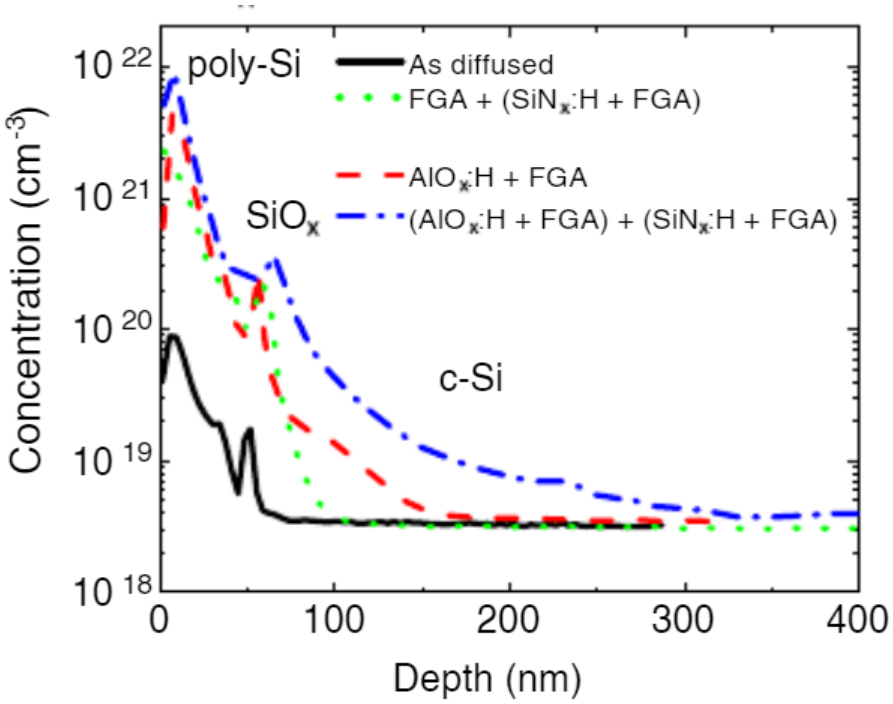


Figure 4.1 Hydrogen concentration profile taken by SIMS (Secondary Ion Mass Spectroscopy) with and without capping layers [67].

The source of hydrogen used by most of the research groups is Forming Gas (FG), which is gas mixture of hydrogen and nitrogen in the ratio 1:10 [20], [58]. The nitrogen gas acts as the carrier gas to transport hydrogen and as a means to dilute hydrogen.

4.2 Factors influencing Hydrogenation

There are many factors that influence the hydrogenation process. To name a few, the temperature and time of the process, H_2 partial pressure, layer(s) used for capping hydrogen, the annealing set-up (meaning if forming gas annealing is carried out in a furnace or in a rapid-thermal processing set-up), hydrogen content and diffusion coefficient of the capping layer, annealing atmosphere, flow rate of FG and so on. Some of these factors and their influence on the passivation quality are discussed in this section.

In this thesis work, the factors such as annealing time, annealing temperature, capping layer structures and annealing set-up are studied and optimised for both the n^+ and p^+ poly-Si

CSPCs. Factors such as capping layer deposition pressure are reaction gases ratio are kept constant throughout the study.

4.2.1 Annealing Time and Temperature

The annealing time and temperature of the hydrogenation process plays an important role in deciding the passivation quality. In our case, high temperature processes can be detrimental to the thin t-SiO_X layer. Hence, a temperature lower to that of the t-SiO_X growth temperature is preferred while hydrogenation. From Figure 4.2 it can be seen that, there is no significant rise in passivation effects as the temperature increases. The drop in the iV_{OC} values after an annealing temperature of 500°C is due to the effusion of hydrogen from the sample. Also, when annealed at 700°C, for just 5 min there is a tremendous drop in iV_{OC} for the n^+ poly-Si samples. This shows that the temperature has the major influence on the passivation rather than the time of annealing when it comes to thermal stability of the layers within the device.

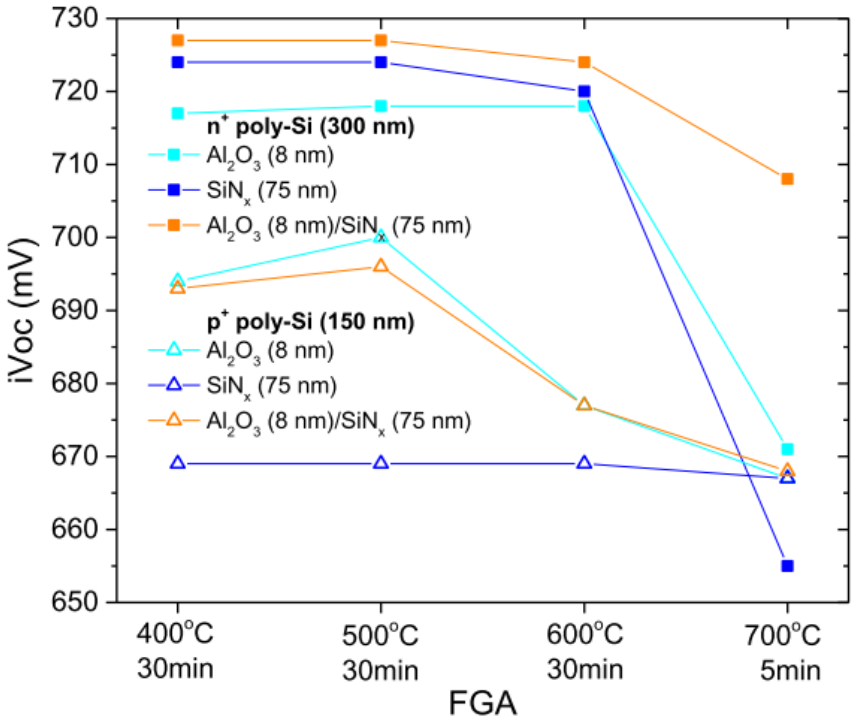


Figure 4.2 Passivation of the poly-Si CSPC with respect to increase in annealing time and temperature [21].

Also, it can be seen that there is a significant difference in the performance of the n^+ and p^+ poly-Si samples under same hydrogenation condition. The n^+ poly-Si SCPC outperforms the p^+ poly-Si CSPC, which is documented by various research groups across the world. Hence, a

novel method for hydrogenation are widely researched for increasing the performance of the p^+ poly-Si layers. This includes trying different capping layers and annealing atmospheres which are explained in the consecutive sections.

4.2.2 Annealing Atmosphere

Hydrogenation in most research works are done in the Forming gas atmosphere. Some research groups have also tested hydrogenation in other gaseous environments such as Nitrogen (N_2) and Deuterium (D_2) [68]. Deuterium is an isotope of hydrogen which has one neutron extra along with the proton in its nucleus. Johnson et al, were the pioneers who studied the deuterium content in c-Si as well as poly-Si when annealed at temperatures at about 350°C [69]. They concluded that in the monoatomic deuterium (D) showed better diffusion in the silicon bulk compared to that of molecular deuterium (D_2). The deuterium concentration of about 10^{21} cm^{-3} was observed in the top 200 nm of the poly-Si samples when annealed at 350°C. This value is around one order of magnitude less than that of the hydrogen concentration as shown in Figure 4.1. When nitrogen is used for annealing a capping layer with high hydrogen content, such as Al_2O_3 is used. During the annealing process the hydrogen in the capping layer gets diffused into the interfaces and provides chemical passivation. The nitrogen atmosphere prevents the effusion of hydrogen from the capping layer through its partial pressure imparted on the sample. Figure 4.3 shows the annealing treatment in nitrogen and FG atmospheres with Al_2O_3 capping layer on a p^+ poly-Si CSPC. It can be seen that annealing in N_2 atmosphere gives almost equal passivation effects as that of FGA. In this thesis work annealing for passivation purposes are carried out in a forming gas atmosphere.

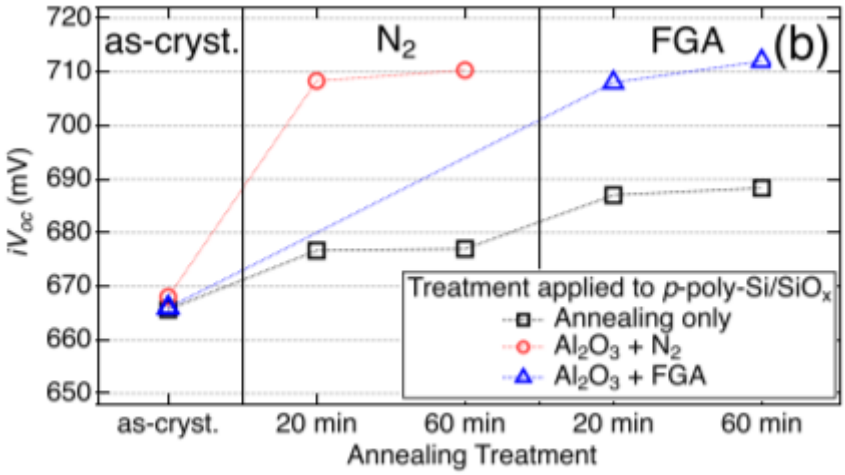


Figure 4.3 Passivation of p^+ poly-Si CSPC with respect to annealing time in nitrogen and forming gas atmosphere with aluminium oxide capping layers [68].

4.2.3 Annealing experimental set-up

The annealing set-up also influences the diffusion rate of hydrogen in the silicon substrate. Two different annealing set-ups are used in this thesis work. Firstly, annealing in the furnace is carried out in a Tempress furnace. In such a type of furnace the annealing temperature is carried out in constant temperature throughout the process. This is much common method used by the various research groups. In this process the thermal flux experienced by the sample remains constant during annealing. This might lead to constant diffusion of the hydrogen atoms into the sample until saturation. Secondly, Rapid Thermal Processing (RTP) can also be used in hydrogenation process in a forming gas atmosphere. The only difference is the temperature profile throughout the annealing process. In RTP, the temperature of the chamber rises from the room temperature to the set value (say 400°C) in a matter of few seconds. This imparts sudden changes in the thermal flux experienced by the sample placed in the annealing chamber. This type of annealing is used in other areas of photovoltaics such as in post-annealing after screen-printing of the metals [70], in relieving the stress imparted by the implantation process in pseudomorphic $Ge_{0.12}Si_{0.88}$ layers on Si substrate [71] and annealing poly-Si layers on glass substrate [72]. RTP process also gives high control over the thermal budget compared to that od furnace annealing [72]. Hence, in this thesis work it is decided to use RTP method of annealing in FG atmosphere to check if it has significant impact on the chemical passivation of the CSPCs. Figure 4.4 shows the temperature profile of process

chamber when annealing process carried out in a furnace and in a rapid thermal process set-up.

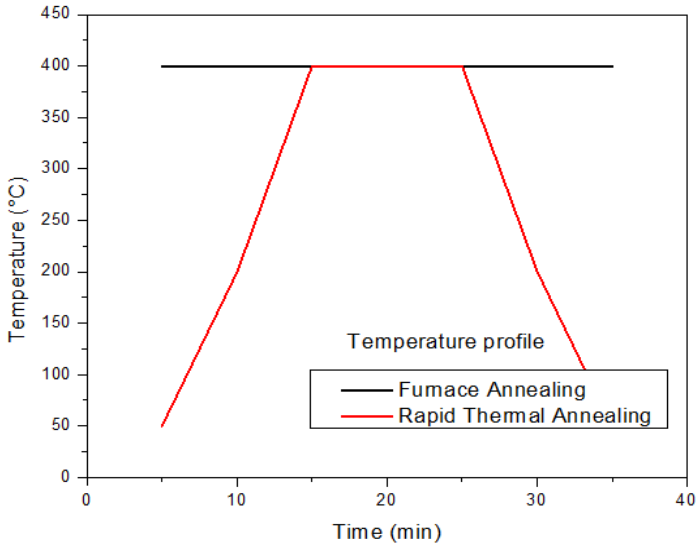


Figure 4.4 Temperature profile in furnace and rapid thermal annealing.

4.2.4 Capping Layers

Capping layers are hydrogen rich layers which helps in passivating the defect states on annealing. These capping layers are usually dielectric materials such Silicon Nitride (SiN_X) or Aluminium Oxide (AlO_X) [21], [68], [73]. These layers are either used individually or stacked upon one another to serve as a hydrogen capping layer [64], [21]. Being dielectric materials, these layers have fixed charge density (Q_f) in them. The materials by its physical and chemical characteristics can have either positive or negative charges associated with them. For instance, fixed charge densities of +2 e12 cm^{-2} and -4 e12 cm^{-2} for Plasma Enhanced Chemical Vapour Deposition (PECVD) of SiN_X and Atomic Layer Deposition (ALD) of AlO_X respectively where noted by J.Schmidt et al [74]. These charges help in providing field-effect passivation to the underlying layer. But in our case, these capping layers only serve as a hydrogen reservoir during hydrogenation and later removed for the ease of Transparent Conducting Oxide (TCO) deposition.

These capping layers can have different hydrogen storage capacities, hydrogen diffusion coefficient and effusion barrier during annealing [21]. SiN_X which is also commonly used as an Anti-Reflection Coating (ARC) in the photovoltaic industry have a hydrogen content of 10 – 15 at. % (Atomic percentage), when deposited by PECVD [75] at temperatures below 400°C. On the other hand, AlO_X have a less hydrogen content of 3.6 at. %, when deposited by ALD at

200°C. The diffusion coefficient of hydrogen in silicon nitride and aluminium oxide is around 10^{-19} cm^2/s [21], [75]. AlO_X have better effusion barrier compared to that of SiN_X [21]. The reason for such behaviour is not clearly understood currently. Hence a combination of a hydrogen rich layer and a layer with higher effusion barrier, an ample amount of hydrogen can be directed to the poly-Si layer and the SiO_x/c-Si interface. This in turn will lead to better passivation effects. So, in this thesis a double (AlO_X/SiN_X) and triple ($AlO_X/SiN_X/AlO_X$) stack of capping layers are studies. From Figure 4.2 it also can be inferred that the passivation quality of the poly-Si CSPC attained through a capping layer depends on the doping type. For instance, a double capping layer (AlO_X/SiN_X) works good for a 300 nm thick n^+ poly-Si sample and a single AlO_X layer works the best for a 150 nm thick p^+ poly-Si sample.

The way these capping layers are deposited on the symmetric samples and the annealing processes performed on them are explained in the following section.

4.3 Sample Preparation

The symmetric samples which were prepared in section 3.4 were subjected to hydrogen treatment. In this thesis four different hydrogenation steps are suggested. Figure 4.5 shows the flow chat of the different hydrogenation processes. The first three hydrogenation steps are tested on all the symmetric samples- textured and flat n^+ and p^+ poly-Si. The last hydrogenation step AlOx/SiNx/AlOx-RTP was tested only on the p^+ poly-Si samples. Also, with the same capping layer structure instead of the last RTP at 650°C for 10 min, annealing in furnace and low temperature RTPs were also performed in this thesis.

Forming Gas Annealing (FGA) is carried out in a tube furnace at 400°C for 1 hr in forming gas atmosphere. The forming gas atmosphere is created by maintaining the flow rated of Nitrogen and Hydrogen at 3 and 0.3 SLM respectively throughout the annealing process.

Rapid Thermal Process (RTP) annealing is carried out in a Solaris 100 RTP system. The forming gas is supplied at a rate of 8 SLM and carried out in a temperature range between 400°C - 700°C. After the ALD deposition of the first layer of AlO_X in a triple capping layer RTP is performed in Nitrogen atmosphere at 600°C for 10 min. The flow rate of N_2 is kept at 5 SLM.

Silicon Nitride deposition is done by PECVD in OXFORD PlasmaLab80Plus. Silane (SiH_4) reacts with ammonia (NH_3) to for silicon nitride. The hydrogen content of these layers varies

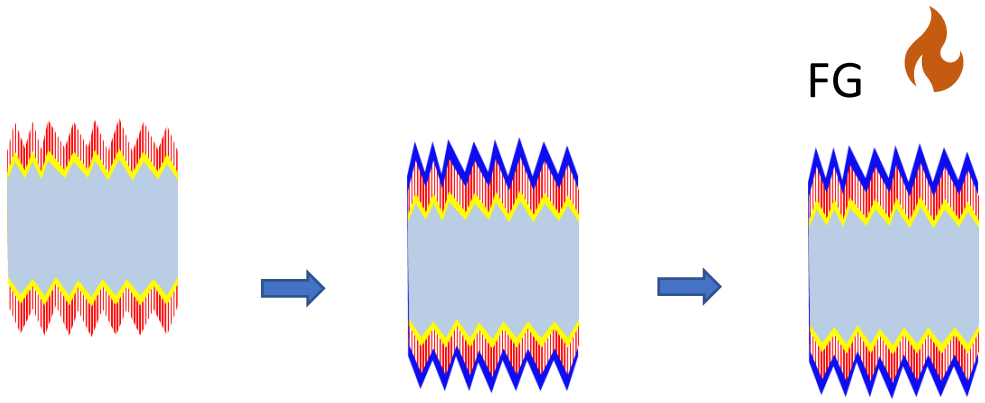
depending upon the deposition temperature. The full stoichiometric form of silicon nitrate has a very low content of hydrogen in it and it varies as a function of processing temperature [76]. Hence, different deposition temperature ranging from 200°C to 400°C is studied in this thesis. The flow rate of silane and ammonia is maintained at 20 sccm.

Aluminium Oxide thin film deposition can be done in many ways. To mention a couple, Chemical Vapour Deposition (CVD) and Atomic Layer Deposition (ALD). Literature shows that AlO_X deposited by ALD is much uniform and denser compared to the other deposition techniques [77]. Oili et al, have observed a decrease in the hydrogen content of the AlO_X layer as the deposition temperature increases [78]. When grown at 300°C the hydrogen content in AlO_X is 1 at. %. A deposition temperature of 110°C yields a hydrogen content of 11.3 at. % [78]. So, AlO_X deposition is carried out at 105°C with Trimethylaluminum [$Al(CH_3)_3$] and H_2O as the metal precursor and co-reactant in Oxford Instruments OpAL^{TM} reactor.

Figure 4.5 Flow chart for the hydrogenation of symmetric sample.

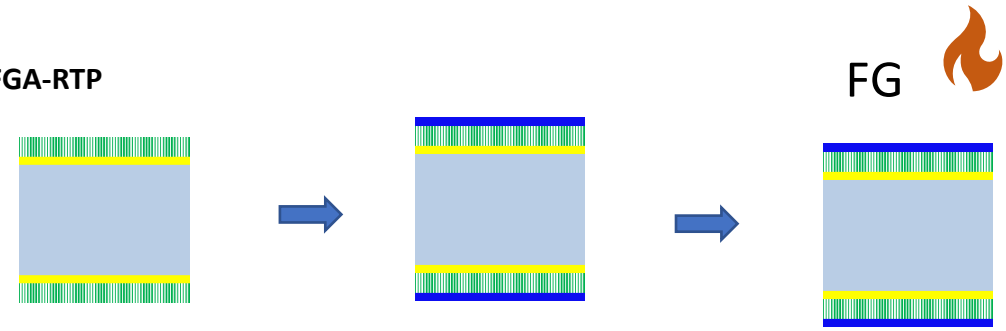
Note: The schematic extends to the next page as well.

SiNx-FGA

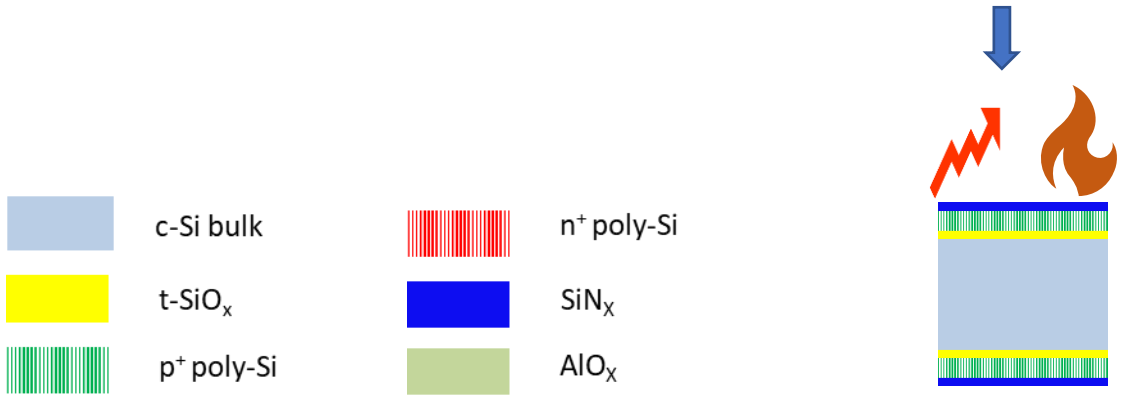


1. n^+ poly-Si textured 2. PECVD - SiN_X 3. FGA

SiNx-FGA-RTP



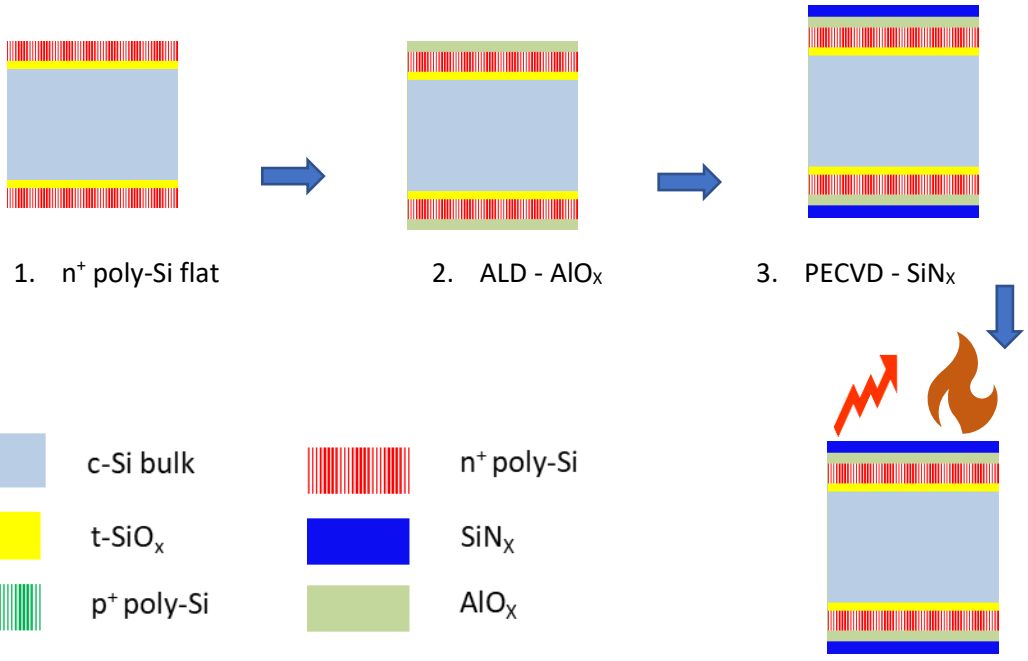
1. p^+ poly-Si flat 2. PECVD - SiN_X 3. FGA



4. RTP in FG @ 500°C,10 min

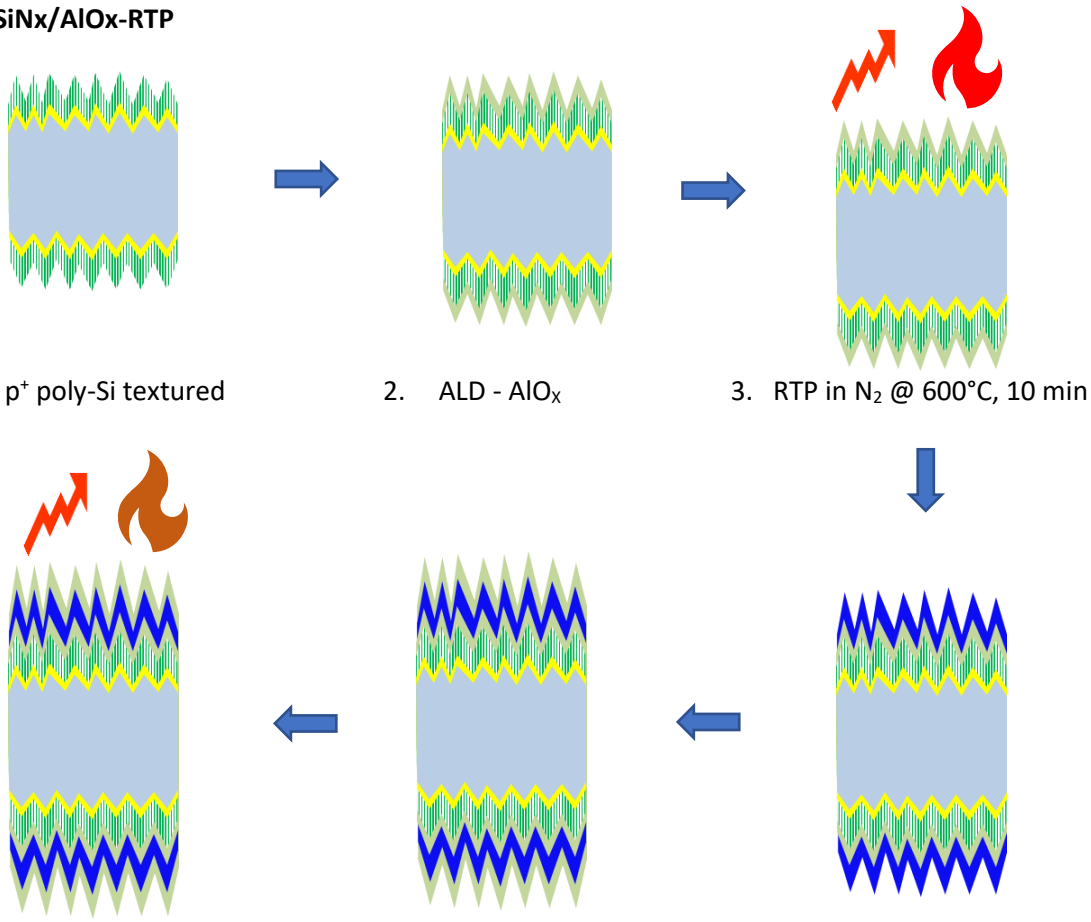
Note: The capping layers are removed after hydrogenation by a dip in BHF (Buffer Hydrofluoric acid)

AlOx/SiNx-RTP



1. n^+ poly-Si flat
2. ALD - AlO_X
3. PECVD - SiN_X
4. RTP in FG @ 500°C, 3 min

AlOx/SiNx/AlOx-RTP



1. p^+ poly-Si textured
2. ALD - AlO_X
3. RTP in N_2 @ 600°C, 10 min
4. PECVD - SiN_X
5. ALD - AlO_X
6. RTP in FG @ 650°C, 10 min

SiNx-FGA – The symmetric samples after FGA as represented as step 8 in Figure 3.9 is subjected to SiN_X deposition on both the sides of the sample by PECVD. This is followed by forming gas annealing in a furnace. At the end of all the hydrogenation processes the capping layers are removed by etching in BOE 7:1 (HF : NH_4F = 12.5 : 87.5% [79]). A few mV drop in iV_{OC} is seen after the removal of the capping layer.

SiNx-FGA-RTP – This is same as that of the above metioned process. The deposition time of SiN_X throughout the thesis was set at 8 min which inturn gives a SiN_X thin layer of 120 nm on a flat surface. The thickness on the textured surface with this same conditions is about 80 nm due to the increaes surface area. The one addition step done after FGA is furthur annealing in FG by RTP at 500°C for 10 min. This is done to check if there is a further increase in passivation by an addition high temperature annealing step.

AlOx/SiNx-RTP – On symmetric samples are very thin layer of AlO_X is grown by ALD at 105°C on both the sides. The deposition thickness is controlled by repeating cycles. The deposition cycle is fixed at 100. This gives a nano layer of AlO_X of thickness 6.5 nm (on flat). This is followed by SiN_X deposition on both sides. Finally, the sample is subjected to RTP annealing at 500°C for 3 min.

AlOx/SiNx/AlOx-RTP – Firstly, thin layer of AlO_X is deposited on both the sides of the sample. This is followed by RTP annealing in N_2 atmosphere at 600°C for 10 min. This is carried out to check if annealing in N_2 atmosphere helps in the diffusion of hydrogen form the AlO_X capping layer to the poly-Si/SiO_X/c-Si interface. Then a second capping layer – SiN_X is deposited on both the sides, which follows a second AlO_X layer deposition. Now, a stack consisting of three dielectric layers are on the symmetric samples. This is follows by a final annealing step. The final annealing step of RTP in FG at 650°C for 10 min is shown in Figure 4.5. RTP annealing at different temperature and furnace annealing were also tested. This hydrogenation process was studied only on p^+ poly-Si CSPC samples as their passivation qualities were not as good as n^+ poly-Si CSPCs.

The results from the above-mentioned hydrogenation processes are inferred in the following section.

4.4 Experimental results and inference

In this section the experimental results are discussed. It consists of four sub sections starting with passivation by single capping layer followed by double and triple capping layers for p^+ poly-Si CSPCs. Within the triple capping layer sub section, the effect of ion dosage used while implantation as discussed earlier in section 3.5.3 is also studied in depth along the course of hydrogenation. Lastly, the consolidated results of different hydrogenation steps are presented for the ease of comparison between the textured and flat p^+ and n^+ poly-Si CSPCs.

The potential in enhancing the chemical passivation of the different hydrogenation processes are analysed by keeping the poly-Si thicknesses at 250 and 200 nm for flat and textured samples respectively. The thermal oxide growth condition used is 675°C, 3 min. Post-implantation annealing is done at 950°C for 5 min.

4.4.1 Silicon Nitride deposition temperature

Before studying the different suggested hydrogenation processes, it is decided to analyse the impact of deposition temperature of SiN_X on the passivation quality of the sample. As discussed previously in section 4.2.4, the deposition temperature greatly has an influence on the hydrogen content of the capping layer. Figure 4.6 shows the changes in the iV_{OC} of the symmetric samples as the SiN_X deposition temperature increases. To check this effect the hydrogenation process used is SiN_X-FGA. Three different annealing temperatures 200, 300 and 400°C were studied for a deposition time of 8 min. It is obvious from the plot that there is an increasing trend in the passivation quality as the deposition temperature increases. Further increased temperatures were not able to be tested because of the operational limit of the equipment.

For the flat and textured n^+ poly-Si CSPC a 10 mV rise in iV_{OC} is seen when SiN_X is deposited at 400°C compared to that of deposition at 200°C. Similarly, for the flat p^+ poly-Si CSPC a 14 mV rise is seen in iV_{OC}. For the textured p^+ poly-Si CSPC a tremendous rise of 25 mV is observed in the passivation quality when the capping layer is deposited at the maximum possible temperature. This significant rise in the iV_{OC} values, also shows that there is still room left for the increase in passivation quality. So, it is decided to carry out all the SiN_X layer deposition at 400°C throughout the thesis work. On the other hand, AlO_x deposition is fixed at 105°C due to high hydrogen content at low temperatures.

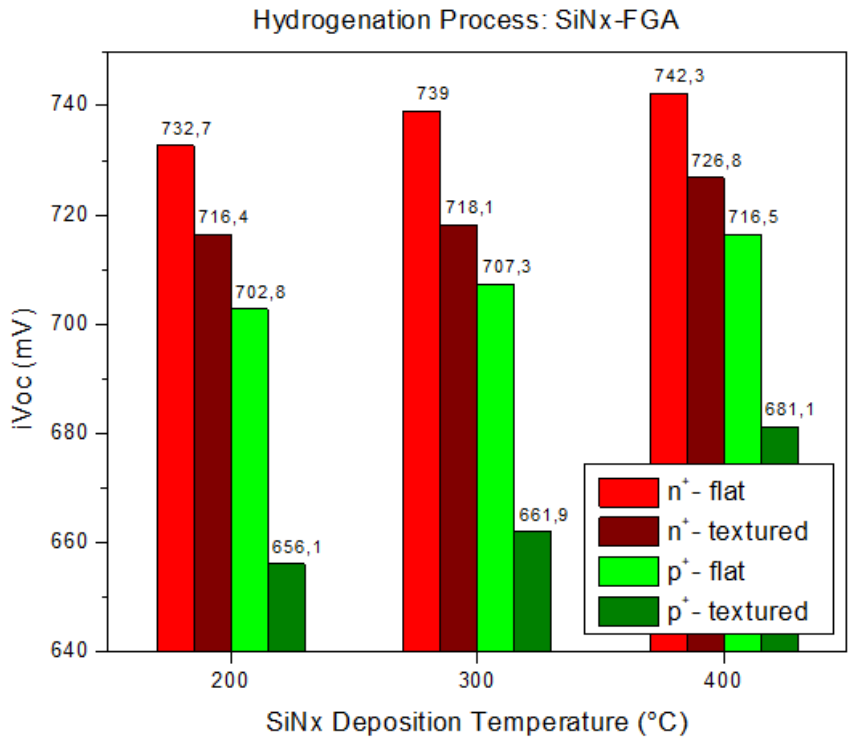


Figure 4.6 Passivation quality of SiN_X capping layer after hydrogenation as a function of SiN_X deposition temperature.

This trend is in accordance with the results concluded by Pierre et al. Hydrogen content ranging between 21 – 25 at. % if found in the PECVD SiN_X of thickness 200 nm at 350°C [80]. It is expected that 120 nm thick SiN_X on the flat surface has to have a hydrogen content between 10 – 20 at. %. Also, high temperature deposition such as at 800°C will also lead to undesirable effect on the hydrogen content of the SiN_X layers. At such elevated temperature hydrogen effusion from the SiN_X layer is enhanced leading to voids, indicating the absence of hydrogen within the layer [81].

Below the optimal SiN_X deposition temperatures, the hydrogen is prevented from effusing from the layers and contained within it. On further annealing steps the hydrogen from the layer diffuses through the poly-Si layer and the SiO_X/c-Si interface. Also, for a single SiN_X used as capping layer the consecutive FGA is also carried out in the same temperature (400°C) as a precaution for hydrogen effusion dominating hydrogen diffusion.

4.4.2 Single Capping layer with single annealing step (SiN_X-FGA)

Initially, hydrogenation was carried out with a single capping layer of SiN_X followed by FGA. The trend in the passivation quality along the hydrogenation process for the symmetric samples are as shown in Figure 4.7.

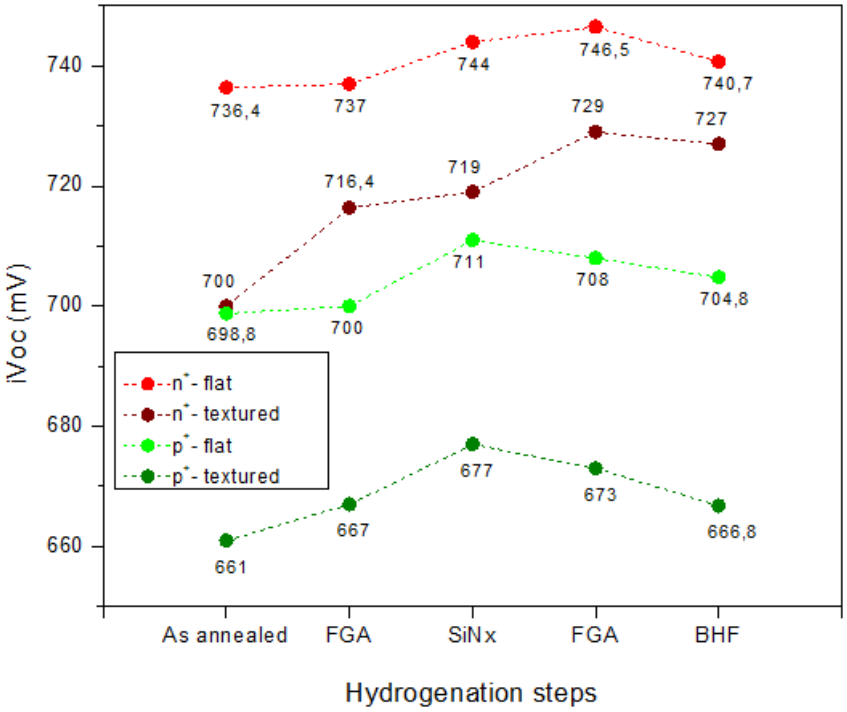


Figure 4.7 Passivation quality of the symmetric samples along the hydrogenation steps of SiN_X-FGA. NOTE: The data points are connected with dotted line just to guide the eyes.

Flat n^+ CSPC – The maximum passivation is achieved at the last FGA process with an iV_{OC} of 746.5 mV. Thus, after post-implantation annealing , the hydrogenation process has increased the chemical passivation in the sample by 10 mV. Also, the sample experiences a 6 mV drop when the capping layer is removed.

Textured n^+ CSPC – The trend in passivation is very much similar to that of the flat sample. The only noticeable change is that the enhancement in chemical passivation is way higher than that of the flat n^+ CSPC samples. A noticeable 29 mV rise in the chemical passivation is achieved in this process till the last FGA. A sizable increase in the chemical passivation is seen compared to the flat n^+ CSPC because of high surface defects induced during the texturing process. After the capping layer is removed a difference of 13 mV is observed between the flat and the textured n^+ CSPC samples.

Flat p^+ CSPC – The behaviour of the flat p^+ poly-Si CSPC samples is quite different as compared to the n^+ poly-Si. The FGA after the capping layer deposition has no positive influence on the hydrogenation process. A slight drop in iV_{OC} is observed during FGA after capping layer deposition. This shows that the 120 nm thick SiN_X capping layer does not help in hydrogen diffusion through the sample. In addition to that the capping layer removal also leads to a 3 mV drop in iV_{OC}. The maximum passivation is attained during the SiN_X deposition.

Textured p^+ CSPC – Similar trend as that of the flat p^+ poly-Si CSPC is observed. The chemical passivation achieved during the capping layer deposition is completely lost during the consecutive steps. Implies V_{OC} of 667 mV is observed at the start and the end of the hydrogenation process. Besides, the p^+ poly-Si CSPC not passivated to the best in this hydrogenation process, a large difference of 40 mV is noticed between the flat and the textured wafers. This shows that there is a large room for improvement in the passivation of the textured p^+ poly-Si CSPC.

In all the symmetric samples, an increase in passivation quality right after the capping layer deposition is notices. This increase is trivial in the n^+ poly-Si samples compared to that of the p^+ poly-Si samples. This behaviour is due to the fact that, the hydrogen atoms that are within the poly-Si from the FGA after post-implantation annealing starts to diffuse through the poly-Si layer as a result of the thermal flux imparted on the sample during the PECVD deposition of SiN_X at 400°C

Since for the p^+ poly-Si CSPCs, the last FGA step of the hydrogenation process does not show a rise in passivation, an addition hydrogenation step is decided to be tested. A rapid thermal process produces a sudden thermal shock in the sample. To check if this effect will have a positive effect on the passivation quality an addition annealing after FGA in RTP set-up is performed at 500°C for 10 min in forming gas atmosphere. The effect of such hydrogenation step is examined in the following section.

4.4.3 Single Capping layer with double annealing steps (SiN_x-FGA-RTP)

Since the FGA after capping layer deposition led to a decrease in passivation quality a higher temperature RTP following the FGA is tested. The RTP process is carried out at 500°C for 10 min. The results are as shown in the Figure 4.8.

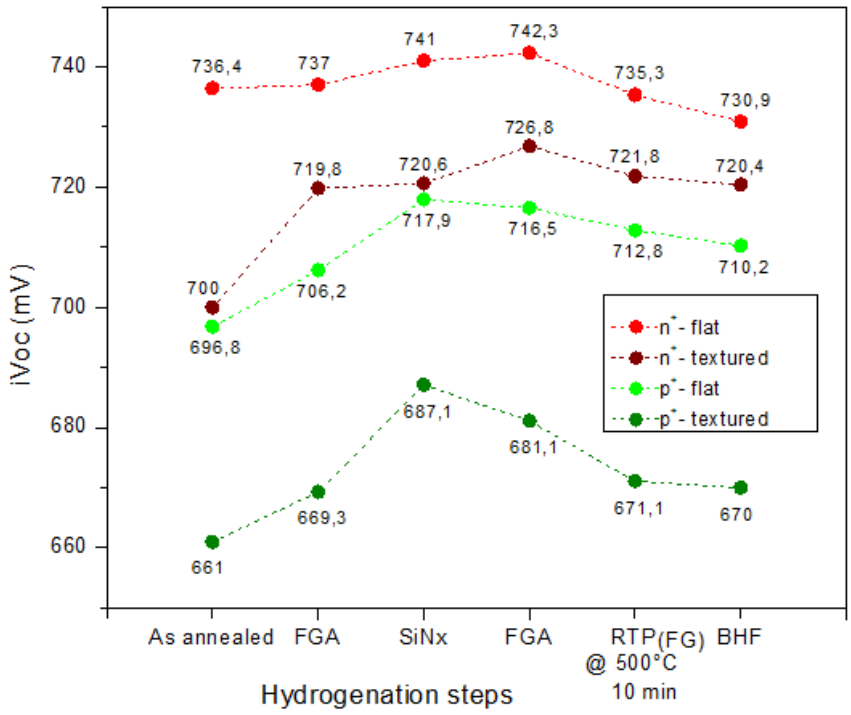


Figure 4.8 Passivation quality of the symmetric samples along the hydrogenation steps of SiN_x-FGA-RTP. NOTE: The data points are connected with dotted line just to guide the eyes.

Flat n^+ CSPC – This hydrogenation step led to the decrease in passivation compared to the former. A 7 mV drop in passivation is seen after the second annealing step done through RTP. After the capping layer removal iV_{OC} of 731 mV is observed, which is 10 mV less as compared to the hydrogenation by SiNx-FGA. The trend till the last FGA is analogous to the previous hydrogenation steps owing to its concordance.

Textured n^+ CSPC – It is obvious that the sample behaves in the same way as the flat sample. The difference in passivation quality compared to the previous hydrogenation process is about 7 mV. The interesting thing observed in this sample is during the capping layer removal step. The loss in passivation during BHF is negligible compared to the RTP step. So, for the n^+ poly-Si samples an addition RTP step after FGA did not show a positive effect on the passivation quality.

Flat p^+ CSPC – Similar trend is seen as that of the n^+ poly-Si samples. But the final passivation is relatively higher than the previous hydrogenation step. An iV_{OC} of 710.2 mV is achieved at the end of the hydrogenation step. But still the process suffers a decrease in passivation after the capping layer deposition. Also, it can be noted that on comparing the step till SiN_X deposition with the previous hydrogenation process there is a 6 mV difference. This shows the inconsistency in the passivation quality on different experimental runs. This can arise due to the non-similarities in the CSPC fabrication under same condition or due to the difference in the hydrogenation atmosphere between different runs under same conditions.

Textured p^+ CSPC – iV_{OC} of 670 mV is achieved in this process. A negligible chance in the iV_{OC} drop is observed on BHF step. During the capping layer deposition set iV_{OC} of 687.1 mV is observed, the highest so far. The passivation during the initial steps also vary compared to the previous hydrogenation process.

The three main conclusions that can be drawn from the above two hydrogenation processes are as follows. Firstly, the optimal hydrogenation process for the n^+ poly-Si CSPC is SiN_X-FGA. Secondly, addition annealing step only lead to the decrease in passivation for both the n^+ and p^+ poly-Si CSPCs. Lastly, the p^+ poly-Si samples don't give similar results during different runs under same operational conditions.

Various research groups are working on the optimisation of the capping layer structure with AlO_x and SiN_X stacks and have claimed to be working the best for p^+ poly-Si CSPCs [21], [68]. So, the following two hydrogenation processes are done with the different combination of these two capping layers and different annealing conditions. The hydrogenation of a double capping layer followed by a single RTP is discussed in the next section.

4.4.4 Double Capping layers with single annealing step (AlO_X/SiN_x-RTP)

The effect of a double capping layer – a relatively thick SiN_x layer on a thin AlO_X layer on hydrogenation is studied in this section. Figure 4.9 shows the passivation trend along the hydrogenation steps with a double capping layer. Also, the comparatively shorter RTP annealing time of 3 min is used to check if annealing time plays an important role in the passivation loss.

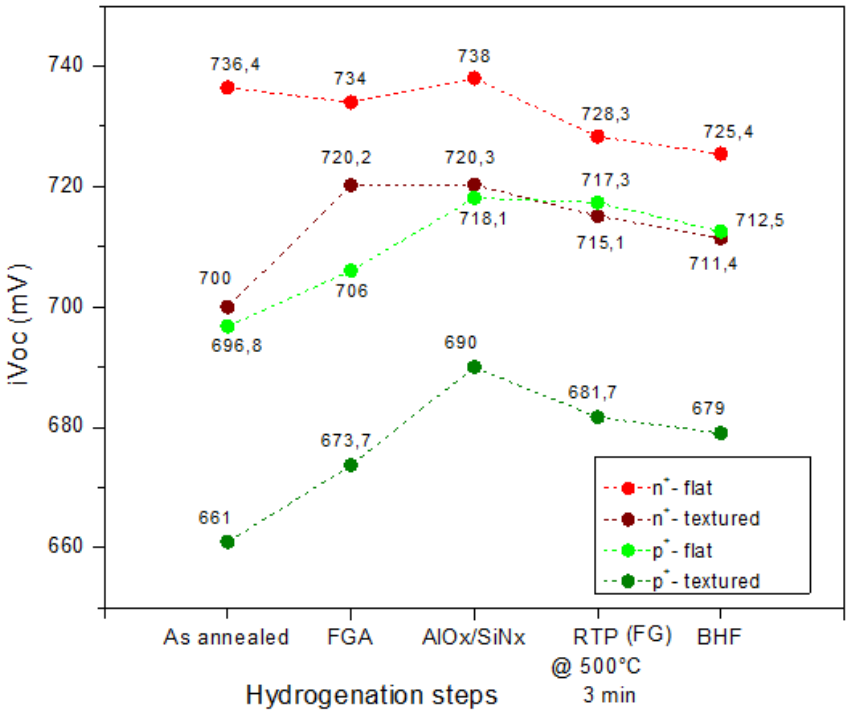


Figure 4.9 Passivation quality of the symmetric samples along the hydrogenation steps of AlO_X/SiN_X-RTP. NOTE: The data points are connected with dotted line just to guide the eyes.

Flat n^+ CSPC – The double capping layer leads to a drop in the iV_{OC} by 6 mV after its deposition compared to the SiN_X single capping layer. At the end of hydrogenation step, iV_{OC} of 725.4 mV is observed, which a 15 mV less than the previous maximum obtained. Also, the low duration RTP at 500°C for 3 min still leads to a loss in passivation after the AlO_X/SiN_X deposition.

Textured n^+ CSPC – Similar passivation result is seen as that of the flat sample. Similar passivation is observed on the deposition of the double capping layer as that of the single SiN_X layer. It can be observed from all the above plots related to hydrogenation the first FGA after post-implantation annealing gives a rise in iV_{OC} of about 20 mV. The short temperature RTP makes the hydrogen from the capping layers to effuse easily out of the sample.

Flat p^+ CSPC – Only a very slight change of 2 mV is observed in iV_{OC} compared to that of the previous hydrogenation step. Also, the passivation effect is the same after the capping layer deposition either if it's a single SiN_X layer or AlO_X/SiN_x stack. The iV_{OC} after the capping layer removal is 712.5 mV.

Textured p^+ CSPC – The double capping layer has resulted in an iV_{OC} of 690 mV after deposition. This increase is seen only as a result of a better FGA after post-implantation annealing. In the end, iV_{OC} of 679 mV is achieved considerably higher than the previous hydrogenation processes.

As mentioned in section 4.2.4 AlO_X is supposed to have a better resilience to hydrogen effusion compared to that of SiN_X. But this effect is only seen in the p^+ poly-Si CSPC samples. Hydrogen from the SiN_X and AlO_X layer initially has to diffuse towards the poly-Si layer for surface and interface passivation during the RTP process. Only then the AlO_X layer will hinder the effusion of the diffused hydrogen. The reason for iV_{OC} drop on RTP might be due to the fact that hydrogen from the rich SiN_X layer might have effused out of the sample during the process even though it is carried out only for 3 min.

To check if the AlO_X layer has better effusion barrier the following idea is proposed. If the reason mentioned in the above paragraph is true and if AlO_X has high rigidity to hydrogen effusion, a layer of $AlO_X/SiN_X/AlO_X$ should show better passivation effects on the samples. So, this triple capping layer of SiN_X sandwiched between AlO_X is tested in the following section. Also, at this point it is decided to test only the p^+ poly-Si CSPC symmetric samples. As a simple single layer SiN_X followed by FGA already gave us the desired high passivation qualities with 741 and 727 mV for the flat and textured n^+ poly-Si CSPCs respectively.

Also, to check if the low performance of the textured p^+ poly-Si sample is due to poor field-effect passivation three different ion dosage concentrations of 7.5 e15, 1 e16 and 1.5 e16 ions/cm^2 are studied. This optimisation involved three annealing steps and the consolidate of this optimisation is also presented in Figure 3.18.

4.4.5 Triple Capping layers with triple annealing steps (AlO_X/ SiN_x/AlO_X-FGARTPs)

In this section the triple capping layer stack with three different annealing steps are studied. The first annealing step in always carried out in N_2 atmosphere at a temperature of 600°C for 10 mins after the deposition of the first layer of AlO_X. This is carried out to prevent the hydrogen form the first AlO_X layer effusing out of the sample during the SiN_X deposition which leads to blistering of layers. After the deposition of second layer of AlO_X two annealing steps were done and they are discussed in the following sub-sections with the last two annealing steps as sub-headings.

4.4.5.1 p^+ textured CSPC

Figure 4.10 Top shows the passivation profile of throughout the hydrogenation process with triple capping layers and triple annealing steps for the textured p^+ poly-Si CSPCs. Also, the plots have the results of different ion dosages used at the time of ion-implantation. The main inference from the plot is in third and fourth step of the process. The N_2 – RTP has indeed helps in preserving the passivation during the SiN_X layer deposition. Between these steps only a feeble drop in the iV_{OC} is noticed. A significant rise in iV_{OC} is seen only in the last three steps of the hydrogenation process. So, the snipped version of the process is as shown in Figure 4.10 Bottom. Initially, it is hard to compare the effect of doping concentration on the field-effect passivation because of the differences in chemical passivation between the samples. After the annealing processes are carried out the effect of ion-dosage on field-effect passivation is clearly seen.

FGA-RTP@ 600°C, 20 min – After the deposition of the first two capping layers the passivation obtained is comparable with the previous hydrogenation processes. After the FGA annealing step an increasing trend in the iV_{OC} is seen for the very first time. A maximum increase of 12 mV is seen for the 1.5 e16 ions/cm^2 sample is seen. Thus, we can confirm that the trip capping layer is preventing the hydrogen effusion from the sample to a great extent during the annealing steps. The second RTP at a higher temperature of 600°C for 20 min is carried out to check if there is an improvement in passivation. iV_{OC} greater than 700 mV were achieved during these steps. The sample with the ion dosage of 1 e16 ion/cm^2 seems to out-perform other two doping concentration. The sample with 1.5 e16 ion/cm^2 shows a lag in the passivation quality and this might be due to the dominance of Auger recombination.

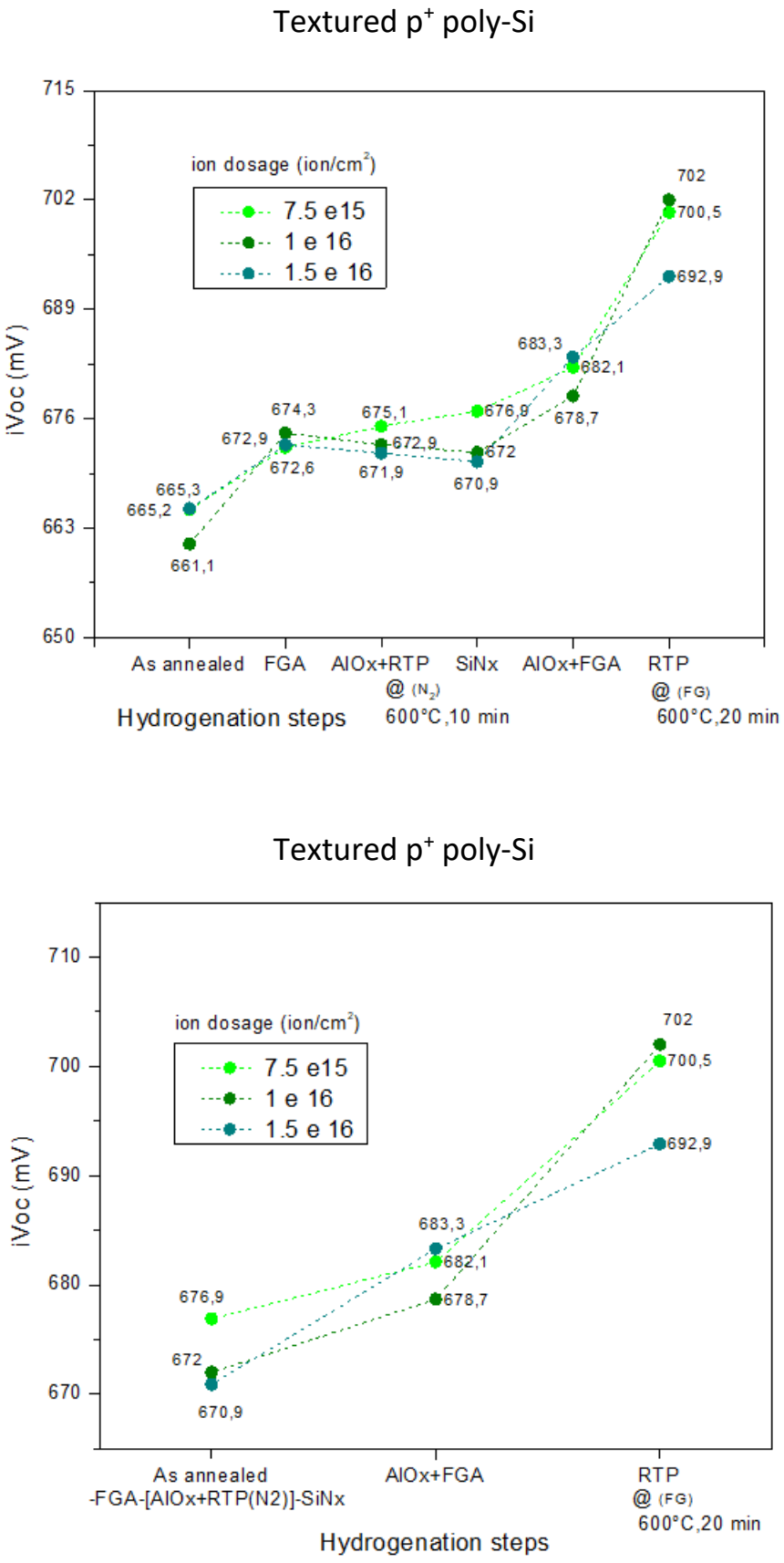


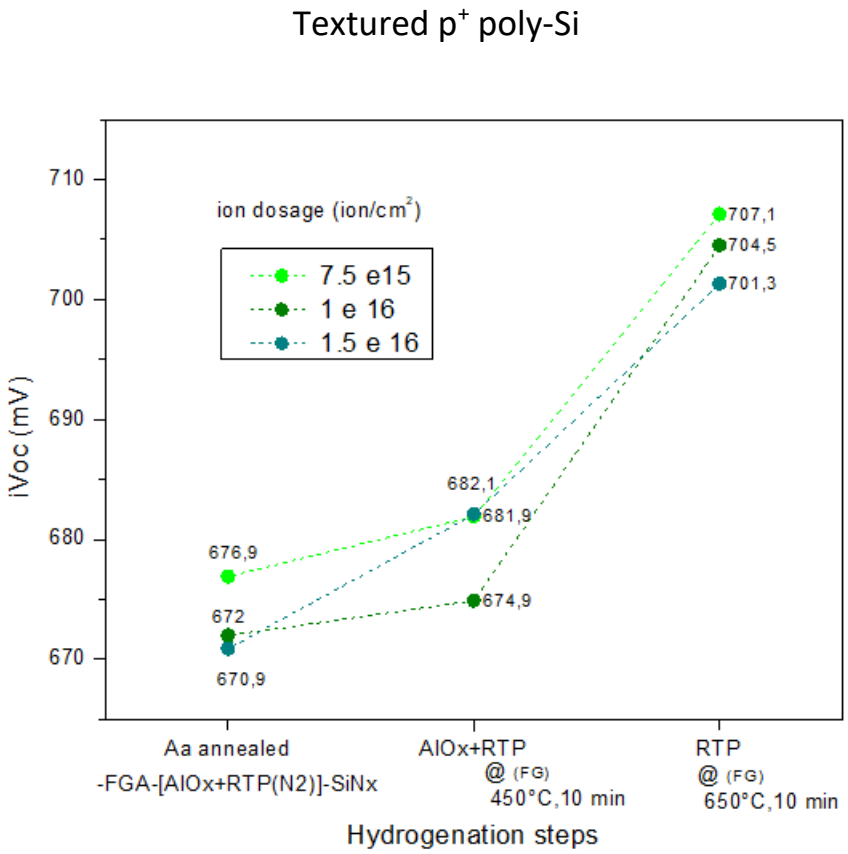
Figure 4.10 Passivation for textured p^+ poly-Si CSPC along the hydrogenation steps of $AlO_X/SiN_X/AlO_X$-FGA-RTP @ 600°C, 20min. NOTE: Top – iV_{OC} values throughout the hydrogenation step, Bottom – iV_{OC} for the last three important steps to see the trend clearly.

The following two paragraphs are inferences from the Figure 4.11. Top – for consecutive RTPs at 450°C and 650°C for 10 min. Bottom – for RTP at 500°C, 10 min followed by three rounds of short interval RTPs at 700°C for 2 min

RTP@ 450°C, 10 min -RTP@ 650°C, 10 min – To check if an RTP step instead of FGA gives a better passivation effect, annealing in FG atmosphere by RTP was carried out at 450°C for 10 min. The passivation at this point is same as that of FGA. An RTP at even higher temperature of 650°C is carried out for 10 min and an increase in iV_{OC} of 25 mV is seen irrespective of the doping concentrations. The sample with the ion dosage of 7.5 e15 ion/cm^2 show the highest passivation of 707,1 mV. But we can still conclude that the sample with the ion dosage of 1 e16 with iV_{OC} of 704,5 mV performs better than the former because the rise in iV_{OC} from the previous step is around 30 mV and the former has a rise of 25 mV. This difference shows the better field-effect passivation in the sample with ion dosage of 1 e16 ion/cm^2. The sample with 1.5 e16 ion/cm^2 dosage performs the same as that of the 7.5 e15 ion/cm^2 sample during the second step but at the end of the hydrogenation steps there is drop due to deterioration in field-effect passivation.

RTP@ 500°C, 10 min -RTP@ 700°C, 2 min(x3) – The RTP set-up can't withstand temperatures greater than 700°C for a period greater than 2 min. So, it was decided to carry out the final RTP annealing at 700°C for 2 min, thrice to have total annealing time of 6 min. But in such a case the number of times the sample experiences thermal shock increases. A maximum iV_{OC} of 702 mV is seen for the sample with 1 e16 ion/cm^2 ion dosage which is similar to that of having an end annealing at 600°C for 10 min. If the RTP was carried out at 700°C for 10 mins the we might have achieved even higher iV_{OC} due to the reduction in thermal shock cycles.

Thus, it is understood that the annealing time and the temperature of the RTP process have significant effect on hydrogenation. For such triple capping layers temperatures as high as 650°C and annealing time of about 10 min are needed for the best passivation results. So, to check the concordance of such behaviour RTP annealing at temperatures greater than 600°C was carried out on the textured p^+ poly-Si samples and the best hydrogenation process was tested on a flat p^+ poly-Si samples in the following sections.



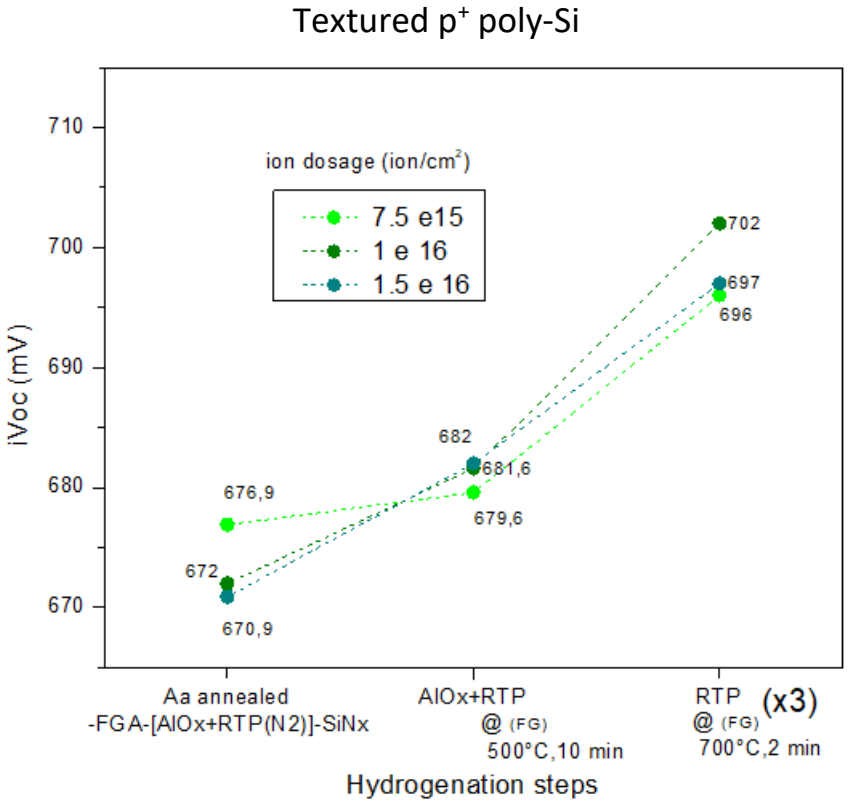


Figure 4.11 Passivation for textured p^+ poly-Si CSPC along the hydrogenation steps of $AlO_X/SiN_X/AlO_X$-RTPs. NOTE: The annealing conditions are mentioned along the x-axis.

RTP@ 600°C, 10 min -RTP@ 650°C, 10 min – The main difference which is observed in this process is during the second step. Previously the second step did not show any improvement in passivation when annealing was carried out by FGA or comparatively lower temperature RTPs. When annealed by RTP at 600°C, iV_{OC} as high as 708.7 mV was achieved even without an addition RTP. A maximum iV_{OC} of 711,3 mV is achieved at the end of a final RTP at 650°C for 10 min, which is the highest achieved in this thesis work.

The main finding in the optimisation of the textured p^+ poly-Si samples are as follows. Firstly, the triple capping layer plays an important role in enhancing the chemical passivation. Secondly, higher the final RTP annealing temperature better is the chemical passivation. Lastly, the ion dosage of 1 e16 ion/cm^2 shows better field-effect passivation.

4.4.5.2 p^+ flat CSPC

The optimised hydrogenation process on the textured sample was tested on the flat sample as well. Figure 4.12 Bottom shows the passivation along the hydrogenation process. The maximum iV_{OC} achieved was 725.3 mV which is about 13 mV higher than previous optimal with SiN_X result. Also, when the final annealing step is either FGA or RTP at temperatures 450°C or 550°C, 10 min then the iV_{OC} of 715 mV was recorded (red dot in the plot). For the flat p^+ poly-Si samples only two annealing steps were carried out. The initially one being the N_2 annealing to prevent the hydrogen effusion during SiNx deposition and the second one after the complete capping layer deposition. Similar steps can be performed for the textured sample with just two annealing steps with the final one being RTP in FG at 650°C for 10 min. From the plot, the importance of all the steps throughout hydrogenation is clear. There is a noticeable change in the iV_{OC} values after each step. The 8 mV rise after the N_2 RTP is due to the hydrogen diffusion from the first AlO_X layer and the next 12 mV rise is due to the hydrogen diffusion from the other two capping layer.

Now, that we have performed different hydrogenation processes and to get a clear picture the results are consolidated into a single plot as shown in Figure 4.13 and discussed in the following section.

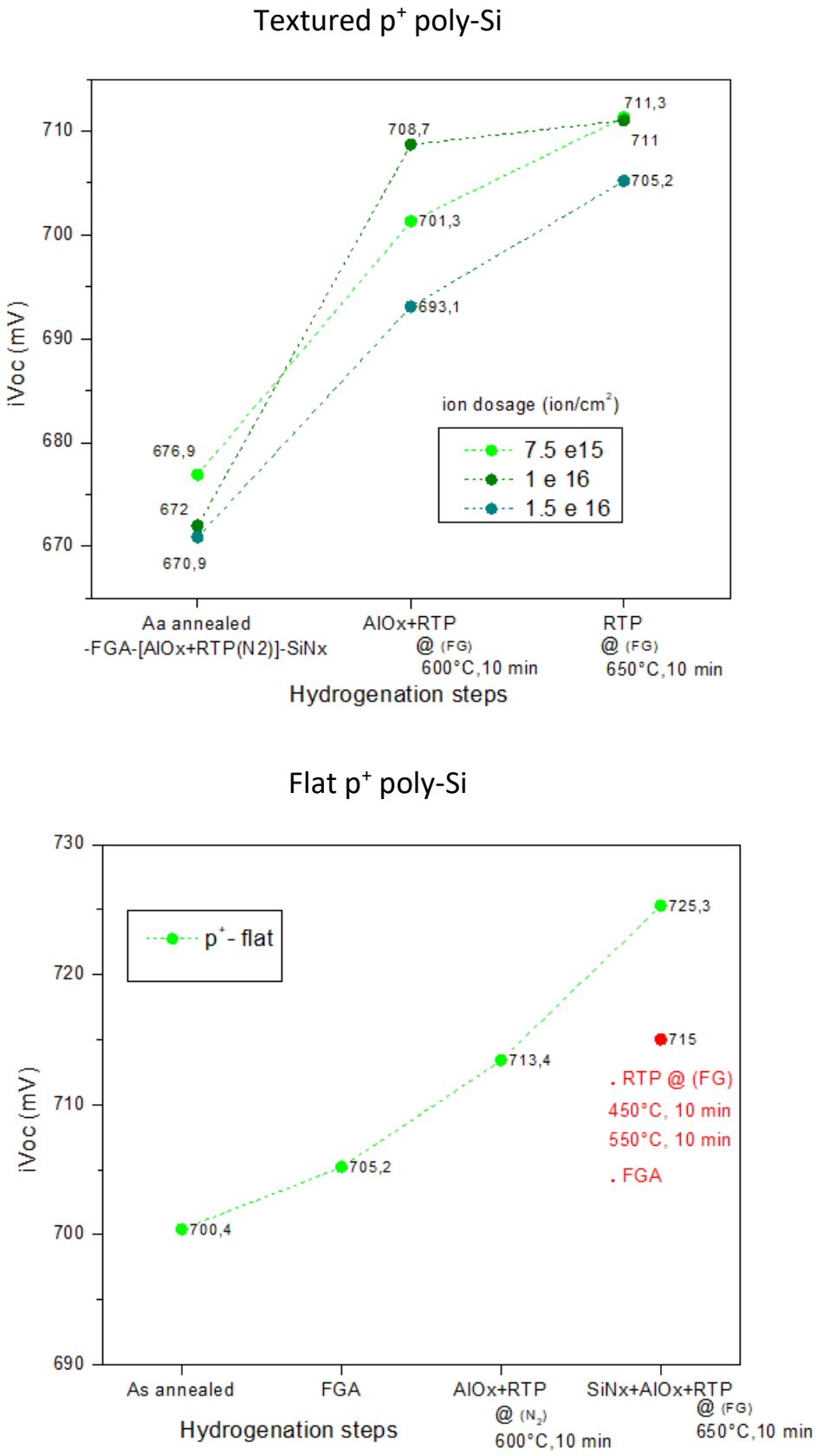


Figure 4.12 Passivation of p^+ poly-Si CSPC along the hydrogenation steps of $AlO_X/SiN_X/AlO_X$-RTPs. NOTE: The annealing conditions are mentioned along the x-axis. Top – textured p^+ poly-Si. Bottom – flat p^+ poly-Si – The red dot shows the results of the other final annealing steps performed.

4.4.6 Consolidated results

In this section the summary of all the different hydrogenation processes is presented.

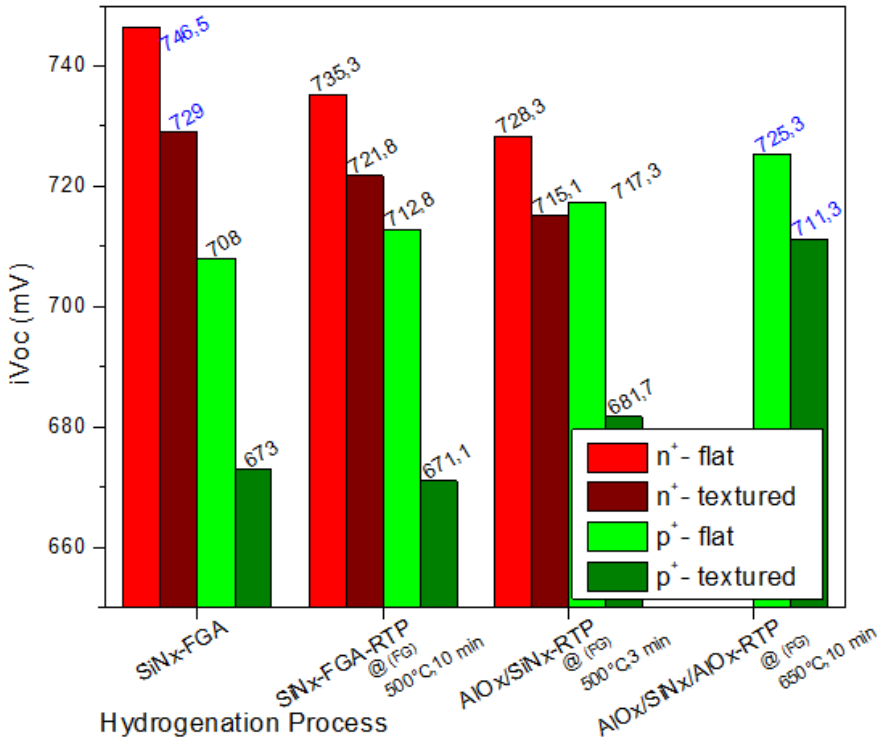


Figure 4.13 Passivation achieved with different hydrogenation processes for four different symmetric samples. NOTE: The hydrogenation conditions are mentioned along the x-axis. The last process is carried out only for the p^+ poly-Si samples. The best results are in blue.

For the n^+ poly-Si samples the best results are achieved with a single 120 nm (on flat) thick SiN_X capping layer followed by forming gas annealing in a furnace at 400°C for 1 hr. The iV_{OC} obtained are 746.5 mV and 729 mV for the flat and textured samples. The double capping layer annealing did not show any improvement in the passivation quality. On the other hand, for the p^+ poly-Si samples the double capping layer shows slight increase in passivation. Finally, when using a sandwich capping layer, the best passivation results were obtained. The best iV_{OC} of 725 mV and 711.3 mV were obtained with a final RTP annealing temperature of 650°C. Also, it is to be notes that these are the best passivation results obtained for the p^+ poly-Si samples both on flat and textured surfaces so far in the PVMD group.

4.5 Conclusion

Initially, the samples were subjected with the hydrogenation process which was previously used in the PVMD group. This hydrogenation technique was working good only for the n^+ poly-Si CSPC. In literature, double capping layers were documented to show a better passivation effect on the p^+ poly-Si samples.

Secondly, these double layer structures were tested and found to have a negative effect on the n^+ poly-Si samples. For the p^+ poly-Si samples only slight improvements in the passivation quality were observed. It was speculated that on annealing the hydrogen from the SiN_X layer effused out rather than crossing the AlO_X layer and passivating the interface (SiO_X/c-Si).

Thirdly, the triple capping layers were tested and found to have positive response in the passivation quality for the p^+ poly-Si layer. Annealing with RTP at 650°C for 10 min was found to give the best passivation results so for achieved in the group.

In this thesis the triple capping layers were not tested for the n^+ poly-Si samples. If there is no drop in the passivation effects, then it becomes simpler while fabricating the IBC solar cells as passivation can be done for both the n^+ and p^+ poly-Si CSPCs simultaneously. This will also reduce the processing time of the IBC solar cells to a great extent.

5 Front back contacted solar cells

In this chapter, in order to prove the carrier selectivity of the optimised poly-Si CSPCs, they are tested in the easy fabricate Front back contacted (FBC) solar cells. The chapter begins with the process flow for fabrication of the solar cells. Different cell structures such as Flat-Flat, Textured-Flat and Textured-Textured solar cells were fabricated and analysed. Three different metallisation processes were tested, namely, screen printing of silver paste, e-beam evaporation of Aluminium, and sputtering of silver. Also, the influence on the solar cell performances due to the TCO deposited on the poly-Si carrier selective contacts contacts were also tested. Post-TCO annealing and Post-metallisation annealing were performed to check for their impacts in the solar cell performance. The chapter ends with the conclusions based on the experiments.

5.1 FBC solar cell fabrication

Different cell structures were tested in this thesis work. But in this section the fabrication of a Textured-Flat FBC solar cell with TCO on each side (both n^+ and p^+ poly-Si CSPCs) is discussed. The metallisation is done by screen printing of silver. The schematic of such solar cell is as shown in Figure 5.1. The flow chart of the process is similar to the symmetric sample preparation as discussed in Section 3.4.1 with additional TCO deposition and metallisation steps. The optimised parameters in Chapter 3 were applied in the fabrication steps of the solar cells.

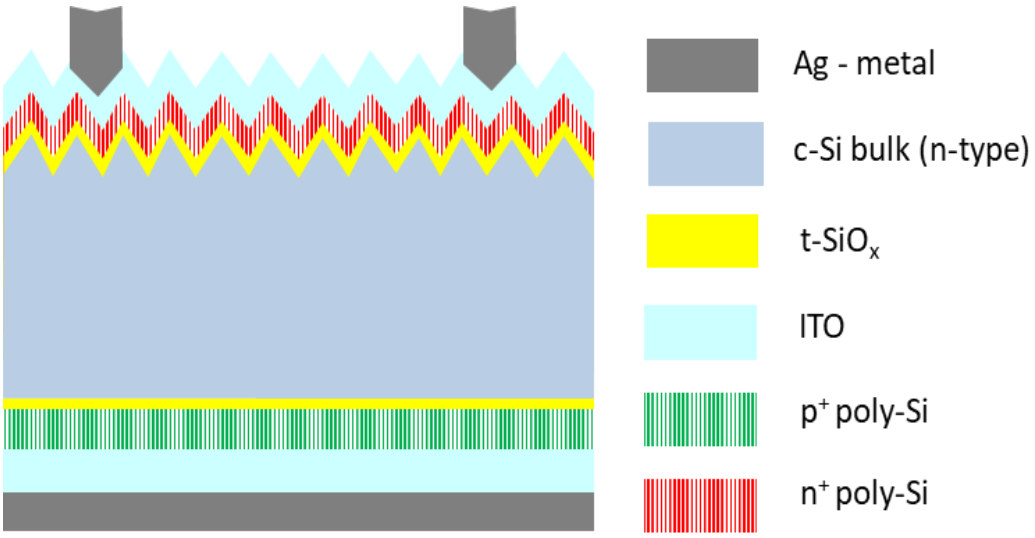


Figure 5.1 Schematic of a Textured-Flat FBC solar cell with a rear junction. Thermal oxide growth condition: 675°C, 3min. Post-implantation annealing condition: 950°C, 5 min. Hydrogenation process: SiN_X-FGA. Metallisation: Screen printing of silver.

The c-Si bulk used is a FZ n-type wafer with crystal orientation <100> and thickness around 280 µm. Initially, one side of the wafer is coated with a thin layer of SiN_X to prevent the surface from texturing. Then the wafer is subjected to texturing for 10 min in TMAH at 80°C. After texturing the size of the wafer is around 270 µm. Then the wafer is cleaned in DI water and dried in a spin dryer. Then the SiN_X layer is removed by etching in BHF. Marangoni drying is done to remove the native oxide and the wafer is subjected to Thermal Oxidation at 675°C for 3 min. Oxidation takes place on both the sides of the wafer. This oxidation condition is estimated to give a t-SiO_X thickness between 1 – 2 nm. This is followed by the deposition of a-Si on both the side by LPCVD. The deposition time is set at 113 min such that the deposited a-Si layer has a thickness of 250 and 200 nm on flat and textured side respectively. Next, ion implantation is carried out. As the cell being fabricated is a rear junction solar cell, the textured front side is doped with phosphorous and the flat back side is deposited with boron. The ion dosage used for phosphorous and boron are 1 e16 and 5 e15 ions/cm^2 respectively. The energy used for phosphorous and boron doping is 20 and 5 keV respectively. Then the wafers are subjected to a standard cleaning process. Then the implanted ions activation and thermal phase transition of a-Si to poly-Si is carried out by the post-implantation annealing step. The post-implantation annealing condition used is 950°C, 5 min. This followed by Forming Gas Annealing at 400°C for 1 hour.

Then the cell precursor is subjected to hydrogenation. The hydrogenation process used in SiN_X-FGA. SiN_X is deposited by PECVD at 400°C for 8 min on both the sides. This gives a SiN_X layer thickness of 120 nm on a flat surface. Then the capping layer is removed in BHF before the deposition of the TCO. This is followed by ITO deposition on both the sides with the help of hard mask. The thickness used for the front side is 75 nm and for the rear side is 120 nm. Then the solar cell fabrication is completed with screen printing of silver for the front and back contacts. The solar cells are then annealed at 170°C for 45 min. This is followed by hot-plate annealing for a better contact with the TCO layer. Lifetime measurements are done between the required steps to keep a track on the iV_{OC} of the cell precursor at each step after post-implantation annealing.

At the end of all these processes, solar cell as shown in Figure 5.1 is fabricated and the characteristics can be studied.

5.2 Solar cells with Screen Printing - Silver

In this section the results of the solar cells metallised by screen printing with silver are discussed. The thickness of the metal obtained from screen printing varies between 10-15 µm. With this metallisation process three different solar cell structures were tested and the importance of TCO layer and post-metallisation annealing are tested on Flat-Flat and Textured-Flat solar cells. The textures-textured solar cells were used in comparing a rear and front junction solar cell. Only the V_{OC} and FF are analysed, because these layers going to be implemented in an IBC solar cell structure in the future. The cells measured have a metal coverage of 4.4% and the size of the cells are 4 cm^2

5.2.1 Flat-Flat Solar Cells

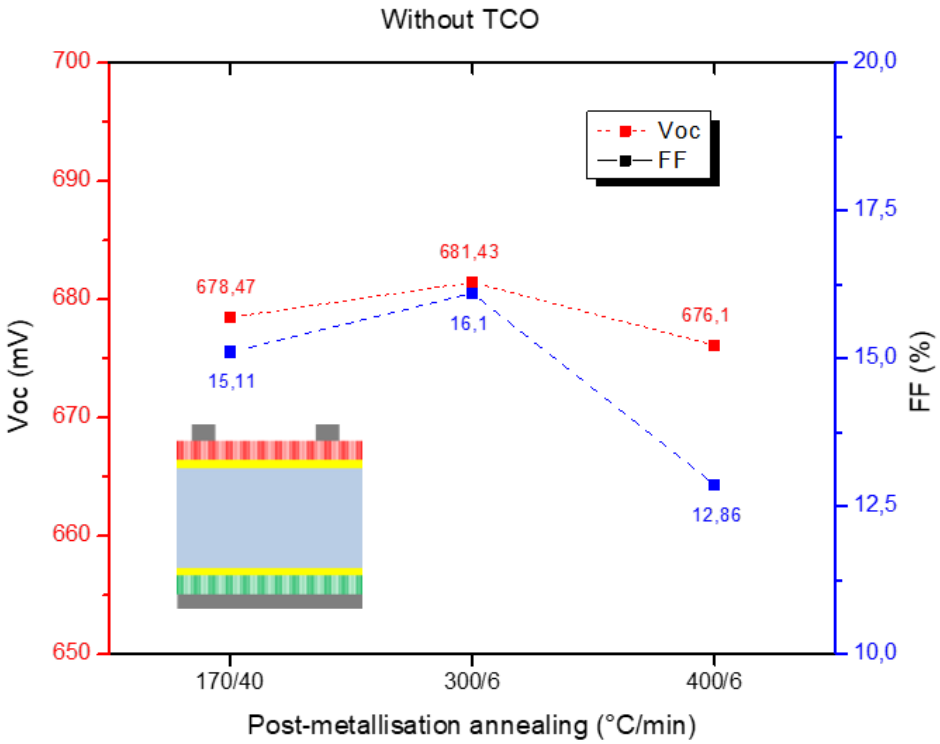
Three different flat-flat solar cells were designed to study the necessity for a TCO layer for metallisation by screen printing. Solar cells with no TCO layers, TCO on the front side and TCO on both sides were fabricated. These cells are rear junction solar cells. The iV_{OC} of a flat-flat poly cell precursor is within the range 715 to 720 mV. This value is within the average iV_{OC} of the corresponding symmetric samples. An annealing step at about 350°C is found to increase the performance of the cells [82]. So, annealing after metallisation is performed.

Solar cell Without TCO – After metallisation a 40 mV drop in the V_{OC} is noticed. The measured FF is 15.11%. To check if there is any improvement in the solar cells, two addition annealing steps were performed by hot plate. A 3 mV gain in V_{OC} and $1\%_{abs}$ rise in FF were notices when annealed at 300°C for 6 mins. On further annealing at 400°C a decrease in FF and V_{OC} is encountered. The low FF can be because of the no proper contact between the metal and the poly-Si layer leading to an increase in series resistance. The Suns-V_{OC} and pseudo-FF (pFF) values for the measured cells after metallisation are 694 mV and 81.8% respectively. The huge difference between the FF and pFF shows the high resistance along the current flow across the CSPC and to the metal. The post-metallisation annealing of the solar cell is shown in Figure 5.2 a.

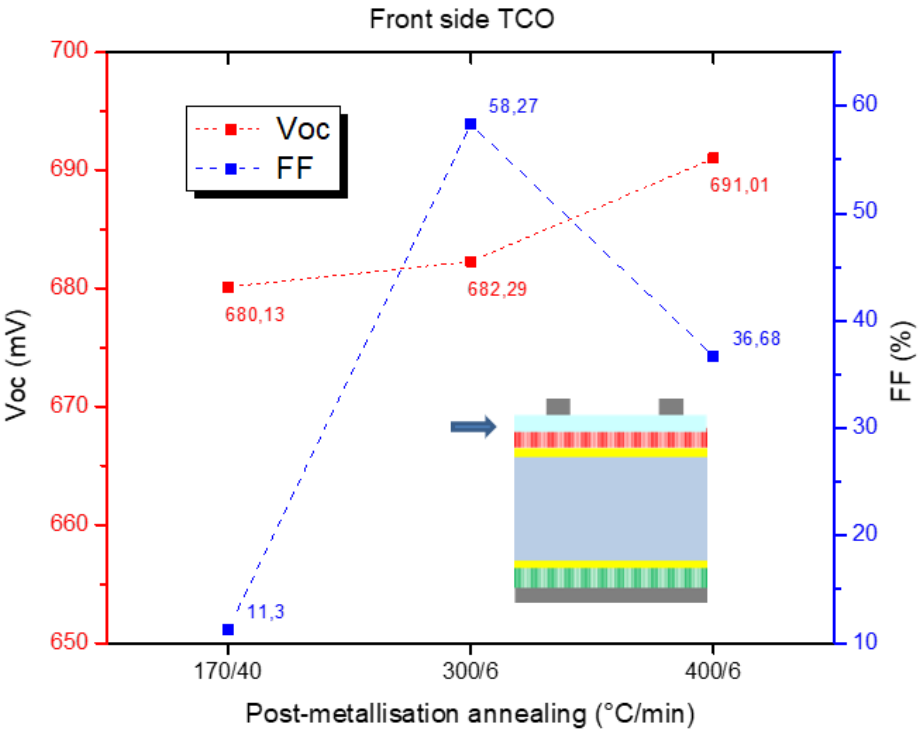
Solar cell Front side TCO – Similar annealing test was carried out with an additiona ITO layer below the front metal. The results are represented in Figure 5.2 b. The maximum V_{OC} of 691

mV was achieved when annealed at 400°C for 6 mins. A tremendous rise of 47% in FF is seen when annealed at 300°C for 6 mins, on further annealing the FF experiences a 21% drop. It is clear that the TCO layer has helped increasing the FF from 16.1% to 58.27% .

(a)



(b)



(C)

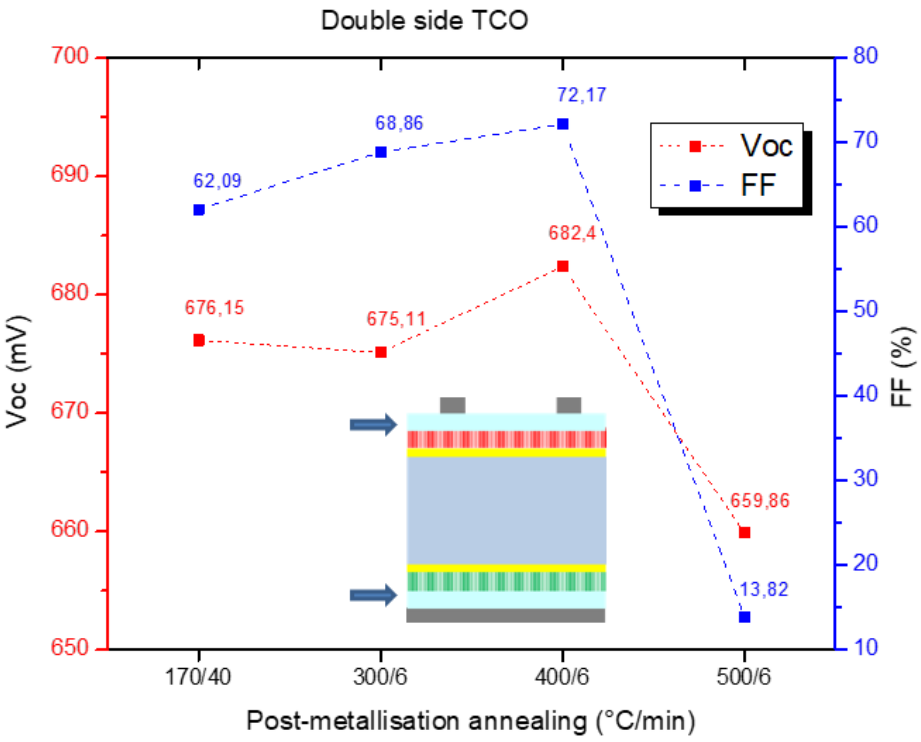


Figure 5.2 V_{OC} and FF of Flat-Flat poly-poly solar cells along different post-metallisation annealing steps. Note: (a) Without TCO, (b) TCO on front side (c) Double side TCO. First annealing step is carried out in an oven. The rest are done by hot-plate annealing.

Solar cell Double side TCO – With doubes side TCO, FF of 69.09 % is achieved even without any extra annealing steps. On hot-plate annealing at 400°C for 6 min, FF as high as 72.17 % and V_{OC} of 682.4 mV is observed.

Hence, the optimised Flat poly-Si CSPCs perform better with the help if a TCO layer above it as a result of better lateral charge transport in case of metallistaion by screen-printing.

Also, Post-TCO annealing is also found to increase the opto-electrical property of the ITO layer [82], [83]. Can Han et al, has experimented post TCO deposition annealing on Fluorin doped Tin Oxde (FTO) in various atmospheres and have found that annealing in H_2 for 60 min have decreased the contact resistivity of the metal/TCO/poly-Si interface. For instance, the contact resistivity of metal/TCO/n^+ poly-Si interface after post deposition annealing has decreased from 34 to 20 mΩ.cm^2 [83]. The thickness of the n^+ poly-Si is 24 nm. So, after TCO deposition the cell precursor is subjected to annealing and the results are as follows.

Influence from post-TCO Deposition – The iV_{OC} and J_0 values of the doulbe side TCO flat-flat cell precursors after TCO deposition is 713.5 mV and 9.62 fA/cm^2 respectively. After annealing for 60 min in hydrogen atmosphere a sight decrease in the passivation quality was obsevered. The iV_{OC} and J_0 values after post deposition annealing are 711.3 mV and 12.3 fA/cm^2. After metallisation, the obseved V_{OC} and FF were 671 mV anf 67.44 % respectively. On furthur annealing at 400°C for 6 min (optimum as per Figure 5.2 c) a 10 mV rise in V_{OC} and 6.2 % drop in FF is encountered.

This behaviour may be due to the fact that the poly-Si layer are very thick and doesn't suffer from any damage during ITO sputtering. Hence such post-deposition Annealing may not be necessary in our case.

5.2.2 Textured-Flat Solar Cells

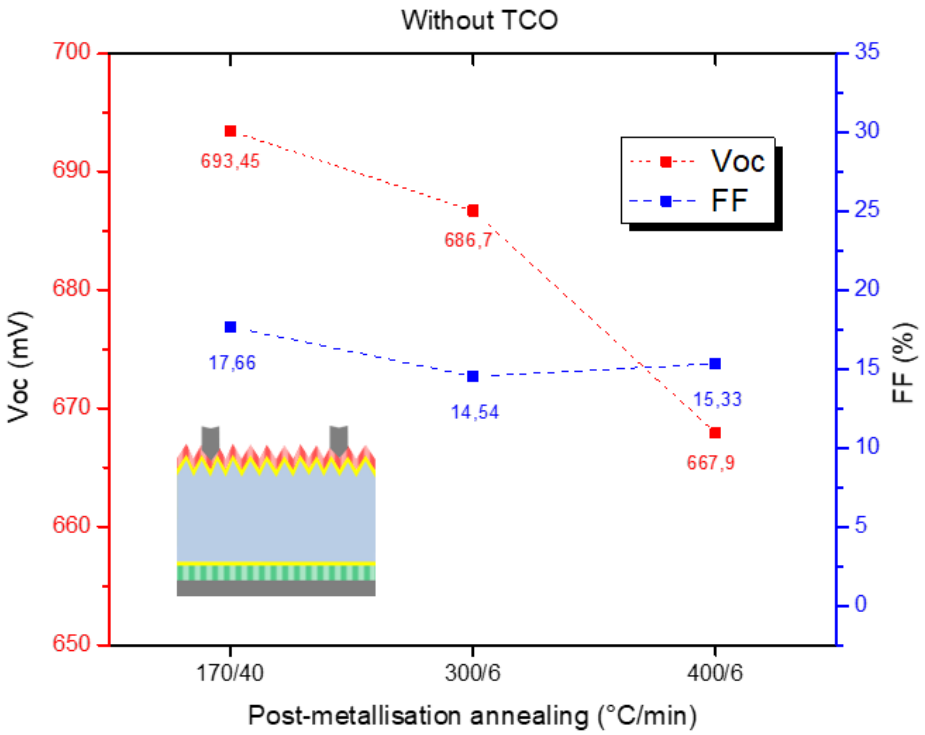
Similar post- metallisation annealing and post- TCO deposition annealing study was carried out with the help of textured-flat poly-ploy solar cells and their results are discussed in this section. Cell precursors with a maximum iV_{OC} of 725.5 mV (after TCO deposition) were achieved in this thesis work.

Solar cell Without TCO – The influence of annealing on the solar cell is shown in Figure 5.3 (a) V_{OC} of 693.45 mV was achieved without any hot-plate annealing step. Very low FF of 17.66 % is observed. The suns-V_{OC} and pFF were 705 mV and 83 % respectively.

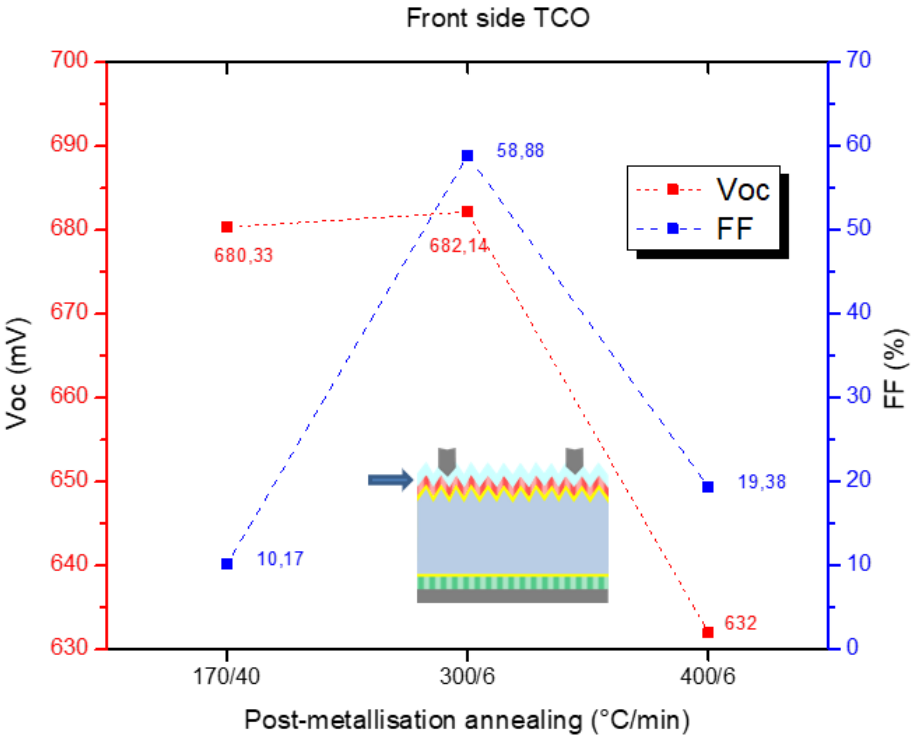
Solar cell Front side TCO – As shown in Figure 5.3 (b), the maximum performance of the cell was observed after hot-plate annealing at 300°C for 6 min. The performace is nearly the same as that of the Flat-Flat cell with Front side TCO.

Solar cell Double side TCO – The maximum V_{OC} and FF in this thesis work is achieved with this solar cell structure reading to 699,7 mV and 72.22 % respectively. The annealing is perormed in 50°C steps to find the accurate annealing conditions. It is found that 350°C, 6 min gives the best performance. This complies with the findings from Leonard et al [82]. The sharp drop after this point might have occurred to two possible reasons. After this temperature the morphology of the ITO layer changes such that its resistivity increases.

(a)


Without TCO
Voc (mV)
FF (%)
Voc
FF
693,45
686,7
667,9
17,66
14,54
15,33
700
690
680
670
660
650
35
30
25
20
15
10
5
0
170/40
300/6
400/6
Post-metallisation annealing (°C/min)

(b)


Front side TCO
Voc (mV)
FF (%)
Voc
FF
680,33
682,14
632
58,88
10,17
19,38
700
690
680
670
660
650
640
630
70
60
50
40
30
20
10
0
170/40
300/6
400/6
Post-metallisation annealing (°C/min)

c)

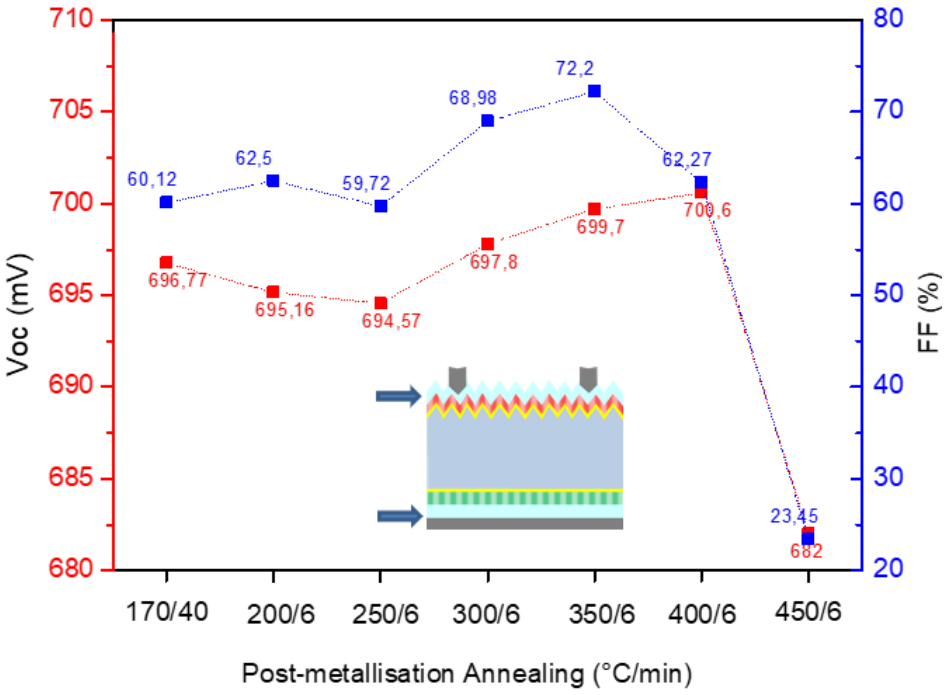


Figure 5.3 V_{OC} and FF of Textured-Flat poly-poly solar cells along different post-metallisation annealing steps. Note: (a) Without TCO, (b) TCO on front side (c) Double side TCO. First annealing step is carried out in an oven. The rest are done by hot-plate annealing.

This behaviour is also observed by Elise et al. The contact resistivity of n^+ poly-Si/ITO interface as after screen printing (32 mΩ.cm^2) rises to 43 mΩ.cm^2 on firing at 550°C [84]. Another reason is that at higher temperatures oxygen from the ITO layer might react with silicon forming a SiO_X layer between poly-Si/TCO interface. Such behaviour is seen when annealed at temperatures greater than 450°C [85].

Post-TCO Deposition Annealing – No significant drop in iV_{OC} is experience after the TCO deposition. The iV_{OC} and J_0 values right after TCO deposition are 725 mV and 11.3 fA/cm^2. After post-TCO depostion annealing at 400°C for 60 mins the iV_{OC} drops by 4 mV and J_0 increases by 4.2 fA/cm^2. After metallisation, the obseved V_{OC} and FF were 689.98 mV anf 62.05 % respectively. On furthur annealing at 350°C for 6 min (optimum as per Figure 5.3 c) the V_{OC} and FF rised to 691 mV and 64.3 % respectively.

The performance of a Texturted-Textured poly-poly solar cells is discussed in the following section.

5.2.3 Textured-Textured Solar Cells

The main purpose of studying the such a solar cell structure is to have a base line for the comparison of a bi-facial IBC solar cell with textured n^+ and p^+ poly-Si CSPCs in the future. The schematic of such a cell is as shown in Figure 5.4

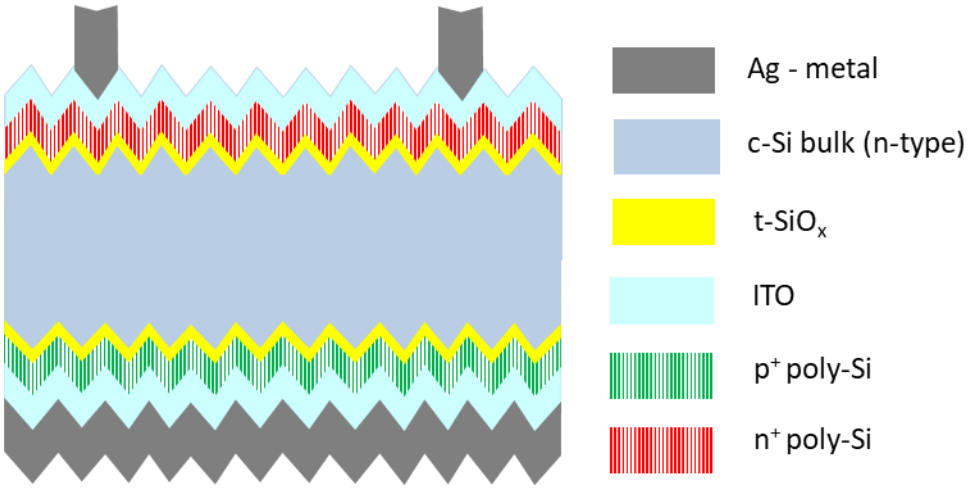


Figure 5.5 Schematic of a Textured-Textured poly-poly solar cell. Metallisation is done by SP.

The iV_{OC} and the J_0 values after hydrogenation and removal of capping layer are 696.1 mV and 64.2 fA/cm^2 respectively. The iV_{OC} value is 10 mV smaller than the average of best values from textured CSPCs. This drop is seen because the hydrogenation process used is SiN_X-FGA, which is not the best hydrogenation step for the textured p^+ poly-Si CSPCs as discussed in Chapter 4. The cells were completed with screen printing, followed by annealing at 170°C for 40 min. The V_{OC} and FF obtained from this cell are 674 mV and 56.45 % respectively. The annealing test were not performed for the textured-textured cells. Due to the low FF values obtained from Screen Printing it was decided to carry out metallisation through e-beam evaporation as discussed in the next section.

5.3 Solar cells with e-beam Evaporation – Aluminium

Textured-flat solar Cells without TCO layers are tested by using metallisation of Aluminium by e-beam evaporation. The cell area and metal coverage of the cells analysed in this section are 8.968 cm^2 and 1.9268 % respectively. The metallisation is done with the help of photolithography and lift-off. The schematic of such a cell is shown in Figure 5.5. SiN_X layer of 80 nm thick is used as an anti-reflection coating. The front and the back metal thickness are around 2 µm.

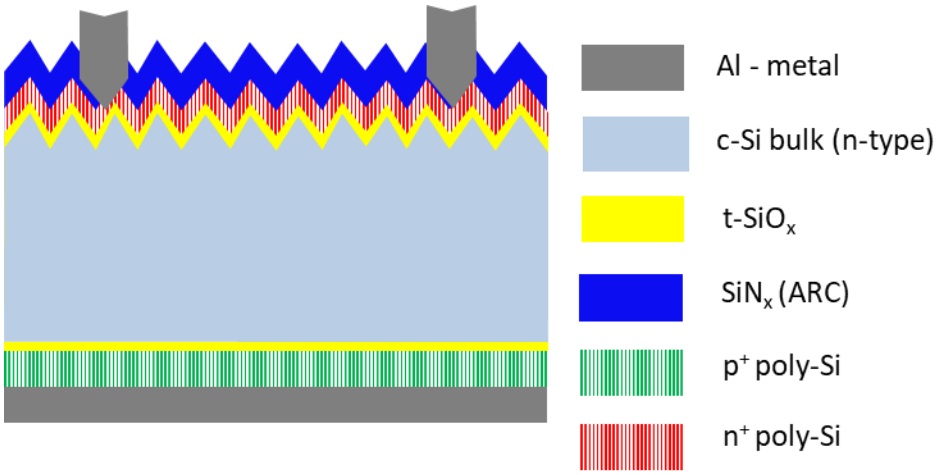


Figure 5.5 Schematic of a Textured-Flat poly-poly solar cell without TCO. Metallisation is done through e-beam Evaporation.

The maximum V_{OC} and FF achieved from this cell is around 711.24 mV and 64.3 %. The suns-V_{OC} and pFF measured for these cells were 720 mV and 80.7%. Hot plate annealing was performed as shown in Figure 5.4 for 90 s at different temperatures. The annealing steps did not have any positive influence on the performance of the solar cell as shown in Figure 5.6.

The low fill Factor achieved compared to that of screen printed solar cells is because the thinner contacts, as the resistivity scales inversely with thickness (height) of the metal contact [5]. Also, the conductivity of aluminium is half the conductivity of silver at room temperatures [86].

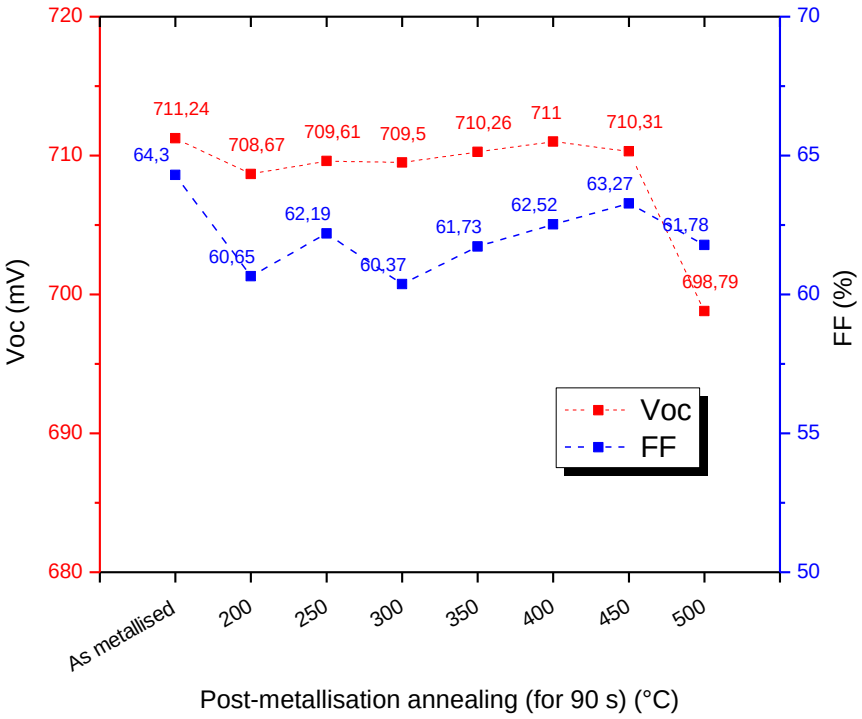


Figure 5.6 V_{OC} and FF of Textured-Flat poly-poly solar cells along different post-metallisation annealing conditions

5.4 Solar cells with sputtering – Silver

Relatively thicker metal contacts can be made through sputtering. Tests were carried on Flat-Flat and Textured-Flat cell precursors. Metal thicknesses of 5 µm and 3 µm were tested. It was found the adhesion between the silver through sputtering and the TCO or poly-Si were poor on both flat and textured surfaces. So, during lift-off the fingers and bus bars were peeled off. The reason for such behaviour is not clearly known. One of the suspected reasons is that the temperature during sputtering is higher than expected leading to poor adhesion. Smaller metal thicknesses have to be studied to find out the maximum thickness that can be still used without any adhesion. The fabricated cells during lift-odd process is shown in Figure 5.7.

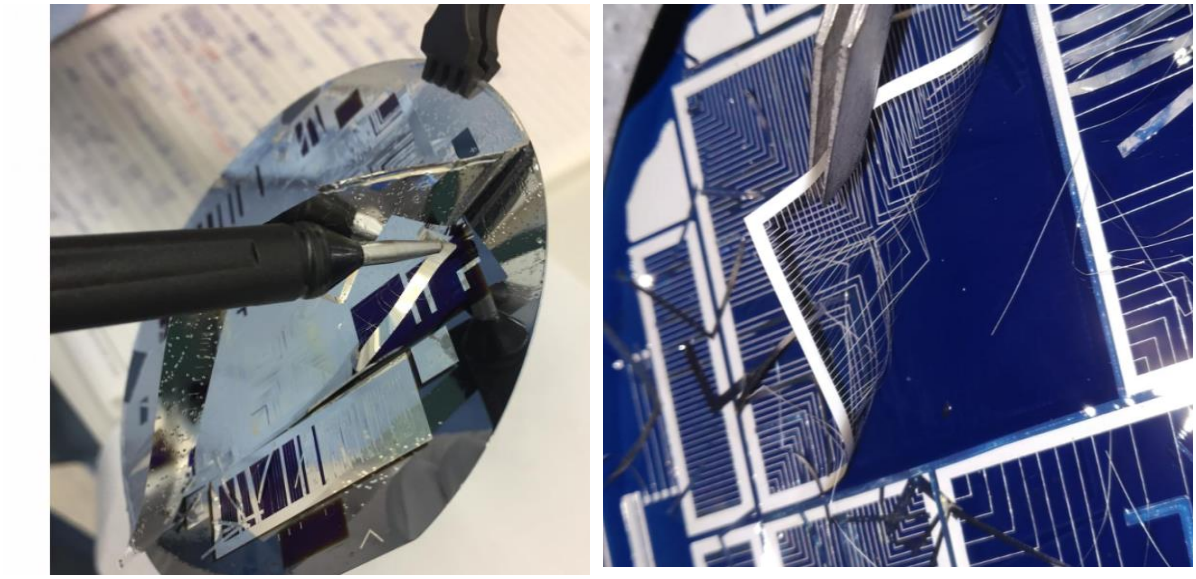


Figure 5.7 Metal peel-off during Lift-off process. Metallisation: Silver sputtering. Note: Left – on flat surface with 5 µm thick metal. Right – on textured surface with 3 µm thick metal.

5.5 Conclusion

In this chapter the optimised CSPCs fabrication conditions were tested in FBC solar cell structures. Three different metallisation techniques were tested with flat and textured CSPCs. The maximum V_{OC} and FF got from the Flat-Flat solar cell through SP were achieved for the CSPCs assisted with a TCO layer after annealing in hot plate at 400°C for 6 min. For the Textured-Flat Screen Printed (Ag) solar cell with TCO on both the sides, the best achieved FF and V_{OC} were 72 % and 699.7 mV when annealed at 350°C for 6 min. Also, metallisation with e-beam evaporation (Al) assisted with photo-lithography were tested on textured-flat wafer without TCO. V_{OC} and FF of 711.24 mV and 64.3 % respectively were achieved after metallisation. No significant improvement in cell performance was noted on post-metallisation annealing. Lastly, by sputtering (Ag) metallisation was not successful due to the poor adhesion of sputtered silver on both flat and textured surfaces.

6 Conclusions

The main objective of the thesis work is to optimise the CSPCs with poly-Si enabled by an ultra-thin thermally grown SiO_X. This is done in two main stages. In stage one, the CSPCs were optimised. This includes finding the suitable thermal oxide growth conditions, doping concentration of the doped poly-Si layers, post-implantation annealing time and optimal poly-Si thicknesses. In stage two, to enhance the passivation effects different hydrogenation steps were conducted on the CSPCs optimised in stage one. Lastly, the performance of these CSPCs were tested with the help of FBC solar cell structures. The outcome of the experiments conducted in all these staged and recommendations for future work are presented in this chapter.

In Chapter 3, Two rounds of optimisation were performed in finding the best conditions for creating CSPCs. *In the first round of optimisation*, it was found that the best common post-implantation annealing temperature for both n^+ and p^+ CSPCs is 950°C. Annealing time of 5 min was observed to perform the best for n^+ CSPCs. Annealing time of 5 min and 15 min were found to perform the same in case of p^+ CSPCs. Also, lower thermal budget of oxide growth conditions such as 600°C, 6 min were found to give the best passivation effects for n^+ textured and flat CSPCs. On the other hand, the p^+ CSPCs were performing better with high thermal budget of oxide growth conditions such as 675°C, 6 min and 8 min. To find an optimal thermal oxide growth conditions and annealing time suitable for both n^+ and p^+ CSPCs second round of optimisation was carried out by fixing the annealing temperature at 950°C. *In the first round of optimisation*, oxide growth condition of 675°C and 3 min was tested for all the CSPCs. Lower annealing time of 2.2 min was found to give the passivation effect for textured and flat n^+ CSPCs and flat p^+ CSPC. Even lower temperature of 0.5 min was found to work the best for textured p^+ CSPC. But the downside of using a very small annealing time is that the contact resistivity of the CSPC at lower annealing time is high, which influences the carrier collection of the contact. Also, the textured p^+ sample showed poor passivation compared to the other CSPCs.

To investigate this issue ECV measurements were done for the textured p^+ poly-Si CSPCs. It was found that the ion dosage used during implantation was not sufficient to arrive at the desired doping concentration within the poly-Si layers. The change in ion-dosage from 7.5 e15 to 1 e16 ions/cm^2 was found to have the same effects after hydrogenation. Contact resistivity of the CSPCs were measured by TLM and the values were in the range of resistivities as found in literature. For the n^+ CSPCs the contact resistivity was found to be in the range 14.5 – 19 m$\Omega.cm^2$ and for the p^+ CSPCs in the range 15.5 to 31 m$\Omega.cm^2$. Decreasing trend in contact resistivity is clearly observed from the n^+ CSPCs as the annealing time increases attributed to the better solubility of the dopants. Finally, at the end of the chapter the Logarithmic Selectivity, S_{10} were calculated for the n^+ CSPCs without hydrogenation for better comparison. The S_{10} values for the textured samples were in the range 13.7 to 13.9 and for flat between 14 to 14.5.

The passivation comparisons are made only with the help of lifetime measurements. Also, we are not sure about the exact thickness of the oxide layer under different thermal budgets. So, it is recommended to carry out TEM – Transmission Electron Microscopy to find the oxide thickness under different conditions. Knowing the exact thickness of the t-SiO_X layer will help us in further optimisation of the oxide growth conditions, as it plays an important role in contributing to the series resistance in a solar cell device. Also, ECV measurements on n^+ poly-Si CSPCs has to be performed with difference in annealing conditions and oxide growth conditions to compare it with the p^+ poly-Si CSPCs.

In Chapter 4, different hydrogenation processes were carried out to improve the chemical passivation of the CSPCs. Initially, Hydrogenation was carried out with SiN_X followed by FGA. High passivation was achieved for the n^+ textured and flat samples. The passivation on p^+ samples were reasonable. To further improve the passivation of p^+ CSPCs hydrogenation with double and triple capping layers were studied in this chapter. With double capping layers the n^+ poly-Si CSPC showed less passivation quality compared to the former and a slight increase in iV_{OC} was observed for p^+ poly-Si sample. Suspecting a further increase when a triple capping layers are used, $AlO_X/SiN_X/AlO_X$ structure was tested on p^+ poly-Si CSPCs, which has given the best passivation so far achieved in the group. These capping layers were subjected to high temperature RTP annealing processes and FGA. The best performance of n^+ CSPC was with

SiN_X-FGA . The iV_{OC} from this hydrogenation process are 746.5 mV and 729 mV for flat and textured samples respectively. The best performance of p^+ CSPC was with $AlO_X/SiN_X/AlO_X$-RTP at 650°C, 10 min in FG atmosphere . The iV_{OC} from this hydrogenation process are 725.3 mV and 711.3 mV for flat and textured samples respectively.

It is recommended to check the hydrogenation process of $AlO_X/SiN_X/AlO_X$-RTP at 650°C, 10 min in FG atmosphere on n^+ poly-Si CSPCs. If there is no significant drop compared to SiN_X-FGA hydrogenation process, then the former can be used in a IBC solar cell for hydrogenation, which might lead to better performing p^+ CSPCs.

Lastly, in Chapter 5 the optimised CSPCs were tested in FBC solar cells. It was found that using TCO layers helped in better performance of the cell metallised through screen printing of silver. A post metallisation annealing at 350°C, 6 min by hot plate gave the best solar cell performance with V_{OC} and FF of 699.7mV and 72%. Also, from post TCO deposition annealing step, it was concluded that the TCO sputtering did not impart damages to the poly-Si CSPCs. The FF by screen printing can be further increased by high temperature fire through pastes which will give better contact between the metal and TCO layer. Also, double print can be implemented to further increase the thickness of the contacts, which reduces the resistivity of the metal.

Also, metallisation by e-beam evaporation of Aluminium assisted by photolithography and lift-off were tested on FBC solar cells. The maximum V_{OC} and FF obtained by this process is 711.27 mV and 64.3% respectively. The low FF compared to the previous can be attributed to relatively thinner metal (2 µm) used compared to that of screen printing (10 – 15 µm).

Moreover, the low FF may have raised due to a thicker oxide layer grown as expected, which could only be concluded if the true thickness of the thermal oxide is known.

In the current research work that is being carried out in the PVMD group, the optimised CSPCs are being tested in a IBC and bi-facial IBC solar cell structure.

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