Optimal topology for a three port PV-EV-Grid power converter

With focus on efficiency and power density

by Albert Bassa de los Mozos

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Thesis committee:	Prof. dr. P. Bauer,	TU Delft, supervisor
	Dr. J. Popovic,	TU Delft
	Dr. O. Isabella,	TU Delft

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Abstract

Environmental awareness keeps increasing among Earth population, and greener technologies arise to reduce the human dependence on fossil fuels and the green house effect. This thesis focuses on the research for a new solution that smooths the path to a green future.

Electrical generation from the sun energy was discovered in 1839 but until 1954 the first practical silicon solar cell was not released by Bell Labs. Since then, the technology has evolved in terms of efficiency and the price of acquisition and installation has been reduced, making it possible to install photovoltaic panels in northern countries with low sunshine and still make profit.

On the other hand, electric vehicles with a relatively high autonomy are just starting to be released. Tesla is the reference on the sector with cars that have a range over four hundred kilometers. However, the electricity used to power these cars comes from the grid, where electricity is formed by a mix of different energy sources, including carbon, fuel and gas. Total efficiency when using electricity from those sources is lower than when using combustion engines directly; therefore, it is convenient to use green sources for electric vehicle charging.

As years go by more private consumers will install photovoltaic panels on their roofs and use electric vehicles to move around. Therefore it is sensible to directly charge the car battery from the energy produced by the owner's solar array. Actual solutions are one-purpose made; two different power converters have to be installed, on for solar energy and another one for car charging, increasing cost and complexity and reducing the efficiency due to a higher number of power conversions.

This thesis focuses on the search of the optimal converter which performs both electric vehicle charging and photovoltaic energy production. The three port converter design in this thesis must be able to charge the battery from both the grid and solar power, and inject current to the grid from both the solar array and the EV battery, allowing Vehicle to Everything (V2X) operation. Maximal efficiency is wanted to reduce heating and maximize profit while keeping the overall volume low, making the product appropriate for both residential and industrial applications, like solar car charging slots in industrial areas.

The first half of the report contains a literature review in order to determine the optimal candidates, a framework with the evaluation criteria to evaluate the topologies, the analytical loss model for the assessment of the converters,the design of the magnetic elements and the selection of the different components.

The second part of the report is a converter per converter review of the selected topologies. A detailed analysis of the steady state equations that describe the operation of each topology is performed, the requirements of the different elements derived and a short explanation regarding methods of efficiency improvement are listed. Afterwards, the design results are displayed in the form of plots and tables, which are used to finally evaluate each converter with respect to the predefined comparison framework.

The optimal multiport converter relies on a DC link at 750V. The PV panels are connected via a four phases Coupled Inductors Interleaved Boost Converter (CIIBC) with reverse coupled inductors with a switching frequency of 50 kHz, the EV charger relies on a four phases Interleaved Bidirectional Flyback Converter (IBFC) working in Boundary Conduction Mode (BCM) and the DC-AC connection on a Two Level Converter (2LC) working at 100 kHz with the Near State Pulse-Width Modulation (NSPWM) technique.

Acronyms

2LC	Two Level Converter.
2M1ZVPWM	2 Medium 1 Zero Vectors Pulse-Width Modulation.
3LNPC²	Three Level Neutral Point Clamped Converter.
3LT²C	Three Level T-Type Converter.
3MVPWM	3 Medium Vectors Pulse-Width Modulation.
AWG	American Wire Gauge.
BCM	Boundary Conduction Mode.
BICM	Boundary Inductor Conduction Mode.
CCM	Continuous Conduction Mode.
CICM	Continuous Inductor Conduction Mode.
CIIBC	Coupled Inductors Interleaved Boost Converter.
CMV	Common Mode Voltage.
CSPI	Cooling System Performance Index.
DAB	Dual Active Bridge.
DAHB	Dual Active Half-Bridge.
DCM	Discontinuous Conduction Mode.
DICM	Discontinuous Inductor Conduction Mode.
DPWM	Discontinous Pulse-Width Modulation.
DPWM1	Discontinous Pulse-Width Modulation 1.
ESR	Equivalent Series Resistance.
EV	Electric Vehicle.
FBT	Flyback Transformer.
FFT	Fast Fourier Transform.
FPGA	Field Programmable Gate Arrays.
HFL	High Frequency Link.
HFT	High Frequency Transformer.

IBC Interleaved Boost Converter.
IBFC Interleaved Bidirectional Flyback Converter.
IGBT Insulated Gate Bipolar Transistor.
iGSE Improved Generalized Steinmetz Equation.
ISSBC Interleaved Soft Switching Boost Converter.

MPP Maximum Power Point.
MPPT Maximum Power Point Tracking.

NSPWM Near State Pulse-Width Modulation.

PCB Printed Circuit Board.
PSM Phase Shift Modulation.
PV Photovoltaic.
PWM Pulse-Width Modulation.

qZSI quasi Z-Source Inverter.
qZSI-2LC quasi Z-Source Two Level Converter.

SMPS Switched Mode Power Supplies.
SPWM Sinusoidal Pulse-Width Modulation.
SVM Space Vector Modulation.
SVPWM Space Vector Pulse-Width Modulation.

THD Total Harmonic Distortion.
TLBC Three Level Boost Converter.

V2X Vehicle to Everything.
VRLA Valve-Regulated Lead-Acid.
VSI Voltage Source Inverter.

ZCS Zero Current Switching.
ZSI Z-Source Inverter.
ZVS Zero Voltage Switching.
ZVS-IBC Zero Voltage Switching Interleaved Boost Converter.

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Acknowledgements

This thesis is the final requirement for the MSc degree in Electrical Engineering and shows the main reason why I started studying at TU Delft. I believe power electronics are the main enabler for a future full of renewable energies and will also play a key role in future mobility.

I would like to thank my supervisor Gautham Ram for his assistance during the writing of this thesis, weekly meetings and incisive questions that have made me dig deeper into the work. It has been a pleasure to have your guidance. Álvaro Conesa also deserves to be mentioned, as the knowledge he has shared with me about the Dual Active Bridge topology has boosted my work pace in the last months of the thesis.

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Last but not least, the love and support of all my family, who have always encouraged me to continue my education and let me do what I like the most. I know it has not been easy to *let me go* but I can proudly say I have done good use of the the time I have spent away from home. Thank you for everything you have done and will do for me.

Delft, University of Technology — Albert Bassa de los Mozos
August 26, 2016

1 Introduction

This report focuses on the research for the optimum topology of a multiport converter which is able to withdraw energy from an array of PV panels, charge or discharge an electric vehicle battery and inject or dump power to the grid at the same time. An all-in-one solution targeted for private households and solar parking slots.

In this chapter the concept and purpose of the multiport converter is explained on Section 1.1, while the state of the art is explained on Section 1.2. Sections 1.3 and 1.4 focus on the research questions that have to be answered at the end of the thesis work and the methodologies used to perform the work. Lastly, in Section 1.5 a summary of the report structure is presented.

1.1. EV and PV integration in a single converter

Environmental awareness keeps increasing among Earth population, and greener technologies arise to reduce the human dependence on fossil fuels and the green house effect. Electrical generation from the sun energy was discovered in 1839 but until 1954 the first practical silicon solar cell was not released by Bell Labs. Since then this technology has evolved in terms of efficiency and the price of acquisition and installation has been reduced, making it possible to install photovoltaic panels in northern countries with low sunshine and still make profit. However, power generated by the solar cells is continuous current, known as DC, but the most part of the electrical energy consumed is in the form of alternating current, known as AC. A device is needed in order to adapt the electrical energy of the photovoltaic panels and inject it to the grid, a power converter which performs DC to AC conversion.

Power converters make use of solid-state electronics for the control and conversion of electric power. The first high power electronic devices were mercury-arc valves. In modern systems the conversion is performed with semiconductor switching devices such as diodes, thyristors and transistors. In contrast to electronic systems concerned with transmission and processing of signals and data, in power electronics substantial amounts of electrical energy are processed. Usually, power converters are unique purpose made; either they rectify, invert or change AC or DC power. The main purposes a power converter is used are:

- AC to DC conversion (rectifier)
- DC to AC conversion (inverter)
- DC to DC conversion
- AC to AC conversion

On the other hand, electric vehicles with higher autonomy are just starting to be released on the market. Tesla, a US based company, is the reference on the sector with cars that have a range over four hundred kilometers. However, the electricity used to power these cars comes from the grid, which is in AC form, and electrical batteries store energy in DC form. Another converter is needed, in this case a rectifier, that converters the energy from the grid into DC form in order to charge the car.

Moreover, the electrical energy provided by the grid is formed by a mix of several different electricity sources, including carbon and fuel. Total efficiency when using electricity from those sources is lower than using combustion engines directly; therefore, it is convenient to use green sources for electric vehicle charging. As more private consumers will install photovoltaic panels on their roof and use electric vehicles to move around, it is sensible to directly charge the car battery from the energy produced by the owner's solar array. Actual solutions are one-purpose made; two different power converters have to be installed, increasing cost and complexity and reducing the efficiency due to a higher number of power conversions.

This thesis focuses on the search for the optimal converter which can be used as a single solution for both Electric Vehicle (EV) charging and Photovoltaic (PV) energy production. The three port converter must be able to charge the battery from both the grid and solar power, and inject current to the grid from both the solar array and the EV battery, allowing Vehicle to Everything (V2X) operation. Maximal efficiency is wanted to reduce heating and maximize profit while keeping the overall volume low, making the product appropriate for both residential and industrial applications, like solar car charging slots in industrial areas.

Currently there are no available all-in-one products which performs this tasks. EV owners who also have a solar panel installation in their households need to have two separate converters, increasing the number of conversion steps and thereby reducing efficiency. The same is also true for commercial installations in parking slots, where this multiport converter would result in a much more integrated solutions.

The V2X operation is not a must for the multiport converter. However, several publications have been made where electric vehicles batteries are pointed as enablers for a higher renewable penetration in the grid [4]. Storing energy in the car battery and withdrawing it at peak hours might increase the limits of renewable energy penetration. In order to do so, a bidirectional converter (known as V2X functionality for both the charger and the car) is needed and therefore considered as a must for the purpose of this work.

1.2. Existing solutions of multiport converters

At the time of writing this lines, there is only one all-in-one commercial product which performs the previously exposed tasks. Power Research Electronics B.V. or PRE is about to release a V2X charger with the possibility of addition of an external module which adds a photovoltaic input to the system with Maximum Power Point Tracking (MPPT) capabilities. It is an isolated charger with 10 kVA nominal power which is intended to be installed in charging posts when used alone or in solar parking slots when used with the complementary photovoltaic module. The characteristics of the system have been resumed in Table 1.1.

The characteristics of the PRE charger are taken as a reference for the development of the work in this thesis. Other aspects, like the power rating and some specifications will be discussed later on the report.

Table 1.1: Specifications of the PRE V2x500V32A charger (without PV port).

Output (Battery)	Voltage range	50 - 500V
	Current Range	-32 – +32A (bidirectional)
	Rated Power	10.000W
	Voltage Ripple + Noise	500mVp-p
	Voltage & Current Tol.	1% (typ.) 2% max.
	Line / Load Reg. (typ.)	2%
	Current Ripple (typ.)	<1Arms @ Rated Power (measured on a resistive Load)
	Hold up Time (typ.)	10mSec.
Input (Mains)	AC Voltage Range	400Vac +10%/-20% 47–63Hz (11kVA max.) 3ph +N + PE
	Power Factor	>0,99 @ 400Vac & Rated Power (THD<5%)
	Efficiency (max.)	Charge mode 95%
	Stand-by consumption	<1W @ Mains Relay Off /12W @ Mains Relay On
	AC Current (typ.)	16A @ 400Vac & Rated Power
	Inrush Current (typ.)	50A Cold Start @ 400Vac
	Leakage Current	<3.5mA @ 400Vac
Protection	Input UVP & OVP	Voltage & Frequency Window, Phase error
	Output OVP & OCP	550V (40A 600Vdc Fuse)
	Over Temperature	70ºC at main Heatsink. Output Power derating at >50 ºC
General	Protection (Isolation)	Class 1 (4kV In-Output/2kV PE-Input)
	Cooling	Fan cooled
	IP protection class	IP20

1.3. Research questions

The multiport converter can be build using different power conversion topologies, which have different advantages and disadvantages. The thesis main focus is to answer the next set of questions, which will make it possible to find the optimal topology.

1. Which is the preferred solution in terms of interconnection of the three ports of the converter?
2. Which is the optimal topology for a multiport converter which integrates photovoltaic energy production and electric vehicle charging, together with a grid connection?
   (a) Which is the optimal topology for the PV port?
   (b) Which is the optimal topology for the EV port?
   (c) Which is the optimal topology for the Grid port?
3. Is this solution competitive in terms of cost, size and development time with respect to actual solutions?

Some requirements apply to the power converter, in terms of safety, electrical regulations and development restrictions. These are explained during the report and have to be considered in order to answer the previous set of questions.

1.4. Research methodologies

The method which is used to find the optimal topology consists of implementing the procedure shown in Figure 1.1 for every topology considered in the comparison. This approach is similar to the one in

[5]. A software like Mathematica or Matlab has to be used in order to run the analytical models; for this work the Matlab software package has been selected because of the incorporation of simulation software Simulink and the Fast Fourier Transform (FFT) Power Analysis tools which are useful for the described work. A script is written for each topology, which follows the methodology described on Figure 1.1.

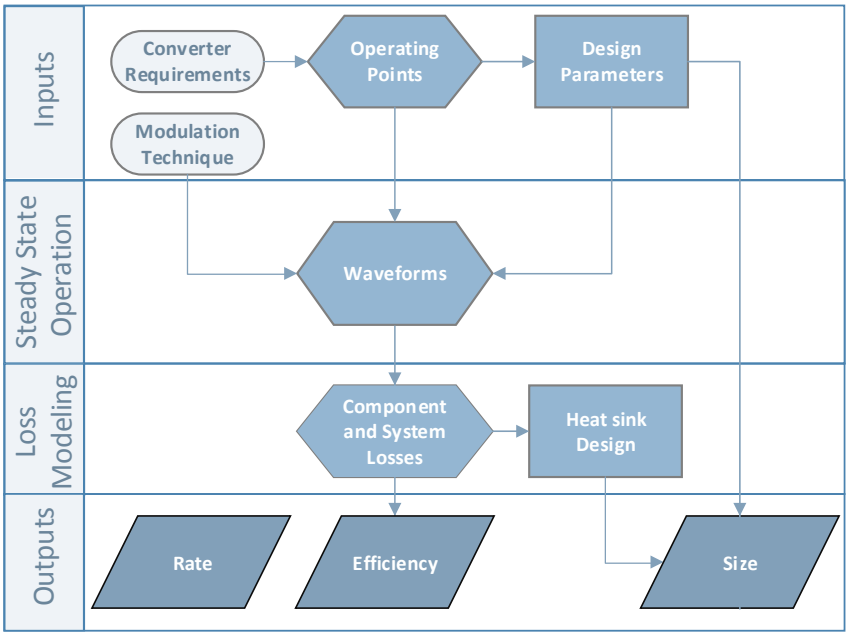


Figure 1.1: Overview of the methodology used to rate every topology

The inputs for every topology are the converter requirements, which are port dependent, and the modulation technique, which might vary in some converters. From this data the operating points of the converter can be obtained, and therefore the design and selection of the different power electronic elements that form the converter can be performed. With this information, and the topology itself, the voltage and current waveforms of the converter are obtained for every operating point. Once this is known, the component and system losses can be found using a loss model for every component. From this information, the efficiency of the converter is easily calculated. The final approximate volume of the converter is obtained by the heat sink size, which depends mainly on the losses, and the magnetic elements, which have been previously designed. As a summary, the steps that will be followed are:

- Literature study to select suitable topologies.
- Analytical analysis of each converter, including steady state operation waveforms.
- Design and selection of the different elements of each converter.
- Analytical analysis of the losses of the converter.
- Volume calculation of each converter.
- Literature review of the converter to analyze control and efficiency improvement possibilities.
- Rate each characteristic of the converter in order to obtain a final score.

This approach is straight forward for linear piece-wise steady state waveforms as found in DC-DC converters. However, when dealing with inverters, where voltages and currents are sinusoidal, a different approach has to be considered. This is reviewed in Section 3.3 of this report.

1.5. Report structure

The report is structured in 9 different chapters. In the first part of the report the candidate selection is made, and the loss model and design methods for the different elements explained. The second part is a topology per topology design and rating, split in four different chapters. The last part of the report is focused on solving the research questions previously stated, where the conclusions and future work are found.

- **Chapter 1**, introduction of the thesis; state of the art, research questions and methodologies.
- **Chapter 2**, literature study; multiport architectures and suitable topologies for each port.
- **Chapter 3**, loss modeling of the different power converter components
- **Chapter 4**, selection procedure or design methodologies for each power component.
- **Chapter 5**, PV port converters design and rating.
- **Chapter 6**, EV port converters design and rating.
- **Chapter 7,** Grid port converters design and rating.
- **Chapter 8**, Impedance Network based converters design and rating.
- **Chapter 9**, conclusions and future work.

2

Literature Study - Available Topologies

This chapter contains the required specifications of the system, on Section 2.1. The different possible system architectures are found on Section 2.2 while a literature study of the different topologies is performed in Section 2.3. Section 2.4 contains the framework designed to do the comparison and finally leakage current requirements of the converter are considered in Section 2.5.

2.1. Requirements of the system

Different topologies for multi-port converters for EV charging from photovoltaic panels have been proposed in literature [6]. For this project only charging one battery will be considered as it is a matter of connections and optimization of energy flows. In order to select the candidates properly the requirements of the multiport converter must be described. Figure 2.1 shows the main structure of the converter and the necessary connections. The different power conversions that have to take place are also represented.

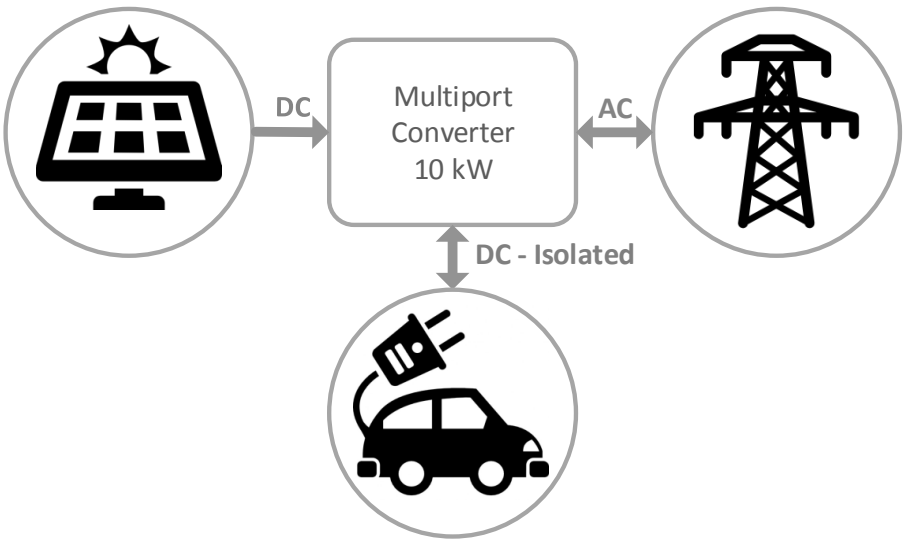


Figure 2.1: Block diagram of three-port DC-DC-AC converter

The rated power of the system has been selected to be 10kW. There are several reasons why

Table 2.1: Electric car data. Source: manufacturers websites.

Car	Battery Size [kWh]	Electric Range [miles]	EPA [miles/kWh]	Max Home Charge [kW]
Tesla Model X 90D	90	257	2.86	22
Tesla Model S 85	85	265	3.12	22
Toyota RAV4 EV	42	100	2.39	10
Mercedes B-Class ED	28	85	3.04	10
Volkswagen e-Golf	27	83	3.13	7.2
Nissan Leaf	24	75	3.13	6.6
Fiat 500e	24	87	3.63	6.6
Ford Focus Electric	23	76	3.30	6.6
BMW i3	22	81	3.68	7.4
Chevrolet Spark EV	21	82	3.85	3.3
Smart Electric Drive	17	68	4.12	3.3

this power rating is appropriate. Around 60 square meters of solar panels are required for a 10 kW solar installation with an efficiency of around 17% and this area is easily achieved in most residential households. If the system is intended for a public/industrial parking, a 60 squared meter roof would cover five cars, making it possible to install one solar powered EV charger for every five parking slots. The average peak sun hours in Europe according to SolarGis data [7], is around 4 hours at $1000W/m^2$ in Europe (2.5 in Stockholm, 2.7 in the Netherlands, 5 in Spain). This means that a 10kW installation can produce around 40 kWh per day in average trough out the year.

In Table 2.1 a list of characteristics of the most common EV vehicles in the market is displayed, in order to show the market maturity and compare it against the possible production of the multiport converter. The table shows how actually there are two ranges of EV battery sizes. Tesla models have a battery size about three times what the other car manufacturers offer. However, most cars have about 3 to 4 miles of range per kWh. This makes a 10 kW charger perfectly viable for any actual car, with full charging in three hours for a mid-range EV while a premium EV would take eight hours, which is a night charge. Most EV owners would be able to install and use a 10 kW multiport charger in their household, and it would fulfill the charging requirements in most of the cases for the actual necessities. If we consider the 40 kWh per day production obtained from the SolarGis data, approximately 120 miles could be charged every day only by using solar power in the multiport converter.

Considering industrial/commercial applications, a 10 kW solar powered multiport converter is also interesting. Assuming a 15 miles one way commuting distance, the multiport converter would cover the necessities of 4 cars in terms of work mobility. If grid power is considered, 80 kWh could be charged in a working day, which could be injected in one or more cars, depending on the station construction. Moreover, a study has been done about the integration of a similar converter in the Netherlands [8], where it is stated that the PV array can be 30% over sized compared to the converter, resulting in only 3.2% energy loss throughout the year, providing even more flexibility to the solar parking slot.

Therefore, the 10 kW power rating of the converter makes it suitable for households, because of the low power contracted by the user, and for industrial parking slots, where a long charging process is accepted. Moreover, fast chargers can be built by paralleling several units of the power converter.

The next sections resume the required specifications of each port of the converter. Some attributes apply for the whole converter and need to be considered in all the converter designs:

- High efficiency
- Minimum volume and weight
- Low number of elements
- Meets all the requirements established by the different standards
- Printed Circuit Board (PCB) mountable elements, to reduce manufacturing cost
- Simplicity

In order to achieve this requirements, Silicon Carbide (SiC) power semiconductors are used because of the low conduction and switching losses. This allows for a higher switching frequency and the corresponding reduction of the size of the elements which form the different topologies. They have been chosen as it is the preferred semiconductor for high power and high frequencies in high efficiency converters. However, SiC devices increase the PCB design complexity due to high $\frac{dV}{dt}$ in the hard switching converters, which cause ringing and EMI problems. This is a major problem when designing the final converter, but considering the purpose of this thesis, PCB design is out of the scope of this project.

2.1.1. PV port

The port which connects to the photovoltaic array needs to have the following characteristics.

- 350 V - 700 V 30 A input
- 10 kW max input
- Maximum Power Point Tracking (MPPT)
- Low input ripple
- Input current ripple peak to peak <5%
- Input voltage ripple peak to peak <0.25%
- Unidirectional

EU standards for grid connected inverters do not require galvanic isolation between the PV panels array and the grid. Standard IEC 61727, which specifies the main requirements of the grid interface and will be reviewed in the Grid port section on the next page, does not specify that any type of electrical isolation is required. Thus, in order to reduce cost, size, weight and complexity of the converter a transformerless solution for this port is adopted. However, leakage currents arise because of the parasitic capacitance of the panels to ground, which create safety problems in the system. This phenomena is more related to the inverter and therefore is treated later on the Grid port section.

The implementation of a Maximum Power Point Tracking (MPPT) algorithm for the PV port results in more power extracted from the PV panels, which might be significant amount of energy in a 10 kW converter. Several MPPT algorithms have been proposed, reviewed and compared in literature [9]. Nowadays most of the commercial inverters have MPPT integrated, and high power inverters have more than one MPPT input in order to maximize power output. Those systems have demonstrated to be specially interesting in northern countries, where temperature and irradiance vary considerably during the day and thus the V_{MPP} fluctuates constantly. This is the reason why it must be implemented in the multiport converter.

Due to the use of switching devices in the converter, a current ripple appears in the photovoltaic panels. This ripple has been demonstrated to cause power loss [10], thereby, a low current ripple is desired. Moreover, most MPPT methods rely on input current measurements, and having a high ripple reduces the efficiency of the algorithm. The current ripple will be a design input parameter for the PV port of the converter, so all the solutions will have the same properties in this aspect.

2.1.2. EV port

At the time of writing this report, multiple standards coexist for the charging of EVs, having different levels of power modes. The actual power of the converter makes it reside in the DC Class 1 Mode 4 electric vehicle chargers, which are DC off-board chargers of up to 36 kW rated power. The port which connects to the electric vehicle needs to have the following characteristics:

- 200 V - 500 V output
- 10 kW max input/output
- 30 A max current input/output
- Isolated
- Low output ripple
- Bidirectional (Vehicle to Everything (V2X) operation)

This specifications fit inside the electric vehicle charging standards CCS (European/American) and CHAdeMO (Japanese). Therefore, the converter could be adapted to those standards with the proper control and connectors. All DC charging standards for electric vehicles require isolation between the car and the power grid. IEC 61851-23 (2014-03):2014-11 also specifies that it is necessary to monitor the insulation resistance of the secondary circuit [11].

Bidirectionality is desired in order to include V2X operation. As stated in [8], the ability to use car batteries as grid storage makes it possible to increase renewable energy penetration in the grid. Considering that the amount of electric vehicles in the automobile park is going to increase exponentially in the following years, and that energy reserves in the grid are the main enabler for further renewable energy penetration, it is sensible to make this new topology bidirectional in order to be ready for the future.

On the characteristics side, excessive DC current ripple might contribute to battery aging. Valve-Regulated Lead-Acid (VRLA) batteries are considered to be extremely susceptible to ripple current since it can lead to cell heating and will accelerate the degradation of cells which are at risk from thermal runaway. Thus, low ripple when charging or discharging the battery is desired.

2.1.3. Grid port

The aim of the multiport converter is to offer maximum flexibility with maximum efficiency. Thus, a grid connection is desired in order to be able to inject energy produced from the panels which is not stored in the EV battery or to withdraw energy in the case of charging a car and solar production is not enough. This port has the following characteristics:

- 3 phase 400 V mains connection
- 10 kW max input/output
- 16 A maximum current
- Bidirectional

These are the main requirements of the port. A three phase connection is desired in order to spread the power injection/withdrawal between the three phases. Moreover, international standards like the *IEC 61727* also apply, which specifies the main requirements of applications with a grid interface. These standard ensures that the inverter is both functional and safe for PV connections of 10 kVA or less. The main requirements make reference to the output power quality:

- Limit the injection of any DC current into the utility to less than 1%
- Total harmonic current distortion should be less than 5%
- Harmonic current distortion for each individual harmonic also limited

- The inverter must control flicker to be in line with IEC 61000
- When the inverter output is greater than 50%, the power factor must be greater than 0.9

Another important issue is non-islanding: if the grid power is lost then for safety reasons the inverter should stop supplying power, as maintenance work could be being performed in the power lines. Moreover, if the utility voltage or frequency goes out of limits the inverter should stop supplying power. The maximum disconnection times are specified in the standard. Finally, once any grid power is restored, the inverter should not connect for some time. This shut off time is typically between 20 seconds to 5 minutes.

Transformerless topologies are used because of the size reduction and higher efficiency, the most important aspects wanted in the resulting converter. However, in transformerless topologies ground leakage current present a danger for humans. Therefore, the leakage current should be limited below the VDE 0126-01-01 standard of 30 mA [1]. More information about this matter can be found later in Section 2.5 of this chapter.

In this chapter the system architectures that can be used to build the multiport converter are compared in the first section. The second section collects a literature study on the different converter topologies that fit the previous architectures. Only the main advantages and disadvantages of each topology are listed as they are designed carefully in the following chapters of the thesis.

This chapter also includes the weighting factors used to evaluate the converter in several operating points. Lastly, a theoretical explanation of the numerical method used to evaluate the losses in DC-AC converters is explained.

2.2. System architecture

The design of the multiport converter can be based on different architectures, depending on the mode of interconnection of the different ports. The different available topologies can be separated into three main architectures, depending on how the conversion steps take place:

1. DC link based multiport converter
2. Impedance network based multiport converter
3. AC link (High Frequency Transformer) based multiport converter

The first set of them are single conversion topologies that are joined by a common DC link, as shown in Figure 2.2.

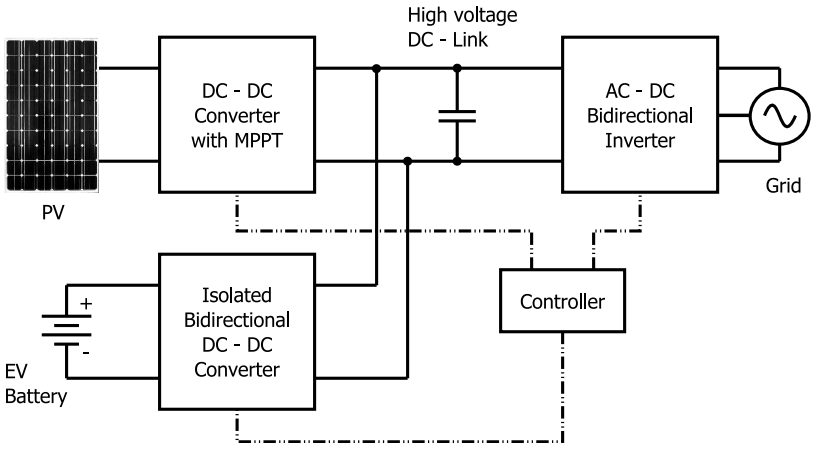


Figure 2.2: Block diagram of a three-port converter with a DC link

As it is seen in Figure 2.2, three different converters are used in order to create a multiport converter which relies in a DC link. This converters have each a different control algorithm, which depends on the topology. Therefore, a central micro-controller with enough computational power is needed, or Field Programmable Gate Arrays (FPGA) have to be used in order to reduce the micro-controller load. The advantages and disadvantages of having a common DC link are listed in Table 2.2.

Table 2.2: List of advantages and disadvantages of the DC link based architecture.

Advantages	**Disadvantages**
Micro grid ready	More components
Easy to implement	Big capacitor in DC link (energy buffer)
Expandable	Three different controls
Simple port based control	
Modularity	

This architecture requires a DC link voltage of at least 750. In order for the inverter to work the DC voltage should be higher than the maximum peak line voltage, which is around 555 V. Moreover, the PV port power conditioning converter is required to boost the voltage, as the input requirements of the PV port specify an input voltage of 350-700 V. Therefore, if very low switching duty cycles want to be avoided, a minimum of 750 V should be selected. Further increasing the voltage is not required and it reduces the efficiency of the system, increasing the voltage ripple of the inverter with respect to grid and reducing the efficiency.

The second available architecture for the implementation of the three port converter only uses two converters, relying on a main topology that has the ability to control both the input and the output, as displayed in Figure 2.3.

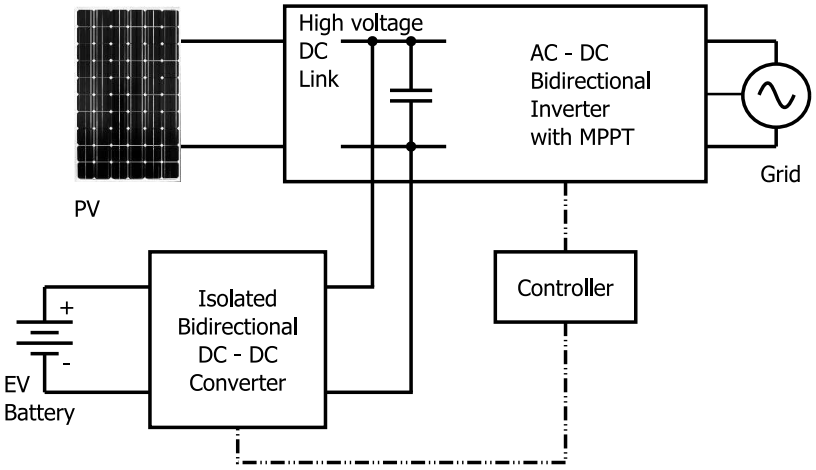


Figure 2.3: Block diagram of a three-port converter with an impedance network

This converter has a DC Link which is inherent to the converter, and can be used in order to connect a third converter for the EV charging. Z-Source Inverter (ZSI) and quasi Z-Source Inverter (qZSI) are the two topologies that fit in this group. This converters rely on an impedance network at the input which is able to boost the voltage input when short-circuiting the output legs of the converter. In this converter topologies, the control of the inverter can modify both the input and the output. The main advantage is that the amount of control in the multiport solution can be reduced, with the problem

of an increased complexity.

Table 2.3: List of advantages and disadvantages of the Impedance Network based architecture.

Advantages	Disadvantages
Reduced active components	High currents in impedance network
Increased reliability	Increased control complexity
Two different controls	Not easily expandable
No dead-time necessary	High currents in three phase bridge
	Variable DC link voltage

The last architecture consists in using a common AC link [12]. A topology like this would isolate the three ports of the converters, relying on a central High Frequency Transformer (HFT) which exchanges energy between the ports and provides the isolation, see Figure 2.4.

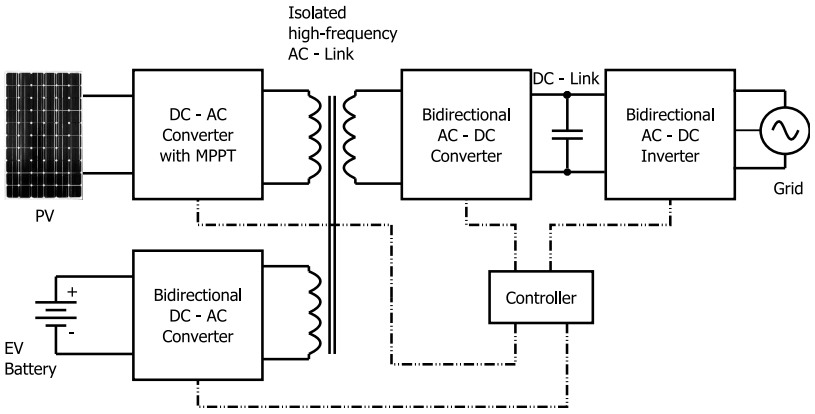


Figure 2.4: Block diagram of a three-port converter with an inner AC link.

Table 2.4: List of advantages and disadvantages of the AC link based architecture.

Advantages	Disadvantages
Isolation between all ports	High complexity
	HFT with three windings
	Difficult to control
	Little research on it
	Non modular
	Non expandable
	DC Link still necessary

Table 2.4 shows how the disadvantages of this type of converter outnumbers the advantages. There is also the possibility of using a matrix converter [13] instead of a rectifier and an inverter in the grid port, but this kind of converters are highly complex and require very precise control. Moreover, isolation between photovoltaic panels and the grid is not strictly required by the European standards.

With this considerations, it is clear that a topology like this increases both the development and manufacturing complexity without any real advantage; therefore, no topologies of this kind are considered in this work. The topology comparison chapters focus on both the DC link based topologies and the Impedance Network based topologies.

2.3. Candidate topologies

The different topology candidates that fit inside each of the previously explained multiport converter architectures are listed in this section, in order to get an overview of the different compared topologies.

2.3.1. DC link - PV port candidates

This section purpose is to make a review of the available topologies that can perform the PV power conditioning of the multiport converter relying on a DC link. There are many topology options which can be used for energy harvesting from PV panels [14] [15]. However, not all of them are equally suitable for the purpose, because of the inherent working principles. Buck topologies, used to step down the DC voltage, are usually more efficient than boost topologies due to the fact that there is lower necessity of energy storage in the inductors. The problem of this topologies is that they have a discontinuous input current, affecting the PV panels. Moreover, the MPPT efficiency when working with buck topologies is also reduced considerably [16], as the current is not constant.

In order to reduce voltage ripple in the solar panels and enhance the MPPT efficiency, a capacitor in parallel with the PV array is used. This used capacitors are film capacitors, which are more reliable than electrolytic capacitors at the cost of being bulkier. This capacitor is shown in the following topologies, because even though the input current ripple is a fixed requirement, the frequency of this ripple is different for each topology and thereby the necessary capacitance varies.

The output capacitors shown in the different topologies are there in order to filter the ripple current and achieve an almost constant voltage in the DC link. The DC link capacitors are not shown because the size is not considered; the necessary capacitance not only depends on the ripple but also on the necessary energy storage when transients occur and the different control systems need to adapt to the new situation. Thus, the necessary capacitance is preferably bigger than just considering ripple currents and are not considered as a part of the topology. The sizing of this capacitance is out of the scope of this thesis as it mainly depends on the control strategies and the frequency. A faster control loop or a higher frequency makes it possible for the converter to react further to power jumps, resulting in a lower capacitance needed.

The candidates for the PV port are:

1. Boost Converter
2. Interleaved Boost Converter (IBC)
3. Coupled Inductors Interleaved Boost Converter (CIIBC)
4. Three Level Boost Converter (3LBC)

1. Boost Converter

The boost converter [17] is the basic topology to step up voltage. It is composed of an inductor, a switch and a diode, as seen in Figure 2.5. The input and output filter capacitors are also shown.

This topology is listed for the sake of completeness. However, it is not suitable for high power applications, and thereby it is not modeled on its own. The main advantages and disadvantages are summarized in the Table 2.5.

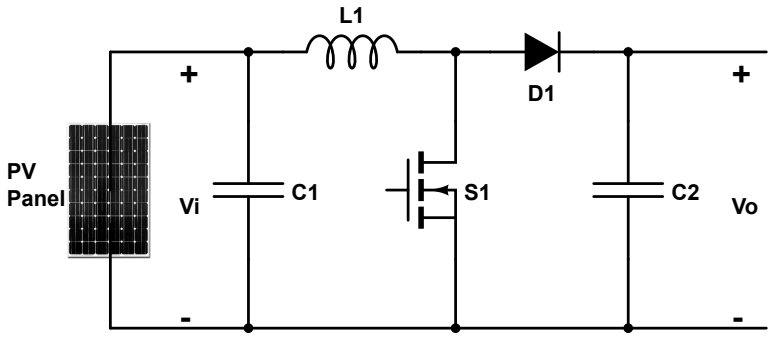


Figure 2.5: Structure of a boost converter

Table 2.5: List of advantages and disadvantages of the Boost Converter.

Advantages	Disadvantages
Basic topology	High input current ripple
Low component count	Non-suitable for high power
Easy to control	Big input capacitor
High reliability	High currents at the input
Many snubber circuits possible	

2. Interleaved Boost Converter

In Figure 2.6 it is shown how the Interleaved Boost Converter (IBC) [18] is built, starting from the conventional boost topology and paralleling N number of phases. Therefore, the number of inductors, switches and diodes is equal to N.

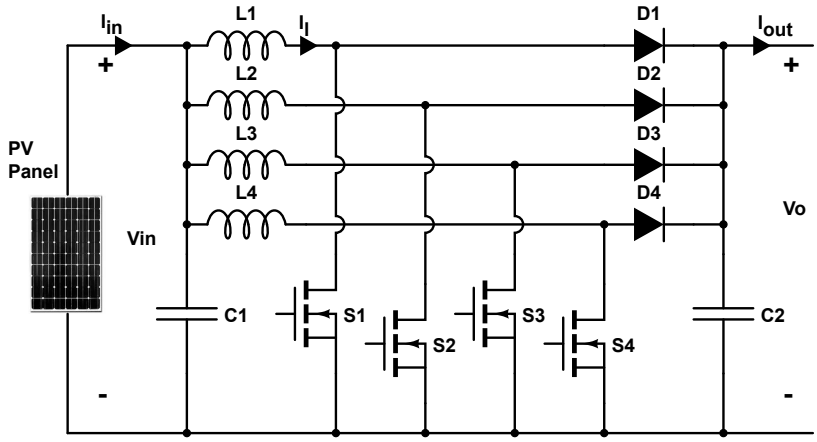


Figure 2.6: Structure of a four phases IBC

The total number of components increases with the number of phases, but the current in each leg is reduced, reducing component ratings and ohmic losses. Another advantage is the input current ripple, which is lower for an equal value of inductance and its equivalent frequency is N times the switching frequency. The main advantages and disadvantages are listed in Table 2.6.

It is clear that efficiency increase by interleaving converters depends on the components used. Therefore, an optimum number of interleaved phases can be found; increasing the number of phases ohmic losses are reduced but switching losses are increased if switching frequency is not changed.

Table 2.6: List of advantages and disadvantages of the IBC.

Advantages	Disadvantages
Lower input ripple	More components
Lower RMS currents	Increase switching losses
Light load efficiency boost	More complex control
Smaller input capacitor	Reduced reliability
Reduced EMI	
Spread energy dissipation	
Higher power by increasing N	

3. Coupled Inductors Interleaved Boost Converter

Interleaving technique increases the number of inductors necessary in the converter, which might result in a bigger volume. This is overcome by employing coupled inductors in the IBC which reduces the converter volume by using one core instead of two or more, at the expense of slightly bigger size. At the same time it improves the regulation of power converters. Figure 2.7 shows how the Coupled Inductors Interleaved Boost Converter (CIIBC) [3] is built, similarly to the IBC, but with the coupled inductors.

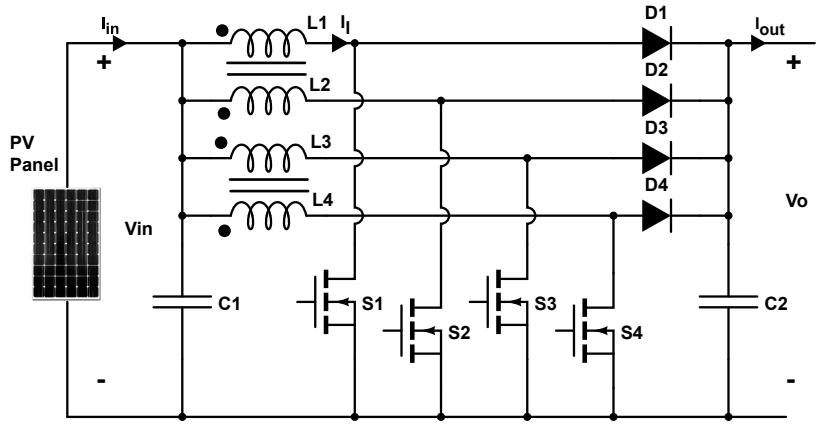


Figure 2.7: Structure of a four phases CIIBC

This inductors can be built using direct coupling or reverse coupling, depending on how the two fluxes of the two windings interact which each other. Direct coupling reduces the input ripple while increasing the inductor current ripple, and reverse coupling does just the opposite. The use of one type or the other is reviewed during the design of the converter. The benefits and disadvantages of using coupled inductors over the standard IBC are summarized in Table 2.7.

Table 2.7: List of advantages and disadvantages of the CIIBC with respect to the IBC.

Advantages	Disadvantages
Less component count than IBC	Increase design complexity
Smaller/Bigger channel inductor current ripple	Increase manufacture complexity
Improve the steady-state efficiency	Core saturation problems

Inductor design complexity increases due to the difficulty of building an inductor with two windings with a certain coupling factor. A thorough design needs to be performed in order to perform a reliable analysis of this topology.

4. Three Level Boost Converter

The Three Level Boost Converter (TLBC) [19] is one of the multilevel converters proposed which is widely used in high frequency DC-DC power conversion. The TLBC has significant advantages compared to conventional boost converters. The size of the inductor is reduced and switch voltage rating is half of the output voltage. This reduces the overall size and improves the efficiency. However, voltage balancing across the DC bus capacitors is required due to non idealities in the components, which is feasible by voltage sensing. This additional number of capacitors might look like a drawback, but in Section 2.5, which deals about leakage currents, it is demonstrated that it is necessary in all topologies. The basic structure of this topology is shown in Figure 2.8.

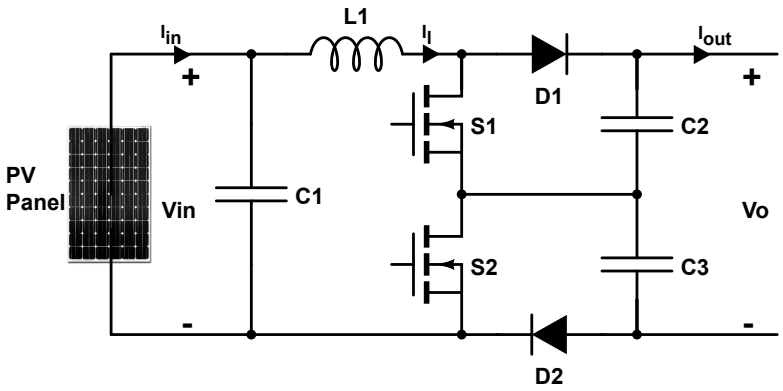


Figure 2.8: Structure of a one phase TLBC

While the number of inductors is kept to one for the non-interleaved version, the number of switches and diodes is doubled with respect to the original boost converter. Interleaving of two or more TLBC is also possible, reducing the current rating in the components. The advantages and disadvantages of the TLBC are summarized in Table 2.8.

Table 2.8: List of advantages and disadvantages of the TLBC.

Advantages	**Disadvantages**
Lower Ripple	Double components
Lower RMS currents	Higher gate drivers complexity
Three level topology	Current goes through two diodes (more losses)
Smaller input capacitor	Control problems at low currents
Half voltage switch rating	

2.3.2. DC link - EV port candidates

Two different DC-DC isolated power converters have been considered as candidates for the EV port:

1. Dual Active Bridge (DAB)
2. Interleaved Bidirectional Flyback Converter (IBFC)

Other DC-DC isolated converters could be considered for the EV port, as the Dual Active Half-Bridge (DAHB) [20]. This topology employs single legs at both sides of the High Frequency Link, reducing the number of semiconductors at the expense of bigger circulating currents in the High Frequency Link. However, this can be considered a variation of the Dual Active Bridge (DAB) and therefore it will not be considered. There are other topologies but most of them can be considered variations of the DAB topology. Therefore, only this two topologies are considered in this work.

1. Dual Active Bridge

The DAB [21] consists of two full bridges connected via a High Frequency Transformer (HFT). A total of eight switches are necessary, together with the transformer and an external inductance, which is needed in the case the transformer's leakage inductance is not enough.

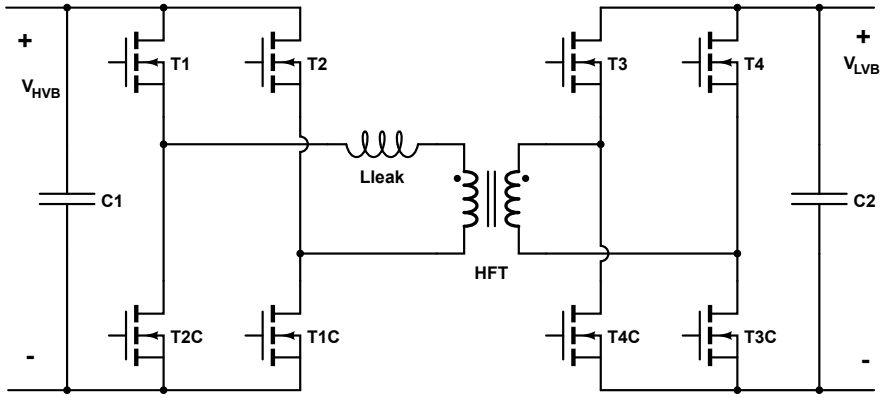


Figure 2.9: Structure of the DAB

The DAB has inherent isolation and bidirectionality. Moreover, Zero Voltage Switching (ZVS) is possible without modifications in the High Frequency Link (HFL). The advantages and disadvantages of this topology are mentioned in Table 2.9.

Table 2.9: List of advantages and disadvantages of the DAB.

Advantages	**Disadvantages**
Acts as ideal current source	High current ripple
Inherent soft switching	Large number of switches
Control easy to implement	
No diodes necessary	
Many improvement possibilities	

2. Interleaved Bidirectional Flyback Converter

The Flyback is a low power DC-DC isolated topology, see Figure 2.10. It uses a Flyback a transformer, which is actually a coupled inductor as it stores energy in the air gap. When the primary switch is turned on, the diode at the secondary is reverse biased and the current at the primary increases, charging the inductor. Once the switch is turned off, the secondary diode is forward biased and the inductor is discharged through the secondary winding. This topology is not suitable for the desired application as it is not bidirectional, it is low power rated and would imply high voltage stresses in the semiconductors.

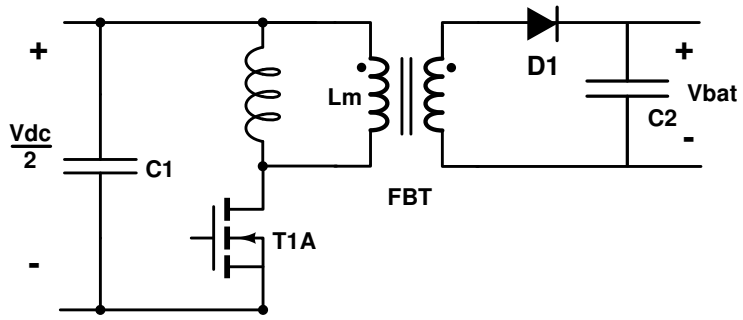


Figure 2.10: Structure of the Flyback converter.

The Interleaved Bidirectional Flyback Converter (IBFC) [22] consists of two or more typical flyback converters in parallel, where the secondary diode has been replaced by a switch in order to add bidirectionality. The topology shown in Figure 2.11 has a split primary winding in order to reduce the voltage stress at the switches of the primary side. The advantages and disadvantages of this topology are listed in Table 2.10.

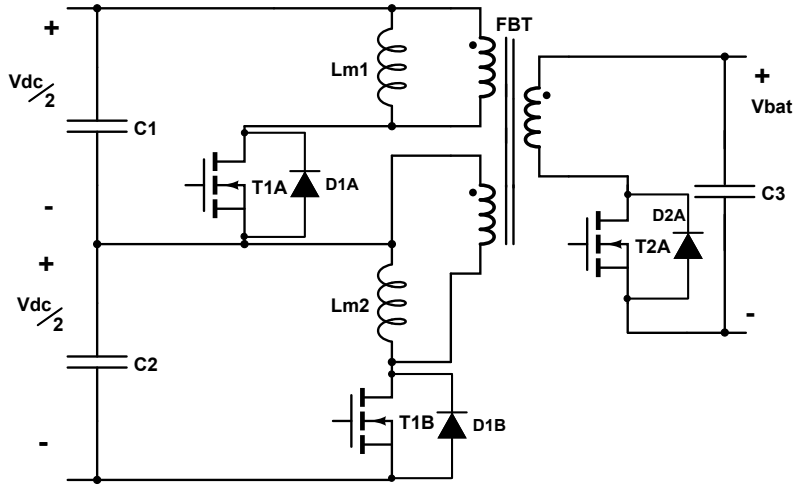


Figure 2.11: Structure of the IBFC

Table 2.10: List of advantages and disadvantages of the IBFC.

Advantages	Disadvantages
Reduced number of semiconductors	One quadrant Flyback Transformer (FBT) utilization
Low ripple if interleaved	FBT must be carefully designed
Soft switching possible	Tipically a low power topology
	High voltage stresses

2.3.3. DC link - Grid port candidates

The candidates for the Grid port are the most used two level and three level topologies and an alternative three level topology:

1. 2 Level Converter (2LC)
2. Three Level Neutral Point Clamped Converter (3LNPC²)
3. Three Level T-Type Converter (3LT²C)

1. 2 Level Converter

The Two Level Converter (2LC) or Voltage Source Inverter (VSI) [23] is the simplest version of a three phase inverter. It consists of six switches with the corresponding freewheeling diodes in anti parallel, as shown in Figure 2.12.

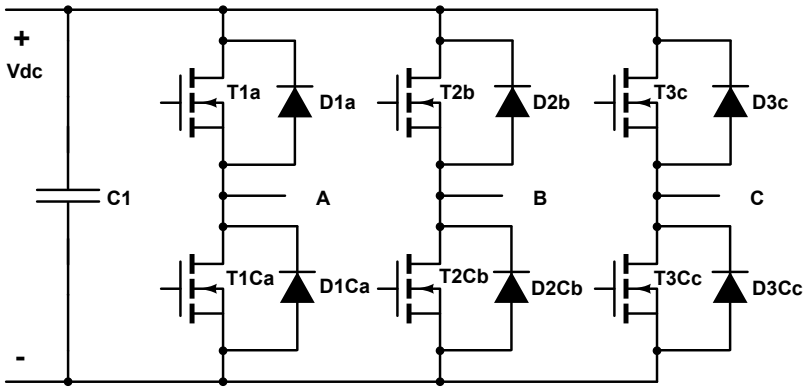


Figure 2.12: Structure of the 2LC

A B and C in Figure 2.12 are the three phase connectors of the converter, where the output filter is connected. The chosen filter topology is LCL, which is formed by two inductors and one capacitor, and is reviewed later in the design chapter of the report. The filter is not displayed in the DC-AC topology figures because it has the same structure in all inverter topologies. The input of the converter is the DC link which consists of two capacitor which split the voltage; the reason of this is found later in the report, see Section 2.5. The advantages and disadvantages of this topology are listed in Table 2.11.

Table 2.11: List of advantages and disadvantages of the 2LC.

Advantages	**Disadvantages**
Low number of components	High THD
Most used topology	High semiconductor rating
Easy to implement modulation techniques	High switching losses

2. Three Level Neutral Point Clamped Converter

The Three Level Neutral Point Clamped Converter (3LNPC²) [24] is the most used three level topology, where the neutral point clamping is achieved with diodes connected to the neutral point, see Figure 2.13.

This topology adds complexity to the system but might be advantageous at high DC link voltages and switching frequencies. The voltage of the switches is halved compared to the 2LC, reducing the switching losses. On the other hand, the LCL filter requirements are lower due to lower output voltage ripple. The advantages and disadvantages of this topology are listed on Table 2.12.

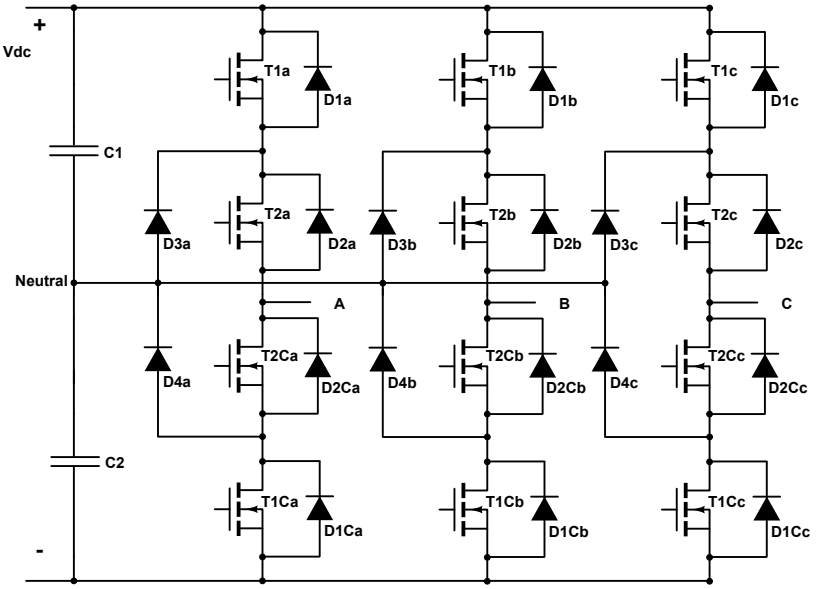


Figure 2.13: Structure of the 3LNPC²

Table 2.12: List of advantages and disadvantages of the 3LNPC².

Advantages	Disadvantages
Low output THD	High component count
Higher efficiency	Increased control complexity
Low output ripple	
Losses are spread between more components	

3. Three Level T-Type Converter

The Three Level T-Type Converter (3LT²C) [25] is also a three level topology, but instead of clamping the neutral point with diodes two mosfets are used. It is similar to the 3LNPC², with lower conduction losses in the main switches but higher switching losses as the whole voltage is found across the switches, see Figure 2.14.

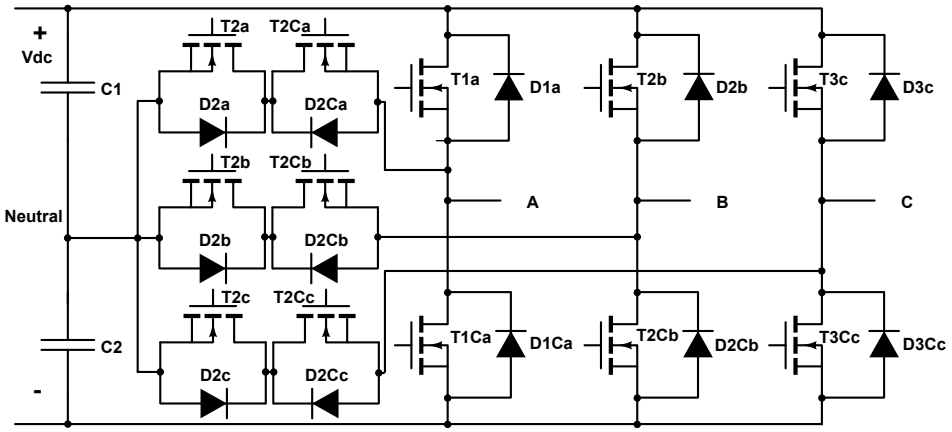


Figure 2.14: Structure of the 3LT²C

The advantages and disadvantages of this topology are listed on Table 2.13

Table 2.13: List of advantages and disadvantages of the 3LT²C.

Advantages	Disadvantages
Low output THD	High component count
Better losses distribution	Increased control complexity
Low output ripple	Higher switching losses
Higher efficiency	

2.3.4. Impedance Network based candidates

Two topologies fit inside this group, being the second one a modification of the first:

1. Z-Source Inverter + EV Port Candidate (ZSI)
2. Quasi Z-Source Inverter + EV Port Candidate (qZSI)

1. Z-Source Inverter + EV Port Candidate

The Z-Source Inverter (ZSI) [26] is a topology which functions as a buck-boost inverter without making use of DC-DC converter bridge due to its unique circuit topology, see Figure 2.15. It is based on the conventional 2LC with an attached impedance network that consists of two inductors, two capacitors and one diode. The impedance network is used to boost the voltage when short circuiting any of the legs of the three phase bridge, while the buck functionality is achieved in the same way as the conventional 2LC.

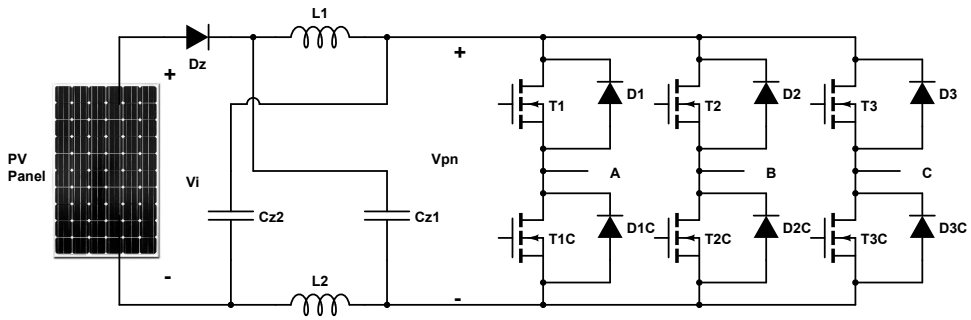


Figure 2.15: Structure of the ZSI.

In this topology one of the EV port converters would be connected across the impedance network capacitors, which have a constant voltage in steady state. This converter presents a major drawback: the input current at the PV port is not continuous. Therefore, it is not suitable for using it as the base of the multiport converter.

2. Quasi Z-Source Inverter + EV Port Candidate

The quasi Z-Source Inverter (qZSI) [27] is a topology derived from the traditional Z-source inverter (ZSI). The qZSI inherits all the advantages of the ZSI, which can realize buck/boost, inversion and power conditioning in a single stage with improved reliability. In addition, the proposed qZSI has the unique advantages of lower component ratings and constant DC current from the source. All of the boost control methods that have been developed for the ZSI can be used by the qZSI.

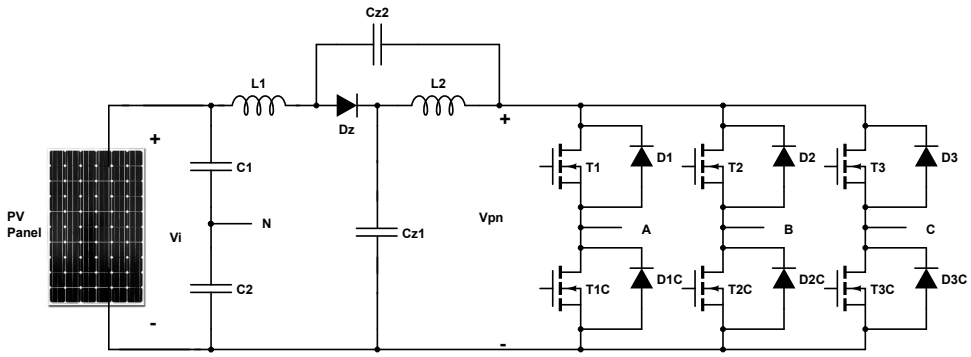


Figure 2.16: Structure of the qZSI.

The qZSI features a wide range of voltage gain which is suitable for applications in photovoltaic (PV) systems. Moreover, the voltages across the capacitors are constant, making the topology suitable for adding another converter, the EV port candidate. The advantages and disadvantages of this topology are listed on Table 2.14.

Table 2.14: List of advantages and disadvantages of the qZSI.

Advantages	**Disadvantages**
Low number of switches	High currents in Z network
3 legs control DC input	Increased control complexity
Buck and Boost	Non modular and expandable
Low Ripple	
Increased reliability	
No dead-time required	

2.4. Comparison framework

A framework is created in order to rate the different candidates and make the comparison well-founded. The framework has been adapted from Todorčević's work [28], where multiple converters are rated considering different criteria in order to obtain the optimal topology.

In the following sections all comparison criteria is given a weight factor and explained in terms of importance. The comparison is done in such way that each criterion carries its own weight factor W_j. The topologies are rated from one (worst) to five (best) for each criterion and then the rating r_{ij} is multiplied with the weight factor of the particular criterion. The sum of all these multiplications per topology results in a total rating $T_{rating,i}$ of a certain converter, given by Equation 2.1.

$$T_{rating,i} = \sum_{j=1}^{N_{cri}} W_j r_{ij} \tag{2.1}$$

Where i is an ordinal number which refers to the topology, j is an ordinal number referred to the criterion and N_{cri} the total number of criteria. The converter with the highest rating is the best suited for the given requirements and application.

2.4.1. Number of switches

The number of switches is one of the most important criterion because a bigger number of active components increases the complexity of the system, the cost and reduces the reliability. However, the number of switches used for the different topologies is usually low, thus a weight of 3 is applied.

Table 2.15: Number of switches n $[j = 1, W_1 = 3]$.

Rating	1	2	3	4	5
Number of switches PV	$n \geq 6$	$n=5$	$n=4$	$n=3$	$n \leq 2$
Number of switches Grid	$n>15$	$12<n \leq 15$	$9<n \leq 12$	$6<n \leq 9$	$n \leq 6$
Number of switches EV	$n>18$	$14<n \leq 18$	$10<n \leq 14$	$6<n \leq 10$	$n \leq 6$

2.4.2. Number of diodes

The number of diodes has to be taken into account because the cost of the converter also increases. However, the importance of the number is not as high to the number of switches, as they are non controlled elements and therefore the complexity they add to the system is lower.

Table 2.16: Number of diodes n $[j = 2, W_2 = 1]$.

Rating	1	2	3	4	5
Number of diodes PV	$n \geq 6$	$n=5$	$n=4$	$n=3$	$n \leq 2$
Number of diodes Grid	$n>15$	$12<n \leq 15$	$9<n \leq 12$	$6<n \leq 9$	$n \leq 6$
Number of diodes EV	$n>12$	$8<n \leq 12$	$4<n \leq 8$	$0<n \leq 4$	$n=0$

2.4.3. Number of magnetic elements

The size of the magnetic elements, which includes power inductors and transformers is evaluated in terms of quantity, as E65 size core restriction is imposed. The higher the number of necessary cores, more the manufacturing complexity increases. A rating of three has been selected for the number of cores, see Table 2.17.

Table 2.17: Number of cores n $[j = 3, W_3 = 3]$.

Rating	1	2	3	4	5
Number of cores PV	$n \geq 6$	$n=5$	$n=4$	$n=3$	$n \leq 2$
Number of cores EV	$n \geq 8$	$6<n \leq 8$	$4<n \leq 6$	$2<n \leq 4$	$n \leq 2$

The number of cores of the grid port is not be evaluated, as the same filter topology is used for all topologies. The total size of inductors will be evaluated together with the volume of the cooling system and capacitors later on.

2.4.4. Number of capacitors

The different topologies require a different number of capacitors depending on the ripple current and the equivalent frequency of the current. Therefore, it is necessary to evaluate the number of film capacitors for each topology. A weight of one has been chosen because the design parameters limit their amount and most topologies result in similar numbers. Moreover, film capacitors have low loses, which results in lower heating and extended lifetime.

Table 2.18: Number of capacitors n $[j = 5, W_5 = 1]$.

Rating	1	2	3	4	5
Number of capacitors PV	$n \geq 6$	n=5	n=4	n=3	$n \leq 2$
Number of capacitors EV	$n \geq 6$	n=5	n=4	n=3	$n \leq 2$
Number of capacitors Grid	$n \geq 6$	n=5	n=4	n=3	$n \leq 2$

2.4.5. Efficiency

Converter efficiency is the most important criterion, so it carries a weight of 5. Additionally, the cooling effort is related to the total losses. A converter with high losses probably needs an expensive water cooling system, whereas a high efficiency converter can be cooled passively with a simple heat sink or with additional fans. The losses occurring in the specific semiconductor devices are an important design criterion as they define, together with the thermal model, the resulting device junction temperatures. The lifetime of the devices is influenced directly by the maximum junction temperature and also by the temperature cycles, as cyclic mechanical stress is related to the thermal cycling. Additionally, a specific maximum junction temperature should not be exceeded as immediate thermal failure of the semiconductor device is the consequence of overheating.

This parameter depends on the converter purpose, thereby different criterion apply for each port.

Table 2.19: Efficiency η[%] $[j = 6, W_6 = 5]$.

Rating	1	2	3	4	5
Efficiency PV	η<98.0	98.0 ≤η<98.5	98.5 ≤η<99.0	99.0 ≤η<99.5	η≥99.5
Efficiency Grid	η<97.5	97.5 ≤η<98.0	98.0 ≤η<98.5	98.5 ≤η<99	η≥99.0
Efficiency EV	η<97.0	97.0 ≤η<97.5	97.5 ≤η<98.0	98.0 ≤η<98.5	η≥98.5

Considering that the efficiency of the converters depend on the operating point, weighted efficiencies will be used for the comparison. The equations used in order to calculate the weighted efficiency are found in Section 3.2 later on the report.

2.4.6. Volume of the converter

As previously explained, the size of the heat sink is directly related to the efficiency of the converter. It is the element that most affects the final volume of the converter, together with the electromagnetic parts and the capacitors. They are all taken into account in order to evaluate the total volume of the converter.

Table 2.20: Converter size V_c [dm^3] [$j = 7, W_7 = 5$].

Rating	1	2	3	4	5
Volume PV	V_c>0.6	0.5≤ V_c<0.6	0.4≤ V_c<0.5	0.3≤ V_c<0.4	V_c<0.3
Volume Grd	V_c>0.9	0.75≤ V_c<0.9	0.6≤ V_c<0.75	0.45≤ V_c<0.6	V_c<0.45
Volume EV	V_c>1.5	1.3≤ V_c<1.5	1.1≤ V_c<1.3	0.9≤ V_c<1.1	V_c<0.9

2.4.7. Leakage currents

Leakage currents are an important aspect which concerns grid-tied photovoltaic installations. It is throughly discussed in Section 2.5. The rating of the converter is selected depending on the fulfillment or not of the *DIN VDE 126-1-1* standard, where a maximum leakage requirement of 30 mA current is established, otherwise the converter has to disconnect from the grid [29]. This coefficients only apply for the grid port of the converter, see Table 2.21.

Table 2.21: Leakage currents [$j = 8, W_8 = 2$].

Rating	1	2	3	4	5
Leakage	High	Outside Limits	Inside limits	Minor	None

2.4.8. Current ripple in EV battery

Due to the compulsory use of isolated topologies, EV charging usually has high current ripples at the DC output. The amplitude of this ripple must be limited in order to improve battery life of the cars [30]. This coefficients only apply for the EV port of the converter.

Table 2.22: Current ripple $I_{rip,pp}$ [A][$j = 9, W_9 = 4$].

Rating	1	2	3	4	5
Current ripple	$I_{rip,pp}$ >50	40<$I_{rip,pp}$ ≤50	30<$I_{rip,pp}$ ≤40	20<$I_{rip,pp}$ ≤30	0<$I_{rip,pp}$ ≤20

2.4.9. Efficiency improvement

Research on the possibilities of increasing the efficiency of each converter is performed by considering the implementation of the following techniques:

- Soft switching
- Other modulation techniques
- Snubbers
- Extra circuitry
- Others

The rating for this parameter depends on how difficult it is to implement the efficiency improvement in the converter, and the efficiency increase due to its implementation, see Table 2.23.

Table 2.23: Efficiency improvement [$j = 10, W_{10} = 1$].

Rating	1	2	3	4	5
Efficiency improvement	futile	hard to implement	doable	minor problems	easy

2.4.10. Controllability

Controllability addresses the control complexity of a given topology, as well as how hard is it to realize proper operation of the converter. It carries a weight of three and the ratings are presented in Table 2.24. Unknown controllability means that the converter is completely new. Solvable means that it is possible to apply certain control methods, but it has not fully tested yet. A hard control method is known but difficult, complex and CPU intensive. A control with minor problems appoints small problems, while easy means that many control methods are known and tested, which are simple to implement.

Table 2.24: Controllability [$j = 11, W_{11} = 3$].

Rating	1	2	3	4	5
Controllability	unknown	solvable	hard	minor problems	easy

2.5. Leakage currents in transformerless topologies

A transformerless topology, which has been selected as a requirement of the designed converter, lacks galvanic isolation between the PV array and the grid. As a consequence, the PV panels are directly connected to the grid, creating a direct path for the leakage ground currents caused by the fluctuations of the potential between the PV array and the ground. These fluctuations charge and discharge the parasitic capacitance formed between the PV cells and grounded frame, which depend on the PV panels, the voltage, the temperature, the humidity and other external factors. The calculation of the capacitance value is therefore complicated. Some authors have performed experimental tests [31], and obtained an equivalent capacitance of around $220\mu F$. Leakage currents decrease the lifetime of the solar panels, and [32] discusses the electrical hazards of photovoltaic installations, where current leakages also play small role. When touching the surface of the panels, a ground current could flow through the human body and if the current is above certain levels it could lead to a shock resulting in personal injury. Several recommendations are found in literature, in order to minimize the leakage current:

- Topologies that isolate the PV array either partially (semiconductors) or completely (High Frequency Transformer)
- Modified modulation strategies, which reduce voltage fluctuations between PV array and ground.
- Isolation of the inverter with a low frequency transformer

The current leakage is due to the variation in the Common Mode Voltage (CMV) produced at the output of the converter. The path of the leakage current I_L is detailed in Figure 2.17.

In a balanced grid, the CMV is equal to zero, whereas in a power converter the switching state determines the CMV. The CMV can be derived based on the power converter voltages for a balanced grid [33]:

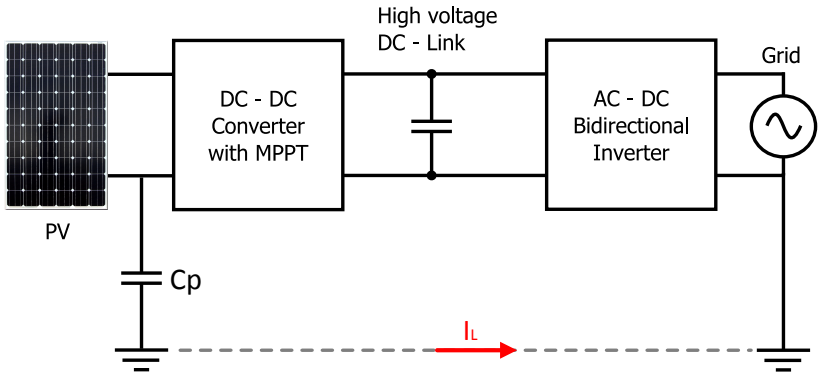


Figure 2.17: Leakage current due to parasitic capacitance in PV systems.

$$V_{CM} = u_{PV} = \frac{V_a + V_b + V_c}{3} \tag{2.2}$$

Where V_a, V_b and V_c are the grid voltages. The leakage currents depend on the voltage applied through the parasitic capacitance to ground. If the CMV was constant, no current leakage would be present. However, as the switching states varies with time, the leakage current is found as:

$$i_L(t) = -C_{PV}\frac{du_{PV}}{dt} \tag{2.3}$$

Where i_L is the leakage current, C_{PV} the capacitance of the PV panels to ground and u_{PV} the voltage of the solar array respect to the ground.

Many research has been performed about leakage currents, concerning single phase and three phase topologies. Some of them focus on the topology while others change the modulation technique in order to achieve a lower variation of the CMV. The most interesting approaches are:

- **Middle point to neutral connection [33].** The article compares three inverter topologies (2LC, 2LC split capacitor with neutral connected, 3LNPC² with neutral connected) and analyzes leakage currents. Concludes that the connection of middle point of the DC link to the neutral line is advisable, and the results show how the leakage current is kept just under limits. If this is performed then the relative voltages of the DC link and the PV array do not fluctuate because the middle point is clamped to the neutral line, which should be zero volts in a balanced grid. However, the effectiveness of the method relies on the fact that the neutral line inductance is low.
- **H7 topology [34].** A new topology based on a 2LC with an added switch to implement galvanic isolation when zero vector is used (derived from the H5 topology for one phase systems). The method shows an easy way to implement the necessary modulation technique (modified Discontinous Pulse-Width Modulation (DPWM)) . However, reduction of the CMV is not too high and both the switching losses and conduction losses increase.
- **4 Leg inverter [35].** The topology presented is based on a 2LC with a fourth leg in order to reduce the CMV variation, where the neutral line is connected. The Total Harmonic Distortion (THD) increases considerably, because of the varying modulation which is unipolar. The fact that two more switches are used is also a handicap.
- **Modulation techniques for two level converters [36].** The article presents a modulation technique which reduces the CMV, the Near State Pulse-Width Modulation (NSPWM). Compared to Space Vector Pulse-Width Modulation (SVPWM), this method does not use the zero vectors, and instead the nearest voltage vectors are used.

- **Modulation techniques for three level converters [37].** This method reduces the use of small vectors, which make for a high amount of variation of the CMV. Another modulation method is applied when capacitors are unbalanced. The method results in a higher THD, but in a three level converter, which is already lower.
- **Other modulation techniques for three level inverters [31].** The article presents two different methods which limit the used vectors in a different way, in order to have a constant or low variation of CMV. 3 Medium Vectors Pulse-Width Modulation (3MVPWM) only makes use of the medium vectors, whereas 2 Medium 1 Zero Vectors Pulse-Width Modulation (2M1ZVPWM) uses two medium vectors and one zero vector.

The easiest solution is therefore the connection of the middle point of the capacitors to the neutral point of the grid. However, as explained in [33], this solution may not satisfy the maximum leakage current requirements because it is dependent on the neutral line inductance. In order to take into account all the options, the converters for the grid port are modeled in the standard modulation techniques and one of the alternative ones explained previously. Therefore, the leakage current rating is different for each modulation technique, depending on its efficiency in terms of CMV variation reduction.

2.6. Conclusion

In this chapter the different architectures that can be used to build the multiport converter have been listed and analyzed. From the three possible architectures, the AC link based multiport converter has been discarded because of the high complexity and high number of components. The DC link based architecture and the Impedance Network based architecture have been found to be possible starting points and will be considered throughout the report.

The different candidate topologies that fit in each architecture have been listed in the second part of the chapter, with the advantages and disadvantages of each one. This topologies are carefully reviewed on Chapter 5, 6, 7 and 8, which contain each port of the DC link based architecture and the impedance based multiport converter respectively.

The framework which is used for the comparison of the topologies, which considers the most important aspects of a power converter and rates them, has also been presented. Finally, a short description of leakage currents and their effect in photovoltaic installations connected to the grid has been performed in order to adapt the multiport converter to the current standards.

3

Loss Modeling and Efficiency

In this chapter the loss model used for the evaluation of all the topologies is presented, together with the analytical equations used and an explanation of how the data is extracted from the manufacturer's datasheet. This is presented prior to the design of the magnetic elements and the selection of the components because how the losses are modeled is crucial for loss optimized designs, and the presented equation are required in the next chapter. Section 3.2 explains how the final efficiency is calculated for every port of the converter. Many different operating points that yield different efficiencies can be taken into account; therefore a weighted efficiency is calculated from the most relevant operating points. In the last section of this chapter, the loss calculation approach for the inverter/rectifier port is explained. In this case the steady state current waveform is sinusoidal and has a low frequency; therefore, the calculation method differs from the more simple piece-wise linear waveforms of the other ports.

3.1. Loss modeling and estimation

Loss estimation accuracy is crucial in order to have a representative model of how a topology performs. Therefore, the dissipated power of every passive and active component of each converter must be known in every possible or representative operating point of the converter, in order to obtain the efficiency and choose the size of the cooling system. The different equations used for this purpose are reviewed in this section, together with the approximations and simplifications performed.

In active components the losses depend on the junction temperature, which is not know in the first iteration. Therefore, an estimation has to be made in order to obtain the losses. The junction temperatures of the converter semiconductors has been considered to be proportional to the power. When maximum current flows through the components, the junction temperature is considered to be 100 °C, whereas when the current is minimum, the temperature is considered to be the ambient one, set at 45°C. Afterwards, an iteration method is used in order to find the correct temperature, which is later explained on Section 4.9 because junction temperatures are strongly dependent on the heat sink design.

3.1.1. Switch losses

The losses in the most important active component of any power converter consist of conduction losses, when the switch is conducting, switching losses, when a transition between the on and off state takes place, and gate losses, which depend on the gate charge and the driving circuit efficiency.

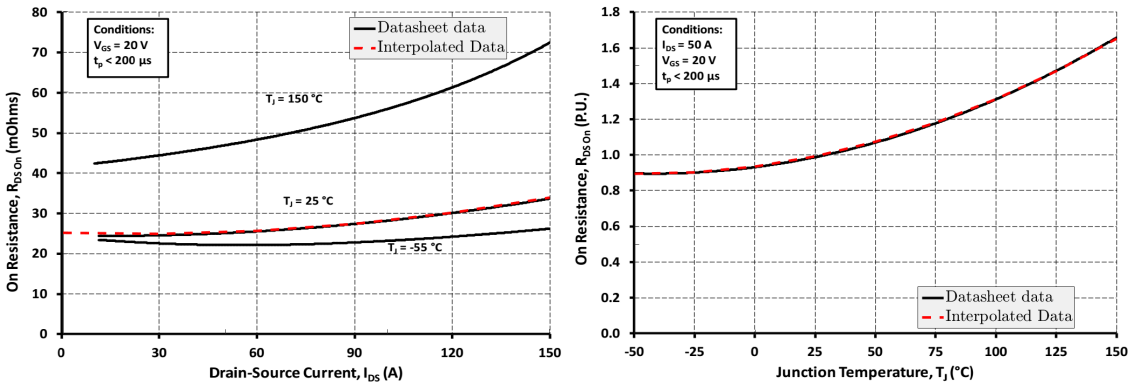
Conduction losses

The switch conduction losses $P_{sw,con}$ on a SiC Mosfet depend on the series resistance of the switch and the current flowing through it. Contrary to Insulated Gate Bipolar Transistor (IGBT), SiC Mosfets do not have an on-state zero-current collector-emitter voltage. Therefore [17]:

$$P_{sw,con} = I_{DS,rms}^2 R_{DS}(I_{DS}, T_j, V_{GS}) \tag{3.1}$$

Where $I_{DS,rms}$ is the RMS value of the current through the SiC Mosfet and R_{DS} is the drain-source on-state resistance. The latter depends on the drain-source current I_{DS}, the junction temperature T_j and the voltage applied at the gate V_{GS}. The higher the gate voltage, the wider the conduction channel of the semiconductor and the lower the series resistance. Considering the comparison purpose of this work, the applied V_{GS} has been fixed to the optimum suggested by the manufacturer in the datasheet. Therefore, this parameter is not included as a variable in the loss modeling.

The R_{DS} value is obtained in every working operating point by using curve fitting from the Mosfet datasheet. It is possible to obtain a second order polynomial for the series resistance dependence on the temperature and on the junction temperature, as seen in Figure 3.1. The two plots show that a high accuracy can be obtained by using this method, allowing for easy calculation of the parameter by knowing the drain-source current I_{DS} (Figure 3.1(a)) and the junction temperature T_j (Figure 3.1(b)).



(a) R_{DS} versus I_{DS}

(b) Normalized R_{DS} versus T_j

Figure 3.1: Example of an interpolation, superimposed to the datasheet (CREE C2M0025120D).

Switching losses

Switching losses are a result of the presence of voltage and current at the same time in the mosfet during switching transitions. The datasheets from the manufacturer provide both the turn on energy E_{on} and the turn off energy E_{off}. Therefore, the switching losses $P_{sw,on}$ and $P_{sw,off}$ are found as [17]:

$$\begin{aligned} P_{sw,on} &= f_{sw} E_{on}(V_{DS}, I_{DS}, T_j) \\ P_{sw,off} &= f_{sw} E_{off}(V_{DS}, I_{DS}, T_j) \end{aligned} \tag{3.2}$$

Where f_{sw} is the switching frequency of the power semiconductors. Equation 3.2 shows that both energies depend on V_{DS}, I_{DS} and T_j, analogous to the conduction losses from the previous section. The dependencies in I_{DS} and T_j are found in the datasheets in a similar manner as the ones for the resistance of the conduction losses, shown in Figure 3.1. The switching energies dependence on V_{DS} is roughly directly proportional to the drain source voltage applied; therefore, it can be computed by multiplying the obtained energy by a factor of $\frac{V_{DS}}{V_{DS,test}}$, where $V_{DS,test}$ is the drain-source voltage of the test used by the manufacturer to obtain the datasheet parameters.

Parasitic output capacitance losses

As switching frequencies increase in Switched Mode Power Supplies (SMPS), parasitic capacitances of power mosfets start to play a role when calculating the power losses. Moreover, in some soft switching topologies, some of this energy is not dissipated and therefore it is necessary to take this capacitances into account when comparing these topologies against the hard switched ones. Figure 3.2 shows the parasitic capacitances of a power mosfet.

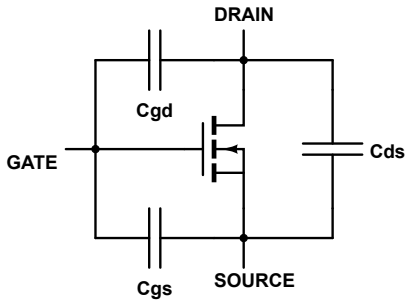


Figure 3.2: Power mosfet parasitic capacitances

At turn off both the drain to source capacitance C_{ds} and gate to drain capacitance C_{gd}, which form the parasitic output capacitance C_{oss}. are charged. This charge depends on V_{DS}, therefore the stored energy E_{oss} in C_{oss} is not linear. At turn on this energy is burned and losses and heating occur. When Zero Voltage Switching (ZVS) occurs, the body diode is conducting and the current is oriented from source to drain, discharging the C_{oss} previously to the the application of the gate voltage and reducing turn on losses.

The E_{oss} energy depending on V_{DS} is given by the mosfet manufacturer, making it possible to apply curve fitting as previously done for the derivation of the conduction losses. This energy is already considered in both E_{on} and E_{off} energies due to the fact that they are obtained experimentally in the Inductive Switching Loss test circuit, found in the datasheets. However, in ZVS topologies, this energy has to be subtracted as it is not lost. As a result in ZVS topologies the turn on is considered to be zero while the turn off losses are reduced. At low currents, considering that E_{oss} is more or less independent of the current I_{DS}, the turn off energy is approximately zero.

Gate losses

Gate losses are low compared to conduction losses and turn on and turn off losses. However, they are different depending on the selected switch and should be considered. Gate losses are linked to the energy required to energize the parasitic capacitance C_{gs} shown in Figure 3.2. The equation that describes this behavior [38] is:

$$E_{gate} = \frac{1}{\eta_{Drivers}} Q_g \Delta V_{GS} \tag{3.3}$$

Where $\eta_{Drivers}$ is the efficiency of the driving circuit, assumed to be 90% [38], Q_g is the gate charge and ΔV_{GS} is the voltage swing applied to the gate of the Mosfet. The power loss $P_{sw,gate}$ is obtained by multiplying E_{gate} times the switching frequency. Finally, the total losses of the power mosfet are:

$$P_{sw} = P_{sw,con} + P_{sw,on} + P_{sw,off} + P_{sw,gate} \tag{3.4}$$

3.1.2. Diode losses

SiC schottky diodes present low forward voltage when conducting and virtually no switching losses. When switching off a Schottky diode, there is no need to remove excess carriers from the n-region as there is for pn diodes; therefore, there is no reverse recovery current. Only a displacement current for charging the junction capacitance of the diode is observed [39]. This charge is very small compared to the reverse recovery charge (Q_{rr}) of conventional diodes, and it is denoted as Q_c in the manufacturer's datasheets.

The forward characteristics can be modeled as a temperature dependent forward voltage V_T and a series resistor R_T, which depend on the junction temperature and forward current. The total forward voltage V_{fT} is found and finally the conduction losses:

$$\begin{aligned} V_{fT} &= V_T(T_j) + I_{f,rms} R_T(T_j) \\ P_{d,con} &= V_{fT}(T_j, I_{f,rms}) I_{f,rms} \end{aligned} \tag{3.5}$$

Where $I_{f,rms}$ is the RMS value of the current through the diode. V_T and R_T values are found via equations of the form $y = ax+b$ where the parameters are directly proportionated by the manufacturer of the diodes.

The switching losses of SiC diodes are very low as explained previously. However, due to the relatively high frequencies considered in this thesis, they should be taken into account. The switching losses occur at the turn off of the diode and are due to the dissipation of the stored energy in the Schottky diode junction. This energy E_c depends on the reverse voltage applied to the diode, and its value is obtained directly from the datasheet. In order to take into account different values of V_R curve fitting has been performed. The switching losses are finally found as:

$$P_{d,off} = V_R E_c(V_R) f_{sw} \tag{3.6}$$

Therefore, the total losses of one diode are found as:

$$P_d = P_{d,con} + P_{d,off} \tag{3.7}$$

3.1.3. Magnetic elements losses

Magnetic elements like power inductors or transformers are formed by a magnetic material core and copper windings. The copper losses are obtained with the following equation:

$$P_{copper} = R_{ac,wire} I_{l,rms}^2 \tag{3.8}$$

Where $R_{ac,wire}$ is the resistance of the copper and $I_{l,rms}$ is the current through it. The resistance is obtained in the design of the magnetic elements, found on the next chapter of this report.

The core losses depend on the material used, the current waveform through the windings and the frequency. Core manufactures usually give the Steinmetz-equation parameters (k, α and B) which are used together with the conventional Steinmetz-equation:

$$P_v = k f^{\alpha} \hat{B}^{\beta} \tag{3.9}$$

Where P_v are the losses of the core per volume. The parameters of this equation are obtained with sinusoidal currents and are not accurate when dealing with the piece-wise linear current waveforms of DC-DC converters. This is the reason why the improved generalized Steinmetz-equation [40] is used for this purpose. The equation that computes the volumetric losses is:

$$P_v = \frac{1}{T}\int_0^T k_i \left|\frac{dB}{dt}\right|^{\alpha} (\Delta B)^{\beta-\alpha}\, dt \tag{3.10}$$

This equation uses the provided α and β parameters, while the k parameter is modified to obtain k_i, using the following equation:

$$k_i = \frac{k}{(2\pi)^{(\alpha-1)} \int_0^{2\pi} |cos\theta|^{\alpha} 2^{(\beta-\alpha)} d\theta} \tag{3.11}$$

The flux density waveform for every switching period depends on the operating point. As the current through the windings is known, simple magnetic circuit equations can be applied in order to find the flux density B, which is used in Equation 3.10. The equations that describe the magnetic behavior of the different power magnetic elements are found in the next chapter, where the design of all the converter components is found.

The final dissipated power depends on the volume of the core V_c , thus:

$$P_{core} = V_c P_v = A_c l_c P_v \tag{3.12}$$

Where A_c makes reference to the cross sectional area of the core and l_c its effective length. In the case of sinusoidal currents, as in the output filters of the converter, the original Steinmetz equation is used (see Equation 3.9).

3.1.4. Capacitor losses

The capacitor losses depend on the Equivalent Series Resistance (ESR) R_{ESR} which is directly obtained from the manufacturer's product datasheet. This resistance is computed from the losses of three different sources in the same capacitor [41]:

- Actual series resistance, in the leads and plates or foils.
- Leakage resistance, a parallel resistance due to leakage current in the capacitor.
- Dielectric losses, due to molecular polarization and interfacial polarization.

The two first sources of losses are frequency independent, but the dielectric losses depend on the equivalent frequency of the RMS current through the capacitor. If the manufacturer gives the nominal Equivalent Series Resistance $R_{ESR,nom}$ at the resonant frequency of the capacitor, this losses are zero [42]. Therefore, with the dielectric losses factor DF, which is material dependent, the R_{ESR} can be calculated. Moreover, as some topologies may require series and paralleled capacitors in order to increase the rated voltage and actual capacity respectively, $N_{c,s}$ and $N_{c,p}$ need to be taken into account too. Notice that when paralleling capacitors the ESR is reduced while connecting them in series makes it increase:

$$R_{ESR,set} = \frac{N_{c,s}}{N_{c,p}}\left(R_{ESR,nom} + \frac{DF}{2\pi f_{eq} C_r}\right) \tag{3.13}$$

Where f_{eq} the equivalent frequency of the capacitor current and C_r the rated capacity of the capacitor. Once this is known, the power losses in the set of capacitors are found as:

$$P_{cap} = R_{ESR,set} I_{cap,rms}^2 \tag{3.14}$$

Where $I_{cap,rms}$ is the RMS of the current through the capacitors.

3.1.5. High Frequency Transformer losses

High Frequency Transformer (HFT) losses are found in a similar way as the inductor losses. Copper losses are calculated in the same manner as copper losses in an inductor, see Equation 3.8. However, in a HFT, the induced flux in the core is proportional to the voltage applied at the windings [43]. According to Faraday's law, a flux $\Phi(t)$ is produced when a voltage across the winding $v_l(t)$ is applied:

$$v_l(t) = N\frac{d\Phi(t)}{dt} \tag{3.15}$$

The flux $\Phi(t)$ is distributed through the core cross-section resulting in a flux density $B(t)$:

$$\Phi(t) = \int_{A_c} B(t)dA \tag{3.16}$$

Finally, combining the previous equations and assuming a uniformly distributed flux through the core and a linear relationship $B = \mu H$ the flux density can be derived:

$$B(t) = \frac{1}{NA_c}\int_0^t v_l(\tau)d\tau \tag{3.17}$$

If it is assumed that the HFT is used in a power converter and that it applies square-shaped voltage waveforms in the windings, with amplitude V_L and time ΔT, the variation of the flux is given by [43]:

$$\Delta B = \frac{V_L \Delta T}{NA_c f_{sw}} \tag{3.18}$$

With this data the flux waveform is built and the Improved Generalized Steinmetz Equation (iGSE) method can be applied to obtain the losses in the core of the HFT, see Equations 3.10 and 3.11.

3.2. Weighted efficiencies

Considering the importance of the efficiency in the comparison framework, a proper method of finding the overall efficiency value which takes into account the different operating points of the multiport converter needs to be applied. The equations used for each port of the converter are listed in the three following sections.

3.2.1. PV port

Photovoltaic panels production heavily depends on weather conditions and localization. Moreover, the power produced during the day is not constant and therefore the converter works in a wide range of operating points, which mainly depend on the Maximum Power Point (MPP) of the PV panels at that instant of time.

Since the PV inverters operate under a fluctuating input power supplied by the PV modules, conversion efficiency must be measured against the weights of the probable power ranges which represent the various irradiation values. This approach of having different weights for different irradiation levels resulted in two basic weighted conversion efficiency models, the η_{EU} and the η_{CEC}. These two models consider the irradiation distribution over the whole annual sunny time and prioritize the different power outputs of the converter with various weight factors. The European based model gives more weight to efficiencies in the low power range due to lower irradiation of most European zones compared to the CEC model [44], which is American.

For this thesis, the European model has been considered as a basis. The European efficiency model is given by Equation 3.19 [45].

$$\begin{aligned}\eta_{EU} =& 0.03\eta(0.05P_{max}) + 0.06\eta(0.1P_{max}) + 0.13\eta(0.2P_{max}) + \\ &+ 0.1\eta(0.3P_{max}) + 0.48\eta(0.5P_{max}) + 0.2\eta(P_{max})\end{aligned} \tag{3.19}$$

Where η is the efficiency and P_{max} the maximum delivered power of the converter. This model takes into account the different powers at which the converter can operate and weights the amount of importance of each one (mainly depending on the amount of time this power is going to be produced by the PV panels). However, it lacks the consideration of different MPP voltages at which the converter can operate at the input. Thereby, it has been decided to apply a second criterion to the weighted efficiency, which is dependent on the DC voltage of the PV panels. Similar to the European efficiency method, it is written as:

$$\begin{aligned}\eta_{volt} =& 0.025 \cdot \eta(400V) + 0.1 \cdot \eta(450V) \cdot + 0.25 \cdot \eta(500V) + \\ &+ 0.5 \cdot \eta(550V) + 0.10 \cdot \eta(600V) + 0.025 \cdot \eta(650V)\end{aligned} \tag{3.20}$$

This weighting coefficients are not standard and have been calculated taking into account that:

- The converter can be installed together with many different models of PV panels and configurations, resulting in many different MPP voltages that have to be inside the converter operating range of 350 V to 700 V.
- The maximum open circuit voltage of the installed PV panels is supposed to be the maximum allowed DC voltage at the input of the converter, 700 V.
- Modern PV panels have a fill factor of around 75% [46] of the open circuit voltage (V_{oc}). As a consequence, the 550 V weight is the most important.
- At lower irradiances the MPP tends to be at a lower voltage. Therefore, the voltages lower than 550 V have more weight than the higher ones. Moreover, it is considered that the installation voltages will be around 500 V and 550 V, with a total weight factor of these two voltages of 75%.
- Voltages which are at both ends of the range have a munch lower weight in the final efficiency.

By using both equations η_{EU} and η_{volt}, a better estimate of the efficiency η_{PV} of the converter in the real application is obtained. The final efficiency of the PV port from the input to the DC link is therefore calculated as:

$$\eta_{PV} = \sum_{j=1}^{6}\sum_{i=1}^{6} \eta(P_j, V_i) \cdot W_{P,i} \cdot W_{V,j} \tag{3.21}$$

Where:

$$\begin{aligned} P_i &= \begin{bmatrix} 0.05 \cdot P_{max} & 0.1 \cdot P_{max} & 0.2 \cdot P_{max} & 0.3 \cdot P_{max} & 0.5 \cdot P_{max} & 1 \cdot P_{max} \end{bmatrix} \\ W_{P,i} &= \begin{bmatrix} 0.03 & 0.06 & 0.13 & 0.1 & 0.48 & 0.2 \end{bmatrix} \\ V_j &= \begin{bmatrix} 400 & 450 & 500 & 550 & 600 & 650 \end{bmatrix} \\ W_{V,j} &= \begin{bmatrix} 0.025 & 0.1 & 0.25 & 0.5 & 0.1 & 0.025 \end{bmatrix} \end{aligned} \tag{3.22}$$

3.2.2. EV port

The EV port efficiency is considered to have an equal weight in all operating points; therefore, the mean efficiency of the converter in the whole operating range is the final efficiency of the converter. There are no standards concerning battery voltages in EVs and therefore there is no weight factor applied to it.

3.2.3. Grid port

A similar approach to the one used to calculate the weighted efficiency of the PV port is applied to the DC-AC bidirectional port of the converter. In contrast to the PV port, there is no need to take into consideration different voltage levels as both the DC link and grid voltages are fixed. However, there is the need to model this converter in inverter mode of operation and rectifier mode of operation. As a result, the efficiency is obtained as:

$$\eta_{GRID} = W_{mode,Inv} \sum_{i=1}^{6} \eta_{Inv}(P_i)\ W_{Inv,i} + W_{mode,Rec} \sum_{i=1}^{6} \eta_{Rec}(P_i) W_{Rec,i} \tag{3.23}$$

Where:

$$\begin{aligned} W_{mode,Inv} &= 0.5 \\ W_{mode,Rec} &= 0.5 \\ P_i &= \begin{bmatrix} 0.05P_{max} & 0.1P_{max} & 0.2P_{max} & 0.3P_{max} & 0.5P_{max} & 1P_{max} \end{bmatrix} \\ W_{Inv,i} &= \begin{bmatrix} 0.03 & 0.06 & 0.13 & 0.1 & 0.48 & 0.2 \end{bmatrix} \\ W_{Rec,i} &= \begin{bmatrix} 0.03 & 0.05 & 0.08 & 0.1 & 0.32 & 0.42 \end{bmatrix} \end{aligned} \tag{3.24}$$

Please notice the difference between the weighting factors of the inverter mode and the rectifier mode. While the same factors as the European efficiency method for inverters have been applied in inverter mode, the factors used in rectifier mode are different. In this case, a greater weight is applied where the power is higher, because of the probability of using the converter during the nights for EV charging. Low powers are also considered as the Grid port can be used at low power, complementary to the PV port when there is a low irradiance, to charge the EV battery at full power.

3.3. Inverter loss calculation approach

In order to compare several topologies with each other, the efficiency is an important criterion. It defines the total power losses and the wasted energy, corresponding to a main part of the operational costs of a power electronic converter. However, the calculation method for DC-AC converters differs from the one used for DC-DC converters, where the current waveform during a switching period was known and simply formed of piece-wise linear segments. The calculations for this kind of waveforms are relatively easy using the equations provided in Section 3.1, but modeling the losses of a sinusoidal waveform requires a different approach.

The DC - AC bidirectional topologies presented in Section 2.3.3 can be controlled in many different ways, which require more or less computational power depending on the method used. Historically, sinusoidal Pulse-Width Modulation (PWM) was first implemented for the modulation of the Two Level Converter (2LC). The conduction and the switching losses of the semiconductor devices in the 2LC can be obtained analytically for the carrier-based PWM [47]. However, newer methods like Space

Vector Pulse-Width Modulation (SVPWM) have been introduced in the converter market because of the ability of using special phase-clamping modulation schemes, which can reduce total losses in the converter at the expense of increasing the Total Harmonic Distortion (THD), between other purposes.

Therefore, a generic loss calculation algorithm is suggested [48] for the calculation of the device losses and the converter efficiency. The algorithm is based on the fact that the state of every component of the inverter is known for every sampling period inside the modulation waveform, denoted as n. The conduction and the switching losses can be averaged as they are known at every n. The number of samples depends on the discretization of the carrier signal, increasing the accuracy when a higher density of samples is considered by switching period. For example, with a switching frequency of 50 kHz, 200 samples per period, and a modulation frequency of 50 Hz, samples ranging from $n = 1$ to $n = 200000$ have to be evaluated in order to obtain the steady state characteristics of the converter for a full cycle in steady state, in other words, the operation during 20 milliseconds. The losses are calculated for all elements of the topology at the same time, and finally averaged to obtain the total losses of the converter.

Applying the SVPWM method the states of the switches in each leg is known for every sampling period, named $\vec{S_n}$, where n denotes the sampling period. This state can take two positions in the two level converters, named P and N, when the output is connected to the positive port of the bus voltage or to the negative, respectively. In the three level converters, the 0 state is added, when the output voltage is clamped to the neutral point between the two bus capacitors. An example of the vector $\vec{S_n}$ is shown in Equation 3.25.

$$\vec{S_n} = \begin{pmatrix} S_{n,a} \\ S_{n,b} \\ S_{n,b} \end{pmatrix} = \begin{pmatrix} P \\ 0 \\ N \end{pmatrix} \tag{3.25}$$

In this example, vector $\vec{S_n}$ applies to a three level converter, and the first leg is connected to the positive, the second one to neutral and the third one to the negative port of the DC Link. Considering the current in each leg is also known, previously derived from the output power, the voltage and power factor, vector $\vec{I_n}$ is easily constructed, similar to $\vec{S_n}$. Therefore, the conduction losses can be defined as:

$$P_{cond,n}(\vec{S_n}, \vec{I_n}) = \begin{pmatrix} P_{T1a,con,n} & P_{D1a,con,n} & \dots & P_{Txa,con,n} & P_{Dxa,con,n} \\ P_{T1b,con,n} & P_{D1b,con,n} & \dots & P_{Txb,con,n} & P_{Dxb,con,n} \\ P_{T1c,con,n} & P_{D1c,con,n} & \dots & P_{Txc,con,n} & P_{Dxc,con,n} \end{pmatrix} \tag{3.26}$$

Equation 3.26 includes all the components which have conduction losses for each leg. Considering the three legs operate in a symmetrical fashion, it is not necessary to calculate the losses for more than one leg. Therefore, the second and third row of the matrix can be skipped in order to reduce computational time. The conduction losses depend on the device characteristics, the current in the leg and the state of the leg. Depending on the current and the state, different diodes or switches may conduct in inverter applications. Therefore, in order to obtain the conduction losses for each component, a conditional equation must be applied:

$$P_{T1a,con,n} = \begin{cases} P_{T1a,con}(i_{a,n}) & if \quad S_{n,a} = P \;\&\; i_a, n \geq 0 \\ 0 & otherwise \end{cases} \tag{3.27}$$

The conduction losses depend on the device, the topology and the switching state. Equations stated in Section 3.1 are used in order to estimate the losses of the device. The conducting devices

will be specified later on for each topology. The total conduction loss of each device is obtained by averaging the conduction losses. As an example, for the first device:

$$P_{T1a,con} = \frac{1}{L}\sum_{n=1}^{L} P_{T1a,con,n} \tag{3.28}$$

Where L denotes the total number of samples present in a sinusoidal cycle, which is equal to $\frac{f_{sw}}{f_{mod}}$ times the amount of samples per period.

Switching losses are obtained by knowing vector $\vec{S_n}$ and $\vec{S_{n-1}}$. When $\vec{S_n} \neq \vec{S_{n-1}}$, switchings have taken place. Therefore, it is possible to calculate the switching energy lost during the transition:

$$E_{sw,n}(\vec{S_n}, \vec{S_{n-1}}, \vec{I_n}) = \begin{pmatrix} E_{T1a,sw,n} & E_{D1a,sw,n} & \dots & E_{Txa,sw,n} & E_{Dxa,sw,n} \\ E_{T1b,sw,n} & E_{D1b,sw,n} & \dots & E_{Txb,sw,n} & E_{Dxb,sw,n} \\ E_{T1c,sw,n} & E_{D1c,sw,n} & \dots & E_{Txc,sw,n} & E_{Dxc,sw,n} \end{pmatrix} \tag{3.29}$$

This matrix is obtained again by using piecewise functions, which depend on the converter state and currents. As an example, the 2LC first device switching loss is calculated as:

$$E_{T1a,sw,n} = \begin{pmatrix} E_{T1a,sw,off}(i_a) & \text{if} & S_{n-1,a} = P \;\&\; S_{n,a} = N \;\&\; i_a \geq 0 \\ E_{T1a,sw,on}(i_a) & \text{if} & S_{n-1,a} = N \;\&\; S_{n,a} = P \;\&\; i_a \geq 0 \\ 0 & & \text{otherwise} \end{pmatrix} \tag{3.30}$$

The equations to obtain the switching losses for the devices have been listed in Section 3.1. The total dissipation energy due to switchings is finally obtained as:

$$P_{T1a,sw} = f_{mod}\sum_{n=1}^{L} E_{T1a,sw,n} \tag{3.31}$$

Where f_{mod} is the modulation frequency. By applying these equations over the whole sinusoidal wave, the total losses of the converter are obtained.

3.4. Conclusion

In this chapter the loss models used for the different components has been explained. This equations are used for the design and evaluation of the different components and converters, which are found on the next chapters.

As the power of a converter highly depends on its operating point, different efficiencies have been obtained. In order to evaluate the final efficiency of the converter, a weight factor is applied to the efficiency in several operating points. The European weighted factors have been explained and modified in this chapter in order to fit the characteristics of the multiport converter, and are used to evaluate the final efficiency of each converter.

Lastly, a generalized calculation method for the losses in the DC-AC converters is explained. This is necessary because different modulation techniques are considered for the inverters in Chapter 7 and 8, and this methodology simplifies the losses calculation.

4

Converter Design Methodology

The design and selection of the different components that form a power converter is decisive for the converter evaluation as efficiency and volume depend on it. This section contains the methods used for the design of the magnetic elements and the sizing and selection of the semiconductors and other devices.

Each considered topology is designed for two switching frequencies, 50 and 100 kHz. These frequencies are common when using SiC devices and allow to compare two different designs, one with lower switching losses ($f_{sw} = 50kHz$) and higher elements volume, and another one with higher losses ($f_{sw} = 100kHz$) but a lower volume. This approach requires of different element designs for each configuration, making it necessary to automate the design process of the different elements which form the topologies.

4.1. Power inductor design

Power inductors are key elements in power electronics; they store energy in the form of a magnetic field to enable power conversion. In order to do so, they are formed by a ferromagnetic core and copper windings, and those elements have to be properly sized in such a way that the necessary energy is stored with the lowest volume and losses possible.

The design process for power inductors based on ferrite cores is explained in this section. The cores selected are six different E shaped cores. E cores are relatively cheap, with windings which are simple to bobbin and have easy assembly. The smaller size is E16 while the biggest one is E65, the maximum size which allows for PCB mounting. The inductor design results include the core size, number of turns, number of strands for the Litz wire, American Wire Gauge (AWG) size, length of the air gap and AC series resistance of the copper. These parameters are later used for the evaluation of the efficiency and size of the different evaluated converters.

Different materials have been considered too. From the manufacturer Magnetics INC, R and P materials have been chosen. On the other hand, from the manufacturer FerroxCube their 3C92 and 3C96 materials are considered. As a result, a total of 24 different cores can be selected initially for the design, see Appendix A for more information.

The design follows an optimization procedure, and it is performed for every core and material:

1. Cores which do not fulfill the requirements in terms of energy storage and losses are discarded.
2. Minimum and maximum number of turns is calculated, considering flux saturation limits of the material.

3. The optimal Litz wire configuration is found for every possible number of turns.
4. Air gap length calculation for the different available number of turns.
5. Calculation of the copper and core losses for every configuration.

Finally, taking into account that the most important parameters for the rating of the topology are efficiency and weight, the cost of each working inductor is set to be:

$$F_{cost} = \frac{1}{2}\frac{P_{loss}}{P_{loss,max}} + \frac{1}{2}\frac{V}{V_{max}} \tag{4.1}$$

Where $P_{loss,max}$ are the losses of the working design with higher losses and V_{max} is the volume of the inductor design with a higher volume. The inductor design with a lower F_{cost} is the optimum design in terms of losses and volume. Both characteristics have been given an equal weight for the final selection, as this thesis focuses both on maximum efficiency and lowest volume possible. A flowchart of the design is found at the end of this section, in Figure 4.1, after all the steps followed for the design have been thoroughly explained.

4.1.1. Core size evaluation

Given a peak winding current I_{max}, it is necessary to make the core reach a maximum flux density lower than the saturation value, B_{max}, which should be chosen to be a little bit lower than the saturation value of the core B_{sat}. Considering a simple magnetic circuit [49], where the reluctance of the gap is much higher than the reluctance of the magnetic material $(\Re_g \gg \Re_c)$, the following relation is obtained:

$$NI_{max} = B_{max}A_c\Re_g = B_{max}\frac{l_g}{\mu_0} \tag{4.2}$$

Where N is the number of turns, A_c is the core area, l_g is the length of the gap and μ_0 is the magnetic permeability of free space. This is the first relation that must be fulfilled with the design of the core. The second requirement is that it has the desired inductance L, which is obtained from Equation 4.3, again considering $(\Re_g \gg \Re_c)$.

$$L = \frac{N^2}{\Re_g} = \frac{\mu_o A_c N^2}{l_g} \tag{4.3}$$

A physical restriction that must be taken into account is that the wire must fit inside the core window:

$$K_u A_W \geq N A_{litz} \tag{4.4}$$

Where K_u is the utilization factor of the winding area A_W, and A_litz is the cross-sectional area of the wire used. The maximum K_u factor is around 0.3 and 0.35 for Litz wire [1], and this value will be used for all designs.

The last necessary equation is related to the actual resistance of the copper, which is required to be as low as possible in order to minimize copper losses:

$$R = \rho\frac{l_b}{A_{litz}} = \rho\frac{N\,(MLT)}{A_{litz}} \tag{4.5}$$

In this equation l_b makes reference to the length of the wire of the bobbin, which is equal to the number of turns times the Mean Length Turn (MLT). ρ is the copper electrical resistance.

If the three unknowns (N, l_g and A_{litz}) are eliminated from the four constraints, the result is a single equation which must be fulfilled:

$$\frac{A_c^2 A_W}{(MLT)} \geq \frac{\rho L^2 I_{max}^2}{B_{max}^2 R K_u} \tag{4.6}$$

The left-hand side of the equation is only related to core geometry, while the right-hand side is dependent on the inductor specifications or are known quantities. Thus, if a pre-set list of cores is considered, only those which fulfill Equation 4.6 are candidates for the final selection. The resistance is the only parameter which is not design driven, and therefore the parameter that decides the core selection. A higher maximum resistance probably leads to smaller cores, or in the case that no core satisfies the previous equation, increasing the resistance limit allows for a design using the same core although increasing the losses. The maximum resistance allowed in the windings throughout the whole thesis is 50 mΩ. This maximum resistance makes the designs have low losses at the copper, therefore enhancing the efficiency, which is the main parameter evaluated in this thesis. As a result, only cores which allow a design with a resistance lower than 0.05 Ω will be considered for further design.

This method is similar to the LI^2 method that manufacturers use, which relies on the energy storage capabilities of the core, but it allows to make a selection between different cores without having to rely on charts provided in the datasheets, which require an approximation and can not be implemented manufacturer independent. Only some geometrical information from the core is needed when using the method presented in this section.

The cores that are used for the designs are listed in Appendix A, including the main key aspects of each one. Bigger cores than E65 have not been considered due to the fact that it is not possible to easily mount them in common PCBs, as previously stated.

4.1.2. Number of turns and air gap length

The number of turns of a design is not a fixed number. As stated in Equation 4.3, the inductance depends on the number of turns and length of the gap. Thus, it is possible to reduce the number of turns while keeping the same inductance by modifying the length of the gap. This results in a decrease of the copper losses and an increase of the core losses. In order to find the optimal number of turns, the losses for a wide range of turns is computed and the number of turns which performs better in terms of losses is selected.

The number of turns has a lower and an upper limit. The lower limit N_{min} is set in such a way that the gap can store the necessary energy in the air gap [50], see Equation 4.7.

$$N_{min} = ceil\left(\frac{LI_{max}}{B_{sat}A_c}\right) \tag{4.7}$$

Where I_{max} is the maximum current through the bobbin and A_c the cross-sectional area of the core. $ceil$ is a function which rounds up to the closest integer. The upper limit is defined by the maximum air gap length $l_{g,max}$, which is set to be of 2 mm per leg, see Equation 4.8. Higher lengths yield to flux fringing, increasing the copper loss.

$$N_{max} = floor\left(\frac{B_{sat}}{I_{max}}\left(\frac{l_{g,max}}{\mu_0} + \frac{l_m}{\mu_0\mu_e}\right)\right) \tag{4.8}$$

Where l_m is the magnetic length of the core and $floor$ a function which rounds down to the closest integer. Any number of turns which is not between N_{min} and N_{max} is not considered. A second maximum number of turns of 150 is also set arbitrarily in order to discard those designs which have a high number of turns and therefore increase manufacturing complexity.

Table 4.1: Parameters for economical Litz Wire [1]

AWG size	32	33	34	35	36	37	38	39	40	41	42	43	44	45
Diam. [mm]	0.202	0.180	0.160	0.143	0.127	0.113	0.101	0.090	0.080	0.071	0.063	0.056	0.050	0.045
F_R	1.06	1.07	1.09	1.11	1.13	1.15	1.18	1.22	1.25	1.30	1.35	1.41	1.47	1.54
k [mm^{-3}]	130	203	318	496	771	1.2k	1.8k	2.8k	4.4k	6.7k	10k	16k	24k	36k

According to Equation 4.3 the inductance depends on both the number of turns and reluctance of the core. A longer gap involves results in a higher reluctance and therefore a bigger number of turns is required, but it reduces the maximum flux in the core and the core losses. Therefore, an optimization method can be followed. The necessary gap length is calculated using Equation 4.3 for every number of turns. The flux density in the core with the specified air gap is is computed using Equation 4.2.

4.1.3. Litz wire design

Litz wires are chosen to reduce eddy current losses in the windings [51] [52], being particularly effective at high switching frequencies. A Litz wire consists of a bundle of strands which are individually enameled and weaved along the entire divided conductor in a way that all wires pass through all points of the bundle's cross section. The total bundle current is then divided equally among the separate strands.

The design of the Litz wire has been performed by using the methods found on [1], an article published by Charles R. Sullivan where a simplified design method for Litz Wire is exposed. This method allows to obtain the optimal number of strands for the inductor, in terms of performance and cost.

The first step is to compute the skin depth δ:

$$\delta = \sqrt{\frac{\rho}{\pi f \mu_0}} \tag{4.9}$$

Where ρ is the resistivity of the conductor, f the frequency of the current and μ_0 the permeability of free space. When this is known, the following step needs the breadth b of the core and the number of turns N. With this information, together with Table 4.1, it is possible to compute the recommended number of strands n_e for different AWG wire sizes:

$$n_e = k\frac{\delta^2 b}{N} \tag{4.10}$$

Where N is the number of turns and k the factor in Table 4.1. When this is done, there is a wide range of good design options to choose from. To select one of these, it is checked weather the design fits in the winding area and if it does, the resulting resistance is calculated, and the option with lowest AC resistance is chosen. The resistance R_{ac}, which is used to calculate the losses, is obtained with 4.11 using the F_R parameter, which is taken from Table 4.1 and the R_{dc} resistance, which is simply computed by the wire length, the cross sectional area, the copper resistivity and the number of strands.

$$R_{ac} = R_{dc}F_R \tag{4.11}$$

A restriction of the wire gauge that has to be applied is the maximum current density J_{max} allowed through the Litz. A current density of maximum 4 A·mm^{-2} has been selected, and those designs that

have a current density higher than this value are automatically discarded. This current density is lower than the theoretical maximum of copper wire, but it is preferred for the litz wire to work under limit conditions, because of the lower thermal conductivity characteristics due to its construction.

4.1.4. Inductor losses calculation

The losses are calculated by using the equations presented in Section 3.1. The thermal requirements of the core are also taken into account, as the core must be able to exchange the generated heat with the exterior. Equation 4.12 is used in order to calculate the maximum amount of power loss that the core can have:

$$P_{max} = \frac{\Delta T_{max}}{R_{th}} \tag{4.12}$$

Where ΔT_{max} is the maximum increase of temperature of the electromagnetic element and R_{th} its thermal resistance. R_{th} for ferrite cores is derived from Equation 4.13 as in [53] (where V_c is the volume of the core), where this empirical equation is derived from data of many publications. In [54] a comparison between this equation and work from various authors is cross-checked in order to validate the results. If the power dissipated by the design is higher than P_{max} it is discarded and the next E core size is chosen.

$$R_{th,ferrite} = 53 V_c^{-0.54} \tag{4.13}$$

4.1.5. Flowchart of the power inductor design

Figure 4.1 shows how the optimum design is found for each needed power inductor, including the necessary databases and which inductor designs are saved for final selection. A validation of the followed procedure for the inductor designs is available on Appendix B.

4.2. Coupled power inductor and Flyback Transformer design

Some of the topologies compared in this report make use of coupled inductors, where to bobbins are found in the same core. In the case of the Interleaved Bidirectional Flyback Converter (IBFC), Flyback Transformers (FBT) are used, which are designed similarly to coupled inductors. The same equations as described in the previous sections have been used, with the proper modifications in order to take into account the presence of two different coils in the same core. The coupling factors k and disposition of the coils is discussed in Appendix B, where a FEM analysis of an E65 core is performed. The coupled inductors could be designed for an specific coupling coefficient. However, this requires custom cores that have to be tailor-made for the converter. In order to be able to compare the Coupled Inductors Interleaved Boost Converter (CIIBC) with the rest of the converters, different direct and reverse couplings have to be considered, while still using E cores in the design.

The equations require the modification of the flux generated in the core, which is proportional to the current flowing in the coils. The equivalent current, seen from inductor number one, is computed using Equation 4.14. Considering that the number of turns in both windings is the same, as only symmetrical designs are considered, only the sum of both the currents have to be taken into account for a proper design.

$$i_{eq} = i_1(t) + \frac{N_2}{N_1} sign(k) i_2(t) \tag{4.14}$$

The configuration with two windings in the middle leg of the E core yield a high coupling factor,

about 0.9. The drawback of this configuration is that the winding area for each coil is halved, making it more difficult to fit a certain number of turns. On the other hand, placing the two coils in the outer legs yields a coupling factor of 0.35, which is expected due to the three legs configuration. For this option the coils can use the whole winding space and the mean turn length of the coils is decreased because the outer legs are slimmer.

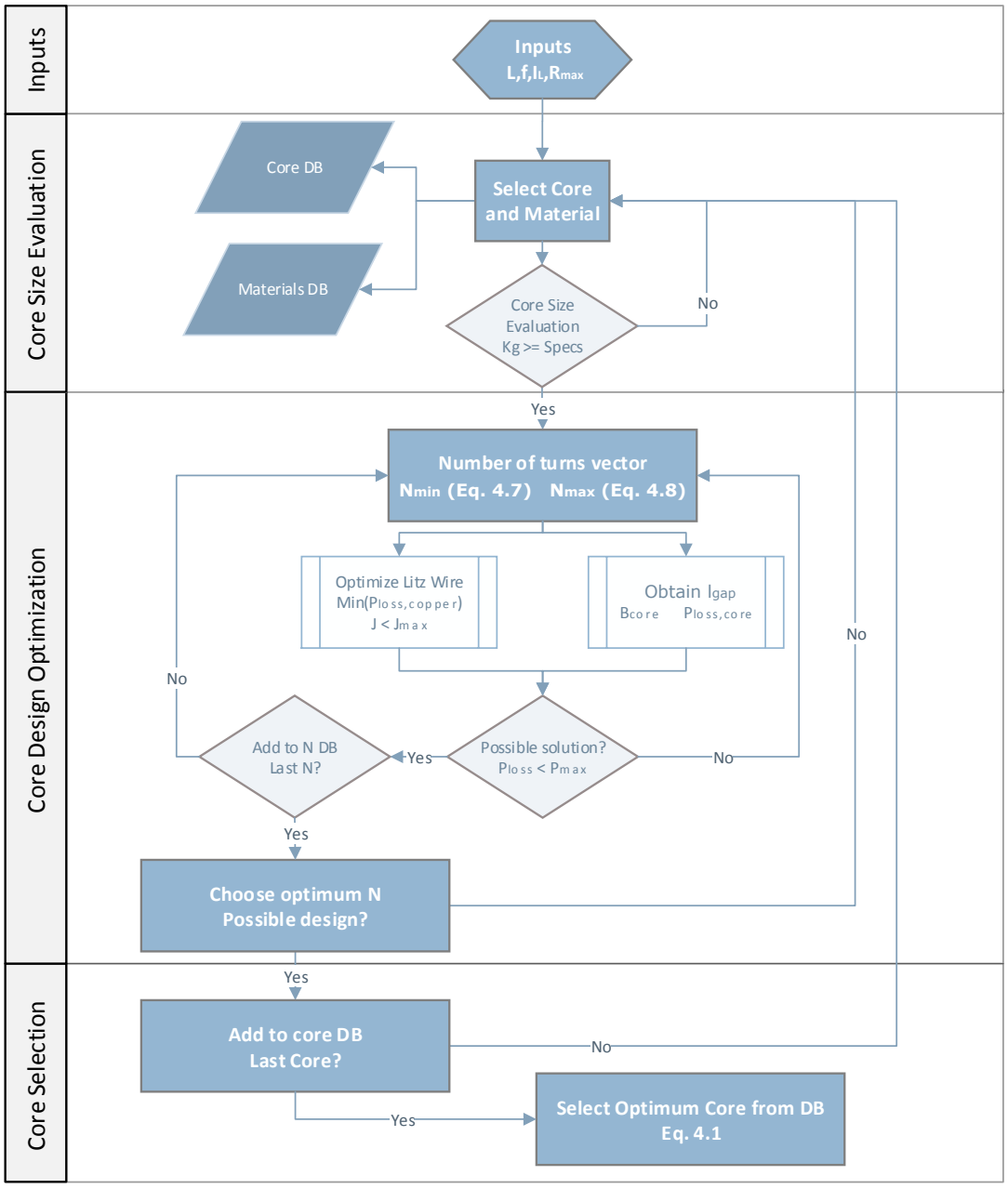


Figure 4.1: Flowchart of the power inductor design.

The configuration with the coils in the inner legs can be treated in the same way as the simple power inductor. However, the configuration with the coils in the outer legs presents a different equivalent circuit which must be solved in order to find the resulting flux density in the core to check for saturation, see Figure 4.2. In order to find the flux density in the core, set of Equations 4.15 have to be solved. Once the flux is known, the flux density can be found by diving it with the core area of the leg. The advantages and disadvantages of each configuration depend on the converter topology

and are considered later on the report.

$$\begin{aligned} Ni_1(t) &= \phi_2 R_2 + \phi_1 R_1 \\ Nsign(k) i_2(t) &= \phi_3 R_3 + \phi_1 R_1 \\ \phi_1 &= \phi_2 + \phi_3 \end{aligned} \tag{4.15}$$

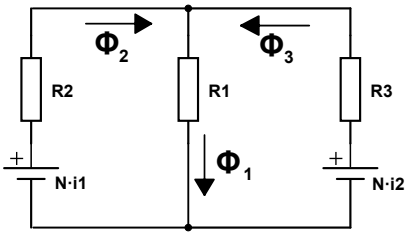


Figure 4.2: Magnetic model of the coupled inductor with the coils in the outer legs.

4.3. Filter inductor design

Filter inductors are necessary for the connection of the multiport converter to the grid; the output of the inverter is not completely sinusoidal and therefore injected power quality needs to be increased in order to reduce the harmonics of the injected current. Compared to power inductors, lower frequencies apply and higher currents must be possible; therefore, toroid cores are used instead of E cores, and powder materials instead of ferrites. Powder materials have higher losses than ferrites, but considering the low frequency and the high amplitude of the AC currents injected to the mains, powder materials are better candidates as the saturation flux is usually higher. Moreover, the cost of the core is reduced.

Powder inductors are different from ferrites because they have a distributed air-gap. Therefore, in order to get the desired inductance, there is a unique number of turns that satisfies the design. MAG INC has several Powder materials and toroid sizes, and their cores have been chosen to design the necessary filters. Not all toroid sizes are constructed in all the materials they have, so a selection has been made in order to evaluate the properties of the materials and obtain the optimal design for the filters. A total of 21 toroids are considered, which are made of different materials like Kool Mu 26 60 and 125, Xflux 26, Amoflux, MPP 26 and 14 and High Flux 26 and 125, see Appendix A.

The design is performed for 21 different toroids and the optimal one is selected, again using Equation 4.1 which yields the optimum solution.

4.3.1. Number of turns

From the manufacturer datasheet, the nominal inductance A_L of the toroid can be obtained. This parameter is in $\frac{nH}{T^2}$, in such a way that the necessary number of turns T can be obtained for a required inductance L:

$$N = \sqrt{\frac{L \cdot 10^9}{A_L}} \tag{4.16}$$

However, depending on the DC Bias, or in other terms, the DC current through the inductor, the A_L paramater changes, because of the distributed air-gap of the powder material. An example of this behavior is shown in Figure 4.3.

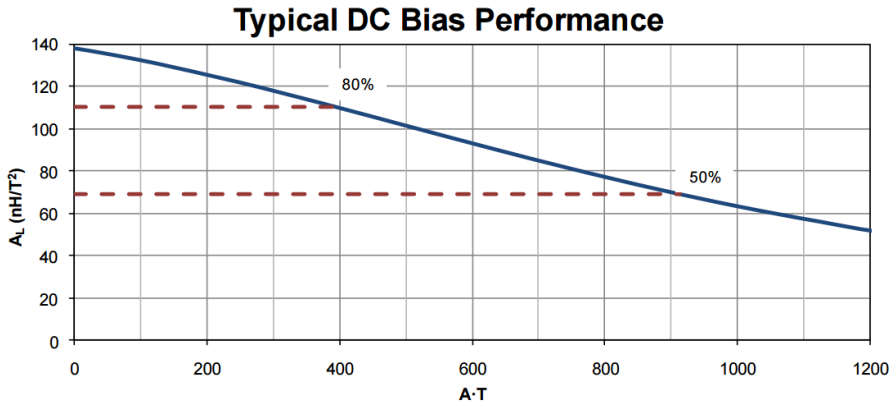


Figure 4.3: DC Bias performance example of Kool Mu 0077192A7 toroid. Source: Datasheet

As a result, in order to find the necessary number of turns for a toroid design, an iterative process is needed. Using the nominal A_L and maximum current a first guess of the necessary number of turns is obtained, which results in a different A_L when looking at the plots like the one on Figure 4.3. Afterwards, using interpolation from the manufacturer data, it is possible to iterate until the necessary number of turns N is found. The maximum current is always used for this purpose. Lower currents yield higher inductances and therefore they lead to no problem in the design, keeping the Total Harmonic Distortion (THD) low.

4.3.2. Core saturation and losses

Magnetization curves are also given by the manufacturer in the form of an equation with input parameter the magnetizing force in $\frac{A \cdot T}{cm}$, which depends on the current, the number of turns and the equivalent magnetic length of the toroid.

As all the parameters are known, it is possible to obtain the flux waveform on the core, check that the maximum flux is not over the saturation limit of the material and afterwards calculate the losses in the material.

4.3.3. Wire size

Considering the grid voltage is fixed and the power of the multiport converter too, the maximum total current is fixed. Therefore, a single wire of AWG 12, equivalent to 3.31 squared millimeters is chosen. Considering a maximum current density J_{max} of 6 A·mm^{-2}, this wire size generously covers the RMS current at the converter output which is just under 15 A.

The winding area is also considered, as the obtained number of turns must fit the toroid. The manufacturer gives in the datasheet an MLT which depends on the winding factor, in other words, the amount of area that is occupied by the windings of the total area available. The data is given in form of a table and interpolation is useful to obtain the MLT of any winding factor. As the total number of turns and the wire size is known, it is possible to obtain the winding factor and afterwards the MLT of the design. When the MLT is known the wire length can be obtained and therefore the resistance.

If the resistance is detected to be too high, over the maximum permitted which is set to be 50mΩ, then a second parallel winding is considered in order to make the design feasible at the cost of increasing the expenses. The second parallel winding increases the winding area and therefore the MLT, but total series resistance is halved. No more than two parallel wires are considered.

4.3.4. Losses calculation

Losses for the different elements of the filter inductors are calculated using equations in Section 3.1 too. In the case of filter inductors powder cores are used, and the manufacturer MAG INC gives an approximation of the power dissipation capabilities. The maximum power dissipation depends on the surface area of the toroid, which is obtained from a linear function derived from datasheet data, because it depends on the winding factor. The equation used for powder cores is:

$$P_{max,powder} = A_s \Delta T^{\left(\frac{1}{0.833}\right)} \tag{4.17}$$

Where A_s is the surface area of the toroid, obtained from the datasheet. Powder cores have a higher thermal conductivity than ferrites and therefore the power losses are allowed to go higher for the same volume.

4.4. High Frequency Transformer design

The High Frequency Transformer (HFT) follows a similar procedure to the power inductor design. The main differences are found in the core shape, which is formed by four U shapes, and the equations used in order to obtain the flux of the core. This materials are found in U shapes or toroidal shapes mainly, and they are not PCB mountable. The different considered sizes can be found on Appendix A. The HFT could also be made using ferrite and E shaped cores, but those yield higher losses, and considering their low conductivity, high volumes are needed. Due to the voltage swing in HFTs, the induced flux is higher and core losses result in approximately 50% of the losses in the transformer, while in the case of power inductors core losses is a much lower faction.

Taking this into account, the best option to build the necessary HFTs is to use amorphous and nanocrystalline materials for the design, which come in U shapes. In this case, four materials are compared:

- METGLAS 2605SA1 (amorphous)
- MKM Nanocrystalline
- VAC Vitroperm500F (nanocrystalline)
- Hitachi Finemet FT-3M (nanocrystalline)

4.4.1. Number of turns

The number of turns of the HFT is not a fixed number, while the turns ratio is fixed by the topology design. It is possible to have a low number of turns with a high flux density or a high number of turns with a low flux density, see Equation 3.18. Again, both copper and core losses play a role in this matter, and the design which produces a lower sum of both losses has to be found.

In order to find the optimal number of turns, the losses for a wide range of turns is computed. The design which performs better will be the final one. The number of turns has a lower and an upper limit. The lower limit is set in such a way that the peak flux density does not exceed a the predefined B_{sat} of the material, which depends on the maximum $V_L \cdot s$ applied across the windings:

$$N_{2,min} = ceil\left(\frac{max(V_L \cdot s)}{B_{sat} A_c f_{sw}}\right) \tag{4.18}$$

The upper limit is defined by the minimum flux at the core B_{min}, which is set to be of 0.05 Tesla in Equation 4.19. This upper limit is not necessary but it reduces the computing time of the different winding configurations.

$$N_{2,max} = floor\left(\frac{max(V_L \cdot s)}{B_{min} A_c f_{sw}}\right) \tag{4.19}$$

Any number of turns which is not between N_{min} and N_{max} is not considered. The number of turns in the primary is found via the turns ratio n for every possible N_2.

$$N_1 = \frac{N_2}{n} \tag{4.20}$$

4.4.2. Litz wire design

Please refer to Section 4.1.3 for the Litz wire design. The main difference with the power inductor wire configuration is that the winding area has to be divided into two zones, one for each winding. The space is arbitrarily split into two zones depending on the turns ratio n and the maximum conducted current, and each winding is made to fit there with the previously explained method.

4.4.3. Core saturation and losses

Core flux density depends on the voltage applied in the windings of the HFT. According to Faraday's law, and as previously explained in Section 3.1.5, the flux density in the core is:

$$\Delta B = \frac{V_L \Delta T}{N A_c f_{sw}} \tag{4.21}$$

Where V_L is the voltage across the winding and ΔT the amount of time during which the voltage is applied. With this equation the flux waveform inside the core can be computed and therefore the peak flux density and losses. In terms of power dissipation capabilities for the materials used in HFT construction, R_{th} is given for various sizes of toroids in the Vitroperm 500F datasheet. If the thermal resistances are plotted, it results in a similar behavior as Equation 4.13 for ferrite cores. An approximation of the data to this Equation has been made in order to make it volume dependent and adaptable to U shaped cores, resulting in Equation 4.22. This has been used together with Equation 4.12 for all nanocrystalline and amorphous materials as manufacturer data is very limited in this aspect.

$$R_{th,nanocr.} = \frac{0.0027}{V_c^{0.6709}} \tag{4.22}$$

4.5. Mosfet selection

A set of Mosfets from CREE whose characteristics are listed on Appendix A is considered. In order to make sure the chosen mosfet meets the converter requirements, both the voltage and the switch current are checked against the parameters provided by the manufacturer, in such a way that those devices that would operate outside the safe operating area of the converter during steady state operation are automatically discarded. A 25% voltage margin is considered in order to account for possible voltage spikes that might occur during the converter operation.

The optimum mosfet is selected by calculating the losses for each mosfet in the most demanding operating point; the mosfet which results in lower losses is the most appropriate switch. This is done because both conduction and switching losses play a role in the efficiency of the converter. A switch with higher switching losses and lower conduction losses might be more advisable for a 50 kHz configuration while at 100 kHz it could be possible that another mosfet, with higher conduction losses but lower switching dissipated energy, performs a better job.

This approach to select the mosfet might not be the best solution when aiming at the highest efficiency, because it is possible that other mosfets have lower losses in most of the operating ranges when compared to selected one and achieve a higher weighted efficiency. However, this method selects the mosfet which yields minimum total losses, reducing the cooling needs and as a consequence the converter volume. This fact is explained later in this chapter, Section 4.9, where the sizing of the cooling system is explained.

4.6. Diode selection

A set of diodes from CREE is considered, whose characteristics can be found on Appendix A. The selection method is similar to the mosfet selection method previously explained, searching for the optimal model.

In some topologies high currents are found through the diodes; as a consequence, high losses occur and high power dissipation is necessary. Considering the positive temperature coefficient of the SiC diodes, it is possible to parallel them. Therefore, in case that high losses are found in one diode, it is checked if it is advisable to add more units in parallel.

4.7. Capacitor set selection

Different film capacitors from TDK with different rated voltages and capacities are considered, whose characteristics can be found in Appendix A. The capacitor design consists on selecting the necessary number of series capacitors $N_{c,s}$ and parallel capacitors $N_{c,p}$ for every considered capacitor, while aiming for the lowest volume and PCB surface. The surface that the capacitors occupy in the PCB is considered to be important because a high number of capacitors with a low volume might be the design with the lowest volume, but it increases the cost of the PCB due to a large area. In order to take this into account, the certain cost of a configuration is computed establishing the same weight for both factors, in a similar way to the cost of an inductor design:

$$F_{cost} = \frac{1}{2}\frac{A_{set}}{A_{set,max}} + \frac{1}{2}\frac{V_{set}}{V_{set,max}} \tag{4.23}$$

The losses of the capacitors are not considered for the cost as they are low compared to the losses in other components. The requisites of the design of the set of capacitors, which might be composed of only one, are the following ones:

- The rated voltage is 25% higher than the maximum voltage applied in the leads, computed from the topology design, in order to accommodate for possible voltage peaks.
- The total capacity is equal or higher to the minimum required capacity, which is obtained from the topology design.
- Two series capacitors are considered in the case the topology requires a split capacitor (middle point connection).
- The voltage ripple is not higher than the maximum required one, characteristic which depends on the port.
- With the capacitors operating at full load the temperature is still kept below 90ºC.

The case temperature T_{case} of the capacitor is wanted to be under 90ºC. Manufacturers establish a maximum temperature that the capacitors can reach and the resulting life expectancy in hours at maximum rating. The relationship between life and temperature follows a chemical reaction formula called Arrhenius' Law of Chemical Activity. The case of film capacitors is quite similar electrolytic capacitors but voltage derating has a greater effect on the life as compared to an aluminum electrolytic

capacitor. The law establishes that the lifetime of a capacitor doubles for every 10 degree Celsius decrease in temperature approximately. Therefore, the number of capacitors in parallel might be incremented in order to decrease the Equivalent Series Resistance (ESR) and the losses.

The thermal resistance $R_{th,c-a}$ of the capacitor case to the ambient is obtained from the manufacturer specifications at rated load:

$$R_{th,c-a} = \frac{T_{max} - T_{amb}}{I_{c,RMS,max}^2 R_{ESR,nom}} \tag{4.24}$$

Where T_{max} and T_{amb} are the maximum and ambient temperatures specified by the manufacturer, $I_{c,RMS,max}$ the maximum RMS current through the capacitor and $R_{ESR,nom}$ the nominal ESR. With $R_{th,c-a}$ and the losses on the capacitors it is possible to determine if the temperature increases too much, having to increase the number of capacitors in parallel in order to decrease the losses.

The voltage ripple of the capacitor would not be a problem if the capacitor did not have an associated parasitic resistance and inductance, because the topology designs already consider the necessary capacitance. However, if the achieved capacitance happens to be very similar to the needed one, the extra voltage due to the parasitic elements would increase the ripple voltage. Therefore, the voltage ripple is computed from the impedance Z_c which depends on the capacitor current frequency:

$$\begin{gathered} Z_{set} = \frac{N_{c,s}}{N_{c,p}} \sqrt{R_{ESR}^2 + (X_c - X_l)^2} \\ V_{set,rip} = Z_{set} I_{cap,rms} \end{gathered} \tag{4.25}$$

Where Z_{set} is the impedance of the set of capacitors, $N_{c,s}$ and $N_{c,p}$ are the number of capacitors in series and parallel, R_{ESR} the ESR of the set and X_c and X_l the impedances. Again, when increasing the number of parallel branches of resistors the impedance is reduced, resulting in a lower voltage ripple $V_{set,rip}$. With this information it is possible to compute how many capacitors in series and parallel are needed for every possible considered capacitor, for later selection of the set with lower cost.

AC capacitors have to be used for the LCL filters. Same procedure as the used for DC capacitors applies, but the modulation frequency ESR has to be taken into account. With the ESR at the modulation frequency, the capacitance and the Equivalent Series Inductance, the impedance at modulation frequency can be found. Losses at both the frequencies have to be taken into account to compute the maximum temperature of the set of capacitors and total losses.

4.8. LCL output filter design

The grid converter injects or withdraws current from the mains. The switching nature of the converter makes this current have a high content of harmonics that have to be limited. There are regulations which indicate the current harmonic limits in percentage of the rated current amplitude [2], which depend on the type of electrical equipment. The multiport converter is considered a power generation equipment and the limits that apply are listed in Table 4.2 for every harmonic h.

Lissere [55] introduced the first method for the design of an LCL filter, which structure is displayed on Figure 4.4. LCL filters are formed by two inductors, the converter inductor $L_{f,conv}$ and the grid inductor $L_{f,g}$, and one capacitor C_f. There is also the necessity to add a damping resistor $R_{f,d}$. The grid inductance L_g also plays a role in the converter behavior, and although it is small, it has been considered for the design. This topology offers advantages over L and LC filters [56] [57]; while the number of components is increased with respect to traditional L and LC filters, the size and cost are reduced and the efficiency is boosted. Lissere's method is based in some restrictions that have to be considered in order to achieve an efficient and low cost design:

Table 4.2: Current harmonic limits of rated current amplitude according to IEEE-519 [%] [2]

I_{SC}/I_g	$h < 11$	$11 \leq h < 17$	$17 \leq h < 23$	$23 \leq h < 35$	$35 \leq h$
< 20	4.0%	2.0%	1.5%	0.6%	0.3%

I_{SC} : grid short circuit current

I_g : maximum demand grid current

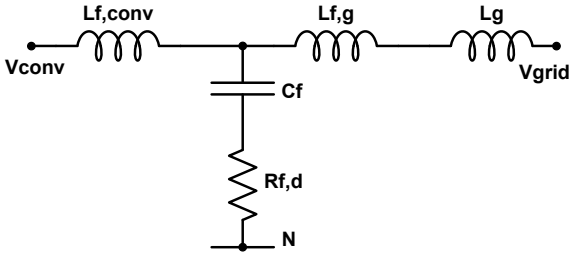


Figure 4.4: LCL filter topology

- Capacitor value limited by the decrease of the power factor (generally less than 5%).
- Total value of inductance less than 0.1pu to limit AC voltage drop.
- Resonant frequency in the range between ten times the line frequency and half the switching frequency.
- Passive damping must be sufficient to avoid oscillation, but not too high to avoid losses.

However, this method does not optimize the filter design and requires of a trial and error method in order to find a compatible LCL design. Therefore, several authors have done research in iterative methods for the design of the LCL filter [58] [59]. In order to find the optimal inductances, capacitor value and proper damping resistor $R_{f,d}$ for the LCL filter, an iterative method has been used.

The minimum converter inductance $L_{f,conv}$ is selected in such a way that both the current ripple at the connection of the converter is under the 20% of the total maximum current and the $(m_f\text{-}x)^{th}$ harmonic of the current respects the limits seen in Table 4.2. The $(m_f\text{-}x)^{th}$ harmonic referes to the most relevant harmonic, and therefore, if it is neutralized all the rest are. This harmonic is found two places before the switching harmonic in most modulation techniques. For example, if the converter switches at 50 kHz and it is connected to a 50 Hz grid and uses Space Vector Pulse-Width Modulation (SVPWM), the harmonic with a higher amplitude is the 998^{th}.

The necessary inductance to limit the current ripple is found via the maximum voltage ripple per second at the output of the converter. Considering that the output voltage of every leg of the converter is known, the voltage applied to the $L_{f,conv}$ inductance is the ripple voltage, or in other words, the voltage difference between the output of the converter and the mains:

$$V_{ripple,Lx}(\omega) = V_{xn}(t) - V_{grid,x}(\omega) \tag{4.26}$$

Where $x = a, b, c$ are the three phases of the grid connection of the multiport converter. This approximation allows for the calculation of the current ripple in every switching cycle, and works independently of the modulation technique used and the topology. The switching cycle with the highest $V \cdot s$, which occurs during time ΔT, is selected as the point where the maximum current ripple is found and the duty cycle obtained. Hence, the necessary inductance is:

$$L_{f,conv} = V_{ripple,Lx}\frac{\Delta T}{\Delta I_{L,max}} \tag{4.27}$$

Where $\Delta I_{L,max}$ is the maximum allowed current ripple at the output of the converter. The second condition is that the $(m_f\text{-}x)^{th}$ harmonic is under the required limits. The necessary total inductance value in order to achieve a desired current harmonic $I_{g,h,Desired,initial}$ is obtained by using the following equation:

$$L_T = \frac{\omega_{res}^2 V_h}{\omega_h(\omega_h^2 - \omega_{res}^2)I_{g,h,Desired,initial}} \tag{4.28}$$

Where L_T is the total inductance of the LCL filter, ω_{res} the resonant angular velocity of the LCL filter, ω_h the angular velocity of the harmonic investigated, V_h the amplitude of the voltage harmonic and $I_{g,h,Desired,initial}$ the desired maximum current in the harmonic. The resonant angular velocity ω_{res} of the filter is selected between the two limits proposed by Lisserre [55], between ten times the modulation frequency and half the switching frequency, making the design for several options in this range.

Therefore, the current harmonic for the $(m_f\text{-}x)^{th}$ as well as any other harmonic can be found using Equation 4.28. V_h is obtained with the Fast Fourier Transform (FFT) analysis tool from Matlab suite. This allows for the simple calculation of the harmonic current for a defined value of L_t. $I_{g,h,Desired,initial}$ is set to be in accordance to the values found in Table 4.2. The first iteration is done with the converter working with the modulation index set in such a way that the voltage output is equal to the voltage grid (no load operation). The resulting inductance forces the converter to work with a different modulation ratio in order to achieve the nominal current output. The required output voltage is found as:

$$V_{ph} = \sqrt{V_{grid}^2 + (\omega_g L_T I_{o,nom})^2} \tag{4.29}$$

Once the necessary output voltage is found, the converter switching waveforms can be calculated again, as well as $V_{h=mf-2}$. The $(m_f\text{-}x)^{th}$ current harmonic can be found by using Equation 4.30:

$$I_{g,h} = \frac{\omega_{res}^2 V_h}{\omega_h(\omega_h^2 - \omega_{res}^2)L_T} \tag{4.30}$$

The difference between the obtained current harmonic and the initial one introduced in Equation 4.28 is used to modify the initial value of desired harmonic current. When the difference between the obtained current harmonic and the initial desired value is close to zero the iteration process is finished, and therefore the total inductance of the LCL filter is found.

As a result two values are already known: L_t and $L_{f,conv}$. It is possible to apply several relation value r to find the value of the two inductance, ranging from r=0.2 to r=1. The relation is defined as:

$$r = \frac{L_{f,g} + L_g}{L_{f,conv}} \tag{4.31}$$

Where L_g is the grid inductance which is part of L_T. The grid inductance is considered to be 80 µH [58] in this thesis. This is used to obtain the necessary value of the grid inductor $L_{f,g}$, as long as L_T, $L_{f,conv}$ and r can keep the relation. Otherwise, the design for the specified r is discarded. Several resonance frequencies can also be computed, and different results are obtained. The C_f capacitance value is obtained from the desired resonant frequency as:

$$C_f = \frac{L_t}{\omega_{res}^2 L_{f,conv}(L_{f,g} + L_g)} \tag{4.32}$$

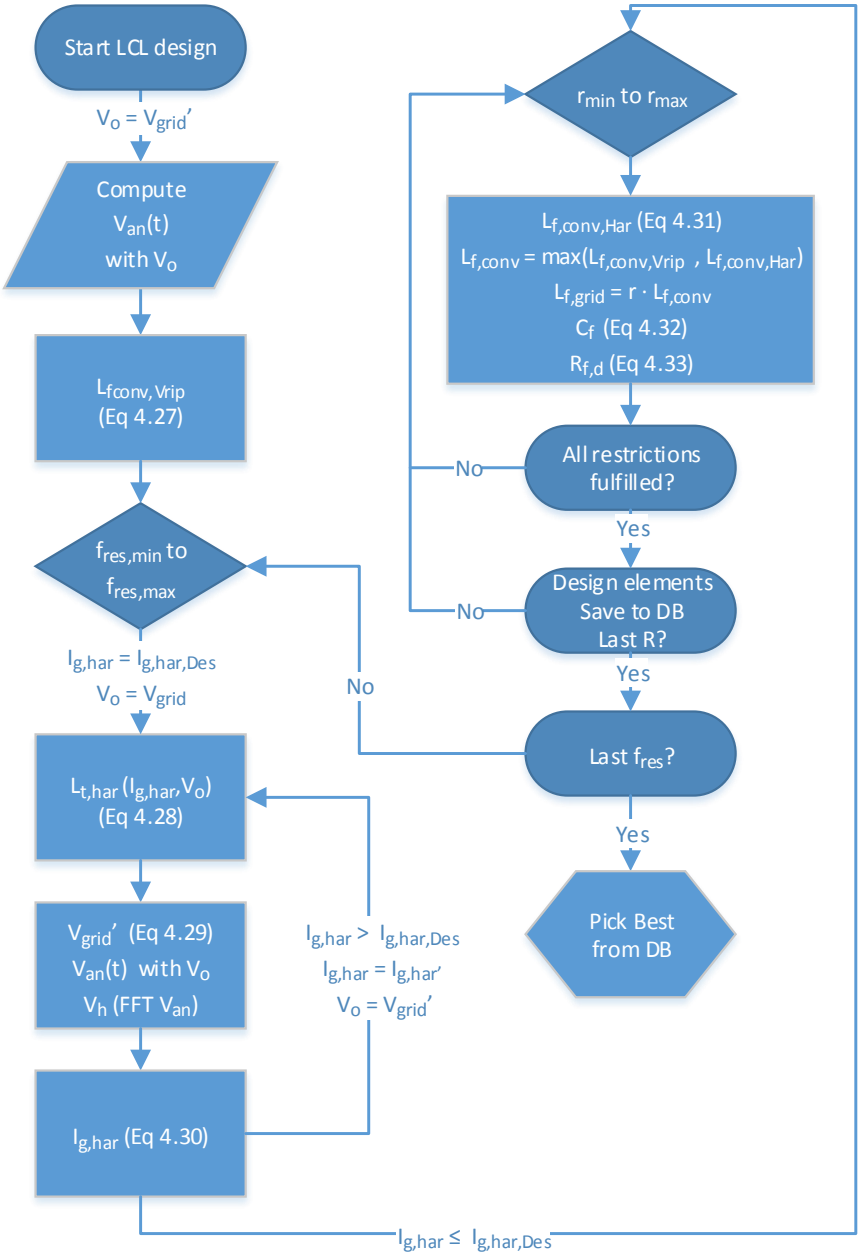


Figure 4.5: LCL filter design procedure

Finally, the required damping resistors $R_{f,d}$:

$$R_{f,d} = \frac{1}{3\omega_{res}C_f} \tag{4.33}$$

The losses for the different elements are obtained as explained previously in Section 3.1 for toroidal inductors. The inductor parameters are found by using the same design as in Section 4.3. The damping resistor losses consist of fundamental current losses and harmonics losses [60]:

$$P_{f,r,d} = 3I_c^2 R_{f,d}$$
$$P_{h,r,d} = \sum_{h=2}^{\infty} I_{g,h}^2 R_{f,d} \tag{4.34}$$

In this equations the different $I_{g,h}$ can be computed using Equation 4.30. The current through the capacitor, which is the same as the one through the resistors, considering that $R_{f,d} \ll Z_{C_f}$ is:

$$I_c = \frac{V_{C_f}}{Z_{C_f}} = \frac{\sqrt{V_{grid}^2 + (\omega_g (L_{f,g} + L_g) I_{o,nom})^2}}{\frac{1}{\omega_g C_f}} \tag{4.35}$$

With all this parameters it is possible to make the design for several resonant frequencies and relation values r. A diagram of the followed procedure to design the LCL filter is displayed in Figure 4.5 When the design is finished, the losses can be calculated and the design with the minimum cost can be selected as the definitive. The restrictions found in [55], which have already been listed in this section, also apply and therefore have to be used to discard possible design solutions that might be found using this method.

4.9. Heat sink design

A lot of effort has been performed in the last years to increase the power density of power electronic converters, while keeping the efficiency high [61]. All passive elements of the previous sections play a role in the final volume of the converter, but at high powers the amount of energy that has to be dissipated is very high, increasing the cooling effort [62]. Different systems including air forced cooling and water cooling have been used for Switched Mode Power Supplies (SMPS). In this comparison work only air forced cooling is considered due to their simplicity and relatively high performance.

The design of the heat sinks can be point of load optimized [63] [64] and lower thermal resistivity of the heat sink can be achieved, for example using copper instead of aluminum, at a higher price. However, the resulting designs are most times very expensive to manufacture and experimental results tend to be lower than the theoretical values achieved with the analytical design. Other researchers have investigated methods to design high performance heat sinks while keeping the costs and manufacturing complexity relatively low [65] [66].

Commercially available air forced heat sinks usually have a low performance. The performance evaluation of the heat sinks can be done with a simple equation known as Cooling System Performance Index (CSPI) [63]. This index can be used to evaluate the power dissipation density or the performance per volume of a cooling device, and it is computed as:

$$CSPI = \frac{1}{R_{th,S-a} V_S} \tag{4.36}$$

Where $R_{th,S-a}$ is the thermal resistance of the heat sink to the ambient in kelvin degrees over watts and V_S the volume of the cooling system in liters. As a result, the CSPI units are $[W(K \cdot l)^{-1}]$. If this parameter is evaluated for commercially available heat sinks, whose datasheets give both the thermal resistance and the volume including the fan, it is around 4 and 7 for common power electronic heat sinks. In the cited literature [63] [64] some prototypes have been built which achieve CSPIs of 18 and 31 for aluminum and copper heat sinks respectively, which is a major improvement with respect to market solutions. Other works [67] [68] achieve CSPIs of 23 and 21, but they are academic work and therefore the cost of the resulting heat sinks is prohibitive.

In order to make an accurate estimation of the heat sink size and to be fair with the different topologies, the same CSPI will be considered for all necessary heat sinks. Considering the previously gathered data, it is believed that a CSPI of 10 can be achieved with a custom design that can be relatively easy manufactured. Therefore, the cooling system volume is derived from Equation 4.36:

$$V_S = \frac{1}{R_{th,S-a,req} CSPI} \tag{4.37}$$

Where $R_{th,S-a,req}$ is the maximum required thermal resistance of the system. The thermal resistance is found with the equivalent model of the heat sink, where all the semiconductors are attached, see Figure 4.6. The model consists of the power dissipated by each element $P_{d,n}$, the different junction to case thermal resistances $R_{th,j-c}$ which are device specific, the $R_{th,c-S}$ which is the thermal resistance of the electrical isolating pad between the case of the semiconductor and the heat sink, the previously mentioned $R_{th,S-a,req}$ and the ambient temperature which is considered to be 45 degrees.

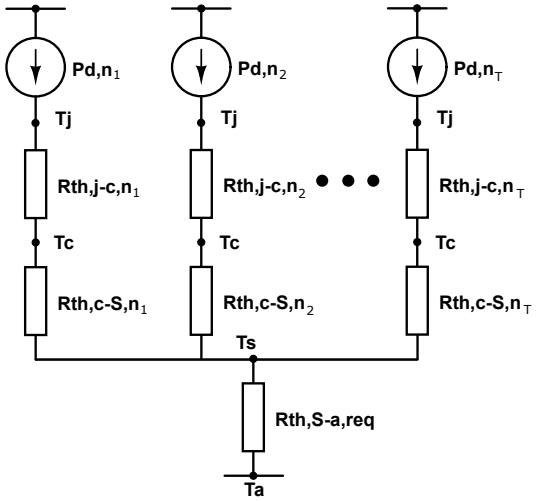


Figure 4.6: Equivalent thermal circuit model of the cooling system

The $R_{th,c-S}$ is due to the fact that a pad has to be inserted between the semiconductor and the heat sink for two reasons. First of all, the contact between the case surface and the heat sink surface must be as free of air as possible, because air is a very good thermal insulator. Considering that the surfaces are not completely flat because of the material properties, a material that fills all the gaps and has a high thermal conductivity must be applied between both. Thermal grease is the most common contact material that has been used in many applications. However, another restriction applies: the semiconductor must be electrically isolated from the heat sink in case they are not electrically paralleled and they have the same voltages, which happens in most cases. Therefore, a material with high thermal conductivity and high electrical resistance is needed for that matter. A very efficient and relatively new to the market option is to use phase change materials such as the Hi-Flow 300P from BERGQUIST. This material changes the phase at 55ºC, resulting in a better thermal contact of both semiconductor and heat sink. Additionally, it has an inner layer of polyimide film which acts as a dielectric, ensuring electrical isolation between the different semiconductors. The thermal resistance of this product is 0.94 ºC/W at 25 psi, obtained from the manufacturer datasheet. It is used for the attachments of all devices.

The necessary $R_{th,S-a,req}$ is obtained via the heat sink temperature T_S, the ambient temperature T_a and the total power that needs to be dissipated by the cooling system $P_{d,t}$:

$$R_{th,S-a,req} = \frac{T_S - T_a}{P_{d,t}} \tag{4.38}$$

$P_{d,t}$ is known from all the losses in the power converter. T_S is calculated from the maximum temperature that the heat sink can reach and still keep all the junction temperatures of the different semiconductors at 100ºC maximum. Therefore, the maximum heat sink temperature T_s that each element would allow needs to be computed, and the minimum chosen in order to keep the temperatures within limits. It can be also derived from the thermal model on Figure 4.6:

$$T_s = min(T_{j,max} - P_{d,n}(R_{th,j-c} + R_{th,c-S})) \tag{4.39}$$

With this information the $R_{th,S-a,req}$ is obtained and therefore the total volume of the cooling system too, using Equation 4.37. It is important to notice that the junction temperature $T_{j,n}$ of the elements with lower dissipation (assuming constant $R_{th,j-c} + R_{th,c-S}$) will be under the estimated $T_{j,max}$, therefore reducing the losses of those components. An iterative method that calculates the losses in the most demanding point of the converter assuming junction temperatures, then computes the necessary heat sink and finally obtains the junction temperatures is used. This process is repeated until the difference between the previous temperature and the new one is under 1ºC, which is accurate enough and rapidly achieved, reducing computing time. Once the heat sink size is known, the same process is applied in every operating point in order to find each T_j accurately.

This approach also shows how equally distributed losses in all the power semiconductors result in a higher utilization of the heat sink and therefore a more compact design. Topologies that have concentrated losses in certain semiconductors score lower because a bigger cooling system is needed.

The junction temperature is desired to be 100ºC maximum, well under the maximum of SiC devices, which is 150ºC for most manufacturers. This improves the reliability of the converter and easies the cooling of the converter. However, in some topologies, it will be seen how keeping $T_{j,max}$ under a hundred degrees is impossible or results in a really low power density. In order to have a working design, two possibilities exist: the CSPI of the cooling system is increased or the maximum acceptable junction temperature $T_{j,max}$. However, this options are not considered in order to evaluate the different topologies in equal conditions.

4.10. Conclusion

In this chapter the different components that the candidate topologies used have been listed and their design method or selection method have been explained. This methods are used for all the components of all the converters reviewed in the following chapters of the thesis. The chapter also includes the LCL filter design method which is used in the DC-AC converter topologies of Chapter 7 and 8.

5

PV Port Analysis

In this chapter the three different non-isolated DC-DC candidates listed in Section 2.3.1 are analyzed and rated. The three converters are the Interleaved Boost Converter (IBC), found on Section 5.1, the Coupled Inductors Interleaved Boost Converter (CIIBC) which is explained on Section 5.2, and finally the Three Level Boost Converter (TLBC), which is studied on Section 5.3. The PV port must meet following requirements:

- 350 V - 700 V 10 kW 30 A max input
- Maximum Power Point Tracking (MPPT)
- Low input ripple
- Input current ripple peak to peak <5%
- Input voltage ripple peak to peak <0.25%

5.1. Interleaved Boost Converter

The IBC consists of two or more interleaved boost converters, where the number of switches, diodes and inductors is equal to the number of phases N that form the converter. The IBC topology is represented in Figure 5.1 for surveyability. The number of capacitors is the same as in the conventional step-up dc-dc converter topology.

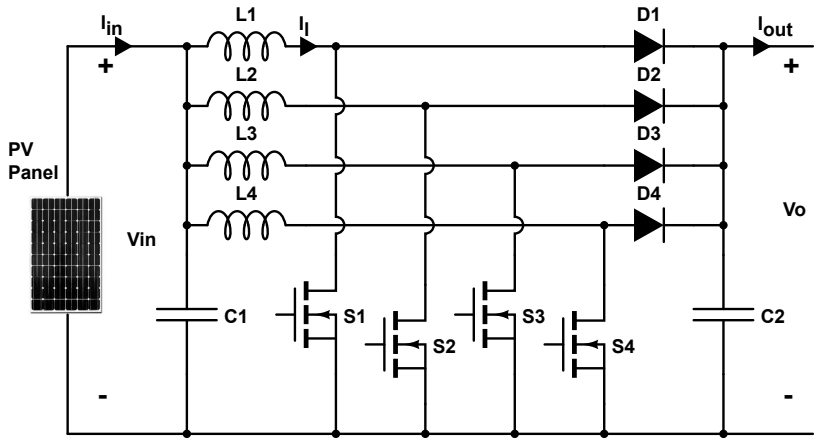


Figure 5.1: Structure of a four phases IBC

The interleaving in boost converters has many advantages. The most interesting of them is the reduction of the sharing of the current between the phases. Moreover, the input current ripple is reduced [18] when keeping the same inductance values, or the net volume of the inductors if the input current ripple is a constraint, as in this report. The output voltage ripple and the RMS current in the different elements is reduced. Thus, conduction losses are decreased and the capacitance values too. In this section the IBC is studied thoroughly, following the next steps:

1. Current waveforms derivation
2. Magnetic elements design
3. Input and output capacitor sizing
4. Switches and diodes requirements
5. Cooling system sizing

5.1.1. Converter design

Current waveforms derivation

The IBC operates with pulse width modulation and a constant frequency in all operating points. The duty cycle or amplitude of the gating signals of the switches is modified in order to regulate the rate of the DC to DC conversion of the converter, in exactly the same way as the conventional boost converter. The output of the converter is fixed at 750 V, the DC link voltage, while the input voltage is regulated by modifying the duty cycle D in order to follow the Maximum Power Point (MPP) of the photovoltaic panels.

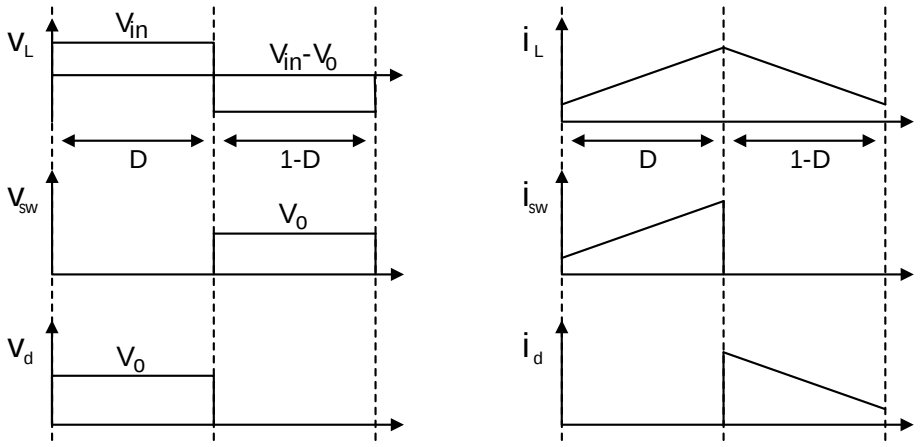
The gating signals of the phases are delayed by an angle of $\frac{2\pi}{N}$ for every phase. For example, in a two phases converter, the second phase is delayed 180º with respect to the first one. This results in an equivalent input and output current frequencies of Nf_{sw}. The peak values of the current through the inductors occur at different times of the main period, reducing the input current ripple.

When the switches are in the ON state, the current flows from drain to source the current in the inductor increases linearly. When the mosfets turn off, the diodes start conducting and the current through the inductor decreases due to the negative voltage applied to the inductor. Therefore, the switch conducts during the duty cycle $D \cdot T_s$ time and the diodes during $(1-D) \cdot T_s$. The input current is the sum of all the inductor currents of the different phases. This behavior is represented in Figure 5.2.

When the converters works in Continuous Inductor Conduction Mode (CICM), the duty cycle and increment of current from peak to peak in the inductor current are found using Equations 5.1. As the average inductor current is calculated by dividing the PV current into the number of interleaved phases $I_l = I_{in}/N$, only the equations for a simple boost converter need to be applied. With the different operating points, which compromise all the ranges of input voltage and input power, all the necessary current waveforms can be calculated. Therefore, the current through the inductor is computed as:

$$D = 1 - \frac{V_{in}}{V_{out}}$$
$$I_{l,pp} = \frac{V_{in}}{L} D T_{sw} \tag{5.1}$$

Where D is the duty cycle, V_{in} and V_o the PV and DC Link voltages respectively, $I_{l,pp}$ the peak to peak current in one inductor, L the inductance of the inductor and T_{sw} the switching period. To find the maximum and minimum values of the current through the inductor, the $I_{l,pp}$ is added and subtracted from I_l, respectively. On the other hand, when the peak to peak ripple current in the inductor is higher than the average current through the inductor, the converter works in Discontinuous Inductor Conduction Mode (DICM). In this mode, the switch conducts during the duty cycle time $D \cdot T_s$ and



(a) 3 phases, 500V, 50kHz (b) 4 phases, 500V, 50kHz

Figure 5.2: Voltage and current waveforms of the IBC in CICM

the diode during the time $D_2 \cdot T_s$, being $(D + D_2) < 1$. In order to do the calculations for the DICM the output current must be known, which can be computed from the output power in each phase, considered to be the same as the input power in an ideal converter [17]:

$$I_o = \frac{V_{in} I_{in}}{N V_o}$$
$$D = \sqrt{\frac{2 I_o L (V_o - V_{in})}{V_{in}^2 T_{sw}}} \tag{5.2}$$

Where I_o is the output current of one phase and N the number of phases. Then, the diode duty cycle D_2 and peak current $I_{l,peak}$:

$$D_2 = D \frac{V_{in}}{V_o - V_{in}}$$
$$I_{l,peak} = \frac{V_{in}}{L} D T_{sw} \tag{5.3}$$

In this case, the current in the inductor starts from zero and rises up to $I_{l,peak}$. In order to obtain the input i_{in} and output i_o current waveforms, the inductor currents i_l and diode currents i_d can be summed up, considering the delay of each phase of the IBC. The current in the switch and the diode, $i_{sw}(t)$ and $i_d(t)$ respectively, are also known as the time of conduction depend on D and D_2.

Size of inductors

The size of the inductors is calculated from the PV specifications, detailed in Section 2.1.1. As stated in [18], the following equation can be used in order to calculate the minimum inductance value of the required inductor for CCM:

$$L = \frac{V_o N}{f_{sw} I_{in,pp}} \left(\frac{floor(DN) + 1}{N} - D \right) \left(D - \frac{floor(DN)}{N} \right) \tag{5.4}$$

Where N is the number of phases of the IBC, D is the duty cycle, L the inductance value, V_o the output voltage (DC link voltage), f_{sw} the switching frequency and $I_{in,pp}$ the maximum permissible

input current ripple. $floor$ makes reference to floor rounding to the nearest integer. If this equation is normalized, considering the maximum ripple in the single phase topology as 100%, the resulting input current ripple for different duty cycles and different number of phases can be obtained. This is shown in Figure 5.3. It is clear that for the same inductor size the ripple is greatly reduced for two and three phases, but increasing to a higher number is not that beneficial.

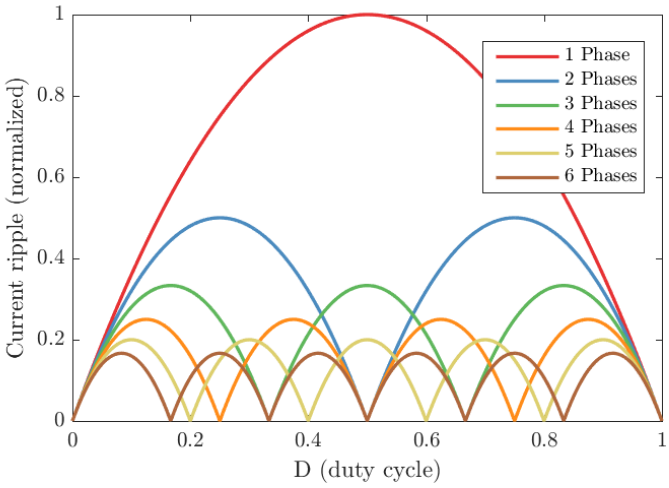


Figure 5.3: Input current ripple versus duty cycle for different levels of interleaving

From Figure 5.3 it is also important to notice that depending on the number of phases different points with zero input current ripple exist. This is the reason why it is important to evaluate the behavior of the IBC for the whole operating range. However, as PV panels can work in a wide voltage range (350 - 700 V), it does not make sense to optimize the number of phases for the lowest current ripple.

Size of capacitances

The input and output capacitance can be calculated from the current ripple in the different configurations. The previously specified requirements dictate that the input voltage ripple must be kept under the 0.25% of the PV voltage. The current ripples for every working condition of the converter are already known, as it is possible to compute the sum of the different inductor current waveforms for the input current and the diode current waveforms for the output current. The application of Equation 5.5 in the operating point with highest ripple results in the change of voltage produced in the capacitors:

$$V(t) = \frac{Q(t)}{C} = \frac{1}{C}\int_{t_0}^{t} I(t)dt + V(t_0) \tag{5.5}$$

Equation 5.5 can be rearranged in order to be a general approximation for the IBC, because the input current waveform is triangular with a DC offset. This results in the following equation:

$$C_{in} = \frac{1}{\Delta V_{in}} \cdot \frac{1}{2} \frac{1}{N \cdot f_{sw}} \cdot \frac{\Delta I_{in,pp}}{2} \tag{5.6}$$

Where C_{in} is the needed capacitance, ΔV_{in} is the maximum admissible voltage increment, N is the number of phases, f_{sw} is the switching frequency and $\Delta I_{in,pp}$ is the current increment peak to peak. The input current frequency is proportional to the number of phases N, making the necessary capacitor inversely proportional to the number of interleaved phases. This leads to a minimum value of the input capacitor, which will be shown later together with the values for the output capacitor. On the other hand, the output current waveform is not triangular, and the necessary capacitance is found

by using Equation 5.5 on the summed output current of all the phases, considering that the maximum difference between voltages of $V(t)$ must be kept under the limits.

Switches and diodes requirements

The voltage that the switches have to stand is the same as the output voltage of the converter, or in other words, the DC link voltage. The current through the switches follows the same waveform as the inductor current while the switches are on. The maximum current through the switches will happen at minimum voltage (350 V) and highest power of the converter (10 kW).

The voltage that the diodes have to stand is the full DC bus voltage, V_o. The current through the diode follows the same waveform as the inductor current while the switch is off. In other words, while the switch is conducting, the current through the diode is zero and the rest of the time follows the inductor current. This has been shown on Figure 5.2.

Efficiency Improvement

When the converter operates in DICM, the switch turns on at zero current. This reduces the switching turn on losses considerably, but they are not zero because of the parasitic capacitances. A Zero Voltage Switching (ZVS) approach is preferred when the aim is to reduce the switching losses. Several topologies have been derived from the conventional IBC in order to achieve soft switching, achieving a higher efficiency at the expenses of increasing the complexity of the circuit:

- CIIBC. Adding coupled inductors to the converter increases efficiency. This converter will be the next one analyzed in this report.
- Interleaved Soft Switching Boost Converter (ISSBC) [69]. One resonant inductor, two capacitors and two diodes are added to every phase of the IBC in order to achieve soft switching using resonance. However, it increases the voltage stresses in the switch by around 20%, which might result in a more expensive switch being necessary. Moreover, the additional circuit is built one per phase, without taking advantage of the interleaved topology.
- Zero Voltage Switching Interleaved Boost Converter (ZVS-IBC)[70]. The diodes are replaced by switches, parallel capacitors are added to all switches and a resonant LC network is connected between every two phases. All mosfets in the converter are turned on at zero voltage and turned off at nearly zero current, considerably reducing the switching losses. The increase in efficiency is demonstrated, but the number of driving circuits is doubled and an extra inductor has to be built for every phase.
- ZVS-IBC [71]. A parallel capacitor is added to every switch and an inductor connected every two phases. ZVS is achieved without increasing the necessary rating of the switches. The increment of efficiency is proved, but it largely depends on the extra inductor attached to the circuit, where a lot of current circulates.
- Passive lossless snubber [72]. A snubber circuit consisting of three diodes, two capacitors and one inductor is attached to every phase. This improves the turn on and turn off transients, but increases the circuit complexity and the size of the converter.

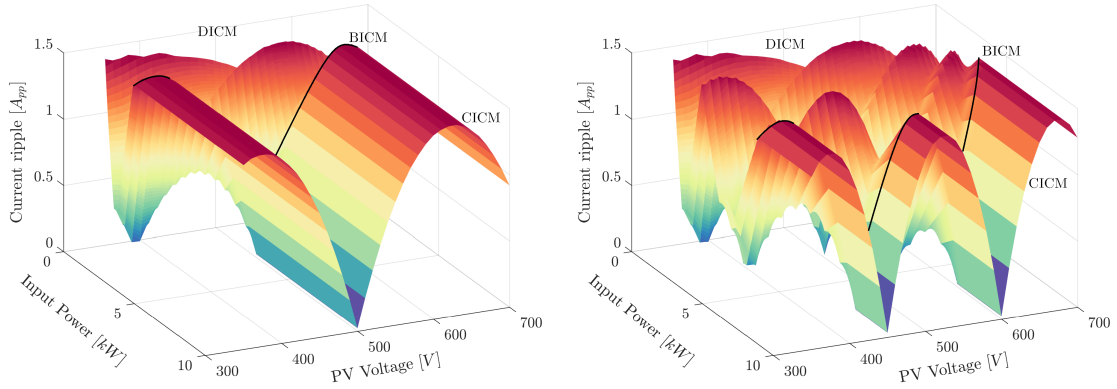
The different options show that adding extra circuitry to the converter allow for increasing the efficiency. The single phase targeted options are not as attractive as the ones which are connected between two phases, reducing the amount of components. However, an even number of phases is necessary for its implementation, reducing the options and increasing the complexity. There are options to increase the efficiency of the converter, parameter which is evaluated in order to rate the performance of each topology in the multiport converter. A grade of 3 has been selected for the converters with even number of phases and a rate of 2 for the converters with odd number of phases in the efficiency improvement criterion.

Controllability

The IBC is controlled via the Pulse-Width Modulation (PWM) technique, as the single phase boost converter. A rating of five would be given to the single phase option. Therefore, a rating of four is given to the interleaved version as increasing the phases does slightly increase complexity in terms of control, as the phase displacement must be accurately controlled in order to have optimum current sharing between the phases. From the gate drivers point of view complexity increases with every additional switch, but this fact is reflected in the rate related to the number of switches. This topology also improves the dynamic behavior of the converter, as the increased equivalent frequency results in faster changes at the input.

5.1.2. Results

As previously stated, the input current ripple when using a higher number of phases has different values compared to when the inductor has a low number of legs and thereby it works in CICM. The input current ripple behavior is represented in Figure 5.4 for three and five phases to show the difference.



(a) 3 phases

(b) 5 phases

Figure 5.4: Input current ripple versus input voltage and power for different levels of interleaving

The input current ripple when the converter is in CICM follows the same trace as what has been shown in Figure 5.3. As the number of phases is increased the number of operating points in DICM also increase due to lower currents, changing the pattern. Figure 5.4 demonstrates how the maximum ripple is the same for both conduction modes, eliminating the need of increasing or decreasing the necessary inductance when the converter works mostly in one mode or the other.

The design is performed for a range of one to six interleaved phases, for 50 kHz and 100 kHz. The design procedure has been previously explained in Chapter 4. The results are shown in Table 5.1, where V_{conv} is the final volume of the converter. The designs for one and two phases do not have working inductors which fit in a PCB; therefore, they are not considered further on. This is due to the high currents that the bobbin would have to support, together with a high inductance that make it impossible to fit a certain number strands while keeping the resistance of the copper low.

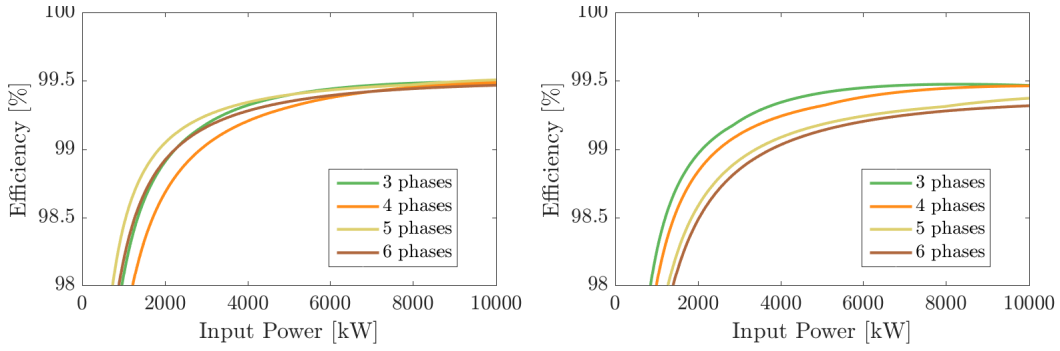
Table 5.1 shows how the necessary inductance is reduced with increasing number of phases, and thus the necessary core size. The results show that doubling the switching frequency halves the necessary inductance, usually involving a smaller core size. The selected mosfets for are equal for three and four phases and for five and six phases. The mosfets for low number of phases have lower conduction losses and higher switching losses with respect to the selected ones for five and six phases, resulting in lowest possible losses.

Table 5.1: Design values of the IBCs.

	50 kHz				**100 kHz**			
Phases	3	4	5	6	3	4	5	6
L [mH]	0.874	0.656	0.5227	0.437	0.437	0.328	0.261	0.218
Core	E65	E65	E55	E55	E55	E55	E42	E42
Material	3C92	R	R	R	3C92	R	3C92	3C92
N	45	38	40	40	35	32	37	37
l_g [mm]	0.786	0.746	0.679	0.813	0.622	0.693	0.586	0.701
R_{ac} [Ω]	0.042	0.031	0.048	0.049	0.038	0.031	0.048	0.048
C_{in} [uF]	0.688	0.515	0.415	0.348	0.344	0.258	0.208	0.174
C_{out} [uF]	8.230	2.911	2.755	2.162	4.115	1.456	1.378	1.063
Mosfets	40 A$^{\triangle}$	40 A$^{\triangle}$	12.5 A$^{\triangle\triangle}$	12.5 A$^{\triangle\triangle}$	12.5 A$^{\triangle\triangle}$	12.5 A$^{\triangle\triangle}$	12.5 A$^{\triangle\triangle}$	12.5 A$^{\triangle\triangle}$
Diodes	25.5 A*	20 A **	20 A**	20 A**	20 A**	14 A$^{\diamond}$	14 A$^{\diamond}$	11 A$^{\diamond\diamond}$
V_{conv} [dm^3]	0.431	0.489	0.384	0.425	0.550	0.421	0.297	0.314

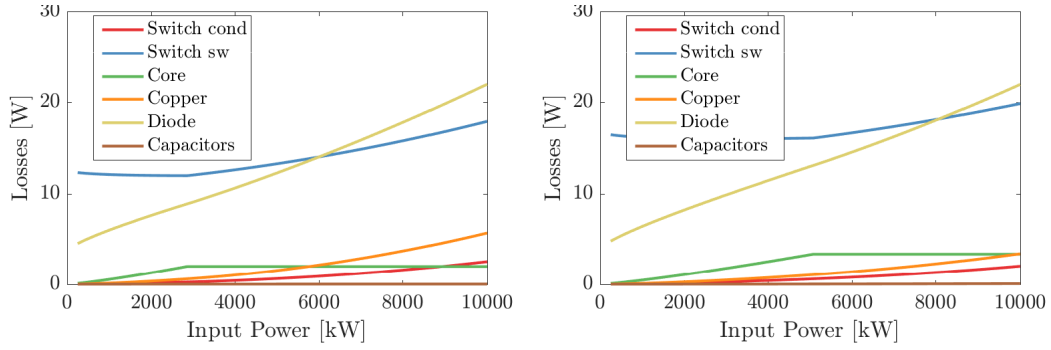
$^{\triangle}$ Cree C2M0040120D * Cree C4D20120A $^{\diamond}$ Cree C4D10120A

$^{\triangle\triangle}$ Cree C2M0160120D ** Cree C4D15120A $^{\diamond\diamond}$ Cree C4D08120A



(a) 500V, 50kHz (b) 500V, 100kHz

Figure 5.5: Efficiency versus input power for different levels of interleaving



(a) 3 phases, 500V, 50kHz (b) 4 phases, 500V, 50kHz

Figure 5.6: Losses versus input power for 3 and 4 phases at 500V

The resulting efficiency is shown for two different frequencies in Figure 5.5. The three phases option perform similarly to the five or six phases option. The four phases IBC uses the same switch as the three phases one, increasing more the switching losses than the reduction in conduction losses, because the R_{ds} is already low. At 100 kHz the efficiency is reduced, while the core size is only reduced in the 3 phases case, from an E65 to an E55.

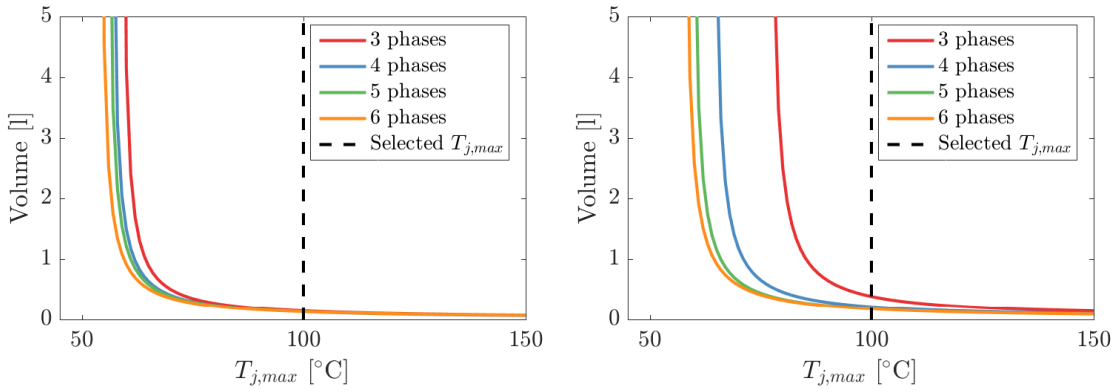
Figure 5.6, where the losses of the different components have been plotted, shows how switching losses increase with the number of phases. While the converter is in DICM, the switching losses are more or less constant and afterwards they increase exponentially. Mosfet conduction losses are slightly reduced because the current per phase goes down by 25%, but they are already low. The core losses of the converter increase linearly when the converter operates at DICM, because the ripple current in the bobbin increases with the duty cycle. Core losses are higher in the four core configuration because the ripple currents are higher. Copper losses and diode losses are reduced because of the current sharing of the interleaved converter. Capacitor losses are low due to the low current ripple of the topology.

The weighted efficiency of the converters, obtained using the method described in section 3.2, is shown in Table 5.2.

Table 5.2: Weighted efficiency of the IBCs.

	50 kHz				**100 kHz**			
Phases	3	4	5	6	3	4	5	6
Efficiency	99.18	99.04	99.27	99.18	99.22	99.13	98.96	98.88

The highest efficiency is obtained by a six phases converter working at 50 kHz. When the losses are known, it is possible to obtain the necessary cooling system size of the converter to keep the maximum junction temperatures $T_{j,max}$ under a certain limit. Figure 5.7 shows the necessary heat sink size for a different number of phases considering different maximum values of junction temperature for 50 and 100 kHz versions. At low temperatures a higher number of phases has a better performance due to the lower differences between the maximum temperature junctions of the mosfets and diodes. However, increasing the number of phases has no positive effect in the established $T_{j,max}$ for the 50 kHz version, resulting in a similar cooling system volume, while in the 100 kHz version the 3 phases converter needs a higher volume.

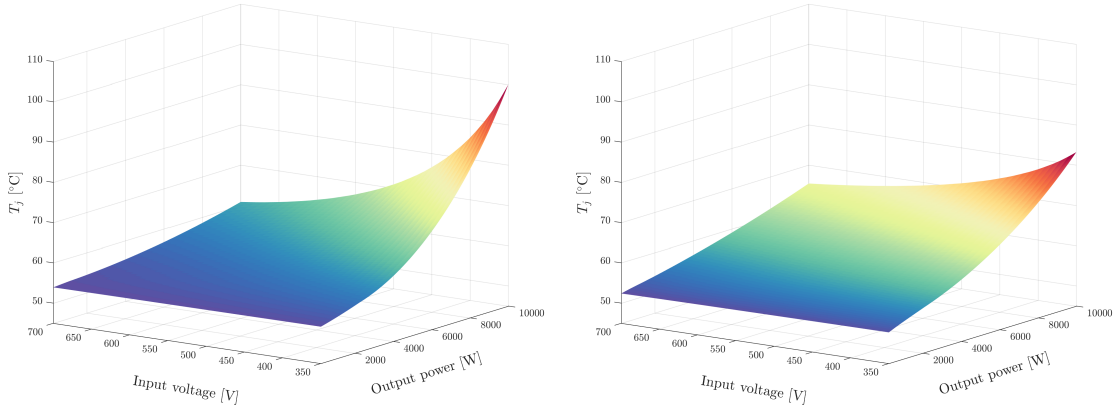


(a) 50 kHz (b) 100 kHz

Figure 5.7: IBC cooling system size for different values of $T_{j,max}$

The junction temperatures of the different elements are also known for every operating point.

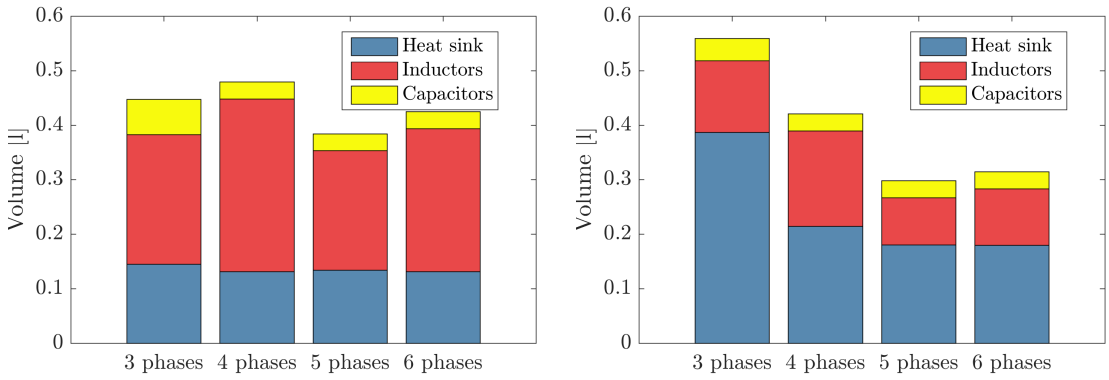
Figure 5.8 shows how the cooling system selected keeps temperatures under the pre-defined $T_{j,max}$. The 3 phases 100 kHz IBC is selected as an example because the significant difference between the maximum mosfet temperature and the highest diode temperature makes the cooling system bigger than if the two temperatures were closer, as seen in Figure 5.9(b).



(a) $T_{j,mosfets}$ (b) $T_{j,diodes}$

Figure 5.8: Junction temperatures of IBC (3 phases 100 kHz example)

The volume of the different configurations, which is calculated from the heat sink size, the inductors size and the capacitors size is shown in Figure 5.9. The plots also show how inductor sizes are reduced when increasing the switching frequency. However, the higher losses of the switches, make the final converter size equal to the 50 kHz option due to bigger cooling system needs.



(a) 50 kHz (b) 100 kHz

Figure 5.9: Volume of the different possible configurations of the IBC

5.1.3. Converter evaluation

Both the complexity increase and reduction of efficiency and reliability in five and six branches overshadow the possible size reduction because of the smaller cores used. Table 5.3 shows the grading of the different converters considered in this section, which results in a total score.

The most interesting converter is the 3 phases IBC at 50 kHz which scores 82 points. The efficiency is similar in all the configurations, but it uses a lower number of switches, diodes and inductors, resulting in a higher score. The converters at 100 kHz have more losses, resulting in lower efficien-

Table 5.3: Evaluation of the IBC.

Freq. [kHz]	Weight	50				100			
Phases	-	3	4	5	6	3	4	5	6
Num. Switches	3	4	3	2	1	4	3	2	1
Num. Diodes	1	4	3	2	1	4	3	2	1
Num. Cores	3	4	3	2	1	4	3	2	1
Capacitors	1	5	5	5	5	5	5	5	5
Efficiency	5	4	4	4	4	4	4	3	3
Volume	5	4	3	4	2	2	4	5	4
Eff. Improve	1	2	3	2	3	2	3	2	3
Controlability	3	4	4	4	4	4	4	4	4
TOTAL		**82**	**76**	**73**	**57**	**77**	**81**	**73**	**62**

cies and big volumes due to the cooling system. The 100 kHz 4 phases version also scores more than 80 points, so it could be selected if the efficiency wants to be increased.

5.2. Coupled Inductors - Interleaved Boost Converter

The Coupled Inductors Interleaved Boost Converter (CIIBC) [3] consists of two or more interleaved boost converters, where the number of switches and diodes is equal to the number of phases that form the converter. The inductors in this topology are coupled, with two or more inductors sharing the same core. The CIIBC topology is represented in Figure 5.10 for the sake of completeness. In this figure the inductors are coupled in pairs. The number of capacitors is the same as in the conventional step-up dc-dc converter topology.

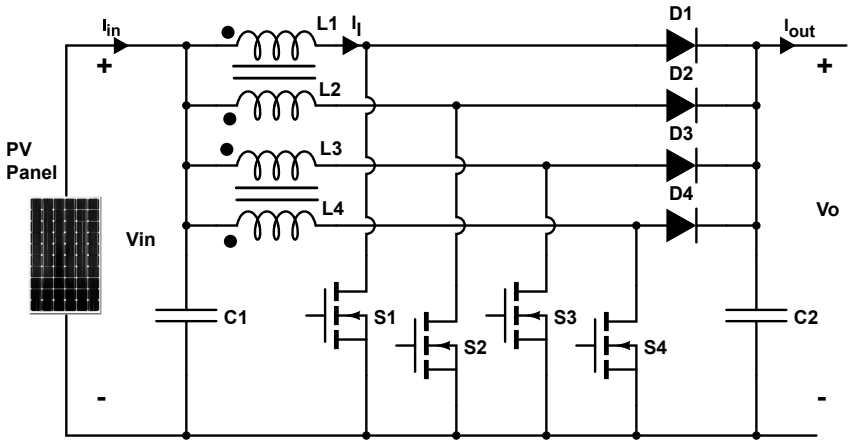
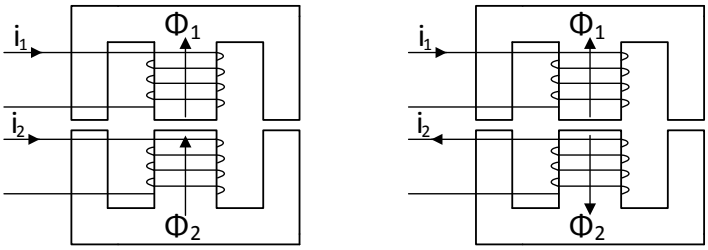


Figure 5.10: Structure of a four phases CIIBC

The coupling of the inductors can be performed in two different manners, depending on the current direction of the coils, as shown in Figure 5.11. Direct coupling technique makes the fluxes in the core sum each other, while when using inverse coupling fluxes have opposite directions and cancelate. Compared to the direct coupling configuration, reverse coupling provides the advantages of lower

inductor ripple current and very low DC flux in the core. Direct coupling provides the advantages of lower input ripple current and AC flux level see Table 5.4. Therefore, the AC flux-density dependent core losses would be higher in an inverse-coupled converter whereas the winding loss would be higher in a direct-coupled converter. Magnetic saturation due to dc flux is a greater design challenge with direct coupled converters, making reverse coupling more suitable in high power applications.



(a) Direct coupling (b) Inverse coupling

Figure 5.11: Coupling configurations in an E core

Table 5.4: Direct coupling and reverse coupling behavior.

Coupling	$I_{l,pp}$	$I_{in,pp}$	L (fixed $I_{in,pp}$)
Direct	+	-	-
Inverse	-	+	+

Only pairs of coupled inductors are considered for the comparison process, as seen on Figure 5.10. There has been some research on triple coupled inductors [73], but the design and build complexity of this inductors has been demonstrated to be much harder than conventionally coupled inductors. Moreover, current waveforms are much harder to predict. Thus only two, four and six phases topologies are considered. The following aspects are analyzed of the CIIBC:

1. Current waveforms derivation
2. Magnetic elements design
3. Input and output capacitor sizing
4. Switches and diodes requirements
5. Cooling system sizing

5.2.1. Converter design

Current waveforms derivation

The equations that describe how the coupling of the inductors affect the equivalent inductance and thus, the ripple in the inductor, have been derived only for CICM, and can be found in Appendix D. The equations for DICM have been obtained from Professor B. Ray work in the CIIBC [3]. Only the basic theory behind the coupled inductors configuration is reviewed in this section in order to give a general overview of the advantages and disadvantages; for more information please refer to Appendix D and [3]. The voltage drop on the inductor depends on the self-inductance L and the mutual inductance M, and the voltage produced by them is directly proportional to the change rate of the current in both inductors:

$$V_1 = L\frac{di_1}{dt} + L\frac{di_2}{dt}$$
$$V_2 = M\frac{di_1}{dt} + L\frac{di_2}{dt} \tag{5.7}$$

Current waveforms in the CIIBC depend on the coupling coefficient of the windings k ($\frac{M}{L}$), which is assumed positive for direct coupling and negative for reverse coupling. The coupling of the windings depends on the amount of generated flux of one inductor that flows through the other one and it depends on core geometry and construction. The corresponding inductor ripple current ratio between inverse $I_{L,rip,inv}$ and direct-coupling $I_{L,rip,dir}$ configurations [74] for a certain coupling factor is given by:

$$\frac{I_{L,rip,inv}}{I_{L,rip,dir}} = \frac{1 - \frac{1-D}{D}k}{1 + \frac{1-D}{D}k} \tag{5.8}$$

Therefore, the inductor ripple current for the inverse-coupling configuration is always less than the direct-coupling configuration. On the other hand, the input ripple current ratio between two coupling configurations is given by:

$$\frac{I_{In,rip,inv}}{I_{In,rip,dir}} = \frac{1+k}{1-k} \tag{5.9}$$

This equations show how a trade-off must be made. While direct-coupling reduces the input ripple making the need for filtering smaller, inverse coupling considerably reduces the current ripples in the inductors and thus the losses are reduced.

The equations that describe how the coupling of the inductors affect the equivalent inductance and the ripple in the inductor have been derived only for CICM and can be found in Appendix D. The equations for DICM have been obtained from [3], where a detailed analysis of the converter can be found. However, the research work from Professor Ray misses one DICM of the converter, which has been denoted as DCM3, and can be computed using Equations 5.10. In this mode of operation no currents are present in both inductors at the same time, making the converter operate as the IBC in the DICM.

$$I_o = \frac{V_{in}I_{in}}{NV_o}$$
$$D = \sqrt{\frac{2I_oL(V_o - V_{in})}{V_{in}^2 T_{sw}}}$$
$$D_2 = D\frac{V_{in}}{V_o - V_{in}} \tag{5.10}$$
$$I_{l,peak} = \frac{V_{in}}{L}DT_{sw}$$

Size of inductors

The size of the inductors is calculated from the PV specifications, explained in Section 2.1.1 inside the Section Requirements of the system. The input current ripple is obtained with Equation 5.11, which is a modification of the one found in [18], taking into account the coupling factor. This equation can be used in order to calculate the minimum value of the required inductor as long as the converter stays in CICM:

$$L = \frac{V_oN}{f_{sw}I_{pp}}\left(\frac{floor(DN)+1}{N} - D\right)\left(D - \frac{floor(DN)}{N}\right)\frac{1}{k+1} \tag{5.11}$$

Where N is the number of phases of the CIIBC. The only difference with respect to the IBC is the last factor, which depends on k, the coupling factor. Derivation of this equation can be found in Appendix D.

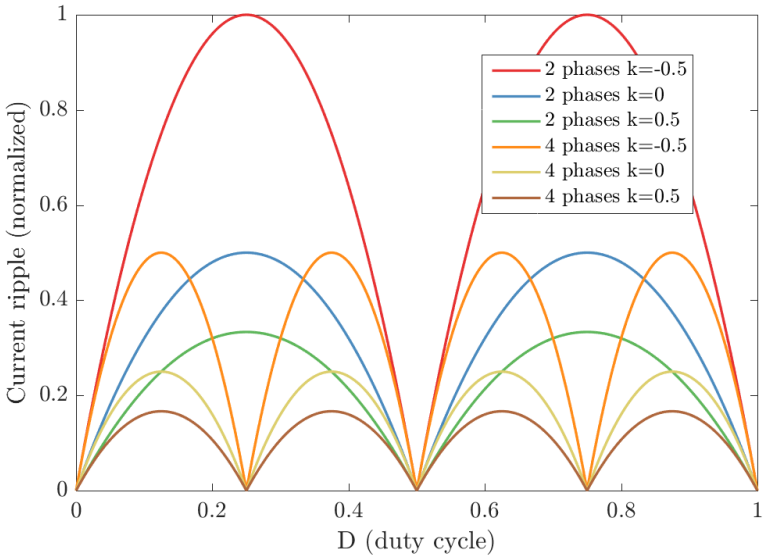


Figure 5.12: Input current ripple versus duty cycle for different levels of interleaving

Figure 5.12 shows how direct and inverse coupling affect the input current ripple for different levels of interleaving. No coupling, which happens when $k = 0$, is found in the plot for comparison purposes. However, these plots are only valid for CICM, giving incorrect results the deeper the converter goes into DICM. The figure shows how with a coupling factor of -0.5 the input current ripple for the two phases converter is the same as for the conventional boost converter (normalised to one), while a positive coupling factor of 0.5 halves the input current ripple with respect to the two phases IBC, shown in Figure 5.3.

Size of capacitances

The size of the input capacitance C_{in} can be obtained in a similar way as the method used in the IBC section, see Equations 5.12.

$$C_{in} = \frac{1}{\Delta V_{in}} \frac{1}{2} \frac{1}{N f_{sw}} \frac{\Delta I_{in,pp}}{2} \tag{5.12}$$

Where ΔV_{in} is the maximum admissible voltage increments, N is the number of phases, f_{sw} is the switching frequency and $\Delta I_{in,pp}$ is the current increment peak to peak. The application of this equation in the working condition with a higher input and output current leads to a minimum value of both capacitors. On the other hand, the output current waveform is not triangular, and the necessary capacitance is found by using Equation 5.13 on the summed output current of all the phases, considering that the maximum difference between voltages of $V(t)$ must be kept under the limits.

$$V(t) = \frac{Q(t)}{C} = \frac{1}{C} \int_{t_0}^{t} I(t)dt + V(t_0) \tag{5.13}$$

Switches and diodes requirements

The minimum breakdown voltage that the switch has to have is the output voltage V_o of the converter, or in other words, the DC link voltage. This maximum voltage rating occurs when the converter works

in CICM. When the low input power makes the converter work in DICM, the drain-source voltage at the terminals of the mosfet is reduced and depends on the operation mode of the converter, the coupling factor and the voltage gain $G = \frac{V_o}{V_{in}}$ of the converter [3], see Table 5.5.

Table 5.5: Switch turn on voltage $V_{ds,on}$ values of the CIIBC [V] [3].

D ≤0.5				D ≥0.5	
CCM-1	DCM-1	DCM-2	DCM-3	CCM-2	DCM-4
V_o	$V_o \frac{1-k+kG}{G}$	$V_o \frac{1-k+kG}{G}$	V_o	V_o	$V_o \frac{1-k}{G}$

The current through the switches follows the same waveform as the inductor current while the switches are on. The maximum current through the switches will happen at minimum voltage (350 V) and highest power of the converter (10 kW).

The maximum reverse voltage applied to the diodes is the full DC bus voltage, V_o, when the converter works in CICM. The turn off voltage of the diodes also depends on the coupling factor and voltage gain for the different DICMs of the converter, see Table 5.6 [3].

Table 5.6: Diode turn off voltage $V_{d,on}$ values of the CIIBC [V] [3].

D ≤0.5				D ≥0.5	
CCM-1	DCM-1	DCM-2	DCM-3	CCM-2	DCM-4
V_o	$V_o\left(1-k-\frac{1-k}{G}\right)$	$V_o\left(1-\frac{1-k}{G}\right)$	V_o	V_o	$V_o\left(\frac{1-k}{G}-1\right)$

The current through the diodes follows the same waveform as the inductor current while the switches are off. In other words, while the switch is conducting, the current through the complementary diode is zero and the rest of the time follows the inductor current.

Efficiency Improvement

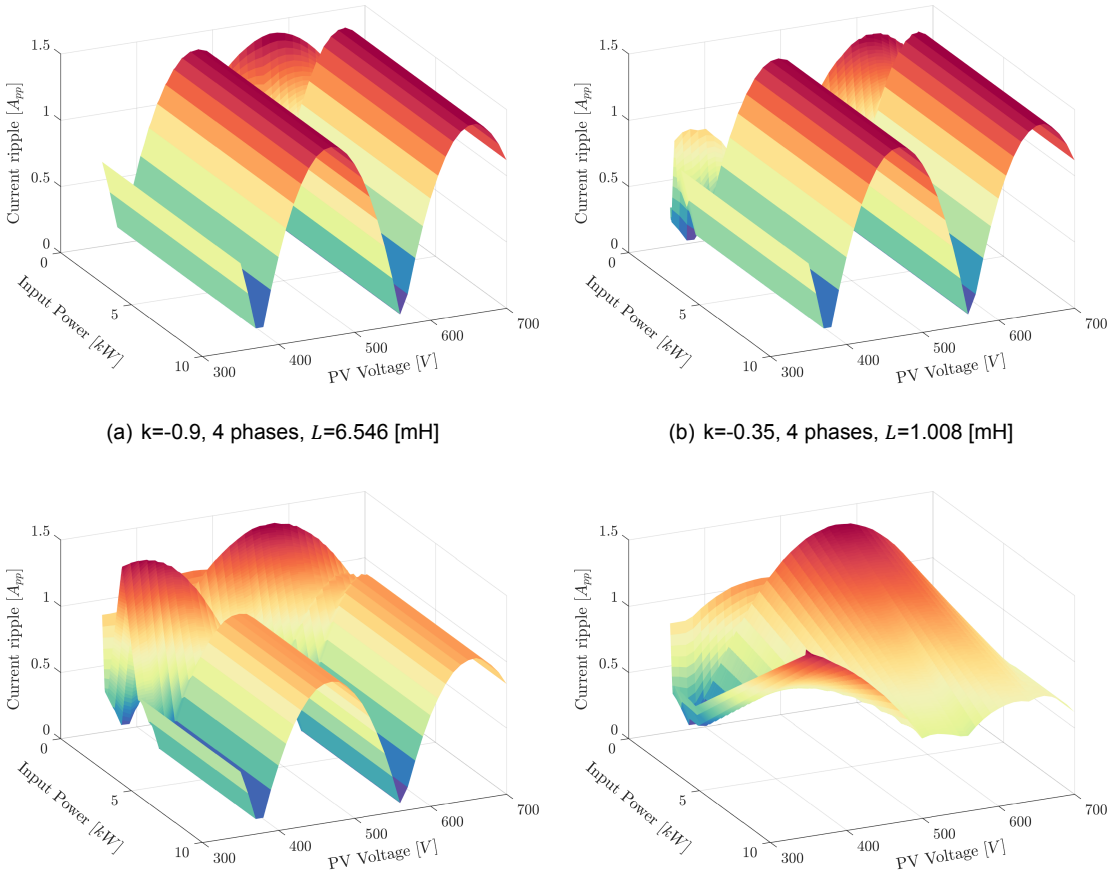
The same methods as those presented in Section 5.1.1 apply of the CIIBC, although the efficiency is already boosted with the use of coupled inductors.

Controllability

In terms of controllability the CIIBC performs similarly to IBC. It has better stability because coupled inductors help stabilize current differences between phases, making the control less problematic.

5.2.2. Results

The design considerations presented in Section 4.2 have been applied for the design of coupled inductors of the CIIBC. More information can be found in Appendix B. The input current ripple behavior is represented in Figure 5.13, where coupling factors of 0.35 and 0.9 both in direct coupling and inverse coupling have been used for this representations in order to make the comparison. The necessary inductance has been selected in such a way that the maximum current ripple is kept within limits, even in DICM. This means that in Figure 5.13 different inductance values are used in order to meet the requirement of maximum input current ripple.



(a) k=-0.9, 4 phases, L=6.546 [mH]

(b) k=-0.35, 4 phases, L=1.008 [mH]

(c) k=0.35, 4 phases, L=0.656 [mH]

(d) k=0.9, 4 phases, L=0.679 [mH]

Figure 5.13: Input ripple in the CIIBC for 4 phases and different coupling factors

In Figure 5.13 behavior of direct coupling and inverse coupling can be observed. Inverse coupling, shown in Figures 5.13(a) and 5.13(b), increases the necessary equivalent inductance to keep the same ripple. Even when the converter goes into DICM the maximum input current ripple is kept within limits. On the other hand, direct coupling need of a lower inductance, as long as CICM is kept. The deeper the converter goes into DICM the bigger the inductance needed with respect to the one obtained with Equation 5.11.

Due to the converter parameters, the higher the number of phases the easier it is to go into DICM, and the previous derived equation becomes inappropriate. Some inductor designs are not possible inside the limits due to the fact that two coils of the same magnitudes have to be wound in the same core. The necessary inductances for the different coupling factors and switching frequencies are found in Table 5.7. In this case, the value of the inductance also depends on the input power. A minimum input power of 250 W has been considered, under which the ripple requirements might not be fulfilled and high ripples might be present in direct coupled configurations.

As Table 5.7 shows, inverse coupling inductances are higher, making the necessary coupled inductor designs bigger than the maximum allowed E65 core. However, some designs with high inductance might be possible due to canceling effects of the flux. The results of the design are shown in Table 5.8. Configurations which have no working inductor that meets the required design specifications are not listed. As expected, inverse coupling is preferred due to the DC flux canceling effect it has on the cores, making it possible to have designs with a 50 kHz switching frequency. The volume of the converters is kept low except on the 6 phases version with $k = 0.9$, because its lower

Table 5.7: Inductance values of the CIIBC [mH].

k	-0.9	-0.35	0.35	0.9
2 phases, 50 kHz	26.204	4.030	2.343	2.632
4 phases, 50 kHz	13.093	2.016	1.312	1.359
6 phases, 50 kHz	8.732	1.345	0.879	0.921
2 phases, 100 kHz	13.102	2.015	1.172	1.316
4 phases, 100 kHz	6.546	1.008	0.656	0.679
6 phases, 100 kHz	4.366	0.673	0.440	0.461

efficiency involves a bigger cooling system.

Table 5.8: Design values of the CIIBCs.

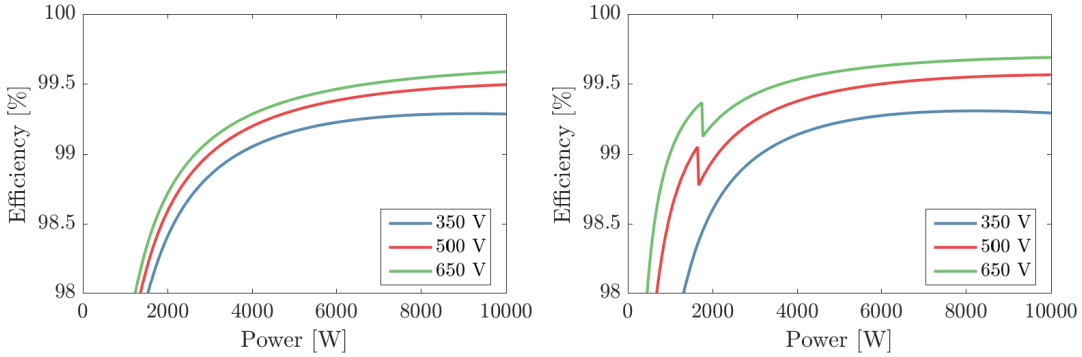
Freq. [kHz]	50		100					
Phases	4	6	4	4	6	6	6	6
k	-0.9	-0.9	-0.9	0.35	-0.9	-0.35	0.35	0.9
Ind. [mH]	11.3066	8.7322	6.5463	0.656	4.366	0.673	0.44	0.461
Core	E 65	E55	E 55	E65	E 55	E55	E65	E65
Material	R	R	3C92	R	R	3C92	R	3C92
turns	29	31	24	47	31	49	49	22
Air gap	0.022	0.024	0.002	0.114	0.0049	0.0792	0.1853	0.0357
Rac []	0.034	0.047	0.028	0.045	0.047	0.050	0.050	0.026
Cin [uF]	0.510	0.340	0.255	0.255	0.170	0.170	0.170	0.170
Cout [uF]	2.258	1.411	1.129	1.281	0.706	0.704	0.905	1.485
Mosfet ID	20 A$^{\triangle}$	12.5 A$^{\triangle\triangle}$	12.5 A$^{\triangle\triangle}$	12.5 A$^{\triangle\triangle}$	12.5 A$^{\triangle\triangle}$	12.5 A$^{\triangle\triangle}$	12.5 A$^{\triangle\triangle}$	12.5 A$^{\triangle\triangle}$
Diode ID	20 A$\star$	14 A$\star\star$	14 A$\star\star$	14 A$\star\star$	11 A$\diamond$	11 A$\diamond$	11 A$\diamond$	14 A$\star\star$
Volume [l]	0.332	0.276	0.345	0.404	0.318	0.315	0.434	0.518
Efficiency	99.036	99.319	99.21	99.22	99.11	99.13	99.04	98.86

$^{\triangle}$ Cree C2M0080120D $\star$ Cree C4D15120A $\diamond$ Cree C4D08120A

$^{\triangle\triangle}$ Cree C2M0160120D $\star\star$ Cree C4D10120A

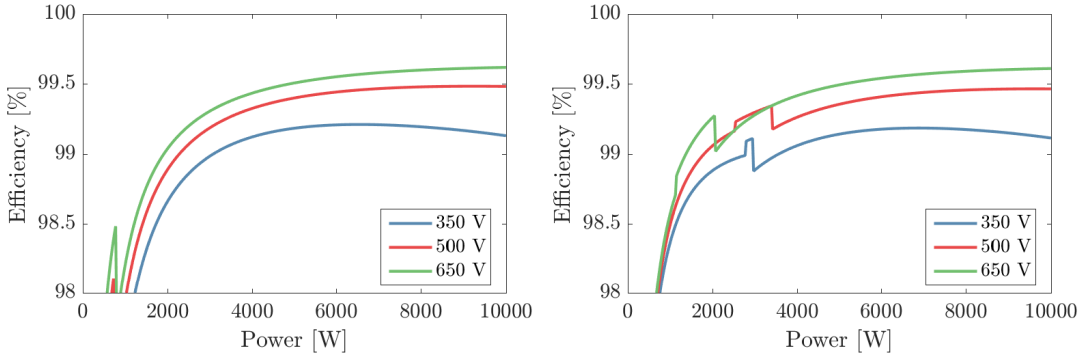
The plots for the different efficiencies can be seen in Figure 5.14. The steep jumps in efficiency are due to the different conduction modes of the converter, meaning that very different amounts of losses can be present on the converter in very similar operating points.

The losses in the different elements of the converter are shown in Figure 5.15, where the different switching voltages that both the diode and switches have depending on the conduction mode are reflected in different amounts of losses. The different voltages are not reflected on the inductor losses as they mainly depend on the current through the windings, which does not change abruptly between similar operating points. The conduction losses of the different elements are kept low because of the high number of phases. Lastly, the core losses also change depending on the conduction mode because of the different current waveforms. Core losses are similar between the different versions too, although higher flux is generated in the direct coupling versions of the converter; the increase of the size of the core in these versions keep the losses contained.



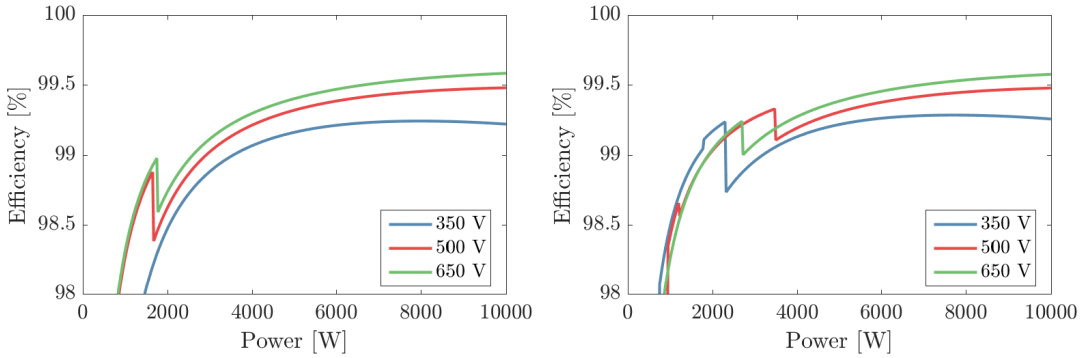
(a) 4 phases, k=-0.9, 50kHz

(b) 6 phases, k=-0.9, 50kHz



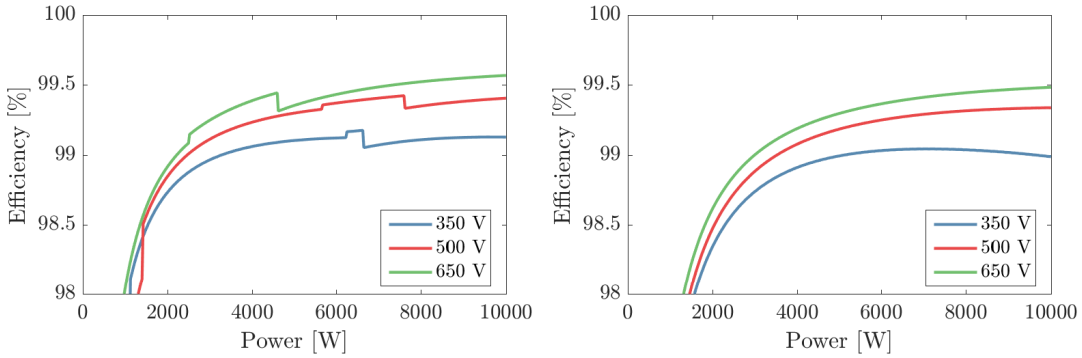
(c) 4 phases, k=-0.9, 100kHz

(d) 4 phases, k=0.35, 100kHz



(e) 6 phases, k=-0.90, 100kHz

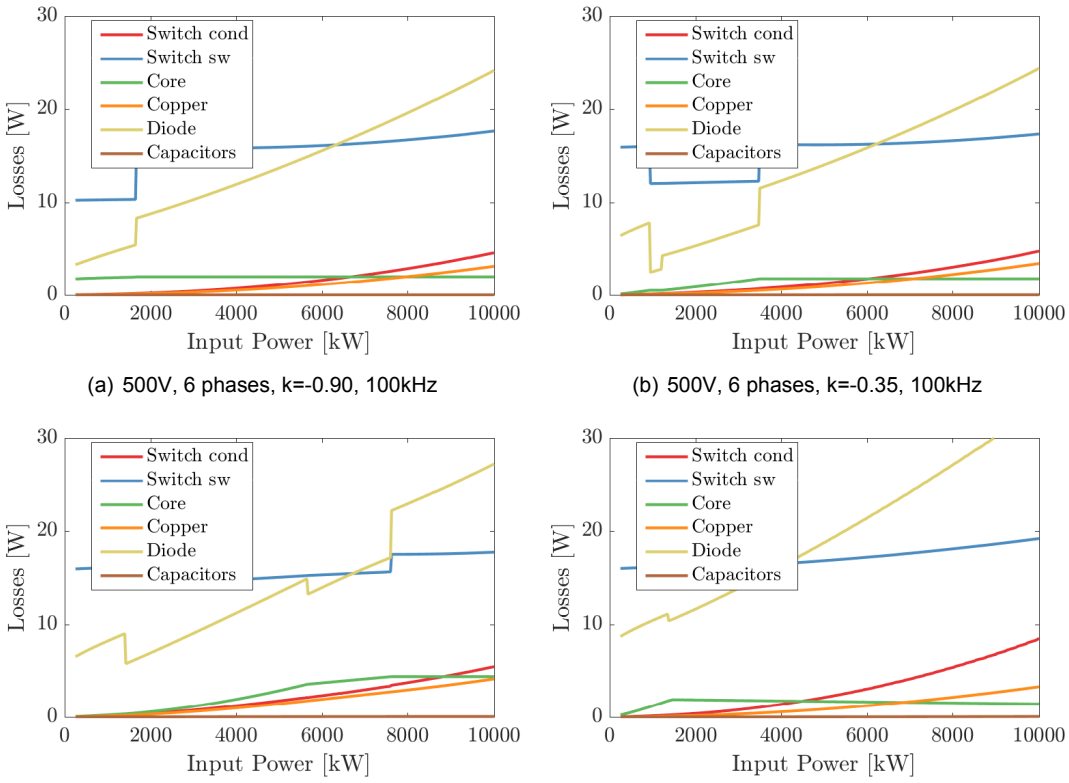
(f) 6 phases, k=-0.35, 100kHz



(g) 6 phases, k=0.35, 100kHz

(h) 6 phases, k=0.9, 100kHz

Figure 5.14: Efficiency versus input power for different levels of interleaving



(a) 500V, 6 phases, k=-0.90, 100kHz

(b) 500V, 6 phases, k=-0.35, 100kHz

(c) 500V, 6 phases, k=0.35, 100kHz

(d) 500V, 6 phases, k=0.90, 100kHz

Figure 5.15: Losses versus input power on the different elements at 500 V

The weighted efficiency of the converters, obtained using the method described in section 3.2, is shown in Table 5.9. Taking into account the fact that the efficiency is not linear, certain configurations of the CIIBC might get higher weighted efficiencies, for example if in a low power state the efficiency is higher, as shown in Figures 5.14(b) and 5.14(d).

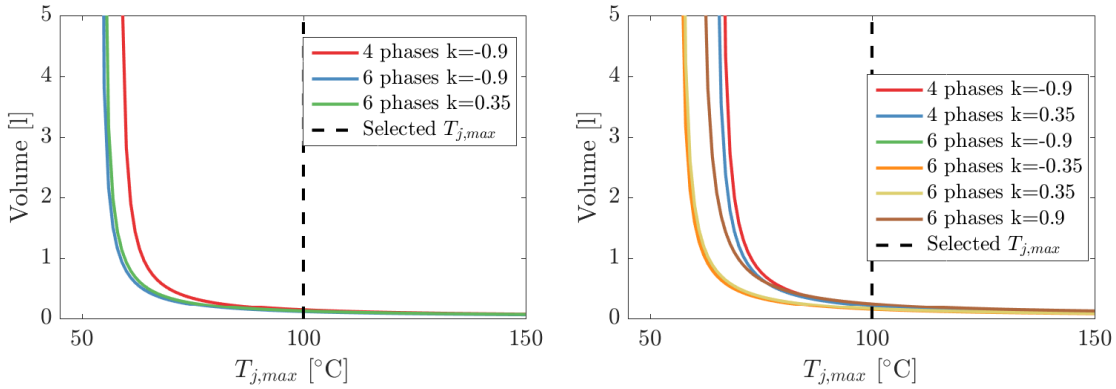
Table 5.9: Efficiency of the CIIBCs.

Freq. [kHz]	50		100					
Phases	4	6	4	4	6	6	6	6
Coupling (k)	-0.9	-0.9	-0.9	0.35	-0.9	-0.35	0.35	0.9
Efficiency	99.04	99.32	99.21	99.22	99.11	99.13	99.04	98.86

Figure 5.16 shows the necessary heat sink size for a different number of phases and both frequencies when considering different maximum values of junction temperature. At low temperatures a higher number of phases has a better performance due to the lower differences between the maximum temperature junctions of the mosfets and diodes. However, increasing the number of phases has almost no effect in the established $T_{j,max}$ for the 50 kHz version, resulting in a similar cooling system volume.

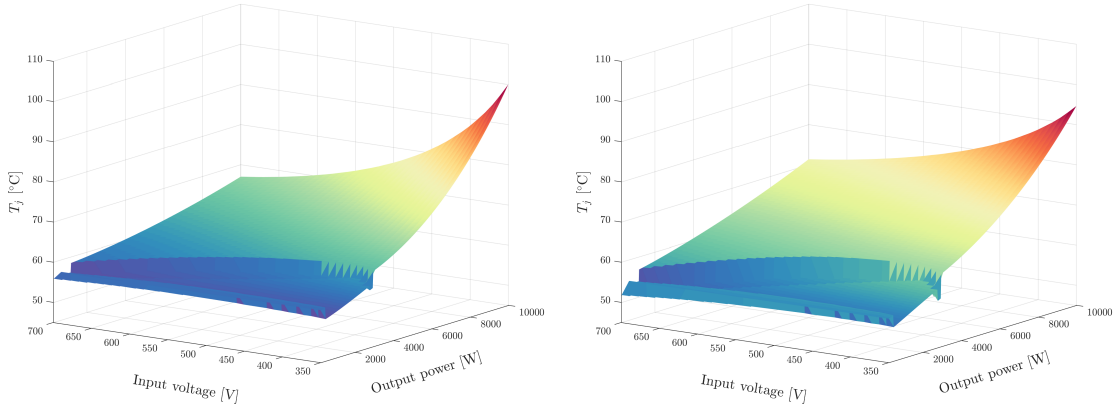
The junction temperatures of the different elements are also known for every operating point. Figure 5.17 shows how the cooling system selected keeps temperatures under the pre-defined $T_{j,max}$. The 4 phases 50 kHz CIIBC is selected as an example because both diodes and switches have similar junction temperatures, resulting in a smaller cooling system (Figure 5.16(a)). Moreover, the effect of

the different conduction modes is seen in the junction temperatures as step jumps, considering that the represented points are in steady state operation of the converter.



(a) 50 kHz (b) 100 kHz

Figure 5.16: CIIBC cooling system size for different values of $T_{j,max}$



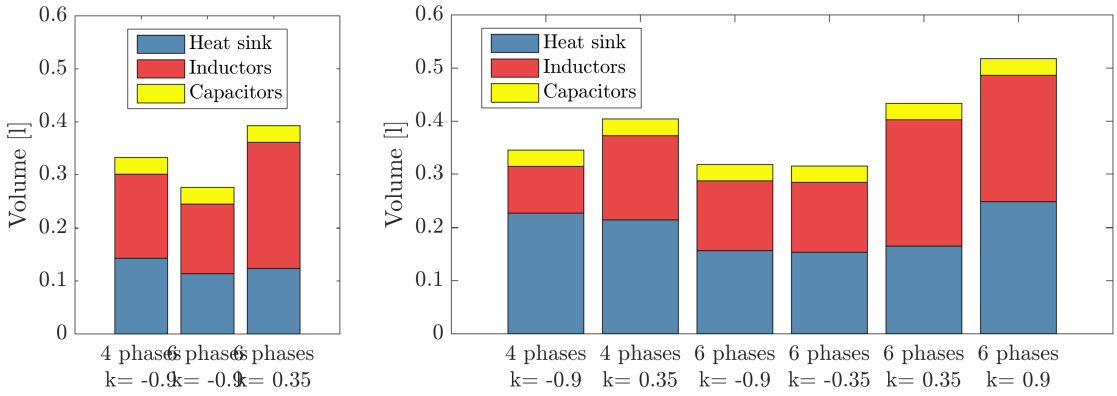
(a) $T_{j,mosfets}$ (b) $T_{j,diodes}$

Figure 5.17: Junction temperatures of CIIBC (4 phases 50 kHz example)

The volume of the different configurations, which is calculated from the heat sink size, the inductors size and the capacitors size is shown in Figure 5.18. The sizes of the different elements are not as predictable as in the IBC, as many different factors play a role in the waveforms and voltages in the evaluated steady state points of the converter.

5.2.3. Converter evaluation

The evaluation of the different parameters is shown in Table 5.10. The ratings are very similar to the ones given to the IBC, being in this case the 4 phases versions of the converter the most attractive ones, as they all score an 87, same rating as the best IBC option. The rating decrease due to the higher number of switches necessary is compensated by the decrease on the number of cores. The efficiency and volumes of the different topologies is very similar to the IBC in all configurations too.



(a) 50 kHz (b) 100 kHz

Figure 5.18: Volume of the different possible configurations of the CIIBC

Table 5.10: Evaluation of the CIIBC.

Freq. [kHz]	Weight	50		100					
Phases	-	4	6	4	4	6	6	6	6
k	-	-0.9	-0.9	-0.9	0.35	-0.9	-0.35	0.35	0.9
Num Switches	3	3	1	3	3	1	1	1	1
Num Didoes	1	3	1	3	3	1	1	1	1
Num Cores	3	5	4	5	5	4	4	4	4
Capacitors	1	5	5	5	5	5	5	5	5
Efficiency	5	4	4	4	4	4	4	4	3
Volume	5	4	5	4	3	4	4	3	2
Eff. Improve	1	3	3	3	3	3	3	3	3
Controlability	3	4	4	4	4	4	4	4	4
TOTAL		**87**	**81**	**87**	**82**	**76**	**76**	**71**	**61**

5.3. Three Level Boost Converter

The TLBC topology [19] is represented again in Figure 5.19 for surveyability. It is composed of two diodes, two switches, one input inductor and three capacitors, one at the input and two at the output, the DC bus.

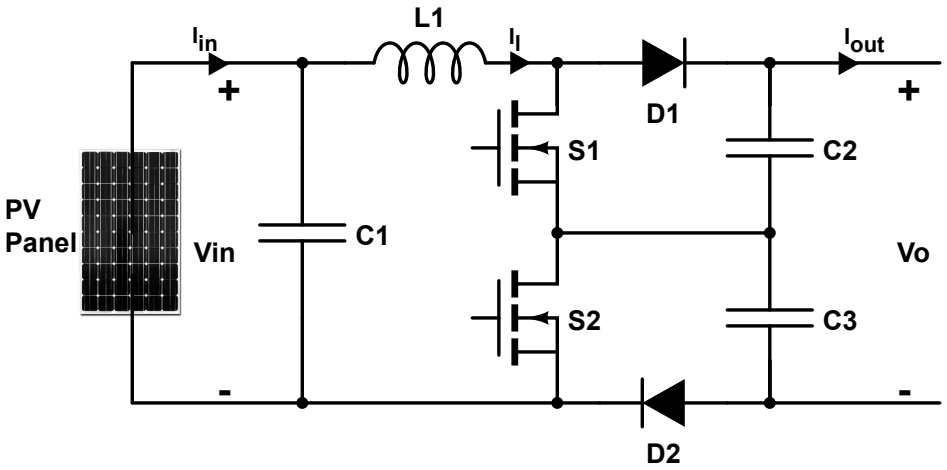


Figure 5.19: Structure of the TLBC

The output filter capacitors are series connected and serve as a capacitive voltage divider to split the output voltage into two equal voltages, which might be useful to provide a neutral point for certain type of inverters. The switch gating patterns are generated by utilizing two carrier signals phase shifted by 180° from each other. In the case of interleaving TLBCs [75], the other phases are shifted $\frac{\pi}{N}$, in such a way that all switches turn on and off at different times.

The use of multiple levels in the converter has many advantages:

- Semiconductors are rated for half the output voltage
- Equivalent switching frequency seen from the input is twice the switching frequency.
- Inductor volume reduced by approximately a factor of 4 [19].
- Depending on the voltage ranges, output capacitance might be reduced.

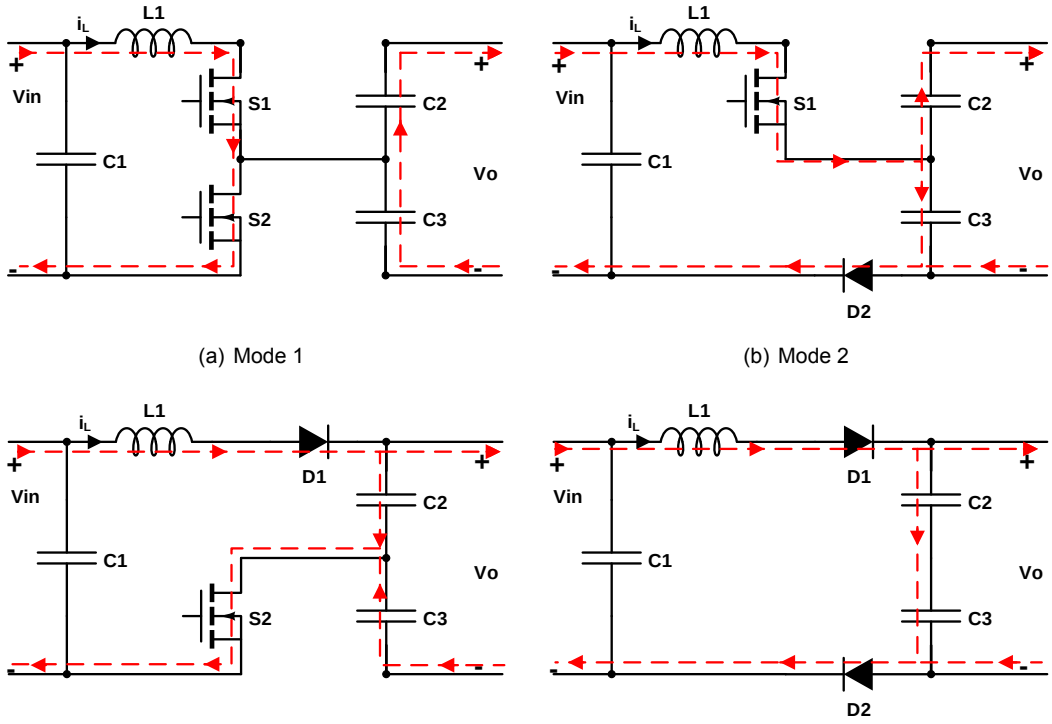
In this section the TLBC is going to be studied thoroughly, following the next steps:

1. Current waveforms derivation
2. Magnetic elements design
3. Input and output capacitor sizing
4. Switches and diodes requirements
5. Cooling system sizing

5.3.1. Converter design

Current waveforms derivation

In order to understand the operation mode of the converter, and to be able to obtain the waveforms that rule its operation, four different switching states must be considered. These four possibilities are differentiated by the conducting switches, see Figure 5.20 [19].

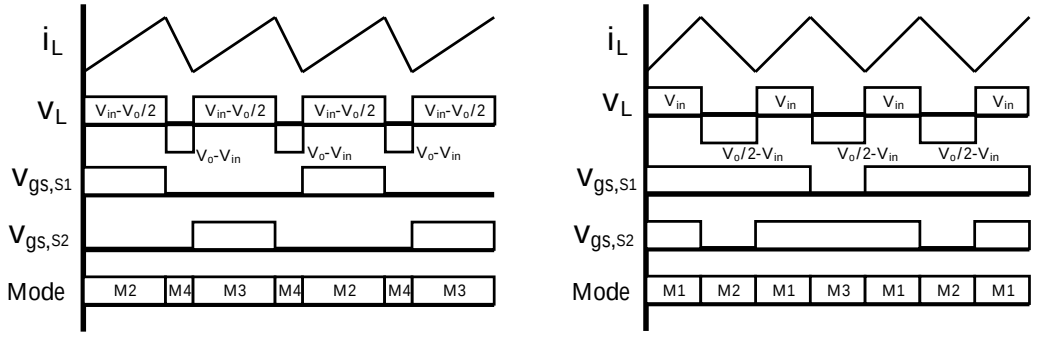


(a) Mode 1 (b) Mode 2

(c) Mode 3 (d) Mode 4

Figure 5.20: Switching states of the TLBC

Depending on the applied duty cycle, Mode 1 or Mode 4 will not take place. When the duty cycle is lower than 0.5, the two switches can not be turned on at the same time: Mode 1 (Figure 5.20(a)) will not be used. On the other hand, when the duty cycle is higher than 0.5, Mode 4 (Figure 5.20(d)) does not take place as there is always one switch conducting. This behavior is represented in Figure 5.21, where the inductor current and the modes of operation in CICM are displayed depending on the duty cycle of the converter.



(a) D<0.5 (b) D>0.5

Figure 5.21: Waveforms of the TLBC for different duty cycles, CICM

Figure 5.21 also demonstrates that the input current ripple frequency is doubled due to the two level configuration. The inductor current ripple can be obtained with the following equation when $D < 0.5$ and the converter works in CICM :

$$I_{l,pp} = \left(V_i - \frac{V_o}{2}\right)\frac{DT}{L} \tag{5.14}$$

When $D > 0.5$ and the converter operates CICM, the equation to apply is:

$$I_{l,pp} = (V_o - V_i)\frac{(D-0.5)T}{L} \tag{5.15}$$

In the case the converter works in DICM, the equations are different but similar to the ones of the IBC, as the derivation method is the same but taking into account the halved voltages at the output. When the duty cycle is under 0.5:

$$\begin{aligned} I_o &= \frac{V_{in}I_{in}}{NV_o} \\ D &= \sqrt{\frac{I_o L}{\left(\frac{(V_{in}-0.5V_o)^2}{V_o - V_{in}} + \frac{V_{in}-V_o}{2}\right)T_{sw}}} \\ D_2 &= D\frac{V_{in} - \frac{V_o}{2}}{V_o - V_{in}} \\ I_{l,peak} &= \frac{V_{in} - \frac{V_o}{2}}{L}DT_{sw} \end{aligned} \tag{5.16}$$

If the output voltage is more than twice the input voltage (the duty cycle is over 0.5), the converter operates in DICM:

$$\begin{aligned} I_o &= \frac{V_{in}I_{in}}{NV_o} \\ D &= \sqrt{\frac{2I_o L(\frac{V_o}{2} - V_{in})}{V_{in}^2 T_{sw}}} \\ D_2 &= D\frac{V_{in}}{\frac{V_o}{2} - V_{in}} \\ I_{l,peak} &= \frac{V_{in}}{L}DT_{sw} \end{aligned} \tag{5.17}$$

With these set of equations and the waveforms shown in Figure 5.21, it is possible to obtain the inductor, switch and diode waveforms in all operating points. The input and output currents, in the case of two or more interleaved phases, is the sum of the different input and output currents in each phase.

Size of inductors

As for the previously designed and evaluated converters, Equation 5.18 can be used in order to calculate the minimum value of the required inductor:

$$L = \frac{V_o}{f_{sw}I_{in,pp}}N\left(\frac{floor(2ND)+1}{2N} - D\right)\left(D - \frac{floor(2ND)}{2N}\right) \tag{5.18}$$

If this equation is normalized, the current ripple at the input of the TLBC can be compared to the conventional boost converter input current ripple. This is shown in Figure 5.22. It is clear that for the same inductor size in the single phase TLBC the ripple is greatly reduced. However, the current through the inductor is the same as in the conventional boost converter, increasing the necessary energy storage of the inductor. When using two interleaved converters, the inductor size reduction is lower in comparison but the current is halved, making it a more suitable topology.

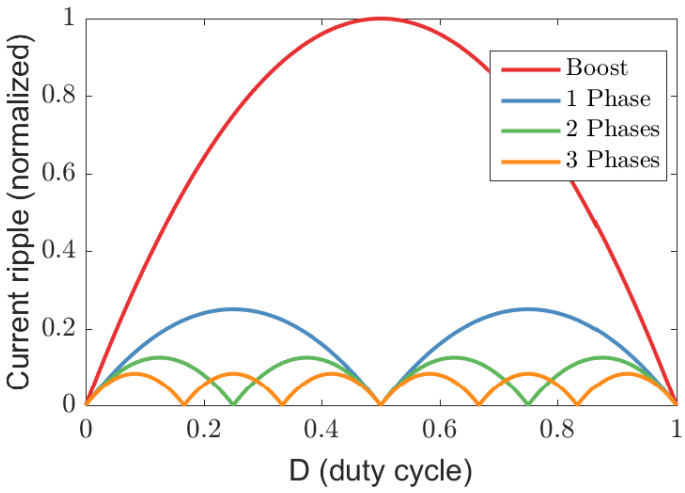


Figure 5.22: Input current ripple for the TLBC versus the normal boost converter

Size of capacitances

The size of the capacitances can be obtained in a similar way as the method used in the IBC section. The main difference is that the equivalent frequency of the input current of the TLBC is doubled, see Equations 5.19.

$$C_{in} = \frac{1}{\Delta V_{in}} \frac{1}{2} \frac{1}{2Nf_{sw}} \frac{\Delta I_{in,pp}}{2} \tag{5.19}$$

Where ΔV_{in} is the maximum admissible voltage increments, N is the number of phases, f_{sw} is the switching frequency and $\Delta I_{in,pp}$ is the current increment peak to peak. The application of this equation in the working condition with a higher input and output current leads to a minimum value of both capacitors. On the other hand, the output current waveform is not triangular, and the necessary capacitance is found by using Equation 5.20 on the summed output current of all the phases, considering that the maximum difference between voltages of $V(t)$ must be kept under the limits.

$$V(t) = \frac{Q(t)}{C} = \frac{1}{C} \int_{t_0}^{t} I(t)dt + V(t_0) \tag{5.20}$$

Switches and diodes requirements

The minimum breakdown voltage of the switch has to be half the output voltage of the converter, or in other words, half the DC link voltage. The current through the switches follows the same waveform as the inductor current while the switches are on. The maximum current through the switches will happen at minimum voltage (350 V) and highest power of the converter (10 kW).

The voltage rating of the diodes has to be the full DC bus voltage, V_o, in Mode 1, see Figure 5.20(a). The current through the diodes follows the same waveform as the inductor current while the switches are off. In other words, while the switch is conducting, the current through the complementary diode is zero and the rest of the time follows the inductor current.

Efficiency Improvement

The fact that the switches of the topology operate at half the DC link voltage reduce the switching losses considerably. However, currents through the switches are relatively high and therefore switching losses still play a role at high switching frequencies. In order to reduce the losses, ZVS

is preferred. Different options have been proposed in literature to improve the performance of the converter in terms of efficiency:

- **Passive lossless snubber [76].** A snubber cell is added to each diode. It consists of a snubber inductor, a snubber capacitor, a buffer capacitor and three diodes. The resonance between the inductor and capacitors realizes the zero current turn-on and zero voltage turn-off of the main power switches as well as zero voltage turn-off and zero voltage turn-on of the freewheel diodes, considerably reducing the switching losses of the converter.
- **Full ZVS with parallel capacitors and diodes [77].** In this case, a parallel capacitor and a diode are added in parallel to each mosfet of the converter. It relies on using Boundary Inductor Conduction Mode (BICM) in order to achieve the ZVS while in DICM it would work too. This method eliminates the switching losses of the converter resulting in higher efficiencies.
- **Coupled inductor and voltage doubler circuits [78].** This topology increases the possible voltage gain of the converter while increasing the efficiency. The input inductor is split and coupled, which together with two extra diodes increase the voltage gain of the converter reducing the losses.

The most interesting option for increasing the efficiency of the converter is to add parallel capacitor and diodes to the mosfets in order to remove the switching losses. However, the fact that it operates mainly in BICM complicates the control of the converter. Therefore, a rate of two is given to the converter on terms of efficiency improvement.

Controllability

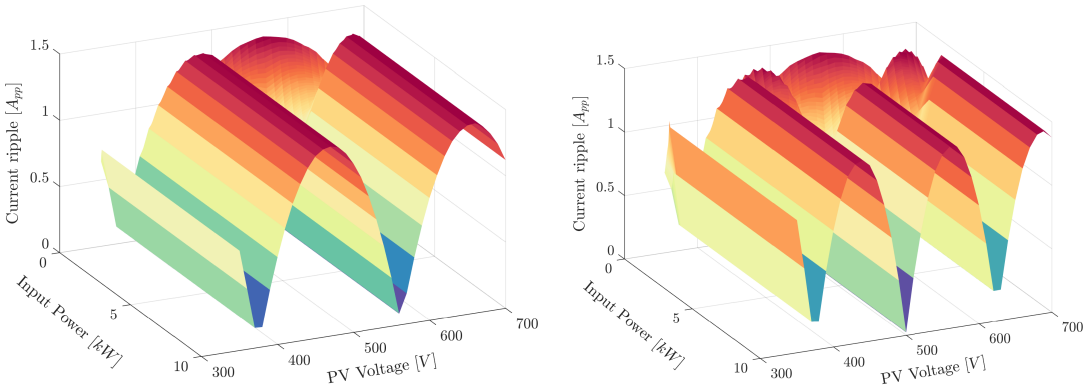
The main difference between the TLBC and the IBC is the fact that it relies in a split capacitor. The control of the converter has to include DC link voltage balance control in order to ensure a correct operation of the converter. Several control methods have been proposed in literature [79] [80], which are not very complex but increase the complexity of the control when compared to the IBC. On the other hand, as explained in [81], CICM is preferred over DICM because controllability issues appear when inductor current goes down to zero. The fact that the diode conducting time is not known complicates the control of the converter in DICM, making it slower and appropriate for applications which do not require high transient stability. Therefore, a rating of three has been given to the controllability of the TLBC.

5.3.2. Results

A monophase version of the TLBC would need an inductor which is able to conduct approximately 30 A of DC current, which is not possible to construct in an E65 core with the needed inductance, around 0.64 mH. This version of the TLBC would be interesting because it would mostly operate in CICM, while the two phased version operates in DICM when the power input is under 1.6 kW (Figure 5.23(a)) and the three phases version when it is under 4 kW. This numbers are indicative as the operation mode depends on the input voltage. This results in a more difficult controllability, as discussed previously.

The input current ripple when the converter is in CICM follows the same trace as what has been seen in Figure 5.22. The design is performed for a single phase TLBC and two and three phases TLBC for 50 kHz and 100 kHz. The design procedure has been previously explained in Chapter 4. The one phase version is not further discussed as all its elements would not be PCB mountable. The design procedure leads to the results in Table 5.11, where V_{conv} is the final converter volume.

Table 5.11 shows how the necessary inductance is reduced with increasing number of phases, and thus the necessary core size. The resulting efficiency is shown at the same operating points and different frequencies in Figure 5.24.



(a) 2 phases (b) 3 phases

Figure 5.23: Input current ripple versus input voltage and power for different levels of interleaving

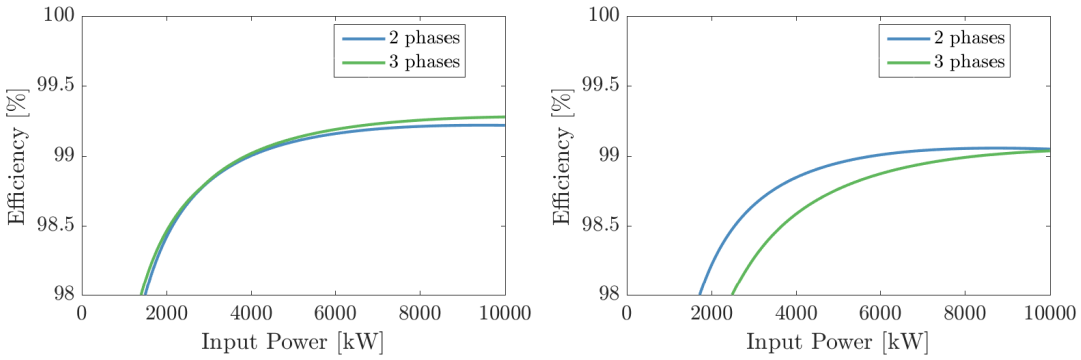
Table 5.11: Design values for the TLBC.

	50 kHz		**100 kHz**	
Phases	2	3	2	3
L [mH]	0.328	0.194	0.164	0.109
Core	E65	E55	E55	E42
Material	3C92	3C92	3C92	3C92
N	22	15	17	15
l_g [cm]	0.500	0.228	0.391	0.230
R_{ac} [Ω]	0.010	0.006	0.007	0.007
C_{in} [uF]	0.511	0.342	0.256	0.171
C_{out} [uF]	4.736	0.742	2.368	0.371
Mosfet	60 A*	40 A**	40 A**	40 A**
Diode	25.5 A⋄	25.5 A⋄	25.5 A⋄	20 A⋄⋄
V_{conv} [dm^3]	0.509	0.398	0.593	0.421

* Cree C2M0025120D ⋄ Cree C4D20120A

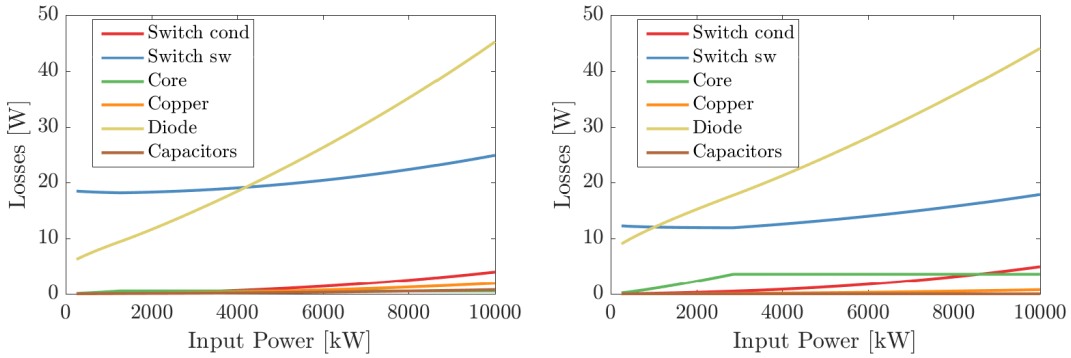
** Cree C2M0040120D ⋄⋄ Cree C4D15120A

Figures 5.24(a) and 5.24(b) show that the two phases version performs better than the three phases configuration, being the differences more remarkable in the 100 kHz versions due to higher switching losses. When the switching frequency is set to be 100 kHz the efficiency is reduced, while the core size is reduced by one E core size. How the losses are spread between the different components for the four configurations is shown in Figure 5.25.

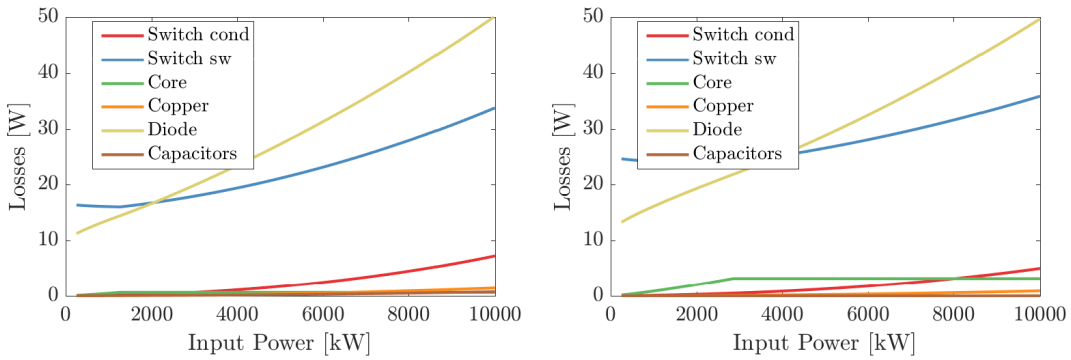


(a) 500V, 50kHz (b) 500V, 100kHz

Figure 5.24: Efficiency versus input power for different levels of interleaving



(a) 2 phases, 500V, 50kHz (b) 3 phases, 500V, 50kHz



(c) 2 phases, 500V, 100kHz (d) 3 phases, 500V, 100kHz

Figure 5.25: Losses versus input power for 3 and 4 phases at 500V

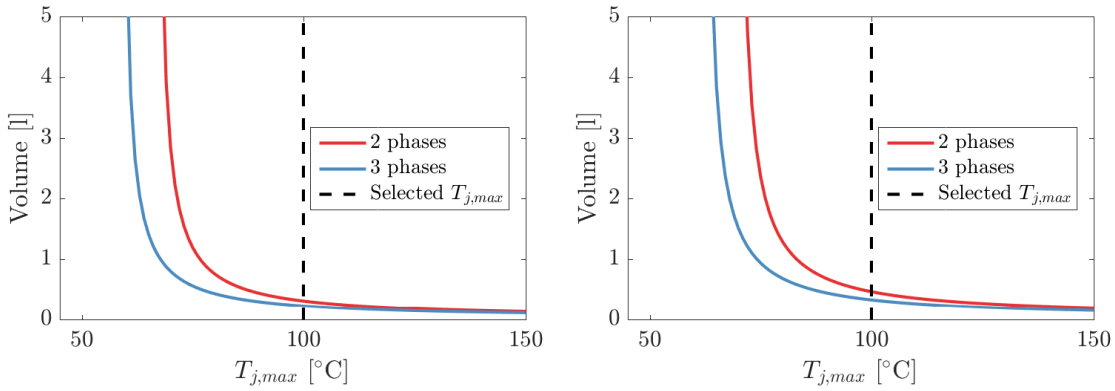
Figure 5.25 show that the biggest losses are due to the diodes, because two of them can be conducting at the same time depending on the mode of operation. Diode paralleling has been also checked and the results do not improve; the losses of the diodes are similar in all configurations because the forward voltage is not decreased enough. The conduction losses of the switch at 100 kHz decrease in the the three phases version while the switching losses increase, as it is expected. However, in the 50 kHz converters the opposite occurs due to the fact that the selected mosfet is changed for one with more conduction losses and lower switching losses for the three phase version.

The weighted efficiency for each setup is shown in Table 5.12. Figure 5.26 shows the necessary heat sink size for both considered frequencies when considering different maximum values of

Table 5.12: Weighted efficiency values for the TLBC.

	50 kHz		100 kHz	
Phases	2	3	2	3
Efficiency	98.77	98.83	98.59	98.24

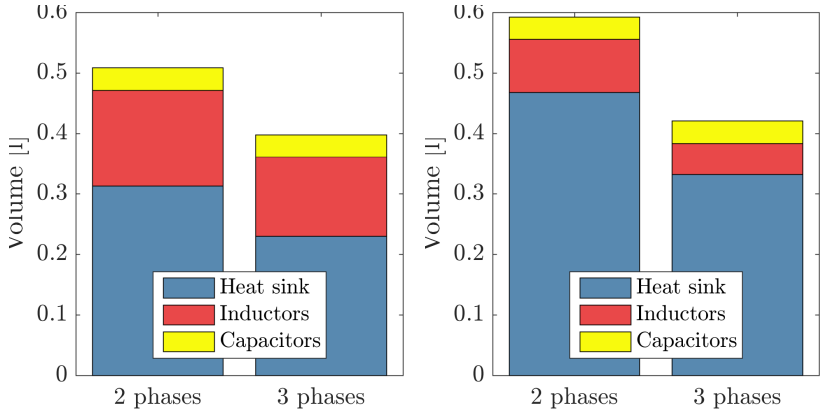
junction temperature. The performances are very similar for all configurations, without the need of increasing the $T_{j,max}$ to further reduce the size of the system. Increasing the number of phases has a considerable impact on this converter, as the diode losses are quite high and splitting the losses between a higher number of diodes improves the cooling efficiency of the heat sink.



(a) 50 kHz (b) 100 kHz

Figure 5.26: TLBC cooling system size for different values of $T_{j,max}$

The volume of the different configurations, which is calculated from the heat sink size, the inductors size and the capacitors size is shown in Figure 5.27. The plot also shows how inductor sizes are reduced when increasing the switching frequency. However, the higher losses of the switches, make the overall converter as big as the 50 kHz option due to bigger cooling system needs.



(a) 50 kHz (b) 100 kHz

Figure 5.27: Volume of the different possible configurations of the IBC

5.3.3. Converter evaluation

The previously obtained results can be transformed into a rating for each converter. Table 5.13 shows how the higher losses of the converter have a big impact on both the efficiency and volume grades of the converter, while the control is more complicated compared to the previously analyzed topologies.

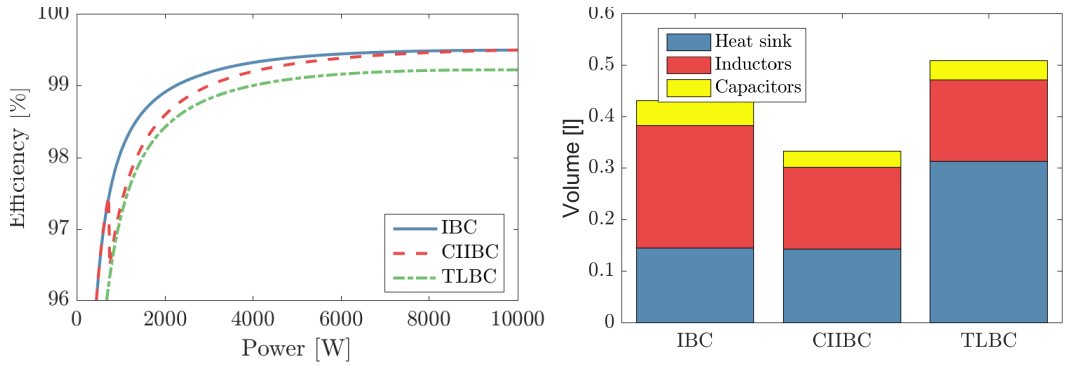
Table 5.13: Evaluation of the TLBC.

Freq. [kHz]	Weight	50		100	
Phases	-	2	3	2	3
Number switches	3	3	1	3	1
Number diodes	1	3	1	3	1
Number cores	3	5	4	5	4
Capacitors	1	4	4	4	4
Efficiency	5	3	3	3	2
Volume	5	2	4	2	3
Eff. Improvement	1	2	2	2	2
Controllability	3	2	2	2	2
TOTAL		**64**	**63**	**64**	**53**

Therefore, the TLBC is not as good as the IBC or the CIIBC. It could be an interesting topology if Silicon mosfets were used, which have lower voltage ratings, or a high voltage DC link was needed. However, for the multiport power converter evaluated in this work, the TLBC is not the best topology.

5.4. Conclusion

In this chapter three converters have been analyzed for the PV port: the Interleaved Boost Converter (IBC), the Coupled Inductors Interleaved Boost Converter (CIIBC) and the Three Level Boost Converter (TLBC). The optimal configurations efficiencies and volumes are shown in Figure 5.28 It has been seen that both the IBC and the CIIBC score higher than the TLBC, mainly due to the distribution of the currents between the different inductors. Between the two topologies based in the boost converter, the CIIBC has a higher score due to the low volume and lower magnetic elements count.



(a) Efficiency

(b) Volume

Figure 5.28: Results of the optimal topologies configurations of the PV port.

6

EV Port Analysis

In this chapter the two isolated DC-DC candidates listed in Section 2.3.2 are analyzed and rated. Those are the Dual Active Bridge (DAB), found on Section 6.1 and the Interleaved Bidirectional Flyback Converter (IBFC) which is explained on Section 6.2. The EV port must meet following requirements:

- 200 V - 500 V isolated output
- 10 kW / 30 A max input/output
- Low output ripple
- Bidirectional (Vehicle to Everything (V2X) operation)

The requirements of the Electric Vehicle (EV) port limit the converter operating area at low voltages and high voltages. At low output voltages, the output current is limited to 30 A; therefore, at 200 V the maximum power output is limited to 6 kW. When the voltage required to charge the battery is higher, the maximum output power sets the maximum current at the output; a maximum current of 20 amperes is set at the output when voltage is equal to 500 V. This behavior is represented in Figure 6.1, where the operating areas in both charging and discharging operation are shown.

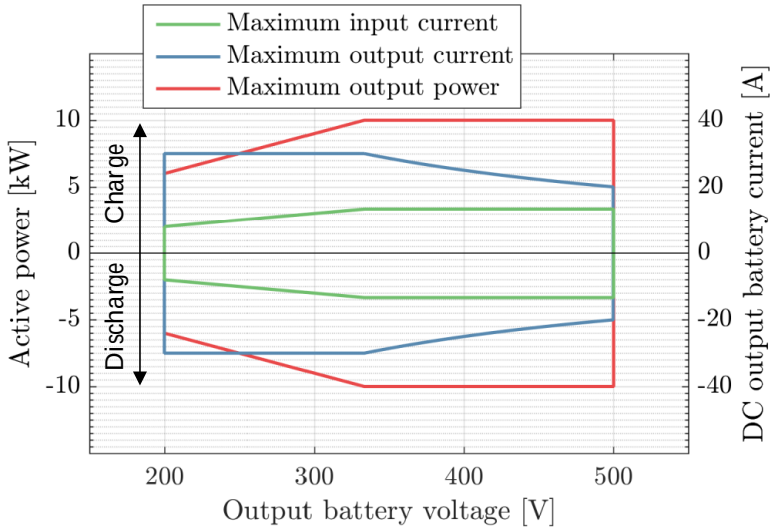


Figure 6.1: Operating area of the DAB

As a consequence, the maximum output current delivered by the converter increases linearly when the voltage ranges from 200 V to 333 V. From this voltage onwards, the current is derated in order to keep the power below the maximum value. This information is needed in order to size the different components accurately.

6.1. Dual Active Bridge

The DAB structure is built with two full bridge converters with an intermediate High Frequency Link (HFL), which consists of an inductor and a High Frequency Transformer (HFT). These two magnetic elements can be build separately or together in the case the flux leakage of the transformer is used to store energy. The DAB topology is represented in Figure 6.2, where it is clear that a total of eight switches is needed for its construction when only one phase is considered. The full bridges do not have freewheeling diodes in anti parallel to the switches because reverse currents in the switches are minimal (under 1% of total switching period) and the body diodes of the SiC Mosfets can be used.

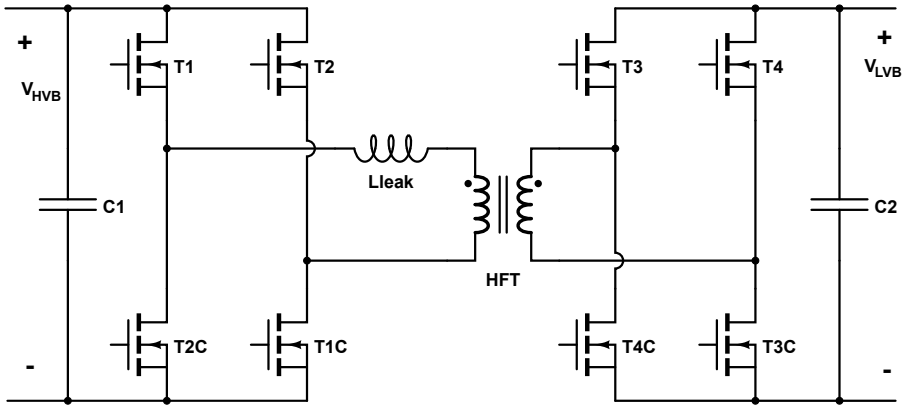


Figure 6.2: Structure of the of the DAB

The two full bridges experience different voltages and currents. The left bridge is referred as high voltage bridge (HVB) while the right bridge, connected at the output, is referred as the low voltage bridge (LVB). The connection points could be referred as input and output but the bidirectional operation capabilities makes this nomenclature inappropriate. Two capacitors are shown in the topology, but only the one connected to the DC link is sized; the other one is necessary in order to perform a pre-charge at the output of the converter before connecting the EV battery. The following aspects of the converter are considered in order to rate the topology:

1. Operating points of the converter
2. Phase-shift modulation and current waveforms
3. Switches requirements
4. Current Based Zero Voltage Switching (ZVS)
5. Leakage inductance
6. Transformer turns ratio
7. High Frequency Transformer (HFT)
8. DC link filter capacitance

The considered DAB is the basic topology of a series of topologies [20] which relies on the same structure to achieve DC to DC conversion. Other DAB topologies use parallel capacitors with the switches to achieve Resonance Based ZVS over a wider range than the ZVS which is considered in this report. Other topologies make use of resonant elements on the HFL in order to boost efficiency

and reduce currents. For the purpose of this project only this basic topology is considered, which already has inherent Current Based ZVS.

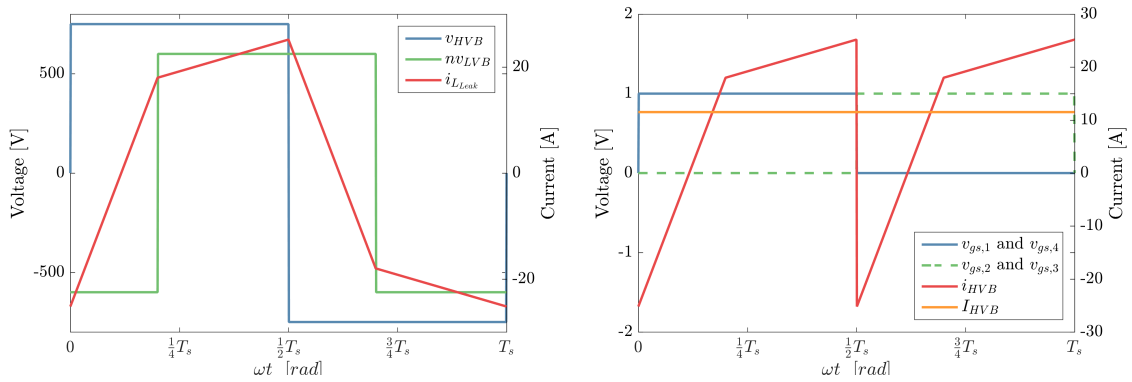
6.1.1. Converter design

Phase Shift Modulation and waveforms

The most used modulation technique to control the DAB is known as Phase Shift Modulation (PSM) [21] [82], and it is the most simple method to control the DAB. Both H bridges of the converter are operated at a fixed duty cycle of 0.5, and only the phase shift angle φ between both is changed in order to control the transferred power. As a consequence, the voltages applied at both sides of the HFL are either V_{HVB} or $-V_{LVB}$ in the High Voltage Bridge and V_{LVB} or $-V_{LVB}$ in the Low Voltage Bridge, see Figure 6.3. This results in a voltage applied to the leakage inductance L_{leak} of the HFL:

$$v_{L_{leak}}(t) = V_{HVB}(t) - nV_{LVB}(t) \tag{6.1}$$

Where $v_{L_{leak}}$ is the voltage applied to the leakage inductance. The voltage of the LVB bridge is reflected into the HVB side of the HFT by the n turns ratio, which is defined as the number of turns of the primary winding over the number of turns of the secondary winding. The voltage and current waveforms at the HFL of the DAB during one switching cycle are shown in Figure 6.3(a).



(a) (b)

Figure 6.3: Operating waveforms of the DAB ($V_{HVB} = 750$, $V_{LVB} = 300$, $T_\varphi = 0.2T_{sw}$, $n = 2$).

Figure 6.3(b) shows the current at the HVB when the DAB is in charging mode. The current waveform is directly derived from the $i_{L_{leak}}$ and the gating times of the different switches. The output waveform is very similar to the i_{HVB} HVB current waveform and therefore it is not shown. The waveforms clearly show that the frequency of the input the current is twice the switching frequency, but the ripple is high and it reaches negative values. The transferred power can be computed from the inductor current waveform $i_{L_{Leak}}$, where only the first half cycle needs to be considered, as voltages V_{HVB} and V_{LVB} remain the same during both half cycles. Considering $t_0 = 0$, the following expression can be derived [38] [83]:

$$P_{HVB} = \frac{1}{T_s}\int_0^{T_s} p_{HVB}(t)dt = \frac{2}{T_s}\int_0^{\frac{T_s}{2}} V_{HVB}(t)i_{L_{Leak}}(t)dt = \frac{2V_{HVB}}{T_s}\int_0^{\frac{T_s}{2}} i_{L_{Leak}}(t)dt \tag{6.2}$$

The current through the inductor during the first half cycle can be separated into two different intervals, where distinct voltages are applied. The first interval ranges from t_o to T_φ, while the second

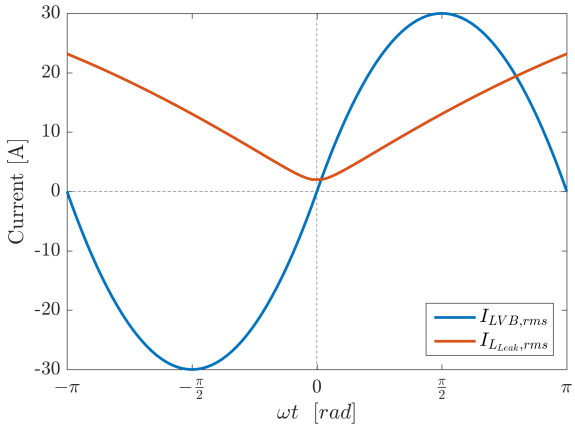


Figure 6.4: Main currents of the DAB ($V_1 = 750V$, $V_2 = 333.33V$, $T_\varphi = 0.25T_{sw}$,$n = 2$)

one is from T_φ to $\frac{T_S}{2}$, see Equation 6.3. T_φ is the phase shift time between the gating signals of the bridges, which is equal to $\varphi T_s/2\pi$.

$$\begin{aligned} i_{L_{Leak}}(t) &= i_{L_{Leak},0} + (V_{HVB} + nV_{LVB})\frac{t}{L_{leak}} \quad 0 < t < T_\varphi \\ i_{L_{Leak}}(t) &= i_{L_{Leak},T_\varphi} + (V_{HVB} - nV_{LVB})\frac{t-T_\varphi}{L_{leak}} \quad T_\varphi < t < \frac{T_s}{2} \end{aligned} \tag{6.3}$$

With Equations 6.3 and the fact that both voltages and currents in the converter repeat every half cycle with negative signs, $i_{L_{Leak},0}$ can be found:

$$i_{L_{Leak},0} = \frac{\pi(nV_{LVB} - V_{HVB}) - 2\varphi nV_{LVB}}{4\pi f_{sw} L_{Leak}} \tag{6.4}$$

Where φ is the phase shift angle. Equation 6.4 is valid for positive phase shift, and a similar expression can be found for negative phase shift or V2X operation. Finally, the transferred power can be derived from Equations 6.2, 6.3 and 6.4, valid for $-\pi < \varphi < \pi$:

$$P_{HVB} = P_{LVB} = \frac{nV_{LVB}V_{HVB}\varphi(\pi - |\varphi|)}{2\pi^2 f_{sw} L_{Leak}} \tag{6.5}$$

Where P_{HVB} and P_{LVB} denote the power transfer of the converter, which takes a positive value when the power transfer is from the HVB to the LVB and a negative value when the power flows in the opposite direction. Considering Equation 6.5, there is a maximum power transfer that can be achieved which occurs at $dP/d\varphi = 0$, see Figure 6.4. The maximum power transfer occurs at $\varphi = \frac{\pi}{2}$ or $T_\varphi = 0.25T_{sw}$. As a consequence, the designed DAB will operate at a maximum phase shift of $\pi/2$ in order to avoid the circulation of large currents in the converter. The maximum power delivered by the converter when the phase shift is fixed at the maximum is found as:

$$P_{\max} = \frac{nV_{LVB}V_{HVB}}{8f_{sw}L_{Leak}} \tag{6.6}$$

This modulation technique is the most used as it only requires the change of one variable, the displacement angle φ, to control the power flow between the two sides of the converter. The disadvantages are the limited operating range with low switching losses, as will be explained later, and the large RMS currents in the HFL, which produce bigger losses. Other modulation methods have been proposed in literature [84] [85] [86], but more variables have to be controlled and the overall complexity of the converter increases.

Switch requirements

The High Voltage Bridge (HVB) of the converter is connected to the DC link of the three port converter. As a result, the maximum voltage across the switches of the HVB is the DC link voltage. On the other hand, the LVB switches need a minimum breakdown voltage of 500 V, which is the maximum output voltage of the EV charger.

The currents through the switches depend on the leakage inductance value and the phase shift angle. The maximum circulating currents occurs at low LVB voltages up to the maximum power and maximum current point of the operating area of the DAB, see Figure 6.1. At higher voltages, the current is limited by reducing the displacement angle. Therefore, the maximum current through the SiC mosfets is calculated at V_{LVB}= 333.33 V and at maximum power, 10 kW.

Zero Voltage Switching

ZVS occurs when the body diode of the mosfet starts conducting during the dead-time (which is necessary to avoid short-circuiting the DC Link)before the mosfet gate signal is triggered, see Figure 6.3(a). If this situation takes place in the converter, v_{DS} is clamped at almost zero volts, because the switches can be gated on at the quasi-zero forward voltage of the body diode. The main requirement for this to happen is that the HFL current must be in such a direction that the body mosfet can conduct before the current direction is reversed.

If the mosfet is turned on at zero voltage, the switching losses are greatly reduced. First of all, the switching losses are virtually zero, as v_{DS} is the mosfets body diode forward voltage. Moreover, as stated previously on Section 3.1.1, the parasitic capacitance C_{oss} of the mosfet is discharged before turn on, reducing the overall losses. This must be taken into account for the loss modeling of the DAB. The boundaries at which ZVS takes place at every bridge can be found with Equations 6.7 [38], which are obtained from the previous derivation of the leakage inductance current.

$$\begin{aligned} ZVS \qquad HVB \rightarrow d &< \frac{1}{\sqrt{1-\frac{8|I_{LVB}|L_{Leak}f_{sw}}{V_{HVB}n}}} = \frac{1}{\sqrt{1-\frac{|I_{LVB}|}{I_{2,max}}}} \\ ZVS \qquad LVB \rightarrow d &< \sqrt{1-\frac{8|I_{LVB}|L_{Leak}f_{sw}}{V_{HVB}n}} = \sqrt{1-\frac{|I_{LVB}|}{I_{LVB,max}}} \end{aligned} \tag{6.7}$$

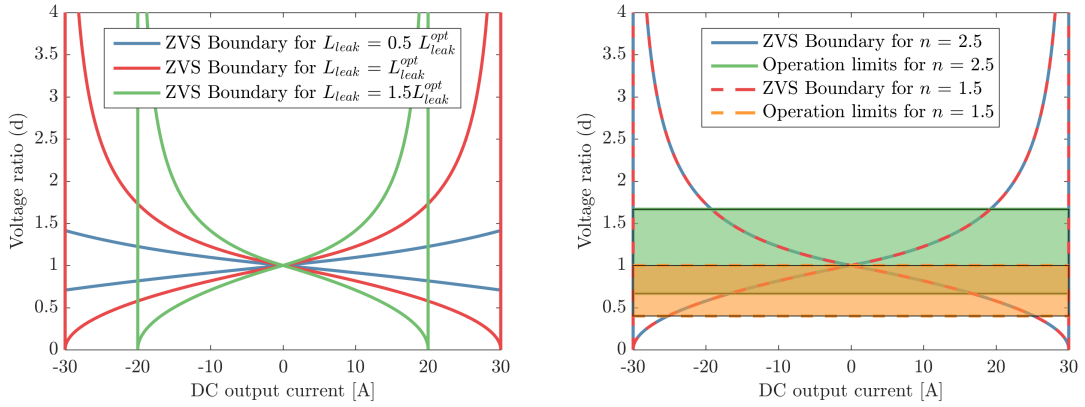
Where d is the voltage ratio $V_{LVB}n/V_{HVB}$.

Leakage inductance

Equation 6.6 can be modified in such a way as to find the proper leakage inductance values depending on the maximum allowed current in the LVB of the converter:

$$L_{Leak}^{opt} = \frac{nV_{HVB}}{8f_{sw}I_{LVB,max}} \tag{6.8}$$

If the leakage inductance value obtained from Equation 6.8 is increased or decreased the ZVS regions of the converter obtained with Equations 6.7. As shown on Figure 6.5(a), the optimal value of leakage inductance that maximizes the area operation on ZVS is obtained with Equation 6.6.



(a) ZVS area for different leakage inductances

(b) ZVS area for different turns ratio

Figure 6.5: ZVS boundaries of the DAB

Transformer turns ratio

The High Frequency Transformer (HFT) turns ratio n_1/n_2 can also be optimized to achieve lower switching losses. Looking at Figure 6.5(b) it is possible to see how depending on the voltage turns ratio the operating area in ZVS of the converter is different, as the voltage ratio limits change. Figure 6.5(b) shows the operating area of two different transformers with different turns ratio, showing which areas of the converter are used depending on the transformer turns ratio of the DAB and which of those operate in ZVS.

In order to optimize the turns ratio two different approaches can be considered; on one hand, it is possible to optimize the turns ratio in such a way that the operation area of the converter encloses the maximum possible zone of ZVS, or in other words, maximize the number of operating points in ZVS (Figure 6.5(b)). On the other hand, if the output power of the converter is considered, it is possible to find the turns ratio which yield the maximum power delivered, further enhancing the efficiency. This is done by considering if the power transfered at one point occurs in ZVS or not, so the ratio of power delivered in every possible turns ratio is known. The results of both this optimizations are shown in Figure 6.6, where the power based ratios and the area based ratios in Current Based ZVS and Hard Switching (HS) are shown.

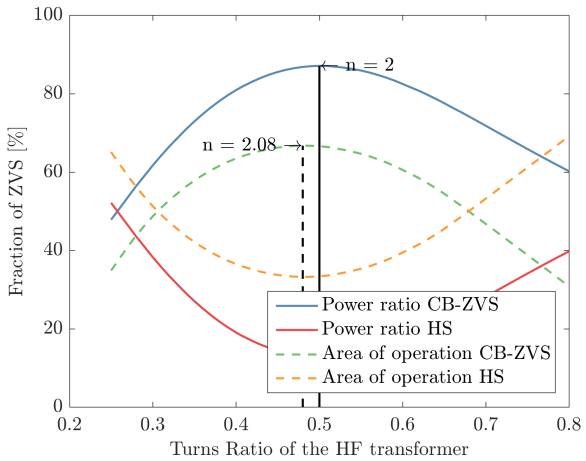


Figure 6.6: Optimum turn ratio for the two optimization approaches for the DAB, $L = L_{Leak}^{opt}$

If the area approach is considered, the optimal turns ratio of the converter is $n = 2.083$. However,

considering that higher efficiency is preferred in order to decrease the amount of power dissipation requirements, the power maximization method is preferred. The optimal turns ratio for the designed DAB is set to be 2.

DC link filter capacitance

The input capacitance, which is connected to the DC link, can be calculated from the HVB current ripple in the different configurations. It is wanted that the input voltage ripple is always under the 0.25% of the DC link voltage. Considering that the input current ripple for every working condition of the converter is already known as shown in Figure 6.3(b), the application of the following equation results in the change of voltage produced in the capacitors:

$$V_{HVB}(t) = \frac{Q(t)}{C} = \frac{1}{C}\int_{t_0}^{t} I_{cap}(t)dt + V_{HVB}(t_0) \tag{6.9}$$

Where I_{cap} is the current through the capacitor C. The voltage ripple can therefore be kept under the maximum 1.875 V peak to peak ripple in the DC link.

Efficiency Improvement

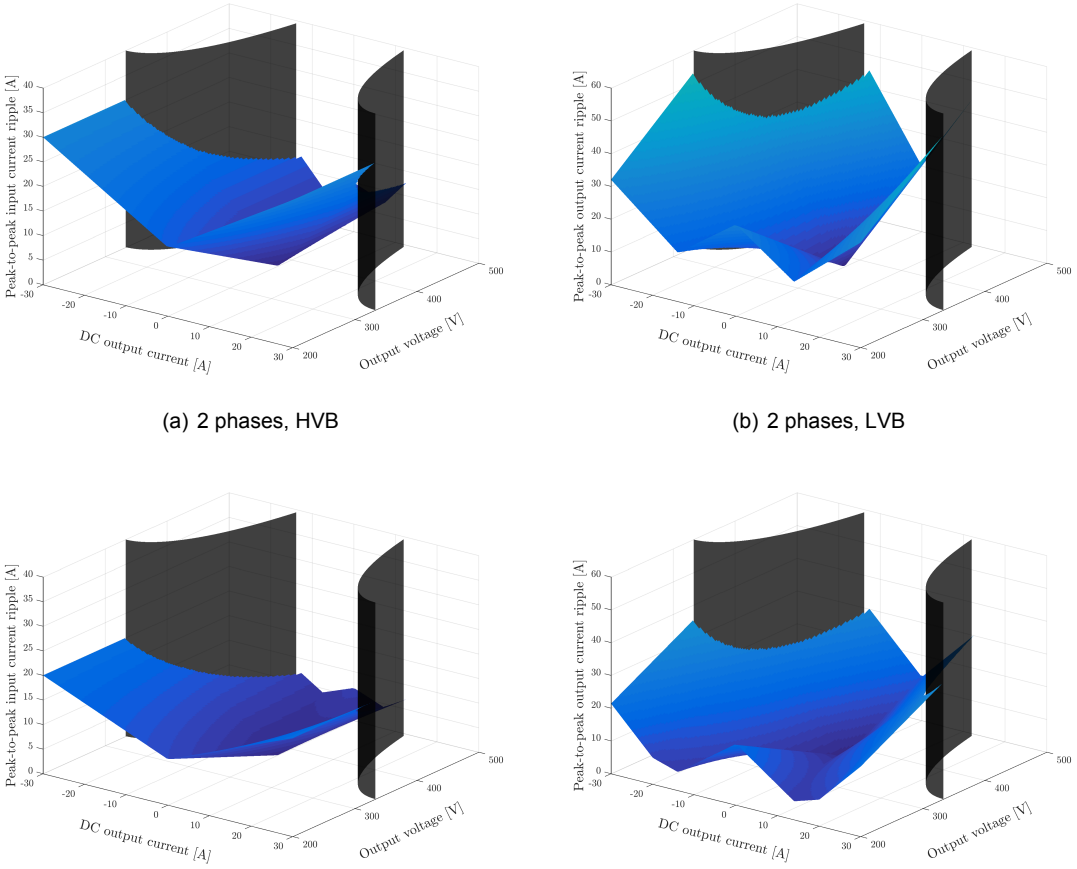
The DAB efficiency can be improved in several ways, with and without modifying the HFL.

- **Other modulation techniques [84] [85] [86].** As previously explained, there are other modulation techniques which besides the phase-shift delay between the bridges control both duty cycles of the bridges or the switching frequency. This methods add complexity to the control development and increase the computational cost, but do not increase the number of components of the system.
- **Resonant Based ZVS by adding parallel capacitors to the switches [87].** With this method it is possible to further expand the ZVS region of the converter and achieve lower losses.
- **Series Resonant HFL [88].** A series capacitor is added to the leakage inductance in order to achieve pure Zero Current Switching (ZCS) in the primary side and combined ZVS/ZCS in the secondary side, further enhancing the efficiency.

Therefore, there are many options to enhance the efficiency of the converter, and a rating of 5 has been chosen for the DAB.

6.1.2. Results

The DAB has been designed for one, two and three interleaved phases for both switching frequencies of 50 kHz and 100 kHz. The one phase version of the converter has very large currents at the LVB in certain conditions, reaching RMS current values of 32 A per switch, due to the very high ripple. This translates into very high losses in the bridge and no possible design (Figure 6.11). There are three options in order to keep the one phase DAB viable: consider a cooling system with a higher Cooling System Performance Index (CSPI), increase the maximum junction temperature $T_{j,max}$ of the SiC mosfets of the converter or paralleling more than one mosfet in order to share current and therefore losses. The two first options are discarded because it would not follow the designs considerations applied to all the designed converters. On the other hand, the second option could be feasible but it is a half way step to adding a second phase to the converter. Therefore, only the two and three phases designs of the DAB are considered.



(a) 2 phases, HVB

(b) 2 phases, LVB

(c) 3 phases, HVB

(d) 3 phases, LVB

Figure 6.7: Current ripple at both bridges of the DAB

The DAB, as shown in Figure 6.3(b), has a very large current ripple in both the input and the output, with twice the switching frequency. The results for the peak to peak current ripple of the two and three interleaved DABs are shown in Figure 6.7. The grey planes in all figures represent the limits of operation of the converter, already shown in Figure 6.1 previously. The ripple increases proportionally to both the current and voltage. In the case of the current ripple of the HVB, as the voltage is kept constant by the DC link, it mainly changes with the different current values. The plots show how by increasing the number of phases from two to three the maximum currents are reduced by approximately one third. Doubling the switching frequency does not reduce the amplitude of the current ripple, but it doubles the frequency.

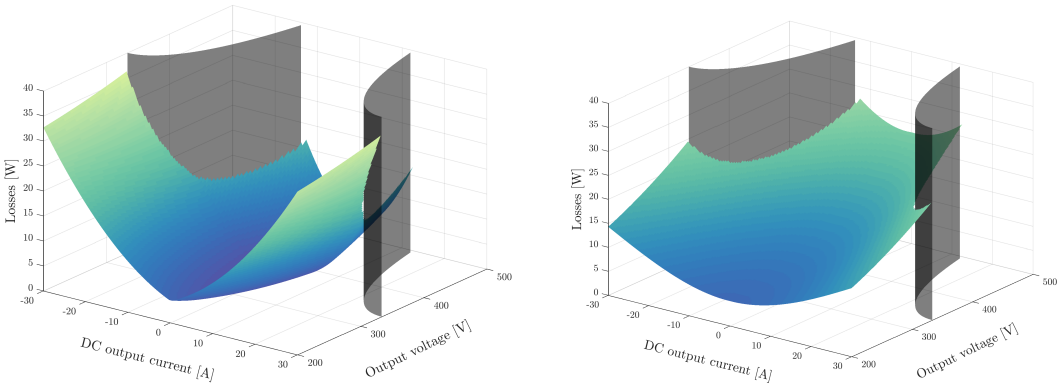
The inductors and transformers design has been done following the steps explained in Section 4.1 and Section 4.4 respectively. In the 50 kHz version two inductors in parallel with twice the inductance are needed in order to comply with the requirements, which state that inductors have to be PCB mounted to reduce manufacturing costs. The results of the design of the magnetic elements of the DAB are shown in Table 6.1. The inductance values are doubled in the 50 kHz version because two inductors are needed in each phase for both configurations.

Table 6.1 shows how the size of the transformer is not necessarily reduced when doubling the switching frequency. HFTs which handle high power have their size more or less restricted by the power capabilities, as the power lost in iron increases with the frequency and therefore the transformer gets heated up more rapidly. As a consequence its surface area has to be increased to increase thermal conduction, resulting in a larger transformer. While the flux density hysteresis loop

Table 6.1: Parameters of the leakage inductors and HFT of the DABs.

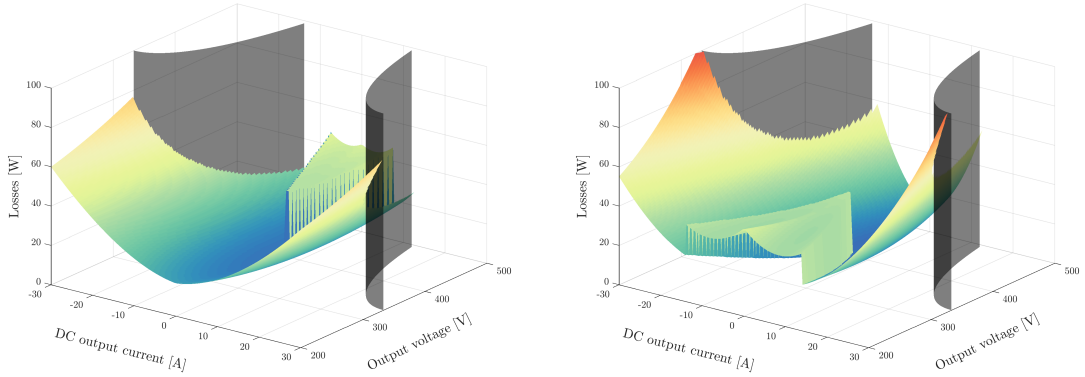
Freq. [kHz]	50		100	
Phases	2	3	2	3
Leakage inductors (per phase)				
L_{leak} [mH]	0.500	0.750	0.125	0.188
Core	2 // E 65	2 // E65	E 65	E 65
Material	3C92	3C92	3C92	3C92
turns	42	42	36	39
Air gap [cm]	0.120	0.080	0.352	0.275
R_{ac} [Ω]	0.049	0.049	0.041	0.048
HFT (per phase)				
Core	AMCC 50	AMCC 32	AMCC 50	AMCC 25
Material	Vitrop. 500F	Vitrop. 500F	Vitrop. 500F	Vitrop. 500F
n_1/n_2	42 / 21	40 / 20	40 / 20	40 / 20
B_{max} [T]	0.181	0.195	0.095	0.117
$R_{ac,1}$ [Ω]	0.019	0.026	0.017	0.024
$R_{ac,2}$ [Ω]	0.010	0.013	0.090	0.012

is reduced by half in terms of magnitude (see Equation 4.21), the frequency is doubled, which results in approximately the same core losses, already quite high in the HFT when compared to inductors. Further optimization on the switching frequency could be considered in order to reduce the size of the transformer further. Moreover, the predefined method for selecting the optimal design between the many different possibilities, which takes into account both the volume and the losses, might result in a bigger design with lower losses being picked. The losses of the magnetic components in the different configurations is shown in Figure 6.8.



(a) Inductor (b) HFT

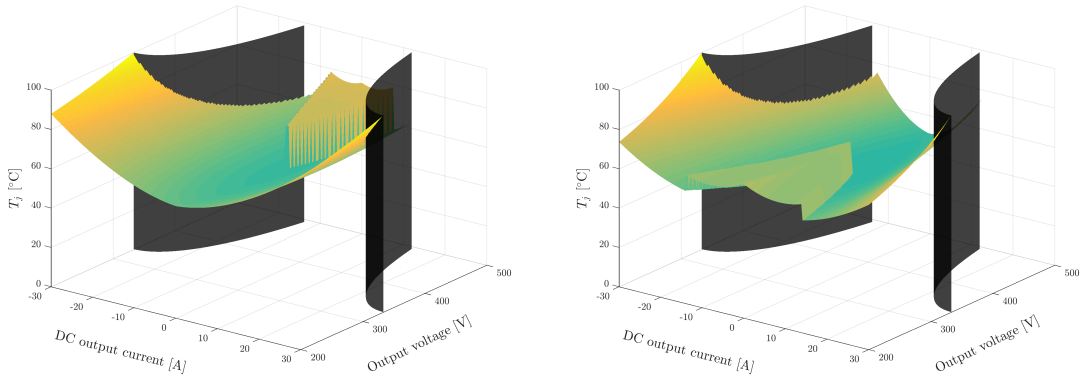
Figure 6.8: Losses at the magnetic elements of the DAB, $N = 2$ and $f_{sw} = 50kHz$



(a) HVB mosfets losses (b) LVB mosfets losses

Figure 6.9: Semiconductor losses of the DAB, $N = 2$ and $f_{sw} = 50kHz$

Table 6.1 shows how the necessary inductance is increased with increasing number of phases, as expected from Equation 6.8. However, as the current capabilities of the inductors are reduced, the inductor sizes do not change in any configuration. This is due to the necessity of a bigger inductance when a lower power is handled, see Equation 6.8. The losses of the converter can be computed, together with the resulting junction temperatures of the switches of the two bridges for every operating point, see Figure 6.9 and 6.10. The effect of the hard switching zones in both the losses and the junction temperature is seen in the different plots.

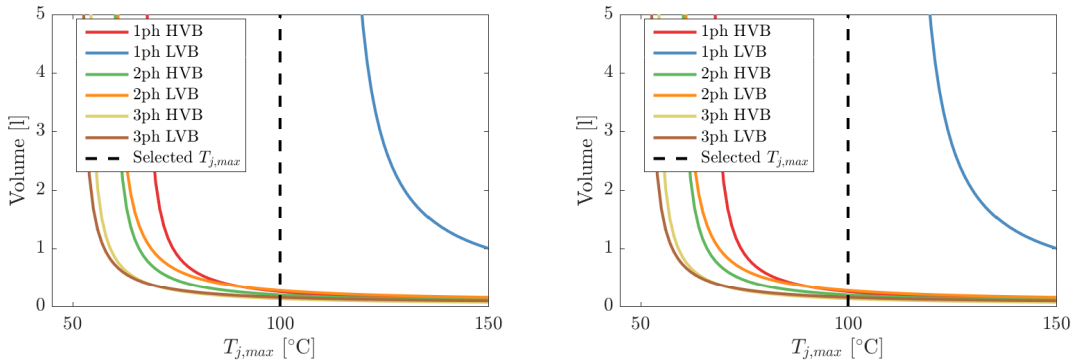


(a) HVB $T_{j,mos}$ (b) HVB $T_{j,mos}$

Figure 6.10: Semiconductor temperatures of the DAB, $N = 2$ and $f_{sw} = 50kHz$

When the losses are known, it is possible to obtain the necessary cooling system size of the converter to keep the maximum junction temperatures $T_{j,max}$ under a certain limit. The operating point with maximum losses is found when the converter LVB voltage is 333.33 V and output current is 30 A. As previously explained, the one phase version of the DAB has a significant amount of losses at the LVB, leading to a non possible design with the predefined conditions, see Figure 6.11.

The total volume of the converter is formed by the leakage inductors, the HFT, the input filtering capacitors and the cooling system, which is composed of two different heat sinks, in order to provide higher isolation and size them accordingly to the losses. Figure 6.12 shows the final size of the different configurations.



(a) $f_{sw} = 50kHz$ (b) $f_{sw} = 100kHz$

Figure 6.11: DAB cooling system size for different values of $T_{j,max}$.

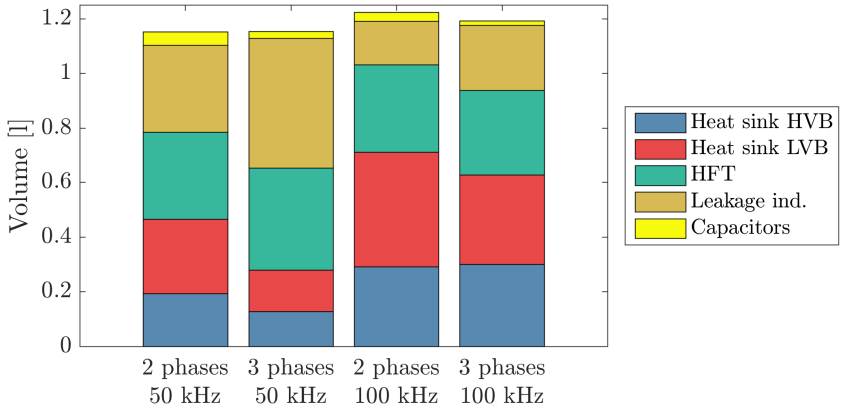
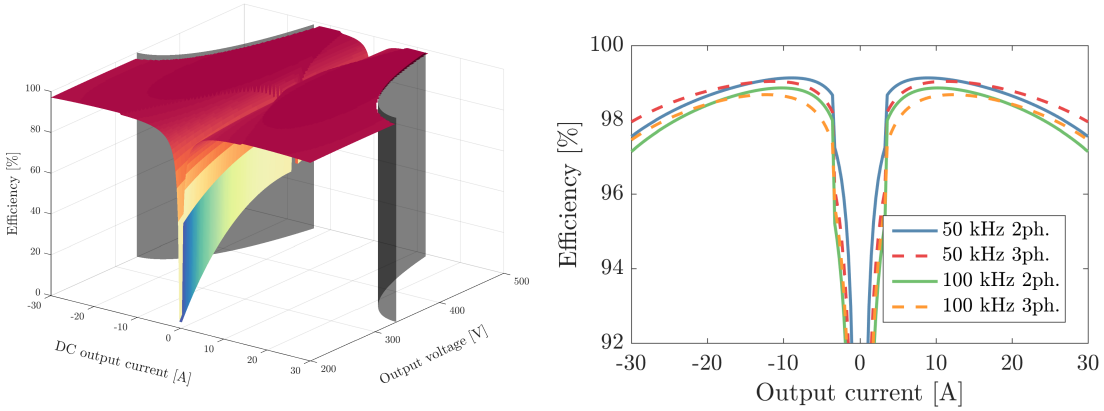


Figure 6.12: Distribution of the total volume of the different DAB configurations



(a) $N = 2$ and $f_{sw} = 50kHz$ (b) All configurations, V_{LVB} = 333.3 V

Figure 6.13: Efficiency of the DAB, 3D plot and all configurations

The resulting efficiency can be plotted, see Figure 6.13. At low currents the efficiency is very low because of the very high circulating currents in the HFL, making it undesirable to operate the converter in this operating points. The averaged efficiencies of the different converters are found on

Table 6.2, together with all the design parameters of each configuration of the DAB.

Table 6.2: Design parameters of the DAB.

Freq. [kHz]	50		100	
Phases	2	3	2	3
Mosfet HVB	20 A$^{\triangle}$	20 A$^{\triangle}$	20 A$^{\triangle}$	20 A$^{\triangle}$
Mosfet LVB	60 A$^{\triangle\triangle}$	60 A$^{\triangle\triangle}$	60 A$^{\triangle\triangle}$	40 A$^{\diamond}$
Cin [uF]	10.186	4.642	5.093	2.321
Capacitors	1	1	1	1
LVB $I_{rip,pp,max}[A]$	53.134	35.432	53.134	35.432
Volume [dm^3]	1.152	1.154	1.223	1.192
Efficiency [%]	98.45	98.42	98.03	97.94

$^{\triangle}$ Cree C2M0080120D $^{\diamond}$ Cree C2M0040120D

$^{\triangle\triangle}$ Cree C2M0025120D

6.1.3. Converter evaluation

The DAB has a high efficiency even though it is an isolated topology. The necessary high number of switches of both two and three phases configurations are compensated by the lack of diodes in the topology for the scoring, see Table 6.3.

Table 6.3: Evaluation of the DAB.

Freq. [kHz]	Weight	50		100	
Phases	-	2	3	2	3
Num Switches	3	2	1	2	1
Num Diodes	1	5	5	5	5
Num Cores	3	3	2	4	4
Capacitors	1	5	5	5	5
Efficiency	5	4	4	4	3
Volume	5	4	3	4	2
Output ripple	4	1	3	1	3
Eff. Improve	1	5	5	5	5
Controlability	3	4	4	4	4
TOTAL		**86**	**75**	**89**	**71**

The most interesting converter is the 2 phases DAB at 100 kHz which scores a total of 89 points. The efficiency is similar between all the converters, but the fact that it uses a lower number of switches and no inductor paralleling is necessary makes it score higher than the other options. The converters at 100 kHz switching frequency have higher losses, resulting in lower efficiencies and bigger heat sinks, but the final volume is very similar to due to the lower number of inductors necessary.

6.2. Interleaved Bidirectional Flyback Converter

The IBFC is a modified flyback converter with the possibility of bidirectional power flow [22]. The switch and the diode found in the conventional topology are replaced by a switch with an anti parallel diode, which enable current flow in both directions, see Figure 6.14. The topology is formed by the different switches with the anti parallel diodes and the Flyback Transformer (FBT), which has the same construction as a coupled inductor. When the converter works in charge operation and the power flows from the DC link to the EV battery, only the primary switches are controlled and the secondary diode conducts alternatively to it. On the other hand, in discharge operation, the secondary switch is controlled and it is the primary diodes that conduct when the secondary switch is OFF.

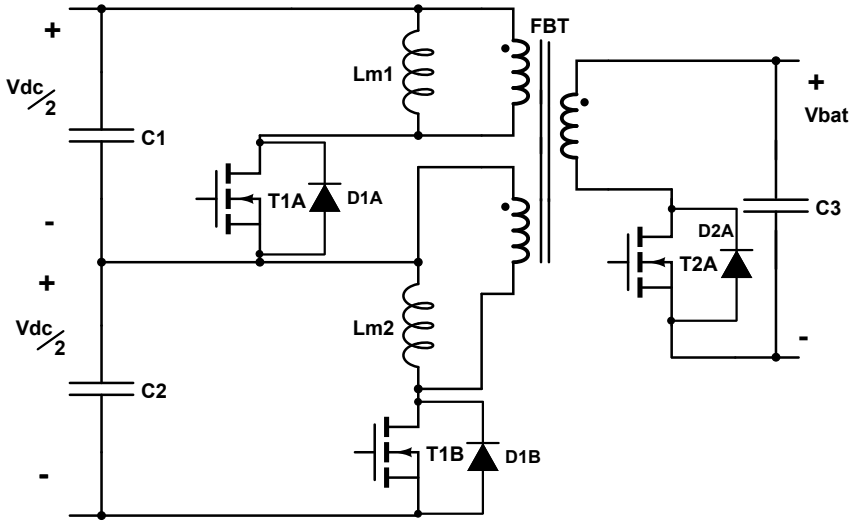


Figure 6.14: Structure of a one phase IBFC

This topology is ideally suited for lower power and lower voltage applications. Therefore, some modifications to the simple flyback on top of the bidirectionality have been performed, as in Figure 6.14, where the primary winding is splitted in two different windings creating a middle point. This is used in order to reduce the high voltage stress at the input, which is later derived. Moreover, interleaving offers the possibility to make a 10 kW EV charger; therefore, different number of phases will be considered for the design. The operating area of the IBFC is the same as the DAB; please refer to Figure 6.1. The following aspects of the converter are considered in order to rate the topology:

1. Current waveforms derivation
2. Switches and diodes requirements
3. Flyback Transformer (FBT) design
4. Input and output capacitor sizing

6.2.1. Converter design

Current waveforms derivation

The Boundary Conduction Mode (BCM) modulation technique has been selected for the IBFC; the duty cycle is fixed as in Continuous Conduction Mode (CCM) and the switching frequency is varied in order to regulate the output current. BCM is implemented as the turn on occurs at zero current and ZVS can be implemented at turn off more effectively than in Discontinuous Inductor Conduction Mode (DICM) if the topology is made to resonate. The basic operation of the flyback converter consists in energizing the FBT during the ON time of the switch, during which the diode at the secondary is

reverse biased and the current increases linearly at the magnetizing inductance L_m. Once the switch is turned off, the diode at the secondary is forwarded biased and the FBT gets de-energized, charging the battery. Due to the operation in BCM, the turn on of the converter is at zero current, reducing the switching losses of the converter.

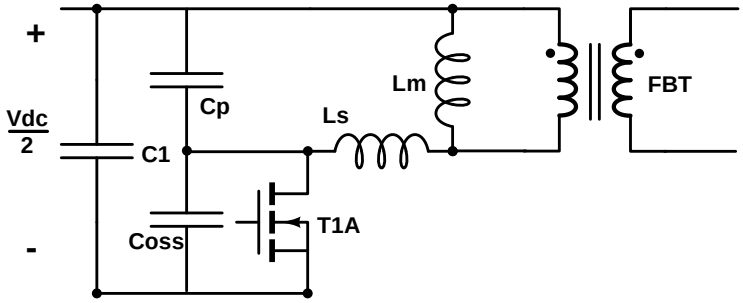
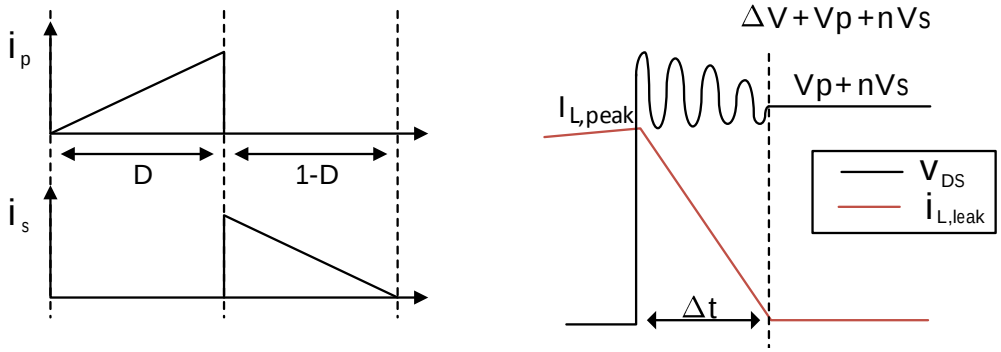


Figure 6.15: Parasitic elements present on the IBFC

The operational characteristics of the flyback are greatly impacted by the presence of parasitics in the different components [89], which have to be carefully designed. An equivalent circuit of the flyback must be derived in order to explain their effects on the converter. In Figure 6.15 the parasitic elements of both the FBT and the mosfet at the primary side of a simple bidirectional flyback are shown.

When the primary switch turns off, there is current present at the leakage inductance L_s of the FBT, which is due to the non-perfectly coupled windings of the transformer. This current is discharged through C_p and C_{oss}, the parasitic capacitances of both the FBT and the switch. As a result, the drain-source voltage of the switch is greatly increased and a mosfet with a higher voltage rating is needed. Figure 6.16 shows the current and voltage waveforms of the different elements of the IBFC.



(a) i_p and i_s (b) V_{DS} and i_s

Figure 6.16: Voltage and current waveforms of the IBFC (charging mode)

In Figure 6.16 only the waveforms in charging mode have been represented because of the inherent symmetry of the system. The extra ΔV present in the switch is due to the leakage inductance L_s of the FBT. The lower the leakage inductance the lower the voltage increment is. Equation 6.10 [89] can be used to calculate the extra necessary voltage rating due to the leakage inductance:

$$\Delta V = I_{peak}\sqrt{\frac{L_s}{C_p + C_{oss}}} \tag{6.10}$$

Where I_{peak} is the peak current at the primary, C_p is the primary parasitic capacitance and C_{oss} is the sum of both the drain to source capacitance C_{ds} and gate to drain capacitance C_{gd} of the switch. Therefore, this parameter is very difficult to predict as it depends mainly on the FBT construction, which has to be performed in such a way as to minimize the leakage inductance. In order to do so, the winding distribution should be carefully chosen in order to avoid gaps between the coils, and the air gap has to be designed to be as small as possible. Another solution is to use foil windings, which significantly reduce the space between the windings lowering the leakage inductance. Lastly, is it possible to use several types of snubber circuits or voltage clamps in order to reduce the stress in the semiconductors [90] [91]. However, in order to have a low-loss snubber, active elements have to be used increasing the overall complexity of the system.

The current waveforms of the IBFC are derived from the duty cycle. For charging operation, the duty cycle of the primary side switch is found as:

$$D = \frac{nV_s}{V_p + nV_s} \tag{6.11}$$

Where V_p is the primary side voltage, V_s the secondary side voltage and n the turns ratio of the FBT. In order to achieve the desired output current, the switching frequency is regulated. It is computed as [92]:

$$f_{sw} = \left(\frac{V_p n V_s}{V_p + nV_s}\right)^2 \frac{1}{2L_m I_s V_s} \tag{6.12}$$

Equation 6.12 can be reorganized in order to find the maximum leakage inductance that keeps the converter working in Boundary Inductor Conduction Mode (BICM), see Equation 6.13. A lower inductance could be used, but that would increase the current stresses at the components.

$$L_m = \left(\frac{V_p n V_s}{V_p + nV_s}\right)^2 \frac{1}{2f_{sw} I_s V_s} \tag{6.13}$$

The peak current can be obtained once the frequency is known, see Equations 6.14.

$$\begin{aligned} I_{p,peak} &= \frac{V_p D}{L_m f_{sw}} \\ I_{s,peak} &= n I_{p,peak} \end{aligned} \tag{6.14}$$

When the converter operates in the discharging mode, the voltages are flipped in the equations as well as the currents direction. Considering the variable switching frequency, in order to achieve low currents the converter might have to reach very high frequencies. Therefore, it has to be limited in order to avoid very high switching losses. Another option would be to implement Discontinuous Conduction Mode (DCM) when the frequency reaches a top value, but it is not considered in this project.

Switch requirements

The switches and diodes need to have the same voltage rating as they are connected in anti parallel. The minimum breakdown voltage for the semiconductors can be obtained from Figure 6.16(b) and Equation 6.10:

$$V_{DS,p} = V_{AK,p} = V_{p,max} + nV_{s,max} + I_{peak,p}\sqrt{\frac{L_{s,p}}{C_{p,p} + C_{oss,p}}}$$
$$V_{DS,s} = V_{AK,s} = V_{s,max} + \frac{V_{p,max}}{n} + I_{peak,s}\sqrt{\frac{L_{s,s}}{C_{p,s} + C_{oss,s}}} \quad (6.15)$$

Where $I_{peak,p}$ and $I_{peak,s}$ are the peak currents at the primary and secondary sides of the converter when the switches are operating, and C_p and C_{oss} the parasitic capacitances of the FBT and the switches in both the primary and the secondary. Therefore, the minimum necessary value of breakdown voltage depends on the leakage inductance of the transformer, making it difficult to predict. With Equation 6.15 it is possible to explain why the input voltage of the FBT has to be shared between two different windings and mosfets. A full DC link voltage plus the output voltage would make the minimum necessary voltage ratings of the switches be 1250 V, even with a FBT turns ratio of unity, which would imply having to consider mosfets with higher ratings than 1200 V. The turns ratio n_1/n_2 needs to be kept low in order to keep the reflected voltage in the primary within limits. Without taking into account ΔV, for a turns ratio of 2 the required breakdown voltage is 875 V for both sides, leaving 325 V for further increase of the voltage due to the leakage inductance.

The currents through the switches and diodes depend on the operating point of the converter. The maximum current occurs at 333.33 V, which is the minimum voltage at which the converter operates at full power.

Flyback Transformer design

The Flyback Transformer (FBT) turns ratio n_1/n_2 can also be optimized in order to reduce the stress of the different elements. This is a difficult task in the present topology due to the already high voltage and current stresses applied to the semiconductors. A lower turns ratio number reduces the voltage stress at the primary while increasing the voltage stress at the secondary, see Equation 6.15. With respect to the currents, a turns ratio that keeps the applied duty cycles (Equation 6.11) as close as 0.5 as possible in both current directions is desired, as lower peaks are reached in the semiconductors. A good trade-off for the turns ratio n is to have double the turns in the primary than in the secondary (n = 2), resulting in the same voltage stress of 875 V in both the primary and the secondary sides, leaving room for the extra ΔV due to the leakage inductance. The duty cycles when operating in charging and discharging mode are not completely symmetrical but the maximum difference is around 0.07, making it sufficiently balanced.

DC link filter capacitance

The input capacitance, which is connected to the DC link, can be calculated from the sum of the current of the different interleaved converters. It is wanted that the input voltage ripple is always under the 0.25% of the DC link voltage. Considering that the input current ripple for every working condition of the converter is already known as shown in Figure 6.16(a), the application of the following equation results in the change of voltage produced in the capacitors:

$$V_p(t) = \frac{Q(t)}{C} = \frac{1}{C}\int_{t_0}^{t} I_{cap}(t)dt + V_p(t_0) \quad (6.16)$$

The voltage ripple can therefore be kept under the maximum 1.875 V peak to peak ripple in the DC link. The different switching frequencies and ripple currents in the overall operating range of the converter must be considered in order to find the point where the voltage increment is maximum.

Efficiency Improvement

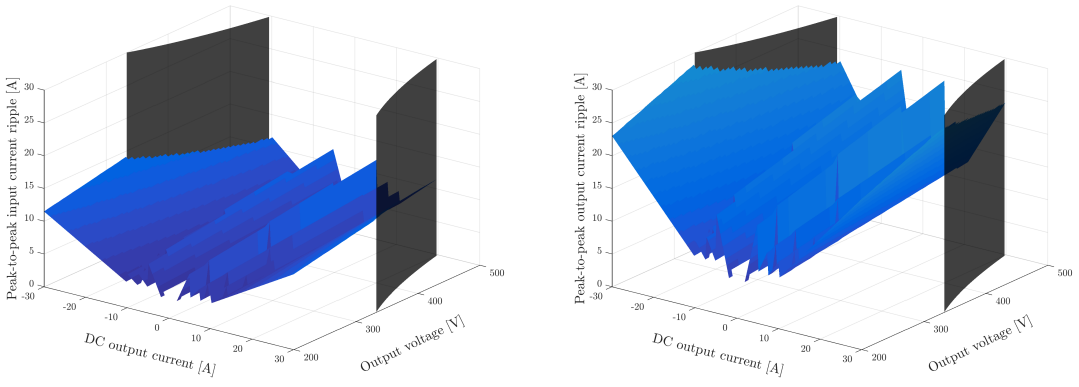
The IBFC topology can be improved in different ways:

- **Passive lossless snubbers [93].** Different snubber topologies can be implemented, which do not enhance the efficiency of the system but reduce the ΔV, reducing the necessity of a perfect inductor design. The leakage energy is either derived to the positive bus or the negative bus, resulting in higher efficiency and lower EMI respectively.
- **Active clamp ZVS [94].** The clamp capacitor captures the leakage energy, and the system recirculates it back to the input, resulting in a virtually lossless snubber. Moreover, it is possible to achieve ZVS if the switching sequence is carefully selected.

Therefore, there is the possibility to enhance the efficiency of the converter. However, due to the high number of phases and semiconductors, and the necessity of adding an extra switch to each of them in order to increase the efficiency, the implementation of an actively clamped topology turns out to be very costly. As a consequence, a rating of 2 has been chosen for the IBFC.

6.2.2. Results

The IBFC has been designed for four, five and six phases. A lower number of phases is not possible due to the E65 core size restriction. The BCM requires a higher switching frequency when the output current of the converter is reduced, resulting in increased losses and reduced efficiency. The minimum BCM frequency has been selected to be 50 kHz, which occurs at the lowest output voltage and maximum current. As the current is reduced the switching frequency is increased, and phase throttling is applied when high frequencies are reached,meaning that the number of active phases N_{active} is reduced. A throttling frequency of 150 kHz has been selected, ensuring that not very high switching frequencies are reached. Moreover, at low power the switching frequency also needs to be limited in order not to increase to infinity when really low currents are wanted, even when only using one phase. This maximum overall frequency is kept at 200 kHz. The results of applying a throttling system like this in the converter in terms of ripple currents are shown in Figure 6.17.



(a) Primary side (b) Secondary side

Figure 6.17: Current ripple at both sides of the 4 phases IBFC

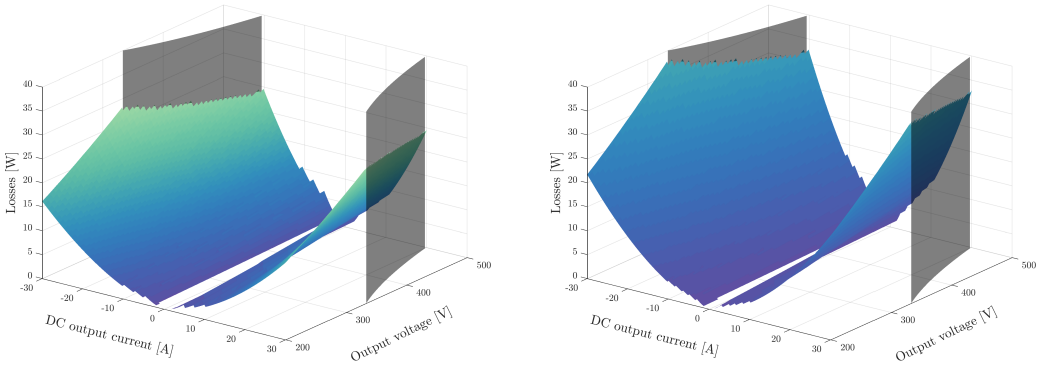
Due to the limitation in the switching frequencies, the converter can not operate at very low power. This is seen in Figure 6.17, where the ripple currents at very low currents are not shown, because the converter is not working. This is not considered to be a major drawback of the topology as EV charging is supposed to work at higher power when charging or discharging. The FBT design has

been done following the steps explained in Section 4.2. The split primary winding is treated as a single winding which is later added a middle point connection.

Table 6.4: Parameters of the FBT of the different IBFCs.

Phases	4	5	6
L_m [mH]	0.454	0.567	0.681
Core	E 65	E 65	E 55
Material	R	R	3C92
n_1/n_2	40 / 20	44 / 22	52 / 26
Air gap [cm]	0.120	0.116	0.088
B_{max} [T]	0.297	0.270	0.350
$Rac, 1$ [Ω]	0.048	0.05	0.098
$Rac, 2$ [Ω]	0.012	0.015	0.025

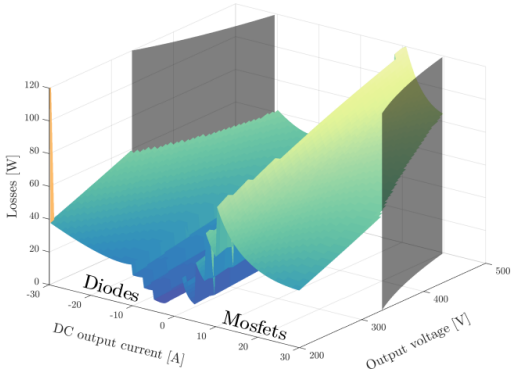
Table 6.4 shows how the size of the transformer is only slightly reduced; as stated in Equation 6.13, a higher number of phases has a bigger maximum inductance. The most important reduction are the peak currents present in the converter, as the average current differences between the different number of phases is not considerable. Figure 6.18 shows the losses in all the FBTs for the four and six phases configurations.



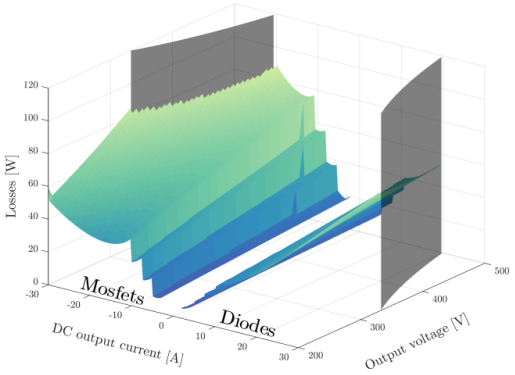
(a) 4 phases (b) 6 phases

Figure 6.18: Losses in the magnetic elements of the IBFC

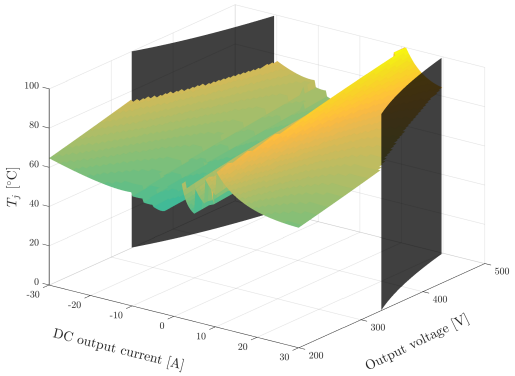
The losses of the semiconductors on the converter can be computed, see Figure 6.19. The losses are higher in the side where the switches are working. Therefore, the cooling system size depends on the losses of the switches because the switching losses of the mosfets are higher than those of the SiC diodes.



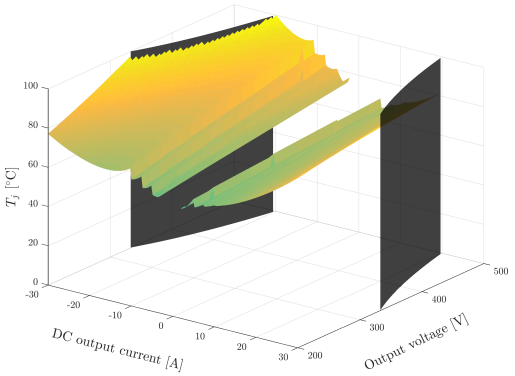
(a) Primary side semiconductors losses



(b) Secondary side semiconductors losses



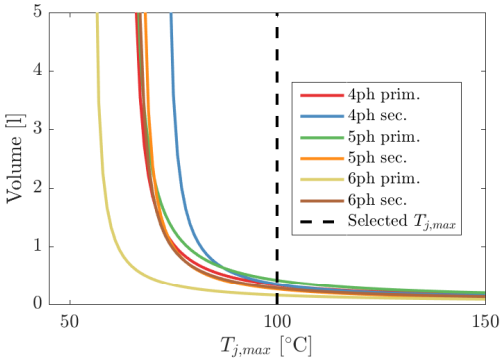
(c) Primary side $T_{j,mos/dio}$



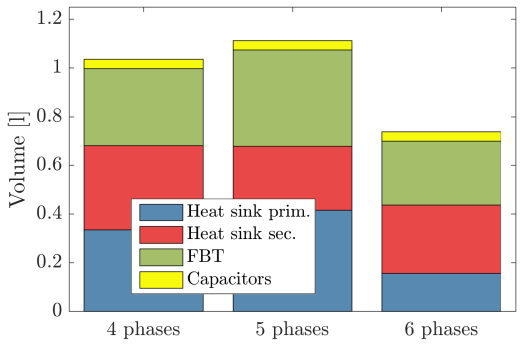
(d) Secondary side $T_{j,mos/dio}$

Figure 6.19: Semiconductor losses and temperatures of the IBFC, 4 phases

When the losses are known, it is possible to obtain the necessary cooling system size of the converter to keep the maximum junction temperatures $T_{j,max}$ under a certain limit. The operating point with maximum losses is found when the all the phases are operating at almost the throttle frequency of 150 kHz at 500 V, see Figures 6.19(c) and 6.19(d).



(a) Cooling system size ($T_{j,max}$)



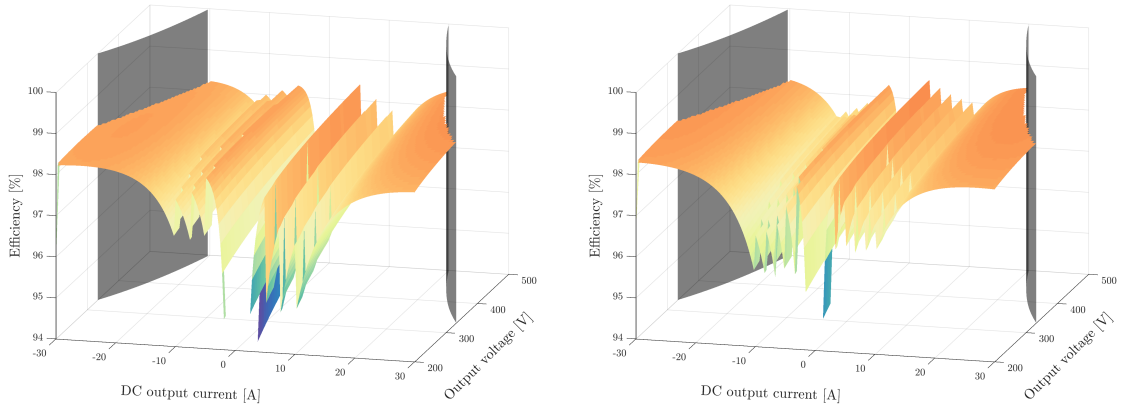
(b) Size distribution

Figure 6.20: IBFC system size

The total volume of the converter is formed by the FBT, the input filtering capacitors and the

cooling system. For the calculation of the input filter capacitors, the worst case scenario has to be taken into account, as the current ripples when the converter operates can be also high. In order to find that point, the point with maximum $\frac{I_{in,pp}}{N_{active}F_{sw}}$ is found and selected for the calculation. Figure 6.20(b) shows the size of the different versions.

The resulting efficiency can be plotted, see Figure 6.21. The plots show that the efficiency could be increased by extending the operation range of each phase (by increasing the throttle frequency), but that would imply an increase of the ripple currents present at the output of the converter, see Figure 6.17(b). The averaged efficiencies of the different considered converters are found on Table 6.5, together with the rest of the design parameters of the different configurations of the IBFC.



(a) 4 phases (b) 6 phases

Figure 6.21: Efficiency of the four and six phases IBFC

Table 6.5: Design parameters of the IBFC.

Phases	4	5	6
Mosfet primary	40 A$^{\triangle}$	40 A$^{\triangle}$	12.5 A$^{\triangle\triangle}$
Mosfet secondary	40 A$^{\triangle}$	40 A$^{\triangle}$	40 A$^{\triangle}$
Diode primary	20 A $\diamond$	20 A $\diamond$	14 A$\diamond\diamond$
Diode secondary	25.5 A*	25.5 A*	25.5 A*
Cin [uF]	11.983	10.303	7.732
Capacitors	2	2	2
$I_{rip,pp,max}$LVB	28.205	22.564	18.892
Volume [dm^3]	1.036	1.112	0.737
Efficiency	97.99	97.86	98.03

$^{\triangle}$ Cree C2M0040120D

$^{\triangle\triangle}$ Cree C2M0160120D

* Cree C4D20120A

$\diamond$ Cree C4D15120A

$\diamond\diamond$ Cree C4D10120A

6.2.3. Converter evaluation

The IBFC has a high efficiency even though it is typically a low power topology. The main problem of this topology is the FBT design, which has a strong influence on the rest of the elements of the converter. If the inductor design is carefully performed, the IBFC scores quite high, see Table 6.6.

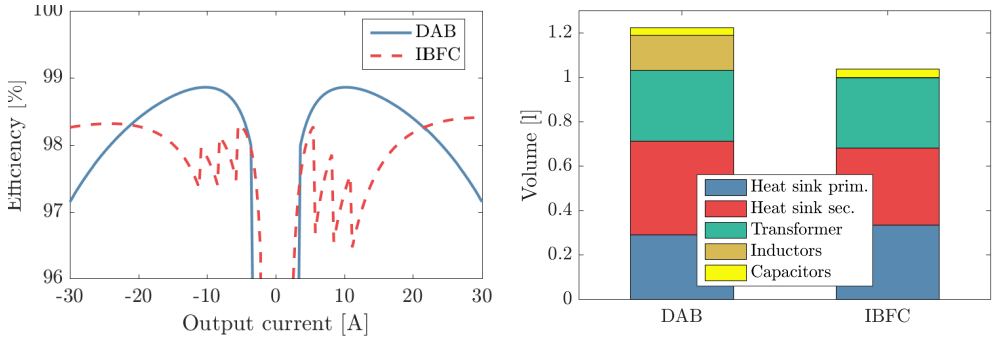
Table 6.6: Evaluation of the IBFC.

Phases	Weight	4	5	6
Num Switches	3	3	2	2
Num Diodes	1	2	1	1
Num Cores	3	4	3	3
Capacitors	1	5	5	5
Efficiency	5	3	3	4
Volume	5	4	3	5
Output ripple	4	4	4	5
Eff. Improvement	1	2	2	2
Controlability	3	3	3	3
TOTAL		**90**	**78**	**93**

The IBFC that has a higher rating is the six phases one. However, although the efficiency is similar between all the converters, in the six phases converter it is just above 98%, making it score five points more than the other two configurations in terms of efficiency. Therefore, it is better to choose the 4 phases IBFC, as it scores 90 points, just three points lower than the 6 phases configuration. The reduction in switches, diodes and FBTs makes it more attractive than the six phases one.

6.3. Conclusion

In this chapter two converters for the EV port have been designed and compared: the Dual Active Bridge (DAB) and the Interleaved Bidirectional Flyback Converter (IBFC), whose optimal configurations results can be found in 6.22. Both converters perform similarly, but the IBFC and its higher number of phases has lower current ripple at the electric vehicle battery, which is necessary in order to increase the battery life. Therefore, it is concluded that the best solution is the IBFC.



(a) Efficiency (b) Volume

Figure 6.22: Results of the optimal topologies configurations of the PV port.

7

Grid Port Analysis

In this chapter the three different inverter/rectifier candidates listed in Section 2.3.3 are analyzed and rated. The three converters are the Two Level Converter (2LC), found on Section 7.1, the Three Level Neutral Point Clamped Converter (3LNPC²) which is explained on Section 7.2, and finally the Three Level T-Type Converter (3LT²C), which is studied on Section 7.3. Some operating waveforms of the DC-AC converters covered in this chapter can be found on Appendix E due to space limitations. The requirements of the Grid port are:

- 3 phase 400 V mains connection
- 10 kW 16 A max input/output
- Bidirectional

7.1. Two Level Converter

The Two Level Converter (2LC) is the basic topology for converting DC to AC and vice versa, also known as Voltage Source Inverter (VSI). The structure of this converter is shown again in Figure 7.1 for surveyability. It is composed of six switches with their respective flywheel diodes, which allow current in both directions independently of the clamped point of the bus.

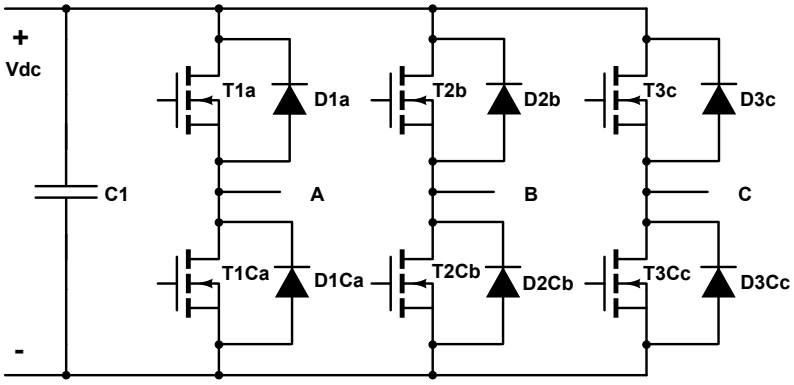


Figure 7.1: Structure of the 2LC

Figure 7.1 does not show the required output filter, as the same filter topology is used for all the compared converters. The LCL filter for the 2LC is discussed later in this section. The DC Link

voltage is split by two equal capacitors, in order to create a middle point where the neutral line is connected. This reduces leakage currents to the ground via the parasitic capacitance of the PV panels, see Section 2.5. However, in Figure 7.1 only one capacitor is shown as it is inverter currents filtering capacitor. The different aspects which are reviewed to design and rate the converter are:

1. Modulation techniques review
2. Switch and diode requirements
3. Loss distribution
4. Cooling system size
5. Total Harmonic Distortion (THD)
6. Leakage currents
7. Efficiency improvement

7.1.1. Converter design

Modulation method

The modulation method of the inverter/rectifier is one of the main aspects of a DC-AC converter, as it defines the switching behavior and thereby the total losses of the converter, which are mainly conduction losses and switching losses. The easiest control scheme technique is Sinusoidal Pulse-Width Modulation (SPWM) [23], where a sinusoidal waveform (reference) is compared against a triangular waveform (carrier), as shown on Figure 7.2, where the carrier waveform frequency has been intentionally reduced for its visualization. The carrier frequency is equal to the switching frequency, while the reference frequency is the modulation (grid) frequency.

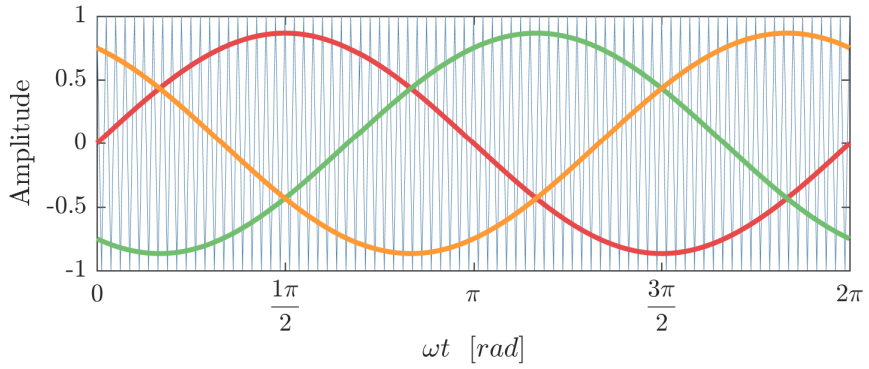


Figure 7.2: Sinusoidal carrier versus triangular wave in SPWM

In Figure 7.2 the three reference waveforms are shown, which indicate the switching state of each leg. When the reference signal is greater than the triangular waveform, the leg is in the P state, with the output connected to the positive bus. When the sinusoidal signal is lower than the carrier waveform, the output is clamped to the negative bus of the 2LC. This comparison has to be performed for every sample period n. The number of samples n is related to the discreet implementation of the carrier signal, achieving higher accuracy when a greater number of points is considered for every switching period. This method of bipolar switching is simple and generates a sinusoidal output which is compromised of three different levels in the line to line waveforms. The switching states for every sampling period for each leg are obtained using the following equation:

$$\vec{S_n} = \begin{bmatrix} \begin{cases} S_{a,n} = P & Ref_{a,n} \geq Carr_n \\ S_{a,n} = N & \text{otherwise} \end{cases} \\ \begin{cases} S_{b,n} = P & Ref_{b,n} \geq Carr_n \\ S_{b,n} = N & \text{otherwise} \end{cases} \\ \begin{cases} S_{c,n} = P & Ref_{c,n} \geq Carr_n \\ S_{c,n} = N & \text{otherwise} \end{cases} \end{bmatrix} \tag{7.1}$$

Space Vector Pulse-Width Modulation (SVPWM) technique [95] was introduced as a better modulation in order to increase DC bus utilization factor and reduce harmonic distortion in three phase inverters. In SVPWM methods, the voltage reference is provided using a revolving reference vector, which is obtained using Clarke transformation [96]. This reference vector is compared against the three nearest voltage vectors that the inverter can provide, which in the case of a 2LC sum up to a total of eight different options, being two of them zero vectors. Once the three vectors have been identified, the time each vector is applied is calculated trigonometrically, as the sum of the three vectors is wanted to be the same as the reference vector. This procedure is shown in Figure 7.3, where the V_{ref} output vector is inside Sector 1 and is created by a combination of vectors V_1, V_2 and V_0 or V_7. The method is not further explained in this report as a lot of research has been performed about SVPWM.

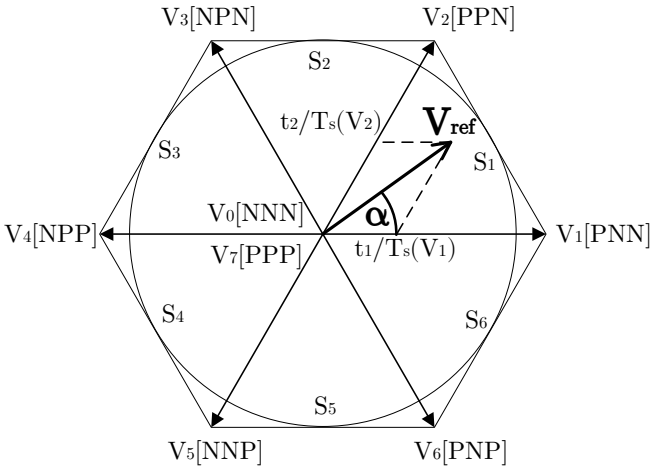


Figure 7.3: Working principle of the Space Vector Modulation (SVM)

SVPWM is a method which requires intensive computation due to the high amount of operations needed in order to obtain the Pulse-Width Modulation (PWM) signal. Some publications have been made where the traditional SPWM is compared to SVPWM [97], where their relation is analyzed. Thereby, modulation methods which combines SVPWM with triangular carrier comparison have been introduced, reducing the need for computational power and the system complexity. In order to have SVPWM like performance, a common mode voltage is added to the original sinusoidal waveform, which can be obtained directly from the mains. For two-level inverters, the common mode offset voltage that has to be added to the three sinusoidal references is obtained as [97]:

$$Offset = -\left[\frac{V_{max} + V_{min}}{2}\right] \tag{7.2}$$

Where V_{max} and V_{min} are the maximum and minimum voltages of the three phases at that sample time. This modification centers the active space vectors in the switching period, and hence matches

carrier modulation to optimized SVM. A modified reference waveform is obtained from the initial sinusoidal waveform, which makes the converter switch like if SVPWM was used, see Figure 7.4.

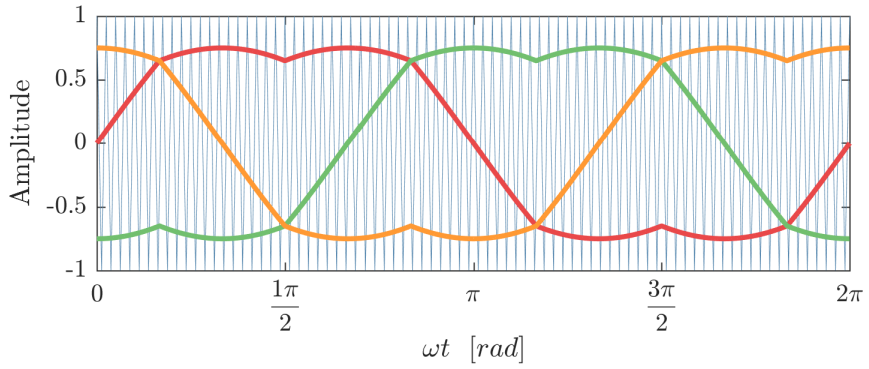


Figure 7.4: SVM like reference signal versus carrier signal

This modulation technique is the most suitable when using the inverter for off-grid solutions or where the leakage currents are not a big problem. Considering that the middle point connection to the neutral of the line has some drawbacks, as explained previously in this report on Section 2.5, it is also advisable to consider other modulation techniques which reduce the Common Mode Voltage (CMV) and therefore current leakages. One of those methods is Near State Pulse-Width Modulation (NSPWM) for 2LC [36]. Compared to SVPWM, this method does not use the zero vectors, and instead the nearest voltage vectors are used. In order to do so, zone identification is necessary, increasing the overall computational cost of the modulation. The sectors are however different from the SVPWM ones shown in Figure 7.3, in order to make use of the three nearest voltage vectors:

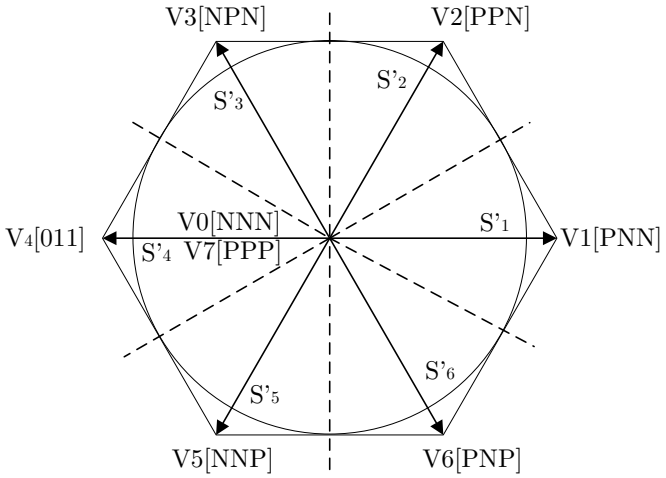


Figure 7.5: Sectors of the NSPWM

The sectors are displaced 30 degrees, for example sector one ranges from -30 to 30 degrees. The vectors used in this sector are V_6, V_1 and V_2. In [36] a scalar method which is based on a reference and carrier comparative is stated. In order to implement this modulation, the reference signal is adapted in the same way as the Discontinous Pulse-Width Modulation 1 (DPWM1) method [98], where the voltage offset is obtained as:

$$Offset = sign(V_{highest}) - V_{highest} \tag{7.3}$$

Where V_{max} is in this case the highest voltage of the three phases, including positive and negative voltages. The carrier waveform needs to be modified in a per phase basis depending on the sector. For more information please refer to [36] section III where the scalar implementation of the method is explained.

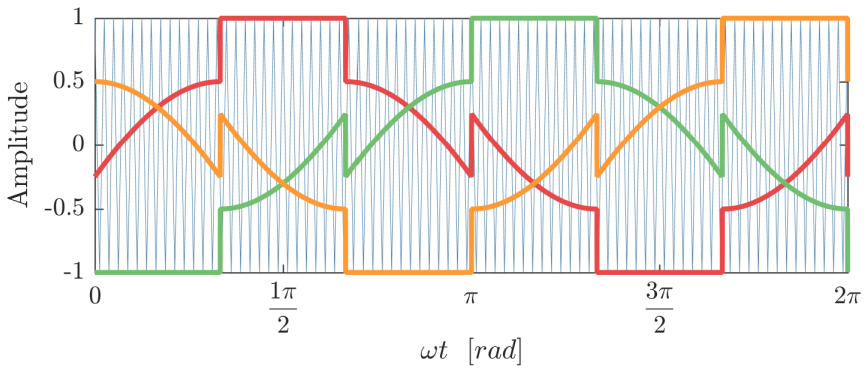


Figure 7.6: Reference waveforms and carrier signal of the NSPWM

This modulation technique has two main advantages. The first one is the previously mentioned reduction of the CMV voltage due to the elimination of the zero vectors. The second one is related to the efficiency, as similarly to DPWM1 some switches are clamped for 60 degrees, reducing the amount of switching losses produced.

The carrier waveform can also be modified in order to obtain different switching patterns. Figure 7.7 shows different carrier waveforms that can be applied and the resulting gating signal for two time periods. If a sawtooth waveform is used, the gate signals are left positioned or right positioned on the switching period, as shown in Figure 7.7 $a)$ and $b)$ respectively. If instead, a triangular waveform of period equal to the switching period is used, the gate signals are positioned in the middle, offering the lowest Total Harmonic Distortion (THD), as shown in $c)$. However, it is also possible to use a triangular waveform of twice the switching period, moving the gate signals to the right side on one switching period and to the left side on the following one, consequently reducing switching losses because only turn-on or turn-off of the switch takes place at one sample time. This is shown in 7.7 $d)$. Despite of the reduction of the switching losses of this method, the final THD increases.

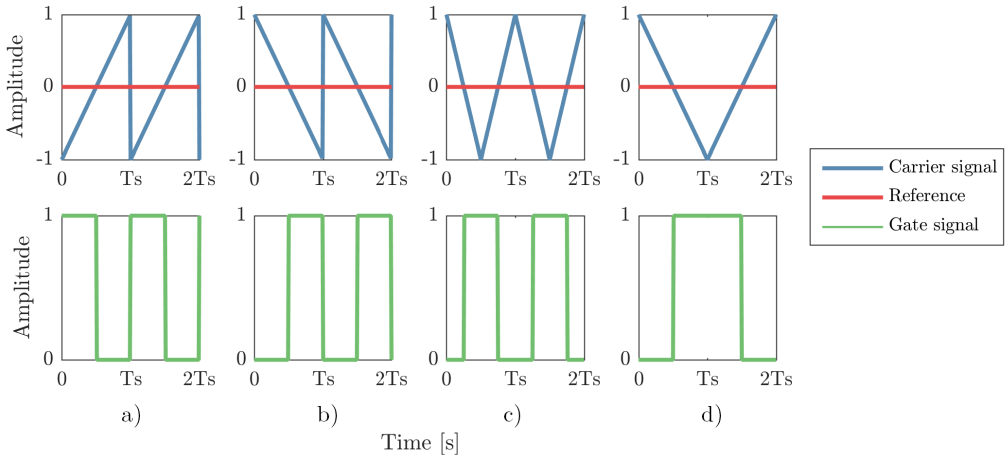


Figure 7.7: Different triangular waves and resulting gate signals

After the analysis of modulation techniques performed in this section, it is possible to implement

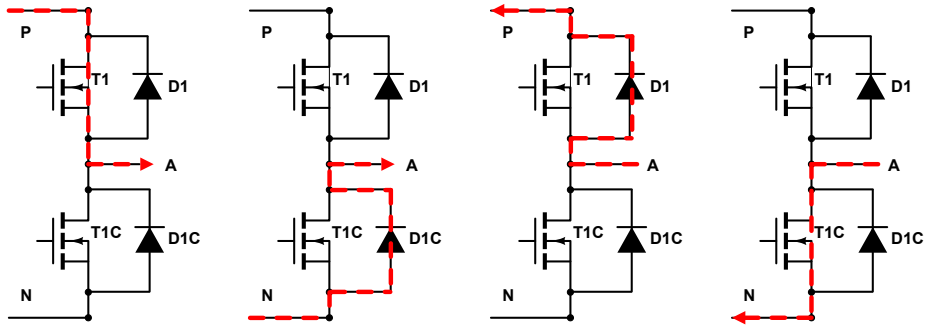
these techniques in order to obtain the final rating of the converter for the different modes of operation. In the case of the 2LC, both SVPWM and NSPWM are considered. The voltage and current waveforms of the 2LC can be found on appendix E.1 as well as the gate signals and other relevant information.

Switch and diode requirements

The voltage that that every switch and antiparallel freewheling diode has to stand is the same as the DC link voltage. The current through the the semiconductors follows the same waveform as the output or input current of the converter, which is directly obtained from the maximum power capability of the converter. The conducting element depends both on the leg state and the output current direction, fact which is explained in the next section.

Loss distribution

The losses have been calculated using the method found in Section 3.3 from this thesis. In order to know which components conduct or switch in each transition, the two operation modes for each leg and the possible current directions are shown in Figure 7.8. Only one leg is considered in the analysis, as the symmetrical operation of the converter makes it possible to only perform the calculations for one and later assign the same values to the two other legs, which are displaced 120 degrees each.



(a) $I_{out} \geq 0$, P (b) $I_{out} \geq 0$, N (c) $I_{out} < 0$, P (d) $I_{out} < 0$, N

Figure 7.8: Switching states of the of the 2LC

From every figure it is possible to determine which elements are conducting and the switching elements for every possible transition, producing Tables 7.1 and 7.2 respectively. These tables together with the equations in Section 3.3 have to be used in combination in order to obtain the conduction power losses and switching energy loss at every time step.

Table 7.1: Conduction losses of the 2LC

Switching State	Conduction losses
$I_{out} \geq 0$	
P	$P_{cond,T1}$
N	$P_{cond,D1C}$
$I_{out} < 0$	
P	$P_{cond,D1}$
N	$P_{cond,T1C}$

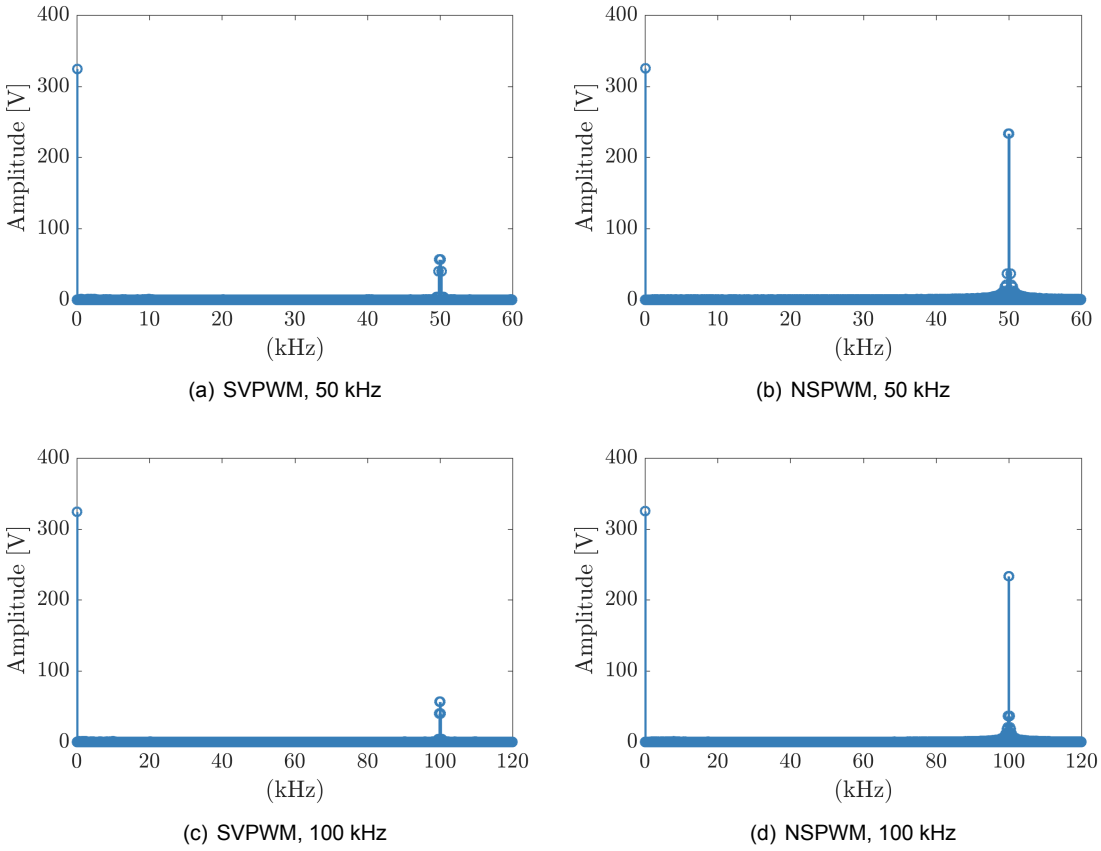
Table 7.2: Switching losses of the 2LC

Switching Transition	Loss energies
$I_{out} \geq 0$	
P → N	$E_{off,T1}$
N → P	$E_{on,T1}$, $E_{off,D1C}$
$I_{out} < 0$	
P → N	$E_{off,T1C}$,$E_{off,D1}$
N → P	$E_{on,T1C}$

This information, together with the switch state in each switching period, makes possible the calculation of the losses in every operating point of the converter, both for inverter mode of operation and rectifier mode. The current through the switches is derived from the power of the converter and the power factor, considered to be unity throughout the report.

THD and output/input filter

The THD analysis has been performed using the Simulink FFT Analysis Tool from the SimpowerSystems Toolbox from the Matlab package. With this tool it is possible to analyze the voltage waveform and obtain the Fourier analysis magnitudes and frequencies of the waveform. When it is applied to the phase voltages obtained for both modes of operation of the 2LC, the results can be plotted.



(a) SVPWM, 50 kHz

(b) NSPWM, 50 kHz

(c) SVPWM, 100 kHz

(d) NSPWM, 100 kHz

Figure 7.9: FFT of the 2LC for both modulation techniques.

Figure 7.9 reveals how the harmonic content around the switching frequency is much higher in the NSPWM. Moreover, the highest harmonic in the SVPWM is found in the $(m_f\text{-}2)^{th}$ harmonic while the NSPWM harmonic is the $(m_f\text{-}1)^{th}$. The effect of doubling the switching frequency moves the most important harmonic further in the spectrum, reducing the importance. Therefore, a higher switching frequency is desired for the minimization of the THD.

DC side filter capacitor

The DC side capacitor must filter the ripple current in the DC link due to the switching behavior of the three phase inverter. The current ripple through the capacitor depends on the output currents of the three phases and the voltage ripple applied to the output LCL filter of the converter. The capacitor current I_{cap} can be given as [99]:

$$I_{cap} = I_{inv} - I_{dc} \tag{7.4}$$

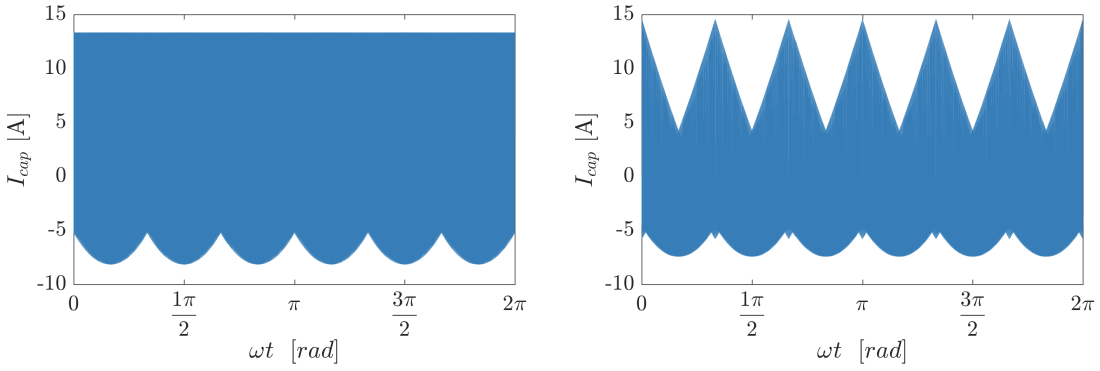
Where I_{inv} is the current of the 2LC and I_{dc} is the current of the source, which is constant in steady state operation of the converter. Assuming a loss-less system, the DC current is found via the power of the system and DC link voltage. The current through the 2LC is derived from the switching states of the converters and the current at the different phases, see Equation 7.5.

$$I_{inv} = \begin{pmatrix} 1 & if & S_{a,n} = P \\ 1 & if & S_{b,n} = P \\ 1 & if & S_{c,n} = P \end{pmatrix} \begin{pmatrix} I_{a,n} & I_{b,n} & I_{c,n} \end{pmatrix} \tag{7.5}$$

When the three legs share the same state, the 2LC I_{inv} current is zero and the capacitors are charged. On the other hand, when the switching states are different, the current depends on the number of active switches at the top and the bottom and the output current. The output current, at the same time, depends on the voltage ripple of the converter and the filter. As the voltage output of the converter is known, the ripple current at the output can be derived and superimposed to the output current:

$$I_x = I_{x,sin} + I_{x,rip} \tag{7.6}$$

Where the x term makes reference to each of the three phases of the system. The capacitor current is shown in Figure 7.10 for both modulation techniques. As expected, NSPWM requires of a bigger filter compared to SVPWM.



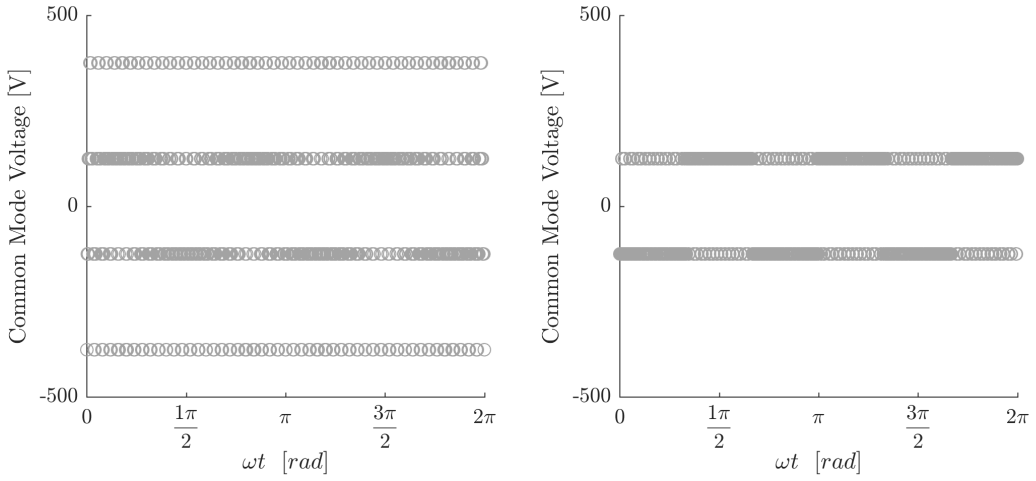
(a) SVPWM, inverter mode

(b) NSPWM, inverter mode

Figure 7.10: Input capacitor current of the 2LC, F_{sw} = 50 kHz

Leakage current

Leakage current is considered to be lower in the case of NSPWM due to its ability of reduction of the Common Mode Voltage (CMV). When using NSPWM the CMV jumps between plus and minus one sixth of V_{dc} depending on if the voltage vector is odd or even. On the other hand, when using SVPWM, when the zero vectors are active the CMV reaches plus and minus $V_{dc}/2$, see Figure 7.11



(a) SVPWM (b) NSPWM

Figure 7.11: Common Mode Voltage of the 2LC

Therefore, a rate of 4 is given to the 2LC operated with NSPWM while a rate of 3 is given to the 2LC operated with SVPWM. The lower grade of the topology working in SVPWM, although it has the middle point connected to ground, is because this solution does not ensure a current leakage under limits, which have been explained in Section 2.5. The use of NSPWM does not ensure a constant CMV at the output of the converter either, and therefore it is considered to perform better, without ensuring the complete elimination of the leakage currents.

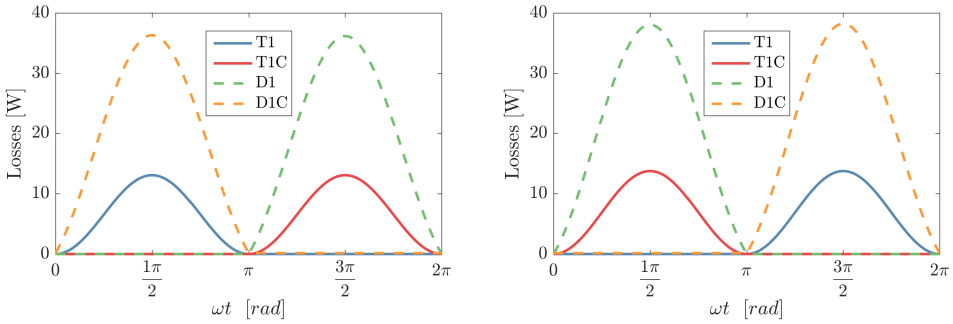
Efficiency improvement

Some search has been performed in order to find methods to improve the efficiency of inverters and rectifiers. Most of the research is focused in modulation techniques like the Discontinous Pulse-Width Modulation (DPWM) which reduce the switching losses, which has already been considered with the NSPWM. Another method is to use different hardware depending on the voltages and current ratings of the converter, but considering that SiC semiconductors are being used for the design there is not a lot of improvement margin in this aspect. The last possibility is the use of a different topology like the ones on the next two sections of this chapter . A rating of one is given to the converter as the possibility to improve the efficiency is very small.

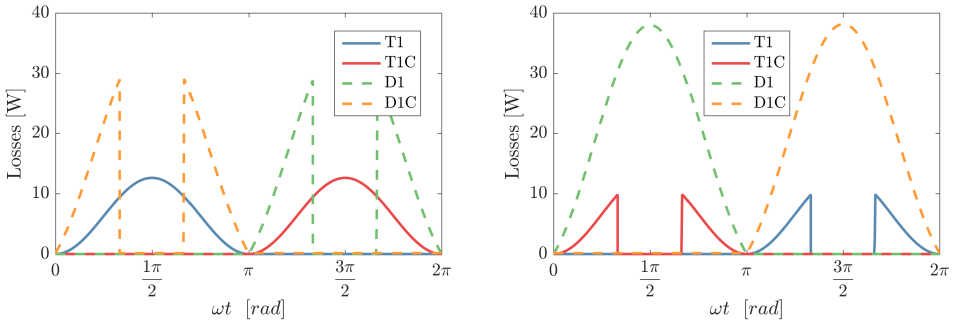
7.1.2. Results

The analysis of the converter has been done for both SVPWM and NSPWM modulation techniques and a switching frequencies of 50 kHz and 100 kHz. Due to the high amount of plots necessary to show all behaviors only 50 kHz switching frequency plots are shown in this section. When using 100 kHz as switching frequency the main changes are in switching losses, which doubles, and filter size, which is reduced. The method used can compute the losses at different power factors. However, a unity power factor is considered for the calculation of the losses as it is the preferred mode of operation of the multiport converter.

Conduction losses are shown in Figure 7.12 for both modulation techniques and inverter and rectifier modes of operation. Both modes are considered separately because the components that conduct or switch are different. These plots are shown as if the losses were constant throughout the whole cycle. However, this has been done for visualization purposes. In reality, the switches or diodes are not conducting all the time, because it depends in the switching duty cycle at the moment.

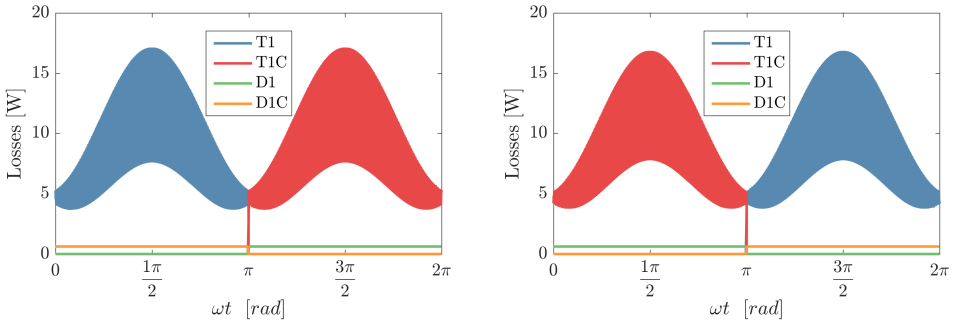


(a) SVPWM, inverter mode (b) SVPWM, rectifier mode

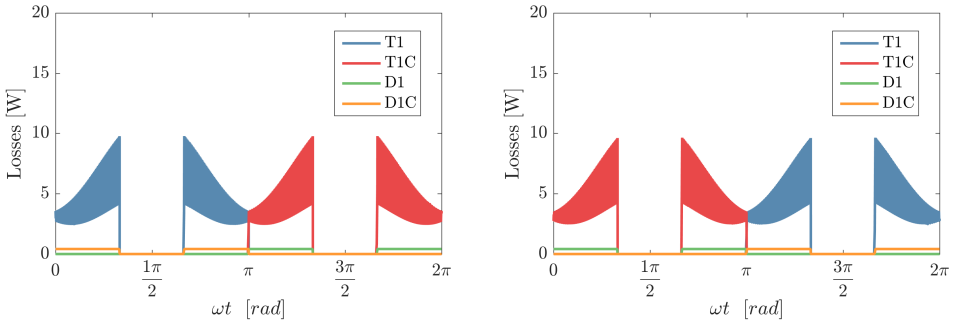


(c) NSPWM, inverter mode (d) NSPWM, rectifier mode

Figure 7.12: Conduction losses of the 2LC, F_{sw} = 50 kHz



(a) SVPWM, inverter mode (b) SVPWM, rectifier mode



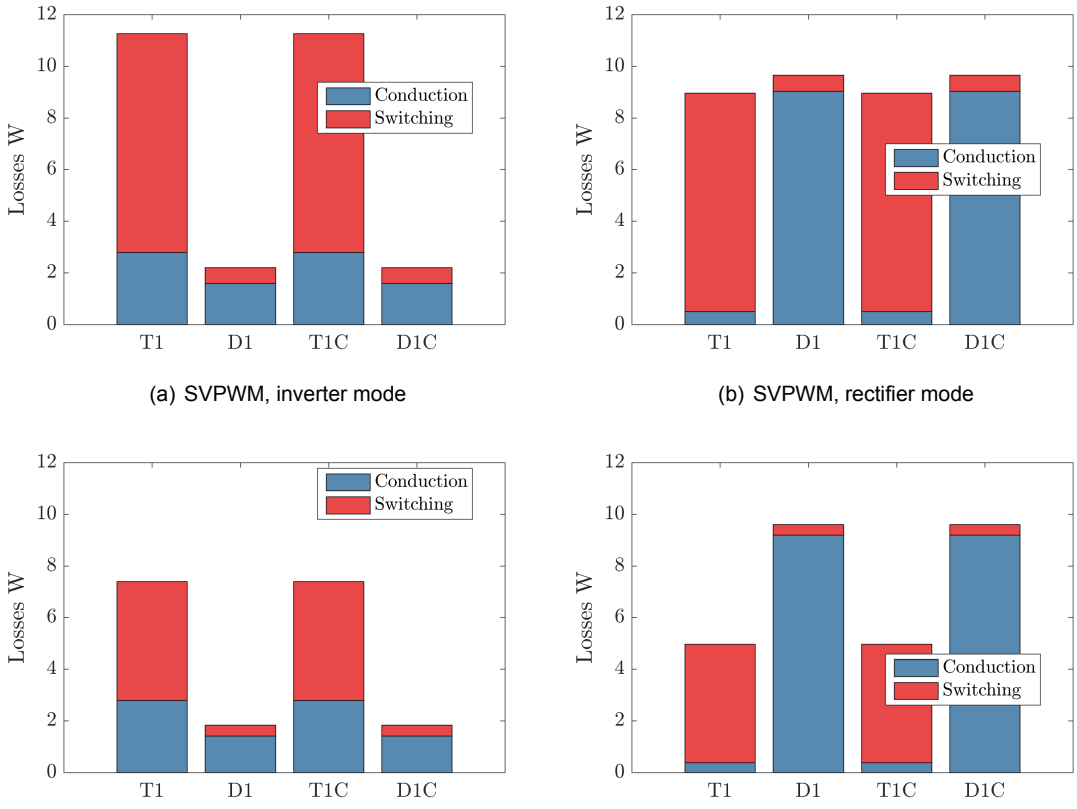
(c) NSPWM, inverter mode (d) NSPWM, rectifier mode

Figure 7.13: Switching losses of the 2LC, F_{sw} = 50 kHz

The value of the losses shown in the plots is as if the switch was conducting, not the RMS value. Due to the 60 degrees clamping conduction losses also change. When the output is clamped to one position only mosfets (inverter mode) or the diodes (rectifier mode) conduct during that certain time.

In Figure 7.13 the switching losses are shown. The value shown is a representation of the losses the switch would have if it was switching all the time with the same voltage and current values, the ones at that point of the cycle. This is helpful in order to compare the losses with other topologies and switching frequencies. The varying width of the losses is due to the difference between turn-on loss and turn-off losses. When NSPWM is applied the main difference is found in the switching losses, which are zero during the highest current points of the cycle, reducing the overall losses.

In Figures 7.14 the distribution of the losses is displayed. The bar plots show how whereas in inverter mode the conduction losses are mainly found in the power mosfets, in rectifier mode it is the diodes that conduct most of the current and therefore exhibit higher losses. The converter is thus more efficient when working in inverter mode than when it is in rectifier mode, because diodes have higher conduction losses.



(a) SVPWM, inverter mode

(b) SVPWM, rectifier mode

(c) NSPWM, inverter mode

(d) NSPWM, rectifier mode

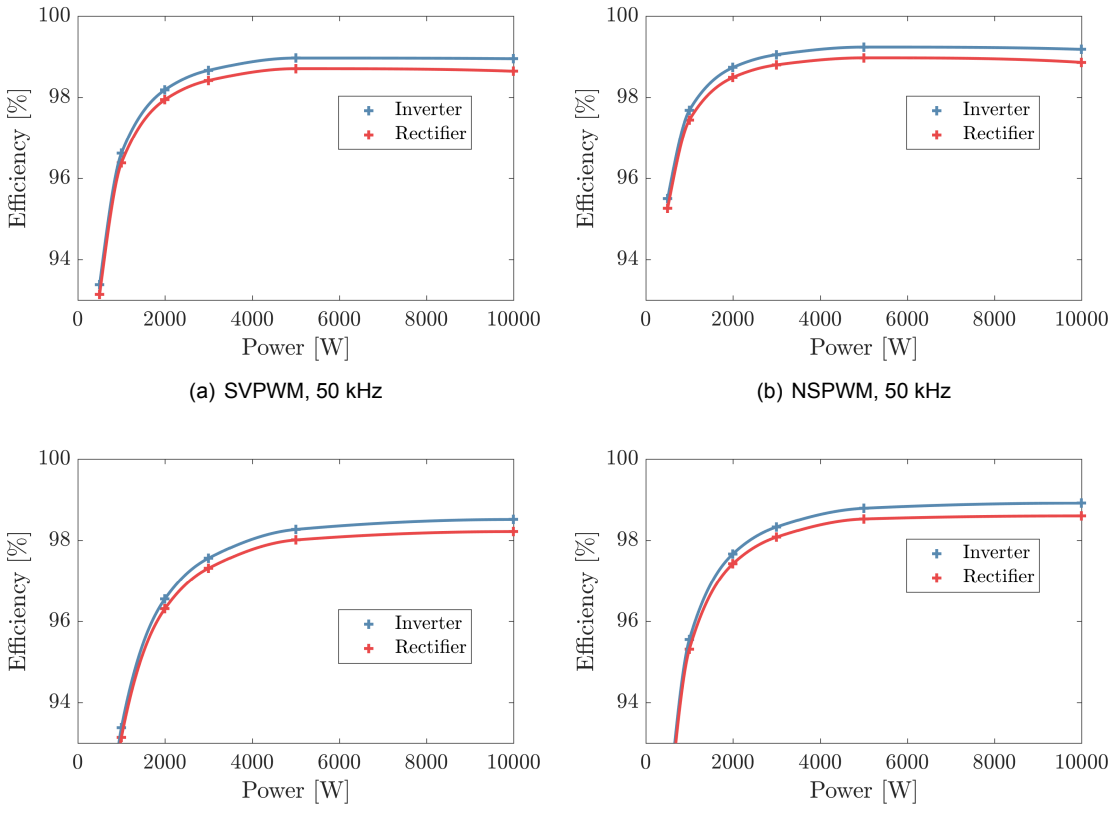
Figure 7.14: Losses of the 2LC, F_{sw} = 50 kHz

The filter design has been performed using the procedure found in Section 4.8. Table 7.3 lists the different values of the LCL filter for the different converter switching frequencies and modulation techniques:

Table 7.3: Design parameters of the 2LC LCL filter

F_{sw} [kHz]	50		100	
Modulation	SVPWM	NSPWM	SVPWM	NSPWM
Lfconv [mH]	0.476	0.805	0.236	0.446
Lfg [mH]	0.014	0.081	0.014	0.009
Cf [µF]	2.067	3.358	0.4176	0.852
Rf [Ω]	2.05	2.11	4.2344	3.12
fres [Hz]	12500	7500	30000	20000
Volume [dm^3]	0.162	0.360	0.117	0.162
Max loss [W]	23.06	25.89	11.24	21.39

As expected, the power losses in the filter are kept low, as the same maximum series resistance applies for all of them. The main difference is found in the maximum losses, which is different depending on the modulation technique used. Using NSPWM results in a bigger LCL filter with higher losses, while the configuration with a smaller and less lossy filter is the converter operating with SVPWM at 100 kHz. With this information it is possible to plot the efficiencies of the converter for both modes of operation and for both modulation techniques, see Figure 7.15.



(a) SVPWM, 50 kHz

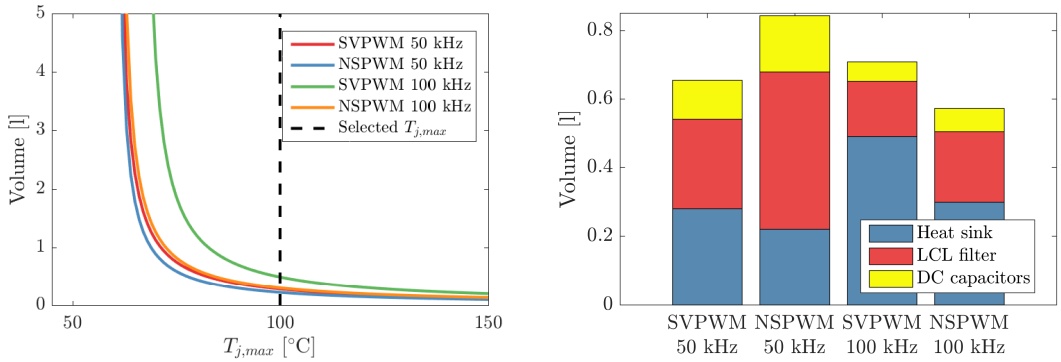
(b) NSPWM, 50 kHz

(c) SVPWM, 100 kHz

(d) NSPWM, 100 kHz

Figure 7.15: Efficiency of the 2LC at different operating points

Figure 7.15 shows how the efficiencies are similar for the four different options. However, NSPWM has the advantage of lower switching losses due to lower switchings, most of them at high current levels. The 100 kHz options have double the switching losses with respect to the 50 kHz version, resulting in lower efficiencies.



(a) Cooling system size ($T_{j,max}$)

(b) Size distribution

Figure 7.16: 2LC system size

When the losses are known, it is possible to obtain the necessary cooling system size of the converter to keep the maximum junction temperatures $T_{j,max}$ under a certain limit. The operating point with maximum losses is found when the converter acts as rectifier at full power. Figure 7.16(a) shows the necessary heat sink size for the different configurations when considering different maximum values of junction temperature. The total volume of the converter, formed by the cooling system, the LCL filter and the capacitors is found in Figure 7.16(b).F inally, a resume of the main converter parameters can be found in Table 7.4.

Table 7.4: Design values of the 2LC.

Freq. [kHz]	50		100	
Modulation	SVPWM	NSPWM	SVPWM	NSPWM
Mosfets	60 A*	60 A*	60 A*	60 A*
Diodes	25.5 A⋄	25.5 A⋄	25.5 A⋄	25.5 A⋄
Capacitance [µF]	25.67	35.73	12.46	18.22
Capacitors	2	5	1	2
Efficiency [D%]	98.42	98.81	97.35	98.12
Volume [dm^3]	0.655	0.843	0.709	0.573

* Cree C2M0025120D ⋄ Cree C4D20120A

7.1.3. Converter evaluation

The most interesting 2LC is the one working at 100 kHz and using NSPWM. Even though the switching losses are doubled, the 60°clamping this modulation technique performs at every switch reduces the switching losses while still making the LCL inductor smaller, achieving a higher final score. If SVPWM had to be selected, a switching frequency of 50 kHz would be preferred as it has a higher efficiency.

Table 7.5: Evaluation of the 2LC.

Freq. [kHz]	Weight	50		100	
Modulation	-	SVPWM	NSPWM	SVPWM	NSPWM
Num Switches	3	5	5	5	5
Num Diodes	1	5	5	5	5
Capacitors	1	5	2	5	5
Efficiency	5	3	4	1	3
Volume	5	3	2	3	4
Leakage currents	2	3	4	3	4
Eff. Improve	1	1	1	1	1
Controlability	3	4	3	4	3
TOTAL		**74**	**70**	**60**	**78**

7.2. Three Level Neutral Point Clamped Converter

The Three Level Neutral Point Clamped Converter (3LNPC²) [24] is the most used three level topology for converting DC to AC and vice versa. The structure of this converter is shown again in Figure 7.17 for the sake of completeness. It is composed of 12 switches with their respective flywheel diodes, which allow current in both directions independently of the clamped point of the bus. The middle point between every pair of switches is connected via a diode to the neutral point of the bus, making it possible to have three different clamped voltages to every output phase of the converter.

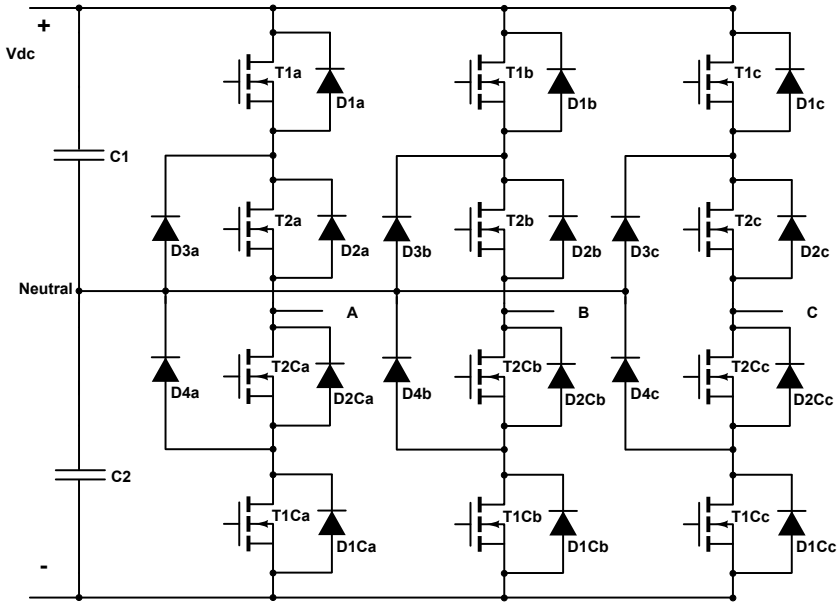


Figure 7.17: Structure of the 3LNPC²

Figure 7.17 does not show the required output filter, as the same filter topology is used for every inverter. It is designed and analyzed later on this section. The DC Link voltage is split by two equal capacitors, in order to create the middle point where the neutral line is connected. In this case, the

DC filter capacitors are also split. The different aspects which are reviewed in order to design and rate the converter are:

1. Modulation techniques review
2. Switch and diode requirements
3. Loss distribution
4. Cooling system size
5. Total Harmonic Distortion (THD)
6. Leakage currents
7. Efficiency improvement

7.2.1. Converter design

Modulation method

The modulation method of the inverter/rectifier is the most important part of the converter, as has been previously demonstrated in the 2LC section; it defines the switching behavior and thereby the total losses of the converter, which are mainly compromised of conduction losses and switching losses. In the case of three level converters the reference signal and carrier solutions adopted previously have to be modified in order to accommodate the three different positions each converter leg can adopt.

For three level converters, two carrier signals have to be used, $Carr_n^-$ ranging from -1 to 0 and $Carr_n^+$ ranging from 0 to 1. This two waveforms are shown later on Figure 7.19. The comparison of the reference signals with the carrier waveforms is performed in a similar manner as discussed in the previous section. However, when the reference signal happens to be between both the carrier signals, the phase is neutral clamped. This behavior is expressed in Equation 7.7, where P means the leg is connected to the positive of the bus, 0 to the neutral point and N to the negative of the bus.

$$\vec{S_n} = \begin{bmatrix} \begin{cases} S_{a,n} = P & Ref_{a,n} \geq Carr_n^+ \\ S_{a,n} = N & Ref_{a,n} \leq Carr_n^- \\ S_{a,n} = 0 & \text{otherwise} \end{cases} \\ \begin{cases} S_{b,n} = P & Ref_{b,n} \geq Carr_n^+ \\ S_{b,n} = N & Ref_{b,n} \leq Carr_n^- \\ S_{b,n} = 0 & \text{otherwise} \end{cases} \\ \begin{cases} S_{c,n} = P & Ref_{c,n} \geq Carr_n^+ \\ S_{c,n} = N & Ref_{c,n} \leq Carr_n^- \\ S_{c,n} = 0 & \text{otherwise} \end{cases} \end{bmatrix} \tag{7.7}$$

In order to have SVPWM like switching in three level converters, the reference signals need to be modified differently with respect to the two level converters. SVPWM is composed of a much larger number of vectors in three level converters, which have been represented in Figure 7.18. The zero vector, represented as V_0, can be accomplished by using three different switching vectors ([PPP], [000] and [NNN]). The small vectors, which range from V_{13} to V_{18}, have two different possibilities each.

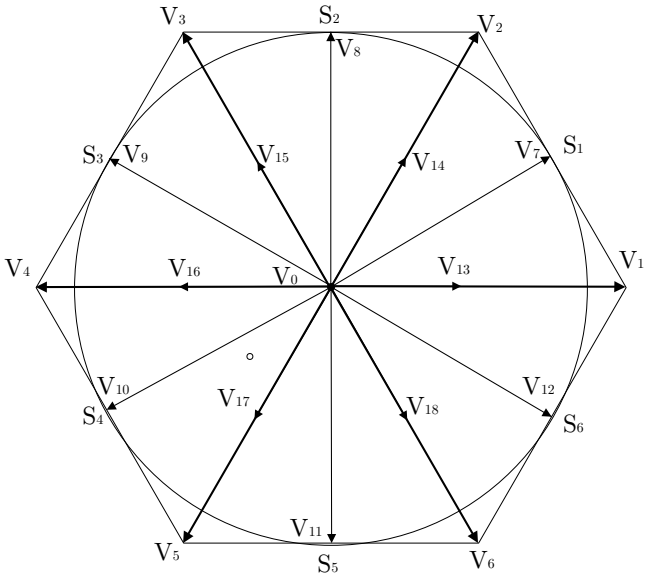


Figure 7.18: Working principle of the SVM.

Therefore, if the SVPWM already requires superior computational power for two level converters, in three level topologies the complexity is further increased. The necessary offset in order to have SVM like switching has to be calculated with a modification of the reference signals. In the case of having a negative reference signal, a unit value has to be added to the reference, in order to move the references which are found in $Carr_n^-$ to $Carr_n^+$. Therefore, the offset is [100]:

$$\begin{cases} V_a = V_a + 1 & if \quad V_a < 0 \\ V_b = V_b + 1 & if \quad V_b < 0 \\ V_c = V_c + 1 & if \quad V_c < 0 \end{cases} \tag{7.8}$$

$$Offset = 0.5 - \left[\frac{V_{max} + V_{min}}{2}\right]$$

Where V_{max} and V_{min} are the maximum and minimum voltages of the three modified reference voltages at that instant. This modification centers the active space vectors in the switching period, and hence matches carrier modulation to optimized SVM. Thereby, a modified sinusoidal waveform is obtained, see Figure 7.19.

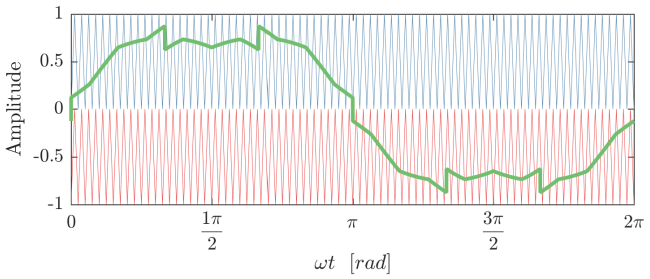


Figure 7.19: SVM like reference signal versus carrier signal

This modulation technique is the most suitable when using the inverter for off-grid solutions or where the leakage currents are not a big problem. Considering that the middle point connection to

the neutral of the line has some drawbacks, as explained previously in this report, it is also advisable to consider other modulation techniques which reduce the CMV and therefore current leakages. One of those methods is 2 Medium 1 Zero Vectors Pulse-Width Modulation (2M1ZVPWM) [101] for 3 level converters like the 3LNPC². Compared to SVPWM, this method only uses vectors which have the same CMV, resulting in no leakage current through the parasitic capacitance of the photovoltaic panels. The selected vectors are shown in Figure 7.20.

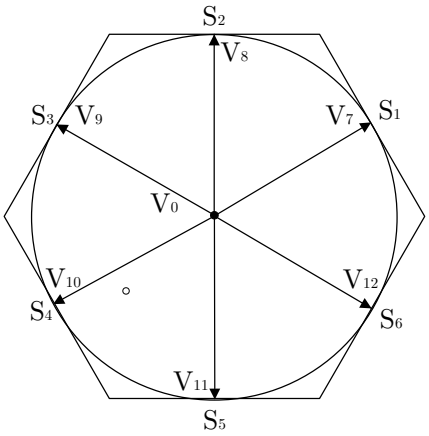


Figure 7.20: Sectors of the 2M1ZVPWM

In [102] a scalar method for the 2M1ZVPWM which is based on a reference and carrier comparative is stated. Depending on the reference signal obtained as if SVPWM for two level converters was used (see Equation 7.2), the switching state of all the switches that form the 3LNPC² are known. This method is simple and can be implemented in an FPGA too, in such a way that microprocessor load is reduced. For more information please refer to [102] where the scalar implementation of the method is explained.

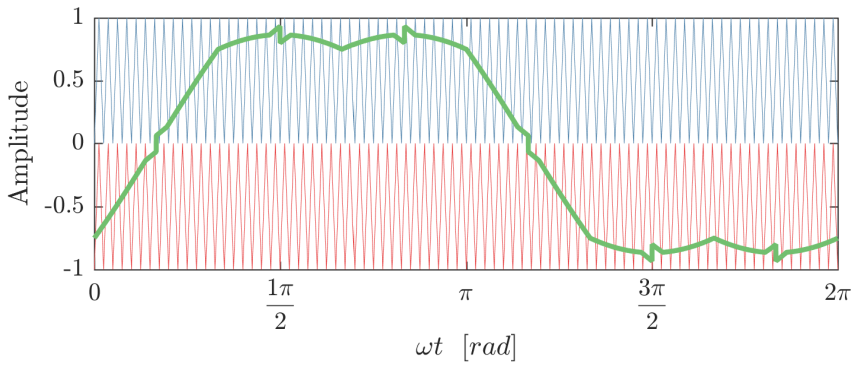


Figure 7.21: Reference waveforms and carrier signal of the 2M1ZVPWM

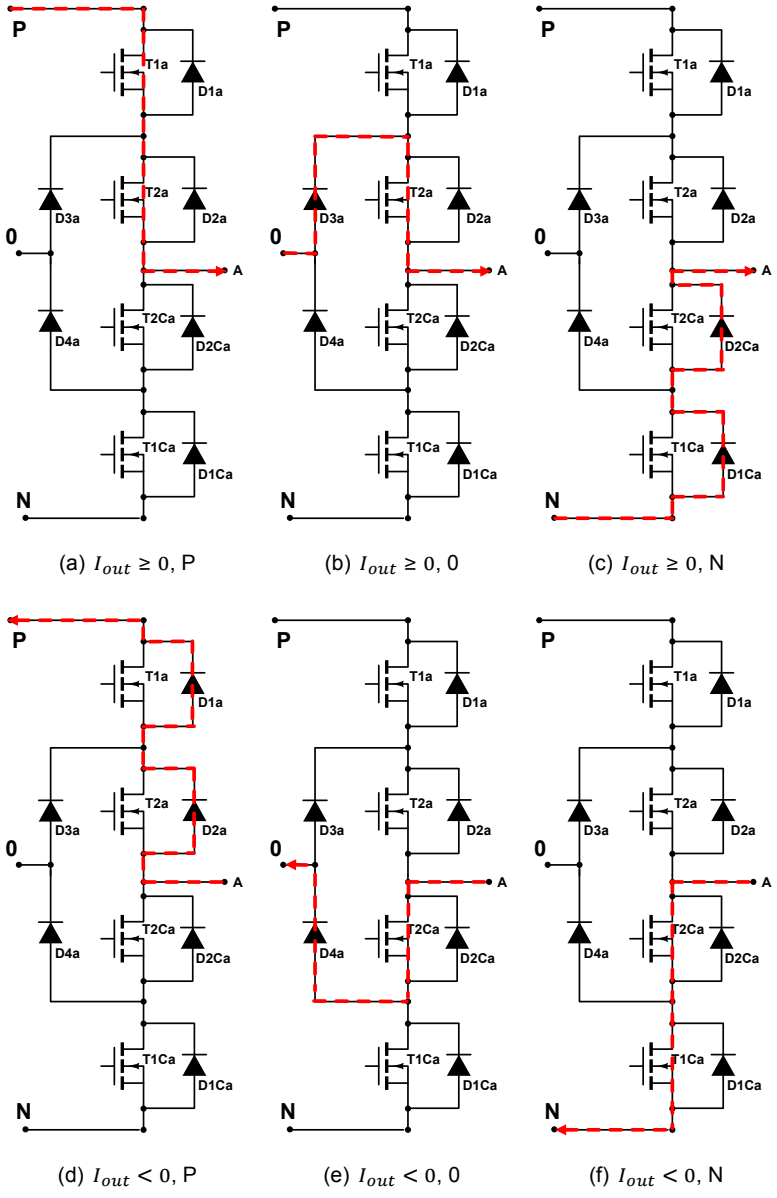
.

This modulation technique theoretically eliminates the leakage current due to the constant CMV at the output of the converter, which is fixed to $\frac{V_{PN}}{2}$. On the other hand, the cost of using such a modulation technique is high, as most of the possible voltage vectors that a three level converter has are not used, increasing the THD and the output voltage ripple.

After the analysis of modulation techniques performed in this section, it is possible to implement these techniques into a script in order to obtain the final rating of the converter for the different modes of operation. The voltage and current waveforms of the 3LNPC² can be found on Appendix E.2 as well as the gate signals and other relevant information.

Switch and diode requirements

The minimum breakdown voltage of both switches and diodes has to be half the DC link voltage. The current through the switches follows the same waveform as the output or input current of the converter, which is directly obtained from its maximum power capability. The conducting element depends both on the leg state and the output current direction, fact which is explained in the next section.



(a) $I_{out} \geq 0$, P (b) $I_{out} \geq 0$, 0 (c) $I_{out} \geq 0$, N

(d) $I_{out} < 0$, P (e) $I_{out} < 0$, 0 (f) $I_{out} < 0$, N

Figure 7.22: Switching states of the of the 3LNPC²

Loss distribution

The losses have been calculated using the method found in Section 3.3 from this thesis. In order to know which components conduct or switch in each transition, the three operation modes for each leg and the possible current directions are shown in Figure 7.22. Only one leg is considered in the analysis, as the symmetrical operation of the converter makes it possible to only perform the calculations for one and later assign the same values to the two other legs, which are displaced 120

degrees each.

From every figure it is possible to determine which elements are conducting and which switch for every possible transition, producing tables 7.6 and 7.7 respectively. The required equations that have to be implemented in the method are obtained from this table, in the form of the equations from Section 3.3, in order to obtain the conduction power losses and switching energy loss at every time step.

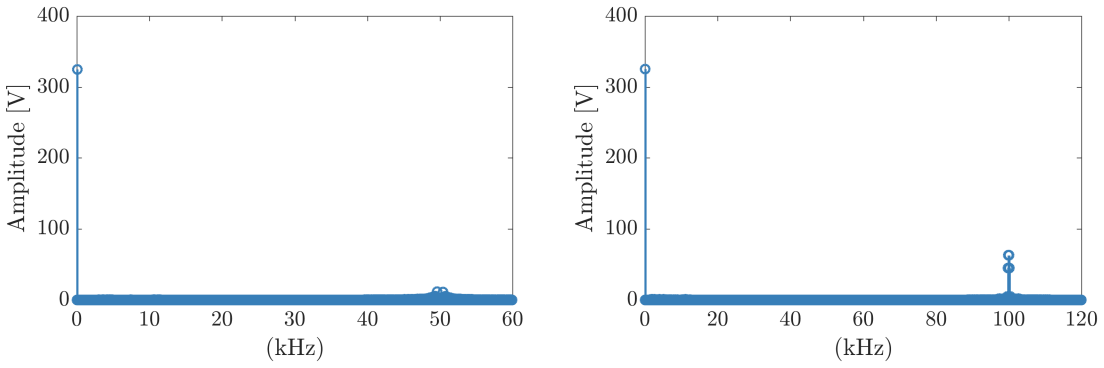
Table 7.6: Conduction losses of the 3LNPC².

Switching State	Conduction losses
$I_{out} \geq 0$	
P	$P_{cond,T1}$, $P_{cond,T2}$
0	$P_{cond,T2}$,$P_{cond,D3}$
N	$P_{cond,D1C}$,$P_{cond,D2C}$
$I_{out} < 0$	
P	$P_{cond,D1}$,$P_{cond,D2}$
0	$P_{cond,T2C}$,$P_{cond,D3C}$
N	$P_{cond,T1C}$,$P_{cond,T2C}$

Table 7.7: Switching losses of the 3LNPC².

Switching Transition	Loss energies
$I_{out} \geq 0$	
P → N	$E_{off,T1}$, $E_{off,T2}$
P → 0	$E_{off,T1}$
N → P	$E_{on,T1}$, $E_{on,T2}$, $E_{off,D1C}$,$E_{off,D2C}$
N → 0	$E_{on,T2}$,$E_{off,D1C}$
0 → P	$E_{on,T1}$,$E_{off,D3}$
0 → N	$E_{off,T2}$
$I_{out} < 0$	
P → N	$E_{on,T1C}$, $E_{on,T2C}$, $E_{off,D1}$,$E_{off,D2}$
P → 0	$E_{on,T2C}$,$E_{off,D1}$
N → P	$E_{off,T1C}$, $E_{off,T2C}$
N → 0	$E_{off,T1C}$
0 → P	$E_{off,T2C}$
0 → N	$E_{on,T1C}$,$E_{off,D3C}$

This information, together with the switch state in each switching period, makes it possible to calculate of the losses in every operating point of the converter, for inverter mode and rectifier mode.



(a) SVPWM (b) 2M1ZVPWM

Figure 7.23: FFT of the 3LNPC² for both modulation techniques. F_{sw} = 50 kHz

THD and output/input filter

The THD analysis has been performed using the Simulink FFT Analysis Tool from the SimpowerSystems Toolbox from the Matlab package. With this tool it is possible to analyze the voltage waveform and obtain the Fourier analysis magnitudes and frequencies. When it is applied to the phase voltages obtained for both modes of operation of the 3LNPC², the results can be plotted.

Figure 7.23 reveals how the harmonic content is much lower when using a three level converter instead of a two level one, compared to what has been previously seen on Figure 7.9. Moreover, the harmonic content around the switching frequency is much higher in the 2M1ZVPWM. The highest harmonic in the SVPWM is found in the $(m_f\text{-}2)^{th}$ harmonic in both cases.

DC side filter capacitor

The DC side capacitor must filter the ripple current in the DC link due to the switching behavior of the three phase inverter. The current ripple through the split capacitors depends on the output currents of the three phases and the voltage ripple applied to the output LCL filter of the converter. In the case of three level converters, it is necessary to calculate the currents through both the capacitors, in order to find the voltage ripple between the positive and negative of the bus. The capacitor currents $I_{cap,top}$ and $I_{cap,bot}$ can be given as [99]:

$$\begin{aligned} I_{cap,top} &= I_{inv,top} - I_{dc} \\ I_{cap,bot} &= I_{cap,top} + I_{inv,neu} \end{aligned} \tag{7.9}$$

Where $I_{inv,top}$ and $I_{inv,neu}$ are the current of the 3LNPC² in the positive and neutral connections and I_{dc} is the current of the source, which is constant in steady state operation of the converter. Assuming a loss-less system, the DC current is found via the power of the system and DC link voltage. The current through the 3LNPC² positive connection is derived from the switching states of the mosfets at the top, while the current flows to or from the neutral point when the leg state is 0, see Equation 7.10:

$$\begin{aligned} I_{inv,top,n} &= \begin{pmatrix} 1 & if & S_{a,n} = P \\ 1 & if & S_{b,n} = P \\ 1 & if & S_{c,n} = P \end{pmatrix} \begin{pmatrix} I_{a,n} & I_{b,n} & I_{c,n} \end{pmatrix} \\ I_{inv,neu,n} &= \begin{pmatrix} 1 & if & S_{a,n} = 0 \\ 1 & if & S_{b,n} = 0 \\ 1 & if & S_{c,n} = 0 \end{pmatrix} \begin{pmatrix} I_{a,n} & I_{b,n} & I_{c,n} \end{pmatrix} \end{aligned} \tag{7.10}$$

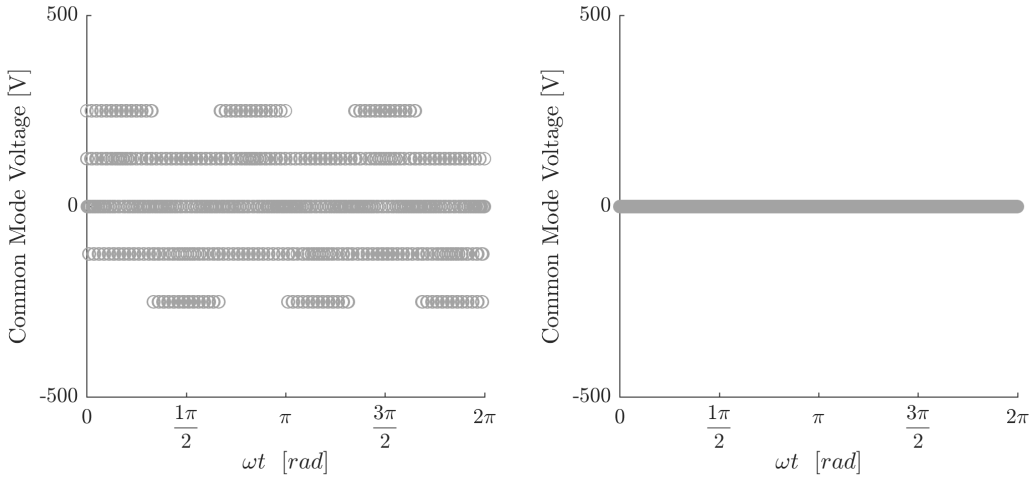
The output current, at the same time, depends on the voltage ripple of the converter and the filter. As the voltage output of the converter, the ripple current at the output can be derived and superimposed to the output current, see Equation 7.11. The sum of currents $I_{cap,top}$ and $I_{cap,bot}$ is used to calculate the necessary input capacitor capacitance in order to avoid voltage ripple at the DC bus.

$$I_x = I_{x,sin} + I_{x,rip} \tag{7.11}$$

Leakage current

Leakage current is considered to be lower in the case of 2M1ZVPWM due to its ability of reduction of the CMV. When using 2M1ZVPWM the CMV does not change, see Figure 7.24(b). Therefore, a

rate of 5 is given to the 3LNPC² operated with 2M1ZVPWM while a rate of 3 is given to the 3LNPC² operated with SVPWM.



(a) SVPWM (b) 2M1ZVPWM

Figure 7.24: Common Mode Voltage of the 3LNPC²

Efficiency Improvement

In the case of the 3LNPC², the same considerations as the ones explained for the 2LC on page 119 apply. There are not many options to increase the efficiency except for changing the modulation technique.

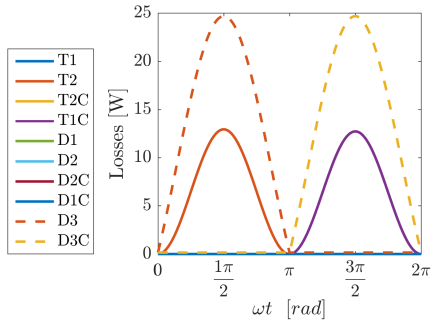
7.2.2. Results

The analysis of the converter has been done for both SVPWM and 2M1ZVPWM modulation techniques and a switching frequency of 50 kHz and 100 kHz. Due to the high amount of plots necessary to show all behaviors only 50 kHz switching frequency plots are shown in this section. When using 100 kHz as switching frequency the main changes are in switching losses, which doubles, and filter size, which is reduced.

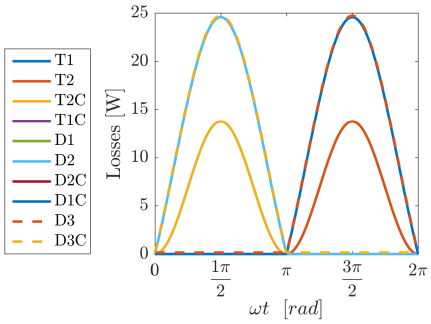
Conduction losses are shown in Figure 7.25 for both modulation techniques and inverter and rectifier modes of operation, in a similar manner as performed in Section 7.1.2 for the 2LC. Please notice that different devices conduct depending on the mode of operation and the modulation technique.

In Figure 7.26 the switching losses are shown. The value shown is a representation of the losses the switch would have if it was switching all the time with the same voltage and current values, the ones at that point of the cycle. This is helpful in order to compare the losses with other topologies and switching frequencies. The varying width of the losses is due to the difference between turning on loss and turn off loss. Due to the three level topology, switching losses are halved in every switch, reducing the total switching losses.

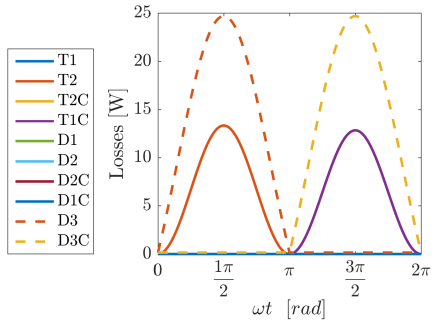
In Figures 7.27 the distribution of the losses is displayed. The bar plots bars show how whereas in inverter mode the conduction losses are mainly found in the power mosfets, in rectifier mode it is the diodes that conduct most of the current and therefore exhibit higher losses. The converter is thus more efficient when working in inverter mode than when it is in rectifier mode, because diodes have higher conduction losses. It is also important to notice that some of the semiconductors are not used depending on the mode of operation. For example, diodes D1, D1C, D2 and D2C are not used in inverter mode for the selected grid voltage.



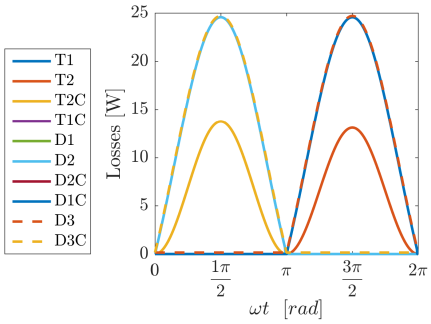
(a) SVPWM, inverter mode



(b) SVPWM, rectifier mode

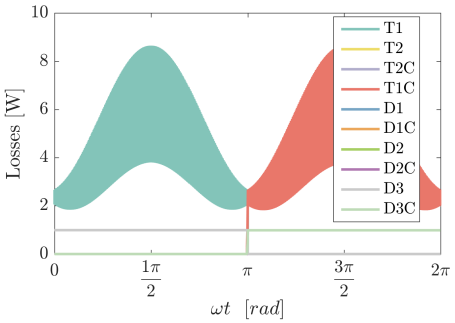


(c) 2M1ZVPWM, inverter mode

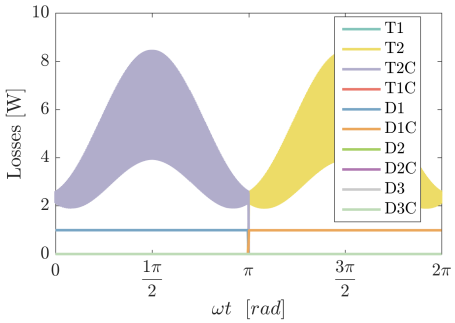


(d) 2M1ZVPWM, rectifier mode

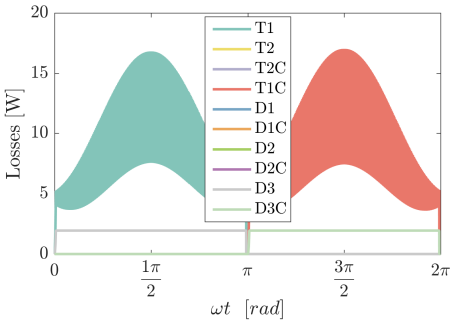
Figure 7.25: Conduction losses of the 3LNPC², F_{sw} = 50 kHz



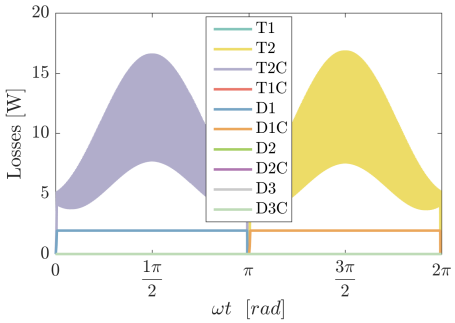
(a) SVPWM, inverter mode



(b) SVPWM, rectifier mode

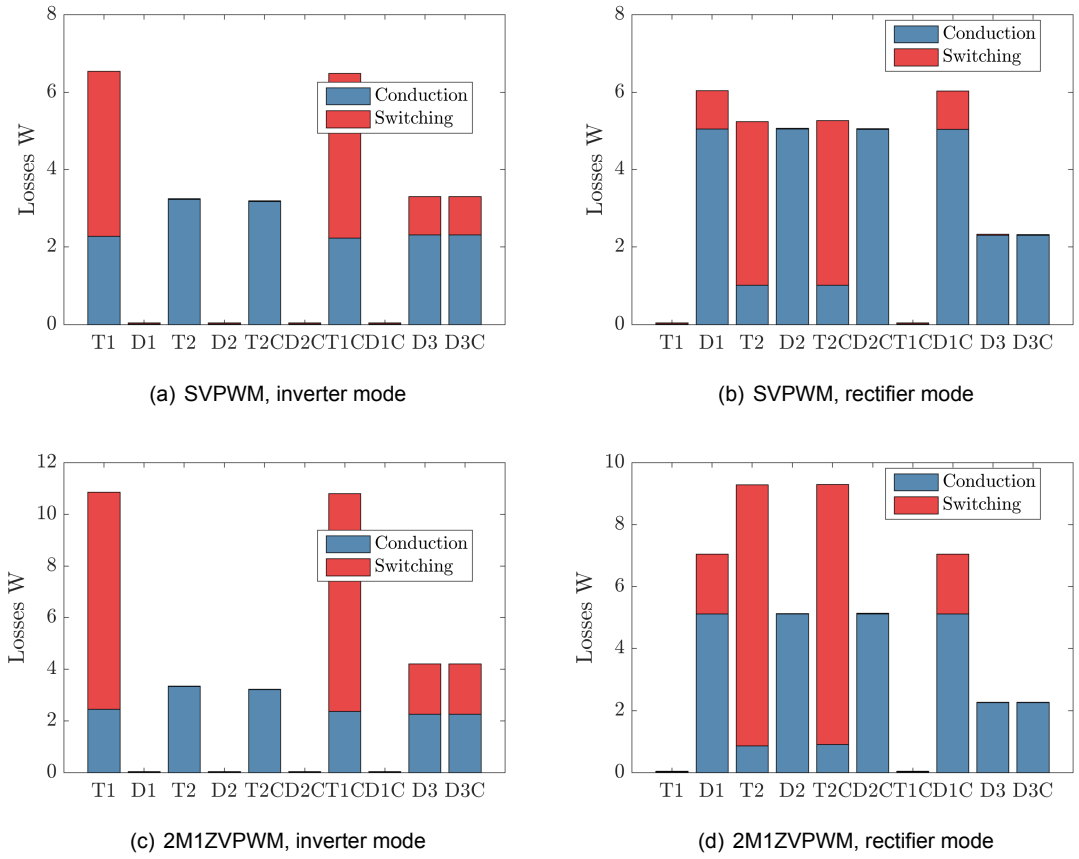


(c) 2M1ZVPWM, inverter mode



(d) 2M1ZVPWM, rectifier mode

Figure 7.26: Switching losses of the 3LNPC², F_{sw} = 50 kHz



(a) SVPWM, inverter mode

(b) SVPWM, rectifier mode

(c) 2M1ZVPWM, inverter mode

(d) 2M1ZVPWM, rectifier mode

Figure 7.27: Losses of the 3LNPC², F_{sw} = 50 kHz

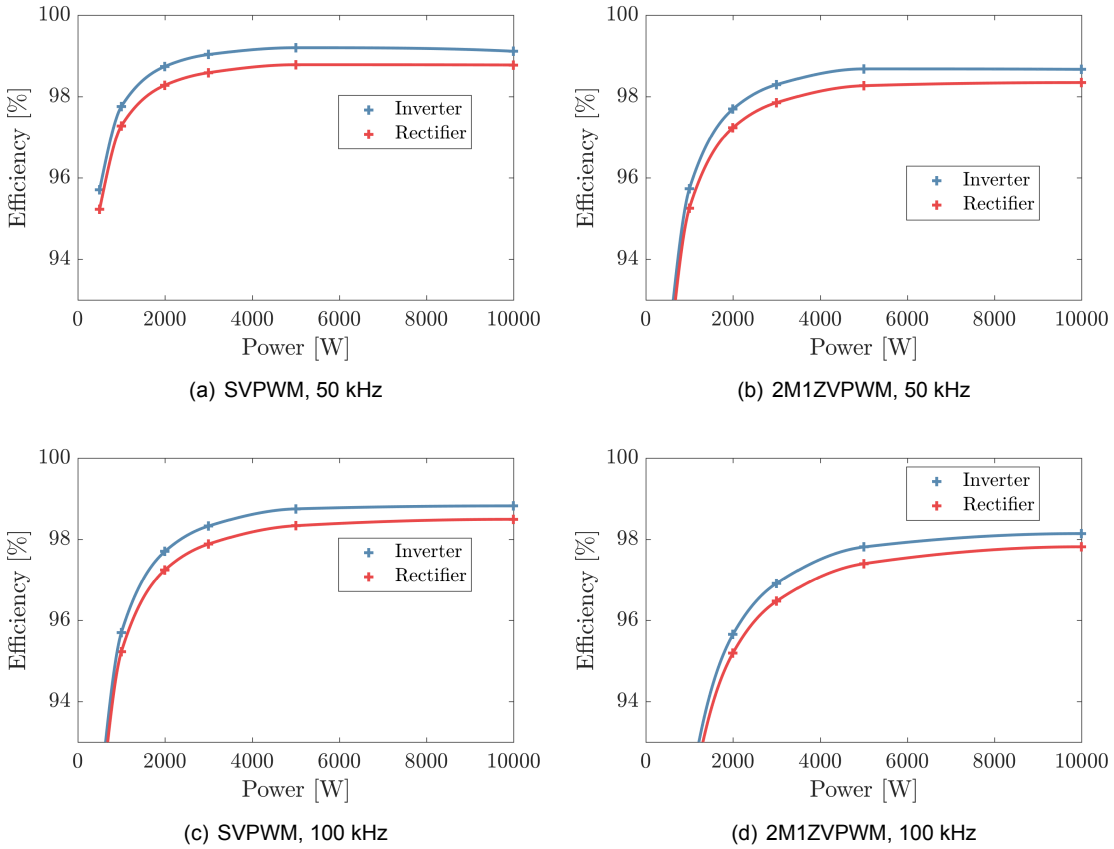
The filter design has been performed using the procedure explained in Section 4.8. Table 7.8 lists the different values of the LCL filter for the different switching frequencies and modulation techniques.

Table 7.8: Design parameters of the 3LNPC² LCL filter

F_{sw} [kHz]	50		100	
Modulation	SVPWM	MVPWM	SVPWM	MVPWM
Lfconv [mH]	0.214	0.449	0.135	0.236
Lfg [mH]	0.006	0.010	0.001	0.015
Cf [µF]	1.034	2.167	0.120	0.496
Rf [Ω]	2.566	1.959	5.314	3.891
fres [Hz]	20000	12500	50000	27500
Volume [dm^3]	0.098	0.142	0.117	0.117
Max loss [W]	9.81	21.98	6.34	11.42

As expected, the power losses in the filter are kept low, as the same maximum series resistance applies for all of them. The main difference is found in the maximum losses, which depend on the modulation technique used. Using 2M1ZVPWM results in a bigger LCL filter with higher losses, while the configuration with the smaller losses and volume is the 3LNPC² with SVPWM at 100 kHz. Finally

it is possible to plot the efficiencies for both modes of operation and both modulation techniques, see 7.28.



(a) SVPWM, 50 kHz

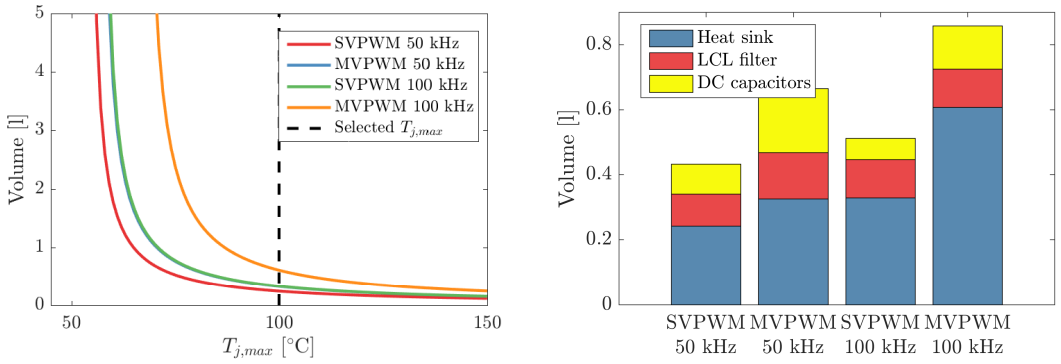
(b) 2M1ZVPWM, 50 kHz

(c) SVPWM, 100 kHz

(d) 2M1ZVPWM, 100 kHz

Figure 7.28: Efficiency of the 3LNPC² at different operating points.

When the losses are known, it is possible to obtain the necessary cooling system size of the converter to keep the maximum junction temperatures $T_{j,max}$ under a certain limit. In the case of the 3LNPC², operation in rectifier mode at full power yields the maximum losses. Figure 7.29(a) shows the necessary heat sink size for the studied configurations when considering different maximum values of junction temperature. The figure makes it clear that due to the distribution of the losses in a higher number of components the necessary size is quite low.



(a) Cooling system size ($T_{j,max}$)

(b) Size distribution

Figure 7.29: 3LNPC² system size

The losses when 2M1ZVPWM is used are higher than when SVPWM is used, resulting in a bigger cooling system needed. Figure 7.29(b) shows the volumes of the different configurations. The main converter parameters are found in Table 7.9.

Table 7.9: Design values of the 3LNPC².

Freq. [kHz]	50		100	
Modulation	SVPWM	2M1ZVPWM	SVPWM	2M1ZVPWM
Mosfets	60 A*	60 A*	60 A*	60 A*
Diodes	50 A 650V ⋄	50 A 650V ⋄	50 A 650V ⋄	50 A 650V ⋄
C_{in} [µF]	36.39	59.43	18.36	23.15
Capacitors (split)	8	4	2	2
Efficiency	98.73	97.97	98.04	96.64
Volume [dm^3]	0.43245	0.66524	0.51176	0.8583

* Cree C2M0025120D ⋄ Cree C5D50065D

Following the design considerations, the chosen SiC mosfets are 1200 V rated. Considering this topology needs half the DC bus rating, this is oversized. However, those switches are the ones that yield lower losses, mainly due to their series drain-source on resistance of 0.025 Ω. On the other hand, the selected diodes do have half the rated voltage compared to the ones selected for the 2LC.

7.2.3. Converter evaluation

The most interesting 3LNPC² is the one working at 50 kHz with SVPWM. The 2M1ZVPWM modulation technique increases the both the losses and volume, making it less suitable than the previously used NSPWM for the 2LC. As expected, this three level topology in the common SVPWM performs better than the 2LC with the same modulation technique.

Table 7.10: Evaluation of the 3LNPC².

Freq. [kHz]	Weight	50		100	
Modulation	-	SVPWM	2M1ZVPWM	SVPWM	2M1ZVPWM
Num Switches	3	3	3	3	3
Num Diodes	1	1	1	1	1
Capacitors	1	1	3	5	5
Efficiency	5	4	2	3	1
Volume	5	5	3	4	2
Leakage currents	2	3	5	3	5
Eff. Improve	1	1	1	1	1
Controlability	3	4	3	4	3
TOTAL		**75**	**58**	**69**	**50**

7.3. Three Level T-Type Converter

The Three Level T-Type Converter (3LT²C) [25] is an alternative three level topology for converting DC to AC and vice versa. The structure of this converter is shown again in Figure 7.30 for the sake of completeness. It is composed of 12 switches with their respective flywheel diodes, which allow current in both directions independently of the clamped point of the bus. The output of the converter can be clamped to the neutral point of the DC bus via two switches that allow bidirectionality.

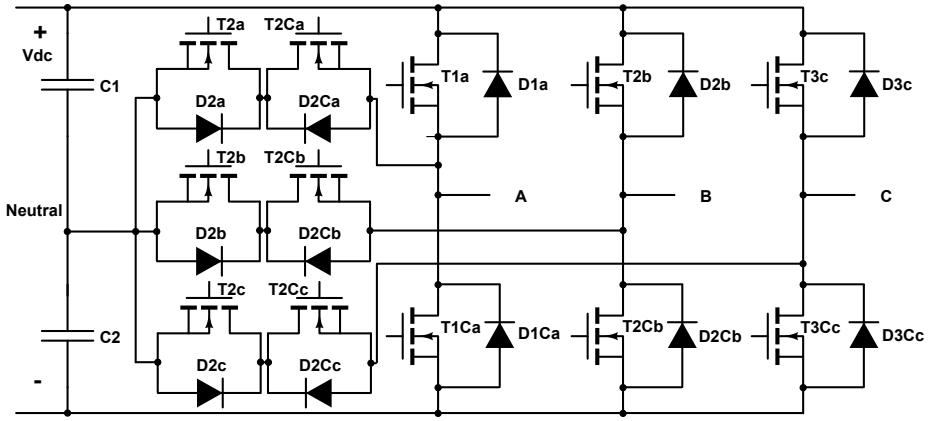


Figure 7.30: Structure of the 3LT²C

Again, the LCL filter is not shown in Figure 7.30. This converter is really similar to the conventional 3LNPC²; therefore, it is not going to be explained in the same detail, as most of the aspects are shared. First of all, the same modulation techniques apply; both SVPWM and 2M1ZVPWM will be used for the analysis of this topology. The semiconductor requirements are different to the 3LNPC², and therefore the losses distribution. Both the LCL output filter and the DC filter capacitors are the same as the 3LNPC², because the output currents and voltages are equal. The heat sink size is computed again because of the different losses distribution of this topology. Leakage currents are given the same rating as the CMV variation is the same for both topologies.

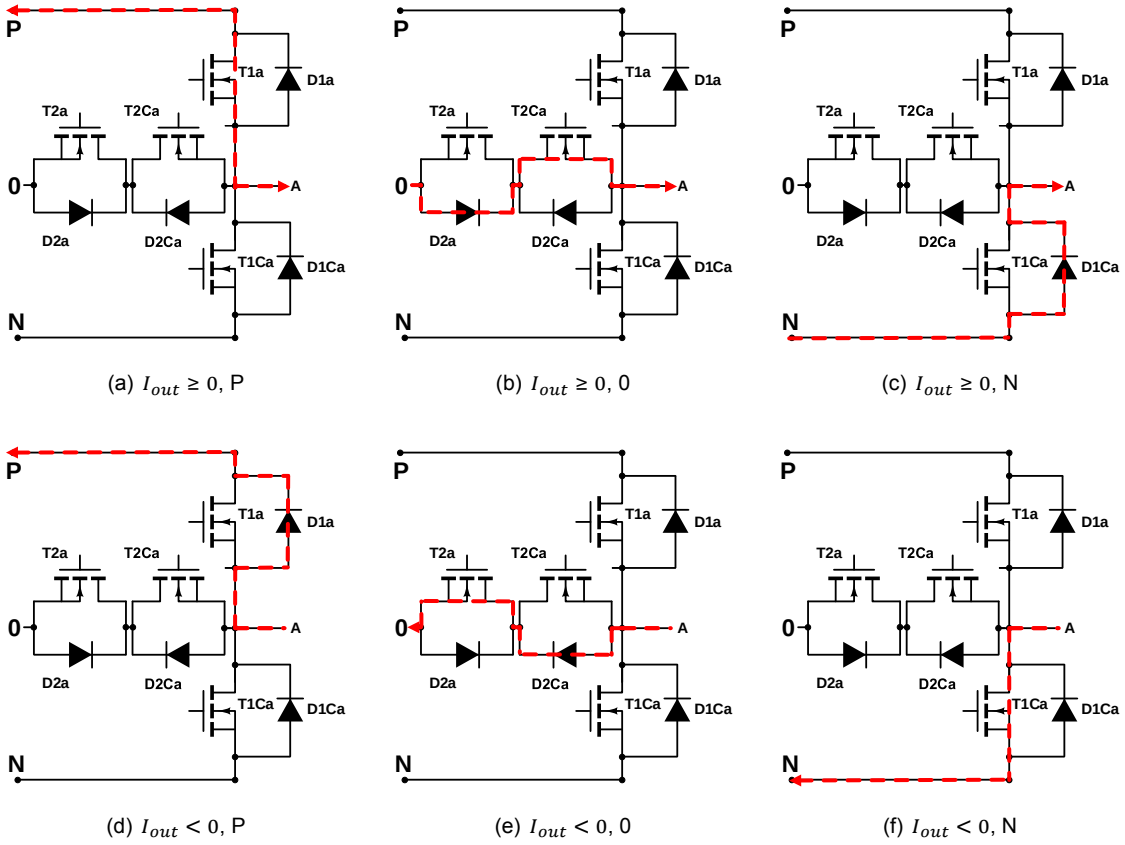
7.3.1. Converter design

Switch and diode requirements

The maximum voltage across the switches and diodes connected to the positive and negative buses of the DC link is the full DC link voltage. On the other hand, the switches and diodes that are connected to the neutral point of the DC bus need to have half the voltage rating. The current through all the switches and diodes follows the same waveform as the output or input current of the converter, which is directly obtained from the maximum power capability of the converter. The conducting element depends both on the leg state and the output current direction, fact which is explained in the next section.

Loss distribution

The losses have been calculated using the method found in Section 3.3. In order to know which components conduct or switch in each transition, the three operation modes for each leg and the possible current directions are shown in Figure 7.31. Only one leg is considered in the analysis, as the symmetrical operation of the converter makes it possible to only perform the calculations for one and later assign the same values to the two other legs, which are displaced 120 degrees each.



(a) $I_{out} \geq 0$, P (b) $I_{out} \geq 0$, 0 (c) $I_{out} \geq 0$, N

(d) $I_{out} < 0$, P (e) $I_{out} < 0$, 0 (f) $I_{out} < 0$, N

Figure 7.31: Switching states of the of the 3LT²C

From every figure it is possible to determine which elements are conducting and which switch for every possible transition, producing tables 7.11 and 7.12 respectively. The required equations that have to be implemented in the method are obtained from this table, in the form of the equations from Section 3.3, in order to obtain the conduction power losses and switching energy loss at every time step.

Table 7.11: Conduction losses of the 3LT²C

Switching State	Conduction losses
$I_{out} \geq 0$	
P	$P_{cond,T1}$
0	$P_{cond,T2}$,$P_{cond,D2C}$
N	$P_{cond,D1C}$
$I_{out} < 0$	
P	$P_{cond,D1}$
0	$P_{cond,T2C}$,$P_{cond,D2}$
N	$P_{cond,T1C}$

Table 7.12: Switching losses of the 3LT²C

Switching Transition	Loss energies
$I_{out} \geq 0$	
P → 0	$E_{off,T1}$
0 → P	$E_{on,T1}$,$E_{off,D2C}$
N → 0	$E_{on,T2}$,$E_{off,D1C}$
0 → N	$E_{off,T2}$
$I_{out} < 0$	
P → 0	$E_{on,T2C}$,$E_{off,D1}$
0 → P	$E_{off,T2C}$
N → 0	$E_{off,T1C}$
0 → N	$E_{on,T1C}$,$E_{off,D2}$

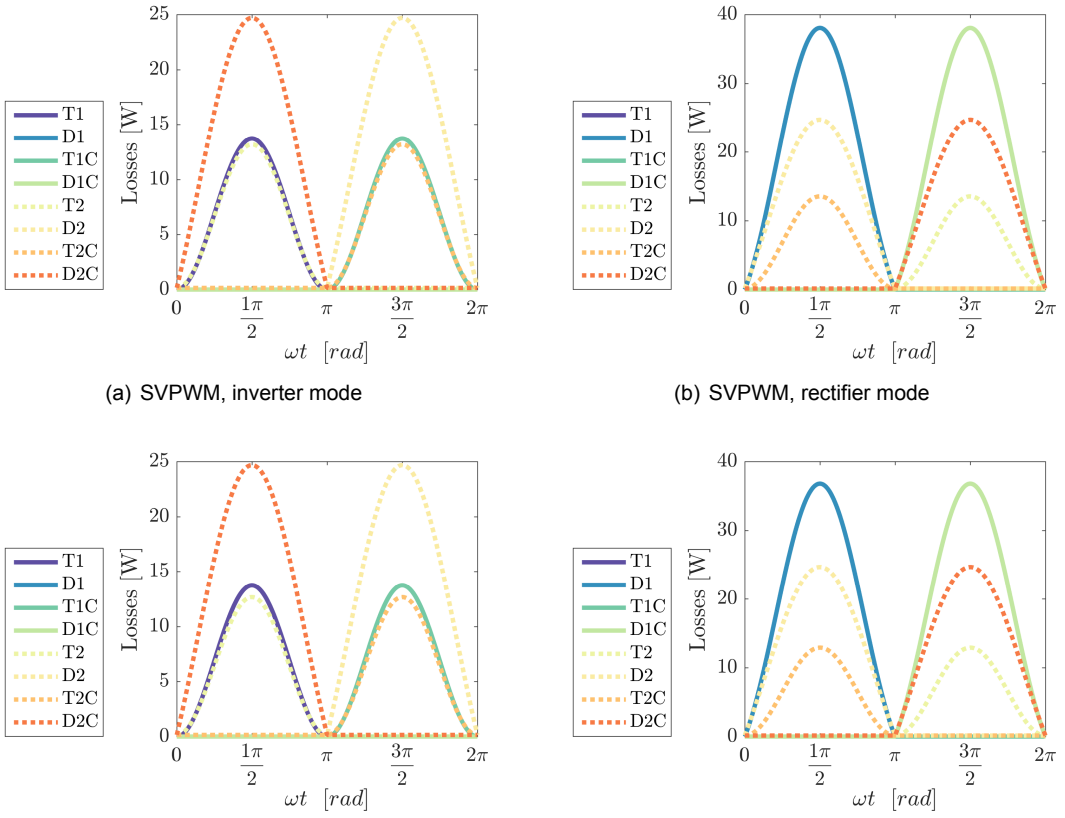
Efficiency Improvement

In the case of the 3LT²C, the same considerations as the ones explained for the 2LC on page 119 apply. There are not many options to increase the efficiency except for changing the modulation technique.

7.3.2. Results

The analysis of the converter has been done for both SVPWM and 2M1ZVPWM modulation techniques and a switching frequencies of 50 kHz and 100 kHz. Due to the high amount of plots necessary to show all behaviors only 50 kHz switching frequency plots will be shown in this section.

Conduction losses are shown in Figure7.32 for both modulation techniques and inverter and rectifier modes of operation, in a similar manner as performed in Section 7.1.2 for the 2LC. Please notice that different devices conduct depending on the mode of operation and the modulation technique.



(a) SVPWM, inverter mode

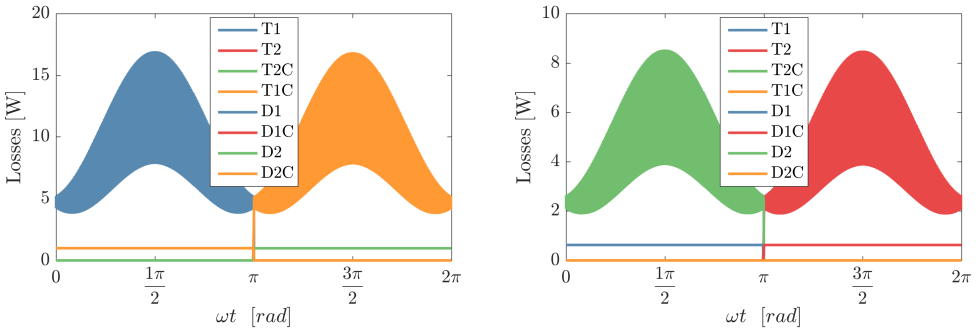
(b) SVPWM, rectifier mode

(c) 2M1ZVPWM, inverter mode

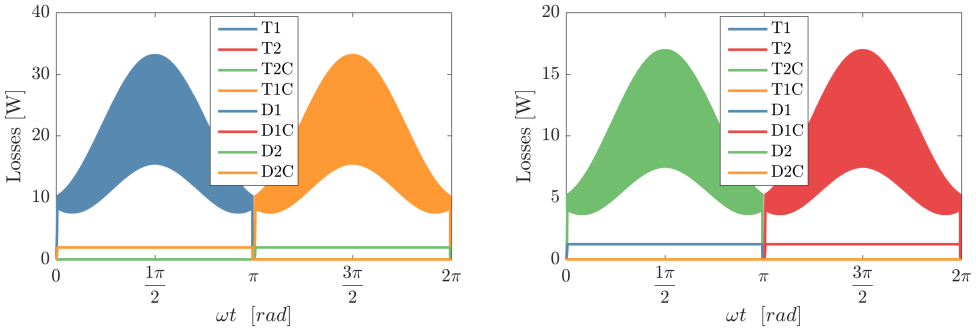
(d) 2M1ZVPWM, rectifier mode

Figure 7.32: Conduction losses of the 3LT²C, F_{sw} = 50 kHz

In Figure 7.33 the switching losses are shown. The value shown is a representation of the losses the switch would have if it was switching all the time with the same voltage and current values, the ones at that point of the cycle. This is helpful in order to compare the losses with other topologies and switching frequencies.

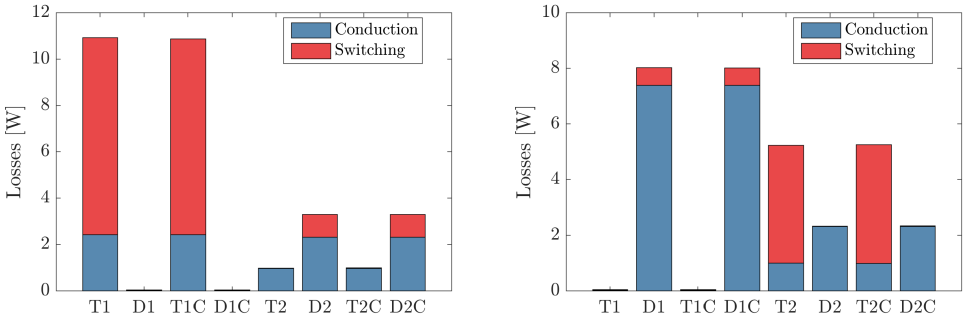


(a) SVPWM, inverter mode (b) SVPWM, rectifier mode

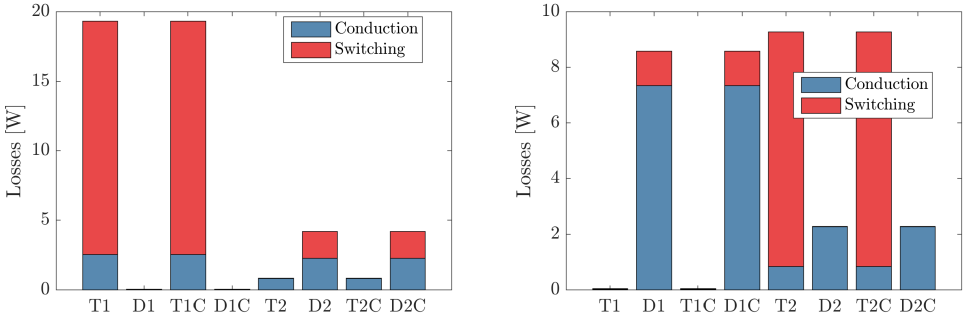


(c) 2M1ZVPWM, inverter mode (d) 2M1ZVPWM, rectifier mode

Figure 7.33: Switching losses of the 3LT²C, F_{sw} = 50 kHz



(a) SVPWM, inverter mode (b) SVPWM, rectifier mode

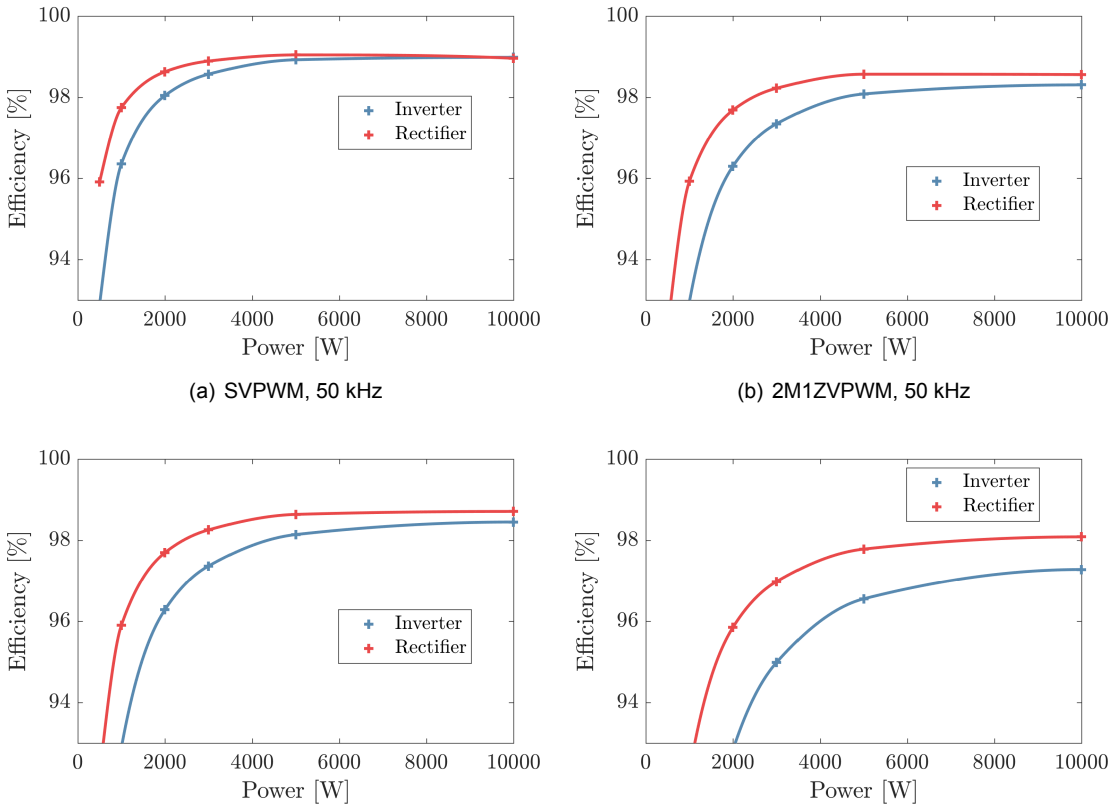


(c) 2M1ZVPWM, inverter mode (d) 2M1ZVPWM, rectifier mode

Figure 7.34: Losses of the 3LT²C, F_{sw} = 50 kHz

In Figure 7.34 the distribution of the losses is displayed. The bar plots show how whereas in inverter mode the conduction losses are mainly found in the power mosfets, in rectifier mode it is the diodes that conduct most of the current and therefore exhibit higher losses, in the same way as the other two considered topologies.

With this information it is possible to plot the efficiencies of the converter for both modes of operation and for both modulation techniques, see Figure 7.35.



(a) SVPWM, 50 kHz

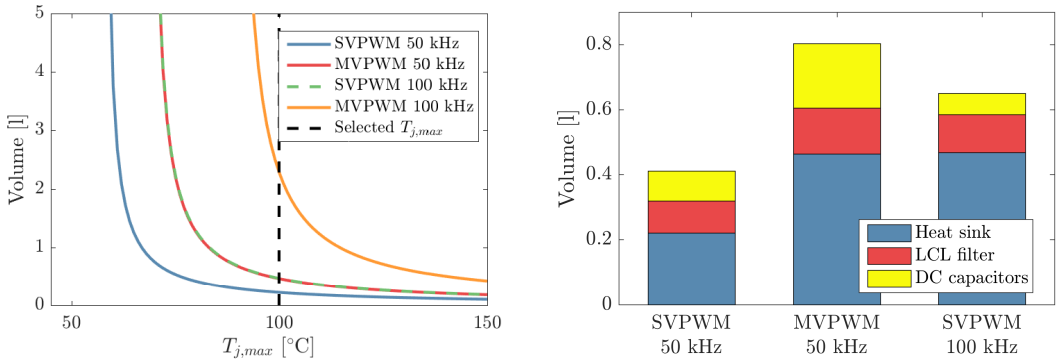
(b) 2M1ZVPWM, 50 kHz

(c) SVPWM, 100 kHz

(d) 2M1ZVPWM, 100 kHz

Figure 7.35: Efficiency of the 3LT²C at different operating points.

The cooling system size of the converter plot is shown in Figure 7.36(a).



(a) Cooling system size ($T_{j,max}$)

(b) Size distribution

Figure 7.36: 3LT²C system size

As previously stated, the filters used for the different considered converters are the same as for the 3LNPC², see Table 7.8 in the previous section of this chapter. The main difference with respect to the 3LNPC² in terms of size is due to the cooling system, as shown on Figure 7.36(b). The main converter parameters are found in Table 7.13, where the T semiconductors make reference to those connected to the middle point of the split DC link.

Table 7.13: Design values of the 3LT²C.

Freq. [kHz]	50		100	
Modulation	SVPWM	2M1ZVPWM	SVPWM	2M1ZVPWM
Mosfets	60 A*	60 A*	60 A*	60 A*
Mosfets T	60 A*	60 A*	60 A*	60 A*
Diodes	25.5 A⋆	25.5 A⋆	25.5 A⋆	25.5 A⋆
Diodes T	50 A⋄	50 A⋄	50 A⋄	50 A⋄
C_{in} [µF]	36.39	59.43	18.36	22.15
Capacitors (split)	8	4	2	2
Efficiency	98.63	97.65	97.72	95.86
Volume [dm^3]	0.411	0.803	0.651	2.536

* Cree C2M0025120D ⋄ Cree C5D50065D

⋆ Cree C4D20120A

Again, all the mosfets are rated 1200 V because they yield lower losses. The diodes connected to the positive and negative of the bus are rated 1200V, while the diodes which are connected to the neutral point are 650 V breakdown voltage diodes, because of the lower forward voltage.

7.3.3. Converter evaluation

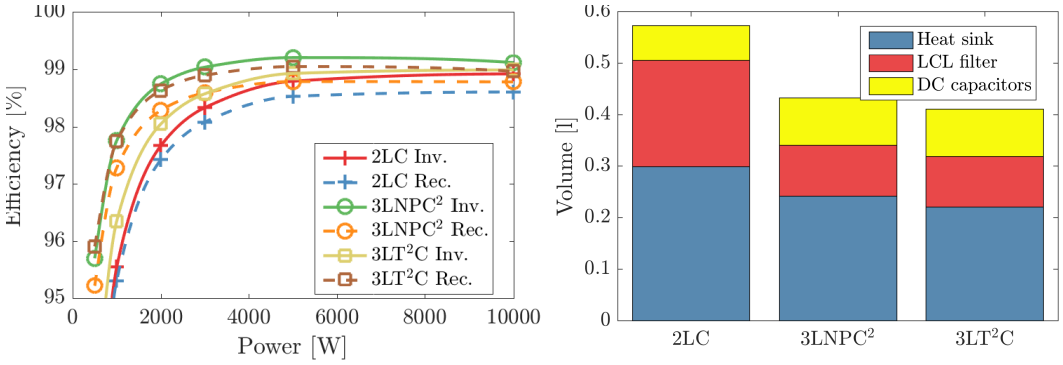
In this three level converter, the use of 2M1ZVPWM yields higher losses than in the 3LNPC². As a result, the converter operating with this modulation technique at 100 kHz has very high losses, resulting in a large cooling system needed. This configuration is already discarded in Table 7.14, where the grading of the different configurations is done. It is shown how in the case of using 2M1ZVPWM the final score is lower, but when using the standard SVPWM technique it performs a little bit better than the 3LNPC².

7.4. Conclusion

In this chapter three DC-AC converters have been analyzed for the Grid port: the Two Level Converter (2LC), the Three Level Neutral Point Clamped Converter (3LNPC²) and the Three Level T-Type Converter (3LT²C), see Figure 7.37. The converter that scores higher is the 2LC with Near State Pulse-Width Modulation (NSPWM) because of the lower component count and special modulation method which reduces the leakage currents and also the switching losses.

Table 7.14: Evaluation of the 3LT²C.

Freq. [kHz]	Weight	50		100
Modulation	-	SVPWM	2M1ZVPWM	SVPWM
Num Switches	3	3	3	3
Num Diodes	1	3	3	3
Capacitors	1	1	3	5
Efficiency	5	4	2	2
Volume	5	5	2	3
Leakage currents	4	3	5	3
Eff. Improve	1	1	1	1
Controlability	3	4	4	4
TOTAL		**77**	**58**	**61**



(a) Efficiency (b) Volume

Figure 7.37: Results of the optimal topologies configurations of the PV port.

8

Impedance Network Based Converters Analysis - Quasi Z-Source Two Level Converter

The quasi Z-Source Inverter (qZSI) is an interesting topology for converting DC to AC with buck and boost possibilities. In this chapter only this topology is analyzed as it is the most interesting Impedance Network based topology for the design of the multiport converter. The structure of this converter is shown again in Figure 8.1 for the sake of completeness. It is composed of six switches with their respective flywheel diodes, which allow current in both directions independently of the clamped point of the bus. Attached to the DC voltage source, the PV panels, an impedance network consisting of two inductors and two capacitors is introduced, which endows the converter the required boost capabilities.

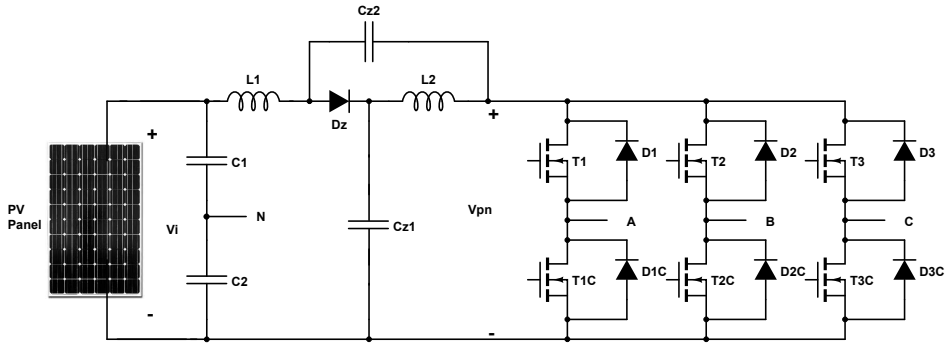


Figure 8.1: Topology of the qZSI

Figure 8.1 does not show the required output filter, as the same LCL filter will be used for this topology. There is no inverter DC filter sizing as the topology does not require one. This topology uses a split capacitor in the input filter capacitor of the PV panels. This ensures the reduction of the leakage currents of the converter. The steps followed in order to design and rate the converter are:

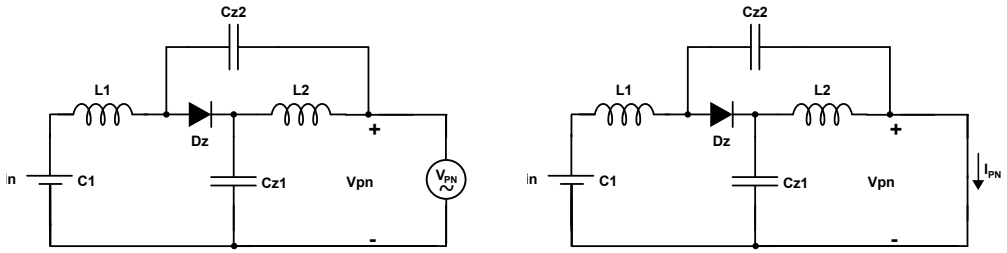
1. Operation principle review
2. Modulation techniques
3. Switch and diode requirements

4. Loss distribution
5. Total Harmonic Distortion (THD)
6. Leakage current
7. Efficiency improvement

8.1. Converter design

Operation principle

The converter operation can be divided in two main states, the Active state (A) and the Shoot Through state (ST). In the Active state, which takes place during T_1, the converter works as the already known Two Level Converter (2LC), where either the P or N bus is clamped, see Figure 8.2(a). The six switches keep following the reference vector in order to modulate the output of the converter.



(a) Active state (b) Shoot through state

Figure 8.2: Possible states of the of the qZSI

The Shoot Through state (ST) takes places during time T_0 and is shown in Figure 8.2(b). In this state both the upper and lower switches of the triple bridge are gated, in such a way that the output of the converter is 'short circuited'. Considering the presence of the impedance network, it boosts the input voltage to the desired one at the input of the inverter. The Shoot through state can be realized by gating all or only two of the legs of the triple bridge, the last option resulting in higher conduction and lower switching losses. Both options are discussed later in this section.

The steady state analysis equations for the qZSI can be found in [27]. However, only the most relevant equations for understanding the operation of the converter are listed in this report. All the equations regarding the currents and voltages of the different elements of the impedance network are derived in Reference [27]. The most important information that has to be extracted is the fact that the diode currents are as high as two times the input current of the converter, which means that one diode would have to conduct approximately 60 A in the worst case scenario. For this reason, more than one parallel diode in the impedance network has been considered. The inductor currents are also very high, as they are equal to the input current from the PV side. For this matter, several configurations of parallel and series inductors are considered. Lastly, it is important to know that the voltages across the capacitors C_{z1} and C_{z2} are fixed and might be used as a DC link to connect a third converter, used for EV charging.

The converter can operate in two modes, buck and boost. When the DC input voltage from the photovoltaic panels is higher than $\sqrt{2}\sqrt{3}V_{grid}$ there is no need for boosting the input, therefore the boosting factor B of the converter is unity. At this voltage, the modulation index M is one. At higher input voltages the boost factor is kept to one while the modulation index is decreased, just as the conventional 2LC for different DC link voltages. On the other hand, when the voltage is lower, both factors must be known. The boost factor increases in order to enhance the voltage at the impedance network, while the modulation index is decreased in order to make it possible to insert the Shoot Through states in the converter. The peak AC voltage at the output of the converter is:

$$\hat{V_p} = \frac{V_{in}}{2} BM = \frac{V_{in}}{2} G \tag{8.1}$$

Where G is the gain of the converter. With Equation 8.1 one can conclude that when G is one or lower than one, $B = 1$ and $M <= 1$. The Shoot Through states are not present in this mode ($T_0 = 0$,$D = 0$) and the modulation index M is found as:

$$M = \frac{2\hat{V_p}}{V_{in}} \tag{8.2}$$

At this point, as the boost is zero, the input voltage of the PV panels is reflected at the connections of the inverter, in such a way that $V_{PN} = V_{in}$. On the other hand, when $G > 1$ both the boost factor and modulation index are related. First of all, from Equation 8.1, the gain factor must be found:

$$G = \frac{2\hat{V_p}}{V_{in}} \tag{8.3}$$

According to [27], the boost factor and modulation index can be computed as:

$$\begin{aligned} M &= \frac{G}{\sqrt{3}G - 1} \\ B &= \frac{1}{\sqrt{3}M - 1} \end{aligned} \tag{8.4}$$

Finally, both the duty cycle of the Shoot through states and the voltage across the inverter can be derived, and all the important information regarding the steady state of the qZSI is known:

$$\begin{aligned} D &= 1 - \frac{\sqrt{3}M}{2} \\ V_{PN} &= BV_{in} \end{aligned} \tag{8.5}$$

The ST current I_{PN} is twice the input current at the DC port of the converter, which can be derived from the input power and input voltage. Lastly, the required inductances are found using Equation 8.6.

$$L_1 = L_2 = \frac{2M_{max}V_{in,min}}{\Delta I_{in,pp} T_{0,max}} \tag{8.6}$$

Where $T_{0,max}$ is found as:

$$T_{0,max} = \frac{2 - \sqrt{3}M_{min}}{2f_{sw}} \tag{8.7}$$

Modulation method

The modulation method used is a modified Space Vector Pulse-Width Modulation (SVPWM), which has already been explained in the 2LC section. The Shoot Through states are introduced into the switching cycle when the carrier is greater than V_P or less than V_N, voltages that are complementary. This voltage values are obtained directly from the duty cycle, $V_P = 1 - D$, as unity values are used for the implementation of the modulation techniques. As this Shoot Through states (ST) are evenly spread during the whole switching cycle, there is no low frequency ripple present in the converter [27]. Therefore, a total of five reference waveforms must be considered in order to obtain the switching pattern of the converter, see Figure 8.3.

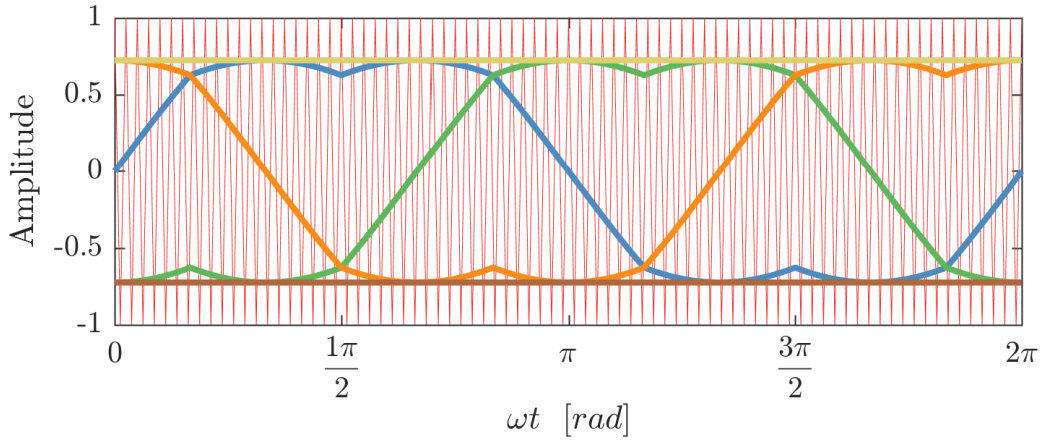


Figure 8.3: Reference waveforms versus triangular wave in qZSI ($V_{in} = 350V$)

In Figure 8.3 the three main reference waveforms are shown, together with the two additional ones, which are used to compute the switching state of the leg. As in the conventional 2LC, when the reference signal is greater than the triangular waveform, the leg is in the P state, with the output connected to the positive bus. When the sinusoidal signal is lower than the carrier waveform, the output is clamped to the negative bus of the qZSI. On top of that, when the reference signal is higher than V_P or lower than V_N the Shoot Through state (ST) is activated, meaning that both switches of the leg are active. This comparison has to be performed for every sample period n, see Equation 8.8.

$$\vec{S_n} = \begin{bmatrix} \begin{cases} S_{a,n} = ST & V_{P,n} < Carr_n \quad OR \quad V_{N,n} > Carr_n \\ S_{a,n} = P & Ref_{a,n} \geq Carr_n \quad AND \quad V_{P,n} > Carr_n \\ S_{a,n} = N & otherwise \end{cases} \\ \begin{cases} S_{b,n} = ST & V_{P,n} < Carr_n \quad OR \quad V_{N,n} > Carr_n \\ S_{b,n} = P & Ref_{b,n} \geq Carr_n \quad AND \quad V_{P,n} > Carr_n \\ S_{b,n} = N & otherwise \end{cases} \\ \begin{cases} S_{c,n} = ST & V_{P,n} < Carr_n \quad OR \quad V_{N,n} > Carr_n \\ S_{c,n} = P & Ref_{c,n} \geq Carr_n \quad AND \quad V_{P,n} > Carr_n \\ S_{c,n} = N & otherwise \end{cases} \end{bmatrix} \tag{8.8}$$

Switch and diode requirements

The breakdown voltage of every switch and anti parallel freewheling diode has to be at least the maximum V_{PN} voltage, which occurs at maximum boost. Considering that the minimum considered input voltage for the PV panels is 350 V, the maximum voltage can be derived by using Equations 8.3 8.4 and 8.5. This voltage goes up to 777 V, a little bit higher than the previously selected DC link voltage for the different multi port converter configurations.

The current through the semiconductors follows the same waveform as the output or input current of the converter, which is directly obtained from the maximum power capability of the converter. However, due to the Shoot through states present in this topology, the I_{PN} current has to be taken into account, which is two times the input current of the converter. This makes the overall necessary current rating of the different switches increase. On the other hand, the diodes can keep the same current rating as the traditional 2LC because they do not conduct during the Shoot Through states. The maximum current is derived in the next section as it depends of the chosen Shoot through mode.

Shoot Through state currents

The currents in Shoot Through mode can be derived by using Kirchoff's law and the equivalent circuit of the three legs in this state. In [103] a very detailed analysis of the currents in this states is performed. When three legs ST is used, the gate signals are high for all the switches in the converter in the ST state. The I_{PN} current is shared between the three legs, which also conduct the output current of the converter:

$$\begin{aligned} i_{Tx} &= \frac{I_{PN}}{3} + \frac{i_x}{2} \\ i_{TxC} &= \frac{I_{PN}}{3} - \frac{i_x}{2} \end{aligned} \tag{8.9}$$

Where i_{Tx} and i_{TxC} are the currents of the upper and lower currents for the phases $x = a, b, c$, and i_x is the instantaneous current through the phase. However, this currents have to be positive; otherwise the switches do not conduct and only two legs are in real ST state while in the third one only one switch conducts. The condition for the all the currents to be positive is therefore:

$$\frac{I_{PN}}{3} > |\frac{i_x}{2}| \tag{8.10}$$

In the case this condition is not fulfilled for one phase, that phase only conducts the output current as in the freewheeling mode of the 2LC and the I_{PN} current is divided between the other two phases. For example, if Equation 8.10 is false for phase B and i_b is negative, the currents are computed as follows:

$$\begin{array}{ccc} i_{T1} = \frac{I_{PN}}{2} + \frac{2i_a+i_c}{4} & i_{T2} = 0 & i_{T3} = \frac{I_{PN}}{2} + \frac{2i_c+i_a}{4} \\ i_{T1C} = \frac{I_{PN}}{2} - \frac{2i_a+i_c}{4} & i_{T2C} = -i_b & i_{T3C} = \frac{I_{PN}}{2} - \frac{2i_c+i_a}{4} \end{array} \tag{8.11}$$

On the other hand, two legs Shoot Through could be used, by choosing the ST state legs. This introduces complexity in the system, as the best technique for 2 legs ST is to let the leg of the phase with the lowest current to freewheel [103]. Moreover, in the power range of the multiport converter in research, this solution is not advisable. If the maximum I_{PN}, which is two times the maximum input current of the converter, is shared between two legs, the maximum current is greatly increased, as the converter output current must be taken into account too. In this case Equation 8.11 has to be used in order to obtain the currents in the two legs mode.

Loss distribution

The losses have been calculated using the method in Section 3.3 from this thesis. The Active states in the qZSI are the same as in the 2LC, which have already been shown in Figure 7.8. On top of those 6 possibilities in the Active states, there are the Shoot Through states, where both SiC mosfets conduct and the short circuit current I_{PN} current flows through the triple bridge of the converter.

Therefore, three different states are possible in each leg, named as P when the upper switch is active, N when the lower switch is active and ST when both switches are active. The different states are analyzed for the conduction losses in Table 8.1 and the possible transitions where switchings occur are listed in Table 8.2. The ST currents $I_{a,T1,ST}$ and $I_{a,T1C,ST}$ are derived as in detailed previously.

Table 8.1: Conduction losses of the qZSI

Switching State	Conduction losses
$I_{out} \geq 0$	
P	$P_{cond,T1}$
N	$P_{cond,D1C}$
$I_{out} < 0$	
P	$P_{cond,D1}$
N	$P_{cond,T1C}$
ST	$P_{cond,T1}(I_{a,T1,ST})$, $P_{cond,T1C}(I_{a,T1C,ST})$

Table 8.2: Switching losses of the qZSI

Switching Transition	Loss energies
$I_{out} \geq 0$	
P → N	$E_{off,T1}$
N → P	$E_{on,T1}$, $E_{off,D1C}$
P → ST	$E_{on,T1C}(I_{a,T1C,ST})$
N → ST	$E_{on,T1}(I_{a,T1,ST})$, $E_{off,D1C}$
ST → P	$E_{off,T1C}(I_{a,T1,ST})$
ST → N	$E_{off,T1}(I_{a,T1,ST})$
$I_{out} < 0$	
P → N	$E_{off,T1C}$, $E_{off,D1}$
N → P	$E_{on,T1C}$
P → ST	$E_{on,T1C}(I_{a,T1C,ST})$, $E_{off,D1}$
N → ST	$E_{on,T1}(I_{a,T1,ST})$
ST → P	$E_{off,T1C}(I_{a,T1,ST})$
ST → N	$E_{off,T1}(I_{a,T1,ST})$

This information, together with the switch state in each switching period, makes it possible to calculate the losses in every operating point of the converter, both for inverter mode of operation and rectifier mode.

THD and output/input filter

The THD analysis has been performed using the Simulink FFT Analysis Tool from the SimpowerSystems Toolbox from the Matlab package. With this tool it is possible to analyze the voltage waveform and obtain the Fourier analysis magnitudes and frequencies of the waveform. When it is applied to the phase voltages obtained for the qZSI, the results can be plotted, see Figure 8.4. It is shown that the THD is a little bit higher than the more simple 2LC due to a lower modulation index being used. The 100 kHz version is not shown as the design is not possible, fact that will be treated in the next sections.

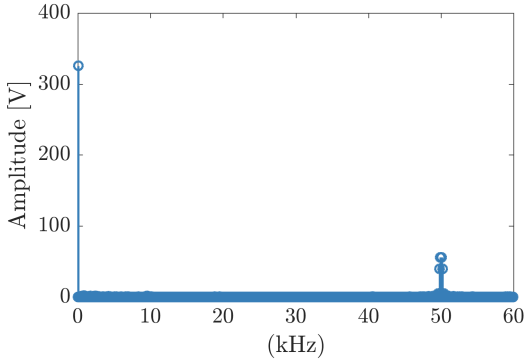


Figure 8.4: FFT of the qZSI at 50 kHz.

Leakage current

A rate of 3 is given to the qZSI operated with the modified SVPWM, as no special arrangements besides the connection of the middle point of the split capacitor at the input to the neutral of the line have been considered. In terms of leakage currents, the qZSI has the same characteristics as the 2LC using SVPWM.

Efficiency Improvement

The converter has very little possibilities of increasing the efficiency. Other boosting methods are possible, like the maximum boost control for Z source inverters [104], at the cost of introducing low frequency ripple in the DC capacitors of the converter. As a consequence, a rating of 1 is given to the topology.

8.2. Results

The main drawbacks of this topology are the currents in both the inductors and diodes, which are very high. This makes the diode conduction losses too high and the design of inductors that use E65 cores for such a current is not possible. Therefore, several diode and inductor configurations have been tested in order to make the design possible. The installation of series and parallel inductors has been considered in order to make the design possible. Parallel have been considered too, as the positive temperature coefficient of such devices make paralleling possible.

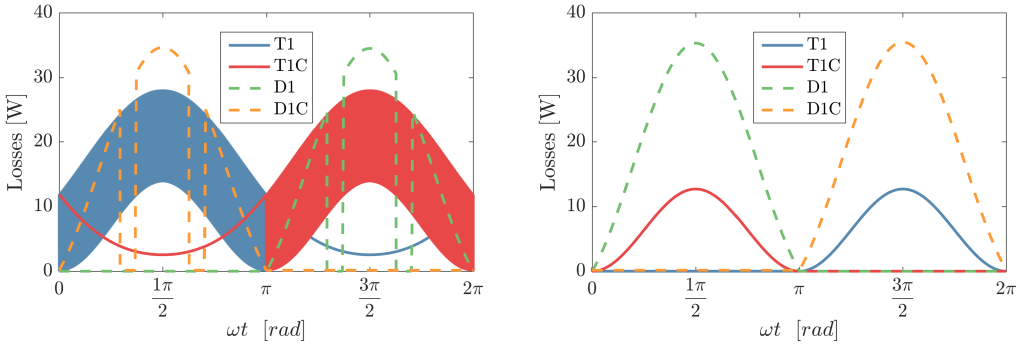
The analysis of the converter has been done for both 3 legs ST and a switching frequency of 50 kHz. Using two legs ST or 100 kHz as switching frequency yield very high losses and requires a large cooling system as shown later in Figure 8.9(a). The impedance network is composed of a total of sixteen E65 inductors because of the high currents, with each main inductor consisting of four series inductors in two parallel rows. Moreover, three diodes have to be installed in parallel in order to reduce and spread the losses. The specifications of the Z impedance network and the 3 leg bridge are listed in Table 8.3.

Table 8.3: Design parameters of the qZSI LCL filter, 3 legs ST F_{sw} = 50 kHz

Mosfets	Diodes	Capacitors	Inductors
6 x 60 A*	9x25.5 A	11	16 x E65

* Cree C2M0025120D

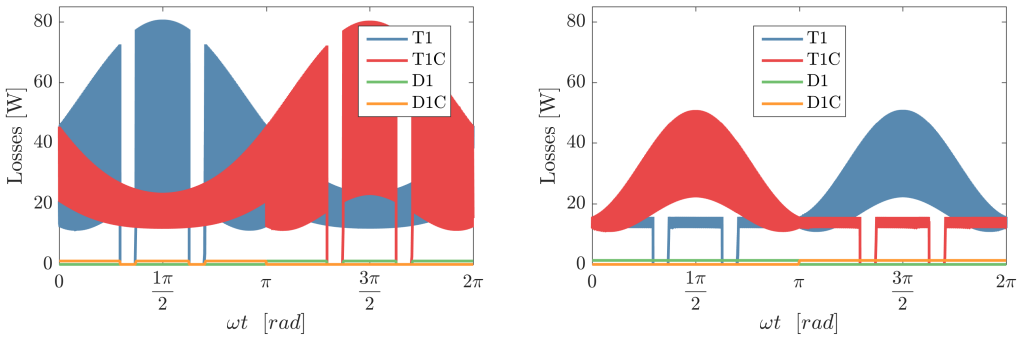
Conduction losses for the three leg bridge are shown in Figure 8.5. The worst case scenario is chosen for the plots, meaning that that PV voltage is fixed at the minimum acceptable 350 V and the input power is maximum. In Figure 8.5(a), the losses in inverter mode are shown. The time during witch the diodes do not conduct in Figure 8.5(a) are due to the clamping of the complementary switch; the reference signal is equal to the ST signals and therefore only two states take place, clamping one switch of the leg. The conduction losses of the qZSI have two different current amplitudes, because of the difference in the currents between the Active state and the ST state. This is the reason for the thickness of the plot. In the interval $0 - \pi$, switch T1C only conducts when in ST state, therefore the losses are lower. The same phenomena takes place in T1 during $\pi - 2\pi$ because of the inherent symmetrical behavior. In rectifier mode, as the currents of the PV panels are considered to be zero, the diode conduction losses are equal to the 2LC.



(a) 3 legs ST, inverter mode (b) 3 legs ST, rectifier mode

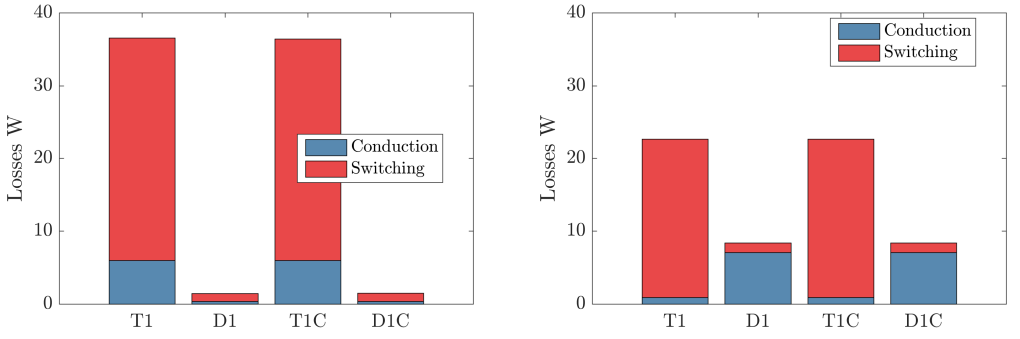
Figure 8.5: Conduction losses of the qZSI, F_{sw} = 50 kHz

In Figure 8.6 the switching losses are shown. The value shown is a representation of the losses the switch would have if it was switching all the time with the same voltage and current values, the ones at that point of the cycle. This is helpful in order to compare the losses with other topologies and switching frequencies. The varying width of the losses is due to the difference between turning on loss and turn-off losses. As expected, the ST states increase the losses considerably due to the higher currents present in the converter.



(a) 3 legs ST, inverter mode (b) 3 legs ST, rectifier mode

Figure 8.6: Switching losses of the qZSI, F_{sw} = 50 kHz



(a) 3 legs ST, inverter mode (b) 3 legs ST, rectifier mode

Figure 8.7: Losses of the qZSI, F_{sw} = 50 kHz

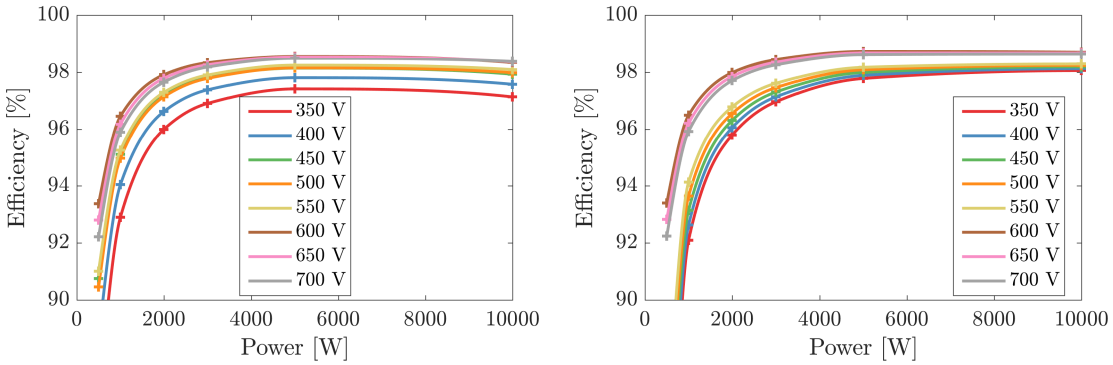
In Figure 8.7 the distribution of the losses is displayed. The plot bars show how whereas in inverter mode the conduction losses are mainly found in the power mosfets, in rectifier mode it is the diodes that conduct most of the current. The switching losses are also reduced in rectifier mode as the ST currents are not present because the input power of the PV is considered to be zero.

The filter design has been performed using the procedure in Section 4.8. Table 8.4 lists the different values of the LCL filter for 50 kHz switching frequency and 3 legs ST.

Table 8.4: Design parameters of the qZSI LCL filter, 3 legs ST F_{sw} = 50 kHz

Lfconv [mH]	Lfg [mH]	Cf [µF]	Rf [Ω]	fres [Hz]	Volume [dm^3]	Max loss [W]
0.711	0.062	0.698	4.34	17500	0.36	23.07

With this information it is possible to plot the efficiencies of the converter for both modes of operation and for both modulation techniques, see Figure 8.8. Both plots reveal that at higher boost factor B the losses are higher, decreasing the efficiency. It is also clear that the closer the modulation factor M is to one, the higher the efficiency. Therefore, maximum efficiency is found around $\sqrt{2}\sqrt{3}V_{grid}$.



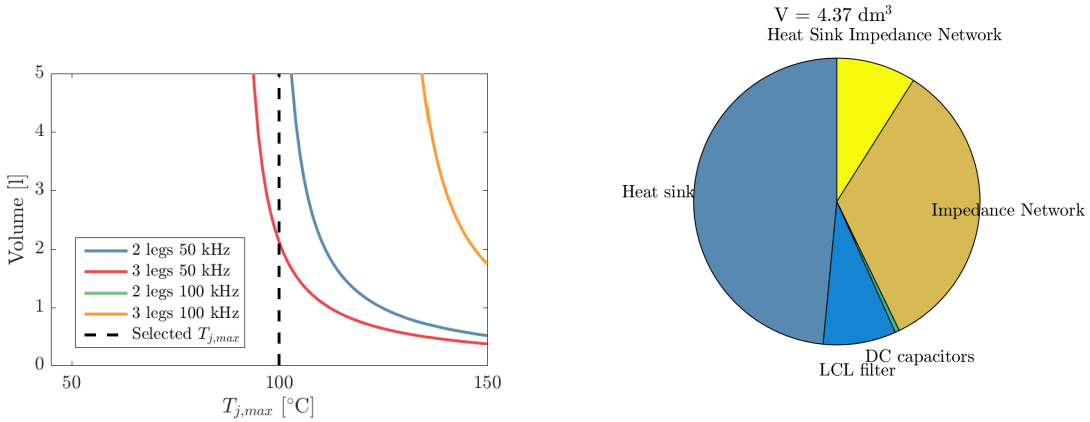
(a) Inverter mode (b) Rectifier mode

Figure 8.8: Efficiency of the qZSI at different operating points.

The design results for the qZSI with 3 legs ST switching at 50 kHz have already been displayed in Table 8.3. The weighted efficiency, calculated following the methods in Section 3.2 for both PV and Grid ports, has been computed to be 97.58%.

When the losses are known, it is possible to obtain the necessary cooling system size of the converter to keep the maximum junction temperatures $T_{j,max}$ under a certain limit. The operating point with maximum losses is found when the converter acts in the inverter mode and maximum input current from the PV panels, because the ST currents are maximum. Figure 8.9(a) shows the necessary heat sink size for the different configurations when considering different maximum values of junction temperature.

As expected, the losses when using 2 legs ST are much higher and make the cooling system either very big or not possible. The same happens for the converter working at 100 kHz switching frequency, which requires a very large cooling system; therefore, 2 legs ST and a switching frequency of 100 kHz have not been displayed in the results. The total volume and the distribution of the different elements that form the converter are shown in Figure 8.9(b).



(a) Cooling system size ($T_{j,max}$)

(b) Size distribution

Figure 8.9: qZSI system size

8.3. Converter evaluation

The qZSI rating shows how this topology is not a good solution for the multiport converter. Moreover, the fact that the inner DC voltages depend on the photovoltaic input make the implementation of the third converter much more difficult. The actual switching frequency is much higher than the predefined 50 kHz due to the ST states. However, implementing a lower switching frequency would increase the size of the impedance network, where already a lot of inductors have been considered.

Table 8.5: Evaluation of the qZSI.

Criterion	Total weight	Rating
Num Switches	3+3	5
Num Diodes	1+1	4
Num Cores	3	1
Capacitors	1+1	2
Efficiency	5+5	4
Volume	5+5	1
Leakage currents	4	3
Eff. Improve	1+1	1
Controlability	3+3	3
TOTAL		**125**

9

Conclusions

This master thesis project aims to select the optimum topology of a multiport converter which integrates photovoltaic on-grid generation and electric vehicle charging in an all-in-one power converter. The optimal topology is the one which performs better in a set of criteria, being the most important ones efficiency, to maximize profit, and volume, to achieve a highly integrable product. The first half of the report contains a literature review in order to determine the optimal candidates, a framework with the evaluation criteria to rank the topologies, the design of the magnetic elements, the selection of the different components and the analytical loss model for the assessment of the converters.

The second part of the report is a converter per converter review of the selected topologies. A detailed analysis of the steady state equations that describe the operation of each topology is performed, the requirements of the different elements derived and a short explanation regarding methods to improve the efficiency are listed. Afterwards, the design results are displayed in the form of plots and tables, which are used to finally evaluate each converter with respect to the predefined comparison framework. The topologies that have been compared are:

- DC Link based topologies
  - PV Port
    - Interleaved Boost Converter (IBC)
    - Coupled Inductors Interleaved Boost Converter (CIIBC)
    - Three Level Boost Converter (TLBC)
  - EV Port
    - Dual Active Bridge (DAB)
    - Interleaved Bidirectional Flyback Converter (IBFC)
  - Grid Port
    - Two Level Converter (2LC)
    - Three Level Neutral Point Clamped Converter (3LNPC²)
    - Three Level T-Type Converter (3LT²C)
- Impedance Network based topologies
  - quasi Z-Source Inverter (qZSI)

Some discussions can be done before concluding about the converter design and topology comparison:

- **SiC devices.** The topology comparison in this project has been performed taking into account that Silicon Carbide devices are used. SiC power devices have several advantages with respect

to Si power semiconductors; namely higher breakdown voltage, wider temperature range, and lower switching and conduction losses. Despite photovoltaic installations voltage is raising to increase the efficiency, the higher blocking voltages of SiC devices makes it possible to use single level topologies while still yielding very high efficiency.

- **Magnetic elements design.** In this report a detailed design procedure for inductors, coupled inductors and High Frequency Transformers is explained and used for the magnetics of all the topologies. Magnetic design is generally a difficult task as it differs considerably from ideal components to reality. Moreover, the design of coupled inductors in direct and reverse configuration presents even higher complexity, making it difficult to rely only in the parameters obtained from the analytical equations. FEM simulations have been performed, which indicate that the used equations are accurate enough, proving that the design procedure presented is accurate enough for comparison purposes.
- **Volume of the topologies.** It is commonly accepted that using higher switching frequencies results in a converter with lower volume. This is true in the case of the magnetic components, which usually see their size reduced with higher frequencies. However, higher frequencies yield higher losses in the semiconductors, increasing the cooling system size. An optimum in terms of cost regarding the magnetic elements and the heat sinks has to be found, as highly efficient cooling systems are also difficult to design and are expensive.
- **Interleaving.** Interleaving of converters has great impact in the final converter scores. For every topology, depending on the used components and necessary power rating, an optimum number of interleaved phases can be found. This fact is more remarkable in the DC-DC isolated topologies, where the current ripples are inherently high and interleaving reduces them considerably. Therefore, converters with low element count per phase, perform better than those which rely in a high number of semiconductors.
- **Framework influence.** A comparison framework has been proposed in order to compare the topologies. However, the weight of each criterion and the selected ranges for each criterion have a major influence in the final converter score. Therefore, it is important to have previous experience in the design of power converters to design the framework, resulting in better comparison results.

9.1. Optimal topology selection

The main focus of the thesis has been to answer the next set of questions, which result in the selection of the best topology for the multiport converter.

1. Which is the preferred solution in terms of interconnection of the three ports of the converter?

   Three different options have been reviewed in terms of internal structure of the multiport converter. First of all the common DC link, which relies in a central buffer to transfer the energy between the ports. Secondly, a three winding transformer or AC link, which would isolate all the ports in the converter. Lastly, the impedance network topologies, like the Z source inverter and derived topologies.

   The AC link architecture has numerous disadvantages, which are listed on Table 2.4 on Page 13, and the converter would still need a DC link for the interconnection of the grid. Moreover, it would result in a power converter with isolation between all ports, characteristic which is not needed between the PV and the Grid and increases the complexity of the system. Therefore, it has been the first discarded configuration in the report.

   On the other hand, the analyzed quasi Z-Source Inverter (qZSI) has many disadvantages with the maximum core size restriction, making it necessary to use a high number of inductors to reduce the stress. From the qZSI evaluation results, found on Page 152, the converter scores 122 points, which is much lower than two separate converters for PV and

Grid connection. Moreover, the fact that the inner DC voltages depend on the photovoltaic input make the implementation of the third converter much more difficult. This topology might prove more competitive in lower power/lower current applications, like single phase inverters.

Therefore, relying on a DC link is the preferred method for the multiport converter. It is more flexible and easier to implement, as the different ports are more or less independent. Moreover, it is a solution that could be easily adapted to future DC microgrids, enhancing the uses of the power converter.

2. Which is the optimal topology for a multiport converter which integrates photovoltaic energy production and electric vehicle charging, together with a grid connection?

   (a) Which is the optimal topology for the PV port?

   Three converters have been analyzed for the PV port: the Interleaved Boost Converter (IBC), the Coupled Inductors Interleaved Boost Converter (CIIBC) and the Three Level Boost Converter (TLBC). The evaluations of the different converters are found on pages 68, 78 and 87, while a summary which includes the best configuration of each topology is found on Table 9.1. The TLBC performs much worse than the other two topologies, scoring significantly lower.

Table 9.1: Review of the optimal configurations of the analyzed PV port converters.

Criterion	Weight	IBC 3 phases 50 kHz	CIIBC k=-0.9 4 ph. 50 kHz	TLBC 2 phases 50 kHz
Num. Switches	3	4	3	3
Num. Diodes	1	4	3	3
Num. Cores	3	4	5	5
Capacitors	1	5	5	4
Efficiency	5	4	4	3
Volume	5	3	4	2
Eff. Improve	1	2	3	2
Controlability	3	4	4	2
TOTAL		**82**	**87**	**64**

The selection between the IBC and the CIIBC is a difficult choice, as both score quite similar. The main difference is the number of cores and switches, as the coupled inductors version requires one less inductor but one more switch. Despite the increased design complexity, the preferred topology for the PV port is the four phases CIIBC. The CIIBC in the PV Port is built with:

- Two E65 cores, R material
- Four C2M0080120D SiC Mosfets
- Four C4D15120A SiC Diodes
- Two B32776 DC capacitors, 1100 V rated, 2 pins, 3µF

   (b) Which is the optimal topology for the EV port?

   Two converters have been analyzed for the EV port: the Dual Active Bridge (DAB) and the Interleaved Bidirectional Flyback Converter (IBFC). The evaluations of the different configurations of the converters are found on pages 100 and 109, while a summary

which includes the best configuration of each topology is found on Table 9.2.

Table 9.2: Review of the optimal configurations of the analyzed EV port converters.

Criterion	Weight	DAB 2 phases 100 kHz	IBFC 4 phases 50 kHz BCM
Num. Switches	3	2	3
Num. Diodes	1	5	2
Num. Cores	3	4	4
Capacitors	1	5	5
Efficiency	5	4	3
Volume	5	4	4
Output ripple	4	1	4
Eff. Improve	1	5	2
Controlability	3	4	3
TOTAL		**89**	**90**

The selection between the DAB and the IBFC is a difficult choice, as both topologies are very different and yet score almost the same. Due to the lower current ripple of the IBFC, this topology is preferred for EV charging, resulting in an extended life for the EV batteries. However, the design of such a converter is complicated and requires of a lot of experimentation and experience, as has already been seen in Section 6.2. The IBFC in the EV Port is built with:

- Four E65 cores, R material
- Twelve C2M0040120D SiC Mosfets
- Eight C4D15120A SiC Diodes for the primary side and four C4D20120A SiC Diodes for the secondary.
- Two B32776 DC capacitors, 700V rated, 3 pins, 8.5µF

(c) Which is the optimal topology for the Grid port?

Three converters have been analyzed for the Grid port: the Two Level Converter (2LC), the Three Level Neutral Point Clamped Converter (3LNPC²) and the Three Level T-Type Converter (3LT²C). The evaluations of the different converters are found on pages 124, 135 and 142, while a summary which includes the best configuration of each topology is found on Table 9.3.

The optimal topology for the case is the 2LC, the most used topology for DC-AC conversion. The fact that it requires a low number of switches and diodes and the reduced losses of the Near State Pulse-Width Modulation (NSPWM) technique makes the converter a very good solution, resulting in a high score. In the case that the most common Space Vector Pulse-Width Modulation (SVPWM) technique had to be used, the 3LT²C would be the most interesting topology. It has the advantage of being a three level configuration, with a reduced amount of semiconductors, topology that is easier to build with 1200 V rated semiconductors. The 2LC in the EV Port is built with:

- Six C2M0025120D SiC Mosfets
- Six C4D20120A SiC Diodes
- Two B32776 DC capacitors in parallel, 1100V rated, 3 pins, 12µF

- LCL filter:
  - MPP 26 Toroid, 906 0055909A2 ($L_{f,conv}$)
  - Kool Mu 125 Toroid, 168 0077254A7 ($L_{f,grid}$)
  - One B32796 3000 V RMS 5.6 µF AC capacitor

Table 9.3: Review of the optimal configurations of the analyzed Grid port converters.

Criterion	Weight	2LC 100 kHz NSPWM	3LNPC² 50 kHz SVPWM	3LT²C 50 kHz SVPWM
Num. Switches	3	5	3	3
Num. Diodes	1	5	1	3
Capacitors	1	5	1	1
Efficiency	5	3	4	4
Volume	5	4	5	5
Leakage currents	2	4	3	3
Eff. Improve	1	1	1	1
Controlability	3	3	4	4
TOTAL		**78**	**75**	**77**

3. Is this solution competitive in terms of cost, size and development time with respect to actual solutions?

   The previous answers yield to the optimal multiport converter topology: a four phases CIIBC at 50 kHz with reverse coupled inductors in the PV port, a four phases IBFC in the EV port in Boundary Conduction Mode (BCM) and a 100 kHz 2LC in the grid connection which uses NSPWM, see Figure 9.1. Both the IBC and 2LC are extensively used topologies, therefore they should not represent any problem in terms of design, cost or manufacture. On the other hand, the IBFC is a strange topology to use in high power applications, but has proved to be more suitable than the DAB.

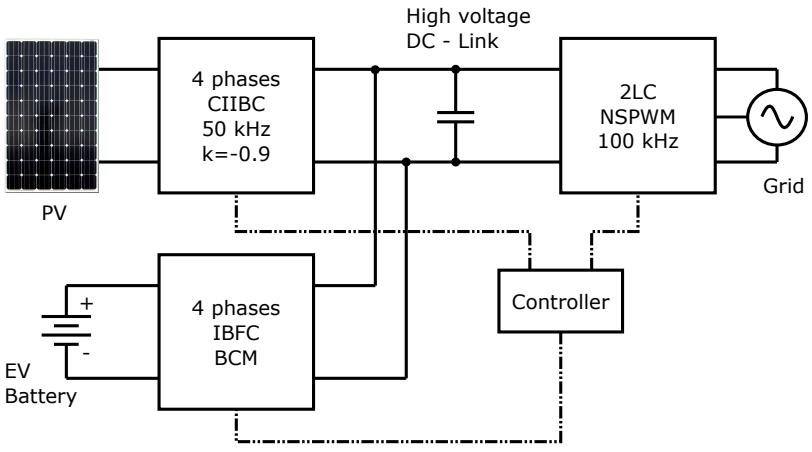


Figure 9.1: Block diagram of the final multiport converter

In terms of cost and size the proposed multiport converter is more competitive that the actual solution, which is using to separate power converters. The fact that only one DC-AC

converter is used reduces the total amount of components and the size of the converter, achieving a product with a lower cost. On the other hand, this converter has to be developed. DC link voltage balancing between the three ports should not present a much higher effort than the actual solutions which already rely on a DC link for power conversion. Therefore, the resulting multiport converter is a product that can be highly integrated in both solar charging stations and private households.

9.2. Future work

- **Extra EV topology.** The two selected EV port topologies are completely different; the IBFC is targeted for low power applications and the DAB for higher voltage and power applications. The considered IBFC has to be adapted from the regular Flyback topology in order to accommodate higher voltages, currents and bidirectionality, making it a more complicated topology. On the other hand, interleaving in the DAB has been proved to be advantageous in terms of current ripple but at the cost of using a high number of switches, reducing the score considerably. Therefore, other topologies could be considered for this power range, which are based in the same concept as the DAB but with lower amount of switches, as the Dual Active Half-Bridge (DAHB) [20] [105] shown in Figure 9.2. The addition of this topology to the work would allow for a better final decision.

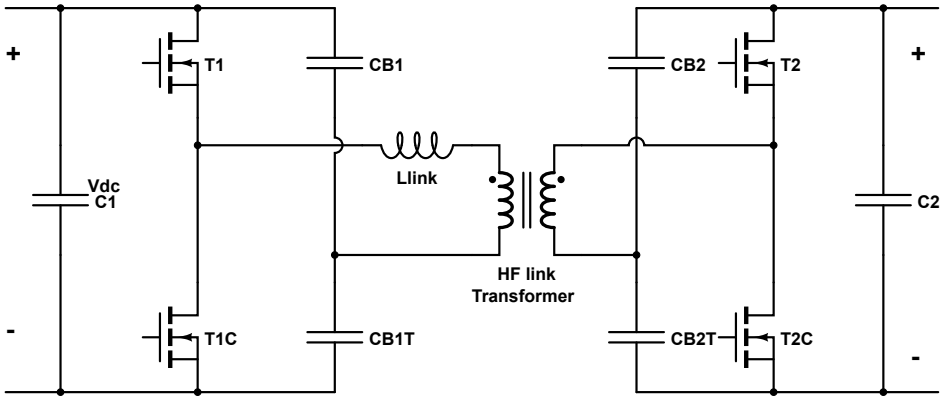


Figure 9.2: Structure of the DAHB

- **Resonant topologies.** This work has been based in the basic structure of some topologies which do not have inherent ZVS. However, there are certain topologies or modifications to the analyzed ones that use resonance in order to reduce the switching losses considerably.
- **Include cost in the framework.** The main missing criterion in the framework is the cost of the converter. Although commercially available devices have been used, it is very difficult to correctly determine the price of each converter as the component prices greatly depend on buying quantities and suppliers. Moreover, the rest of the converter parts like the PCB and controller board have also an impact on the converter cost and this aspects are very difficult to determine without having previous experience in converter design.
- **No inductor size restriction.** Some topologies, like the qZSI, have been affected by size restrictions in the magnetic elements, which allows for PCB mounting and the reduction of manufacturing costs. The same comparison could be performed with bigger E core sizes, which would allow for lower number of interleaved phases in some cases and better solutions in other topologies.
- **Silicon devices.** The difference in performance of using Si devices when compared to SiC could be evaluated. The main difference would be in terms of cost, as SiC devices are at the

moment considerably more expensive than traditional Silicon devices. A mixture of semiconductor technologies could be considered on the design too, by only replacing the devices with higher power losses, like diodes, by SiC elements. This could also improve the final converter selection but it increases the complexity of the design and comparison of every topology.

- **Further design optimization.** This work has intended to optimize each converter design as much as possible while still keeping some characteristics common between most topologies, like the switching frequency. For example, further research on different switching frequencies could have been done in each topology to find the optimal balance between efficiency and size. However, this is needs a more extensive research, reason why most designs are performed in two different switching frequencies, as the results show the advantages and disadvantages of the different frequencies.

Bibliography

[1] Charles R Sullivan and Richard Y Zhang. Simplified design method for litz wire. In *Applied Power Electronics Conference and Exposition (APEC), 2014 Twenty-Ninth Annual IEEE*, pages 2667–2674. IEEE, 2014.

[2] I F II. Ieee recommended practices and requirements for harmonic control in electrical power systems. 1993.

[3] Biswajit Ray, Hiroyuki Kosai, Seana McNeal, Brett Jordan, and James Scofield. A comprehensive multi-mode performance analysis of interleaved boost converters. pages 3014–3021, 2010.

[4] Jayakrishnan Radhakrishna Pillai and Birgitte Bak-Jensen. Integration of vehicle-to-grid in the western danish power system. *IEEE Transactions on Sustainable Energy*, 2(1):12–19, 2011.

[5] Yi Wang, Sjoerd De Haan, and Jan Abraham Ferreira. Methods for experimental assessment of component losses to validate the converter loss model. In *Power Electronics and Motion Control Conference, 2008. EPE-PEMC 2008. 13th*, pages 187–194. IEEE, 2008.

[6] GR Chandra Mouli, P Bauer, and M Zeman. Comparison of system architecture and converter topology for a solar powered electric vehicle charging station. In *Power Electronics and ECCE Asia (ICPE-ECCE Asia), 2015 9th International Conference on*, pages 1908–1915. IEEE, 2015.

[7] SolarGis s.r.o. Solargis solar databases and maps. 2015.

[8] GR Chandra Mouli, P Bauer, and M Zeman. System design for a solar powered electric vehicle charging station for workplaces. *Applied Energy*, 168:434–443, 2016.

[9] Roberto Faranda and Sonia Leva. Energy comparison of mppt techniques for pv systems. *WSEAS transactions on power systems*, 3(6):446–455, 2008.

[10] Wook Kim, Van-Huan Duong, Thanh-Tuan Nguyen, and Woojin Choi. Analysis of the effects of inverter ripple current on a photovoltaic power system by using an ac impedance model of the solar cell. *Renewable Energy*, 59:150–157, 2013.

[11] International Standard. Electric vehicle conductive charging system - part 23: Dc electric vehicle charging station. 2016.

[12] Hariharan Krishnaswami and Ned Mohan. Three-port series-resonant dc–dc converter to interface renewable energy sources with bidirectional load and energy storage ports. *IEEE Transactions on Power Electronics*, 24(10):2289–2297, 2009.

[13] Gierri Waltrich, Jorge L Duarte, and Marcel AM Hendrix. Multiport converter for fast charging of electrical vehicle battery. *IEEE Transactions on Industry Applications*, 48(6):2129–2139, 2012.

[14] Quan Li and Peter Wolfs. A review of the single phase photovoltaic module integrated converter topologies with three different dc link configurations. *IEEE Transactions on Power Electronics*, 23(3):1320–1333, 2008.

[15] Soeren Baekhoej Kjaer, John K Pedersen, and Frede Blaabjerg. A review of single-phase grid-connected inverters for photovoltaic modules. *IEEE transactions on industry applications*, 41(5):1292–1306, 2005.

[16] JM Enrique, E Duran, M Sidrach-de Cardona, and JM Andujar. Theoretical assessment of the maximum power point tracking efficiency of photovoltaic facilities with different converter topologies. *Solar Energy*, 81(1):31–38, 2007.

[17] Ned Mohan and Tore M Undeland. *Power electronics: converters, applications, and design*. John Wiley & Sons, 2007.

[18] Shaoting Zhang. Analysis and minimization of the input current ripple of interleaved boost converter. In *Applied Power Electronics Conference and Exposition (APEC), 2012 Twenty-Seventh Annual IEEE*, pages 852–856. IEEE, 2012.

[19] Michael T Zhang, Yimin Jiang, Fred C Lee, and Milan M Jovanovic. Single-phase three-level boost power factor correction converter. In *Applied Power Electronics Conference and Exposition, 1995. APEC'95. Conference Proceedings 1995., Tenth Annual*, pages 434–439. IEEE, 1995.

[20] Yu Du, Srdjan Lukic, Boris Jacobson, and Alex Huang. Review of high power isolated bi-directional dc-dc converters for phev/ev dc charging infrastructure. In *2011 IEEE Energy Conversion Congress and Exposition*, pages 553–560. IEEE, 2011.

[21] MN Kheraluwala, Randal W Gascoigne, Deepakraj M Divan, and Eric D Baumann. Performance characterization of a high-power dual active bridge dc-to-dc converter. *IEEE Transactions on Industry applications*, 28(6):1294–1301, 1992.

[22] K Venkatesan. Current mode controlled bidirectional flyback converter. In *Power Electronics Specialists Conference, 1989. PESC'89 Record., 20th Annual IEEE*, pages 835–842. IEEE, 1989.

[23] Ahmet M Hava, Russel J Kerkman, and Thomas A Lipo. Simple analytical and graphical methods for carrier-based pwm-vsi drives. *IEEE Transactions on Power Electronics*, 14(1):49–61, 1999.

[24] Akira Nabae, Isao Takahashi, and Hirofumi Akagi. A new neutral-point-clamped pwm inverter. *IEEE Transactions on industry applications*, (5):518–523, 1981.

[25] Mario Schweizer and Johann W Kolar. Design and implementation of a highly efficient three-level t-type converter for low-voltage applications. *IEEE Transactions on Power Electronics*, 28(2):899–907, 2013.

[26] Fang Zheng Peng. Z-source inverter. *IEEE Transactions on industry applications*, 39(2): 504–510, 2003.

[27] Yuan Li, Joel Anderson, Fang Z Peng, and Dichen Liu. Quasi-z-source inverter for photovoltaic power generation systems. pages 918–924, 2009.

[28] T Todorčević, P Bauer, and JA Ferreira. Comparison of bidirectional medium-voltage dc-dc converters for energy harvesting using dielectric elastomers. In *PCIM Europe*, pages 673–680, 2013.

[29] organization=DIN VDE VERLAG, year=2013. Automatic disconnection device between a generator and the public low-voltage grid.

[30] Kotub Uddin, Andrew D Moore, Anup Barai, and James Marco. The effects of high frequency current ripple on electric vehicle battery performance. *Applied Energy*, 178:142–154, 2016.

[31] Marcelo C Cavalcanti, Alexandre M Farias, Kleber C Oliveira, Francisco AS Neves, and João Luiz Afonso. Eliminating leakage currents in neutral point clamped inverters for photovoltaic systems. *Industrial Electronics, IEEE Transactions on*, 59(1):435–443, 2012.

[32] Ward I Bower and John C Wiles. Analysis of grounded and ungrounded photovoltaic systems. In *Photovoltaic Energy Conversion, 1994., Conference Record of the Twenty Fourth. IEEE Photovoltaic Specialists Conference-1994, 1994 IEEE First World Conference on*, volume 1, pages 809–812. IEEE, 1994.

[33] Tamas Kerekes, Marco Liserre, Remus Teodorescu, Christian Klumpner, and Mark Sumner. Evaluation of three-phase transformerless photovoltaic inverter topologies. *Power Electronics, IEEE Transactions on*, 24(9):2202–2211, 2009.

[34] Kheng Suan Freddy Tan, Nasrudin A Rahim, Wooi-Ping Hew, and Hang Seng Che. Modulation techniques to reduce leakage current in three-phase transformerless h7 photovoltaic inverter. *Industrial Electronics, IEEE Transactions on*, 62(1):322–331, 2015.

[35] Xiaoqiang Guo, Ran He, Jiamin Jian, Zhigang Lu, Xiaofeng Sun, and Josep M Guerrero. Leakage current elimination of four-leg inverter for transformerless three-phase pv systems. *Power Electronics, IEEE Transactions on*, 31(3):1841–1846, 2016.

[36] Emre Ün and Ahmet M Hava. A near-state pwm method with reduced switching losses and reduced common-mode voltage for three-phase voltage source inverters. *Industry Applications, IEEE Transactions on*, 45(2):782–793, 2009.

[37] June-Seok Lee and Kyo-Beum Lee. New modulation techniques for a leakage current reduction and a neutral-point voltage balance in transformerless photovoltaic systems using a three-level inverter. *Power Electronics, IEEE Transactions on*, 29(4):1720–1732, 2014.

[38] Florian Krismer. *Modeling and optimization of bidirectional dual active bridge DC-DC converter topologies*. PhD thesis, Diss., Eidgenössische Technische Hochschule ETH Zürich, Nr. 19177, 2010, 2010.

[39] C Miesner, R Rupp, Holger Kapels, Michael Krach, and I Zverev. thinq!™ silicon carbide schottky diodes: An smps circuit designer's dream comes true! *Technical White Paper*, 2001.

[40] Kapil Venkatachalam, Charles R Sullivan, Tarek Abdallah, and Hernán Tacca. Accurate prediction of ferrite core loss with nonsinusoidal waveforms using only steinmetz parameters. In *IEEE Workshop on Computers in Power Electronics*, volume 2002, pages 36–41, 2002.

[41] Inc. QuadTech. Equivalent series resitance (esr) of capacitors, application note. 2007. URL `http://my.ece.ucsb.edu/York/Bobsclass/194/References/General/ESR%20of%20Capacitors.pdf`.

[42] Inc. Electronic Concepts. Current ratings and dissipated power in dc and ac applications, application note. 2009. URL `http://www.ecicaps.com/tech-tools/technical-papers/current-ratings-dissipated-power-dc-ac-applications/`.

[43] Muhammad H Rashid. *Power electronics handbook: devices, circuits and applications*. Academic press, 2010.

[44] CE Commission et al. Emerging renewables program guidebook. 2011.

[45] C. Kurz R. Pfatischer H. te Heesen, M. Baron. Definition of the euro efficiency of solar modules. *5th World Conference on Photovoltaic Energy Conversion*, pages 4154–4155, 2010.

[46] Martin A Green, Keith Emery, Yoshihiro Hishikawa, Wilhelm Warta, and Ewan D Dunlop. Solar cell efficiency tables (version 45). *Progress in photovoltaics: research and applications*, 23(1): 1–9, 2015.

[47] Michael H Bierhoff and Friedrich W Fuchs. Semiconductor losses in voltage source and current source igbt converters based on analytical derivation. In *Power Electronics Specialists Conference, 2004. PESC 04. 2004 IEEE 35th Annual*, volume 4, pages 2836–2842. IEEE, 2004.

[48] Mario Schweizer. *System-oriented efficiency optimization of variable speed drives*. PhD thesis, ETH Zürich, 2012.

[49] Colonel Wm T McLyman. *Transformer and inductor design handbook*. CRC press, 2016.

[50] Ralf Kories and Heinz Schmidt-Walter. *Electrical engineering: a pocket reference*. Springer Science & Business Media, 2011.

[51] JA Ferreira. Ånalytical computation of ac resistance of round and rectangular litz wire windings. *Electric Power Applications, IEE Proceedings B*, 139(1):21–25, 1992.

[52] J Muhlethaler, Johannw Walter Kolar, and Andreas Ecklebe. Loss modeling of inductive components employed in power electronic systems. In *Power Electronics and ECCE Asia (ICPE & ECCE), 2011 IEEE 8th International Conference on*, pages 945–952. IEEE, 2011.

[53] Sanjaya Maniktala. *Switching Power Supplies A-Z*. Elsevier, 2012.

[54] Stan Zurek. Thermal resistance of ferrite cores. 2016. URL `http://encyclopedia-magnetica.com/doku.php/thermal_resistance_of_ferrite_cores`.

[55] Marco Liserre, Frede Blaabjerg, and Steffan Hansen. Design and control of an lcl-filter-based three-phase active rectifier. *Industry Applications, IEEE Transactions on*, 41(5):1281–1291, 2005.

[56] Khaled H Ahmed, Stephen J Finney, and Barry W Williams. Passive filter design for three-phase inverter interfacing in distributed generation. In *Compatibility in Power Electronics, 2007. CPE'07*, pages 1–9. IEEE, 2007.

[57] Hanju Cha and Trung-Kien Vu. Comparative analysis of low-pass output filter for single-phase grid-connected photovoltaic inverter. In *Applied Power Electronics Conference and Exposition (APEC), 2010 Twenty-Fifth Annual IEEE*, pages 1659–1665. IEEE, 2010.

[58] Kamran Jalili and Steffen Bernet. Design of filters of active-front-end two-level voltage-source converters. *Industrial Electronics, IEEE Transactions on*, 56(5):1674–1689, 2009.

[59] Remus Beres, Xiongfei Wang, Frede Blaabjerg, Marco Liserre, and Claus Bak. A review of passive power filters for three-phase grid connected voltage-source converters. 2016.

[60] Rafael Pena-Alzola, Marco Liserre, Frede Blaabjerg, Rafael Sebastián, Jorg Dannehl, and Friedrich Wilhelm Fuchs. Analysis of the passive damping losses in lcl-filter-based grid converters. *Power Electronics, IEEE Transactions on*, 28(6):2642–2646, 2013.

[61] Juergen Biela, Uwe Badstuebner, and Johann W Kolar. Impact of power density maximization on efficiency of dc–dc converter systems. *IEEE Transactions on Power Electronics*, 24(1): 288–300, 2009.

[62] Johann W Kolar, Uwe Drofenik, Juergen Biela, Marcello L Heldwein, Hans Ertl, Thomas Friedli, and Simon D Round. Pwm converter power density barriers. In *Power Conversion Conference-Nagoya, 2007. PCC'07*, pages P–9. IEEE, 2007.

[63] Uwe Drofenik, Gerold Laimer, and Johann W Kolar. Theoretical converter power density limits for forced convection cooling. In *Proceedings of the International PCIM Europe 2005 Conference*, pages 608–619, 2005.

[64] Seri Lee. Optimum design and selection of heat sinks. In *Semiconductor Thermal Measurement and Management Symposium, 1995. SEMI-THERM XI., Eleventh Annual IEEE*, pages 48–54. IEEE, 1995.

[65] Uwe Drofenik and Johann W Kolar. Sub-optimum design of a forced air cooled heat sink for simple manufacturing. In *Power Conversion Conference-Nagoya, 2007. PCC'07*, pages 1189–1194. IEEE, 2007.

[66] Madhusudan Iyengar and Avram Bar-Cohen. Design for manufacturability of sise parallel plate forced convection heat sinks. In *Thermal and Thermomechanical Phenomena in Electronic Systems, 2000. ITHERM 2000. The Seventh Intersociety Conference on*, volume 1. IEEE, 2000.

[67] Juergen Biela, Mario Schweizer, Stefan Waffler, and Johann W Kolar. Sic versus si—evaluation of potentials for performance improvement of inverter and dc–dc converter systems by sic power semiconductors. *IEEE transactions on industrial electronics*, 58(7): 2872–2882, 2011.

[68] Uwe Drofenik and Johann W Kolar. Analyzing the theoretical limits of forced air-cooling by employing advanced composite materials with thermal conductivities> 400w/mk. In *Integrated Power Systems (CIPS), 2006 4th International Conference on*, pages 1–6. VDE, 2006.

[69] Doo-Yong Jung, Young-Hyok Ji, Sang-Hoon Park, Yong-Chae Jung, and Chung-Yuen Won. Interleaved soft-switching boost converter for photovoltaic power-generation system. *IEEE transactions on power electronics*, 26(4):1137–1145, 2011.

[70] Majid Pahlevaninezhad, Pritam Das, Josef Drobnik, Praveen K Jain, and Alireza Bakhshai. A zvs interleaved boost ac/dc converter used in plug-in electric vehicles. *IEEE Transactions on Power Electronics*, 27(8):3513–3529, 2012.

[71] Yao-Ching Hsieh, Te-Chin Hsueh, and Hau-Chen Yen. An interleaved boost converter with zero-voltage transition. *IEEE Transactions on Power Electronics*, 24(4):973–978, 2009.

[72] Ching-Jung Tseng and Chern-Lin Chen. A passive lossless snubber cell for nonisolated pwm dc/dc converters. *IEEE Transactions on Industrial Electronics*, 45(4):593–601, 1998.

[73] Jun Imaoka, Masayoshi Yamamoto, and Takahiro Kawashima. High-power-density three-phase interleaved boost converter with a novel coupled inductor. *IEEJ journal of industry applications*, 4(1):20–30, 2015.

[74] Hiroyuki Kosai, Seana McNeal, Austin Page, Brett Jordan, Jim Scofield, and Biswajit Ray. Characterizing the effects of inductor coupling on the performance of an interleaved boost converter. *Proc. 29th Annual Passive Components and Exhibition (CARTS USA-2009)*, pages 237–251, 2009.

[75] Maja Harfman Todorovic, Leonardo Palma, and Prasad N Enjeti. Design of a wide input range dc–dc converter with a robust power control scheme suitable for fuel cell power conversion. *IEEE Transactions on Industrial Electronics*, 55(3):1247–1255, 2008.

[76] Hongyang Wu and Xiangning He. Single phase three-level power factor correction circuit with passive lossless snubber. *IEEE Transactions on Power Electronics*, 17(6):946–953, 2002.

[77] Vasiliy Vorobei, Janis Zakis, Oleksandr Husev, Oleksandr Veligorskyi, and Oleksandr Savenko. Simulation study of the three-level boost dc-dc converter with full zvs for pv application. In *2015 9th International Conference on Power Electronics and ECCE Asia (ICPE-ECCE Asia)*, pages 2038–2043. IEEE, 2015.

[78] Lung-Sheng Yang, Tsorng-Juu Liang, Hau-Cheng Lee, and Jiann-Fuh Chen. Novel high step-up dc–dc converter with coupled-inductor and voltage-doubler circuits. *iEEE Transactions on industrial Electronics*, 58(9):4196–4206, 2011.

[79] Jung-Min Kwon, Bong-Hwan Kwon, and Kwang-Hee Nam. Three-phase photovoltaic system with three-level boosting mppt control. *IEEE Transactions on Power Electronics*, 23(5): 2319–2327, 2008.

[80] Hung-Chi Chen and Jhen-Yu Liao. Design and implementation of sensorless capacitor voltage balancing control for three-level boosting pfc. *IEEE Transactions on Power Electronics*, 29(7): 3808–3817, 2014.

[81] Deepak E Soman, Remya Krishna, Mats Leijon, Kasthuri Vikram, Sasi K Kottayil, Lais A Vitoi, Janaina G Oliveira, and Sanjay S Kumar. Discontinuous conduction mode of a three-level boost dc-dc converter and its merits and limits for voltage cross regulation applications. In *IECON 2014-40th Annual Conference of the IEEE Industrial Electronics Society*, pages 4268–4272. IEEE, 2014.

[82] Rik W DeDoncker, Mustansir H Kheraluwala, and Deepakraj M Divan. Power conversion apparatus for dc/dc conversion using dual active bridges, June 25 1991. US Patent 5,027,264.

[83] DJ Costinett. *Analysis and Design of High Efficiency, High Conversion Ratio, DC-DC Power Converters*. PhD thesis, Citeseer, 2013.

[84] Y Wang, SWH De Haan, and JA Ferreira. Optimal operating ranges of three modulation methods in dual active bridge converters. In *Power Electronics and Motion Control Conference, 2009. IPEMC'09. IEEE 6th International*, pages 1397–1401. IEEE, 2009.

[85] German G Oggier, Guillermo O Garcia, and Alejandro R Oliva. Switching control strategy to minimize dual active bridge converter losses. *IEEE Transactions on Power Electronics*, 24(7): 1826–1838, 2009.

[86] Hua Bai and Chris Mi. Eliminate reactive power and increase system efficiency of isolated bidirectional dual-active-bridge dc–dc converters using novel dual-phase-shift control. *IEEE Transactions on Power Electronics*, 23(6):2905–2914, 2008.

[87] Biao Zhao, Qiang Song, Wenhua Liu, and Yandong Sun. Overview of dual-active-bridge isolated bidirectional dc–dc converter for high-frequency-link power-conversion system. *IEEE Transactions on Power Electronics*, 29(8):4091–4106, 2014.

[88] F Krismer, J Biela, and JW Kolar. A comparative evaluation of isolated bi-directional dc/dc converters with wide input and output voltage range. In *Fourtieth IAS Annual Meeting. Conference Record of the 2005 Industry Applications Conference, 2005.*, volume 1, pages 599–606. IEEE, 2005.

[89] Christophe Basso. How to deal with leakage elements in flyback converters. *On Semiconductor, AN1679/D*, 2005.

[90] Robert Watson, Fred C Lee, and Guichao C Hua. Utilization of an active-clamp circuit to achieve soft switching in flyback converters. *IEEE Transactions on Power Electronics*, 11(1): 162–169, 1996.

[91] Ahmed Elasser and David A Torrey. Soft switching active snubbers for dc/dc converters. *IEEE transactions on Power electronics*, 11(5):710–722, 1996.

[92] Jae-Eul Yoon. Application note: An-8025 design guideline of single-stage flyback ac-dc converter using fan7530 for led lighting. *Fairchild Semiconductor*, 2009.

[93] Chih-Sheng Liao and Keyue M Smedley. Design of high efficiency flyback converter with energy regenerative snubber. In *Applied Power Electronics Conference and Exposition, 2008. APEC 2008. Twenty-Third Annual IEEE*, pages 796–800. IEEE, 2008.

[94] Gang Chen, Yim-Shu Lee, SYR Hui, Dehong Xu, and Yousheng Wang. Actively clamped bidirectional flyback converter. *IEEE Transactions on Industrial Electronics*, 47(4):770–779, 2000.

[95] Thomas G Habetler, Francesco Profumo, Michele Pastorelli, and Leon M Tolbert. Direct torque control of induction machines using space vector modulation. *IEEE Transactions on Industry Applications*, 28(5):1045–1053, 1992.

[96] WC Duesterhoeft, Max W Schulz, and Edith Clarke. Determination of instantaneous currents and voltages by means of alpha, beta, and zero components. *Transactions of the American Institute of Electrical Engineers*, 70(2):1248–1255, 1951.

[97] Donald Grahame Holmes. The general relationship between regular-sampled pulse-width-modulation and space vector modulation for hard switched converters. In *Industry Applications Society Annual Meeting, 1992., Conference Record of the 1992 IEEE*, pages 1002–1009. IEEE, 1992.

[98] Ahmet M Hava, Russel J Kerkman, and Thomas A Lipo. Simple analytical and graphical methods for carrier-based pwm-vsi drives. *Power Electronics, IEEE Transactions on*, 14(1):49–61, 1999.

[99] Ghanshyamsinh Gohil, Lorand Bede, Remus Teodorescu, Tamas Kerekes, and Frede Blaabjerg. Analytical method to calculate the dc link current stress in voltage source converters. In *Power Electronics, Drives and Energy Systems (PEDES), 2014 IEEE International Conference on*, pages 1–6. IEEE, 2014.

[100] RS Kanchan, MR Baiju, KK Mohapatra, PP Ouseph, and K Gopakumar. Space vector pwm signal generation for multilevel inverters using only the sampled amplitudes of reference phase voltages. *IEE Proceedings-Electric Power Applications*, 152(2):297–309, 2005.

[101] Marcelo C Cavalcanti, Alexandre M Farias, Kleber C Oliveira, Francisco AS Neves, and João Luiz Afonso. Eliminating leakage currents in neutral point clamped inverters for photovoltaic systems. *Industrial Electronics, IEEE Transactions on*, 59(1):435–443, 2012.

[102] Xiaoqiang Guo, Marcelo C Cavalcanti, Alexandre M Farias, and Josep M Guerrero. Single-carrier modulation for neutral-point-clamped inverters in three-phase transformerless photovoltaic systems. *Power Electronics, IEEE Transactions on*, 28(6):2635–2637, 2013.

[103] Qianfan Zhang, Shuai Dong, Chunyang Zhao, Haole Wang, Shukang Cheng, and Rui Wang. Analysis of freewheeling state in z-source inverter under three-phase shoot-through mode. pages 5505–5510, 2015.

[104] Miaosen Shen, Jin Wang, Alan Joseph, Fang Z Peng, Leon M Tolbert, and Donald J Adams. Maximum constant boost control of the z-source inverter. In *Industry Applications Conference, 2004. 39th IAS Annual Meeting. Conference Record of the 2004 IEEE*, volume 1. IEEE, 2004.

[105] Xinyu Xu, Ashwin M Khambadkone, and Ramesh Oruganti. A soft-switched back-to-back bidirectional dc/dc converter with a fpga based digital control for automotive applications. In *Industrial Electronics Society, 2007. IECON 2007. 33rd Annual Conference of the IEEE*, pages 262–267. IEEE, 2007.

Appendices

A

List of elements

In this Appendix the different elements used for the design of the different converters are listed. Only the most important data of each component is listed, and not the linear regressions performed in the different datasheets in order to obtain an accurate loss model. A selection of datasheets can be found in Appendix F.

A.1. Mosfets

CREE SiC mosfets have been selected for the design of the different converters. Table A.1 shows their most important characteristics.

Table A.1: Available SiC Mosfets for the designs.

CREE Mosfet	$V_{DS,max}$ [V]	$I_{DS,max}$ [A]	$R_{DS,on}$ [mΩ]	R_{tj}	E_{on} [µJ]	E_{off} [µJ]
C3M0280090D	900	7.5	280	2.3	57	6
C3M0120090D	900	15	120	1.3	170	25
C3M0065090D	900	23	65	1.0	226	36
C2M0280120D	1200	6	280	2.0	32	37
C2M0160120D	1200	12.5	160	1.0	79	57
C2M0080120D	1200	20	80	0.7	265	135
C2M0040120D	1200	40	45	0.4	1000	400
C2M0025120D	1200	60	25	0.27	1400	300

A.2. Diodes

CREE SiC diodes have been selected for the design of the different converters. Table A.2 shows their most important characteristics.

Table A.2: Available SiC Diodes for the designs.

CREE Diode	$V_{r,max}$ [V]	$I_{f,max}$ [A]	$V_{f,max}$ [V]	R_{tj}	Q_c [nC]
C3D04065A	650	6	1.7	2.9	10
C3D08065A	650	11	1.8	1.4	20
C3D10065A	650	14	1.8	1.1	24
C3D20065D	650	26	1.8	0.65	48
C5D50065D	650	50	1.8	0.5	110
C4D02120A	1200	5	1.8	2.5	11
C4D05120A	1200	8	1.8	1.85	27
C4D08120A	1200	11	1.8	1.26	37
C4D10120A	1200	14	1.8	1.1	52
C4D15120A	1200	20	1.8	0.78	77.5
C4D20120A	1200	25.5	1.8	0.62	99
C4D20120D	1200	33	1.8	0.43	104
C4D30120D	1200	43	1.8	0.34	155
C4D40120D	1200	54	1.8	0.29	198

A.3. Insulation pad

The same insulation pad has been considered for all semiconductor attachments to heat sinks. Its comercial name is Hi-Flow 300P form the company BERGQUIST. It has a thermal performance of 0.94 ºC/W at 0.0010 psi. The maximum continued use temperature is 150 ºC and the phase change temperature is 55 ºC. The dielectric breakdown voltage V_{ac} is stated to be 5000 V at the datasheet.

A.4. Power inductor E cores

The E core shapes listed in Table A.3 have been considered for the design of power inductor and coupled inductors, as well as the Flyback Transformer (FBT)s.

Table A.3: Available core options for the designs.

Ferrite Cores	le [cm]	Ac [cm^2]	Wa [cm^2]	MLT [cm]	V_c [cm^3]
E16	3.76	0.201	0.216	3.3	0.76
E25	4.9	0.395	0.562	4.91	1.94
E32	7.4	0.83	0.97	6	6.14
E42	9.7	1.78	1.78	9.3	17.27
E55	12.4	3.53	2.5	11.6	43.77
E65	14.7	5.4	3.94	15	79.38

The materials that have been considered for the E cores are shown in Table A.4.

Table A.4: Characteristics of the different ferrite materials.

Ferrites	Manufacturer	B_{sat}	μ	K	a	b
3C96	Ferroxcube	0.4	2500	0.00512	1.34	2.66
3C92	Ferroxcube	0.42	2500	0.0265	1.19	2.65
R material	MAG Inc	0.4	2300	0.0027	1.43	2.85
P material	MAG Inc	0.4	2500	0.0095	1.36	2.86

A.5. Filter inductor toroid cores

In Table A.5 the different considered toroids for the LCL filter design for the grid output of the multiport converter are listed.

Table A.5: Available toroids for the LCL filter designs.

Toroid MAG Inc	Material	Ac [cm^2]	Wa [cm^2]	V_c [cm3]
195 0077192A7	Kool Mu 60	2.29	5.14	28.60
102 0077099A7	Kool Mu 60	3.58	97.64	86.90
102 0077102A7	Kool Mu 26	3.58	24.70	86.90
620 0077615A7	Kool Mu 26	3.60	7.89	51.80
930 0077894A7	Kool Mu 60	0.65	1.56	4.15
620 0078615A7	Xflux 26	3.60	7.89	51.80
0088192A7	Amoflux	2.29	5.14	28.60
620 0077620A7	Kool Mu 125	3.60	7.89	51.80
195 0077192A7	MPP 26	2.29	5.14	28.60
620 0077620A7	Kool Mu 60	3.60	7.89	51.80
906 0078615A7	Kool Mu 26	2.21	18.20	43.40
906 0077907A7	Kool Mu 60	2.21	18.20	43.40
906 0055909A2	MPP 14	2.21	18.20	43.40
906 0055909A2	MPP 26	2.21	18.20	43.40
620 0055908A2	High Flux 26	2.21	18.20	43.40
102 0058102A2	High Flux 26	3.58	24.70	86.90
287 0077195A7	Kool Mu 125	2.29	5.14	28.60
60 0078191A7	Xflux 26	2.29	5.14	28.60
287 C058195A2	High Flux 125	2.29	5.14	28.60
168 0077254A7	Kool Mu 125	1.07	4.27	10.60
88 0078735A7	Xflux 26	4.97	15.50	91.40

The different powder materials characteristics are found on Table A.6

Table A.6: Characteristics of the different powder materials.

Toroid Materials	B_{sat}	μ	K	a	b
Kool Mu 60	0.9	60	0.026	1.29	2.01
Kool Mu 125	0.9	125	0.012	1.63	2.2
Kool Mu 26	0.9	26	0.05	1.46	2.09
Xflux 26	1.4	26	0.0011	1.825	1.332
Amoflux	1.4	60	0.0006	1.65	2.2
MPP 26	0.6	26	0.0008	1.65	2.34
MPP 14	0.6	14	0.0003	1.87	2.5
High Flux 26	1.4	26	0.0093	1.54	2.31
High Flux 125	1.4	125	0.0093	1.47	2.23

A.6. HFT U shaped cores

The U core shapes listed in Table A.7 have been considered for the design of High Frequency Transformer (HFT).

Table A.7: Available U core options for the HFT designs.

Core No.	l_m[cm]	A_c [cm^2]	W_a [cm ^{2}]	V_c [cm^3]
2x AMCC 4	12.2	2.22	3.3	27
AMCC 6.3	12.8	3.2	3.6	42
AMCC 8	13	3.6	3.9	47
AMCC 10	15.4	3.6	5.2	54
AMCC 16A	15.1	4.6	5.2	68
AMCC 16B	17	4.6	6.5	77
AMCC 20	17.5	5.4	6.5	92
AMCC 25	19.6	5.4	8.4	104
AMCC 32	20	6.4	8.4	124
AMCC 40	19.9	7.4	8.4	145
AMCC 50	24.9	6.6	14	160
AMCC 63	25.3	7.8	14	192
AMCC 80	25.4	10.4	14	256
AMCC 100	25	11.8	14	288
AMCC 125	30.2	11	20.8	318
AMCC 160	28.5	12.4	20.8	364
AMCC 200	29.8	15.6	20.8	455
AMCC 250	31.4	18.6	22.5	572

The materials of Table A.8 have been considered for the designs of the HFT.

Table A.8: Characteristics of the different HFT materials.

HFT materials	B_{sat}	K	a	b
METGLAS 2605SA1	1.56	0.0467	1.51	1.74
MKM Nanocrystalline	1.1	0.000156	1.58	2.1
VAC Vitroperm500F	1.2	0.0000987	1.8	2.08
Hitachi Finemet FT-3M	1.23	0.000111	1.62	1.98

A.7. DC filter capacitors

In Table A.9 a list of EPCOS capacitors can be found, which have been used for DC filtering purposes.

Table A.9: Available DC capacitors for the designs.

DC Capacitors	$V_{c,max}$ [V]	$I_{c,rms,max}$ [A]	C [µF]	ESR [mΩ]	ESL [nH]	A_c [cm^2]	V_c [cm^3]
B32776 - 450 - 12	450	7	12	17.1	19	9.84	14.76
B32776 - 450 - 30	450	14	30	7	11	8.3	32.79
B32776 - 700 - 8.5	700	7.5	8.5	17.8	18	9.96	18.92
B32776 - 700 - 15	700	12	8.5	9.6	10	8.3	32.79
B32776 - 700 - 20	700	14.5	20	7.5	10	11.76	43.51
B32776 - 700 - 25	700	17	25	6.1	11	11.62	49.39
B32776 - 700 - 35	700	22	35	4.3	14	13.86	66.53
B32776 - 1100 - 2.7	1100	5	2.7	34.7	19	9.96	14.94
B32776 - 1100 - 8	1100	11	8	12.1	12	8.3	32.79
B32776 - 1100 - 12	1100	14.5	12	8.1	12	11.62	49.39
B32776 - 1100 - 14	1100	17	14	6.8	14	12.6	56.7
B32776 - 1100 - 16	1100	19	16	6	15	14.03	67.32
B32776 2p- 450 - 10	450	8	10	10.9	24	4.725	11.58
B32776 2p - 700 - 5	700	6.5	5	15.3	23	4.41	10.8
B32776 2p - 1100 - 3	1100	7	3	16	24	5.67	15.59
B32776 2p - 1100 - 5	1100	10.5	5	9.8	33	6.93	25.29

A.8. AC LCL filter capacitors

In Table A.10 a list of EPCOS capacitors can be found, which have been used for the LCL filter design.

Table A.10: Available AC capacitors for the designs.

AC capacitors	$V_{c,max}$ [V]	$I_{c,rms,max}$ [A]	C [µF]	ESR [mΩ]	ESL [nH]	A_c [cm^2]	V_c [cm^3]
B32796 - 250 - 8	250	8	8	9	21	9.96	14.94
B32796 - 250 - 22	250	15	22	3.2	30	8.4	33.18
B32796 - 250 - 40	250	21	40	2.3	33	12.6	56.7
B32796 - 300 - 5.6	300	7	5.6	12	21	9.96	14.94
B32796 - 300 - 16	300	14	16	3.9	30	8.4	33.18
B32796 - 300 - 20	300	15	20	3.1	30	11.76	43.512
B32796 - 300 - 30	300	19	30	2.2	33	12.6	56.7
B32796 - 400 - 2.7	400	7	2.7	15	21	9.96	14.94
B32796 - 400 - 7.5	400	11	7.5	5.5	30	8.4	33.18
B32796 - 400 - 1	400	14	10	4.5	30	11.76	43.512
B32796 - 400 - 13	400	17	13	3.5	33	12.6	56.7
B32796 - 400 - 16	400	18	16	3.5	33	14.03	67.32

B

Inductor design

In this chapter the verification of the inductor design is performed. The free software FEMM 4.2 is used in order to model the behavior of the inductor. The E65 core, being the most selected core in the whole thesis, is selected for the analysis, see Figure B.1.

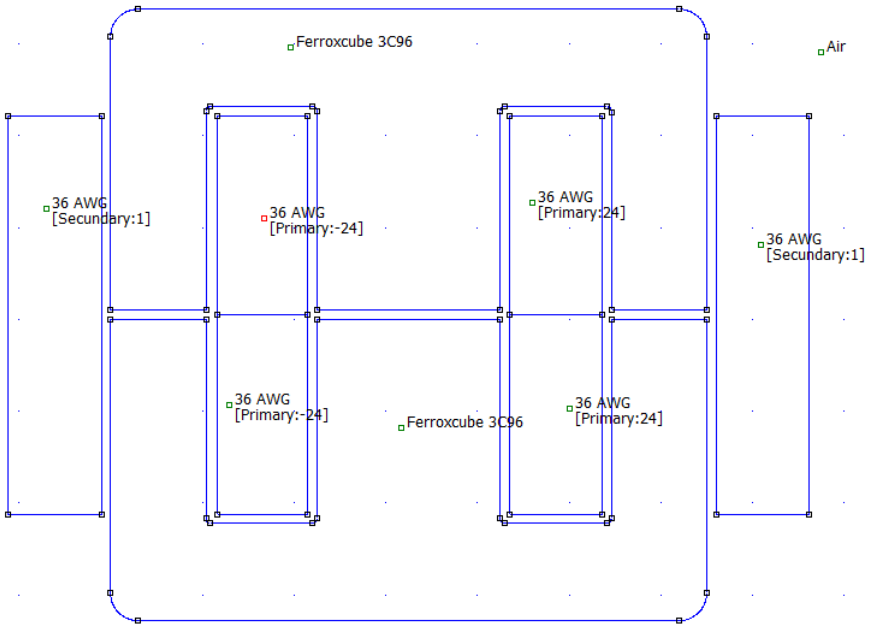


Figure B.1: Input current ripple versus input voltage and power for different levels of interleaving.

This design allows for multiple inductor configurations without having to modify the drawing. In case of a single coil inductor, the outer coils area is set to have zero current flowing, so no flux is generated. The fact that the permeability of copper is the same as the air allows for no modification at all. The inner inductor can be configured by setting the rest of the characteristics between the four areas, two at each side of the center leg.

In case of a two inductor configuration, two configurations are possible. By using the inner rectangles, two inductors in the center leg can be configured, one on top of each other. If the inductors are to be wounded in the outer legs, both rectangles at each side are used as returning zones for the copper of the coils in the outer legs.

B.1. One coil inductor design validation

The inductor for the three phases Interleaved Boost Converter (IBC) operating at 50Hz will be modeled. The chacteristics of the power inductor or this converter are shown in Table 5.1 on page 5.1, and listed again for the sake of completeness:

- Inductance: 0.874 mH
- Core: E65
- Turns: 45
- Strands: 112
- Air gap: 0.786 mm
- B_{max} = 0.418 T

The results of the Finite Element Method analysis are shown in B.2.

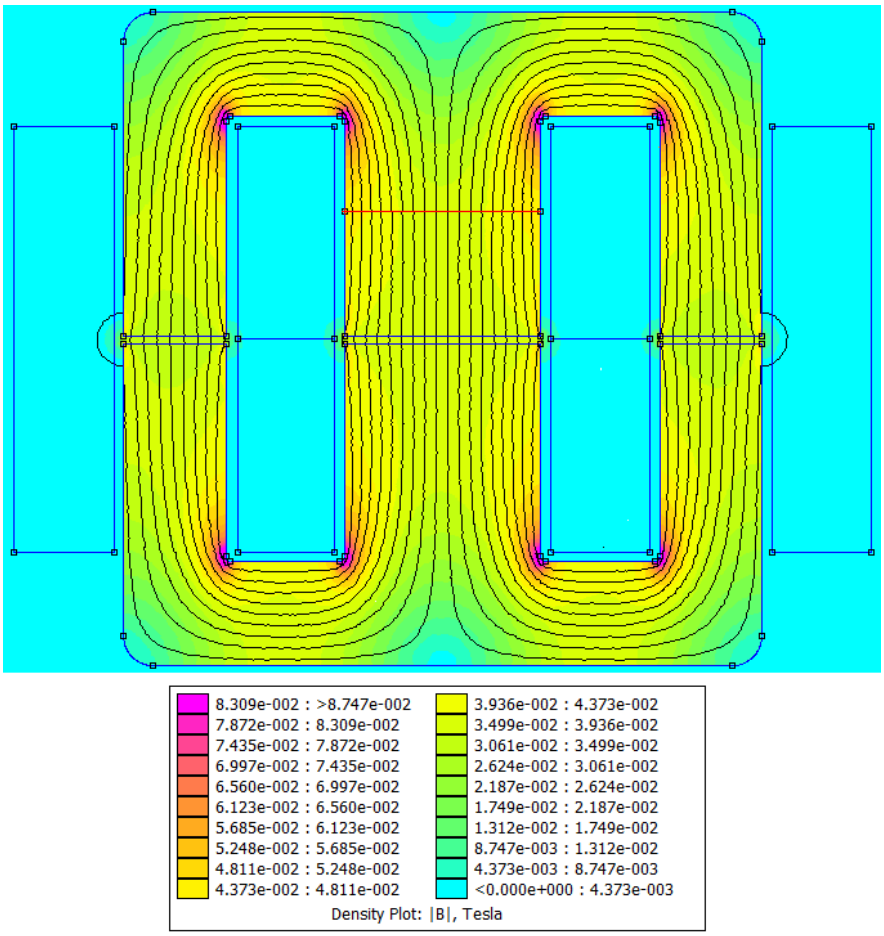


Figure B.2: FEM results of the 3 phases IBC inductor

The resulting inductance is 0.990 mH, quite close to the desired 0.874 mH. The flux density is kept around 420mT in average, as shown by the legend, except in the inner corners where it goes up to 800mT due to flux concentration. The integral line, shown in red, shows an average of 420mT in the middle of the center leg. Other zones may have a higher average but it is around the established 400mT of saturation, which is well under the 450/500mT specified by the core manufacturer.

B.2. Coupled inductors coupling factor

The two coils seen in Figure B.1 are used for this purpose. FEMM shows the flux linkage in the secondary coil due to the current in the primary circuitThe coupling factor is independent on the number of turns and strands because both coils are considered to be equal; it is just a matter of core geometry. If a current of one ampere is made to circulate in the primary coil, the relation can be obtained directly.:

$$k = \frac{M}{L} = \frac{L_s}{L_p} = \frac{\frac{\lambda_s}{I}}{L_p} \tag{B.1}$$

The results show a coupling factor of 0.35 (-0.35 in case of reverse coupling) when using the outter legs for winding the coil while the coupling factor when using the inner legs with two completely separate windings is 0.87 and -0.87. With this results is made clear that coupling factors of 0.35 and 0.9 are achievable with the current core and can be used in order to model the Coupled Inductors Interleaved Boost Converter (CIIBC) converter. A higher coupling factor could be achieved if the turns of both windings where interleaved, but it is not considered in this thesis.

B.3. Coupled inductor design validation

The coupled inductor design of the 4 phases CIIBC is also checked. The main characteristics are:

- Inductance: 13.1 mH
- Core: E65
- Turns: 29
- Strands: 74
- Air gap: 0.02 mm
- B_{max} = 0.120 T

The results show a final inductance of 14.01mH, which is quite close to the desired inductance. On the other hand, the magnetic flux density in the core is not uniform at all due to the reverse configuration. Figure B.3 shows the flux density inside the E65 core. While in the center leg the flux density is zero or close to zero, in the outter legs the maximum flux density is arround 0.133 Tesla, a value which is slightly superior to the calculated value. Therefore, the derived equivalent model used for the coupled inductors is accurate enough at least to compare the different topologies accurately and perform a preliminary design of the different magnetic elements.

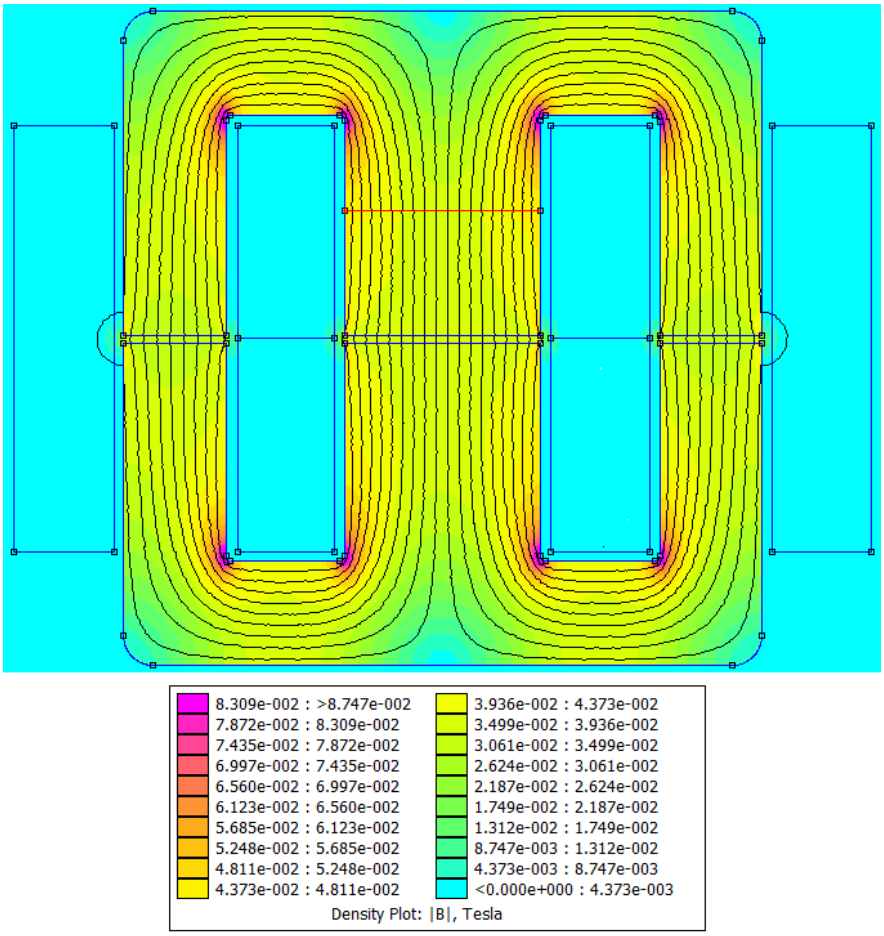


Figure B.3: FEM results of the 4 phases CIIBC inductor

C

Mosfet losses

In this chapter the verification of the mosfet losses is performed. The KIT8020-CRD-8FF1217P-1CREE MOSFET Evaluation Kit from CREE is used in order to evaluate the losses of the switch. The switch used in the kit is the C2M0080120D, see Appendix A. The test setup circuit used is shown in Figure C.1.

A input capacitor is used at the DC input in order to reduce ringing, which is quite high in the development board. Due to power supply limitations, only 70 Vdc have been applied to the two legs system. The gating signals have 50 kHz frequency and 50% duty cycle, and the load is a 25 Ωpower resistor with low inductance. This results in a turn on and turn of currents of 2.8 A and an average current of 1.4 A. The total dissipated power in the resistor is therefore 98W, a really low power compared to the SiC switch capabilities.

There are several differences between the actual setup and the datasheet:

1. A 2.5 Ωgate resistor has been considered throughout the report. This is a very low value which leads to high speed switchings and therefore lower losses, but results in high dV/dt and ringing. The evaluation board has an asymmetrical gate resistor, 10 Ωat turn on and 5 Ωat turn off. This results in higher switching losses than the ones predicted.
2. The test is performed at low switching voltage, where the proportionality applied with respect to V_{DS} to the E_{on} and E_{off} switching energies is less accurate. Therefore, higher voltages should have been used in the test.

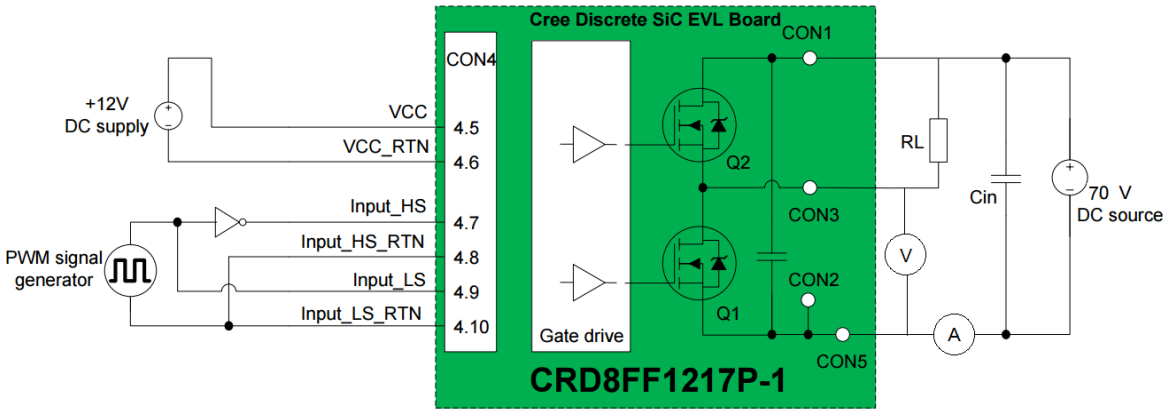
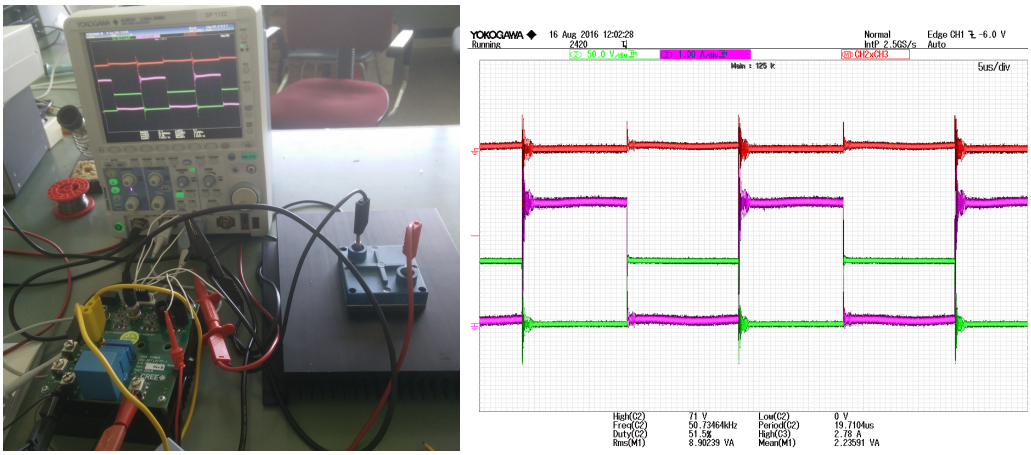


Figure C.1: Test setup of the evaluation board.

3. The test is different from the one performed by the manufacturer to create the Datasheet. The test on Figure C.1 is different from the clamped inductive switching test circuit, resulting in a different environment.

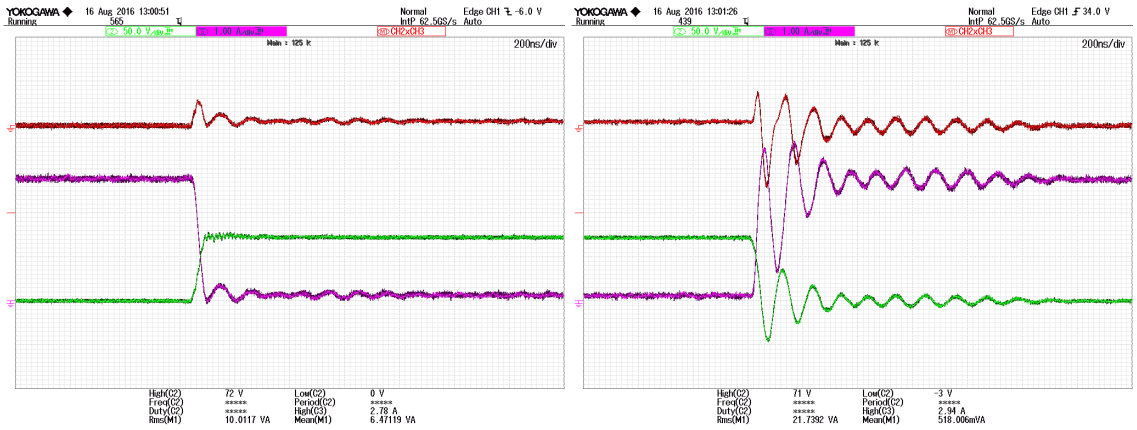
The method used to obtain the losses is also not the most appropriate one; power meters should be used but due to the low power setup, small inaccuracies of the test equipment result in high differences in losses. Therefore, the built-in mathematical functions of the oscilloscope have been used, and the product of the voltage across the switch and the current through it considered to be the losses, see Figure C.2.



(a) Test setup (b) Test waveforms

Figure C.2: Test overview

The losses and the board are seen in Figure C.3. The oscilloscope shows RMS losses of 9 W, which is a very high value. The mean losses, which take into account positive and negative values of the V I product, are 2.24 W. The analytical expressions used during the thesis, for a 70 Vdc V_{DS}, a mean current of 1.4A, a RMS current of 2.12A, switching currents of 2.8 A, 50000 kHz switching frequency and junction temperature of 60 degrees result in losses of 0.8 W, which is very different from the obtained results. The turn on and turn of waveforms are shown in Figure C.3.



(a) Turn on (b) Turn off

Figure C.3: Switching waveforms

D

Current waveforms CIIBC

The equations that describe how the coupling of the inductors affect the equivalent inductance and thus, the ripple in the inductor, will be described only for Continuous Inductor Conduction Mode (CICM). The equations for Discontinuous Inductor Conduction Mode (DICM) have been obtained from [3]. The voltage drop on the inductor depends on the self-inductance L and the mutual inductance M, and the voltage produced by them is directly proportional to the change rate of the current in both inductors:

$$\begin{aligned} V_1 &= L\frac{di_1}{dt} + M\frac{di_2}{dt} \\ V_2 &= M\frac{di_1}{dt} + L\frac{di_2}{dt} \end{aligned} \tag{D.1}$$

Although the inductances of the inductors could be considered to be different, in this case they are taken to have the same value as the construction of the different phases of the interleaved converter should be as similar as possible. Moreover, this simplifies the following development of the final equations. The rearrangement of this equations lead to the following:

$$\begin{aligned} \frac{di_2}{dt} &= \frac{V_2}{L} - \frac{M}{L}\frac{di_1}{dt} \\ \frac{di_1}{dt} &= \frac{V_1}{L} - \frac{M}{L}\frac{di_2}{dt} \end{aligned} \tag{D.2}$$

$\frac{M}{L}$ is the coupling factor (k) of the pair of inductors. Depending on the construction it can take a value from minus one to one, if it is reverse coupled or direct coupled, respectively. In the case the inductors are not coupled at all, the value of (k) is then zero. If equation D.1 is replaced into D.2, the following equations result:

$$\begin{aligned} V_1 - \frac{M}{L}V_2 &= \left(L - \frac{M^2}{L}\right)\frac{di_1}{dt} \\ V_2 - \frac{M}{L}V_1 &= \left(L - \frac{M^2}{L}\right)\frac{di_2}{dt} \end{aligned} \tag{D.3}$$

The equivalent inductance can have three different values, depending on the state of the switches. Inductor 1 will be considered in the following derivations. In the first case, the switch connected with inductor one is in the ON state, while the switch connected to inductor 2 is in the OFF state. Thereby,

$V_1 = V_i$ and $V_2 = V_i - Vo$. Taking into account that the voltage boost is established by the duty cycle equation ($V_o = \frac{V_i}{1-D}$), the following equation is derived:

$$V_2 = -V_1 \frac{D}{1-D} \tag{D.4}$$

If equation D.4 is substituted in the first equation of D.3, the resulting equation is:

$$V_1 = \frac{L - \frac{M^2}{L}}{1 + \frac{M}{L}\frac{D}{1-D}} \frac{di_1}{dt} \tag{D.5}$$

This equation can be modified in order to show the equivalent inductance in a more representative way. If the factor $k = \frac{M}{L}$ is introduced, the resulting voltage equation is:

$$V_1 = \left(\frac{1-k^2}{1+k\frac{D}{1-D}}\right) L \frac{di_1}{dt} \tag{D.6}$$

Where the equivalent inductance value is clearly shown. The equivalent inductance is finally:

$$L_{eq1} = \left(\frac{1-k^2}{1+k\frac{D}{1-D}}\right) L \tag{D.7}$$

In the second case, the switch connected directly to inductor 1 is in the OFF state while the switch connected in the inductor 2 is in the ON state. Thus, $V_1 = V_i - Vo$ and $V_2 = V_i$. If the same procedure is applied, the equivalent inductance in this state is:

$$L_{eq2} = \left(\frac{1-k^2}{1+k\frac{1-D}{D}}\right) L \tag{D.8}$$

Finally, in the last state both the switches are either in the ON state or the OFF state, making the two inductor voltages the same $V_1 = V_2$. If this equivalence is introduced into equation D.3, the equivalent inductance in this state is:

$$L_{eq0} = (1+k)\, L \tag{D.9}$$

The equivalent inductance in this state is the same for both the inductors, as they have the same voltage applied.

In order to calculate the input ripple in the Coupled Inductors Interleaved Boost Converter (CIIBC), the four phases interleaved boost converter with couple inductors will be analyzed. Depending on the duty cycle of the converter, 4 different sates must be considered, as the switch states differ between them, and thus the equivalent inductance in the inductors. The working conditions of the switches for different duty cycles are represented in the next picture:

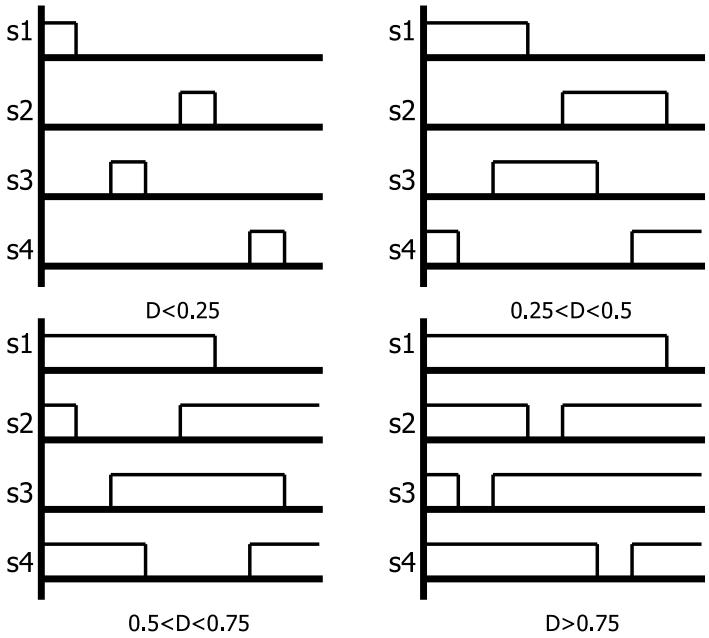


Figure D.1: Switching patterns for different values of duty cycle in the CIIBC.

The operation of the CIIBC is also seen in figure D.1. Compared to the Interleaved Boost Converter (IBC), the switching pattern is delayed by $\frac{2\pi}{2}$ in the second inductor of each couple, while the first inductor of each pair is delayed by $\frac{2\pi}{N}$, being N the total number of phases, which must be an even number.

D>0.25

When the duty cycle is smaller than 0.25, the converter operates with the following waveforms:

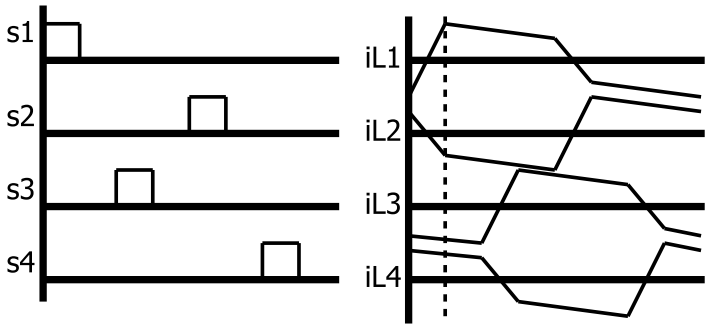


Figure D.2: Switching patterns and inductor current ripple in the CIIBC.

The total ripple is the sum of the slopes of the different inductors multiplied by the time. The rate of current increment in every inductor is the voltage over the equivalent inductance ($S = \frac{V}{Leq}$), which depends on the sate of the couple of switches which inductors are coupled:

$$S_t = S_1 + S_2 + S_3 + S_4 = \frac{V_i}{L_{eq1}} + \frac{V_i - V_o}{L_{eq2}} + \frac{V_i - V_o}{_{eq0}} + \frac{V_i - V_o}{L_{eq0}} \tag{D.10}$$

By developing the different slopes the following equations are obtained:

$$
\begin{aligned}
S_1 &= \frac{V_i}{L}\left(\frac{1+k\frac{D}{1-D}}{1-k^2}\right) \\
S_2 &= \frac{V_i - V_o}{L}\left(\frac{1+k\frac{1-D}{D}}{1-k^2}\right) = \frac{-V_i}{L}\left(\frac{k+\frac{D}{1-D}}{1-k^2}\right) \\
S_3 &= \frac{V_i - V_o}{L}\left(\frac{1}{1+k}\right) = \frac{V_i}{L}\left(\frac{\frac{D}{1-D}}{1+k}\right) \\
S_4 &= \frac{V_i - V_o}{L}\left(\frac{1}{1+k}\right) = \frac{V_i}{L}\left(\frac{\frac{D}{1-D}}{1+k}\right)
\end{aligned}
\tag{D.11}
$$

The peak to peak to peak current ripple can finally be defined as:

$$\Delta I_{in} = S_t D T_s \tag{D.12}$$

Where δI_{in} is the peak to peak current ripple at the input, S_t the total sum of the slopes of the current in the different inductors, D is the operating duty cycle and T_s the switching period.

If the different slopes derived in D.11 are added, and substituted into equation D.12, the total input current ripple is:

$$\Delta I_{in} = \frac{V_i T}{L}(D)\left(\frac{1-4D}{1-D}\right)\left(\frac{1}{k+1}\right) \tag{D.13}$$

0.25<D<0.5

When the duty cycle is between 0.25 and 0.5, the converter operates with the following waveforms:

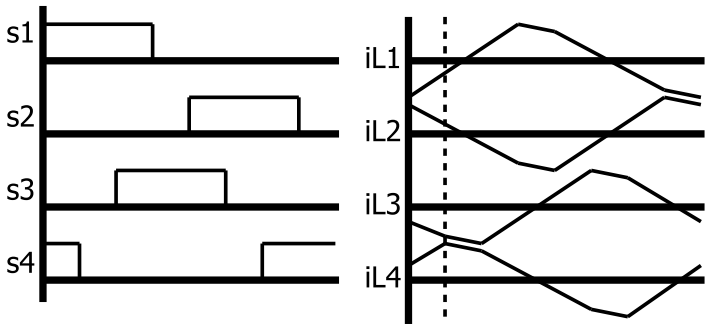


Figure D.3: Switching patterns and inductor current ripple in the CIIBC.

The total ripple is the sum of the slopes of the different inductors multiplied by the time. The rate of current increment in every inductor is the voltage over the equivalent inductance ($S = \frac{V}{Leq}$), which depends on the sate of the couple of switches which inductors are coupled:

$$S_t = S_1 + S_2 + S_3 + S_4 = \frac{V_i}{L_{eq1}} + \frac{V_i - V_o}{L_{eq2}} + \frac{V_i - V_o}{L_{eq2}} + \frac{V_i}{L_{eq1}} \tag{D.14}$$

By developing the different slopes the following equations are obtained:

$$
\begin{aligned}
S_1 &= \frac{V_i}{L}\left(\frac{1+k\frac{D}{1-D}}{1-k^2}\right) \\
S_2 &= \frac{V_i - V_o}{L}\left(\frac{1+k\frac{1-D}{D}}{1-k^2}\right) = \frac{-V_i}{L}\left(\frac{k+\frac{D}{1-D}}{1-k^2}\right) \\
S_3 &= \frac{V_i - V_o}{L}\left(\frac{1+k\frac{1-D}{D}}{1-k^2}\right) = \frac{-V_i}{L}\left(\frac{k+\frac{D}{1-D}}{1-k^2}\right) \\
S_4 &= \frac{V_i}{L}\left(\frac{1+k\frac{D}{1-D}}{1-k^2}\right)
\end{aligned}
\tag{D.15}
$$

The peak to peak to peak current ripple can finally be defined as:

$$
\Delta I_{in} = S_t(D-\frac{1}{4})T_s = \frac{V_i T}{L}(D-\frac{1}{4})\left(\frac{2-4D}{1-D}\right)\left(\frac{1}{k+1}\right) \tag{D.16}
$$

0.5<D<0.75

The same procedure applies when the duty cycle is between 0.5 and 0.75. The equations to use are:

$$
\begin{aligned}
S_1 &= \frac{V_i}{L}\left(\frac{1}{1+k})\right) \\
S_2 &= \frac{V_i}{L}\left(\frac{1}{1+k})\right) \\
S_3 &= \frac{V_i - V_o}{L}\left(\frac{1+k\frac{1-D}{D}}{1-k^2}\right) = \frac{-V_i}{L}\left(\frac{k+\frac{D}{1-D}}{1-k^2}\right) \\
S_4 &= \frac{V_i}{L}\left(\frac{1+k\frac{D}{1-D}}{1-k^2}\right)
\end{aligned}
\tag{D.17}
$$

Finally, the input current ripple is:

$$
\Delta I_{in} = S_t(D-\frac{2}{4})T_s = \frac{V_i T_s}{L}(D-\frac{2}{4})\left(\frac{3-4D}{1-D}\right)\left(\frac{1}{k+1}\right) \tag{D.18}
$$

0.75<D

The same procedure applies when the duty cycle is between 0.5 and 0.75. The equations to use are:

$$
\begin{aligned}
S_1 &= \frac{V_i}{L}\left(\frac{1}{1+k})\right) \\
S_2 &= \frac{V_i}{L}\left(\frac{1}{1+k})\right) \\
S_3 &= \frac{V_i}{L}\left(\frac{1}{1+k})\right) \\
S_4 &= \frac{V_i}{L}\left(\frac{1}{1+k})\right)
\end{aligned}
\tag{D.19}
$$

Finally, the input current ripple is:

$$\Delta I_{in} = S_t(D - \frac{3}{4})T_s = \frac{V_i T_s}{L}(D - \frac{3}{4})\,(4)\left(\frac{1}{k+1}\right) \tag{D.20}$$

0<D<1

Those equations, which change according to the duty cycle, are the same as Equation 5.4 from the IBC section, when $k = 0$. Thus, the same equation can be used, adding the term $\frac{1}{1+k}$ which is the change introduced by inductance coupling:

$$L = \frac{V_{out} \cdot N}{f_{sw} \cdot I_{pp}} \cdot \left(\frac{floor(D \cdot N) + 1}{N} - D\right) \cdot \left(D - \frac{floor(D \cdot N)}{N}\right)\left(\frac{1}{k+1}\right) \tag{D.21}$$

E

Grid converter waveforms

E.1. Two Level Converter

In this chapter some of the most important waveforms related to the Two Level Converter (2LC) are shown. In Figure E.1 the gate signals of the Space Vector Pulse-Width Modulation (SVPWM) are represented, while the Near State Pulse-Width Modulation (NSPWM) gate signals can be found in Figure E.2

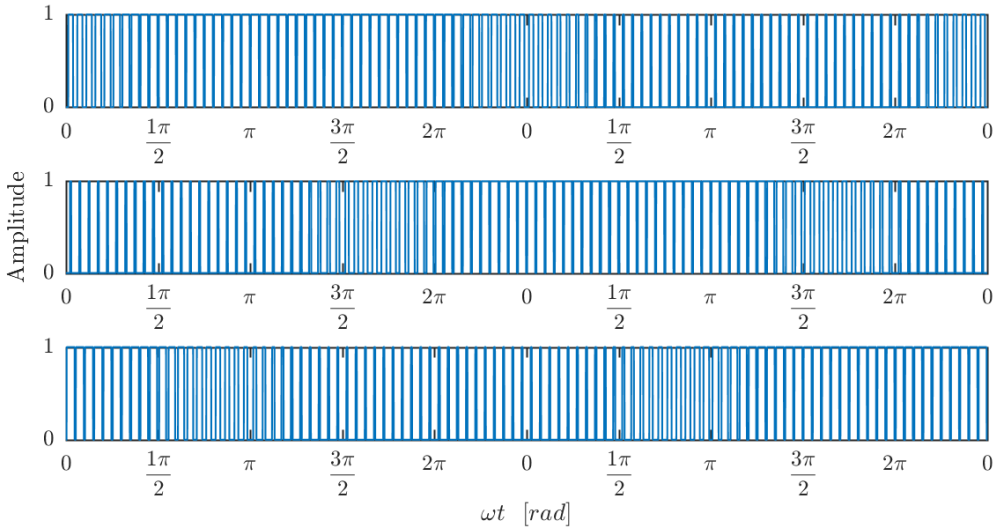


Figure E.1: Gate signals of the upper switches of the 2LC in SVPWM, $Fsw = 4kHz$

In the case of NSPWM, the switches are clamped to one voltage for 60 degrees, and therefore, the switching losses are reduced considerably. The bottom switches signals are complementary to the ones shown in these figures.

It is also possible to plot the switching vectors used in each case. Figure E.3 shows the active zones for a whole cycle for both modes of operation, and the switching vectors used in each zone.

Please notice the vectors used. While in SVPWM in every switching period there are two voltage vectors used together with the two zero voltage vectors, in NSPWM only voltage vectors are used and no zero voltage vectors take place. Another important fact is the difference between sectors in

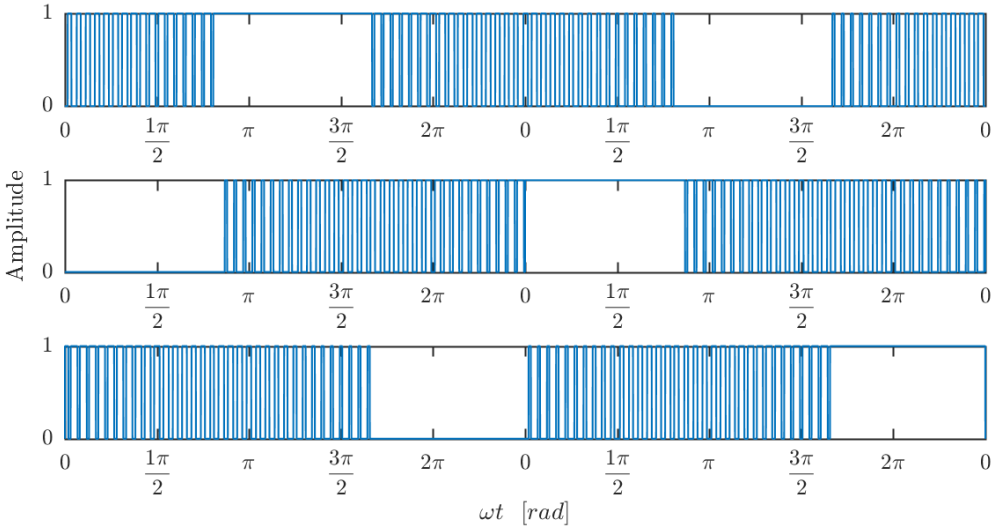
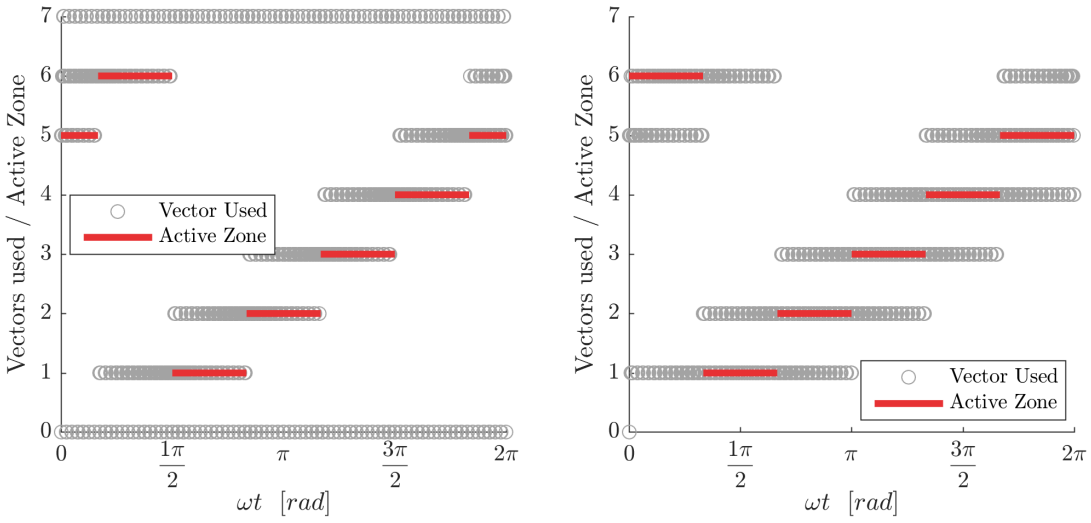


Figure E.2: Gate signals of the upper switches of the 2LC, $Fsw = 4kHz$

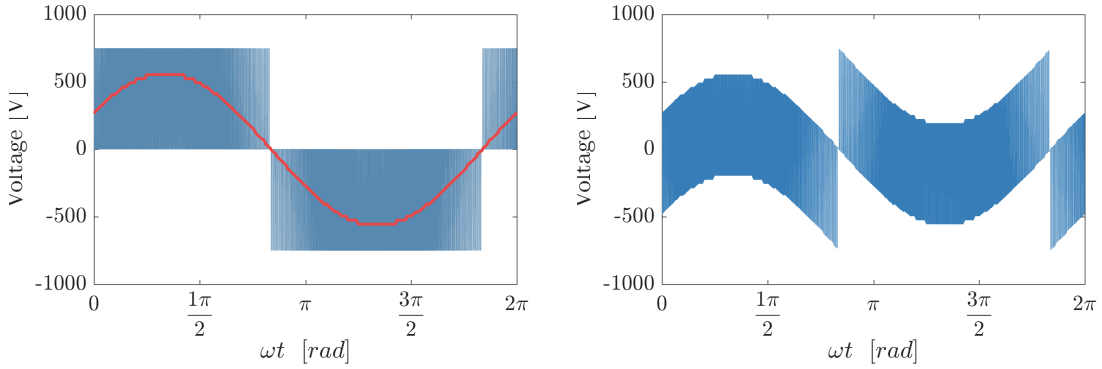


(a) SVPWM (b) NSPWM

Figure E.3: Used vectors of the 2LC using SVPWM and NSPWM, $Fsw = 4kHz$

the whole cycle, as NSPWM uses a modified sector separation as explained in this thesis.

The line voltage of the 2LC and the voltage ripple with respect to the filtered voltage are shown in E.4, where the used modulation technique is SVPWM. The same plots are not shown for NSPWM because differences are not visible.



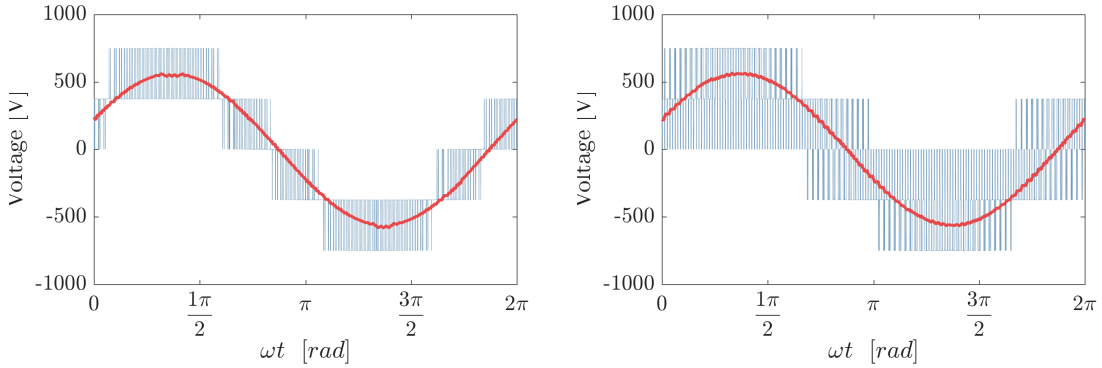
(a) Output line voltage (b) Output voltage ripple

Figure E.4: Voltage waveforms of the 2LC using SVPWM. $Fsw = 4kHz$

The working principle of two level converters is seen in E.4. While in E.4(a) the two level output and the bipolar switching is seen, in E.4(b) the large amount of voltage ripple due to the difference of voltage between the grid and the DC bus is seen.

E.2. Three Level Neutral Point Clamped Converter

In this section some of the most important waveforms related to the Three Level Neutral Point Clamped Converter (3LNPC²) are exposed. These waveforms are also valid for the Three Level T-Type Converter (3LT²C) as they are both three level topologies. In Figure E.5 the output line voltages of one phase of the 3LNPC² is shown.

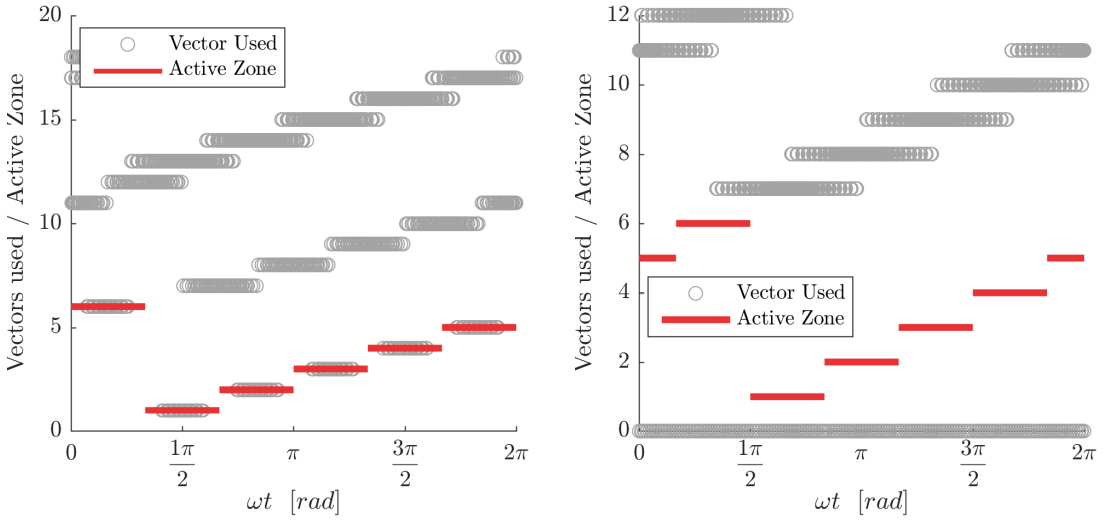


(a) SVPWM (b) 2M1ZVPWM

Figure E.5: Output line voltages of the 3LNPC² with both modulation techniques. $Fsw = 4kHz$

In the case of 2M1ZVPWM, the zero vectors are applied during the whole modulation waveform of the converter. On the other hand, SVPWM uses voltage vectors with higher amplitude instead of the zero vectors, resulting in lower voltage ripple at the LCL filter. It is also possible to plot the switching vectors used in each case. Figure E.6 shows the active zones for a whole cycle for both

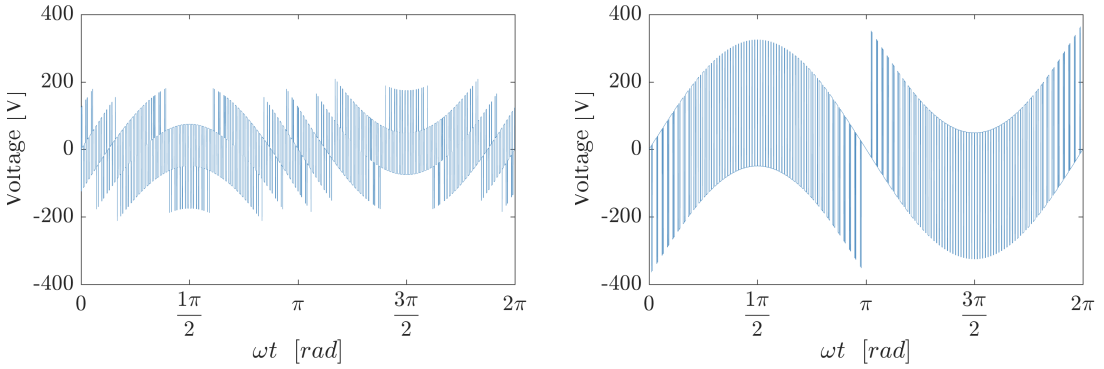
modes of operation, and the switching vectors used in each zone.



(a) SVPWM (b) 2M1ZVPWM

Figure E.6: Used vectors of the 3LNPC² using SVPWM and 2M1ZVPWM. $Fsw = 4kHz$

Please notice the vectors used. While in SVPWM almost all the vectors are used, in 2M1ZVPWM only medium voltage vectors and the zero vectorare used. As a consequence, the phase ripple is also increased, as shown in E.7.



(a) SVPWM (b) 2M1ZVPWM

Figure E.7: Phase voltage ripple of the 3LNPC². $Fsw = 4kHz$

F

Datasheets

CREE

V_{DS}	1200 V
$I_{D\ @\ 25^{\circ}C}$	36 A
$R_{DS(on)}$	80 mΩ

C2M0080120D

Silicon Carbide Power MOSFET
C2M™ MOSFET Technology

N-Channel Enhancement Mode

Features

- High Blocking Voltage with Low On-Resistance
- High Speed Switching with Low Capacitances
- Easy to Parallel and Simple to Drive
- Avalanche Ruggedness
- Halogen Free, RoHS Compliant

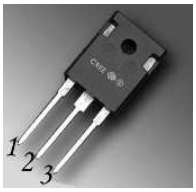
Benefits

- Higher System Efficiency
- Reduced Cooling Requirements
- Increased Power Density
- Increased System Switching Frequency

Applications

- Solar Inverters
- Switch Mode Power Supplies
- High Voltage DC/DC Converters
- Battery Chargers
- Motor Drives
- Pulsed Power applications

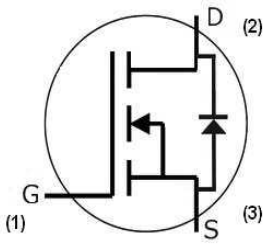
Package



TO-247-3

Halogen-Free

RoHS



Part Number	Package
C2M0080120D	TO-247-3

Maximum Ratings (T_C = 25 ˚C unless otherwise specified)

Symbol	Parameter	Value	Unit	Test Conditions	Note
V_{DSmax}	Drain - Source Voltage	1200	V	V_{GS} = 0 V, I_D = 100 µA	
V_{GSmax}	Gate - Source Voltage	-10/+25	V	Absolute maximum values	
V_{GSop}	Gate - Source Voltage	-5/+20	V	Recommended operational values	
I_D	Continuous Drain Current	36	A	V_{GS} = 20 V, T_C = 25˚C	Fig. 19
		24		V_{GS} = 20 V, T_C = 100˚C	
$I_{D(pulse)}$	Pulsed Drain Current	80	A	Pulse width t_P limited by T_{jmax}	Fig. 22
P_D	Power Dissipation	192	W	T_C=25˚C, T_J = 150 ˚C	Fig. 20
T_J , T_{stg}	Operating Junction and Storage Temperature	-55 to +150	˚C		
T_L	Solder Temperature	260	˚C	1.6mm (0.063”) from case for 10s	
M_d	Mounting Torque	1 8.8	Nm lbf-in	M3 or 6-32 screw	

CREE

Electrical Characteristics (T_C = 25˚C unless otherwise specified)

Symbol	Parameter	Min.	Typ.	Max.	Unit	Test Conditions	Note
$V_{(BR)DSS}$	Drain-Source Breakdown Voltage	1200			V	V_{GS} = 0 V, I_D = 100 µA	
$V_{GS(th)}$	Gate Threshold Voltage	2.0	2.6	4	V	V_{DS} = V_{GS}, I_D = 5 mA	Fig. 11
			2.1		V	V_{DS} = V_{GS}, I_D = 5 mA, T_J = 150ºC	
I_{DSS}	Zero Gate Voltage Drain Current		1	100	µA	V_{DS} = 1200 V, V_{GS} = 0 V	
I_{GSS}	Gate-Source Leakage Current			250	nA	V_{GS} = 20 V, V_{DS} = 0 V	
$R_{DS(on)}$	Drain-Source On-State Resistance		80	98	mΩ	V_{GS} = 20 V, I_D = 20 A	Fig. 4, 5, 6
			128			V_{GS} = 20 V, I_D = 20A, T_J = 150ºC	
g_{fs}	Transconductance		8.1		S	V_{DS}= 20 V, I_{DS}= 20 A	Fig. 7
			7.8			V_{DS}= 20 V, I_{DS}= 20 A, T_J = 150ºC	
C_{iss}	Input Capacitance		950		pF	V_{GS} = 0 V V_{DS} = 1000 V f = 1 MHz V_{AC} = 25 mV	Fig. 17, 18
C_{oss}	Output Capacitance		80				
C_{rss}	Reverse Transfer Capacitance		7.6				
E_{oss}	C_{oss} Stored Energy		45		µJ		Fig. 16
E_{AS}	Avalanche Energy, Single Pluse		1		J	I_D = 20A, V_{DD} = 50V	Fig. 29
E_{ON}	Turn-On Switching Energy		265		µJ	V_{DS} = 800 V, V_{GS} = -5/20 V, I_D = 20A, $R_{G(ext)}$ = 2.5Ω, L= 142 µH	Fig. 25
E_{OFF}	Turn Off Switching Energy		135				
$t_{d(on)}$	Turn-On Delay Time		11		ns	V_{DD} = 800 V, V_{GS} = -5/20 V I_D = 20 A, $R_{G(ext)}$ = 2.5 Ω, R_L = 40 Ω, Timing relative to V_{DS} Per IEC60747-8-4 pg 83	Fig. 27
t_r	Rise Time		20				
$t_{d(off)}$	Turn-Off Delay Time		23				
t_f	Fall Time		19				
$R_{G(int)}$	Internal Gate Resistance		4.6		Ω	f = 1 MHz, V_{AC} = 25 mV	
Q_{gs}	Gate to Source Charge		15		nC	V_{DS} = 800 V, V_{GS} = -5/20 V I_D = 20 A Per IEC60747-8-4 pg 21	Fig. 12
Q_{gd}	Gate to Drain Charge		23				
Q_g	Total Gate Charge		62				

Reverse Diode Characteristics

Symbol	Parameter	Typ.	Max.	Unit	Test Conditions	Note
V_{SD}	Diode Forward Voltage	3.3		V	V_{GS} = - 5 V, I_{SD} = 10 A	Fig. 8, 9, 10
		3.1		V	V_{GS} = - 5 V, I_{SD} = 10 A, T_J = 150 °C	
I_S	Continuous Diode Forward Current		36	A	T_C = 25˚C	Note 1
t_{rr}	Reverse Recover time	32		ns	V_{GS} = - 5 V, I_{SD} = 20 A, V_R = 800 V dif/dt = 2400 A/µs	Note 1
Q_{rr}	Reverse Recovery Charge	192		nC		
I_{rrm}	Peak Reverse Recovery Current	10		A		

Note (1): When using SiC Body Diode the maximum recommended V_{GS} = -5V

Thermal Characteristics

Symbol	Parameter	Typ.	Max.	Unit	Test Conditions	Note
$R_{\theta JC}$	Thermal Resistance from Junction to Case	0.60	0.65	°C/W		Fig. 21
$R_{\theta JA}$	Thermal Resistance From Junction to Ambient		40			

Typical Performance

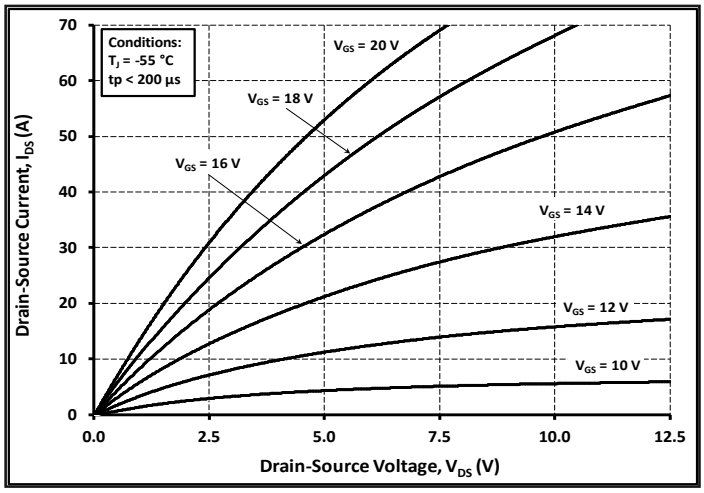


Figure 1. Output Characteristics T_J = -55 ºC

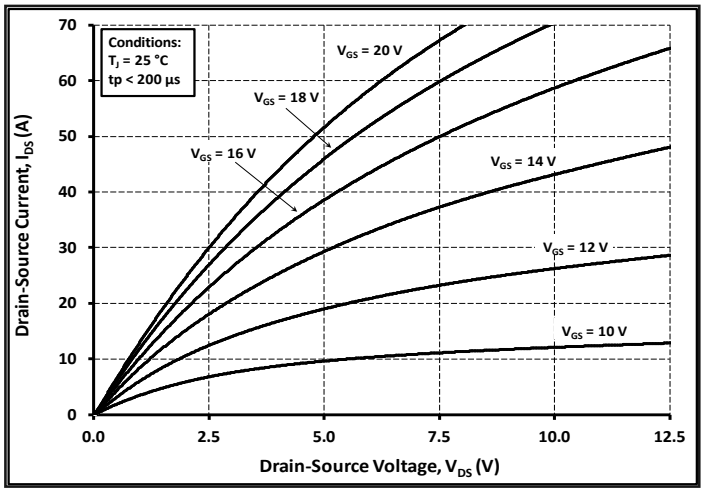


Figure 2. Output Characteristics T_J = 25 ºC

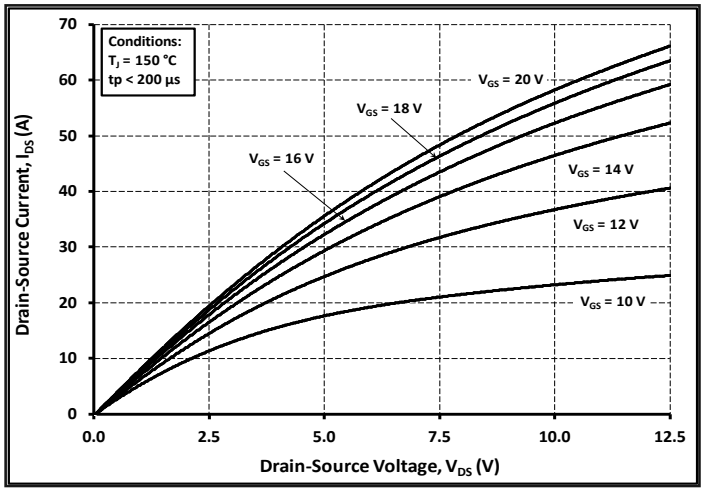


Figure 3. Output Characteristics T_J = 150 ºC

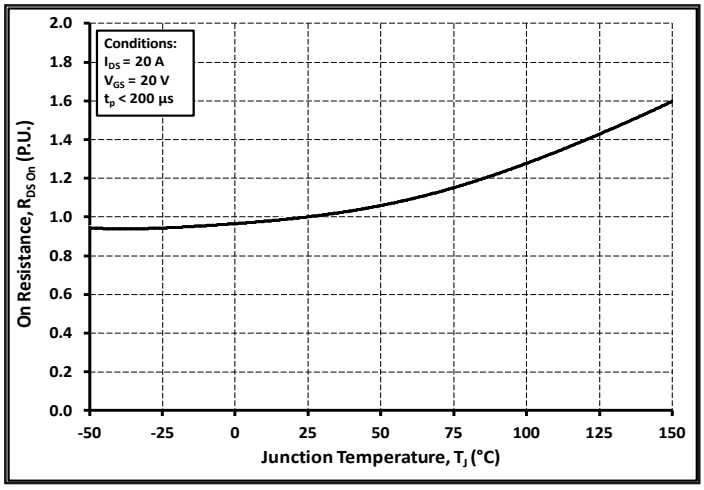


Figure 4. Normalized On-Resistance vs. Temperature

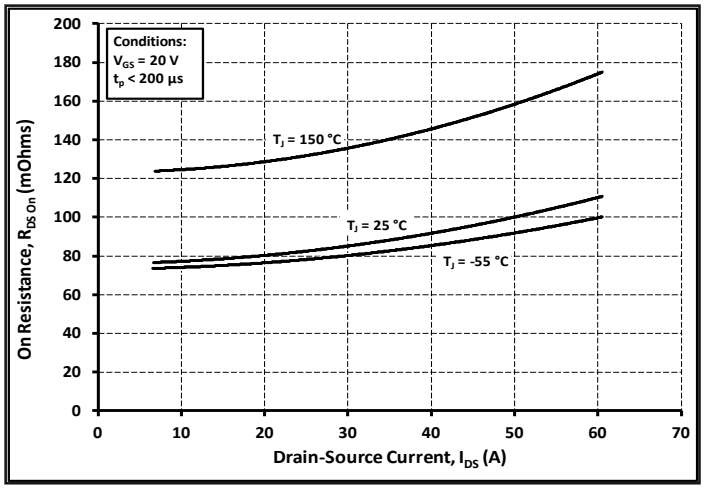


Figure 5. On-Resistance vs. Drain Current
For Various Temperatures

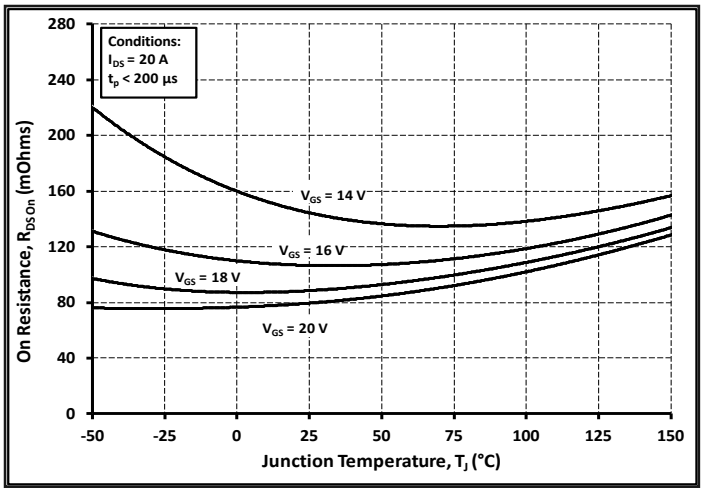


Figure 6. On-Resistance vs. Temperature
For Various Gate Voltage

Typical Performance

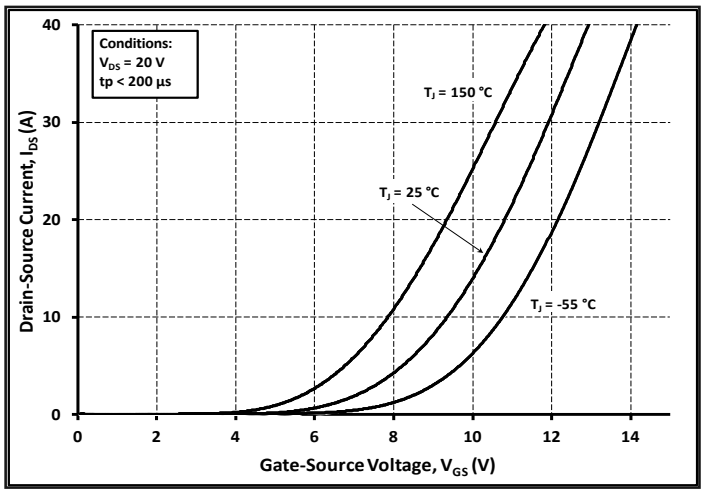


Figure 7. Transfer Characteristic for Various Junction Temperatures

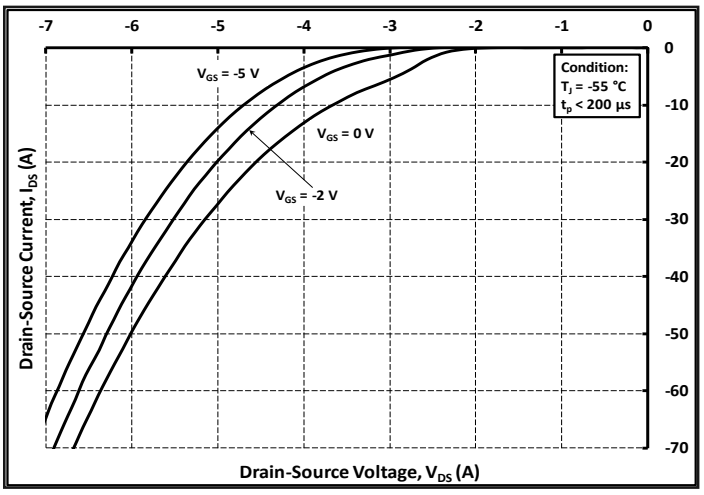


Figure 8. Body Diode Characteristic at -55 °C

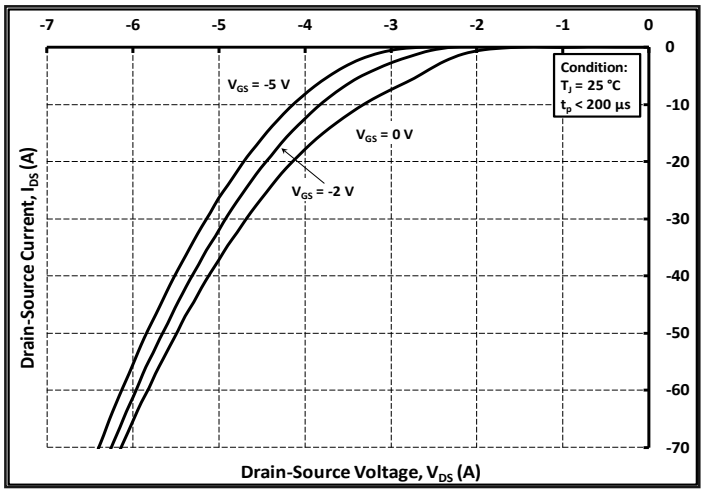


Figure 9. Body Diode Characteristic at 25 °C

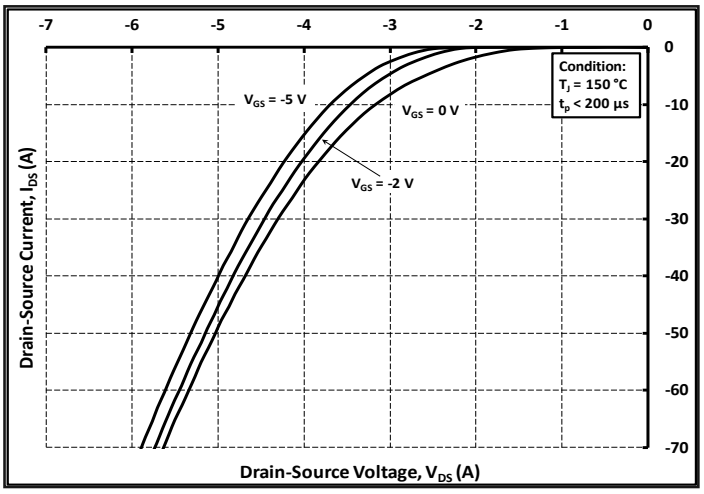


Figure 10. Body Diode Characteristic at 150 °C

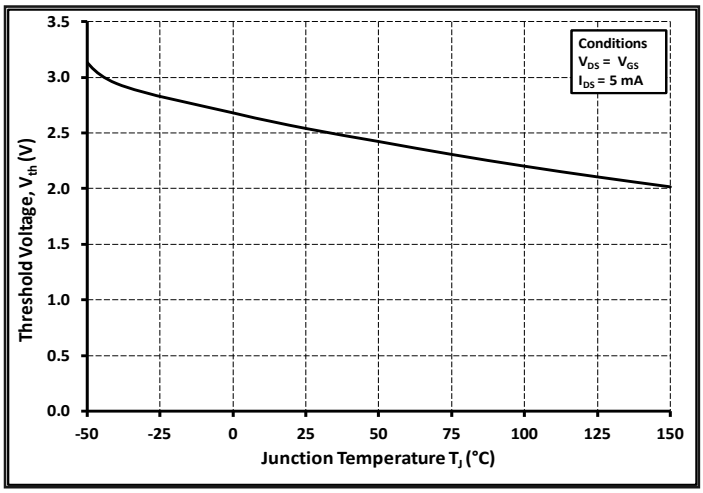


Figure 11. Threshold Voltage vs. Temperature

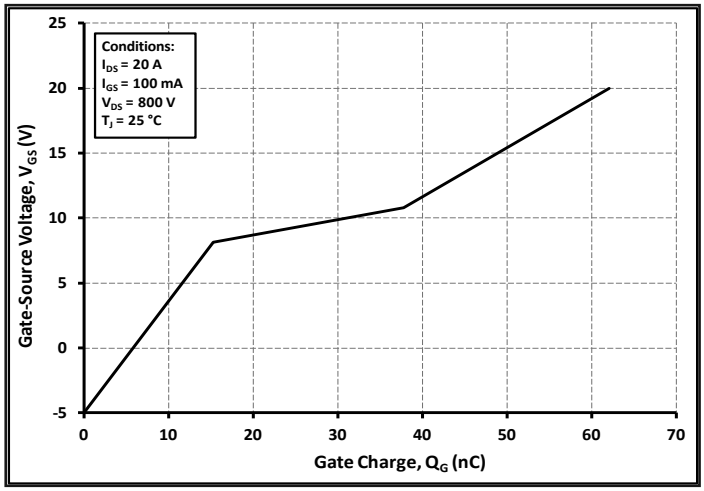


Figure 12. Gate Charge Characteristics

Typical Performance

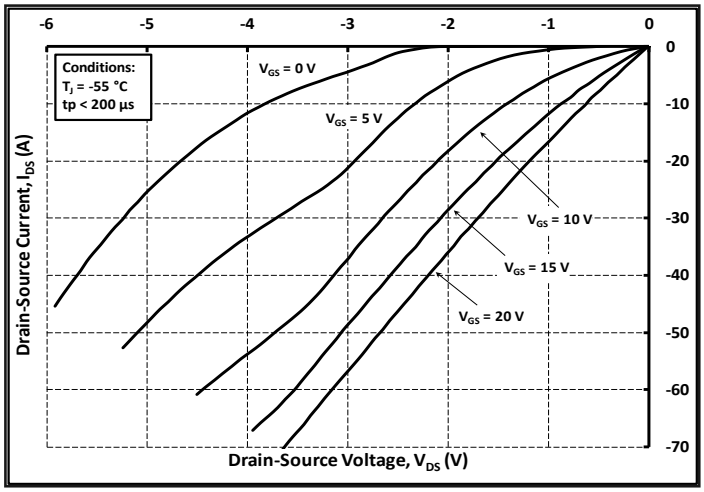


Figure 13. 3rd Quadrant Characteristic at -55 ºC

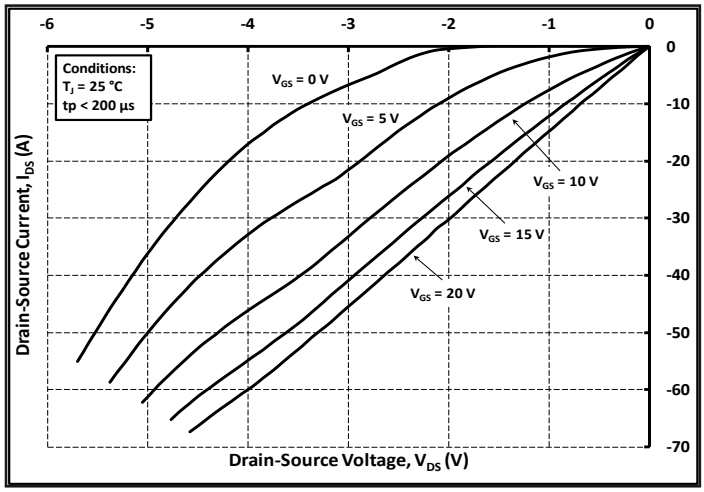


Figure 14. 3rd Quadrant Characteristic at 25 ºC

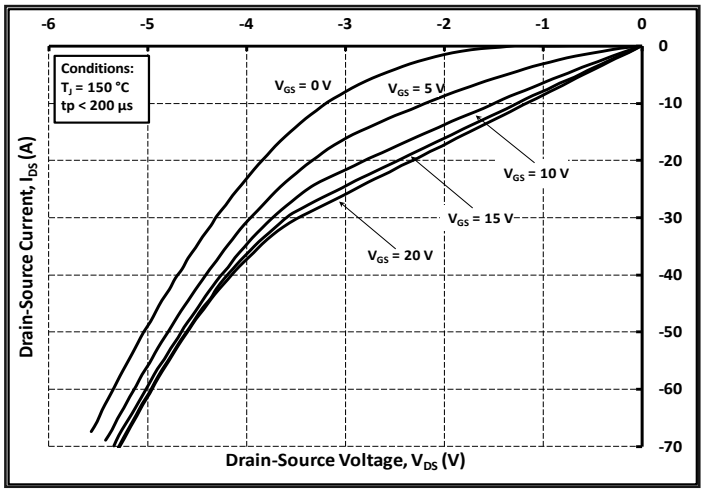


Figure 15. 3rd Quadrant Characteristic at 150 ºC

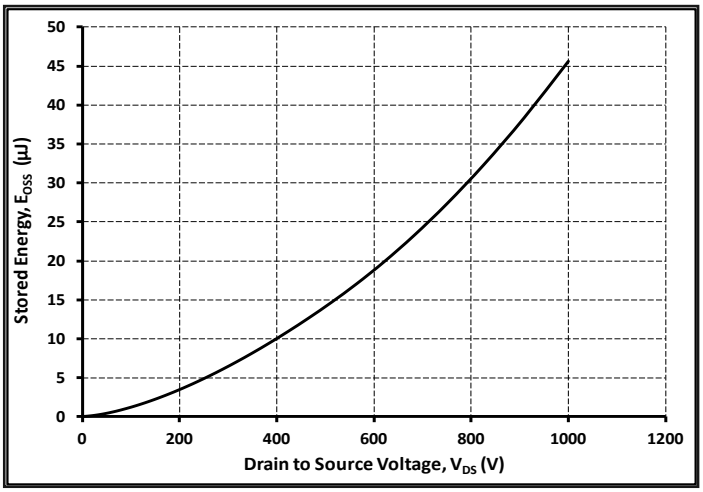


Figure 16. Output Capacitor Stored Energy

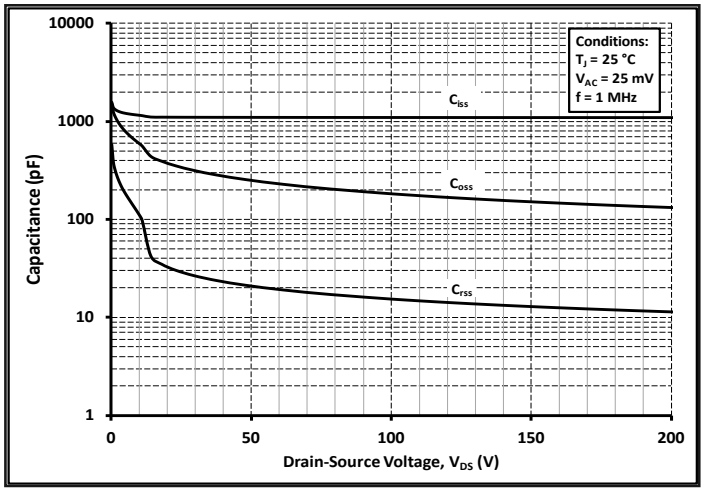


Figure 17. Capacitances vs. Drain-Source Voltage (0 - 200V)

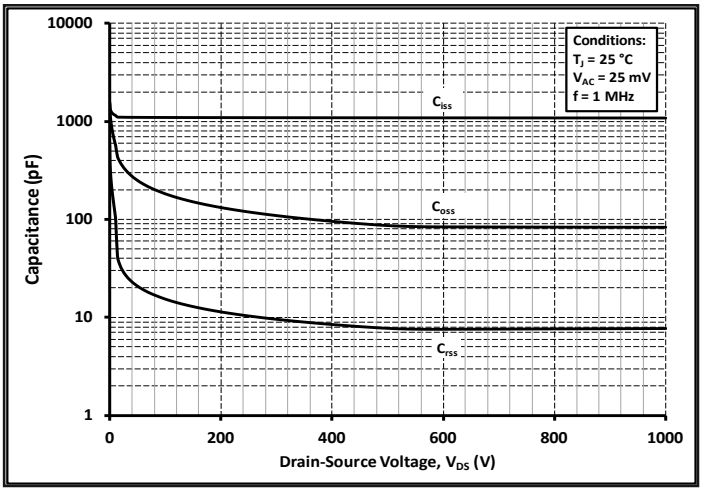


Figure 18. Capacitances vs. Drain-Source Voltage (0 - 1000V)

Typical Performance

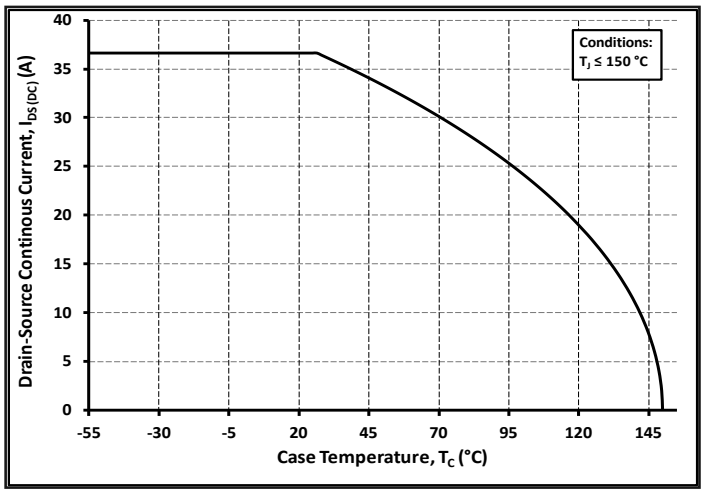


Figure 19. Continuous Drain Current Derating vs. Case Temperature

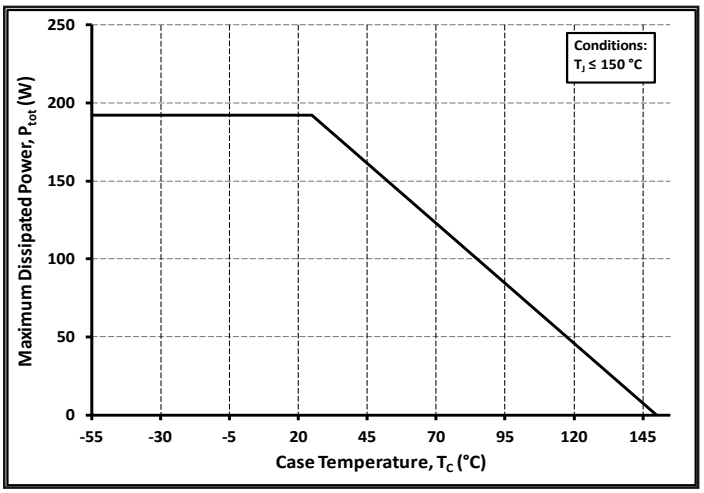


Figure 20. Maximum Power Dissipation Derating vs. Case Temperature

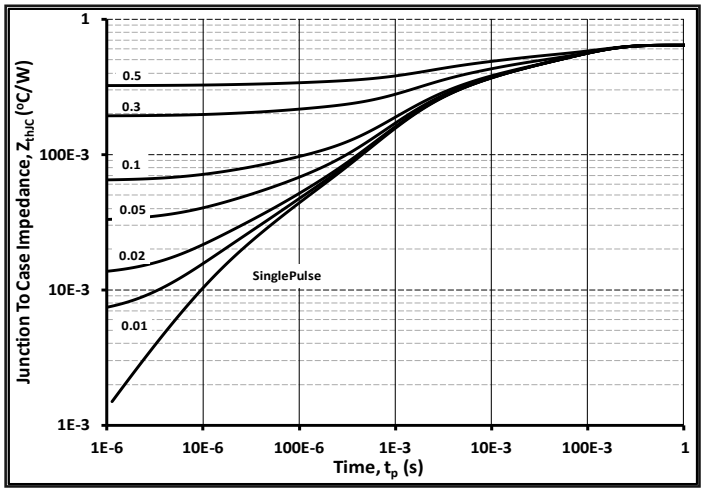


Figure 21. Transient Thermal Impedance (Junction - Case)

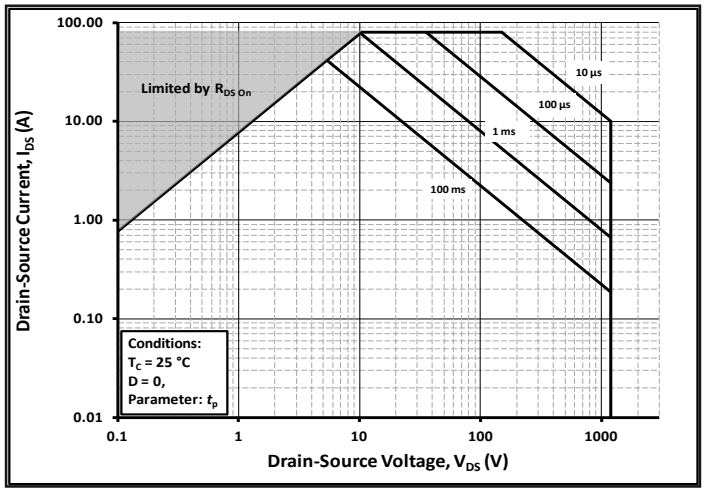


Figure 22. Safe Operating Area

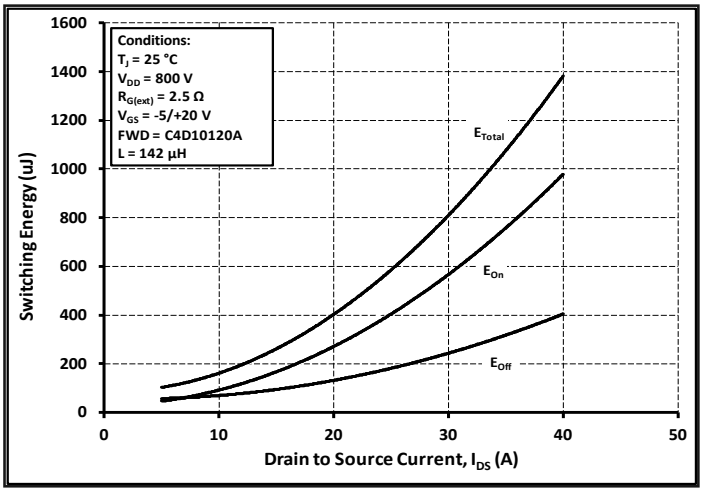


Figure 23. Clamped Inductive Switching Energy vs. Drain Current (V_{DD} = 800V)

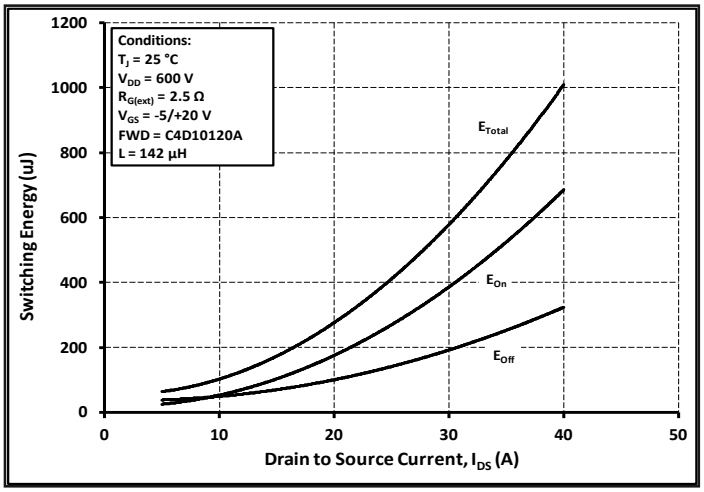


Figure 24. Clamped Inductive Switching Energy vs. Drain Current (V_{DD} = 600V)

Typical Performance

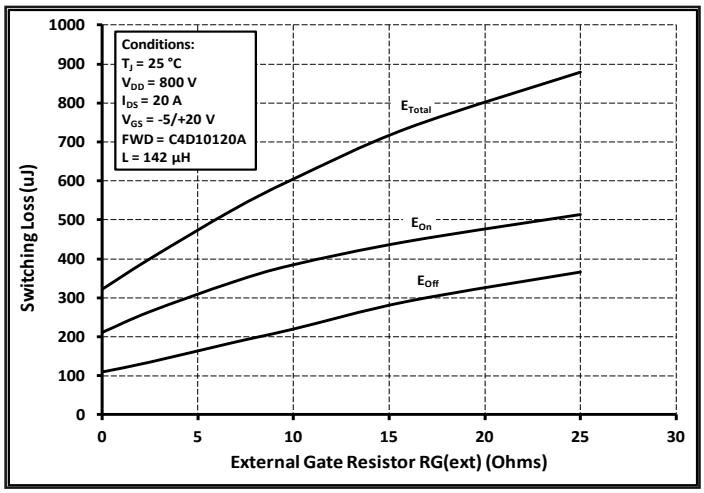


Figure 25. Clamped Inductive Switching Energy vs. $R_{G(ext)}$

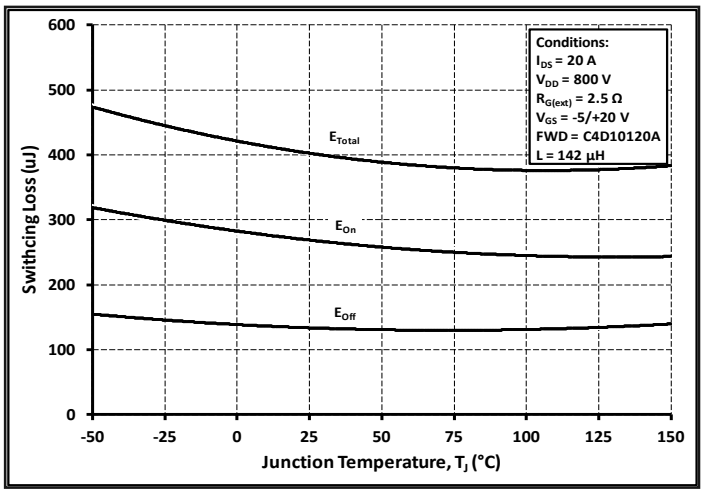


Figure 26. Clamped Inductive Switching Energy vs. Temperature

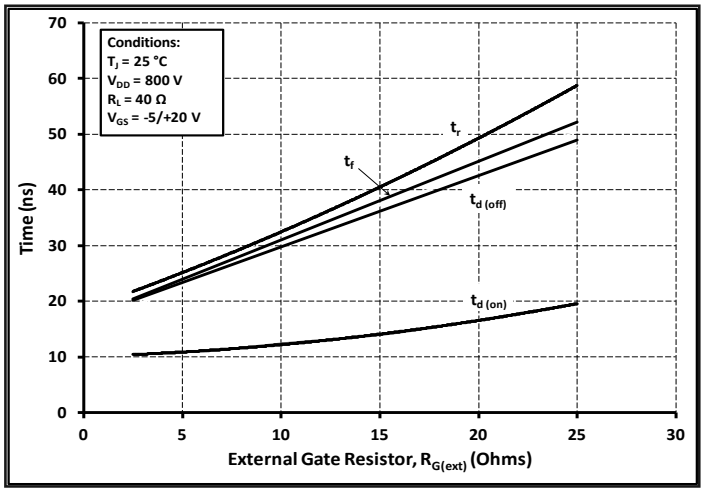


Figure 27. Switching Times vs. $R_{G(ext)}$

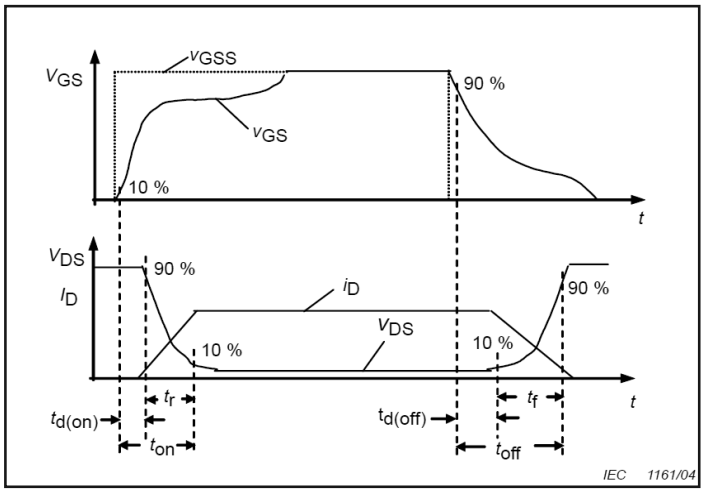


Figure 28. Switching Times Definition

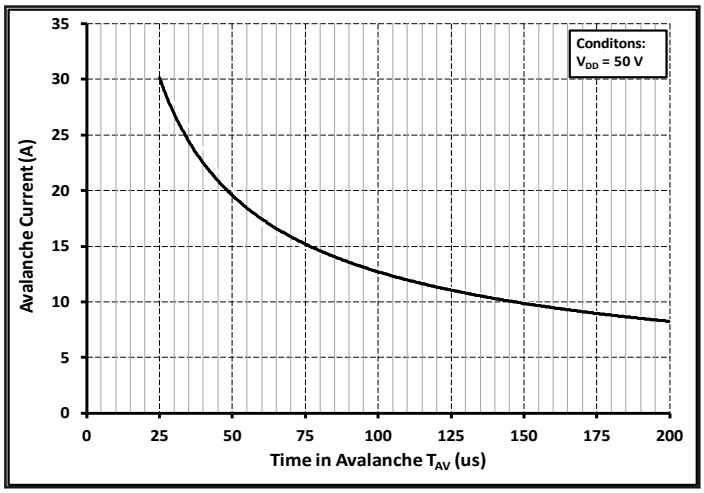


Figure 29. Single Avalanche SOA curve

Test Circuit Schematic

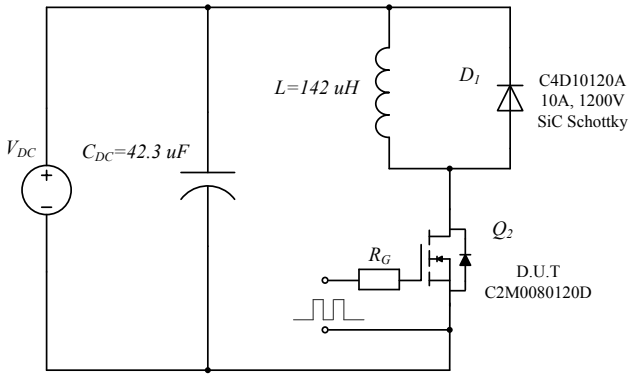


Figure 30. Clamped Inductive Switching Waveform Test Circuit

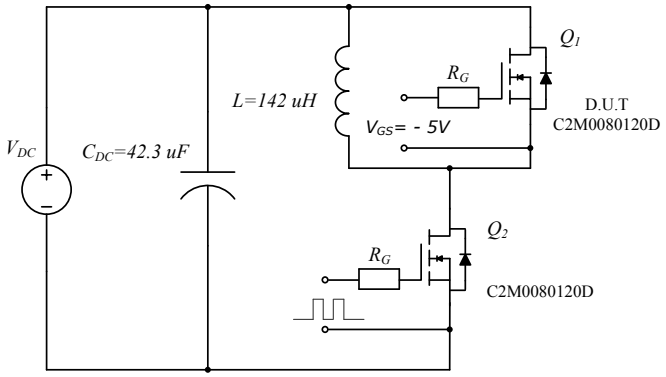


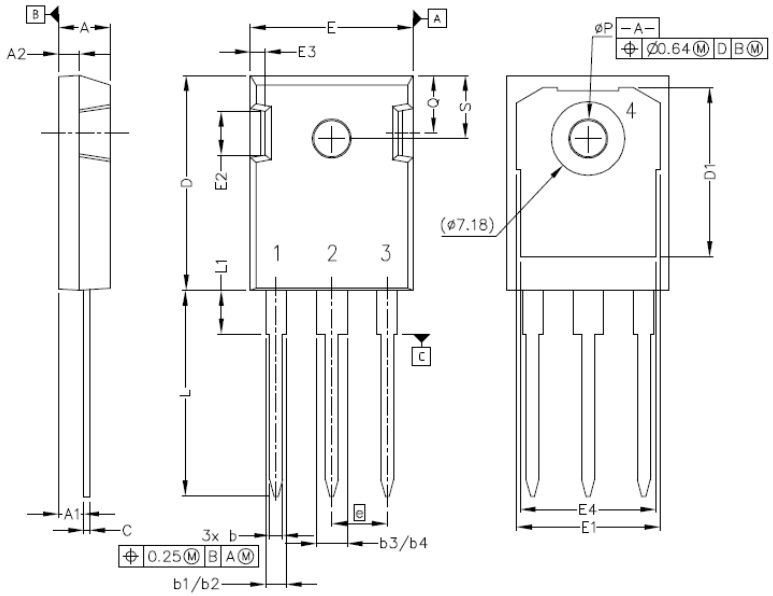
Figure 31. Body Diode Recovery Test Circuit

ESD Ratings

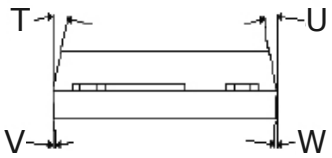
ESD Test	Total Devices Sampled	Resulting Classification
ESD-HBM	All Devices Passed 1000V	2 (>2000V)
ESD-MM	All Devices Passed 400V	C (>400V)
ESD-CDM	All Devices Passed 1000V	IV (>1000V)

Package Dimensions

Package TO-247-3



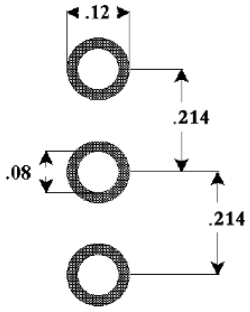
POS	Inches		Millimeters	
	Min	Max	Min	Max
A	.190	.205	4.83	5.21
A1	.090	.100	2.29	2.54
A2	.075	.085	1.91	2.16
b	.042	.052	1.07	1.33
b1	.075	.095	1.91	2.41
b2	.075	.085	1.91	2.16
b3	.113	.133	2.87	3.38
b4	.113	.123	2.87	3.13
c	.022	.027	0.55	0.68
D	.819	.831	20.80	21.10
D1	.640	.695	16.25	17.65
D2	.037	.049	0.95	1.25
E	.620	.635	15.75	16.13
E1	.516	.557	13.10	14.15
E2	.145	.201	3.68	5.10
E3	.039	.075	1.00	1.90
E4	.487	.529	12.38	13.43
e	.214 BSC		5.44 BSC	
N	3		3	
L	.780	.800	19.81	20.32
L1	.161	.173	4.10	4.40
ØP	.138	.144	3.51	3.65
Q	.216	.236	5.49	6.00
S	.238	.248	6.04	6.30
T	9°	11°	9°	11°
U	9°	11°	9°	11°
V	2°	8°	2°	8°
W	2°	8°	2°	8°



Pinout Information:

- Pin 1 = Gate
- Pin 2, 4 = Drain
- Pin 3 = Source

Recommended Solder Pad Layout



TO-247-3

Part Number	Package	Marking
C2M0080120D	TO-247-3	C2M0080120

Notes

- **RoHS Compliance**
  The levels of RoHS restricted materials in this product are below the maximum concentration values (also referred to as the threshold limits) permitted for such substances, or are used in an exempted application, in accordance with EU Directive 2011/65/EC (RoHS2), as implemented January 2, 2013. RoHS Declarations for this product can be obtained from your Cree representative or from the Product Documentation sections of www.cree.com.

- **REACh Compliance**
  REACh substances of high concern (SVHCs) information is available for this product. Since the European Chemical Agency (ECHA) has published notice of their intent to frequently revise the SVHC listing for the foreseeable future,please contact a Cree representative to insure you get the most up-to-date REACh SVHC Declaration. REACh banned substance information (REACh Article 67) is also available upon request.

- This product has not been designed or tested for use in, and is not intended for use in, applications implanted into the human body nor in applications in which failure of the product could lead to death, personal injury or property damage, including but not limited to equipment used in the operation of nuclear facilities, life-support machines, cardiac defibrillators or similar emergency medical equipment, aircraft navigation or communication or control systems, air traffic control systems.

Related Links

- **C2M PSPICE Models: http://wolfspeed.com/power/tools-and-support**
- **SiC MOSFET Isolated Gate Driver reference design: http://wolfspeed.com/power/tools-and-support**
- **SiC MOSFET Evaluation Board: http://wolfspeed.com/power/tools-and-support**

Cree, Inc.
4600 Silicon Drive
Durham, NC 27703
USA Tel: +1.919.313.5300
Fax: +1.919.313.5451
www.cree.com/power

C4D15120A

Silicon Carbide Schottky Diode

Z-Rec® Rectifier

V_{RRM}	=	1200 V
I_F (T_C=135˚C)	=	20 A
Q_c	=	77.5 nC

Features

- 1.2kV Schottky Rectifier
- Zero Reverse Recovery Current
- High-Frequency Operation
- Temperature-Independent Switching
- Extremely Fast Switching
- Positive Temperature Coefficient on V_F

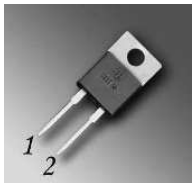
Benefits

- Replace Bipolar with Unipolar Rectifiers
- Essentially No Switching Losses
- Higher Efficiency
- Reduction of Heat Sink Requirements
- Parallel Devices Without Thermal Runaway

Applications

- Switch Mode Power Supplies (SMPS)
- Boost diodes in PFC or DC/DC stages
- Free Wheeling Diodes in Inverter stages
- AC/DC converters

Package



TO-220-2

Part Number	Package	Marking
C4D15120A	TO-220-2	C4D15120

Maximum Ratings (T_C=25°C unless otherwise specified)

Symbol	Parameter	Value	Unit	Test Conditions	Note
V_{RRM}	Repetitive Peak Reverse Voltage	1200	V		
V_{RSM}	Surge Peak Reverse Voltage	1300	V		
V_R	DC Peak Reverse Voltage	1200	V		
I_F	Continuous Forward Current	41 20 15	A	T_C=25˚C T_C=135˚C T_C=150˚C	Fig. 3
I_{FRM}	Repetitive Peak Forward Surge Current	68 44	A	T_C=25˚C, t_p=10 ms, Half Sine Pulse T_C=110˚C, t_p=10 ms, Half Sine Pulse	
I_{FSM}	Non-Repetitive Forward Surge Current	100 85	A	T_C=25˚C, t_p=10 ms, Half Sine Pulse T_C=110˚C, t_p=10 ms, Half Sine Pulse	Fig. 8
$I_{F,Max}$	Non-Repetitive Peak Forward Current	900 750	A	T_C=25˚C, t_p=10 µs, Pulse T_C=110˚C, t_p=10 µs, Pulse	Fig. 8
P_{tot}	Power Dissipation	192 83	W	T_C=25˚C T_C=110˚C	Fig. 4
T_J	Operating Junction Range	-55 to +175	°C		
T_{stg}	Storage Temperature Range	-55 to +135	°C		
	TO-220 Mounting Torque	1 8.8	Nm lbf-in	M3 Screw 6-32 Screw	

Electrical Characteristics

Symbol	Parameter	Typ.	Max.	Unit	Test Conditions	Note
V_F	Forward Voltage	1.6 2.3	1.8 3	V	I_F = 15 A T_J=25°C I_F = 15 A T_J=175°C	Fig. 1
I_R	Reverse Current	35 120	200 300	µA	V_R = 1200 V T_J=25°C V_R = 1200 V T_J=175°C	Fig. 2
Q_C	Total Capacitive Charge	77.5		nC	V_R = 800 V, I_F = 15A d*i*/d*t* = 200 A/µs T_J = 25°C	Fig. 5
C	Total Capacitance	1200 70 50		pF	V_R = 0 V, T_J = 25°C, f = 1 MHz V_R = 400 V, T_J = 25°C, f = 1 MHz V_R = 800 V, T_J = 25°C, f = 1 MHz	Fig. 6
E_C	Capacitance Stored Energy	22		µJ	V_R = 800 V	Fig. 7

Note:This is a majority carrier diode, so there is no reverse recovery charge.

Thermal Characteristics

Symbol	Parameter	Typ.	Unit	Note
$R_{\theta JC}$	Thermal Resistance from Junction to Case	0.78	°C/W	Fig. 9

Typical Performance

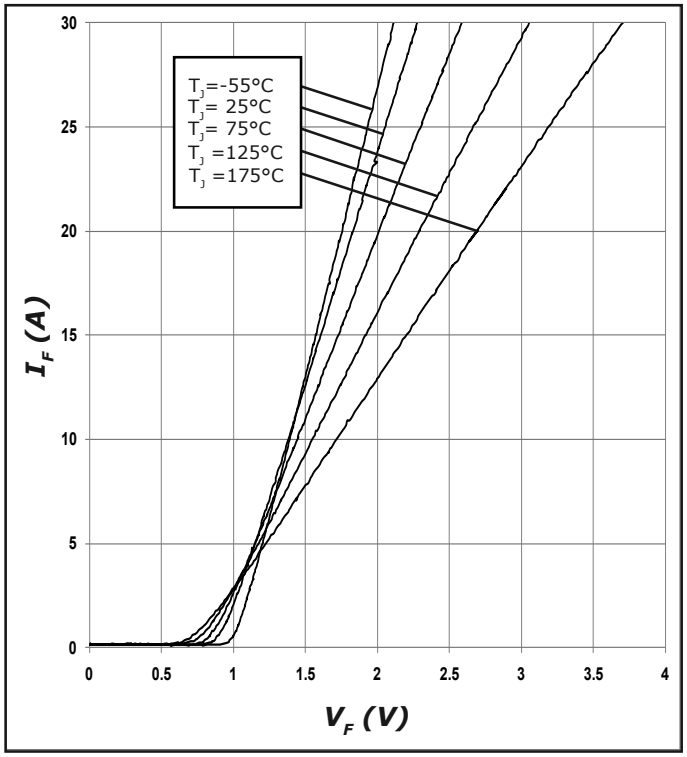


Figure 1. Forward Characteristics

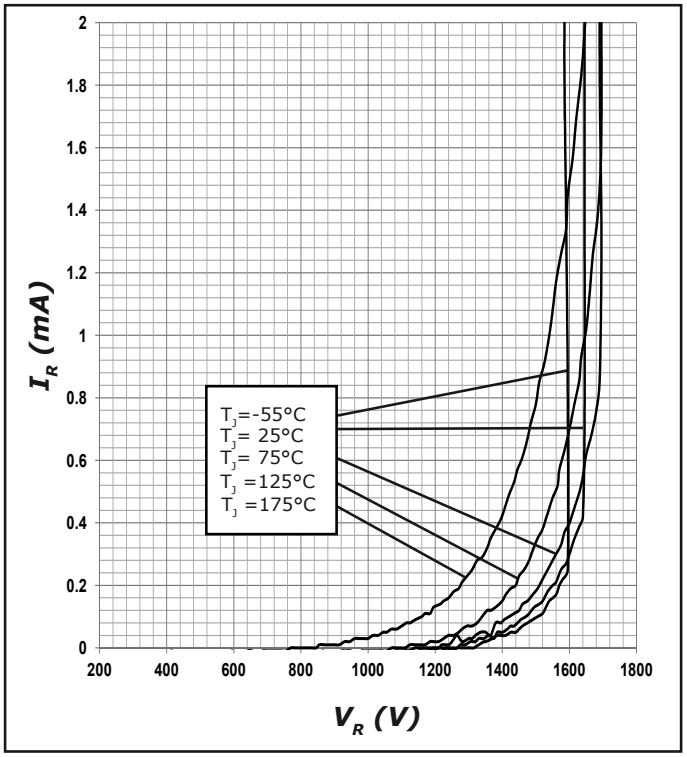


Figure 2. Reverse Characteristics

Typical Performance

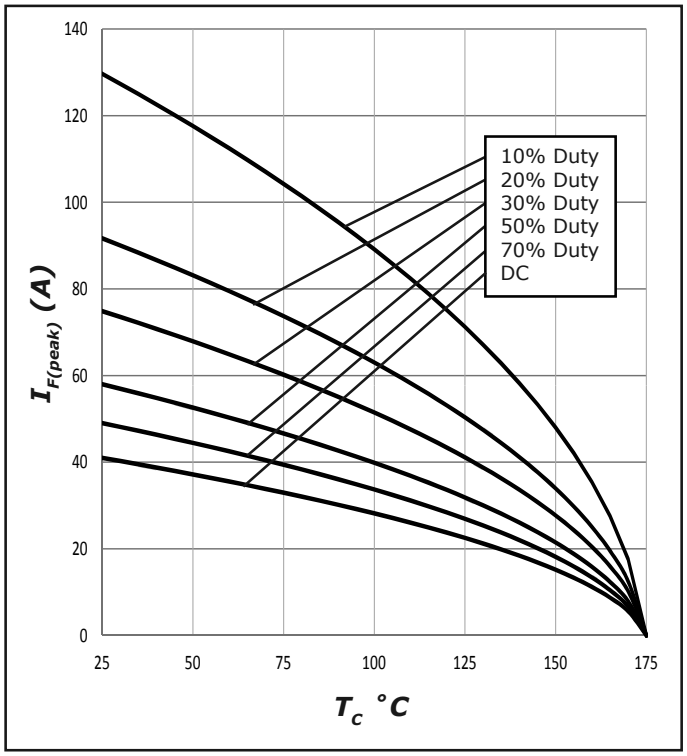


Figure 3. Current Derating

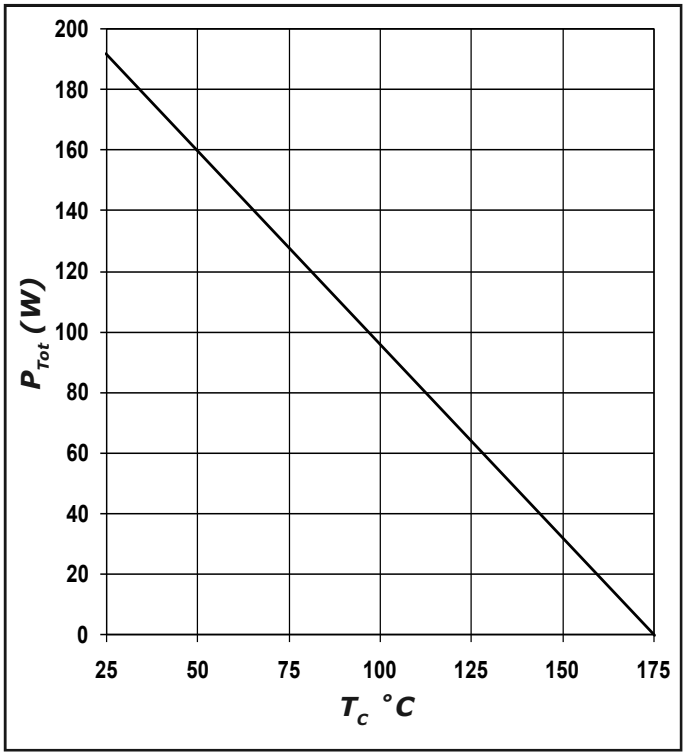


Figure 4. Power Derating

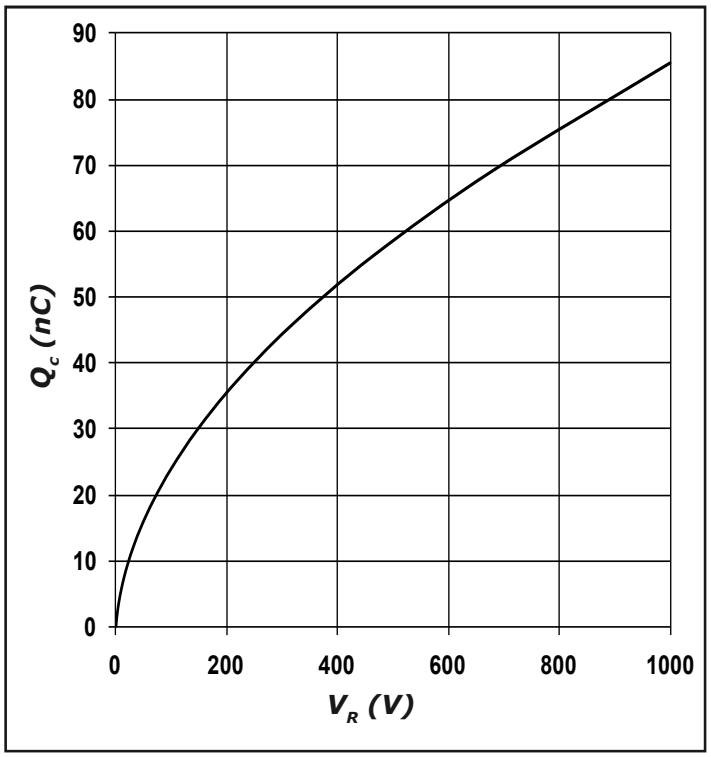


Figure 5. Recovery Charge vs. Reverse Voltage

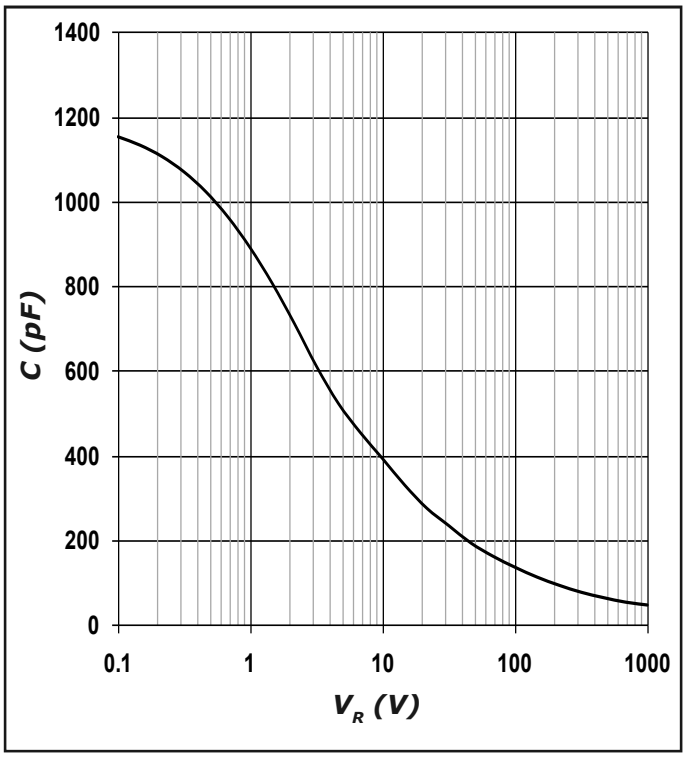


Figure 6. Capacitance vs. Reverse Voltage

Typical Performance

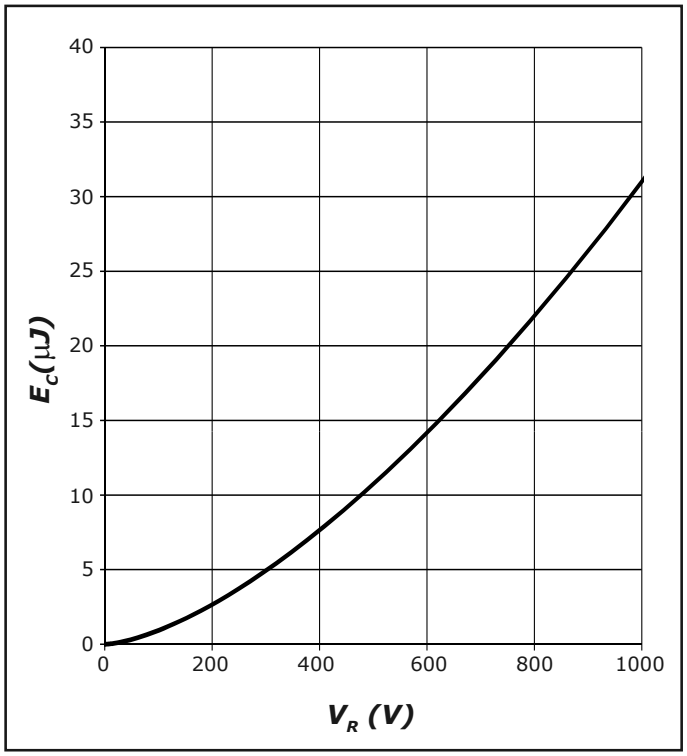


Figure 7. Typical Capacitance Stored Energy

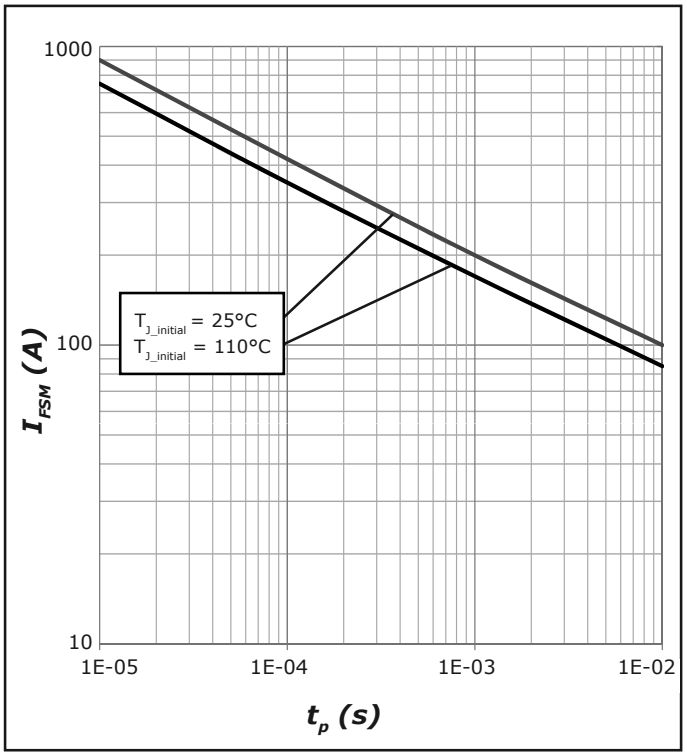


Figure 8. Non-repetitive peak forward surge current versus pulse duration (sinusoidal waveform)

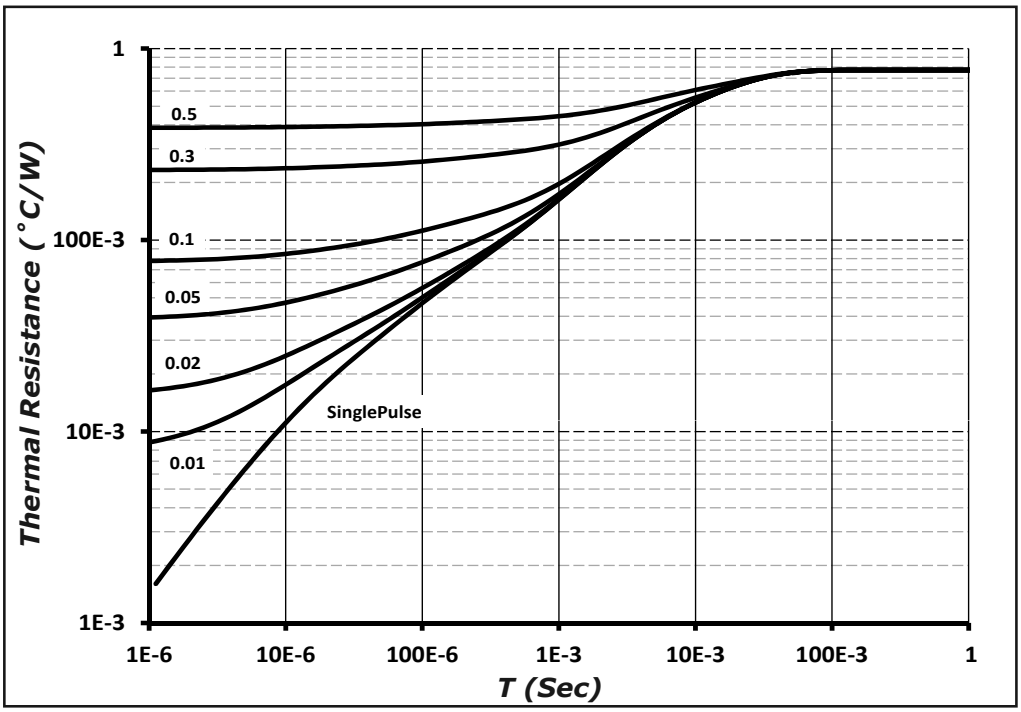
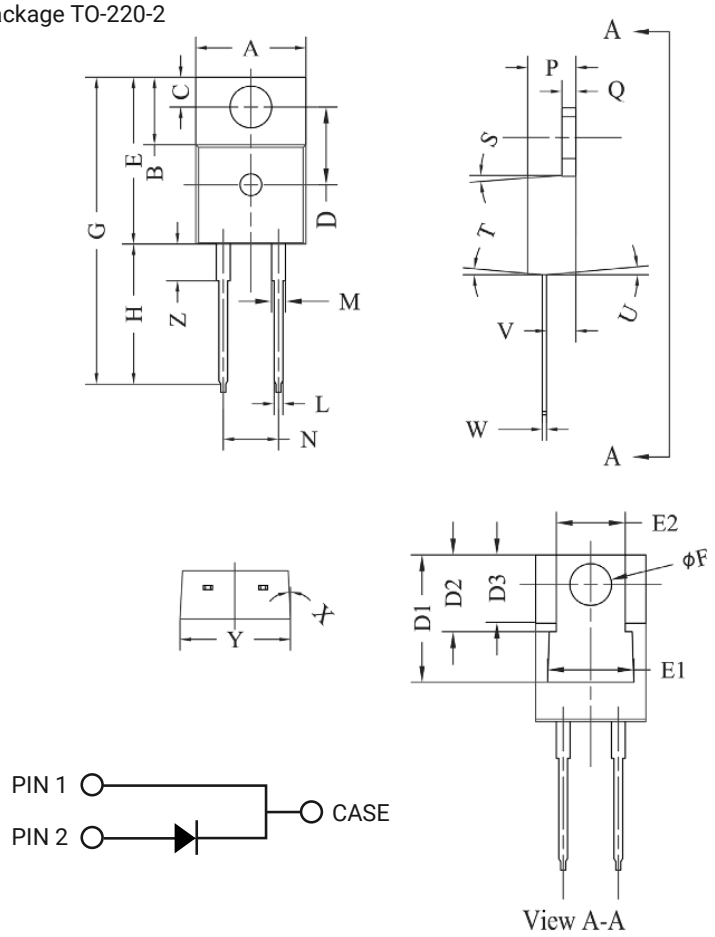


Figure 9. Transient Thermal Impedance

Package Dimensions

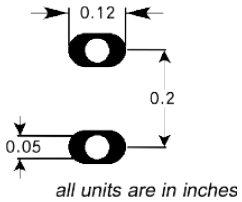
Package TO-220-2



POS	Inches		Millimeters	
	Min	Max	Min	Max
A	.381	.410	9.677	10.414
B	.235	.255	5.969	6.477
C	.100	.120	2.540	3.048
D	.223	.337	5.664	8.560
D1	.457-.490		11.60-12.45 typ	
D2	.277-.303 typ		7.04-7.70 typ	
D3	.244-.252 typ		6.22-6.4 typ	
E	.590	.615	14.986	15.621
E1	.302	.326	7.68	8.28
E2	.227	251	5.77	6.37
F	.143	.153	3.632	3.886
G	1.105	1.147	28.067	29.134
H	.500	.550	12.700	13.970
L	.025	.036	.635	.914
M	.045	.055	1.143	1.550
N	.195	.205	4.953	5.207
P	.165	.185	4.191	4.699
Q	.048	.054	1.219	1.372
S	3°	6°	3°	6°
T	3°	6°	3°	6°
U	3°	6°	3°	6°
V	.094	.110	2.388	2.794
W	.014	.025	.356	.635
X	3°	5.5°	3°	5.5°
Y	.385	.410	9.779	10.414
z	.130	.150	3.302	3.810

NOTE:
1. Dimension L, M, W apply for Solder Dip Finish

Recommended Solder Pad Layout

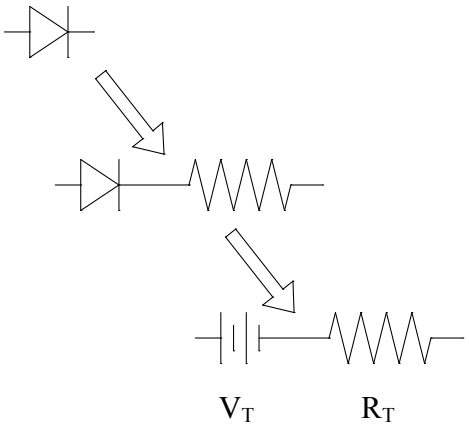


TO-220-2

Part Number	Package	Marking
C4D15120A	TO-220-2	C4D15120A

Note: Recommended soldering profiles can be found in the applications note here:
http://www.wolfspeed.com/power_app_notes/soldering

Diode Model



$$Vf_T = V_T + If * R_T$$

$$V_T = 0.97 + (T_j * -2.12*10^{-3})$$

$$R_T = 0.031 + (T_j * 3.92*10^{-4})$$

Note: T_j = Diode Junction Temperature In Degrees Celsius, valid from 25°C to 175°C

Notes

- **RoHS Compliance**
  The levels of RoHS restricted materials in this product are below the maximum concentration values (also referred to as the threshold limits) permitted for such substances, or are used in an exempted application, in accordance with EU Directive 2011/65/EC (RoHS2), as implemented January 2, 2013. RoHS Declarations for this product can be obtained from your Wolfspeed representative or from the Product Ecology section of our website at http://www.wolfspeed.com/power/tools-and-support/product-ecology.

- **REACh Compliance**
  REACh substances of high concern (SVHCs) information is available for this product. Since the European Chemical Agency (ECHA) has published notice of their intent to frequently revise the SVHC listing for the foreseeable future,please contact a Cree representative to insure you get the most up-to-date REACh SVHC Declaration. REACh banned substance information (REACh Article 67) is also available upon request.

- This product has not been designed or tested for use in, and is not intended for use in, applications implanted into the human body nor in applications in which failure of the product could lead to death, personal injury or property damage, including but not limited to equipment used in the operation of nuclear facilities, life-support machines, cardiac defibrillators or similar emergency medical equipment, aircraft navigation or communication or control systems, or air traffic control systems.

Related Links

- Cree SiC Schottky diode portfolio: http://www.wolfspeed.com/SiCSchottkydiodes
- Schottky diode Spice models: http://www.wolfspeed.com/Schottky-diode-model-request
- SiC MOSFET and diode reference designs: http://www.wolfspeed.com/Power-reference-designs

Cree, Inc.
4600 Silicon Drive
Durham, NC 27703
USA Tel: +1.919.313.5300
Fax: +1.919.313.5451
www.cree.com/power

BERGQUIST

Technical Data Sheet

Hi-Flow® 300P

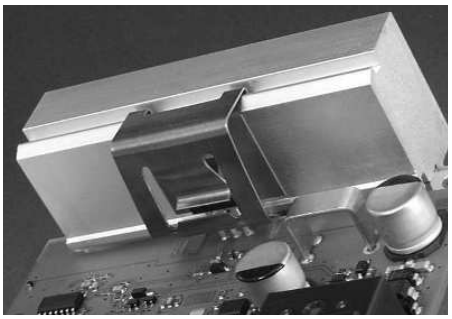
November 2013

PRODUCT DESCRIPTION

Electrically Insulating,Thermally Conductive Phase Change Material

FEATURES AND BENEFITS

- Thermal impedance: 0.13°C-in2/W (@25 psi)
- Field-proven polyimide film
  - excellent dielectric performance
  - excellent cut-through resistance
- Outstanding thermal performance in an insulated pad



Hi-Flow® 300P consists of a thermally conductive 55°C phase change compound coated on a thermally conductive polyimide film.The polyimide reinforcement makes the material easy to handle and the 55°C phase change temperature minimizes shipping and handling problems.

Hi-Flow® 300P achieves superior values in voltage breakdown and thermal performance when compared to its competition.The product is supplied on an easy release liner for exceptional handling in high volume manual assemblies. Hi-Flow 300P is designed for use as a thermal interface material between electronic power devices requiring electrical isolation to the heat sink.

Bergquist suggests the use of spring clips to assure constant pressure with the interface and power source. Please refer to thermal performance data to determine nominal spring pressure for your application.

Note: To build a part number, visit our website at www.bergquistcompany.com.

TYPICAL PROPERTIES OF HI-FLOW 300P

PROPERTY	IMPERIAL VALUE	METRIC VALUE	TEST METHOD
Color	Green	Green	Visual
Reinforcement Carrier	Polyimide	Polyimide	—
Thickness (inch) / (mm)	0.004 - 0.005	0.102 - 0.127	ASTM D374
Film Thickness (inch) / (mm)	0.001 - 0.002	0.025 - 0.050	ASTM D374
Elongation (%)	40	40	ASTM D882A
Tensile Strength (psi) / (MPa)	7000	48	ASTM D882A
Continuous Use Temp (°F) / (°C)	302	150	—
Phase Change Temp (°F) / (°C)	131	55	ASTM D3418
ELECTRICAL			
Dielectric Breakdown Voltage (Vac)	5000	5000	ASTM D149
Dielectric Constant (1000 Hz)	4.5	4.5	ASTM D150
Volume Resistivity (Ohm-meter)	10^{12}	10^{12}	ASTM D257
Flame Rating	V-O	V-O	U.L. 94
THERMAL			
Thermal Conductivity (W/m-K) (1)	1.6	1.6	ASTM D5470

THERMAL PERFORMANCE vs PRESSURE					
Pressure (psi)	10	25	50	100	200
TO-220 Thermal Performance (°C/W) 0.0010"	0.95	0.94	0.92	0.91	0.90
TO-220 Thermal Performance (°C/W) 0.0015"	1.19	1.17	1.16	1.14	1.12
TO-220 Thermal Performance (°C/W) 0.0020"	1.38	1.37	1.35	1.33	1.32
Thermal Impedance (°C-in²/W) 0.0010" (2)	0.13	0.13	0.12	0.12	0.12
Thermal Impedance (°C-in²/W) 0.0015" (2)	0.17	0.16	0.16	0.16	0.15
Thermal Impedance (°C-in²/W) 0.0020" (2)	0.19	0.19	0.19	0.18	0.18

1) This is the measured thermal conductivity of the Hi-Flow coating. It represents one conducting layer in a three-layer laminate. The Hi-Flow coatings are phase change compounds. These layers will respond to heat and pressure induced stresses. The overall conductivity of the material in post-phase change, thin film products is highly dependent upon the heat and pressure applied. This characteristic is not accounted for in ASTM D5470. Please contact Bergquist Product Management if additional specifications are required.
2) The ASTM D5470 test fixture was used and the test sample was conditioned at 70°C prior to test. The recorded value includes interfacial thermal resistance. These values are provided for reference only. Actual application performance is directly related to the surface roughness, flatness and pressure applied.

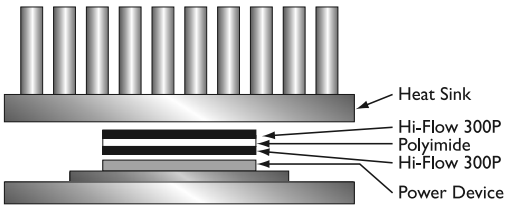
TYPICAL APPLICATIONS INCLUDE

- Spring / clip mounted
- Discrete power semiconductors and modules

CONFIGURATIONS AVAILABLE

- Roll form, die-cut parts and sheet form, dry both sides

We produce thousands of specials. Tooling charges vary depending on tolerances and complexity of the part.



Henkel

DATA SHEET

E65/32/27
E cores and accessories

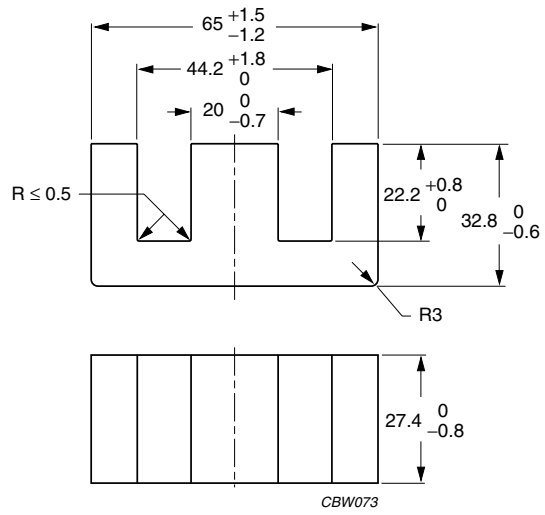
Supersedes data of September 2004 2008 Sep 01

FERROXCUBE
A YAGEO COMPANY

CORE SETS

Effective core parameters

SYMBOL	PARAMETER	VALUE	UNIT
$\Sigma(l/A)$	core factor (C1)	0.274	mm^{-1}
V_e	effective volume	79000	mm^3
l_e	effective length	147	mm
A_e	effective area	540	mm^2
A_{min}	minimum area	530	mm^2
m	mass of core half	≈205	g



Dimensions in mm.

Fig.1 E65/32/27 core half.

Core halves

A_L measured in combination with a non-gapped core half, clamping force for A_L measurements 60 ±20 N, unless stated otherwise.

GRADE	A_L (nH)	μ_e	TOTAL AIR GAP (μm)	TYPE NUMBER
3C90	100 ±5%(1)	≈ 22	≈ 14380	E65/32/27-3C90-E100
	160 ±5%(1)	≈ 35	≈ 7560	E65/32/27-3C90-E160
	250 ±5%(1)	≈ 54	≈ 4100	E65/32/27-3C90-E250
	315 ±5%(1)	≈ 68	≈ 3020	E65/32/27-3C90-E315
	400 ±8%(1)	≈ 87	≈ 2200	E65/32/27-3C90-E400
	630 ±10%(1)	≈ 136	≈ 1240	E65/32/27-3C90-E630
	8600 ±25%	≈ 1860	≈ 0	E65/32/27-3C90
3C92 des	6000 ±25%	≈ 1310	≈ 0	E65/32/27-3C92
3C94	8600 ±25%	≈ 1860	≈ 0	E65/32/27-3C94
3C95 des	10600 ±25%	≈ 2300	≈ 0	E65/32/27-3C95
3F3	100 ±5%(1)	≈ 22	≈ 14380	E65/32/27-3F3-E100
	160 ±5%(1)	≈ 35	≈ 7560	E65/32/27-3F3-E160
	250 ±5%(1)	≈ 54	≈ 4100	E65/32/27-3F3-E250
	315 ±5%(1)	≈ 68	≈ 3020	E65/32/27-3F3-E315
	400 ±8%(1)	≈ 87	≈ 2200	E65/32/27-3F3-E400
	630 ±10%(1)	≈ 136	≈ 1240	E65/32/27-3F3-E630
	7300 ±25%	≈ 1580	≈ 0	E65/32/27-3F3

Note

1. Measured in combination with an equal gapped core half.

Core halves of high permeability grades

Clamping force for A_L measurements, 60 ±20 N.

GRADE	A_L (nH)	μ_e	AIR GAP (μm)	TYPE NUMBER
3C11	16700 ±25%	≈ 3620	≈ 0	E65/32/27-3C11

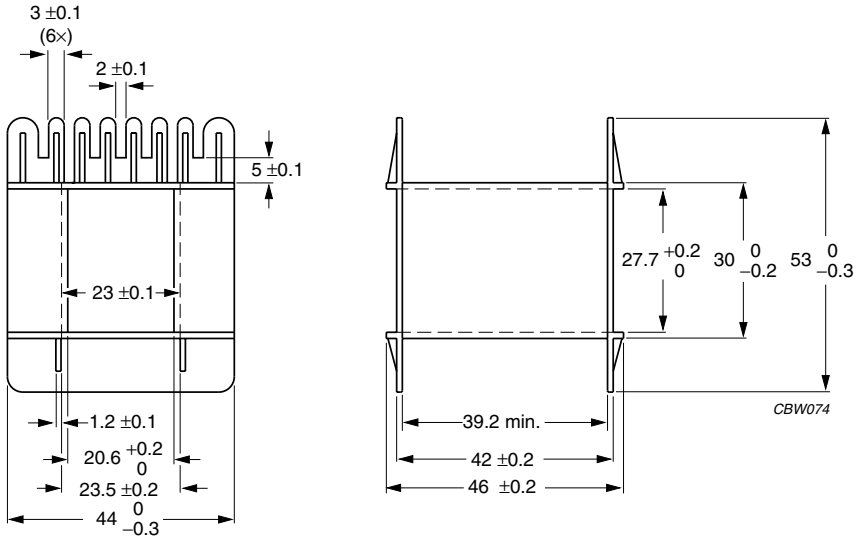
Properties of core sets under power conditions

GRADE	B (mT) at	CORE LOSS (W) at				
	H = 250 A/m; f = 25 kHz; T = 100 °C	f = 25 kHz; $\hat{B}$ = 200 mT; T = 100 °C	f = 100 kHz; $\hat{B}$ = 100 mT; T = 100 °C	f = 100 kHz; $\hat{B}$ = 200 mT; T = 25 °C	f = 100 kHz; $\hat{B}$ = 200 mT; T = 100 °C	f = 400 kHz; $\hat{B}$ = 50 mT; T = 100 °C
3C90	≥320	≤ 9.1	≤ 12	–	–	–
3C92	≥370	–	≤ 8.5	–	≤ 47	–
3C94	≥320	–	≤ 8.5	–	≤ 47	–
3C95	≥320	–	–	≤ 49.8	≤ 47.4	–
3F3	≥320	–	≤ 10.5	–	–	≤ 21

COIL FORMER

General data for E65/32/27 coil former without pins

PARAMETER	SPECIFICATION
Coil former material	polyethylene terephtalate (PET), glass reinforced, flame retardant in accordance with *"UL 94V-0"*; UL file number E107536
Maximum operating temperature	130 °C, *"IEC 60085",* class B



Dimensions in mm.

Fig.2 E65/32/27 coil former.

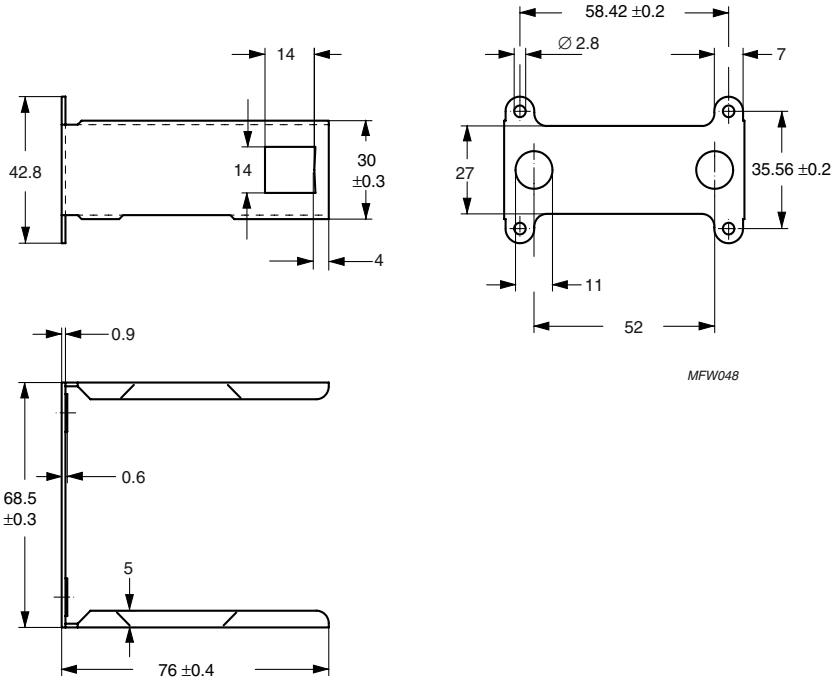
Winding data and area product for E65/32/27 coil former without pins (E)

NUMBER OF SECTIONS	MINIMUM WINDING AREA (mm^2)	NOMINAL WINDING WIDTH (mm)	AVERAGE LENGTH OF TURN (mm)	AREA PRODUCT Ae x Aw (mm^4)	TYPE NUMBER
1	394	39.2	150	213000	CP-E65-1S-T

MOUNTING PARTS

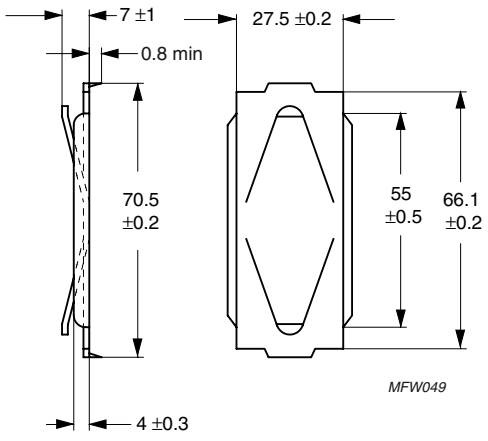
General data for mounting parts

ITEM	REMARKS	FIGURE	TYPE NUMBER
Clasp	steel, zinc (Zn) plated	3	CLA-E65/32/27
Spring	steel, zinc (Zn) plated	4	SPR-E65/32/27



Dimensions in mm.

Fig.3 E65/32/27 clasp.



Dimensions in mm.

Fig.4 E65/32/27 spring.

DATA SHEET STATUS DEFINITIONS

DATA SHEET STATUS	PRODUCT STATUS	DEFINITIONS
Preliminary specification	Development	This data sheet contains preliminary data. Ferroxcube reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.
Product specification	Production	This data sheet contains final specifications. Ferroxcube reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.

DISCLAIMER

Life support applications — These products are not designed for use in life support appliances, devices, or systems where malfunction of these products can reasonably be expected to result in personal injury. Ferroxcube customers using or selling these products for use in such applications do so at their own risk and agree to fully indemnify Ferroxcube for any damages resulting from such application.

PRODUCT STATUS DEFINITIONS

STATUS	INDICATION	DEFINITION
Prototype	prot	These are products that have been made as development samples for the purposes of technical evaluation only. The data for these types is provisional and is subject to change.
Design-in	des	These products are recommended for new designs.
Preferred		These products are recommended for use in current designs and are available via our sales channels.
Support	sup	These products are **not** recommended for new designs and may not be available through all of our sales channels. Customers are advised to check for availability.

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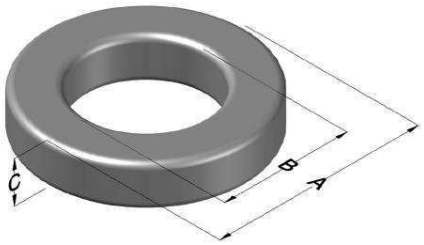
110 Delta Drive
Pittsburgh, PA 15238
NAFTA Sales: (1)800-245-3984
HK Sales : (852)3102-9337
magnetics@spang.com
www.mag-inc.com



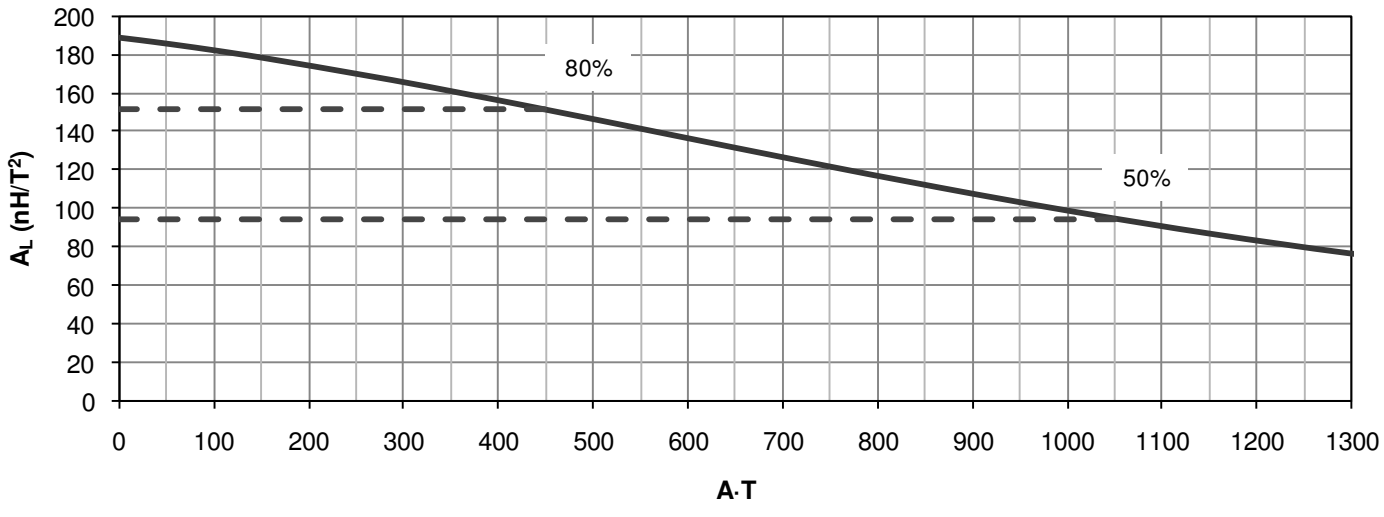
Kool Mμ Permeability (μ)	A_L (nH/T²)	Core Marking			Coating Color
		Lot Number	Part Number	Inductance Grade	
60	189 ± 8%	XXXXXX	77617A7	N/A	Black

Dimensions	Uncoated		Coated Limits			Packaging
	(mm)	(in)	(mm)	(in)		
OD (A)	62.00	2.440	62.91	2.477	max	Cardboard cut-outs Box Qty= 45 pcs
ID (B)	32.60	1.283	31.69	1.248	min	
HT (C)	25.0	0.984	25.91	1.020	max	

Electrical Characteristics			Physical Characteristics						
Watt Loss @ 100 kHz, 50mT MaxI (mW/cm³)	DC Bias min (A·T/cm)		Voltage Breakdown wire to wire min (V_{AC})	Break Strength min (kg)	Window Area W_A(mm²)	Cross Section A_e (mm²)	Path Length L_e (mm)	Volume V_e (mm³)	Weight (g)
	80%	50%							
240	34.2	75.5	2000	113	789	360	144	51,800	320

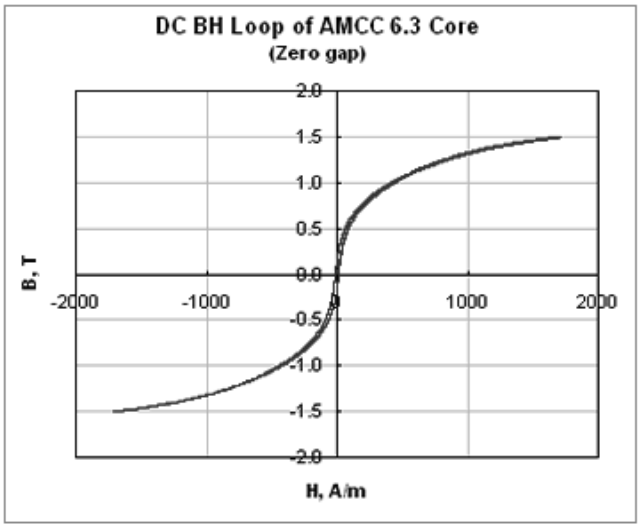
Winding Information							Temperature Rating
Winding Length Per Turn				Wound Coil Dimensions (mm)			Curie Temp: 500˚C
Winding Factor	(mm)	Winding Factor	(mm)	40% Winding Factor	OD	75.3	Coating Temp (Continuous up to): 200˚C
					HT	39.7	
				Completely Full Window	Max OD	81.4	Notes:
0%	83.0	40%	99.5		Max HT	47.4	
20%	91.3	45%	102	Surface Area (mm²)			
25%	93.4	50%	104				
30%	94.9	60%	109	Unwound Core	12,000		
35%	97.5	70%	115	40% Winding Factor	21,000		

Typical DC Bias Performance



Revision 12/4/2014

POWERLITE® C-Cores are manufactured with iron based Metglas® amorphous Alloy 2605SA1.Their unique combination of low loss and high saturation flux density take advanced power conditioning applications to higher performance levels than previously possible with conventional ferromagnetic
Materials.



Applications

For a wide range of high frequencies and hot-spot temperatures (up to Class F), POWERLITE C-Cores are used in a growing list of advanced power conditioning applications including:

- UPS and SMPS Power Factor Correction Chokes
- UPS Harmonic Filter Inductors
- High-Power Outdoor Industrial Ballasts
- Welding Power Supplies
- High-Speed Rail Power Systems

Benefits

Manufactured in a variety of ultra-efficient core configurations, POWERLITE C-Cores provide significant cost, design and performance benefits over ordinary Si-Fe, ferrite and MPP cores such as:

- High Saturation Flux Density (1.56 T)
- Low Profile – enables weight and volume reductions of up to 50%
- Low Temperature Rise – enabling smaller compact designs
- Low Loss – resulting from micro-thin Metglas ribbon (25 µm)

Physical Properties METGLAS Alloy 2605SA1

Ribbon Thickness (µm)	.23
Density (g/cm^3)	7.18
Thermal Expansion (ppm/°C)	7.6
Crystallization Temperature (°C)	508
Curie Temperature (°C)	399
Continuous Service Temperature (°C)	150
Tensile Strength (MN/m2)	1k-1.7k
Elastic Modulus (GN/m2)	100-110
Vicker's Hardness (50g load)	900

Magnetic Properties METGLAS Powerlite Cores

Saturation Flux Density (T)	1.56
Permeability (depending on gap size)	VARIABLE
Saturation Magnetostriction (ppm)	27
Electrical Resistivity (µΩ.cm)	130

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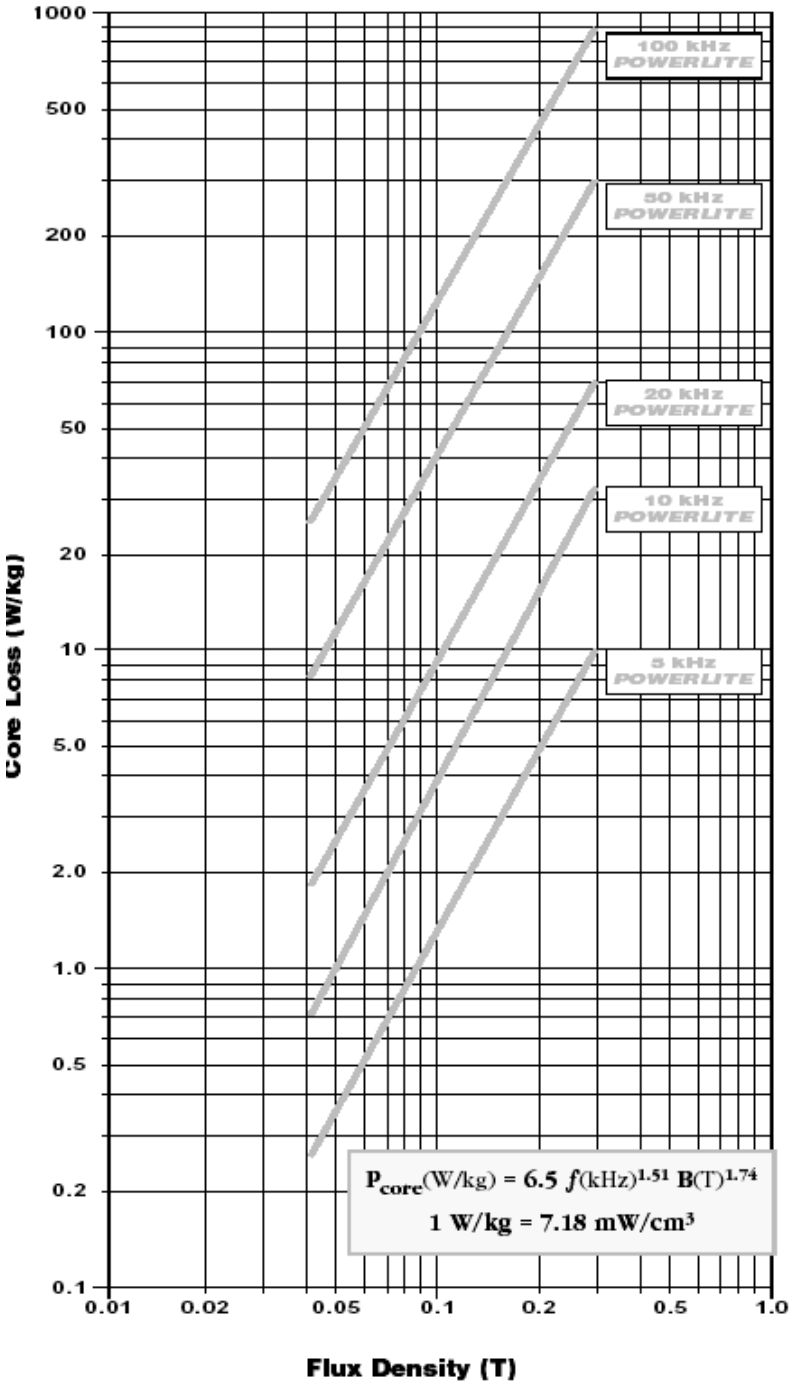
1-800-581-7654

Core Loss vs. Flux Density† @ 25°C



† *These curves were determined from ac data; use 1/2 the actual .B to determine core loss for unidirectional applications.*

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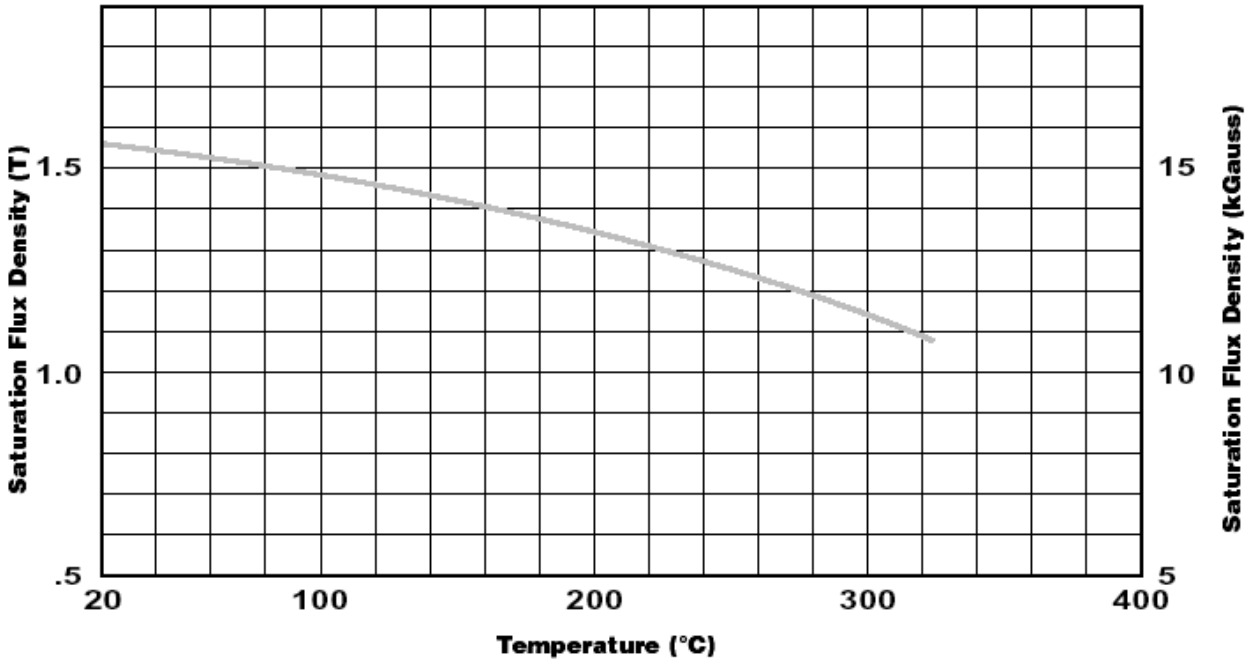
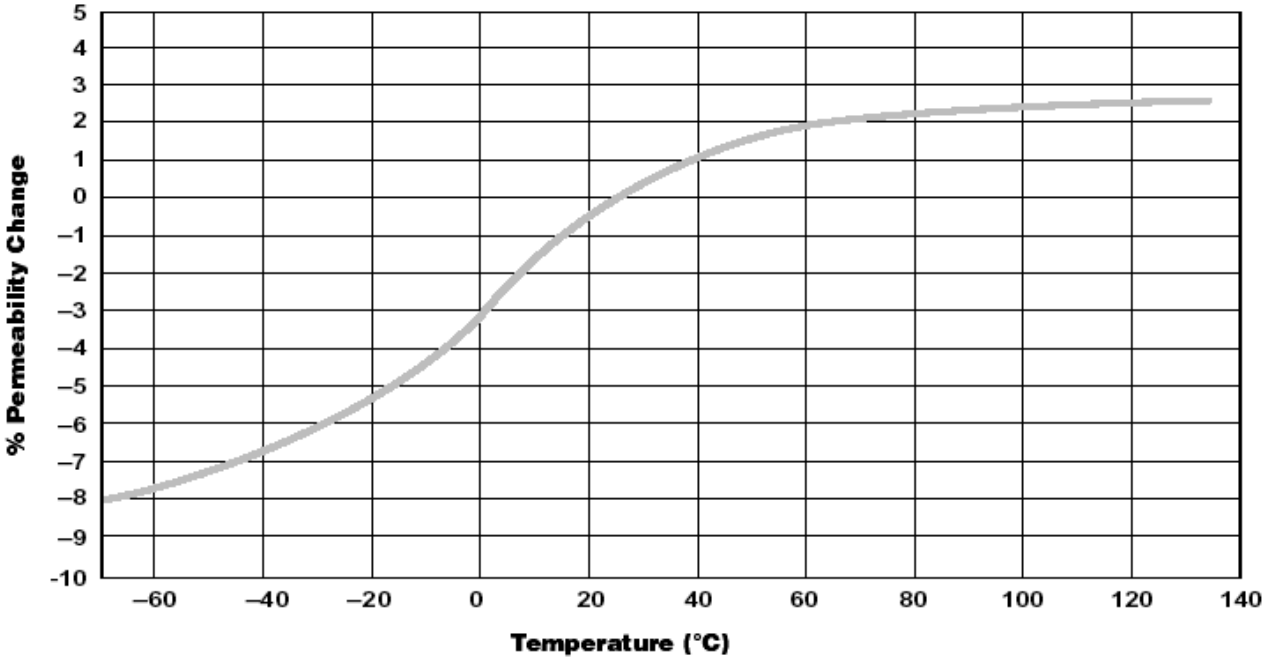
Saturation Induction vs. Temperature
POWERLITE® C-Cores



Permeability vs. Temperature
POWERLITE® C-Cores



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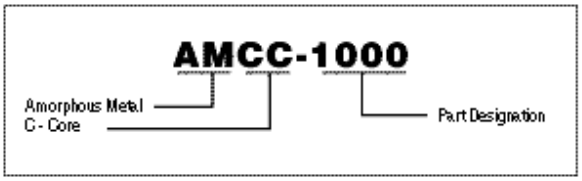
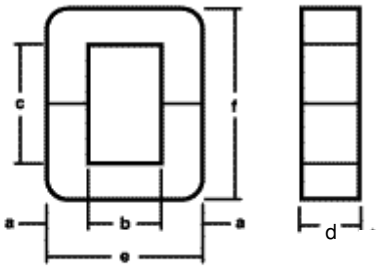
Product Code Designation





POWERLITE® C - Cores

	CORE DIMENSION										PERFROMANCE PARAMETERS				
Core No.	a (mm)	±	b (mm) ref *	c (mm) ref *	d (mm)	±	e (mm)	±	f (mm)	±	lm (cm)	Ac (cm^2)	Wa (cm^2)	Ap (cm^4)	Mass (g)
AMCC 4	9.0	0.50	10.0	32.80	15.0	0.50	28.00	1.50	50.8	1.25	12.20	1.11	3.30	3.60	99
AMCC 6.3	10.0	0.50	11.0	33.00	20.0	0.50	31.00	1.00	53.0	2.00	12.80	1.60	3.60	6.0	154
AMCC 8	11.0	0.80	13.0	30.00	20.0	0.50	35.00	1.00	52.0	2.00	13.00	1.80	3.90	7.00	172
AMCC 10	11.0	0.80	13.0	40.00	20.0	0.50	35.00	1.00	62.0	2.00	15.40	1.80	5.20	9.40	198
AMCC 16A	11.0	0.80	13.0	40.00	25.0	0.50	35.00	1.00	62.0	2.00	15.10	2.30	5.20	11.70	248
AMCC 16B	11.0	0.80	13.0	50.00	25.0	0.50	35.00	1.00	72.0	2.00	17.00	2.30	6.50	14.70	281
AMCC 20	11.0	0.80	13.0	50.00	30.0	0.50	35.00	1.00	72.0	2.00	17.50	2.70	6.50	17.60	337
AMCC 25	13.0	0.80	15.0	56.00	25.0	0.50	41.00	1.00	82.0	2.00	19.60	2.70	8.40	22.40	379
AMCC 32	13.0	0.80	15.0	56.00	30.0	0.50	41.00	1.00	82.0	2.00	20.00	3.20	8.40	26.90	454
AMCC 40	13.0	0.80	15.0	56.00	35.0	0.50	41.00	1.00	82.0	2.00	19.90	3.70	8.40	31.30	530
AMCC 50	16.0	1.00	20.0	70.00	25.0	0.50	52.00	1.00	102.0	3.00	24.90	3.30	14.00	45.90	586
AMCC 63	16.0	1.00	20.0	70.00	30.0	0.50	52.00	1.00	102.0	3.00	25.30	3.90	14.00	55.10	703
AMCC 80	16.0	1.00	20.0	70.00	40.0	1.00	52.00	1.00	102.0	3.00	25.40	5.20	14.00	73.50	938
AMCC 100	16.0	1.00	20.0	70.00	45.0	1.00	52.00	1.00	102.0	3.00	25.00	5.90	14.00	82.7	1,055
AMCC 168S	20.4	0.50	30.0	154.20	20.0	0.50	70.50	1.25	195.0	3.00	45.40	3.35	45.80	153.2	1,101
AMCC 125	19.0	1.00	25.0	83.00	35.0	1.00	63.00	1.00	121.0	3.00	30.20	5.50	20.80	113.1	1,166
AMCC 160	19.0	1.00	25.0	83.00	40.0	1.00	63.00	1.00	121.0	3.00	28.50	6.20	20.80	129.3	1,333
AMCC 200	19.0	1.00	25.0	83.00	50.0	1.00	63.00	1.00	121.0	3.00	29.80	7.80	20.80	161.6	1,666
AMCC 367S	25.8	1.00	67.0	97.80	25.0	0.70	117.60	1.50	149.4	1.50	43.78	5.29	63.81	340.1	1,668
AMCC 250	19.0	1.00	25.0	90.00	60.0	1.00	63.00	1.00	128.0	3.00	31.40	9.30	22.50	210.3	2,095
AMCC 320	22.0	1.00	35.0	85.00	50.0	1.00	79.00	1.00	129.0	4.00	32.50	9.00	29.80	268.3	2,167
AMCC 400	22.0	1.00	35.0	85.00	65.0	1.00	79.00	1.00	129.0	4.00	33.60	11.70	29.80	348.8	2,817
AMCC 500	25.0	1.00	40.0	85.00	55.0	1.00	90.00	1.00	135.0	4.00	35.60	11.30	34.00	383.4	2,890
AMCC 630	25.0	1.00	40.0	85.00	70.0	1.00	90.00	1.00	135.0	4.00	35.60	14.30	34.00	487.9	3,678
AMCC 800A	25.0	1.00	40.0	85.00	85.0	1.50	90.00	1.00	135.0	4.00	35.60	17.40	34.00	592.5	4,466
AMCC 800B	30.0	1.00	40.0	95.00	85.0	1.50	100.00	1.00	155.0	4.00	39.30	21.00	38.00	794.6	5,972
AMCC 1000	33.0	1.00	40.0	105.00	85.0	1.50	106.00	1.00	171.0	5.00	42.70	23.00	42.00	966.0	7,109

** Products generally do not fully comply with material characteristics – deviations may occur due to shape and size.*

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Film Capacitors

Metallized Polypropylene Film Capacitors (MKP)

Series/Type: **B32774 ... B32778**

Date: June 2015

EPCOS AG is a TDK Group Company.

Recommended applications

- Frequency converters
- Industrial and high-end power supplies
- Solar inverters

Climatic

- Max. operating temperature: 105 °C (case)
- Climatic category (IEC 60068-1): 40/105/56

Construction

- Dielectric: Polypropylene (MKP)
- Plastic case (UL 94 V-0)
- Epoxy resin sealing (UL 94 V-0)

Features

- Capacitance values up to 480 µF
- High CV product, compact
- Good self-healing properties
- Over-voltage capability
- Low losses with high current capability
- High reliability
- Long useful life
- RoHS-compatible

Terminals

- Parallel wire leads, lead-free tinned
- 2-pin, 4-pin and 12-pin versions
- Standard lead lengths: 6 ! 1 mm

Marking

Manufacturer's logo and lot number,
date code, rated capacitance (coded),
capacitance tolerance (code letter) and
rated DC voltage

Delivery mode

Bulk (untaped)

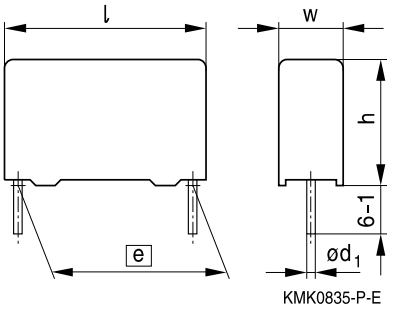
Dimensional drawings

Dimensions in mm

Number of wires	Lead spacing e ±0.4	Lead diameter d_1 ±0.05	Type
2-pin	27.5	0.8	B32774D
2-pin	37.5	1.0	B32776E
2-pin	37.5	1.0	B32776T
4-pin	37.5	1.2	B32776G
4-pin	37.5	1.2	B32776T
4-pin	52.5	1.2	B32778T
4-pin	52.5	1.2	B32778G
12-pin	52.5	1.2	B32778J

Dimensional drawings 2-pin versions

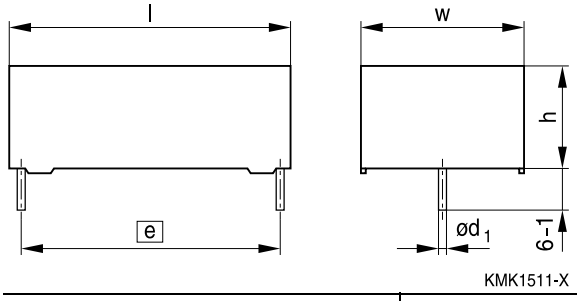
B32774D, B32776E



	B32774D	B32776E
Lead spacing e ±0.4:	27.5	37.5
Lead diameter d_1:	0.8	1.0

(Dimensions in mm)

B32776T (low profile)

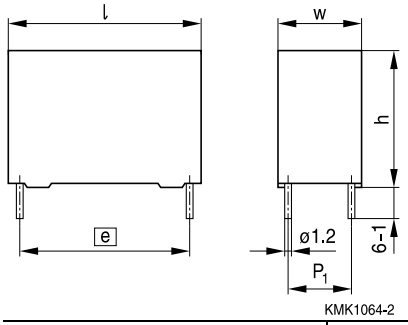


Lead spacing e ±0.4:	37.5
Lead diameter d_1:	1.0

(Dimensions in mm)

Dimensional drawings 4-pin versions

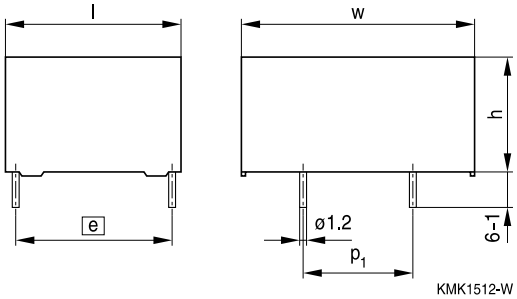
B32776G, B32778G

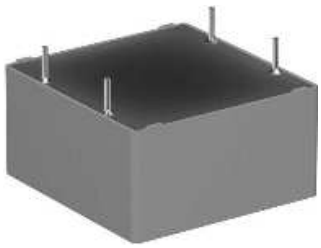


	B32776G	B32778G
Lead spacing e ±0.4:	37.5	52.5
Lead diameter d_1:	1.2	1.2

(Dimensions in mm)

B32776T, B32778T (low profile)



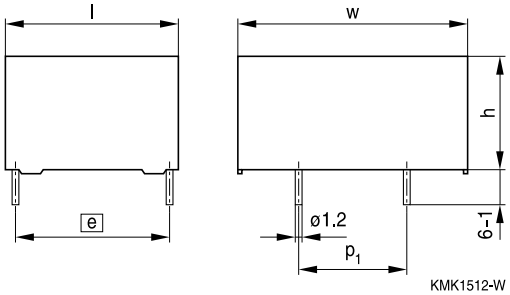


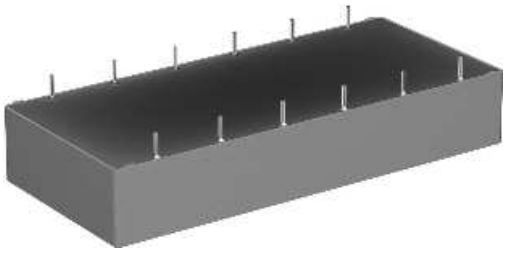
	B32776T	B32778T
Lead spacing e ±0.4:	37.5	52.5
Lead diameter d_1:	1.2	1.2

(Dimensions in mm)

Dimensional drawing 12-pin version

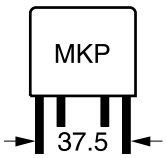
B32778J





Lead spacing e ±0.4:	52.5
Lead diameter d_1:	1.2

(Dimensions in mm)



B32776

MKP DC link ! high density series ! up to 480 µF

Ordering codes and packing units (lead spacing 37.5 mm)

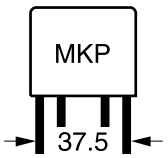
C_R[1] µF	Max. dimensions w × h × l mm	P_1 mm	Ordering code (composition see below)	$I_{RMS,max}$[2] 70 °C 10 kHz A	ESR_{typ} 70 °C 10 kHz mΩ	ESL_{typ}[3] 70 °C 10 kHz nH	tan δ 1 kHz 10^{-3}	tan δ 10 kHz 10^{-3}	pcs. MOQ
$V_{R,70\,°C}$ = 450 V DC, $V_{op,85\,°C}$ = 450 V DC									
12	24.0 × 15.0 × 41.5	!	B32776T4126K000	7.0	17.1	19.0	2.2	21.0	1040
16	24.0 × 19.0 × 41.5	!	B32776T4166K000	8.0	13.0	18.0	2.3	21.2	780
30	20.0 × 39.5 × 41.5	10.2	B32776G4306+000	14.0	7.0	11.0	2.3	21.3	640
30	20.0 × 39.5 × 41.5	!	B32776E4306+000	14.0	7.3	28.0	2.4	22.3	640
35	28.0 × 37.0 × 42.0	10.2	B32776G4356+000	16.5	6.0	10.0	2.3	21.4	440
35	28.0 × 37.0 × 42.0	!	B32776E4356+000	16.0	6.4	24.0	2.4	22.6	440
40	28.0 × 37.0 × 42.0	10.2	B32776G4406+000	17.5	5.3	11.0	2.3	21.4	440
40	28.0 × 37.0 × 42.0	!	B32776E4406+000	17.0	5.6	26.0	2.4	22.7	440
40	43.0 × 22.0 × 41.5	20.3	B32776T4406K000	17.0	5.2	13.0	2.3	21.2	280
50	28.0 × 42.5 × 41.5	10.2	B32776G4506+000	20.0	4.3	12.0	2.3	21.7	440
50	28.0 × 42.5 × 41.5	!	B32776E4506+000	19.0	4.7	30.0	2.5	23.8	440
60	30.0 × 45.0 × 42.0	20.3	B32776G4606+000	23.5	3.6	14.0	2.4	22.3	400
60	30.0 × 45.0 × 42.0	!	B32776E4606+000	22.0	4.0	32.0	2.5	24.2	400
65	33.0 × 48.0 × 42.0	20.3	B32776G4656+000	25.5	3.3	14.0	2.3	22.2	180
$V_{R,70\,°C}$ = 575 V DC, $V_{op,85\,°C}$ = 500 V DC									
8.5	24.0 × 15.0 × 41.5	!	B32776T5855+000	6.5	19.9	19.0	1.9	17.2	1040
12	24.0 × 19.0 × 41.5	!	B32776T5126K000	8.0	14.4	18.0	1.9	17.4	780
25	20.0 × 39.5 × 41.5	10.2	B32776G5256K000	14.0	7.0	12.0	1.9	17.5	640
25	20.0 × 39.5 × 41.5	!	B32776E5256K000	13.5	7.4	28.0	2.0	18.3	640
30	28.0 × 37.0 × 42.0	10.2	B32776G5306K000	16.5	5.8	11.0	1.9	17.6	440
30	28.0 × 37.0 × 42.0	!	B32776E5306K000	16.5	6.1	26.0	2.0	18.5	440
30	43.0 × 22.0 × 41.5	20.3	B32776T5306K000	16.5	5.8	13.0	1.9	17.3	280
35	28.0 × 42.5 × 41.5	10.2	B32776G5356+000	19.0	5.0	12.0	1.9	17.8	440
35	28.0 × 42.5 × 41.5	!	B32776E5356+000	18.0	5.3	29.0	2.0	19.0	440
45	30.0 × 45.0 × 42.0	20.3	B32776G5456K000	22.0	4.0	13.0	1.9	17.9	400
45	30.0 × 45.0 × 42.0	!	B32776E5456K000	21.0	4.4	32.0	2.1	19.7	400
50	33.0 × 48.0 × 42.0	20.3	B32776G5506K000	25.0	3.5	14.0	2.0	18.1	180

MOQ = Minimum Order Quantity, consisting of 4 packing units.
Intermediate capacitance values are available on request.

Composition of ordering code

+ = Capacitance tolerance code:
J = ±5%
K = ±10%

1) Capacitance value measured at 1 kHz
2) Max ripple current I_{RMS} at 70 °C, 10 kHz for $\Delta T \leq 20$ °C at $\Delta ESR_{typ} \leq \pm 5\%$
3) Typical ESL value measured at resonance frequency (see specific graphs of Z vs freq)



Ordering codes and packing units (lead spacing 37.5 mm)

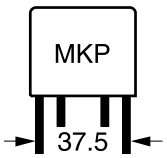
C_R[1] µF	Max. dimensions w × h × l mm	P_1 mm	Ordering code (composition see below)	$I_{RMS,max}$[2] 70 °C 10 kHz A	ESR_{typ} 70 °C 10 kHz mΩ	ESL_{typ}[3] 70 °C 10 kHz nH	tan δ 1 kHz 10^{-3}	tan δ 10 kHz 10^{-3}	pcs. MOQ
$V_{R,70\,°C}$ = 800 V DC, $V_{op,85\,°C}$ = 700 V DC									
6.8	24.0 × 15.0 × 41.5	!	B32776T8685+000	6.0	22.1	18.0	1.7	15.1	1040
8.5	24.0 × 19.0 × 41.5	!	B32776T8855+000	7.5	17.8	18.0	1.7	15.1	780
14	18.0 × 32.5 × 41.5	!	B32776E8146+000	10.0	11.5	23.0	1.8	16.3	720
15	20.0 × 39.5 × 41.5	10.2	B32776G8156+000	12.0	9.6	10.0	1.7	15.2	640
15	20.0 × 39.5 × 41.5	!	B32776E8156+000	11.5	10.3	24.0	1.7	15.7	640
20	28.0 × 37.0 × 42.0	10.2	B32776G8206+000	14.5	7.5	10.0	1.7	15.3	440
20	28.0 × 37.0 × 42.0	!	B32776E8206+000	14.5	7.8	24.0	1.7	15.9	440
20	43.0 × 22.0 × 41.5	20.3	B32776T8206K000	14.5	7.2	14.0	1.7	15.1	280
22	28.0 × 37.0 × 42.0	10.2	B32776G8226+000	15.5	6.8	11.0	1.7	15.3	440
22	28.0 × 37.0 × 42.0	!	B32776E8226+000	15.0	7.1	25.0	1.7	16.0	440
25	28.0 × 42.5 × 41.5	10.2	B32776G8256+000	17.0	6.1	11.0	1.7	15.4	440
25	28.0 × 42.5 × 41.5	!	B32776E8256+000	16.5	6.4	28.0	1.8	16.3	440
30	30.0 × 45.0 × 42.0	20.3	B32776G8306+000	19.5	5.1	12.0	1.7	15.6	400
30	30.0 × 45.0 × 42.0	!	B32776E8306+000	19.0	5.5	30.0	1.8	16.7	400
35	33.0 × 48.0 × 42.0	20.3	B32776G8356+000	22.0	4.3	14.0	1.7	15.7	180
$V_{R,70\,°C}$ = 900 V DC, $V_{op,85\,°C}$ = 800 V DC									
5	24.0 × 15.0 × 41.5	!	B32776T9505+000	5.5	26.1	19.0	1.5	13.4	1040
7.5	24.0 × 19.0 × 41.5	!	B32776T9755K000	7.5	17.8	18.0	1.5	13.5	780
15	20.0 × 39.5 × 41.5	10.2	B32776G9156K000	12.5	9.1	12.0	1.5	13.6	640
15	20.0 × 39.5 × 41.5	!	B32776E9156K000	12.0	9.4	28.0	1.5	14.1	640
16	43.0 × 22.0 × 41.5	20.3	B32776T9166K000	14.0	8.1	14.0	1.5	13.5	280
20	28.0 × 37.0 × 42.0	10.2	B32776G9206K000	15.0	7.0	11.0	1.5	13.6	440
20	28.0 × 37.0 × 42.0	!	B32776E9206K000	15.0	7.3	26.0	1.6	14.2	440
22	28.0 × 42.5 × 41.5	10.2	B32776G9226K000	17.0	6.3	12.0	1.5	13.7	440
22	28.0 × 42.5 × 41.5	!	B32776E9226K000	16.5	6.6	29.0	1.6	14.5	440
25	30.0 × 45.0 × 42.0	20.3	B32776G9256+000	19.0	5.5	13.0	1.5	13.8	400
25	30.0 × 45.0 × 42.0	!	B32776E9256+000	18.5	5.9	32.0	1.6	14.7	400
30	33.0 × 48.0 × 42.0	20.3	B32776G9306+000	21.5	4.7	14.0	1.5	13.9	180

MOQ = Minimum Order Quantity, consisting of 4 packing units.
Intermediate capacitance values are available on request.

Composition of ordering code

+ = Capacitance tolerance code:
J = ±5%
K = ±10%

1) Capacitance value measured at 1 kHz
2) Max ripple current I_{RMS} at 70 °C, 10 kHz for $\Delta T \leq 20$ °C at $\Delta ESR_{typ} \leq \pm 5\%$
3) Typical ESL value measured at resonance frequency (see specific graphs of Z vs freq)



B32776

MKP DC link ! high density series ! up to 480 µF

Ordering codes and packing units (lead spacing 37.5 mm)

C_R[1] µF	Max. dimensions w × h × l mm	P_1 mm	Ordering code (composition see below)	$I_{RMS,max}$[2] 70 °C 10 kHz A	ESR_{typ} 70 °C 10 kHz mΩ	ESL_{typ}[3] 70 °C 10 kHz nH	tan δ 1 kHz 10^{-3}	tan δ 10 kHz 10^{-3}	pcs. MOQ
$V_{R,70\,°C}$ = 1100 V DC, $V_{op,85\,°C}$ = 920 V DC									
3.9	24.0 × 15.0 × 41.5	!	B32776T0395+000	5.0	30.5	18.0	1.4	12.1	1040
5	24.0 × 19.0 × 41.5	!	B32776T0505+000	6.5	23.6	18.0	1.4	12.1	780
12	20.0 × 39.5 × 41.5	10.2	B32776G0126+000	12.0	10.2	12.0	1.4	12.2	640
12	20.0 × 39.5 × 41.5	!	B32776E0126+000	11.5	10.5	28.0	1.4	12.6	640
13	43.0 × 22.0 × 41.5	20.3	B32776T0136K000	13.0	8.9	14.0	1.4	12.1	280
14	28.0 × 37.0 × 42.0	10.2	B32776G0146+000	13.5	8.7	21.0	1.4	12.2	440
14	28.0 × 37.0 × 42.0	!	B32776E0146+000	13.5	9.0	25.0	1.4	12.6	440
16	28.0 × 42.5 × 41.5	10.2	B32776G0166+000	15.5	7.4	12.0	1.4	12.3	440
16	28.0 × 42.5 × 41.5	!	B32776E0166+000	15.0	7.8	30.0	1.4	12.9	440
20	30.0 × 45.0 × 42.0	20.3	B32776G0206+000	18.0	6.0	14.0	1.4	12.4	400
20	30.0 × 45.0 × 42.0	!	B32776E0206+000	17.5	6.5	32.0	1.4	13.1	400
22	33.0 × 48.0 × 42.0	20.3	B32776G0226+000	21.0	4.9	15.0	1.3	11.4	180
$V_{R,70\,°C}$ = 1300 V DC, $V_{op,85\,°C}$ = 1100 V DC									
2.7	24.0 × 15.0 × 41.5	!	B32776T1275+000	5.0	34.7	19.0	1.1	9.6	1040
3.5	24.0 × 19.0 × 41.5	!	B32776T1355+000	6.0	27.4	18.0	1.1	9.7	780
8.0	20.0 × 39.5 × 41.5	10.2	B32776G1805+000	11.0	12.1	12.0	1.1	9.7	640
8.0	20.0 × 39.5 × 41.5	!	B32776E1805+000	10.5	12.4	24.0	1.2	10.0	640
9.0	43.0 × 22.0 × 41.5	20.3	B32776T1905K000	12.0	10.7	13.0	1.1	9.7	280
10	28.0 × 37.0 × 42.0	10.2	B32776G1106+000	13.0	9.6	11.0	1.1	9.7	440
10	28.0 × 37.0 × 42.0	!	B32776E1106+000	12.5	9.9	26.0	1.2	10.0	440
12	28.0 × 42.5 × 41.5	10.2	B32776G1126+000	14.5	8.1	12.0	1.1	9.8	440
12	28.0 × 42.5 × 41.5	!	B32776E1126+000	14.0	8.5	28.0	1.2	10.1	440
14	30.0 × 45.0 × 42.0	20.3	B32776G1146+000	17.0	6.8	14.0	1.1	10.1	400
14	30.0 × 45.0 × 42.0	!	B32776E1146+000	16.5	7.3	32.0	1.2	10.4	400
16	33.0 × 48.0 × 42.0	20.3	B32776G1166+000	19.0	6.0	15.0	1.1	9.9	180

MOQ = Minimum Order Quantity, consisting of 4 packing units.
Intermediate capacitance values are available on request.

Composition of ordering code

+ = Capacitance tolerance code:
J = ±5%
K = ±10%

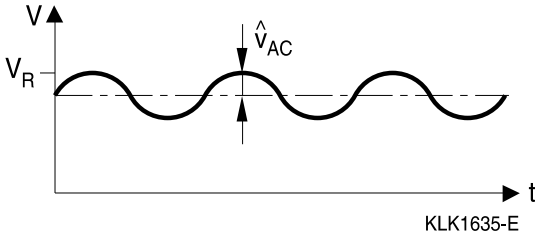
1) Capacitance value measured at 1 kHz
2) Max ripple current I_{RMS} at 70 °C, 10 kHz for $\Delta T \leq 20$ °C at $\Delta ESR_{typ} \leq \pm 5\%$
3) Typical ESL value measured at resonance frequency (see specific graphs of Z vs freq)

Technical data

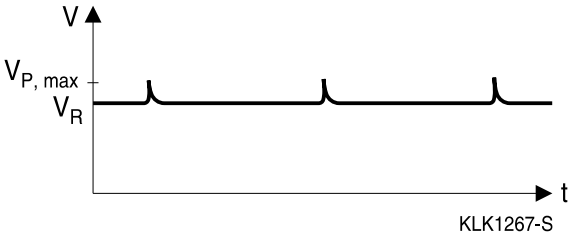
Reference standard: IEC 61071.
All data given at T = 20 °C, unless otherwise specified.

Operating temperature range (case)	Max. operating temperature, $T_{op,max}$ +105 °C Upper category temperature T_{max} +105 °C Lower category temperature T_{min} –40 °C					
Insulation Resistance R_{ins} given as time constant $\tau = C_R$ " R_{ins}, rel. humidity ≤ 65% (minimum as-delivered values)	τ > 10 000 s (after 1 min.) For $V_R \geq$ 500 V measured at 500 V For V_R < 500 V measured at V_R					
DC test voltage between terminals (10 s)	1.5 " V_R					
Voltage test terminal to case (10 s)	2110 V AC, 50 Hz					
Pulse Handling Capability (V/µs)	I_P (A) / C (µF)					
Reliability: Failure rate λ	10 fit (≤ 1 " 10^{-9}/h) at 0.5 " V_R, 40 °C For conversion to other operating conditions, refer to chapter "Quality assurance", data book 2009 "Film capacitors", page 442.					
Service life t_{SL}	100 000 h at V_R and 70 °C					
V_R (V DC)	450	575	800	900	1100	1300
Continuous operation voltage V_{op} (V DC) at 70 °C	450	575	800	900	1100	1300
Continuous operation voltage V_{op} (V DC) at 85 °C	450	500	700	800	920	1100
For temperatures between 85 °C and 105 °C	1.33%/°C of V_{op} derating compared to V_{op} at 85 °C					

Typical waveforms



KLK1635-E



KLK1267-S

Restrictions:
V_R: Maximum operating peak voltage of either polarity but of a non-reversing waveform, for which the capacitor has been designed for continuous operation.
$\hat{v}_{AC} \leq$ 0.2 " V_R

Film Capacitors

Metallized Polypropylene Film Capacitors (MKP)

Series/Type: **B32794 ... B32798**

Date: August 2014

BM@L P ÷D fp ÷ QAH Dd r m@l j m^kv+

MKP AC filtering

Typical applications

- Output AC filtering for power converters UPS, solar inverters, motor drives

Climatic

- Max. operating temperature: 105 °C
- Climatic category (IEC 60068-1): 40/85/56

Construction

- Dielectric: Polypropylene (PP)
- Plastic case (UL 94 V-0)
- Epoxy resin sealing (UL 94 V-0)

Features

- Optimized AC voltage performance
- High ripple current/frequency capability
- Small dimensions
- For PCB mounting
- RoHS-compatible

Terminals

- Parallel wire leads, lead-free tinned
- 2-pin and 4-pin versions
- Standard lead lengths: 6 ! 1 mm
- Special lead lengths available on request

Marking

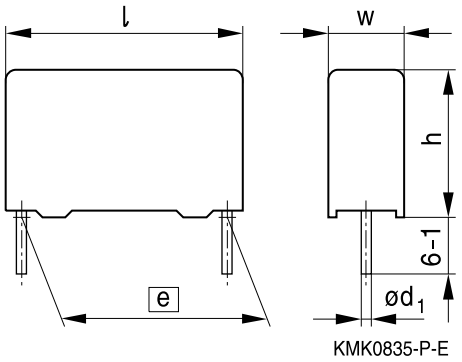
Manufacturer's logo, date code, rated capacitance (coded), capacitance tolerance (code letter), rated AC voltage

Delivery mode

Bulk (untaped, lead length 6 ! 1 mm)

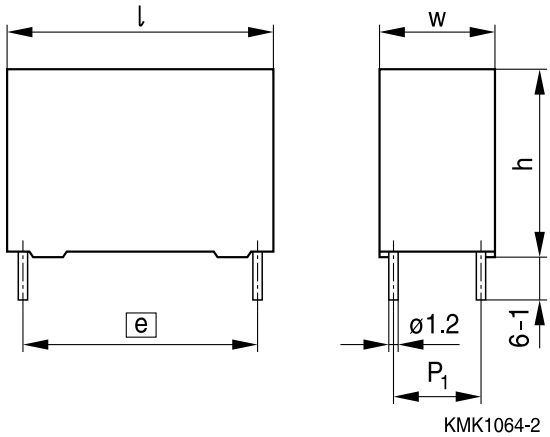
Dimensional drawings

2-pin version



KMK0835-P-E

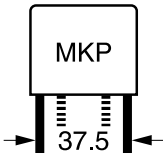
4-pin version



KMK1064-2

Dimensions in mm

Version	Lead spacing e ±0.4	Lead diameter d_1	Type
2-pin	27.5	0.8	B32794D
2-pin	37.5	1.0	B32796E/T
4-pin	37.5	1.2	B32796G
4-pin	52.5	1.2	B32798G



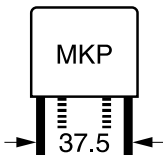
Ordering codes and packing units (lead spacing 37.5 mm)

V_{RMS}	V_R	C_R	Max. dimensions w × h × l	P_1	Ordering code (composition see below)	I_{RMS} 60 °C 10 kHz	ESL	ESR 10 kHz	Untaped pcs./
V AC	V DC	µF	mm	mm		A	nH	mΩ	MOQ
250	630	8	24.0 × 15.0 × 41.5	!	B32796T2805+000	8	21	9	1040
		11	24.0 × 19.0 × 41.5	!	B32796T2116+000	10	23	8	780
		22	20.0 × 39.5 × 42.0	10.2	B32796G2226+000	15	30	3.2	640
		22	20.0 × 39.5 × 42.0	!	B32796E2226+000	14	30	3.2	640
		25	28.0 × 37.0 × 42.0	10.2	B32796G2256+000	17	30	2.9	440
		25	28.0 × 37.0 × 42.0	!	B32796E2256+000	16	30	2.9	440
		40	30.0 × 45.0 × 42.0	20.3	B32796G2406+000	21	33	2.3	400
		40	30.0 × 45.0 × 42.0	!	B32796E2406+000	20	33	2.3	400
		45	33.0 × 48.0 × 42.5	20.3	B32796G2456+000	23	33	1.9	180
300	700	5.6	24.0 × 15.0 × 41.5	!	B32796T3565+000	7	21	12	1040
		7.5	24.0 × 19.0 × 41.5	!	B32796T3755+000	9	23	10	780
		16	20.0 × 39.5 × 42.0	10.2	B32796G3166+000	14	30	3.9	640
		16	20.0 × 39.5 × 42.0	!	B32796E3166+000	13	30	3.9	640
		20	28.0 × 37.0 × 42.0	10.2	B32796G3206+000	15	30	3.1	440
		20	28.0 × 37.0 × 42.0	!	B32796E3206+000	14	30	3.1	440
		30	30.0 × 45.0 × 42.0	20.3	B32796G3306+000	19	33	2.2	400
		30	30.0 × 45.0 × 42.0	!	B32796E3306+000	18	33	2.2	400
		34	33.0 × 48.0 × 42.5	20.3	B32796E3346+000	20	33	1.9	180
350	875	4	24.0 × 15.0 × 41.5	!	B32796T8405+000	7	21	13	1040
		5	24.0 × 19.0 × 41.5	!	B32796T8505+000	9	23	11	780
		10	20.0 × 39.5 × 42.0	10.2	B32796G8106+000	12	30	4.9	640
		10	20.0 × 39.5 × 42.0	!	B32796E8106+000	11	30	4.9	640
		14	28.0 × 37.0 × 42.0	10.2	B32796G8146+000	15	30	3.6	440
		14	28.0 × 37.0 × 42.0	!	B32796E8146+000	14	30	3.6	440
		15	30.0 × 45.0 × 42.0	20.3	B32796G8156+000	15	30	3.0	400
		20	30.0 × 45.0 × 42.0	20.3	B32796G8206+000	19	30	2.6	400
		20	30.0 × 45.0 × 42.0	!	B32796E8206+000	18	30	2.6	400
		24	33.0 × 48.0 × 42.5	20.3	B32796G8246+000	20	30	2.5	180

MOQ = Minimum Order Quantity, consisting of 4 packing units.
Further E series and intermediate capacitance values on request.

Composition of ordering code

+ = Capacitance tolerance code:
K = ±10%
J = ±5%



B32796

MKP AC filtering

Ordering codes and packing units (lead spacing 37.5 mm)

V_{RMS}	V_R	C_R	Max. dimensions w × h × l	P_1	Ordering code (composition see below)	I_{RMS} 60 °C 10 kHz	ESL	ESR 10 kHz	Untaped pcs./
V AC	V DC	µF	mm	mm		A	nH	mΩ	MOQ
400	1050	2.7	24.0 × 15.0 × 41.5	!	B32796T4275+000	7	21	15	1040
		3.5	24.0 × 19.0 × 41.5	!	B32796T4355+000	8	23	13	780
		7.5	20.0 × 39.5 × 42.0	10.2	B32796G4755+000	11	30	5.5	640
		7.5	20.0 × 39.5 × 42.0	!	B32796E4755+000	10	30	5.5	640
		10	28.0 × 37.0 × 42.0	10.2	B32796G4106+000	14	30	4.5	440
		10	28.0 × 37.0 × 42.0	!	B32796E4106+000	13	30	4.5	440
		13	30.0 × 45.0 × 42.0	20.3	B32796G4136+000	17	33	3.5	400
		13	30.0 × 45.0 × 42.0	!	B32796E4136+000	16	33	3.5	400
		16	33.0 × 48.0 × 42.5	20.3	B32796G4166+000	18	33	3.5	180

MOQ = Minimum Order Quantity, consisting of 4 packing units.
Further E series and intermediate capacitance values on request.

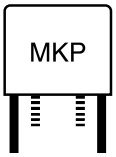
Composition of ordering code

+ = Capacitance tolerance code:
K = ±10%
J = ±5%

Technical data

Reference standard: IEC 61071, EN 61071, VDE 0560-120

Operating temperature range (case)		Max. operating temperature, $T_{op,max}$ +105 °C Upper category temperature T_{max} +85 °C Lower category temperature T_{min} –40 °C Note: At T > 85 °C de-rating for V_{RMS} (V AC) should be 1.5%/°C
Capacitance drift in range (! 40 °C, ! 85 °C)		2% respect the value measured at reference conditions
Insulation Resistance R_{ins} given as time constant $\tau = C_R$ " R_{ins}, rel. humidity ≤ 65% (minimum as-delivered values)		30 000 s
Test voltage between terminals		1.5 " V_R for 10 s 1.65 " V_R for 2 s
Test voltage terminal case (10 s)		2 " V_{RMS} + 1000 V AC (min. 2000 V AC) at 50 Hz
Maximum permissible overvoltage for short operating periods (max 1 min/day)		1.3 " V_{RMS}
Maximum peak current (A)		$I_{P,max} = C_R \cdot \frac{dV}{dt}$
Damp heat test Limit values after damp heat test		56 days/40 °C/93% relative humidity Capacitance change | ΔC/C | ≤ 5% Dissipation factor change Δ tan δ ≤ 1.5 · 10^{-3} (at 1 kHz) Insulation resistance R_{ins} ≥ 50% of minimum as-delivered values
Change of temperature		In accordance with IEC 60068-2-14 (Test Nb)
Reliability:	Failure rate λ	300 fit
	Service life t_{SL}	> 60 000 h at V_{RMS}, 60 °C For conversion to other operating conditions, refer to chapter "Reliability" on page 439 from Data Book 2009.
	Failure criteria:	
	Total failure	Short/open circuit
	Failure due to variation of parameters	Capacitance change | ΔC/C | ≥ 10% Dissipation factor change Δ tan δ > 4 · upper limit value Insulation resistance R_{ins} < 1500 MΩ (C_R≤0.33µF) or time constant $\tau = C_R \cdot R_{ins}$ < 500 s (C_R>0.33µF)



Pulse handling capability

"dV/dt" represents the maximum permissible voltage change per unit of time for non-sinusoidal voltages, expressed in V/µs.

Note:
The values of dV/dt provided below must not be exceeded in order to avoid damaging the capacitor.

Lead spacing	27.5 mm				37.5 mm				52.5 mm			
Type	B32794				B32796				B32798			
V_{RMS} (V AC)	250	300	350	400	250	300	350	400	250	300	350	400
	dV/dt in V/µs											
	27	31	39	47	19	21	26	32	12	14	18	21

Notes: Please take all additional data not mentioned above from our Data Book 2009

G

Article

Optimal topology for a three port PV-EV-Grid 10 kW power converter

Albert Bassa de los Mozos[1], Gautham Ram Chandra Mouli[1] and Pavol Bauer[1]
[1]Electrical Sustainable Energy, Delft University of Technology, Delft, The Netherlands

This paper presents a comparison of topologies to build a multiport converter which performs both Electric Vehicle (EV) charging and Photovoltaic (PV) energy production. The three port converter must be able to charge the battery from both the grid and solar power, and inject current to the grid from both the solar array and the EV battery, allowing Vehicle to Everything (V2X) operation. A literature review is performed to determine the optimal candidates and a framework is created to evaluate all the topologies. Then, the used analytical loss model and the design and selection procedure of the components of each converter are explained. Finally, each converter is designed and evaluated using the predefined comparison framework.

***Index Terms*—Power Electronics, Photovoltaics, Electric Vehicles, Charger, Topologies, Multiport Converter, Comparison, Grid.**

I. Introduction

THE method which is used to find the optimal topology of the Multiport Converter (MPC) is presented in Figure 1 [1], and followed for every topology that is to be compared. Matlab is used in order to run the analytical models. A script is written for each topology: from the requirements, the steady state equations and the loss models the final design and rating of each converter is obtained.

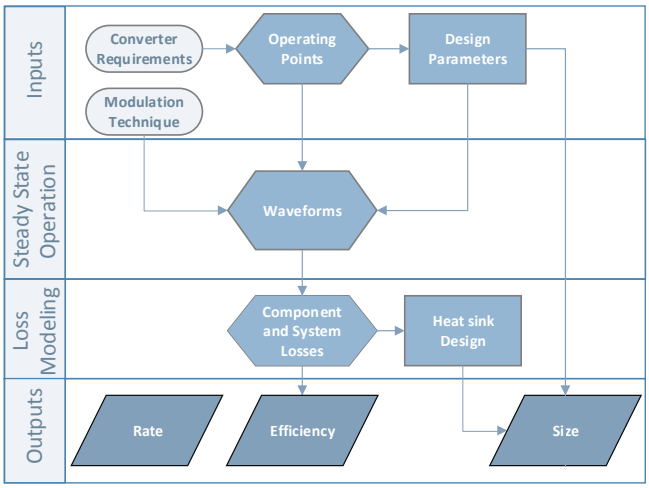


Fig. 1: Overview of the methodology used to rate every topology.

The following characteristics are expected of the MPC:

- High efficiency
- High power density
- Low number of elements (simplicity)
- Uses SiC semiconductors (CREE)
- Meets all standards requirements
- Printed Circuit Board (PCB) mountable elements (E65 core max)
- Semiconductor junction temperatures below 100°C

II. System Architecture

Three different system architectures can be adopted for the construction of the multiport converter. The first architecture

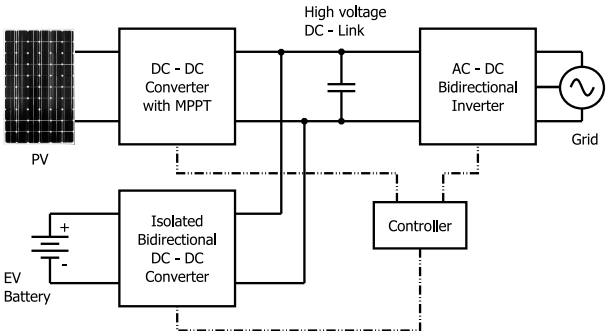


Fig. 2: Block diagram of a three-port converter with a DC Link.

TABLE I: Advantages and disadvantages of the DC link architecture.

Advantages	Disadvantages
Micro grid ready	More components
Easy to implement	Big capacitor as DC link
Expandable	Three different controls
Simple port based control	
Modularity	

is based on a DC link, as shown in Figure 2, which acts as an energy buffer between the ports.

In this case each converter has a different control algorithm, which depends on the topology. The advantages and disadvantages of relying in a common DC Link are listed in Table I.

The second multiport converter architecture is based in two converters, one of which has the ability to control both the input and the output, as displayed in Figure 3. This converter has an inherent variable voltage DC Link which can be used to connect the converter for the EV charging. This converters rely on an impedance network at the input which is able to boost the DC voltage input. The characteristics of this architecture are found on Table II.

The last structure consists in using a common AC link [2], see Figure 4. This structure isolates the three ports of the converters, relying on a central High Frequency Transformer

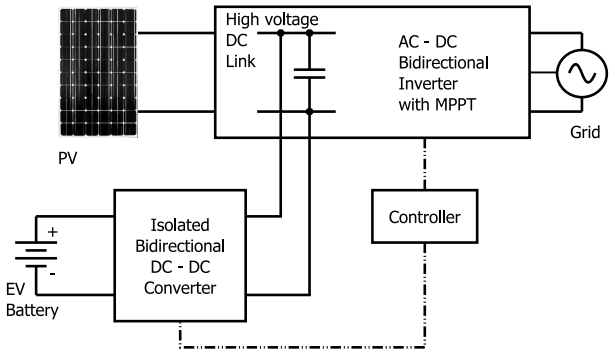


Fig. 3: Block diagram of a three-port converter with an impedance network.

TABLE II: Advantages and disadvantages of the Impedance Network based architecture.

Advantages	**Disadvantages**
Reduced active components	High currents
Increased reliability	Increased control complexity
Two different controls	Not easily expandable
No dead-time necessary	Variable DC link voltage

(HFT) which exchanges energy between the ports. Table III shows how the disadvantages of this type of converter outnumbers the advantages. Moreover, isolation between photovoltaic panels and the grid is not strictly required by the European standards. Therefore, this architecture is not considered in this work.

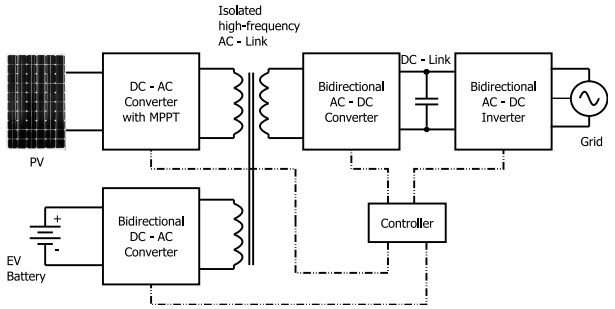


Fig. 4: Block diagram of a three-port converter with an inner AC link.

TABLE III: Advantages and disadvantages of the AC link architecture.

Advantages	**Disadvantages**
Isolation between all ports	High complexity
	HFT with three windings
	Difficult to control
	Little research on it
	Non modular
	Non expandable
	DC Link still necessary

III. Comparison framework

A framework is created in order to rate the different candidates and make the comparison well-founded. The framework has been adapted from Todorčević's work [3], where four topologies were compared. The comparison criteria are explained in terms of importance and given a weight factor. The comparison is done in such way that each criterion carries its own weight factor W_j. The topologies are rated from one (worst) to five (best) for each criterion and then the rating r_{ij} is multiplied by the weight factor of the particular criterion. The total rating $T_{rating,i}$ is given by

$$T_{rating,i} = \sum_{j=1}^{N_{cri}} W_j r_{ij} \tag{1}$$

Where i is an ordinal number which refers to the topology, j is an ordinal number referred to the criterion and N_{cri} the total number of criteria. The converter with the highest rating is the best suited for the given requirements and application.

A. Number of switches

A high number of active components increases the complexity of the system and reduces the reliability. It is identified as criterion number one and has a weight of 3:

TABLE IV: Number of switches n $[j = 1, W_1 = 3]$

Rating	1	2	3	4	5
PV	$n \geq 6$	n=5	n=4	n=3	$n \leq 2$
Grid	$n > 15$	$12 < n \leq 15$	$9 < n \leq 12$	$6 < n \leq 9$	$n \leq 6$
EV	$n > 18$	$14 < n \leq 18$	$10 < n \leq 14$	$6 < n \leq 10$	$n \leq 6$

B. Number of diodes

The number of diodes has to be taken into account, as it affects the cost of the converter. They have a weight of one as they are non controlled elements and therefore the system complexity increase is lower.

TABLE V: Number of diodes n $[j = 2, W_2 = 1]$

Rating	1	2	3	4	5
PV	$n \geq 6$	n=5	n=4	n=3	$n \leq 2$
Grid	$n > 15$	$12 < n \leq 15$	$9 < n \leq 12$	$6 < n \leq 9$	$n \leq 6$
EV	$n > 12$	$8 < n \leq 12$	$4 < n \leq 8$	$0 < n \leq 4$	n=0

C. Number of magnetic elements

The higher the number of necessary cores, the higher the manufacturing complexity. The number of cores of the grid port is not evaluated, as LCL filters are used for all topologies.

TABLE VI: Number of cores n $[j = 3, W_3 = 3]$

Rating	1	2	3	4	5
PV	$n \geq 6$	n=5	n=4	n=3	$n \leq 2$
EV	$n \geq 8$	$6 < n \leq 8$	$4 < n \leq 6$	$2 < n \leq 4$	$n \leq 2$

D. Number of capacitors

The different topologies may require different number of capacitors due to different current ripples and their equivalent frequency. A weight of one is given because film capacitors are used and have a low impact in the system's reliability.

TABLE VII: Number of capacitors n $[j = 5, W_5 = 1]$

Rating	1	2	3	4	5
PV	$n \geq 6$	n=5	n=4	n=3	$n \leq 2$
EV	$n \geq 6$	n=5	n=4	n=3	$n \leq 2$
Grid	$n \geq 6$	n=5	n=4	n=3	$n \leq 2$

E. Efficiency

Converter efficiency is the most important criterion; therefore, it has a weight of 5. A converter with lower losses might result in a lower final size because of reduced cooling needs. Weighted efficiencies like the European Efficiency [4] are computed for this purpose.

TABLE VIII: Efficiency η [%] $[j = 6, W_6 = 5]$

Rating	1	2	3	4	5
PV	η<98.0	98.0 $\leq\eta$<98.5	98.5 $\leq\eta$<99.0	99.0 $\leq\eta$<99.5	$\eta \geq$99.5
Grid	η<97.5	97.5 $\leq\eta$<98.0	98.0 $\leq\eta$<98.5	98.5 $\leq\eta$<99.0	$\eta \geq$99.0
EV	η<97.0	97.0 $\leq\eta$<97.5	97.5 $\leq\eta$<98.0	98.0 $\leq\eta$<98.5	$\eta \geq$98.5

F. Volume of the converter

This criterion involves the size of the main power elements of the converter: the cooling system, the electromagnetic parts and the capacitors. As maximum power density is wanted, the weight of this criterion is 5.

TABLE IX: Converter volume V_c [dm^3] $[j = 7, W_7 = 5]$

Rating	1	2	3	4	5
PV	V_c>0.6	0.5$\leq V_c$<0.6	0.4$\leq V_c$<0.5	0.3$\leq V_c$<0.4	V_c<0.3
Grid	V_c>0.9	0.75$\leq V_c$<0.9	0.6$\leq V_c$<0.75	0.45$\leq V_c$<0.6	V_c<0.45
EV	V_c>1.5	1.3$\leq V_c$<1.5	1.1$\leq V_c$<1.3	0.9$\leq V_c$<1.1	V_c<0.9

G. Leakage currents

Leakage currents are an important aspect which concerns grid-tied photovoltaic installations with transformerless converters. The rating of the converter is with respect to the *DIN VDE 126-1-1* standard, where a maximum leakage requirement of 30 mA current is established; otherwise, the converter has to disconnect from the grid [5].

TABLE X: Leakage $[j = 8, W_8 = 2]$

1	2	3	4	5
High	Outside Limits	Inside limits	Minor	None

H. Current ripple in EV battery

As EV charging standards require isolated topologies [6], EV charging usually has high current ripples at the DC output. The amplitude of this ripple must be limited in order to improve battery life of the cars [7].

TABLE XI: Current ripple I_{pp} [A] $[j = 9, W_9 = 4]$

1	2	3	4	5
I_{pp} >50	40<I_{pp} $\leq$50	30<I_{pp} $\leq$40	20<I_{pp} $\leq$30	0<I_{pp} $\leq$20

I. Efficiency improvement

The possibility of increasing the efficiency is evaluated by the possibilities of implementing better modulation techniques and the use of snubbers or extra circuitry to implement Zero Voltage Switching (ZVS). The rating of this parameter depends on how difficult it is to achieve the efficiency improvement in the converter and the final efficiency increase:

TABLE XII: Efficiency improvement $[j = 10, W_{10} = 1]$.

1	2	3	4	5
futile	hard to implement	doable	minor problems	easy

J. Controllability

Controllability addresses the control complexity of a given topology, as well as how hard is it to properly operate the converter. It has a weight of 3:

TABLE XIII: Controllability $[j = 11, W_{11} = 3]$

1	2	3	4	5
unknown	solvable	hard	minor problems	easy

IV. Loss modeling and design

The dissipated power of the passive and active components of each converter must be known in order to perform low loss designs, calculate the efficiency and design the cooling system. In active components the losses depend on the junction temperature, which is unknown in the first instance. The losses are calculated iteratively in order to find the junction temperatures in every operating point.

A. Switches

The losses in the SiC mosfets consist of conduction losses, switching losses and gate losses:

$$P_{sw} = P_{sw,con} + P_{sw,on} + P_{sw,off} + P_{sw,gate} \qquad (2)$$

The switch conduction losses on a SiC Mosfet depend on the drain-source on-state resistance R_{DS} and the RMS current through it $I_{DS,rms}$ [8]:

$$P_{sw,con} = I^2_{DS,rms} R_{DS}(I_{DS}, T_j, V_{GS}) \qquad (3)$$

Where R_{DS} depends on the drain-source current I_{DS}, the junction temperature T_j and the voltage applied at the gate V_{GS}. The higher the gate voltage, the wider the channel of the semiconductor and the lower the series resistance. The resulting R_{DS} is obtained by curve fitting from the Mosfet datasheet. The switching losses are a result of the simultaneous presence of voltage and current in the Mosfet during transitions. The E_{on} and E_{off} switching losses are found as [8]:

$$\begin{aligned} P_{sw,on} &= f_{sw} E_{on}(V_{DS}, I_{DS}, T_j) \\ P_{sw,off} &= f_{sw} E_{off}(V_{DS}, I_{DS}, T_j) \end{aligned} \tag{4}$$

Being f_{sw} the switching frequency of the power semiconductors. Equation 4 shows that both energies depend on V_{DS}, I_{DS} and T_j. The switching energies dependence on V_{DS} is roughly directly proportional to the drain source voltage applied.

Figure 5 shows the parasitic capacitances of a power mosfet, which are a source of losses. At turn off both the drain to source capacitance C_{ds} and gate to drain capacitance C_{gd}, which form the parasitic output capacitance C_{oss}, are charged. At turn on this energy is burned and losses and heating occur. When ZVS occurs, the body diode is conducting and the current is oriented from source to drain, discharging the C_{oss} and reducing turn on losses. The E_{oss} energy depending on V_{DS} is given in the datasheet. Therefore, in ZVS topologies, this energy has to be subtracted from the E_{on} and E_{off}.

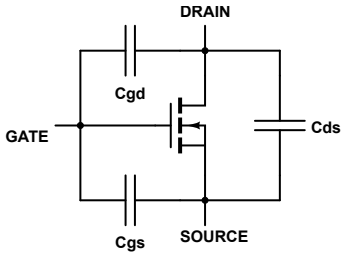


Fig. 5: Power mosfet parasitic capacitances

Gate losses are low compared to conduction losses and switching losses, and are related to the energy required to energize with the gate charge Q_g the parasitic capacitance C_{gs} shown in Figure 5 [9]:

$$E_{gate} = \frac{1}{\eta_{Drivers}} Q_g \Delta V_{GS} \tag{5}$$

Where $\eta_{Drivers}$ is the efficiency of the driving circuit, assumed to be 90%, and ΔV_{GS} is the voltage swing applied to the gate of the mosfet. The power loss $P_{sw,gate}$ is E_{gate} times the switching frequency.

In order to find the optimal switch for each topology, the worst case operating point is considered in multiple switches that satisfy voltage and current requirements. The switch which yields lower losses is selected for the topology. This method does not prioritize the maximum overall efficiency but minimizes the maximum power dissipation, reducing the cooling system size.

B. Diodes

SiC schottky diodes present low forward voltage when conducting and virtually no switching losses. The forward characteristics can be modeled as a temperature dependent forward voltage V_T and a series resistor R_T, which depend on the junction temperature and forward current:

$$\begin{aligned} V_{fT} &= V_T(T_j) + I_{f,rms} R_T(T_j) \\ P_{d,con} &= V_{fT}(T_j, I_{f,rms}) I_{f,rms} \end{aligned} \tag{6}$$

Where $I_{f,rms}$ is the RMS value of the current through the diode. V_T and R_T values are obtained via equations found in the datasheets. When switching off a Schottky diode, only a small displacement current for charging the junction capacitance of the diode is observed [10]. This charge is very small compared to the reverse recovery charge (Q_{rr}) of conventional diodes. This switching off energy E_c depends on the reverse voltage applied to the diode:

$$P_{d,off} = V_R E_c(V_R) f_{sw} \tag{7}$$

Therefore, the total losses of one diode are obtained using Equation 8. The optimal diode for each topology is found using the same method as for the switches.

$$P_d = P_{d,con} + P_{d,off} \tag{8}$$

C. Magnetic elements

Magnetic elements like power inductors or transformers are formed by a magnetic material core and copper windings. Copper losses are obtained as:

$$P_{copper} = R_{ac,wire} I_{l,rms}^2 \tag{9}$$

Where $R_{ac,wire}$ is the resistance of the copper and $I_{l,rms}$ the current. The core losses depend on the material used, the magnetic flux in the core and the frequency. Core manufactures usually give the Steinmetz-equation parameters (k, α and β), used in the conventional Steinmetz-equation. However, this parameters are obtained with sinusoidal currents, not piecewise linear currents as in DC-DC converters. The Improved Generalized Steinmetz Equation (iGSE) method [11] presents an improved Steinmetz-equation for piecewise linear waveforms:

$$P_v = \frac{k_i \left(\Delta B\right)^{(\beta-\alpha)}}{T} \sum_m \left| \frac{B_{m+1} - B_m}{t_{m+1} - t_m} \right|^{\alpha} (t_{m+1} - t_m) \tag{10}$$

$$k_i = \frac{k}{(2\pi)^{(\alpha-1)} \int_0^{2\pi} |cos\theta|^{\alpha} 2^{(\beta-\alpha)} d\theta} \tag{11}$$

Simple magnetic circuit equations can be applied in order to find the flux density B, depending on the number of turns, the core and the current waveform. The total dissipated power depends on the volume of the core V_c:

$$P_{core} = V_c P_v \tag{12}$$

In the case of sinusoidal currents, as in the LCL toroidal filters, the original Steinmetz equation is used. Multiple E cores, ferrite toroids and different materials are considered, resulting in multiple possible designs. The cost of each design is computed as:

$$F_{cost,ind} = \frac{1}{2}\frac{P_{ind,loss}}{P_{ind,loss,max}} + \frac{1}{2}\frac{V_{ind}}{V_{ind,max}} \tag{13}$$

Where $P_{ind,loss,max}$ are the losses of the working design with higher losses and $V_{ind,max}$ is the volume of the inductor design with a higher volume. The inductor design with a lower F_{cost} is the optimum design in terms of losses and volume.

D. Capacitors

The capacitor losses depend on the Equivalent Series Resistance (ESR) R_{ESR}, found on the datasheet. Some topologies may require a number of series $N_{c,s}$ and paralleled $N_{c,p}$ capacitors in order to increase the rated voltage and actual capacity respectively. The total R_{ESR} is found as:

$$R_{ESR,set} = \frac{N_{c,s}}{N_{c,p}}\left(R_{ESR,nom} + \frac{DF}{2\pi f_{eq} C_r}\right) \tag{14}$$

Where f_{eq} the equivalent frequency of the capacitor current, C_r the rated capacity of the capacitor and DF the dielectric factor. With the RMS of the ripple current through the capacitors $I_{cap,rms}$ the total power losses in the set of capacitors are:

$$P_{caps} = R_{ESR,set} I^2_{cap,rms} \tag{15}$$

As different models of capacitors are considered, the optimum set of capacitors is selected with Equation 16, which minimizes final volume and PCB surface:

$$F_{cost} = \frac{1}{2}\frac{A_{set}}{A_{set,max}} + \frac{1}{2}\frac{V_{set}}{V_{set,max}} \tag{16}$$

E. High Frequency Transformer (HFT)

Copper losses in HFTs are found in a similar way as inductor losses, see Equation 9. However, in a HFT, the induced flux in the core is proportional to the voltage applied to the windings [12]. According to Faraday's law, a flux $\Phi(t)$ is produced when a $v_l(t)$ is applied:

$$v_l(t) = N\frac{d\Phi(t)}{dt} \tag{17}$$

The flux $\Phi(t)$ is distributed through the core cross-section resulting in a flux density $B(t)$:

$$\Phi(t) = \int_{A_c} B(t) dA \tag{18}$$

Finally, combining the previous equations and assuming a uniformly distributed flux through the core and a linear relationship $B = \mu H$ the flux density can be derived:

$$B(t) = \frac{1}{NA_c}\int_0^t v_l(\tau) d\tau \tag{19}$$

Using this equation, the flux waveform inside the core can be computed and the iGSE method can be applied to obtain the losses in the core of the HFT, see Equations 10 and 11. In order to choose the optimum HFT, Equation 13 is used.

F. Cooling system

The heat sink size is computed from the losses in each semiconductor and the junction temperature. The Cooling System Performance Index (CSPI) method, first proposed in [13], is used to find the heat sink volume. This index evaluates the performance per volume of a cooling device. When calculated for different commercial heat sinks, the resulting CSPIs range between 4 and 7. On the other hand, high performance cooling systems have been designed [13] [14] which achieve CSPIs of 18 and 31 for aluminum and copper heat sinks respectively, which is a major improvement with respect to market solutions. For the designs, a CSPI of 10 has been selected. The volume of the heat sink is:

$$V_S = \frac{1}{R_{th,S-a,req} CSPI} \tag{20}$$

Where $R_{th,S-a}$ is the thermal resistance of the heat sink to the ambient in kelvin degrees over watts and V_S the volume of the cooling system in liters. The necessary $R_{th,S-a,req}$ is obtained via the heat sink temperature T_S, the ambient temperature T_a and the total power that needs to be dissipated by the cooling system $P_{d,t}$:

$$R_{th,S-a,req} = \frac{T_S - T_a}{P_{d,t}} \tag{21}$$

$P_{d,t}$ is known from all the losses in the power converter. T_S is computed from the maximum temperature that the heat sink can reach and still keep all the junction temperatures below 100°C.

V. DC LINK - PV PORT CANDIDATES

There are many DC-DC topology options which can be used for energy harvesting from PV panels [15] [16]. However, not all of them are equally suitable for the purpose. For example buck converters have a discontinuous input current ripple, which highly affects Maximum Power Point Tracking (MPPT) performance. The PV port must meet following requirements:

- 350 V - 700 V 10 kW 30 A max input
- Maximum Power Point Tracking (MPPT)
- Low input ripple
- Input current ripple peak to peak $<5\%$
- Input voltage ripple peak to peak $<0.25\%$

Three different topologies have been considered for this port: the Interleaved Boost Converter (IBC) [17], shown in Figure 6, the Coupled Inductors Interleaved Boost Converter (CIIBC) [18] in Figure 7 and the Three Level Boost Converter (TLBC) [19], see Figure 8.

The IBC is based on paralleling the conventional boost converter, which allows reducing the current in each leg and therefore ohmic losses. It provides reduced EMI and high efficiency at light load, at the expense of a higher number of components and reduced reliability. The CIIBC is an improved

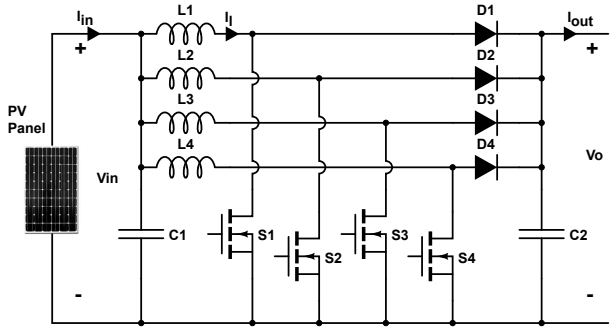


Fig. 6: Structure of a four phases IBC

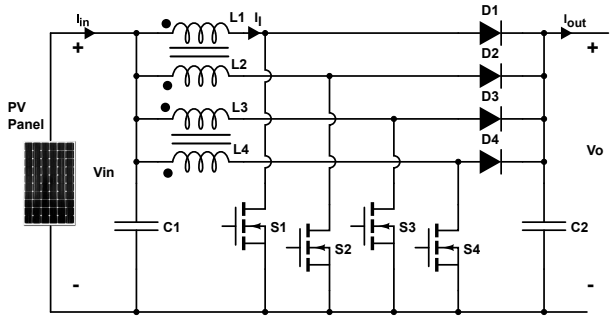


Fig. 7: Structure of a four phases CIIBC

version of the IBC which reduces the number of inductors by using coupled inductors. It reduces the overall size and it improves the regulation of power converters, and direct and reverse coupling configurations can be used to reduce input ripple or inductor ripple. Lastly, the TLBC offers the advantages of a three level topology, like reduced voltage ratings and double switching frequency at the input current. However, the output current circulates through two diodes, increasing the losses.

The design has been performed for different number of phases and of each topology and 50 and 100 kHz switching frequencies. Only the results of the configurations with higher scores are shown in Figure 9 and Figure 10: the 3 phases IBC, the 4 phases CIIBC with coupling factor -0.9 and the 2 phases TLBC, all of them switching at 50 kHz.

The final ratings of each topology considering the previously described framework are found on Table XIV. The CIIBC is the optimum topology for the PV port due to the lower number of cores and volume.

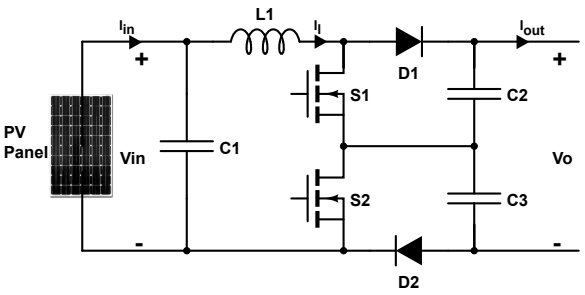


Fig. 8: Structure of a one phase TLBC

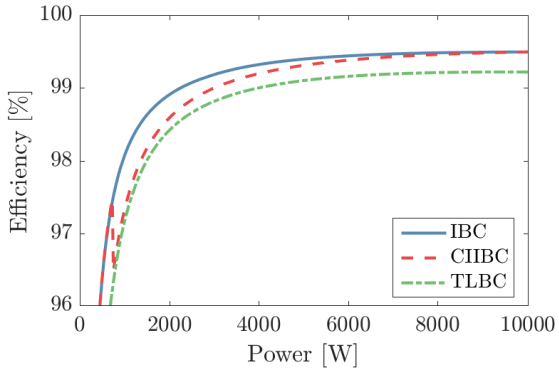


Fig. 9: Efficiency of the PV port candidates ($V_i = 500V$)

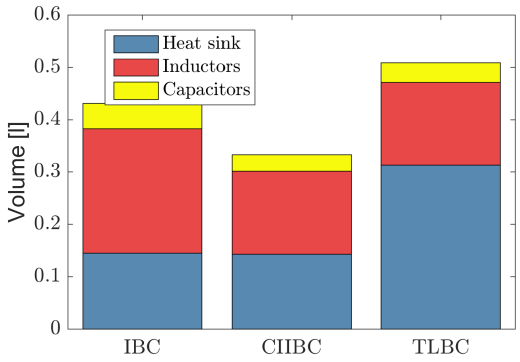


Fig. 10: Size distribution of the PV port candidates

TABLE XIV: Review of the analyzed PV port converters.

Criterion	W_j	IBC 3 ph. 50 kHz		CIIBC k=-0.9 4 ph. 50 kHz		TLBC 2 ph. 50 kHz	
		V	R	V	R	V	R
Switches	3	3	4	4	3	4	3
Diodes	1	3	4	4	3	4	3
Cores	3	3	4	2	5	2	5
Caps.	1	2	5	2	5	3	4
Eff. [%]	5	99.18	4	99.04	4	98.77	3
Vol. [dm^3]	5	0.43	3	0.32	4	0.49	3
Eff. Imp.	1	-	2	-	3	-	2
Control	3	-	4	-	4	-	2
TOTAL			**82**		**87**		**69**

VI. DC LINK - EV PORT CANDIDATES

Several DC-DC isolated topologies can be selected for the purpose of charging EV batteries. For this comparison, the Dual Active Bridge (DAB) [20], shown in Figure 11, and the Interleaved Bidirectional Flyback Converter (IBFC) [21], shown in Figure 12 have been selected as possible topologies. The requirements of the EV port are:

- 200 V - 500 V isolated output
- 10 kW / 30 A max input/output
- Low output ripple
- Bidirectional (Vehicle to Everything (V2X) operation)

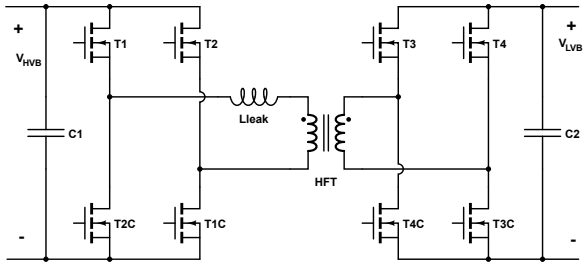


Fig. 11: Structure of the DAB

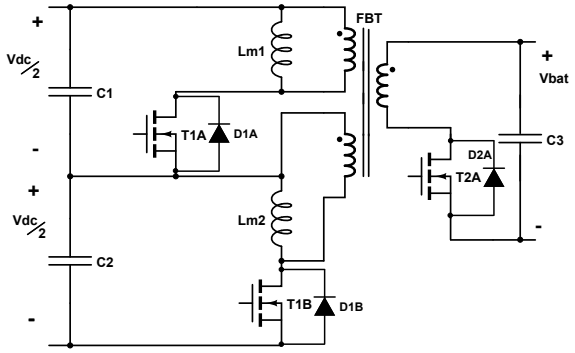


Fig. 12: Structure of the IBFC

The DAB consists of two full bridges connected via a HFT. A total of eight switches are necessary, together with the transformer and an external inductance, necessary if the transformer's leakage inductance is not enough. The DAB has inherent isolation and bidirectionality. Moreover, ZVS is possible without modifications in the High Frequency Link (HFL). It acts as an ideal current source and the control is easy to implement, but it has high current ripple both at the input and the output.

On the other hand, the IBFC consists of two or more typical flyback converters in parallel, where the secondary diode has been replaced by a switch in order to add bidirectionality. In the topology shown in Figure 12, the Flyback Transformer (FBT) has a split primary winding in order to reduce the voltage stress at the switches of the primary side. Flyback converters are typically a low power solution; therefore, a high number of phases must be considered. The HFT must be carefully designed in order to minimize the leakage inductance and reduce voltage stress at the semiconductors. The main advantage is the lower current ripple if a high number of phases is interleaved.

The design has been performed for different number of phases and 50 and 100 kHz switching frequencies. Only the configurations with higher scores are shown in Figure 13 and Figure 14: the 2 phases DAB at 100 kHz and the 4 phases IBFC which works in Discontinuous Inductor Conduction Mode (DICM) with frequency throttling. Despite the differences, both topologies score almost the same, but the IBFC is preferable due to lower current ripple in the EV battery.

VII. DC LINK - GRID PORT CANDIDATES

Two level and three level inverters have been considered for the connection of the multiport converter to the grid. The Two

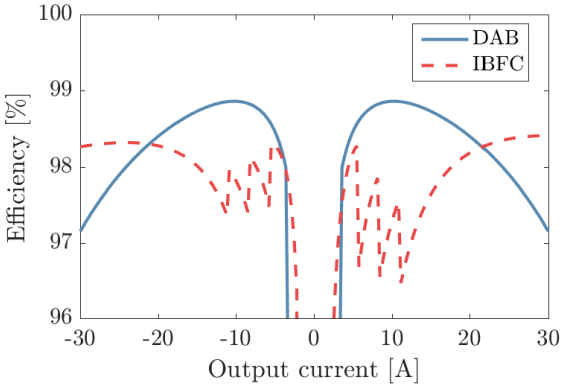


Fig. 13: Efficiency of the EV port candidates ($V_o = 332V$)

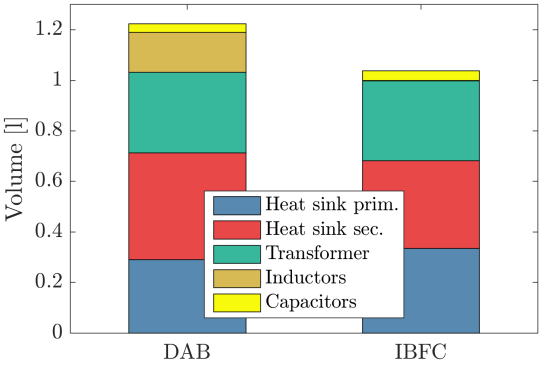


Fig. 14: Size distribution of the EV port candidates

TABLE XV: Review of the analyzed EV port converters.

Criterion	W_i	DAB 2 phases 100 kHz		IBFC 4 phases 50 kHz BCM	
		V	R	V	R
Switches	3	16	2	12	3
Diodes	1	0	5	12	2
Cores	3	3	5	4	5
Caps.	1	1	5	1	5
Eff. [%]	5	98.03	4	97.99	3
Vol. [dm^3]	5	1.22	4	1.04	4
Curr. Rip.	4	53.13	1	28.21	4
Eff. Impr.	1	-	5	-	2
Control	3	-	4	-	3
TOTAL			**89**		**90**

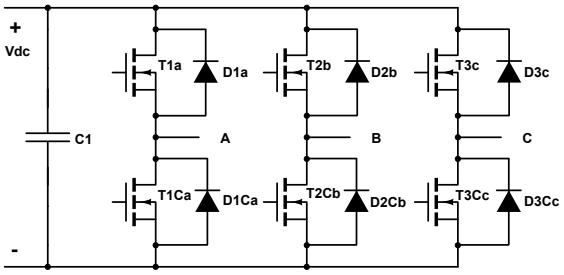


Fig. 15: Structure of the 2LC

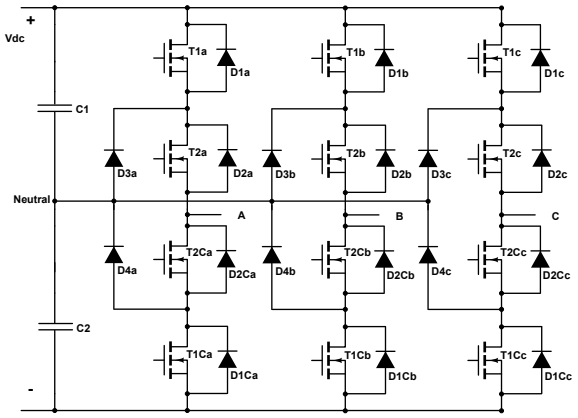


Fig. 16: Structure of the 3LNPC

Level Converter (2LC) also known as Voltage Source Inverter (VSI) [22] in Figure 15 is the simplest two level topology of a three phase inverter. It consists of six switches with the corresponding freewheeling diodes in anti parallel, as shown in Figure 15. It is the most used DC-AC topology, due to the low number of components and the low requirements of the modulation technique. However, it has a high THD and high switching losses. The requirements of the port are:

- 3 phase 400 V mains connection
- 10 kW 16 A max input/output
- Bidirectional

The Three Level Neutral Point Clamped Converter (3LNPC) [23] in Figure 16 and the Three Level T-Type Converter (3LTC) [24] in Figure 17 are three level topologies which are able to clamp the neutral of the DC bus to the output. The 3LNPC achieves the clamping through diodes while the 3LTC relies on two mosfets in series with anti parallel diodes, which allow bidirectionality. These topologies have lower output

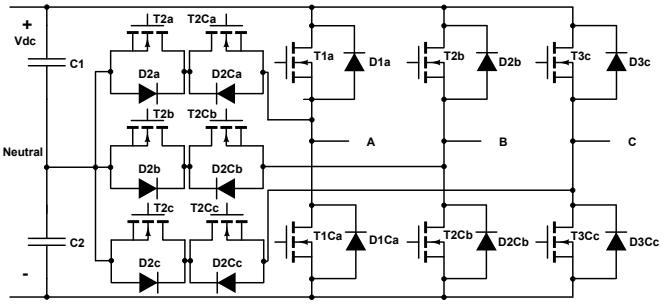


Fig. 17: Structure of the 3LTC

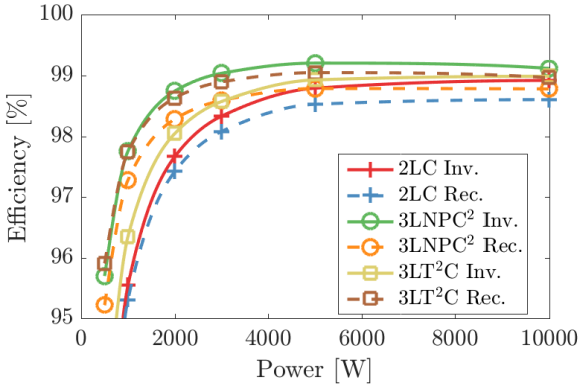


Fig. 18: Efficiency of the Grid port candidates ($V_p = 230V$)

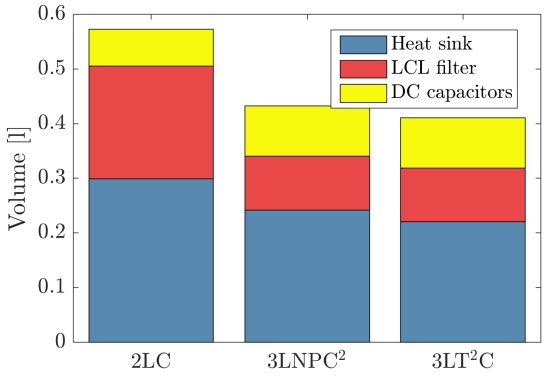


Fig. 19: Size distribution of the EV port candidates

THD and lower output ripple, at the cost of increasing the number of components and the modulation complexity. The 3LTC requires less components than the 3LNPC but has higher voltage ratings.

Each topology is designed with two different modulation techniques, Space Vector Pulse-Width Modulation (SVPWM) and a second one to reduce the leakage currents. For the 2LC Near State Pulse-Width Modulation (NSPWM) [25] is considered, which does not make use of the zero vectors and therefore reduces the voltage amplitude of the Common Mode Voltage (CMV). On the other hand, 2 Medium 1 Zero Vectors Pulse-Width Modulation (2M1ZVPWM) [26] is applied to booth three level topologies, which only uses vectors which have the same CMV.

The topologies are designed at 50 and 100 kHz switching frequencies together with the LCL filter topology, which is the same for the 3LNPC and 3LTC. The higher efficiencies and lower volume of three level topologies are shown in Figure 18 and 19, but the 2LC has a higher punctuation as it requires less components and yields a high efficiency due to the combination of 100 kHz switching frequency and NSPWM, see Table XVI.

VIII. Impedance Network Based Candidates

The quasi Z-Source Inverter (qZSI) [27] in Figure 20 is a topology derived from the traditional Z-source inverter (ZSI)

TABLE XVI: Review of the optimal configurations of the analyzed Grid port converters.

Criterion	W_i	2LC		3LNPC		3LTC	
		V	R	V	R	V	R
Switches	3	6	5	12	3	12	3
Diodes	1	6	5	18	1	12	3
Caps.	1	2	5	8	1	8	1
Eff. [%]	5	98.12	3	98.73	4	98.63	4
Vol. [dm^3]	5	0.5730	4	0.43245	5	0.4109	5
Leak.	2	-	4	-	3	-	3
Eff. Impr.	1	-	1	-	1	-	1
Control	3	-	3	-	4	-	4
TOTAL			**78**		**75**		**77**

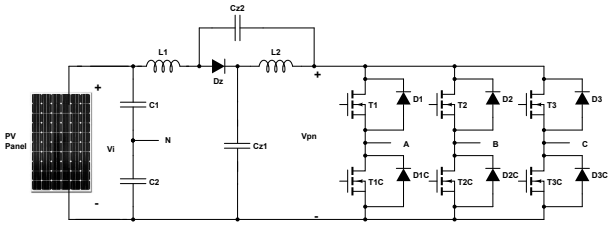


Fig. 20: Structure of the qZSI.

[28]. The requirements of this topology are those of the PV port and the Grid port. The qZSI inherits all the advantages of the ZSI, which can realize buck/boost, inversion and power conditioning in a single stage with improved reliability as no dead-time is required. In addition, the proposed qZSI has the unique advantages of lower component ratings and constant DC current from the source, which is considered a must. All of the boost control methods that have been developed for the ZSI can be used by the qZSI.

The voltages across the capacitors are constant in steady state, making the topology suitable for adding another converter, the EV port candidate. However, this voltage ranges between $\sqrt{2}\sqrt{3}V_{ph}$ = 563 V and 777 V, the inverter voltage when maximum boost is required, increasing the complexity of designing the EV port converter. The qZSI boosts the input voltage by turning on all the switches in the triple bridge, known as Shoot Through state. When the converter is not in the Shoot Through state, it is controlled like the 2LC, with SVPWM.

The main problem of the qZSI is the need of two big inductors if the current ripple limit has to be satisfied. The impedance network diodes have high currents too, twice the input current. This requires the use of 16 E65 inductors, which are configured in two parallel rows of four inductors each, and three parallel diodes which share current and losses. The efficiency of the converter is quite high, see Figure 21, but most of the losses are concentrated in the same elements resulting in a big heat sink required. The final converter volume is 4.37 liters, see the distribution in Figure 22. The final score of the converter, shown in Table XVII, is much lower than the combination of two different PV and Grid topologies.

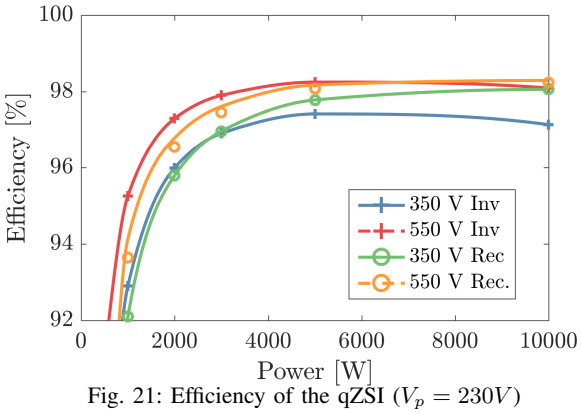


Fig. 21: Efficiency of the qZSI ($V_p = 230V$)

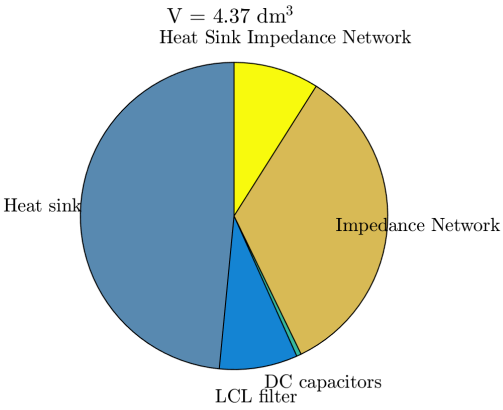


Fig. 22: Size distribution of the quasi Z-Source Inverter (qZSI).

IX. Conclusion

The optimal multiport converter topology: a four phases CIIBC at 50 kHz with reverse coupled inductors in the PV port, a four phases IBFC in the EV port in Boundary Inductor Conduction Mode (BICM) and a 100 kHz 2LC in the grid connection which uses NSPWM. Both the IBC and 2LC are extensively used topologies, therefore they should not represent any problem in terms of design, cost or manufacture. On the other hand, the IBFC is a strange topology to use in high power applications. Although it has proved to be more suitable than the DAB, careful design and testing must be done in order to manufacture appropriate FBTs, which are essential for the correct operation of the converter.

TABLE XVII: Review of the qZSI.

Criterion	W_i	V	R
Switches	3+3	6	5
Diodes	1+1	9	4
Cores	3	16	1
Caps.	1+1	11	2
Eff. [%]	5+5	97.58	4
Vol. [dm^3]	5+5	4.37	1
Leak.	4	-	3
Eff. Impr.	1+1	-	1
Control	3+3	-	3
TOTAL			**125**

REFERENCES

[1] Y. Wang, S. De Haan, and J. A. Ferreira, "Methods for experimental assessment of component losses to validate the converter loss model," in *Power Electronics and Motion Control Conference, 2008. EPE-PEMC 2008. 13th*. IEEE, 2008, pp. 187–194.

[2] H. Krishnaswami and N. Mohan, "Three-port series-resonant dc–dc converter to interface renewable energy sources with bidirectional load and energy storage ports," *IEEE Transactions on Power Electronics*, vol. 24, no. 10, pp. 2289–2297, 2009.

[3] T. Todorčević, P. Bauer, and J. Ferreira, "Comparison of bidirectional medium-voltage dc-dc converters for energy harvesting using dielectric elastomers," in *PCIM Europe*, 2013, pp. 673–680.

[4] C. Commission *et al.*, "Emerging renewables program guidebook," 2011.

[5] o. VDE VERLAG, year=2013, "Automatic disconnection device between a generator and the public low-voltage grid."

[6] I. Standard, "Electric vehicle conductive charging system - part 23: Dc electric vehicle charging station," 2016.

[7] K. Uddin, A. D. Moore, A. Barai, and J. Marco, "The effects of high frequency current ripple on electric vehicle battery performance," *Applied Energy*, vol. 178, pp. 142–154, 2016.

[8] N. Mohan and T. M. Undeland, *Power electronics: converters, applications, and design*. John Wiley & Sons, 2007.

[9] F. Krismer, "Modeling and optimization of bidirectional dual active bridge dc-dc converter topologies," Ph.D. dissertation, Diss., Eidgenössische Technische Hochschule ETH Zürich, Nr. 19177, 2010, 2010.

[10] C. Miesner, R. Rupp, H. Kapels, M. Krach, and I. Zverev, "thinq! silicon carbide schottky diodes: An smps circuit designers dream comes true!" *Technical White Paper*, 2001.

[11] K. Venkatachalam, C. R. Sullivan, T. Abdallah, and H. Tacca, "Accurate prediction of ferrite core loss with nonsinusoidal waveforms using only steinmetz parameters," in *IEEE Workshop on Computers in Power Electronics*, vol. 2002, 2002, pp. 36–41.

[12] M. H. Rashid, *Power electronics handbook: devices, circuits and applications*. Academic press, 2010.

[13] U. Drofenik, G. Laimer, and J. W. Kolar, "Theoretical converter power density limits for forced convection cooling," in *Proceedings of the International PCIM Europe 2005 Conference*, 2005, pp. 608–619.

[14] S. Lee, "Optimum design and selection of heat sinks," in *Semiconductor Thermal Measurement and Management Symposium, 1995. SEMI-THERM XI., Eleventh Annual IEEE*. IEEE, 1995, pp. 48–54.

[15] Q. Li and P. Wolfs, "A review of the single phase photovoltaic module integrated converter topologies with three different dc link configurations," *IEEE Transactions on Power Electronics*, vol. 23, no. 3, pp. 1320–1333, 2008.

[16] S. B. Kjaer, J. K. Pedersen, and F. Blaabjerg, "A review of single-phase grid-connected inverters for photovoltaic modules," *IEEE transactions on industry applications*, vol. 41, no. 5, pp. 1292–1306, 2005.

[17] S. Zhang, "Analysis and minimization of the input current ripple of interleaved boost converter," in *Applied Power Electronics Conference and Exposition (APEC), 2012 Twenty-Seventh Annual IEEE*. IEEE, 2012, pp. 852–856.

[18] B. Ray, H. Kosai, S. McNeal, B. Jordan, and J. Scofield, "A comprehensive multi-mode performance analysis of interleaved boost converters," pp. 3014–3021, 2010.

[19] M. T. Zhang, Y. Jiang, F. C. Lee, and M. M. Jovanovic, "Single-phase three-level boost power factor correction converter," in *Applied Power Electronics Conference and Exposition, 1995. APEC'95. Conference Proceedings 1995., Tenth Annual*. IEEE, 1995, pp. 434–439.

[20] M. Kheraluwala, R. W. Gascoigne, D. M. Divan, and E. D. Baumann, "Performance characterization of a high-power dual active bridge dc-to-dc converter," *IEEE Transactions on Industry applications*, vol. 28, no. 6, pp. 1294–1301, 1992.

[21] K. Venkatesan, "Current mode controlled bidirectional flyback converter," in *Power Electronics Specialists Conference, 1989. PESC'89 Record., 20th Annual IEEE*. IEEE, 1989, pp. 835–842.

[22] A. M. Hava, R. J. Kerkman, and T. A. Lipo, "Simple analytical and graphical methods for carrier-based pwm-vsi drives," *IEEE Transactions on Power Electronics*, vol. 14, no. 1, pp. 49–61, 1999.

[23] A. Nabae, I. Takahashi, and H. Akagi, "A new neutral-point-clamped pwm inverter," *IEEE Transactions on industry applications*, no. 5, pp. 518–523, 1981.

[24] M. Schweizer and J. W. Kolar, "Design and implementation of a highly efficient three-level t-type converter for low-voltage applications," *IEEE Transactions on Power Electronics*, vol. 28, no. 2, pp. 899–907, 2013.

[25] E. Ün and A. M. Hava, "A near-state pwm method with reduced switching losses and reduced common-mode voltage for three-phase voltage source inverters," *Industry Applications, IEEE Transactions on*, vol. 45, no. 2, pp. 782–793, 2009.

[26] M. C. Cavalcanti, A. M. Farias, K. C. Oliveira, F. A. Neves, and J. L. Afonso, "Eliminating leakage currents in neutral point clamped inverters for photovoltaic systems," *Industrial Electronics, IEEE Transactions on*, vol. 59, no. 1, pp. 435–443, 2012.

[27] Y. Li, J. Anderson, F. Z. Peng, and D. Liu, "Quasi-z-source inverter for photovoltaic power generation systems," pp. 918–924, 2009.

[28] F. Z. Peng, "Z-source inverter," *IEEE Transactions on industry applications*, vol. 39, no. 2, pp. 504–510, 2003.