A highly linear downconverter for on-chip linearization of digital power amplifiers

By

Gilbert Hardeman

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Supervisors:
prof.dr. L.C.N. de Vreede,
ir. D.P.N Mul

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Abstract

This work presents a highly linear quadrature down-converter topology intended for the linearization of digital Transmitters(DTX). By integrating it with a DTX, a fully integrated on-chip output-signal correction loop comes closer to its realization. The proposed down conversion architecture can measure the errors introduced by the non-linearity of the transmitter, rather than the transmitter output itself. These errors are determined by comparing the downconverted transmitter output signals with its analog ideal baseband I and Q reference signals. The reference signals are provided by low-power digital-to-analog converters(DACs), using the same IQ data input as the power DTX. This approach reduces the resolution/dynamic range requirements on the trans-impedance-amplifier (TIA) and analog-to-digital converters(ADCs) since the error signals have a reduced dynamic range compared to the transmitter's output signal itself. These lower requirements on the ADCs and elimination of off-chip couplers and filters ease the integration of a complete digital pre-distortion (DPD) correction loop in future DTX implementations.

As the core of this thesis work, a linear harmonic rejection mixer was designed. It uses resistors in its mixer branches to implement the proper currenct scaling needed for harmonic rejection (HR). The resulting HR mixer avoids the unwanted down-conversion of the higher harmonics of the DTX to the baseband frequencies of interest. Also, a trans-impedance amplifier was designed with the proposed passive mixer. These TIAs are based on an inverter topology for maximum tranconductance and were biased for optimal linearity and offered a bandwidth over 1.8GHz. The proposed DTX error-detection architecture is implemented in the current domain. Performing the subtraction before the TIA drastically reduces the voltage swing at the input of the TIA, benefiting the linearity of the mixer and reference DAC. The overall HR-mixer configuration is simulated for its linearity, yielding an IIP3 of 49dBm, which to the best of the author's knowledge, is the best-reported linearity for high bandwidth down-converting applications.

Acknowledgements

First and foremost I want to express my utmost gratitude to Prof. Leo de Vreede and Dieuwert Mul for their generous time investment into my future. We have had many lengthy discussions which led to the insights gained in this thesis project. Their passion for creative solutions is truly inspiring. The work being carried out in the ELCA group is very interesting and I am glad I could be involved. Furthermore, I want to thank Mohammad Ali Montazerolghaem for joining in meetings, his expertise on passive mixers and TIA's was of great help. I want to thank dr. Morteza Alavi, dr. Dante Muratore and John Gajardharsing for being part of my thesis committee, I sincerely hope you will find this work interesting. I also want to thank dr. Morteza Alavi specifically for inspiring me to choose this master. I want to thank Ampleon for supporting this project. Last but not least, I want to thank my girlfriend Eva, for always supporting me.

Contents

1 Introduction

The last decades have shown a rapid increase in demand for wireless data transfer. This trend is expected to continue and even accelerate, as visualized in Fig. 1.1. The increased demand can be attributed to higher data rates per device and a rapid increase of connected devices.

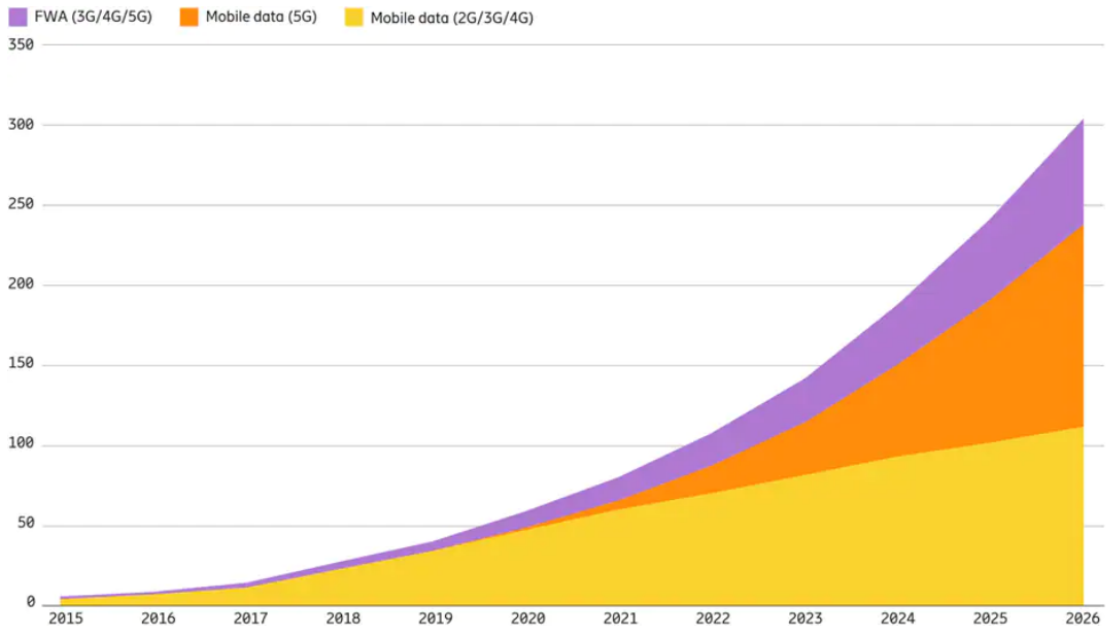

Figure 1.1: Global mobile network data traffic (EB per month) [1]

The fifth-generation cellular networks(5G) take a multifaceted approach to cope with the increased data demands. Namely, the data rates are increased using higher-order modulation schemes and by increasing the signal bandwidth. The latter is enabled by shifting to higher operating frequencies where more bandwidth is available. Unfortunately, transmitted signals fade more quickly over distance at these higher frequencies, especially when objects are in the way. Beamforming is used in 5G to overcome path losses, while massive multiple-input and multiple-output (mMIMO) techniques utilize different transmission paths to increase data capacity. Beamforming is based on the coherent summation of mulitple transmit/receive signals to reach an increased antenna gain in a specific direction(Fig. 1.2). Finally, there is a trend of using smaller wireless cells at these high frequencies, allowing the re-use of frequencies in a network.

The above mentioned techniques increase the total number of required transmitters dramatically, while transmitter efficiency tends to worsen due to the higher operating frequencies and more stringent linearity requirements. Consequently, a new type of transmitter is needed to limit the energy consumption of 5G systems while offering higher integration at lower costs.

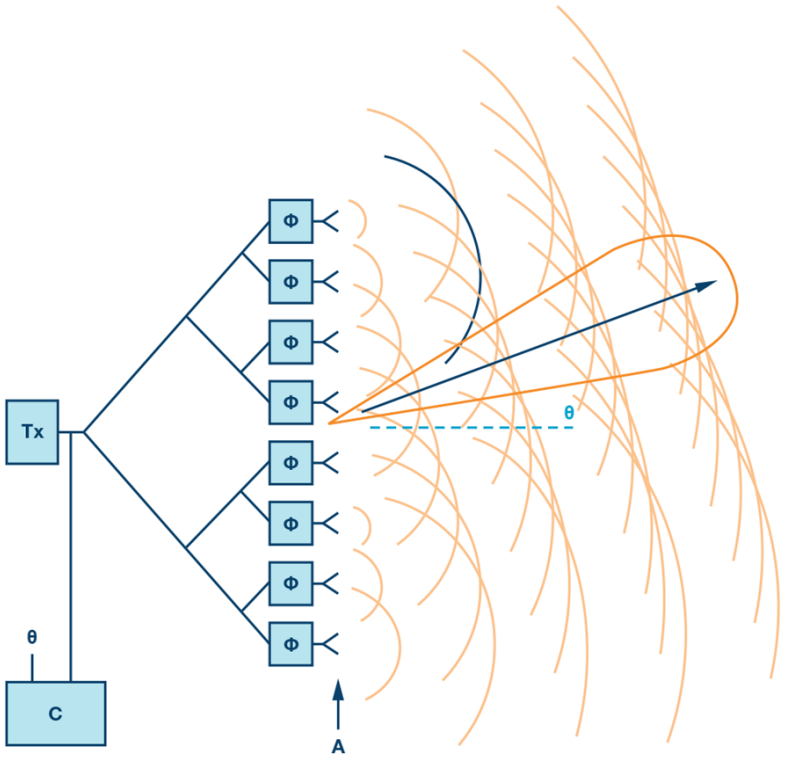

Figure 1.2: Beamforming using the coherent addition of many transmit paths [2]

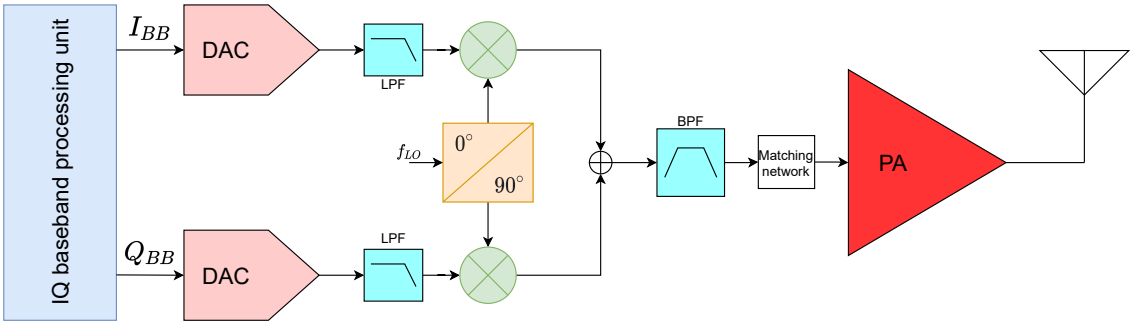

Figure 1.3: Traditional Analog Cartesian TX line-up

1.1 Digital Power amplifiers

Today's commercial base station implementations employ analog PA's(power- amplifiers), resulting in poor integration and high static power dissipation of the TX line-up. An illustration of a traditional Analog Cartesian TX line-up is shown in Fig. 1.3. The figure shows that the conversion from the digital to analog is already done in baseband. Consequently, all subsequent filtering, upconversion, summing, and amplification, are done in the analog domain. The digital-to-analog-converter(DAC), upconverter, and PA are mostly implemented in separate IC's since they use different technologies.

Typically, the most power-hunger component in a transmitter is the PA. There are several reasons for this; namely, designers must operate their PAs below their maximum output power rating(Power-backoff) to meet wireless linearity requirements, lowering their efficiency. Furthermore, an analog PA cannot be-fully turned-off for linearity reasons and should have at all times a quiescent current resulting in a relatively

high static power dissipation. The increased linearity requirements have degraded the energy efficiency of a single TX line-up. Consequently efficiency enhancement schemes like Doherty [3] need to be applied to improve the average efficiency of a TX line-up. However, Doherty transmitters use multiple RF signal paths to achieve load modulation, yielding challenges in providing the optimum drive signals to the main and peak output stages. For practical designs, this results in bandwidth, linearity and efficiency limitations. Digitally controlled power "amplifiers" are perfectly adjustable for their input conditions and, as such, are excellent candidates to implement the branch amplifiers of a Doherty configuration. In addition, they offer higher integration at reduced power consumption. In handsets, digital amplifiers have already been investigated [4]. These implementations benefit directly from the scaling of CMOS technology. However, high-power base stations require dedicated technologies such as LDMOS or GaN, complicating the development of fully integrated digital transmitters.

The ELCA group, together with its industry partners, specifically Ampleon, are integrating a complete digital-intensive transmitter for base-station applications. A simplified schematic of a cartesian Radio-Frequency-Digital-to-Analog-converter (RFDAC) is shown in Fig. 1.4. The input bits are individually fed to an upconverter, implemented by an AND gate. The AND gates drive current sources that are implemented in a high-power LDMOS technology. In an analog PA, the input voltage sets the output current through the g_m of the power device. In the proposed digital PA, the output power is set by the number of current sources that are turned on. The output current is converted to a voltage by the load impedance. Compared to an analog approach, one source of non-linearity is eliminated, namely the transistor's non-linear I_D/V_{GS} characteristic. In turn, the RFDAC's linearity is limited by its current sources' mismatch and limited output impedance. The non-linearity caused by mismatch can be reduced by using unary bits. However, every unary bit needs a driver circuit and interconnect. Consequently, a trade-off has to be made regarding hardware complexity, unary/binary bits, and the aimed resolution.

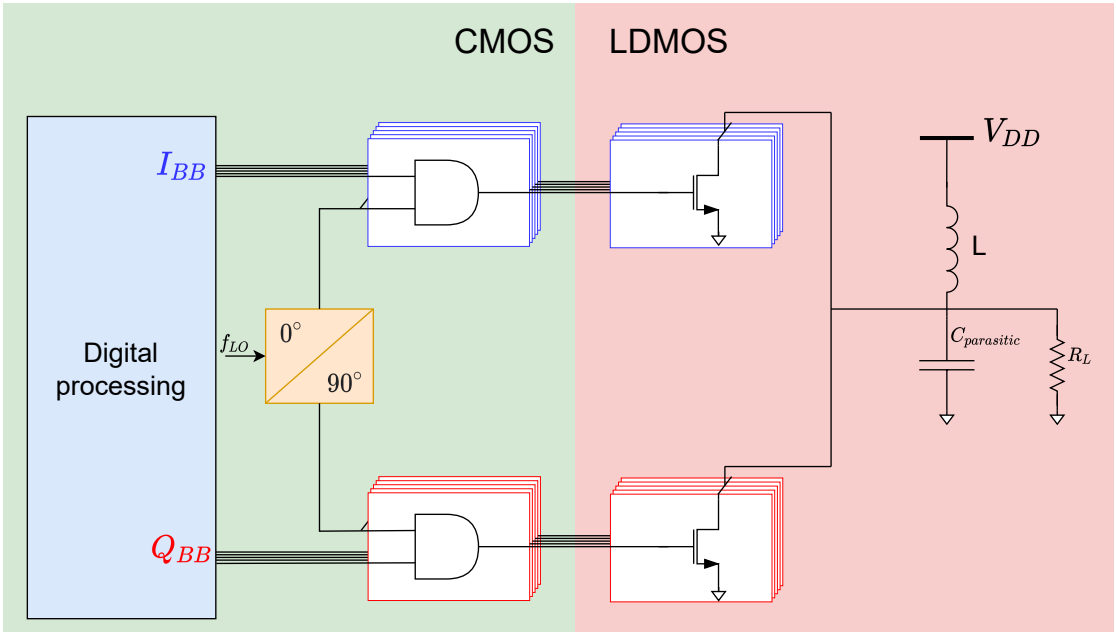

Figure 1.4: Cartesian RFDAC

Combinations of square waves drive the RFDAC. As a result, the output spectrum contains many harmonics, particularly at odd multiples of the carrier(assuming a push-pull combination). Figure 1.5 shows a simplified estimate of the output spectrum of the RFDAC. The signal of interest is around a carrier of 3.5GHz, and the most prominent harmonics/spurs appear 10.5GHz and 17.5GHz.

The intended bandwidth of the output signal is 400MHz, composed of an upconverted 200MHz In-phase(I_{BB}) signal and a 200MHz Quadrature-phase(Q_{BB}) signal. The transmitter has an aimed linearity of 50dB, meaning that the intermodulation components must be 50dB below the signal of interest. The

linearity specification is based on the 3GPP for documentation for LTE that gives a minimum Adjacent-channel-leakage-ratio(ACLR) of -45dBc [5].

The RFDAC has an RLC output network, as shown in Fig. 1.4. The inductor at the output provides the DC from the voltage source to the output stages and resonates out the parasitic output capacitance of these segmented output stages. The value of the output capacitance follows from the demanded transmitters output power, and the size of the output stage(s) need to provide this amount of power. Namely, the amount of output capacitance per watt for a given technology sets this output capacitance. The output network will bandpass filter the output. In this thesis work, the filtering at the output stage is estimated using a simple simulation, the result is shown in Fig. 1.6. Markers point out: the carrier frequency, the -3dB frequency, and the odd harmonics. The filtering of the output network is expected to be around 17dB at 10.5GHz. Combined with the fact that the third harmonic of a (50% duty cycle) square wave is about 10dB weaker than its fundamental, the signal content at 10.5GHz is expected to be about 25-27dB weaker than the fundamental content at 3.5GHz. The final output network might look different, but the filtering will be approximately the same.

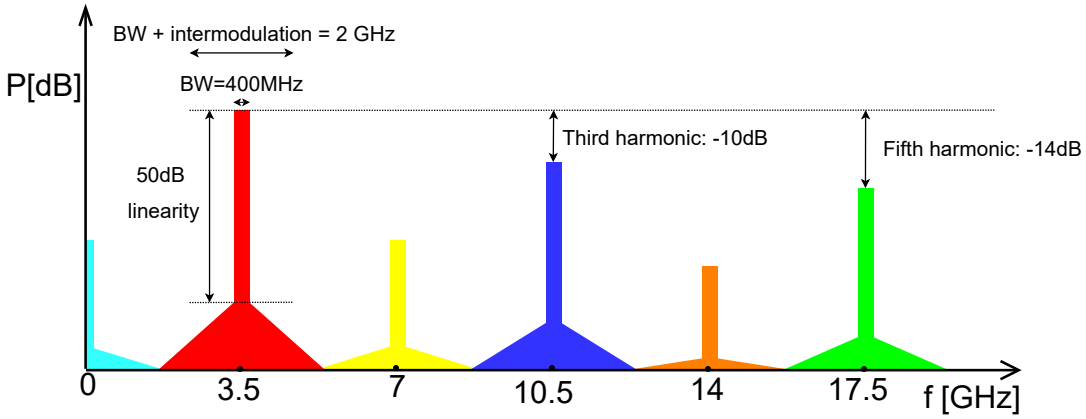

Figure 1.5: Simplified output spectrum RFDAC

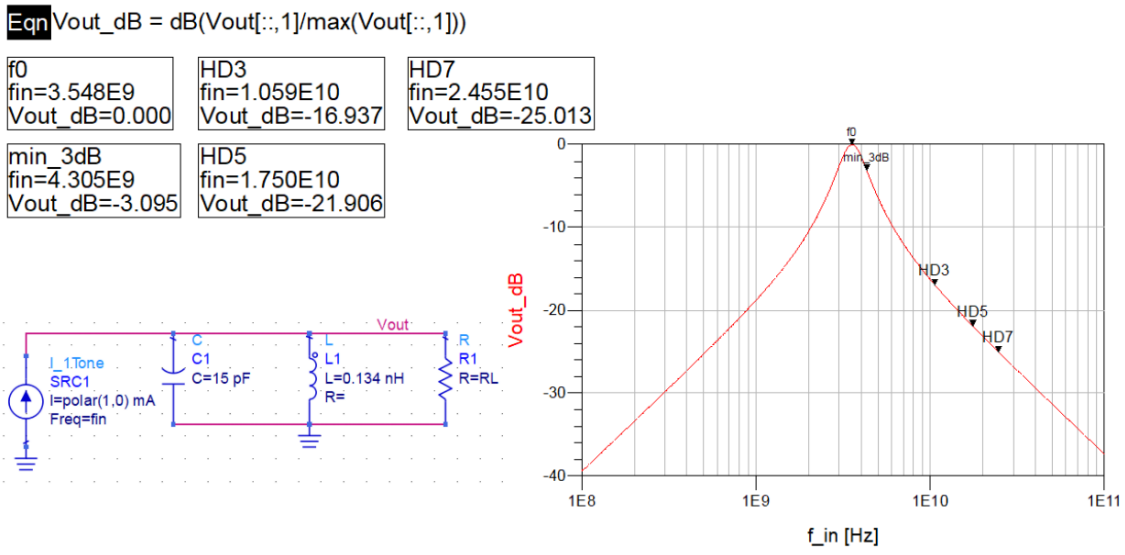

Figure 1.6: Simulation of RLC output network

1.1.1 Flip-chip

A first implementation that proves the concept has been shown in [6]. Measurements show indeed a significantly improved static power dissipation. Figure 1.7 shows a photograph of the first implementation. The drivers in the CMOS chip are connected to the LDMOS segments through bond wires. Unfortunately, the mutual coupling of the bond wires, among other things, limited the Differential-non-linearity(DNL). The currently developed system uses a flip-chip approach, with the CMOS-chip directly flip-chip mountend on top of the LDMOS chip. An artist impression of the flip-chip Digital-TX is shown in Fig. 1.8. Now the interface will have fewer parasitics, and the increased number of interconnects will allow more unary bits. The proposed flip-chip enables the complete integration of the high-power transmitter.

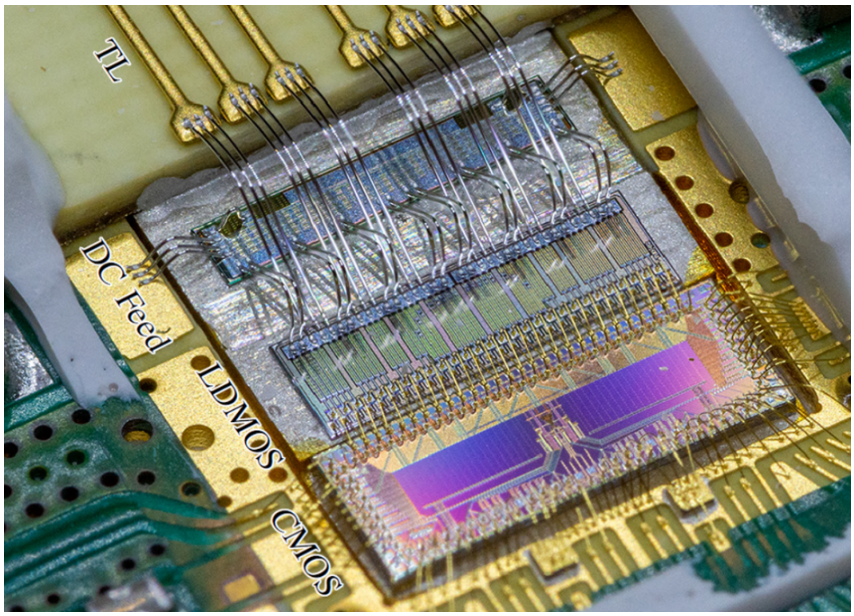

Figure 1.7: World's first high power DAC with $P_{out} > 10W$ [6]

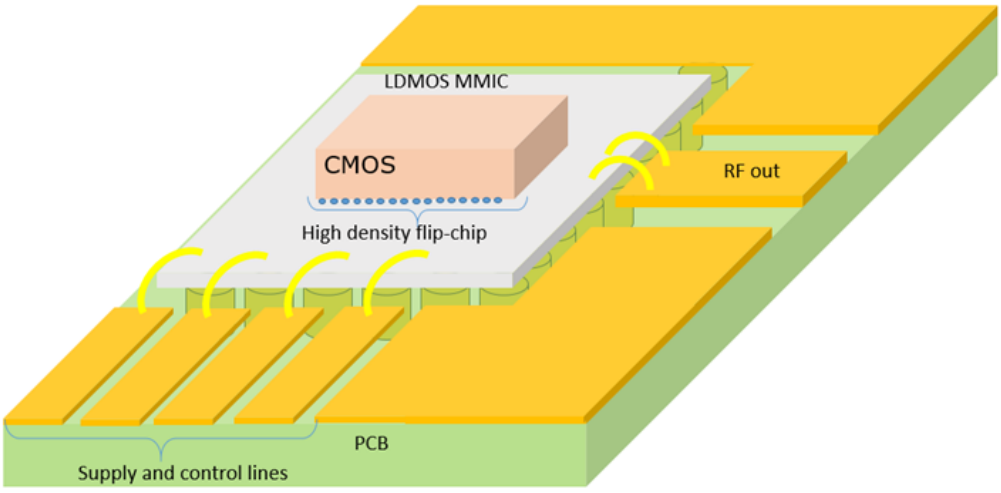

Figure 1.8: Artist impression power DTX using flip-chip connections

1.2 Digital pre-distortion

Power amplifiers have a linearity-efficiency trade-off. Digital pre-distortion (DPD) aims to improve this trade-off by pre-processing in the digital domain, compensating for the PA's non-linearities. Using DPD, an efficient non-linear PA can be made more linear. Figure 1.9 shows an illustration of a simplified typical pre-distortion system [7]. The DPD could use the information from a complete characterization of the PA under all possible conditions, but more practical is using a feedback loop. The DPD builds a model of the non-linear PA and adjusts its transfer function until the output of the PA meets the linearity specifications. A transmitter setup including DPD is shown in Fig. 1.10.

The observation receiver (ORX) uses a down-conversion mixer, mainly because operations like filtering and analog to digital conversion can be done more efficiently at lower frequencies. The DPD works best when the ORX has a larger dynamic range than the transmitter. Therefore, the mixer and ADC need to be highly linear.

In this project, the transmitter generates many harmonics. A harmonic rejection mixer has to be used to avoid the down-conversion of higher harmonics to the baseband. The design of a harmonic rejection mixer is the topic of chapter 3.

The difficulty with the architecture of Fig. 1.10 arises when considering the requirements of the Analog-to-Digital Converter(ADC). To judge the distortion of the PA, we are interested in the output signal, including its intermodulation products. It are the non-linearities of the PA that cause these intermodulation components.

At the output of the RFDAC the input signal is at RF, and therefore, the bandwidth is 400MHz. The 3^{th} and 5^{th} order intermodulation will expand the modulation bandwidth with a factor 5, so the total bandwidth will be expanded to 2GHz, as indicated in Fig. 1.5. Consequently, when using an IQ baseband representation(see Fig. 1.10) the 200MHz single-sideband signals I_{BB} and Q_{BB} will be expanded to 1GHz.

When the RF signal is down-converted with a direct IQ downconversion mixer to baseband, the sampling rate of the ADC must be over $2GS/s$, to satisfy the nyquist requirement, and have a dynamic range of around 65dB [8]. In a practical scenario, the bandwidth should still be increased to ease the processing in the digital domain. Figure 1.11 shows the well known ADC-survey by Murmann [9]. The plot shows that there is a trade-off between speed and dynamic range. One can observe, that the ADC with a bandwidth of 2GHz and a dynamic range of 65dB pushes current limit.

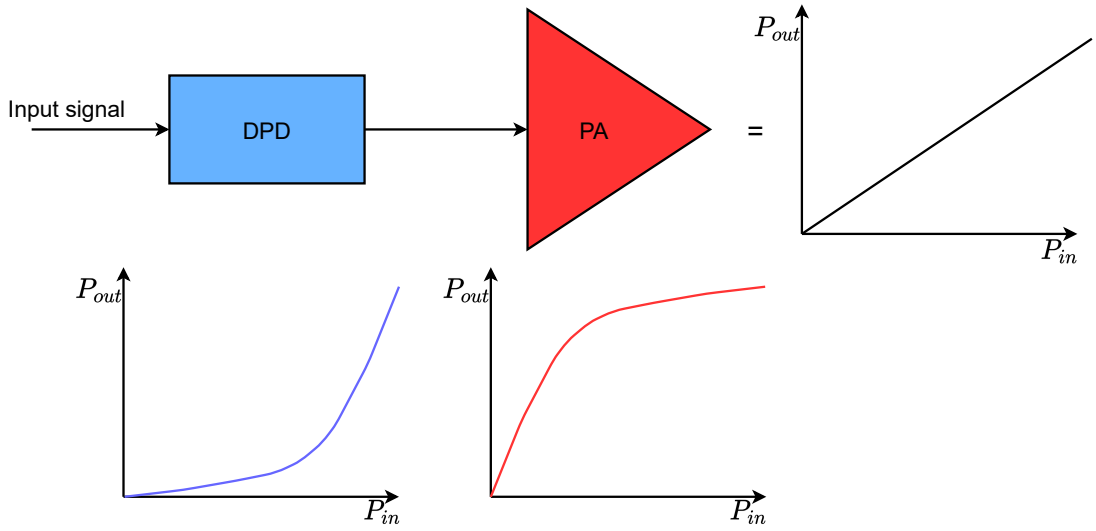

Figure 1.9: A typical pre-distortion system.

Additionally, the efficiency of ADC's decreases for high frequencies. This can be seen when plotting the Schreier figure of merit(SFOM) versus speed, shown in Fig. 1.12. The SFOM is defined in Eq. 1.1 and rewards power, dynamic range and bandwidth. Initially, the power goes up linearly with bandwidth, but beyond roughly 100MHz, the power goes up quadratically with bandwidth.

$$FOM_S = SNDR + 10\log\left(\frac{f_s/2}{P}\right) \tag{1.1}$$

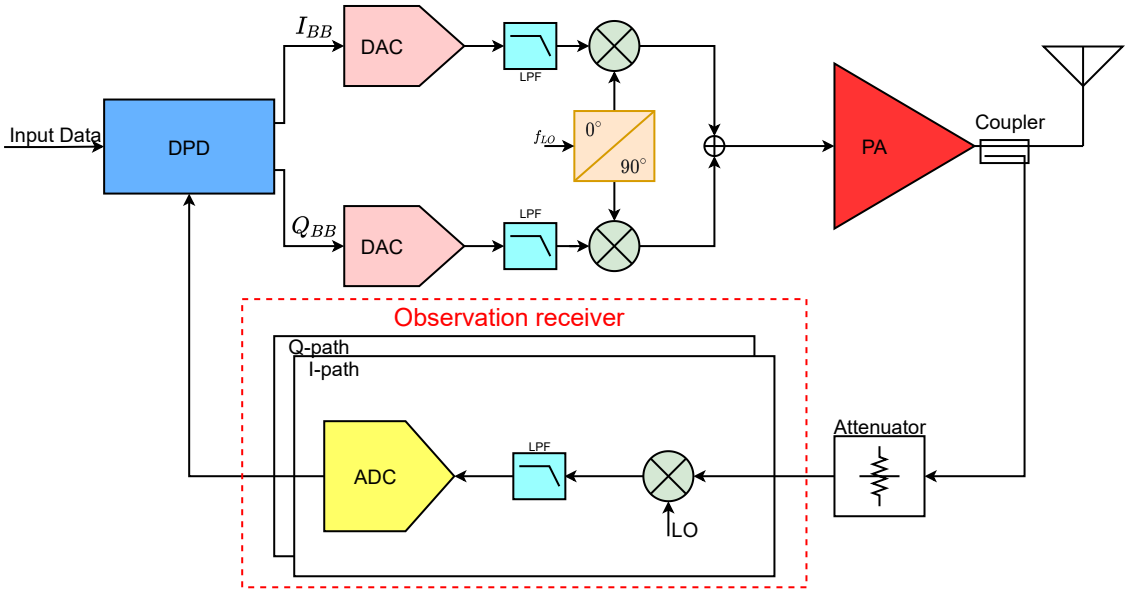

Figure 1.10: A traditional Transmitter line-up, including the feedback path used by the DPD

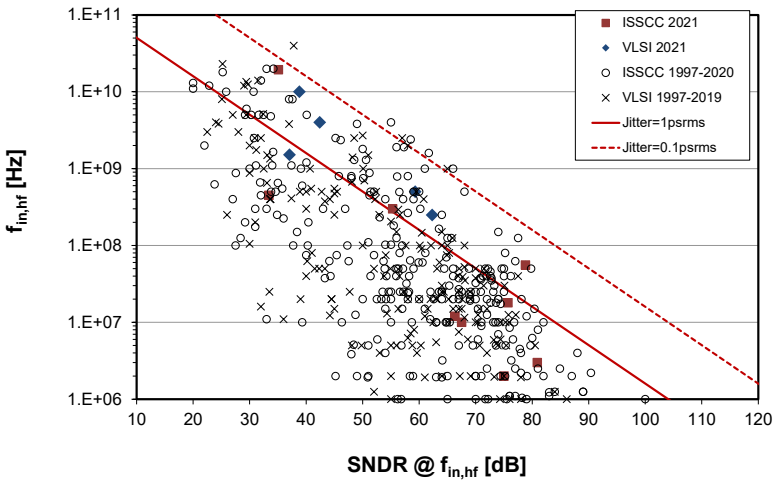

Figure 1.11: ADC publications with speed plotted versus dynamic range [9].

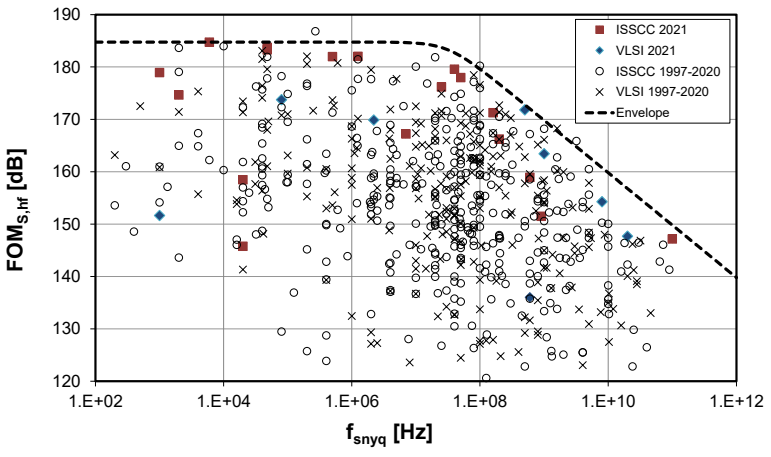

Figure 1.12: ADC publications with Schreier FOM plotted versus speed [9].

1.3 Project scope

This project explores the feasibility of integrating the digital pre-distortion loop with a digital transmitter on-chip. The observation receiver that monitors the output of the RFDAC is of particular interest. A novel architecture is proposed that aims to reduce the dynamic range requirements on the ADC. The proposed architecture is shown in Fig. 1.13. Instead of directly sampling the downconverted RFDAC signal, it is compared to a reference DAC. The reference DAC must be highly linear. The difference signal is the error introduced by the RFDAC. The error signal has a reduced dynamic range compared to the output of the RFDAC itself, and therefore can be sampled with a low resolution ADC. The reference DAC can be made more linear because it is built for lower power and lower frequencies. The proposed architecture is simulated in MATLAB and ADS.

Downconversion architectures typically make use of a mixer. A highly linear harmonic rejection mixer and trans-impedance amplifier have been designed as part of this project. The circuits are simulated at the transistor level using 40nm CMOS technology. Clock generation is not the focus of this thesis, clocks with a 15ps rise/fall time are assumed to be available.

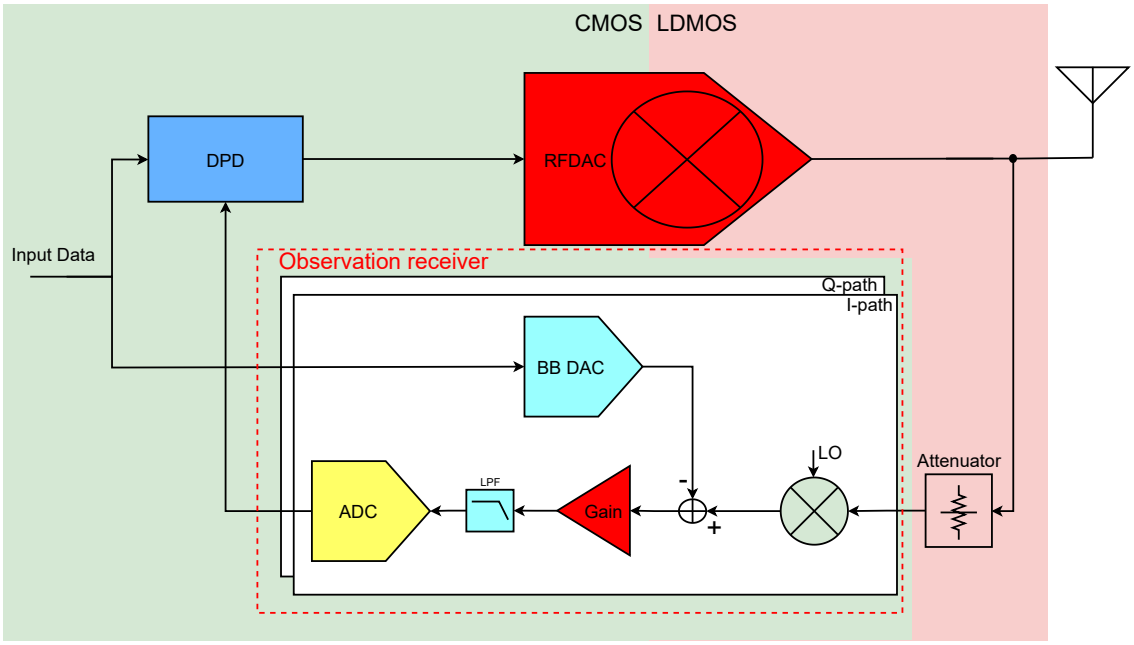

Figure 1.13: Architecture using a baseband reference DAC. The downconverted output of the RFDAC is compared with the output of the BBDAC. The difference signal will have a lower DR than the output of the RFDAC, reducing the requirements on the ADC.

1.3.1 Project objective

The objective is to integrate the digital pre-distortion with a digital transmitter. As part of this objective, there are two sub-objectives:

1. Find the observation receiver architecture that can be integrated the most effectively with a high-power digital transmitter
2. Design a highly linear mixer with harmonic rejection

1.3.2 Specifications

The RFDAC's transfer function is not expected to change rapidly over time, allowing averaging of data produced by the observation receiver. Consequently, noise performance is not the focus of this thesis

and circuits will be compared on their Spurious-Free-Dynamic-Range(SFDR), rather than their Signal-to-Noise-and-Distortion ratio(SNDR).

The RFDAC must offer 50dBc ACPR for a complex modulated signal. To accurately measure the output of the RFDAC, the aimed dynamic range of the observation receiver is 65dB.

In this project, the focus is mainly on the components right before the ADC. ADC's operate best with a close to 1V peak-to-peak(V_{pp}) input swing. Therefore, this project aims to offer the ADC a signal with at least $1V_{pp}$ swing and satisfy the distortion specification at this swing level.

Specifications summed up:

- The observation receiver must have at least 1GHz bandwidth
- The observation receiver must have $1V_{pp}$ swing at the input of the ADC, at this swing, any spurs must 65dB below the signal of interest.
- The downconversion mixer must have at least 40dB harmonic rejection.
- The system must be designed for a carrier frequency of 3.5GHz.

1.4 Thesis Outline

In chapter 2 the different downconversion architectures are compared and are studied on feasibility. Chapter 3 describes the design of a highly linear harmonic rejection mixer and transimpedance amplifier. Chapter 4 goes deeper into the most promising downconversion architecture considering various circuit level limitations of the mixer and transimpedance amplifier. Chapter 5 concludes and proposes future improvements to this thesis work.

2 Downconversion architectures

This chapter discusses architectures that downconvert the RF signal to the baseband. For each architecture, the required specifications of its sub-components will be given. Based on the specifications, the feasibility of integrating the ORX with the transmitter will be studied. Since the goal is to integrate a complete digital transmitter, off-chip bandpass filters are avoided.

Section 2.1 discusses the RF sampling architecture. Section 2.2 discusses a conventional downconversion architecture that employs a mixer, similar to a superheterodyne receiver. Section 2.3 will propose architectures that measure the error made by the RFDAC. The latter architectures drastically reduce the required resolution of the ADC. Two variations of the error measurement are discussed. Section 2.3.1 will treat the architecture that does the error measurement at RF and subsection 2.3.2 will treat the architecture that does the error measurement in the baseband. The architectures proposed in section 2.3 are validated using MATLAB simulations.

2.1 Direct RF sampling

From an architectural standpoint, the simplest way to monitor the output of the RFDAC is to sample it directly. The system architecture is shown in Fig. 2.1. In this architecture example, two ADC's are used to sample at different moments, to detect the I and Q signal content. As explained in chapter 1, an RFDAC produces a spectrum with many harmonics. Even when only considering up to the 5^{th} harmonic at 17.5GHz, the Nyquist condition requires a sampling rate of over 35GHz. An ADC with a sample rate of over 35GHz and 65 SFDR is currently not available. The jitter requirements for such an ADC would be much higher than what is currently possible. Consequently, the direct RF sampling architecture is unsuitable for this project.

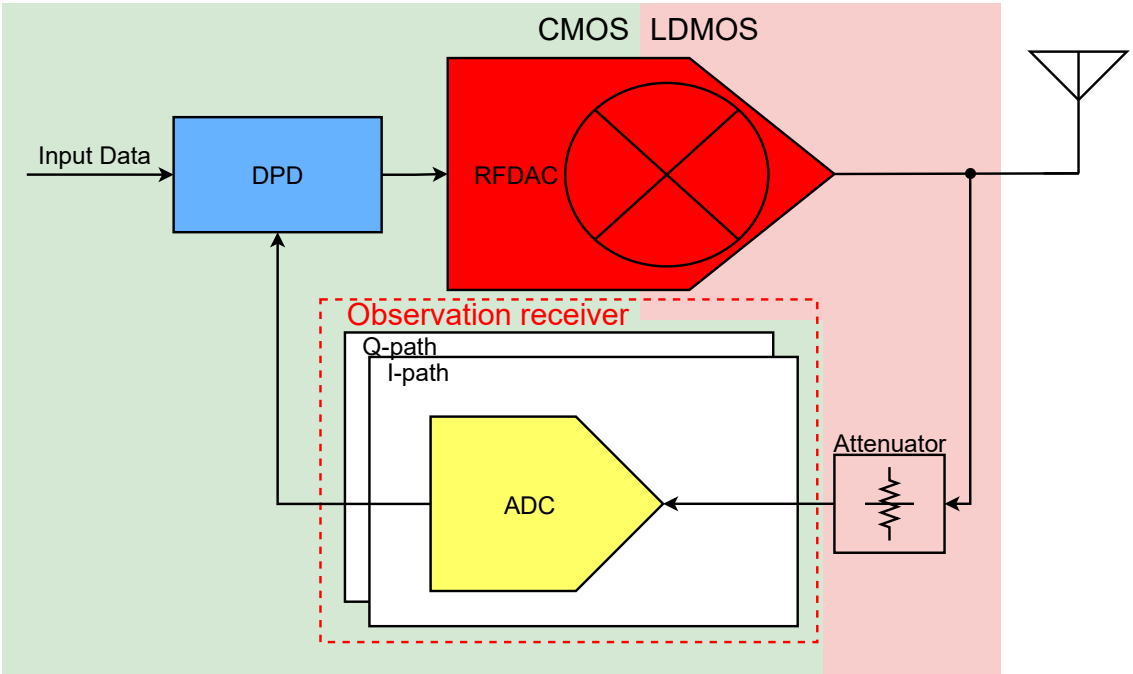

Figure 2.1: Architecture using direct RF sampling.

2.2 Conventional downconverting mixer architecture

By employing a mixer, the signal of interest can first be transferred to the baseband. After mixing, the harmonics can be filtered more effectively, and the signal can be sampled at a lower sample rate. Figure 2.4 shows the conventional downconversion architecture.

Let us compare filtering before and after downconversion. Figure 2.2 shows a simplified RFDAC spectrum with components at 3.5GHz and 10.5GHz; both components have 2GHz of bandwidth. A first-order filter is applied with a cutoff frequency of 5GHz. The resulting filtering at 10.GHz is $20log(\frac{1}{1+(\frac{f}{f_0})^2}) = 20log(\frac{1}{1+(\frac{10.5}{5})^2}) \approx 15dB$. Now compare this to filtering after downconversion. The output of the RFDAC is downconverted with an ideal direct downconversion mixer. Consequently, the component at 3.5GHz is now located around DC and the component at 10.5GHz is downconverted to 7GHz, shown in Fig. 2.3. A first-order filter is applied with a cut-off of 1.1GHz. The resulting filtering at 7GHz is $20log(\frac{1}{1+(\frac{7}{1.1})^2}) \approx 32dB$. The conclusion is that filtering after downconversion more than doubles the effectiveness of the filter. Additionally, the filter after downconversion is more practical to implement.

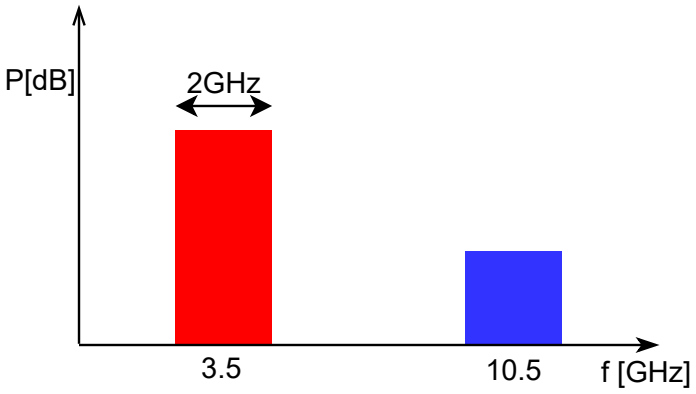

Figure 2.2: Spectrum before downconversion

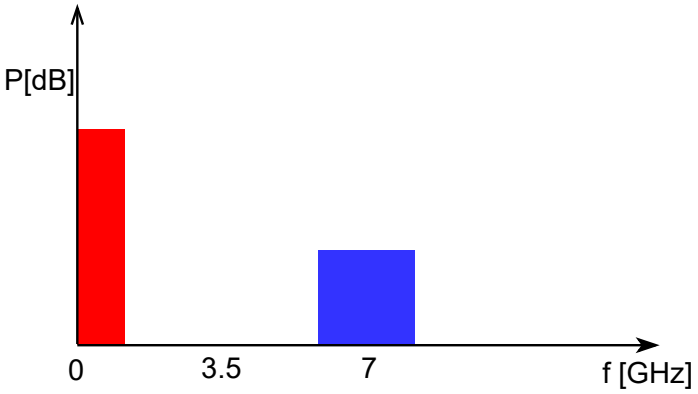

Figure 2.3: Spectrum after direct downconversion

This thesis uses the mixer as a direct IQ downconversion unit, which means that the modulated RF signal is transfered around DC. The choice for a direct downconversion architecture is motivated by the high baseband bandwidth requirement. Since positive and negative frequencies are recombined, the baseband bandwidth requirement is at least two times lower than if a low-IF mixer was used. Additionally, the mixer's gain is improved by a factor of two. Direct downconversion mixers have several challenges, such as DC-offset, even-order intermodulations and flicker noise [10]. Flicker noise is most significant in narrow-band systems. DC-offset and even-order intermodulation might require calibration, such as proposed in [11].

After downconversion and filtering, the signal can be sampled at 2GHz. The SFDR requirement is still 65dB. Compared to the RF sampling architecture of section 2.1, the needed sampling bandwidth is significantly reduced. Though 65dB SFDR at $2GS/s$ is a challenging requirement, there exist ADC's that meet the required specifications. Ali [12] reaches an SFDR of 72dB with a sampling bandwidth of $2.5GS/s$ while using 1.15W and an area of $7.2mm^2$. ADC's that come close to the desired specifications are generally complex, require extensive calibration and will likely need its own clock generation [13–16]. Thus, making integration of a digital transmitter less feasible.

To avoid the undesired down conversion of higher harmonics to the baseband, a harmonic rejection mixer has to be used. The design of a harmonic rejection mixer is the topic of chapter 3. The third harmonic in the RFDAC output spectrum is expected to be 25dB weaker than the signal of interest. Consequently, the mixer must have a harmonic rejection of 40dB to reach 65dB overall system dynamic range.

The mixer must have 65dB SFDR and a flat transfer function vs. frequency within the output's bandwidth of 1GHz. The mixer's gain is less critical since the RF input signal has a very large amplitude, however, at the input of the ADC there should be a $1V_{pp}$ signal swing. So there is a design trade-off between the mixer and any subsequent stages.

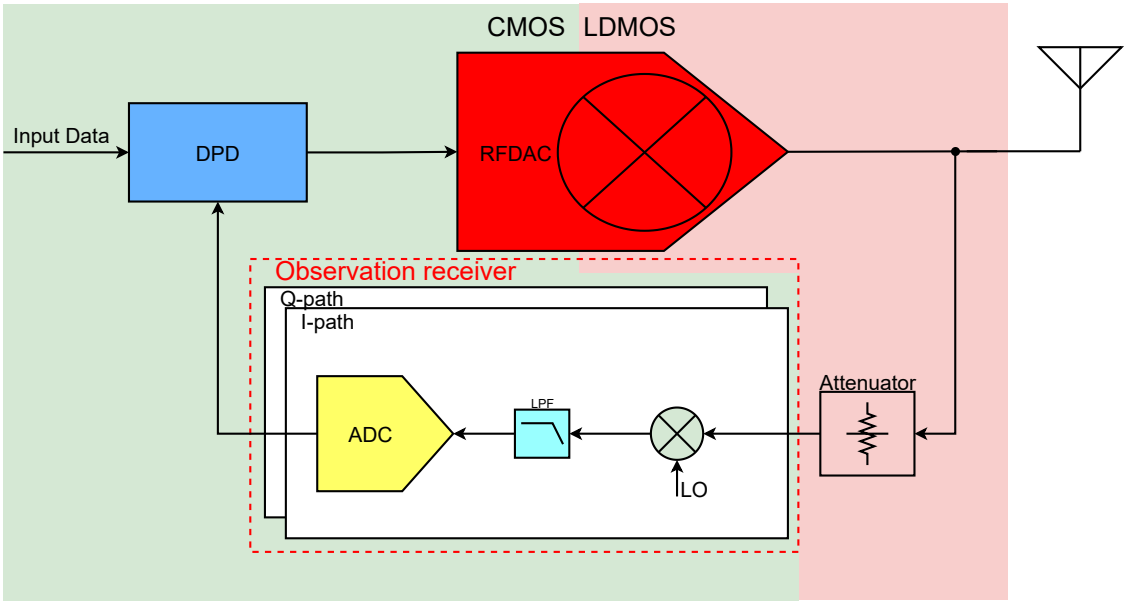

Figure 2.4: Linearization architecture employing a mixer.

2.2.1 Summary

After mixing, the RFDAC's output can be sampled at a lower sampling rate and the higher harmonics can be filtered more efficiently. In this architecture, the ADC's must have a sampling rate of over $2GS/s$, and an SFDR of 65dB. ADC's that can make the required specs will use a DC power in the order of watts and occupy a chip area of over $7mm^2$.

This architecture requires the design of a highly linear harmonic rejection mixer. The mixer must have an SFDR of 65dB at a $1V_{pp}$ output swing. It must have 40dB harmonic rejection and a flat transfer function within the output's bandwidth of 1GHz.

2.3 Error-measurement architectures

So far, the downconversion architectures have aimed to sample the output of the RFDAC, either directly or after downconversion. This chapter introduces a more efficient approach that makes use of knowledge of the RFDAC. The RFDAC has a worst-case linearity of 30dB when no DPD is used. We can use this knowledge to design an observation receiver that reduces the SFDR of the ADC by 30dB. The proposed approach is to subtract the output of the RFDAC from the output of an ideal reference DAC and sample the resulting error signal. A reference DAC can be made significantly more linear than the RFDAC by designing it for lower output power. The RFDAC's output can be formulated as: $V_{RFDAC} = V_{Ideal} + V_{Error}$, and the reference DAC as $V_{Reference} = V_{Ideal}$. After subtraction the error made by the RFDAC is left and can be sampled: $V_{RFDAC} - V_{Reference} = V_{Error}$. The situation is illustrated in Fig. 2.5.

Two scenarios are considered. One is the worst-case scenario, where the linearity of the RFDAC is 30dB. The other is a best-case scenario where the linearity of the RFDAC is 65dB. These two scenarios are illustrated in Fig. 2.6. In the worst-case scenario, the error signal will be 30dB weaker than the output of the RFDAC. In the best-case scenario, the error signal is 65dB weaker than the output of the RFDAC. To measure the error in both scenarios, the error measurement system must have a dynamic range of 35dB. After subtraction, the error signal can be amplified by 30dB, to bring the error signal up to the full scale of an ADC. An SFDR of 35dB for the ADC is a significant improvement over the 65dB required in section 2.1 and section 2.2. Now the SFDR of the observation receiver is limited by the accuracy of the subtraction.

The following subsections will show block diagrams of possible implementations of the error measurement concept.

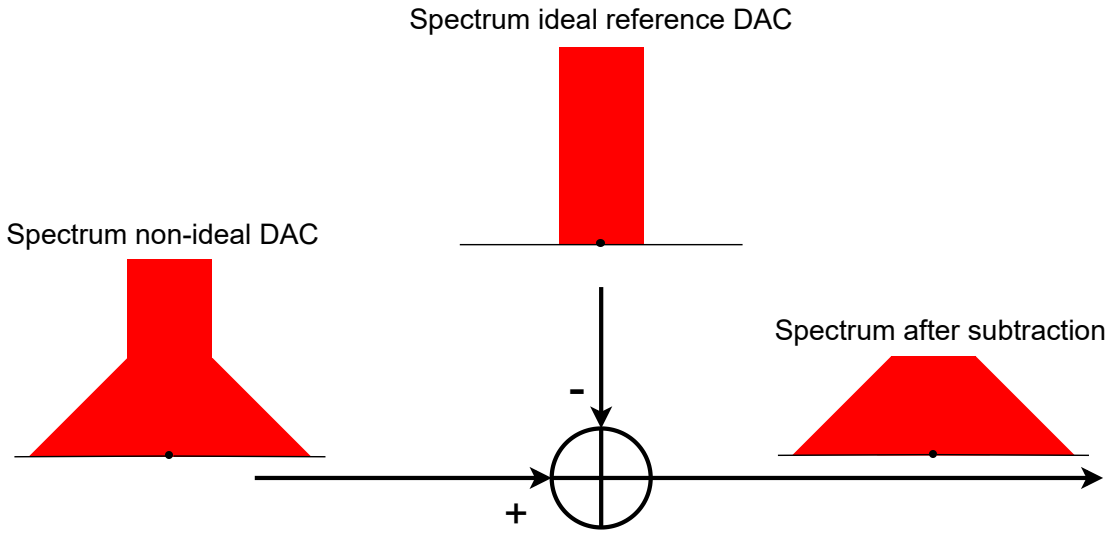

Figure 2.5: Error made by RFDAC found by subtracting Ideal reference signal from the output of the RFDAC

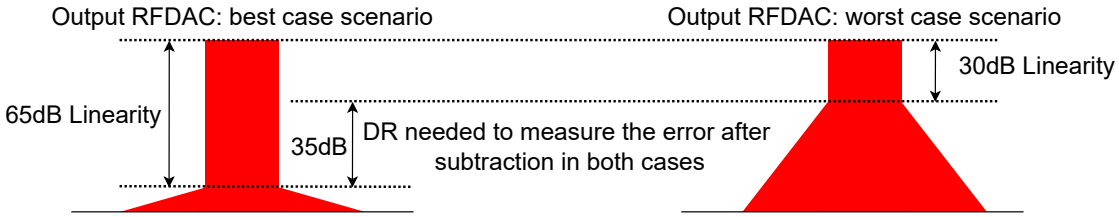

Figure 2.6: Left: Best case scenario, Right: Worst case scenario. After subtraction, a DR of 35dB is needed to measure the error in both scenarios.

2.3.1 Error-measurement at RF

Figure 2.7 shows a possible implementation of the error-measurement architecture. In this approach, the signal coming out of the RFDAC is attenuated and compared to another RFDAC. After subtraction, the error signal is amplified and mixed to the baseband. The error signal has a dynamic range of 35dB. Consequently, all components that come after the subtraction need an SFDR of 35dB. In this case, it means that both the mixer and the ADC have a relaxed linearity specification. The bandwidth of the mixer and ADC are the same as in section 2.2. Namely, 1GHz for the mixer and amplifier and $2GS/s$ for the ADC. The mixer must still have 40dB harmonic rejection because the harmonics of the reference DAC will likely be different from the harmonics of the RFDAC.

The critical parts of this architecture are the reference DAC and the subtraction-circuitry. The reference DAC must have a linearity of 65dB. Additionally, the reference DAC and attenuated RFDAC must be matched in amplitude and phase; the subtraction must not introduce spurs bigger than spurs that the RFDAC with 65dB linearity would introduce. The phase-matching poses a difficult challenge, considering that the signals are RF. To demonstrate how critical phase matching is, a simple MATLAB simulation was done. Two sine waves at 3.7GHz are defined with the same amplitude but a slight phase-mismatch. The frequency of 3.7GHz corresponds to the highest frequency in signal created by upconverting a 200MHz baseband signal to a 3.5GHz carrier. After subtraction, a minor tone is left at 3.7GHz due to the phase-mismatch. The required dynamic range of 65dB leads to a maximum allowed phase-mismatch of 0.027degrees, for a 3.7GHz signal this corresponds to a maximum allowed timing error of 20fs. Such a small timing error is unfeasible. Furthermore, a small phase-mismatch would yield an enormous increase in the error signal

challenging the dynamic range of the down-conversion path. Therefore, the error-measurement architecture using an RF reference DAC is less practical.

Summary

The error measurement using an RF reference DAC architecture lowers the SFDR requirement and ADC to about 35dB. The timing error between the RF reference DAC and the RFDAC cannot be bigger than 20fs. This stringent timing requirement makes the error measurement at RF less practical.

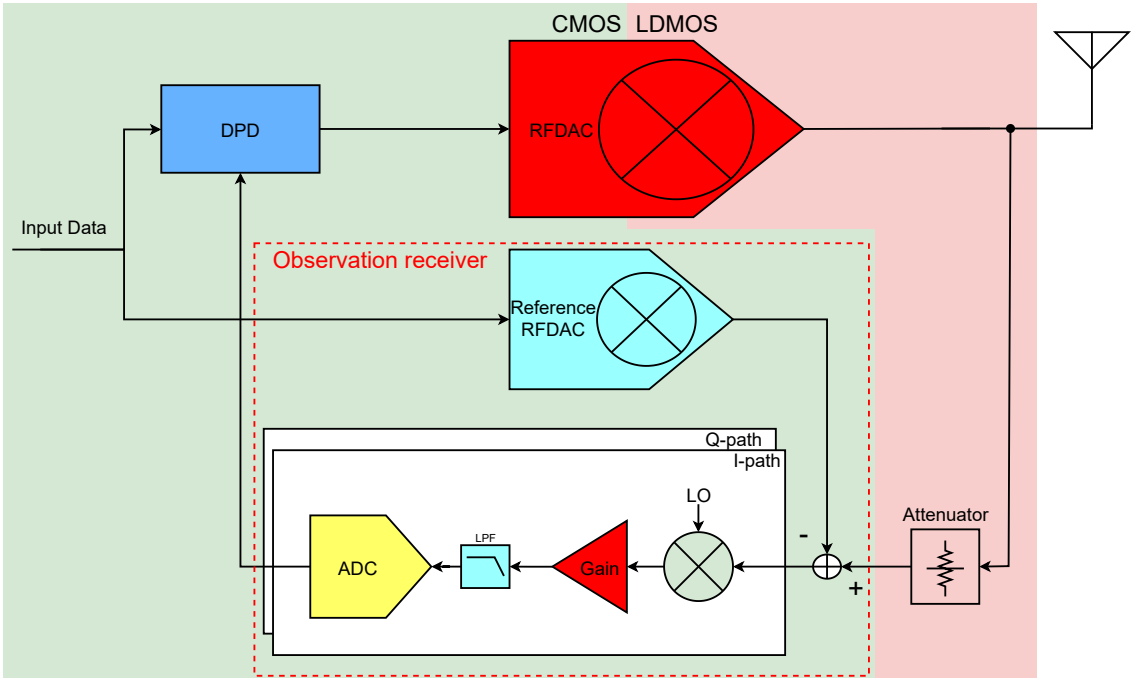

Figure 2.7: Error measurement architecture, error measured at RF

2.3.2 Error-measurement in baseband

The last subsection concluded that measuring the error at RF resulted in unfeasible timing requirements. This subsection proposes an architecture that lowers the timing requirements by first mixing the RFDAC's output to baseband. After mixing, the output can be compared to baseband reference DAC (BBDAC). The proposed architecture is shown in Fig. 2.8.

Now, the allowed phase error of 0.027degrees for a 200MHz signal corresponds to 370fs. Consequently, the timing error between the reference DAC and the output of the mixer can be at most 370fs. The timing requirement is relaxed by a factor $\frac{3.7GHz}{200MHz} = 18.5$. The maximum timing error of 370fs is still challenging. However, the ADC's required in the conventional downconversion architecture of section 2.2 have jitter requirements of less than 100fs. Another advantage of measuring the error in baseband is that the reference DAC is now a baseband DAC, instead of an RFDAC. A baseband DAC is easier to realize with 65dB linearity. Baseband DAC's with the required resolution and bandwidth are available, figure 2.9 shows reported specifications of current DAC's. The intermodulation of the BBDAC is assumed to be negligible compared to the intermodulation of the RFDAC. As a result, the baseband DAC's bandwidth must 200MHz.

The mixer is located before the subtraction. Consequently, it must have an SFDR of 65dB. The amplifier and the ADC are situated after the subtraction and must have an SFDR of 35dB. The mixer and amplifier must have a bandwidth of 1GHz, and the ADC must have a sampling rate of $2GS/s$

ADC's with a SFDR of 35dB and a sampling rate of $2GS/s$ can be realized without time-interleaving. Zhu reaches a SFDR of 48dB and a bandwidth of $2GS/s$ while using $0.08mm^2$ of area and 21mW of

power [17]. This ADC will be more practical to integrate with a transmitter than the high SFDR ADC needed in the conventional downconversion architecture.

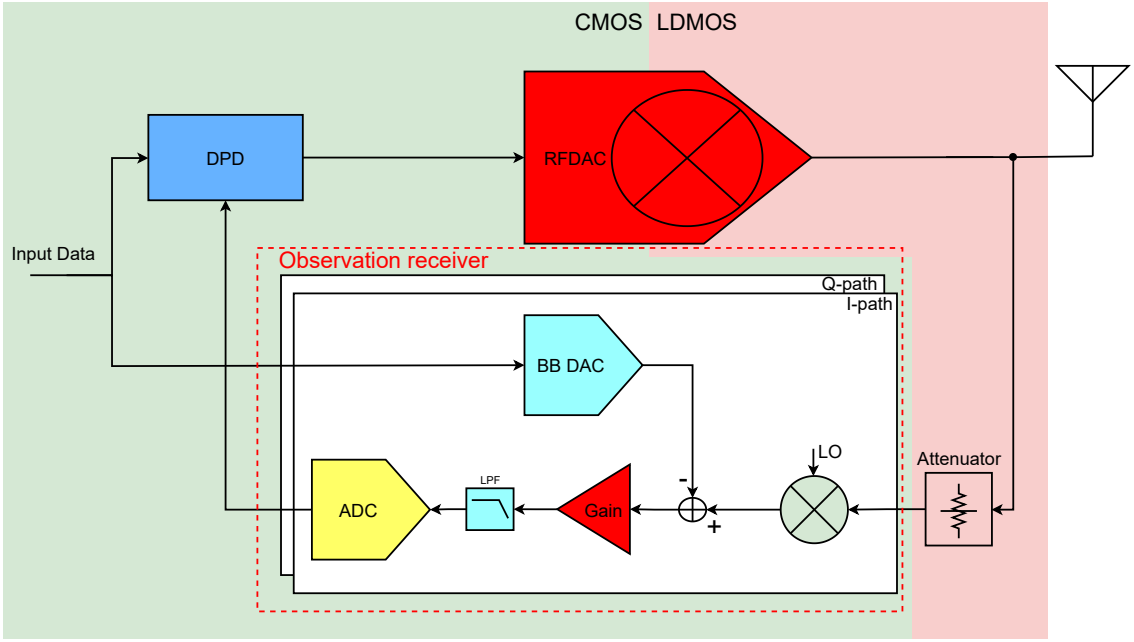

Figure 2.8: Error measurement architecture, the error is measured in baseband.

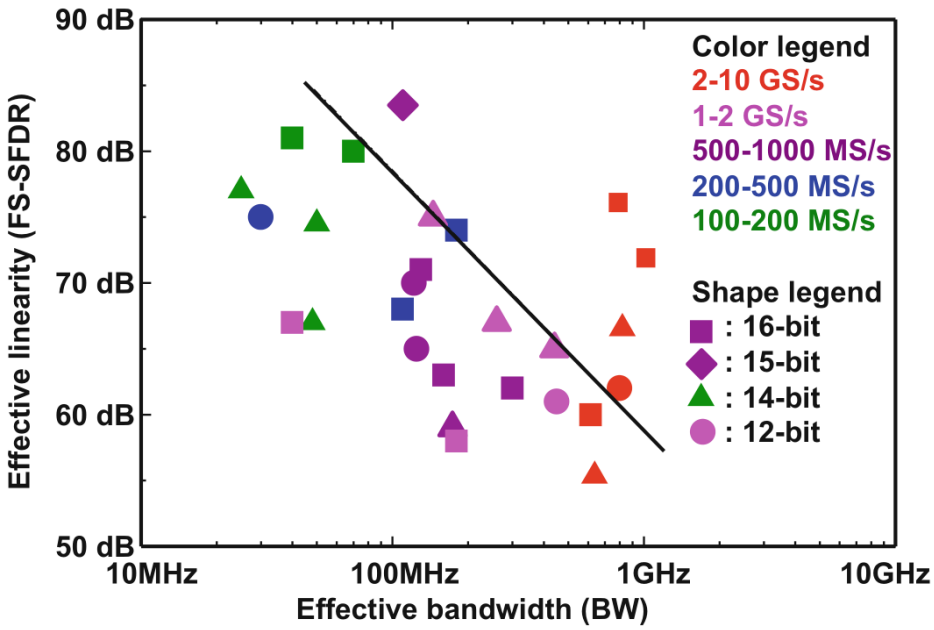

Figure 2.9: Spurious-free dynamic range versus bandwidth for current-steering digital-to-analog converters published from 2000–2015. Based on a plot by: J. Briaire [18]

Apart from the phase, also the amplitude of the RFDAC and reference DAC needs to be matched. The optimum reference DAC gain cannot be predicted with high precision because the non-linearity of the

RFDAC influences the output power of the RFDAC. However, their exist algorithms that can match the amplitude and phase of the two paths. These algorithms are based on auto-correlations; the exact operation of these algorithms is outside the scope of this thesis.

A MATLAB simulation was performed to validate the operation of the proposed architecture. The MATLAB simulation models the RFDAC operation by upconverting a tone of 100MHz using RF carrier frequency of 3.5GHz. After upconversion, a non-linearity of the form $\alpha_1 x + \alpha_3 x^3 + \alpha_5 x^5$ is applied to the upconverted signal. The buildup of the RFDAC's output spectrum is shown in Fig. 2.10. The TX output of the RFDAC is downconverted, as shown in Fig. 2.11. The tone at 100MHz represents the wanted input signal; the intermodulation of the RFDAC causes tones at 300MHz and 500MHz. Next, the ideal reference DAC signal is subtracted. The Reference DAC's signal is shown in Fig. 2.12. The result of the subtraction is shown in Fig. 2.13. All plots are normalized by the power of the largest frequency component. Notice that before subtraction, the intermodulation tone at 300MHz was about 50dB weaker than the signal at 100MHz. After subtraction, the tone at 100MHz is 20dB weaker than the intermodulation tone at 300MHz. Assuming that the subtraction did not affect the third-order intermodulation tone at 300MHz, we can conclude that the subtraction reduced the power of the tone at 100MHz by 70dB. The MATLAB script finds the optimum gain of the reference DAC by adjusting the gain until the signal power after subtraction is minimized. This simulation shows the potential of the error-measurement architecture. Chapter 4 will demonstrate the architecture on the circuit level.

Summary

By first mixing the RFDAC to baseband, the subtraction with the wanted signal can be performed in the baseband. Performing the subtraction in baseband reduces the timing requirements to 370fs.

The mixer is now situated prior to the signal subtraction, and therefore must have a SFDR of 65dB. It must have 40dB harmonic rejection and have a flat transfer function within the output's bandwidth of 1GHz.

The ADC must have a SFDR of 35dB and a sampling rate of $2GS/s$. These specifications can be reached with a factor 100 lower area and power consumption than the ADC needed in the conventional downconversion architecture of section 2.2. Therefore, the error-measurement architecture can be integrated with a digital transmitter the most effectively.

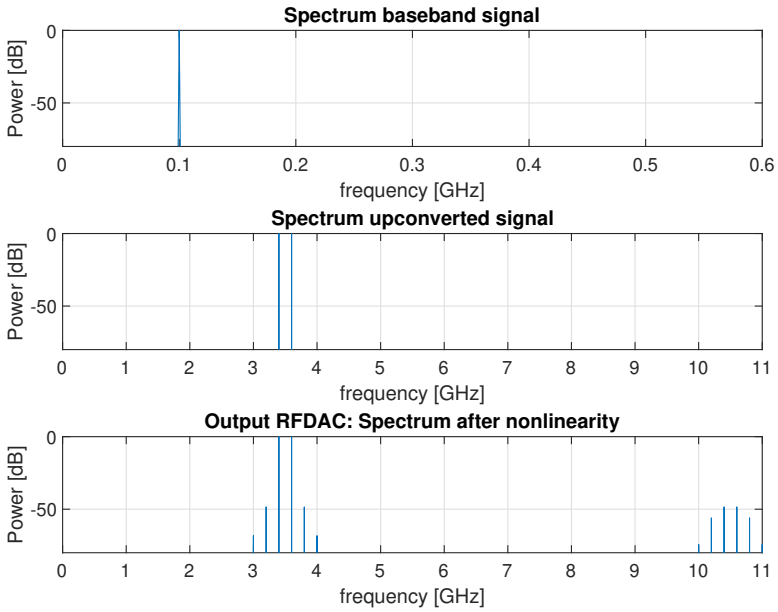

Figure 2.10: Buildup of spectra output RFDAC

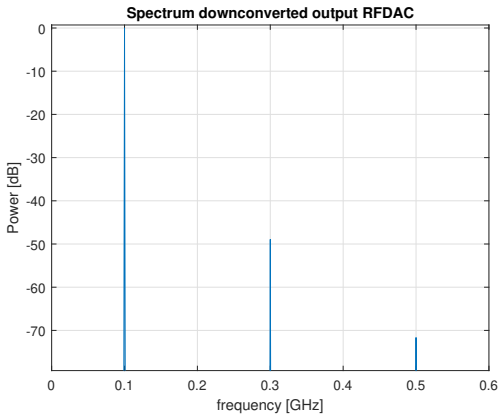

Figure 2.11: Downconverted output RFDAC

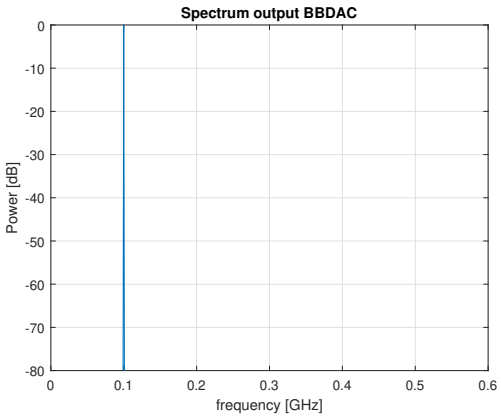

Figure 2.12: Output Reference BBDAC

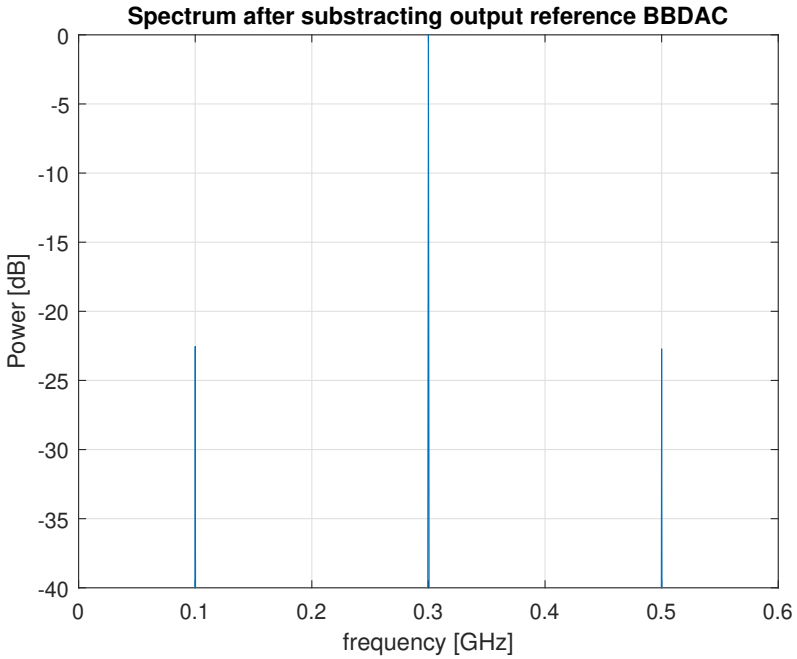

Figure 2.13: Normalized spectrum after subtraction reference DAC signal

2.4 Conclusion

This chapter compared different downconversion architectures. The most promising solutions are based on a conventional down-conversion architecture and the error measurement architecture using a BBDAC.

Both these approaches need a highly linear harmonic rejection mixer, which is discussed in chapter 3. The error detection architecture reduces the SFDR requirement of the ADC to 35dB. Therefore, the error detection architecture that measures the error in baseband is the most promising candidate to be integrated with a digital transmitter. This architecture is discussed at the circuit level in chapter 4.

3 A highly linear harmonic rejection mixer

This chapter discusses the design of a highly linear harmonic rejection mixer. First, some background information is provided in section 3.1. Section 3.2 introduces a novel mixer architecture that implements harmonic rejection by using different resistors in the mixer branches to reach the proper current scaling for harmonic rejection.

The proposed (passive) mixer makes uses an external transimpedance amplifier. Section 3.3 discusses the design of a wide-band transimpedance amplifier. Section 3.4 shows simulations results of the overall mixer. Finally, section 3.5 concludes the work presented in this chapter.

3.1 Background

Subsection 3.1.1 introduces traditional mixer topologies in CMOS technology. Subsection 3.1.2 will discus how a harmonic rejection mixer can be realized in CMOS technology. This thesis initially tried to avoid the need for a TIA. For this reason, the discrete-time mixer topology was studied in subsection 3.1.3. Its evaluation showed that this design approach was less suitable from an implementation point of view.

3.1.1 Common mixer topologies in CMOS

In CMOS technology, mixers are implemented with switches. By switching a waveform can effectively be multiplied by a square wave. An example of a single balanced mixer is shown in Fig. 3.1. The transistor at the bottom with V_{RF} as the input works as a transconductance stage. The commutating switches cause the current to flow to either the right or the left, creating an effective multiplication with a square wave on both sides. The resistor converts the current to an output voltage. In the single balanced mixer, the LO is balanced and RF input is single-ended, causing undesired spurious tones and no common-mode rejection of the RF input signal. This can be improved using a double-balanced mixer, shown in Fig. 3.2. Now all inputs are differential, improving port isolation. Also the linearity is improved because the total swing is divided over the two sides.

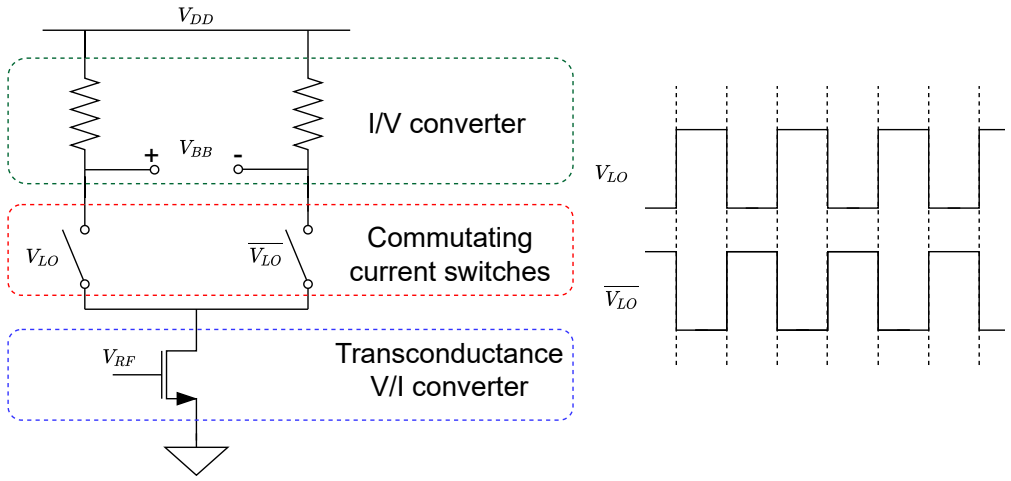

Figure 3.1: Single balanced active mixer with commutating switches

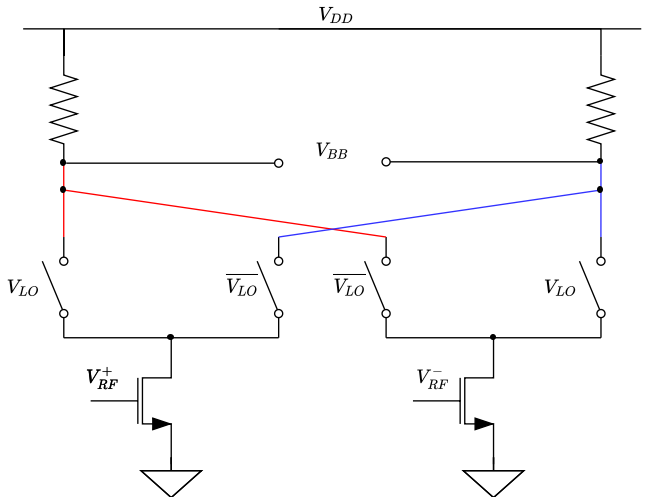

Figure 3.2: Double balanced active mixer

Through the transconductance stage, these mixers topologies can provide a conversion gain. However, typically these transconductance stages will degrade the the linearity. An alternative to these active mixers is a passive mixer. A double balanced passive mixer is shown in Fig. 3.3. Here the switches have already been replaced by transistors. The low input impedance of the TIA benefits the linearity of the mixing core because it prevents the modulation on-resistance of the switches. The (baseband) trans-impedance amplifier now limits the linearity and bandwidth. However, by providing feedback the linearity can be improved. Consequently, practical passive mixers can reach better linearity than active mixers.

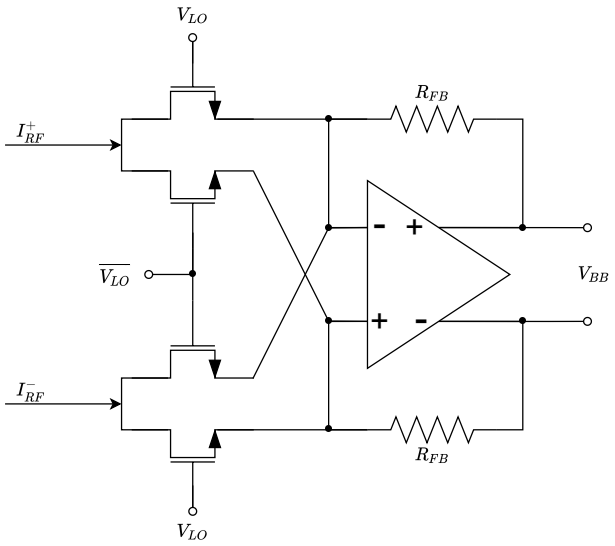

Figure 3.3: Double balanced passive mixer with TIA

3.1.2 Harmonic rejection

In CMOS technology, mixing is done by switching, effectively by multiplying with a square wave. The problem is that a square wave also has components at odd multiples of the fundamental. Equation 3.1 shows the Fourier series of a square wave, the harmonics' amplitude decrease with a factor $\frac{1}{n}$. Figure 3.4 illustrates mixing a signal with odd harmonics with a square wave mixer. The third harmonic will mix with

the third harmonic of the square wave and will also end up in baseband, with an attenuation of only 10dB.

$$f(x) = \frac{4}{\pi} \sum_{n=1,3,5,7,9\ldots}^{\infty} \frac{1}{n} \sin\left(\frac{n\pi x}{L}\right) \tag{3.1}$$

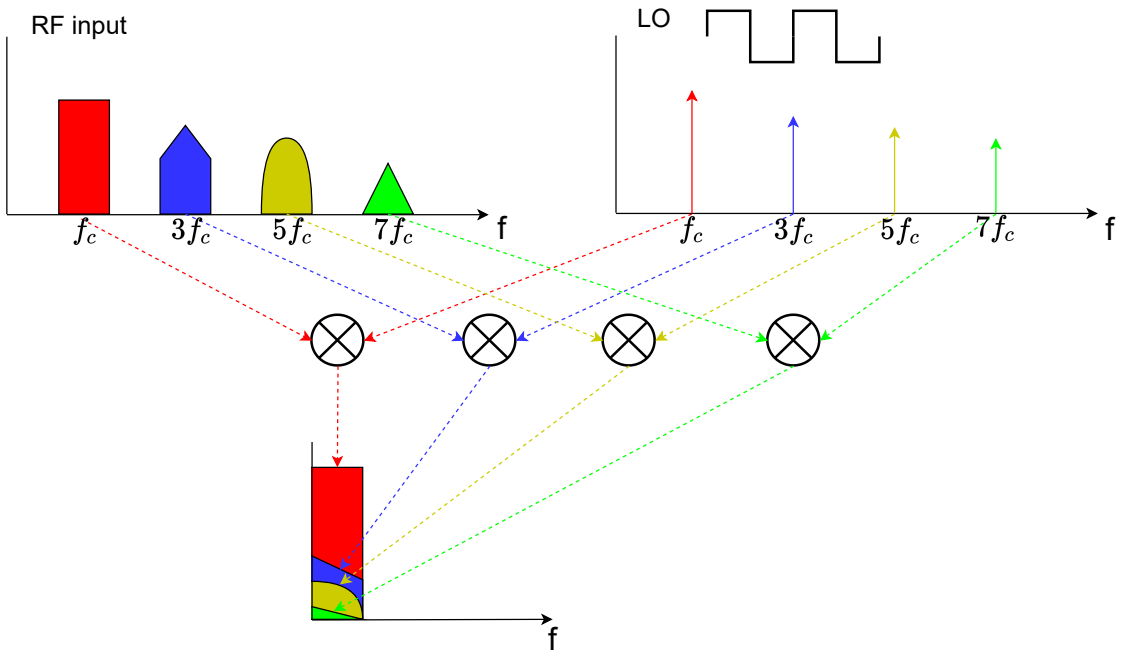

Figure 3.4: A signal with odd harmonics mixed with a square wave. For simplicity only the mixing products that mix to baseband are shown.

Fortunately, more beneficial mixing waveforms can be created by combining multiple square waves. These harmonic rejection waveforms are approximations of a sine wave. Figure 3.5 shows a harmonic rejection waveform that can be composed out of square waves and does not have the third and fifth harmonic.

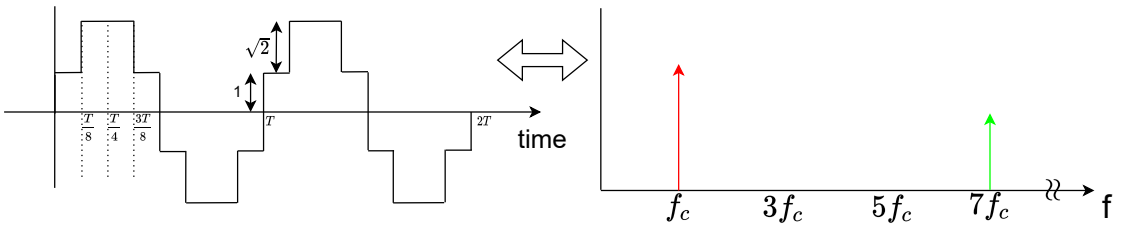

Figure 3.5: Mixing waveform that does not have a third and fifth harmonic.

Figure 3.6 shows how a harmonic rejection waveform can be composed out of square waves. The basic idea is to use multiple square wave mixers with phase shifted LO signals. One of the paths is scaled with a factor $\sqrt{2}$. When the outputs of the three paths are summed, the third and fifth harmonics cancel. In Fig. 3.7 the phasor diagrams for the first, third and fifth harmonic are shown. For the first harmonic the phasors are shifted over $\frac{\pi}{4}$, as a result the phasors are added constructively in the direction of the blue arrow. For the third harmonic the phasors are shifted over $3 \cdot \frac{\pi}{4}$. Because the blue arrow is factor $\sqrt{2}$ longer, the phasors now add destructively. For the fifth harmonic the phasors are shifted over $5 \cdot \frac{\pi}{4}$, again the phasors add destructively. Note that the effective harmonic rejection waveform of Fig. 3.6 is the same as the waveform shown in Fig. 3.5, the only difference is the amplitude. The concept was demonstrated

by Weldon [19], shown in Fig. 3.8. The scaling by $\sqrt{2}$ is implemented by scaling the transconductance stage and the summation is done in the current domain. Harmonic rejection can also be applied to passive mixers, as shown in Fig. 3.9.

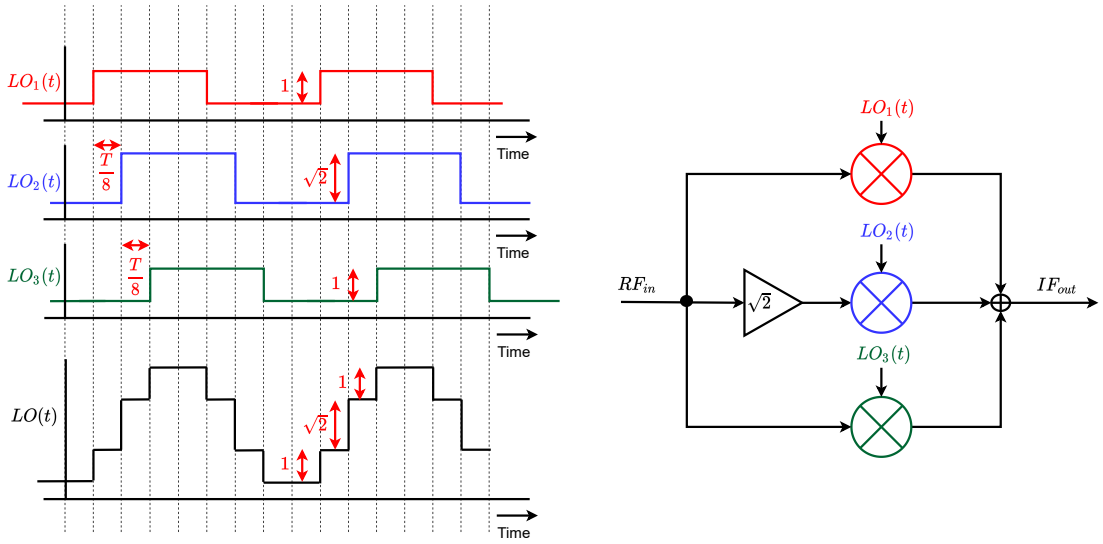

Figure 3.6: Harmonic rejection waveform created by summing three mixers with shifted square waves.

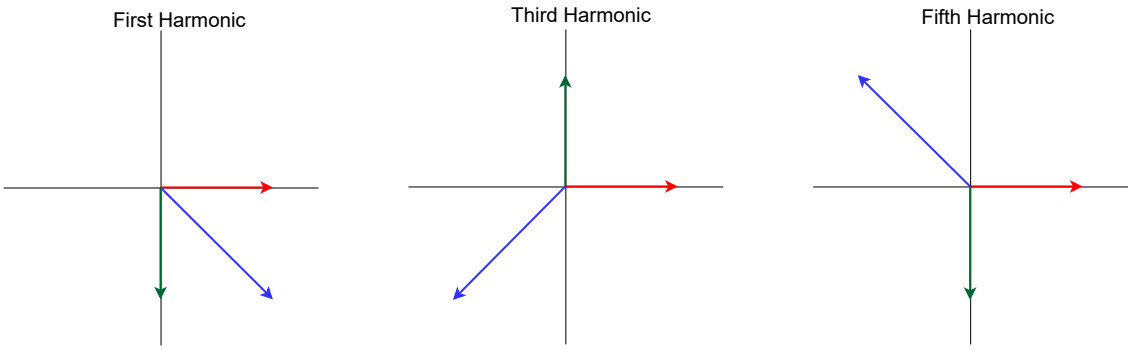

Figure 3.7: Phasor diagrams of the summed square waves. The first harmonic phasor's add constructively. The phasors of the third and fifth harmonic add destructively.

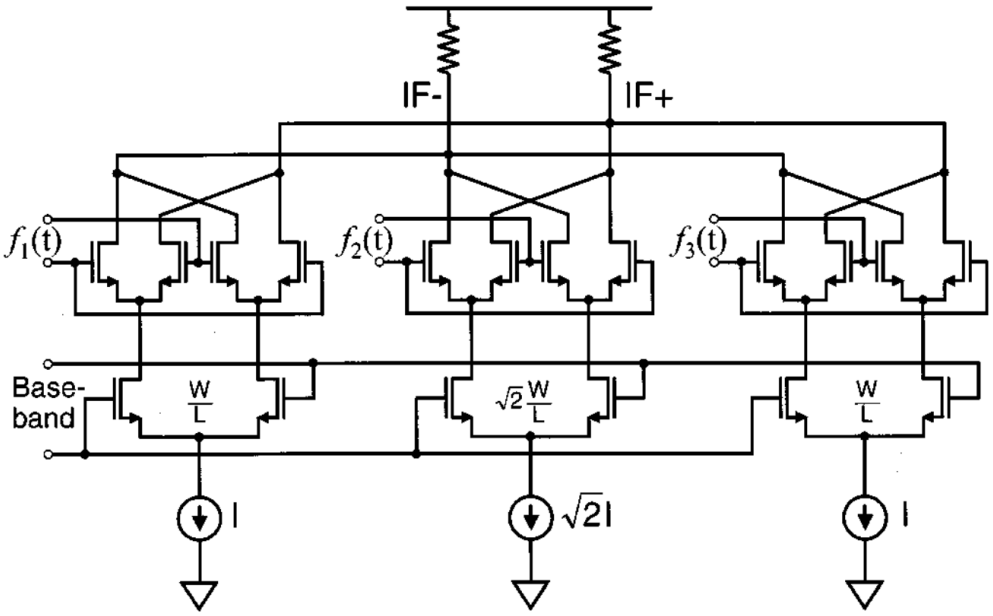

Figure 3.8: Harmonic rejection mixer using double balanced active mixers [19]

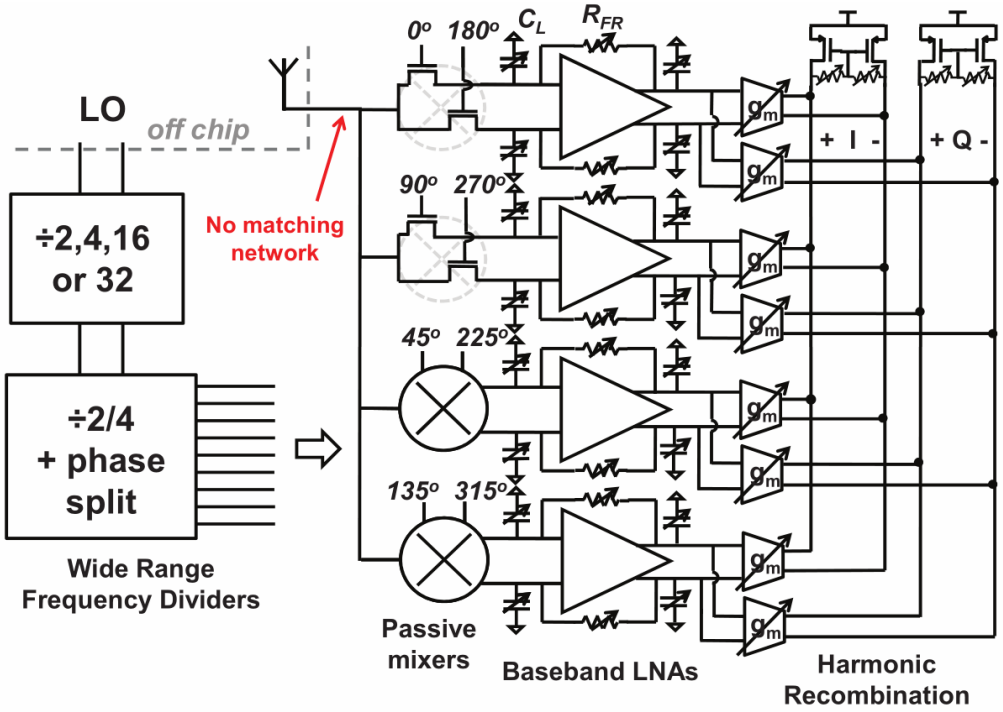

Figure 3.9: Passive mixer with harmonic rejection, as part of a mixer-first receiver [20]

3.1.3 Time-discrete mixing

So far, active and passive mixers have been discussed. An active mixer's linearity is limited by its transconductance stage, and a passive mixer requires a TIA.

Ideally, a mixer would not need an analog stage. This could be achieved by discrete-time(DT) mixing, demonstrated by Ru [21]. Therefore, the feasibility of a DT mixer in this project has been investigated. The idea of DT mixing is to first sample the input signal. After sampling, the signal can be multiplied in discrete time with a mixing waveform. A block diagram is shown in Fig. 3.10. An illustration of the operation in the time domain is shown in Fig. 3.11, in this illustration the mixer is an upconversion mixer. In this example the sampling rate was 8 times higher than the period of the mixing waveform. This can be achieved by using 8 time-interleaved sampling paths. The multiplication with the harmonic rejection waveform can be implemented by scaling the input samples.

Implementing the harmonic rejection mixing in discrete time can be done by using different sampling capacitors in the time-interleaved sampling paths. The charge can then be converted to a scaled voltage by transferring the charge to another capacitor. When $C_a = \sqrt{2}C_b$, C_a will have $\sqrt{2}$ more charge stored after sampling the same voltage on both capacitors. So in the example of Fig. 3.11 the first sample was taken with a sampling branch using a sampling capacitor equal to C_b. The second sample was taken with a sampling branch using a sampling capacitor equal to C_a.

The advantage of the DT mixer is that the harmonic rejection can conveniently be implemented in the charge domain. Which is more accurate than the analog approaches of Fig. 3.8 and Fig. 3.9 that implement the ratio of $\sqrt{2}$ using gain stages.

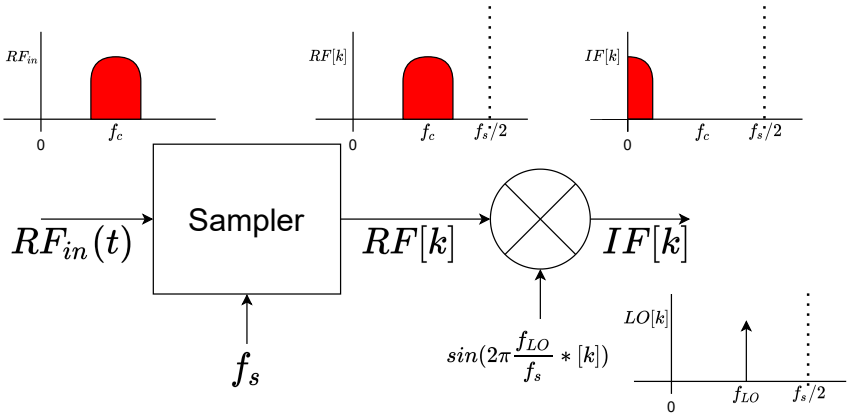

Figure 3.10: Discrete time downconversion mixer in frequency domain

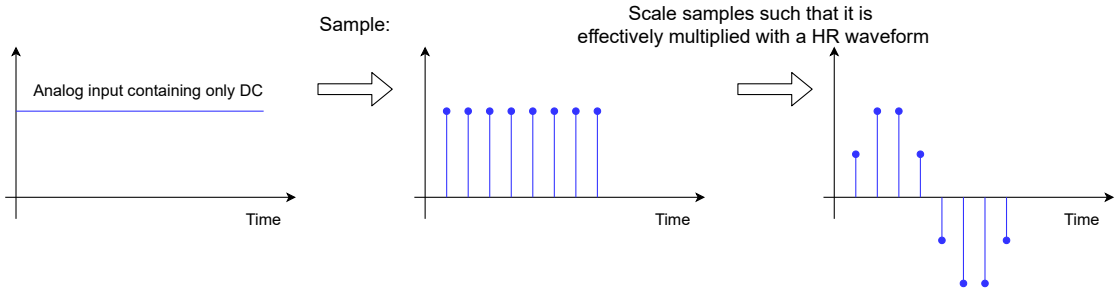

Figure 3.11: Discrete-time upconversion mixer operation in the time-domain

Unfortunately, the sampler at the input has several disadvantages. Firstly, since the sampling is done directly on the RF signal, the observation rate must be high enough to prevent aliasing. Ru [21] uses 8 interleaved paths, effectively getting an f_s of 8 times the f_c. However, this means that the signal around the seventh and ninth harmonic of the RF input will be aliased on top of the first harmonic without any attenua-

tion. Even performing mixing with a continuous-time square wave, which will not effectively suppress the 7^{th} harmonic, will yield a $20og(7) = 17dB$ suppression, which is better than the discrete-time approach provides. A way to improve this is by using a higher number of interleaved sampling paths. However, an interleaving factor of, for example, 16, will be costly to realize.

Secondly, though the sampling can be done in a time-interleaved fashion, at some point, the samples must be recombined on one node. Ru [21] proposes to use an IF buffer, but this means that the DT-Mixer still needs analog components.

Finally, since the sampler is placed first, it has the same speed, and linearity requirements as the direct-RF sampling approach discussed in section 2.1. Even though the signals at high harmonics are not of interest, the samplers timing requirements must be based on the highest frequencies present in the input signal. Combined with the desired DR of over 65dB, this sampler will be hard to realize.

The conclusion is that the idea of DT-mixing is unsuitable for our high bandwidth application. Even though the disadvantages are now apparent, a completely discrete-time approach was first considered to have significant advantages. For this reason, a considerable amount of time was spent on researching DT-mixing.

3.2 Harmonic rejection by scaling currents with resistors

This section introduces the mixer that is designed for this thesis. A passive mixer is chosen for this project because it can achieve better linearity than an active mixer. As explained in subsection 3.1.3, discrete-time mixing is not feasible in this project. The understanding raised was that it is beter to postpone sampling when the input signal contains many harmonics at high frequencies. Therefore the proposed mixer works in continuous time.

Figure 3.12 shows a highly linear square wave mixer. The final harmonic rejection mixer is an extended version of this square wave mixer. The mixer consists of a mixing core and a TIA. The voltage swing at the source is low due to the low input impedance of the TIA. The voltage swing at the drain is lowered by the resistive divider of R_1 and the on-resistance of the switch. The linearity of the switches benefits from low swing at the source and drain because high voltage swing would cause modulation of the on-resistance. Consequently, the mixer's linearity is improved by increasing R_1, or by reducing the on-resistance of the switch. Three of these square wave mixer's can be combined to create a harmonic rejection mixer, such as shown in Fig. 3.6. However, this thesis proposes a more efficient approach that achieves harmonic rejection by extending the mixing-core with additional paths.

The proposed mixer with extended mixing core is shown in Fig. 3.13. This figure only shows the In-phase part. The mixing-core is extended with paths with 25% clocks and a factor $\sqrt{2}$ smaller resistors. By choosing the proper resistor ratios, the input currents can be scaled such that an effective harmonic rejection mixing waveform is implemented. When θ_1 is high and ϕ_1 is low, a current flows from the positive input through R_1 to the positive virtual ground. When both θ_1 and ϕ_1 are high, a current will flow through both R_1 and R_2 to the positive virtual ground. The resistors are chosen such that the total current that flows when both branches are "on", is $(1 + \sqrt{2})$ bigger than when only the branch of R_1 is on. The implementation of harmonic rejection using resistors circumvents the need for a linearity limiting transconductance stage. Additionally, ratio's can be implemented to higher precision with resistors than with transconductance stages, benefiting the harmonic rejection. Moreover, the current injected into the TIA will have a reduced harmonic content, compared to the square wave mixer of Fig. 3.12. The reduced power of harmonics in the current benefits the linearity of the TIA.

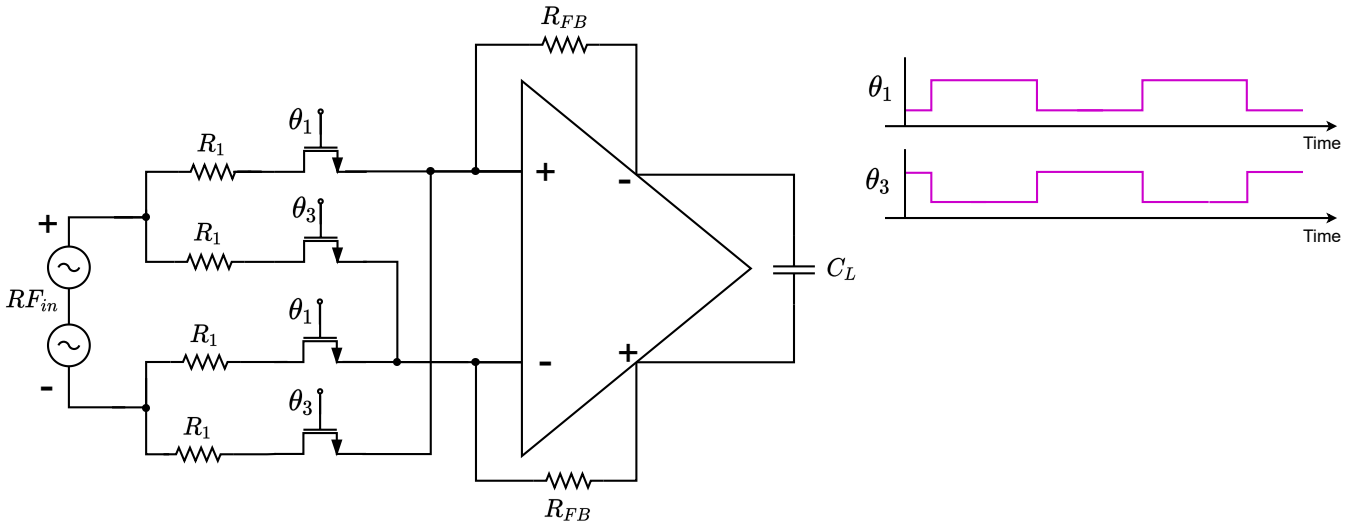

Figure 3.12: Highly linear square-wave mixer

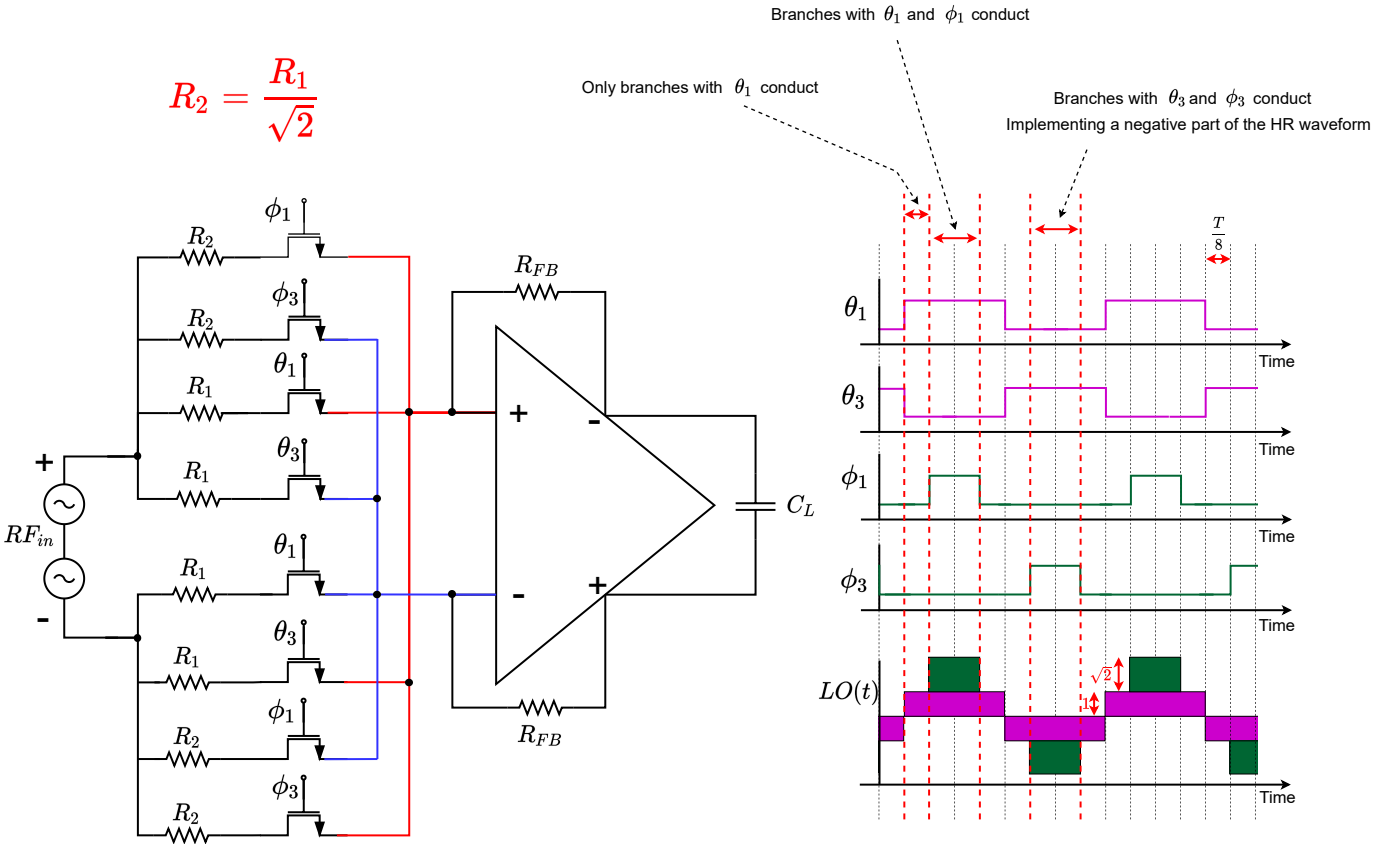

Figure 3.13: Current scaling mixer, only In-phase is shown

Constant input impedance

Harmonic rejection waveforms are approximations of sine waves. The harmonic rejection mixing waveform can be implemented by scaling the paths of the mixing according to Eq. 3.2 [22]. N refers to the number of paths. Assuming a differential implementation, the first harmonic in the harmonic rejection waveform is $(N-1)\cdot f_{LO}$. The proposed mixer implements $N=8$ and therefore rejects up until the 7th harmonic. The γ can be chosen freely. In this thesis γ is π/N, resulting in a symmetric harmonic rejection waveform that can be used to achieve a constant input impedance IQ mixer.

$$A_n = \left|\sin\left(\frac{2n}{N}\pi + \gamma\right)\right| \tag{3.2}$$

As mentioned, the mixer switches between having only the branches with R_1 on, and having the branches with R_1 and R_2 on. This switching of impedance levels causes a periodic variation of the input impedance of the mixer. The harmonic rejection is a consequence of this periodic input impedance variation, the input impedance determines the input currents. The $LO(t)$ in Fig. 3.13 can be interpreted as the input conductance of the In-phase part of the mixer.

However, a varying input impedance is generally not desirable when the input source is not an ideal voltage source. The time-discrete mixer demonstrated by Rhu [21], achieves a constant input load by combining the I and Q paths. The mixer in this project uses a similar combination of I and Q in continuous time, to present an constant input impedance. To understand this, please observe Fig. 3.14. The figure shows the I and Q mixing waveforms. The I and Q parts of the mixer are connected in parallel to the input. Using this specific harmonic rejection waveform, the combined input impedance adds up to be constant

over time. Figure 3.15 shows the complete mixer with both I and Q. The I and Q parts are effectively connected in parallel to the input. The source of each transistor connects to a TIA. The complete mixer only needs two TIA's to implement a harmonic rejection quadrature downconversion mixer. To demonstrate the constant input-impedance on the circuit level, Fig. 3.16 shows the right half of the mixer in three consecutive phases. The TIA input is modeled as a ground node. Please notice that in each phase, there are an equal amount of resistors connected from input to ground. Consequently, the input impedance is constant vs. time. Figure 3.17 shows the mixer modeled as a resistor. The input impedance R_{mixer} can be approximated as $\frac{R_1}{\sqrt{2}+2}$.

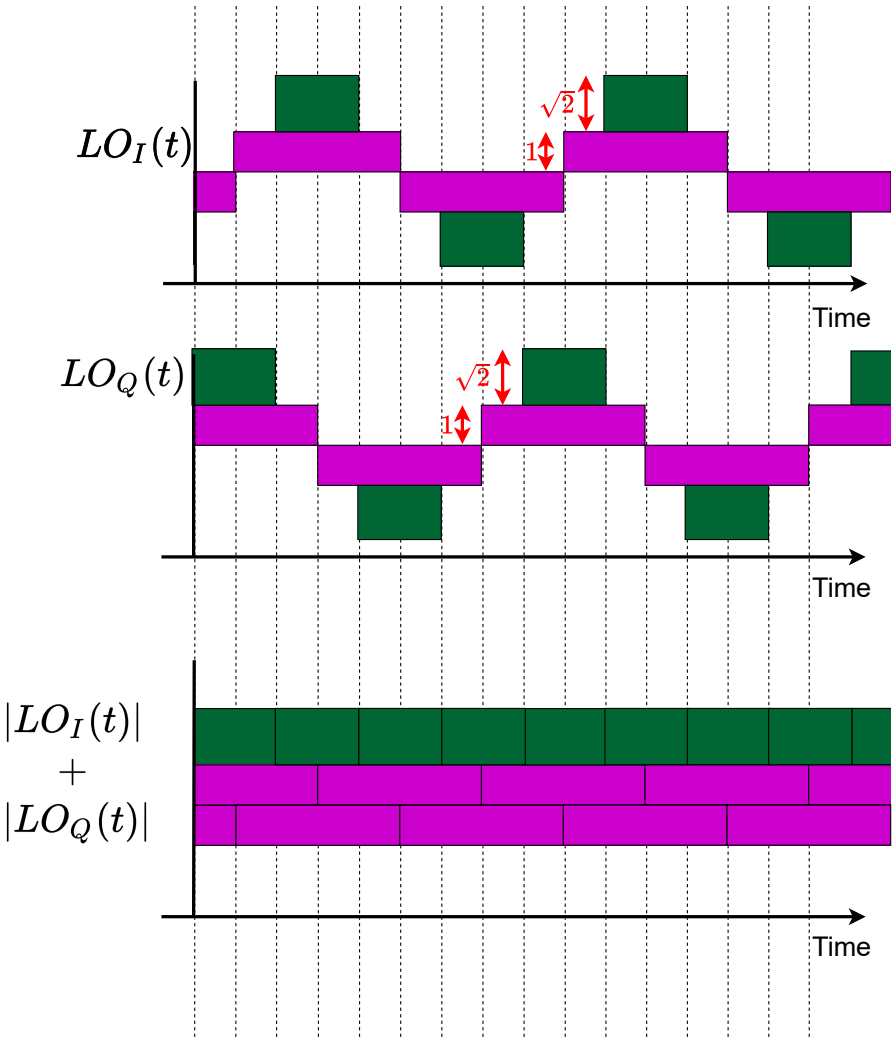

Figure 3.14: The combined I and Q paths present an constant input impedance over time.

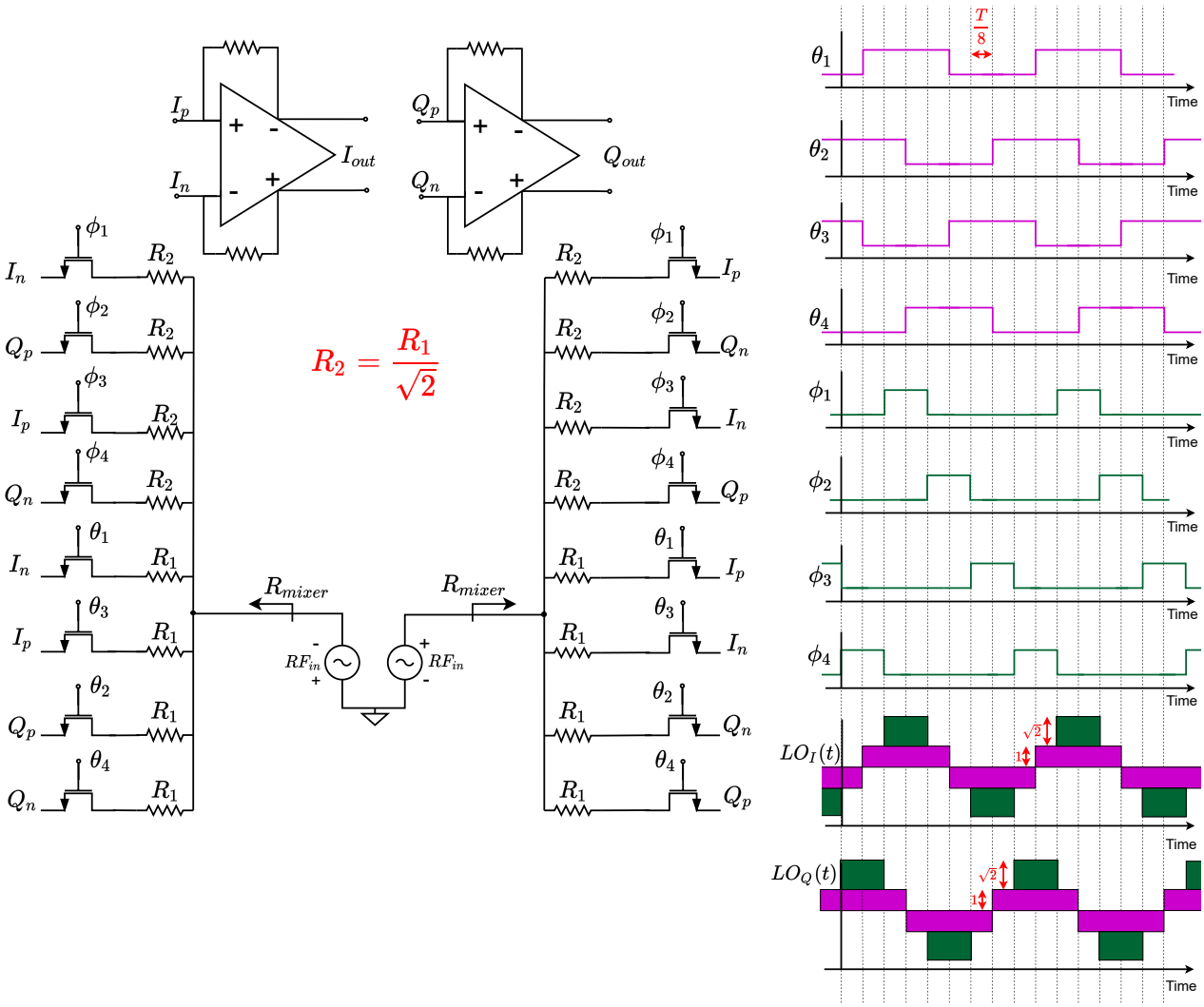

Figure 3.15: Current scaling mixer, with resistors in each branch. Both I and Q paths are shown.

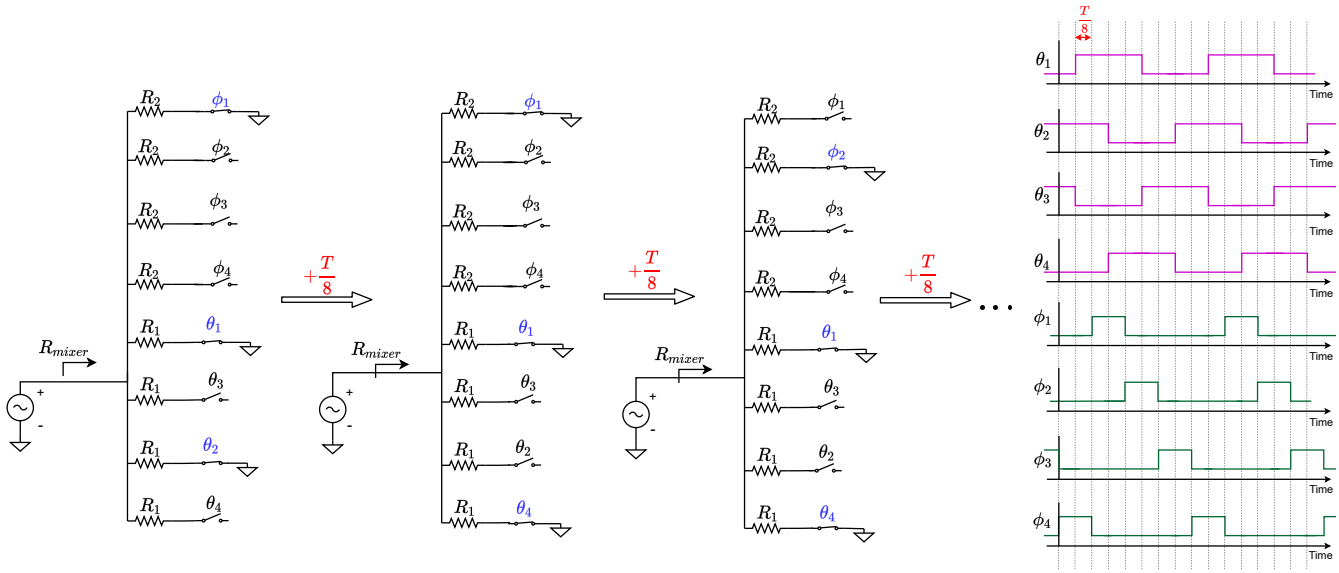

Figure 3.16: Demonstration of three consecutive phases of the mixer, the input impedance of the mixer is the same in all phases.

$$R_2 = \frac{R_1}{\sqrt{2}}$$

$$R_{mixer} = R_1||R_1||R_2 = \frac{R_1}{\sqrt{2}+2} \approx \frac{R_1}{3.4}$$

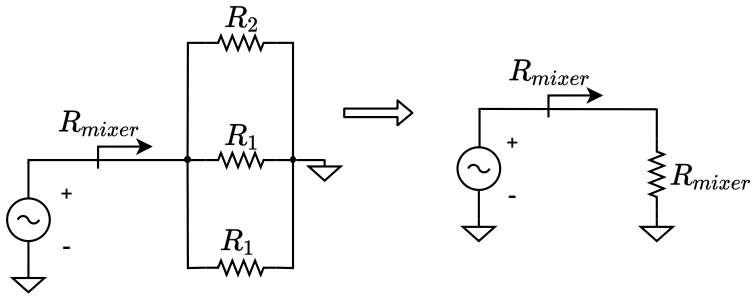

Figure 3.17: Mixer modeled a resistor R_{mixer}

3.2.1 Branches sharing resistors

The mixer concept can be improved by using smart combination of the branches. The proposed improvement is shown in Fig. 3.18. The branches that used 50% clocks are combined with branches with complementary clocks. The branches that use 25% clocks, are combined with three other branches, all of the branches that share a resistor are using a different clock. The operation of the mixer did not change. The benefit of this architecture is that there will now be a low impedance node offered at the drain connections of all transistors at all times.

The branches with R_1 can create the low impedance node with only two devices because those devices use complementary 50% duty cycle clocks. For the branches with R_2 there are four devices needed because they make use of 25% duty cycle clocks. Fortunately, the four 25% duty cycle clocks are precisely the ones

needed to implement the I and Q mixing waveforms. The clocking scheme enables the circuit topology.

In the old approach of Fig. 3.15 the drain of each transistor will switch between a high impedance and a low impedance node, resulting in voltage jumps during switching. Additionally, when the switch is off, the voltage swing will be high. Because the switches are not ideal, the high voltage swing will result in a non-zero current through the devices, even when the devices are meant to be ”off”.

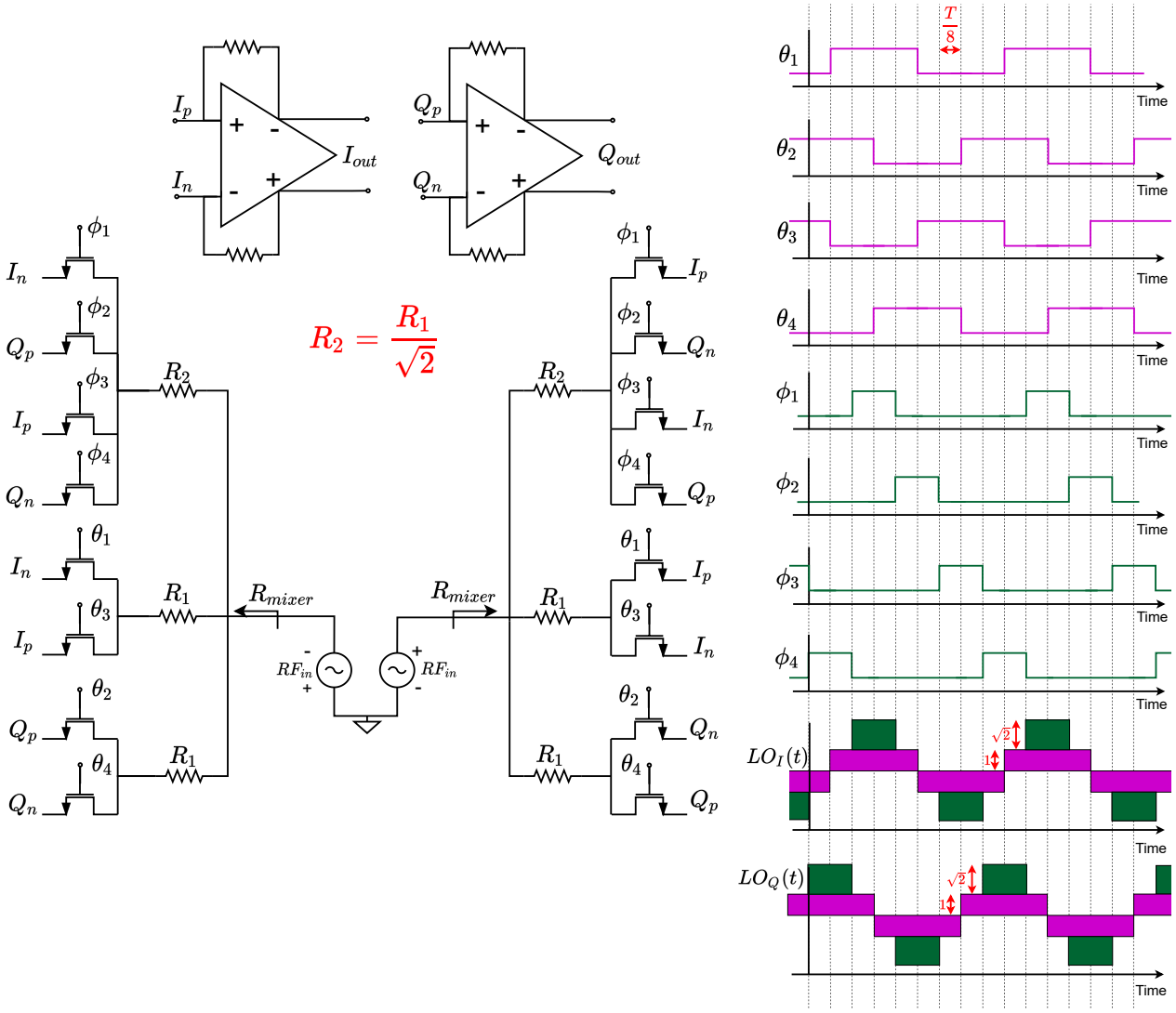

Figure 3.18: Proposed mixer, Both In-phase and Quadrature-phase paths shown.

To demonstrate the advantage of combining branches, a transient simulation was done using the circuits shown in Fig. 3.19. The circuit on top shares R_1 between two transistors with complementary clocks. The bottom circuit has an R_1 for each transistor. Both circuits are driven with a sine wave of 3.55GHz and the clocks have a frequency of 3.5GHz. The $R_{in_{TIA}}$ serves to model a TIA with a non-zero input impedance. The current and voltages of interest are indicated in Fig. 3.19

Figure 3.20 shows the voltage at the drain for both circuits. The right y-axis is used to display the clocking waveform, corresponding to θ_1. The simulation shows that V_1 and V_2 are equal when the switch is on. However when the switch is turned off, V_2 will get much large than V_1. Furthermore, V_1 shows much smaller voltage jumps during switching. Figure 3.21 shows the resulting current waveforms. Current I_1 shows a much lower leakage current than I_2.

The high voltage causes a leakage current to flow through the transistor that is meant to be off. This

can be explained by noting that the off-impedance of the transistor is only 7000Ω at 3.5GHz. The leakage current is also a non-linear current, because the large drain voltage moves the transistor through different regions of operation.

Simulation of the complete mixer shows that the combination of branches improves the harmonic rejection and linearity significantly. Additionally, the low voltage swing at all drains is expected to improve isolation of the baseband signals in different branches.

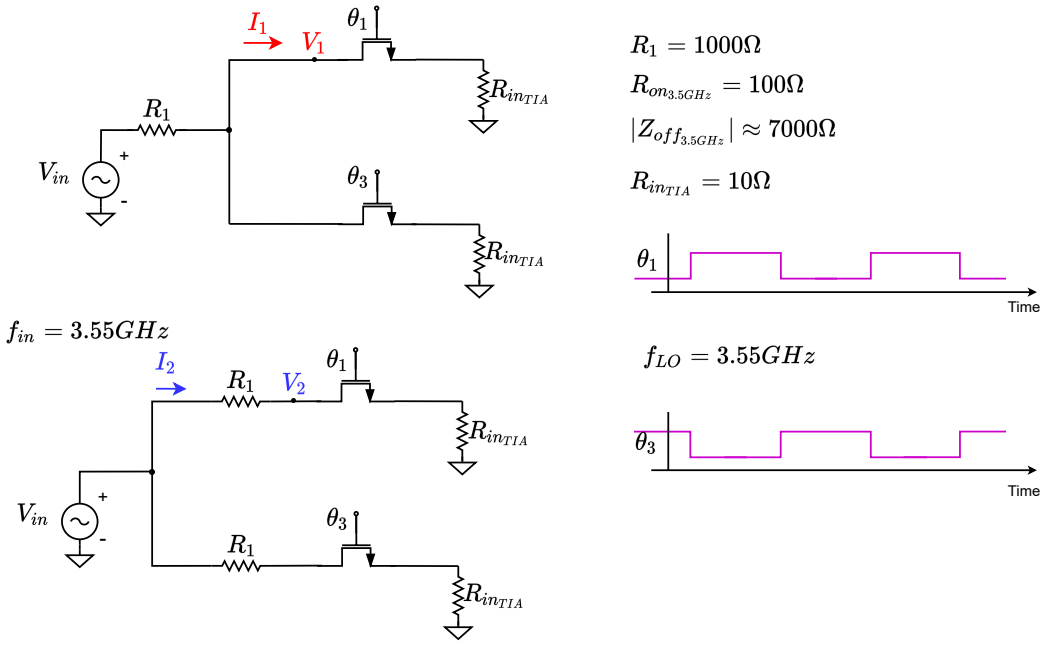

Figure 3.19: Circuits used for demonstrating advantage of combining branches with complementary clocks

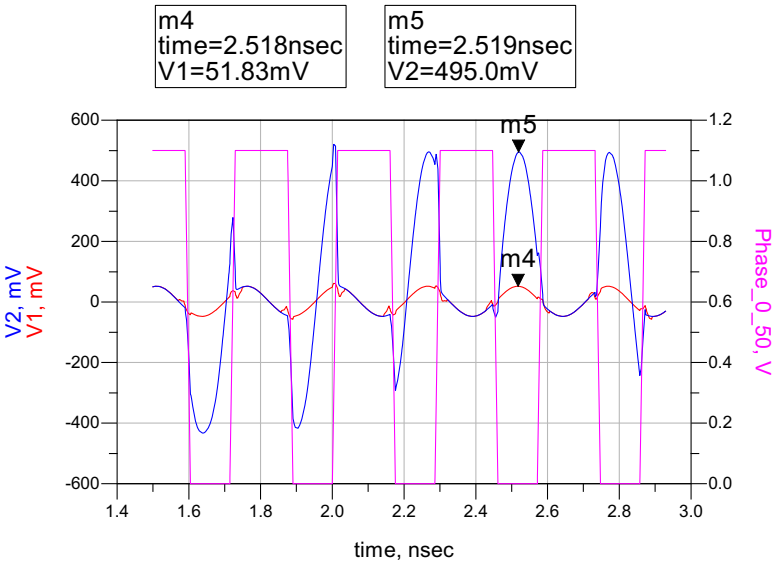

Figure 3.20: Voltages of circuit simulation corresponding to Fig. 3.19

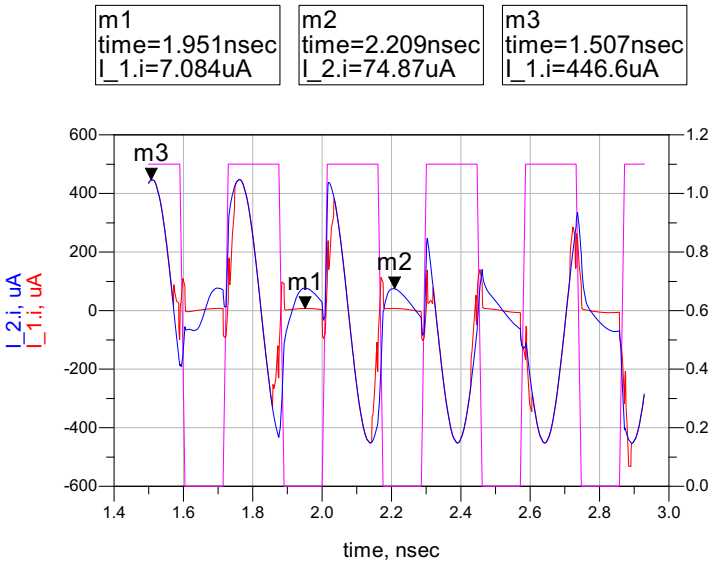

Figure 3.21: Currents of circuit simulation corresponding to Fig. 3.19

3.2.2 Comparison to other work

The proposed mixer in this thesis achieves harmonic rejection in the current domain, before the current is injected into a TIA. In previous work such as shown in Fig. 3.9, the harmonic rejection is achieved by a weighted summation of the output of multiple-square wave mixers with different LO-phases. The key difference is that the harmonic rejection is only achieved after the summation of the different outputs. So each of the TIA's still has many harmonics at its output, limiting the linearity. Furthermore, the weighted summation of the paths needs to be implemented with gain stages, limiting linearity and summation accuracy.

One research group proposes a similar approach to the mixer of this thesis. Kibaroglu [23] also implements harmonic rejection by resistive scaling, the approach is illustrated in Fig. 3.22. According to the authors, the linear current to voltage relation of a resistor allows them to reach an (in-band) Third-order intercept point (IIP3) of 30dBm, the highest reported. Though the latter approach to reach harmonic rejection is similar, there are a few key differences with the mixer proposed in this thesis. A striking difference is that they do not make use of a TIA. The output current is directly converted to an output voltage with a load resister. Consequently, the output signal directly appears at the output of the switching devices. The absence of a TIA results in a substantial trade-off between output swing and other requirements, such as linearity and isolation. In the mixer of this thesis, the TIA serves to improve the trade-off between output swing and the swing appearing at the terminals of the switching devices. A large swing at the terminals of the switching devices results in the modulation of R_{on}, causing non-linearities. Furthermore, since the signal at the output of the switching devices is already downconverted, a large swing causes undesired interaction of the baseband signals in different branches. The commutating switches are bi-directional, the input signal is downconverted but the output signal can also be upconverted back to the input. Moreover, Fig. 3.22 shows that the R_{on} is chosen to be 7.5Ω, resulting in large devices with large parasitics. The small R_{on} helps to achieve a reasonable conversion loss and improves linearity, but decreased R_{off} and large parasitics further decrease the isolation.

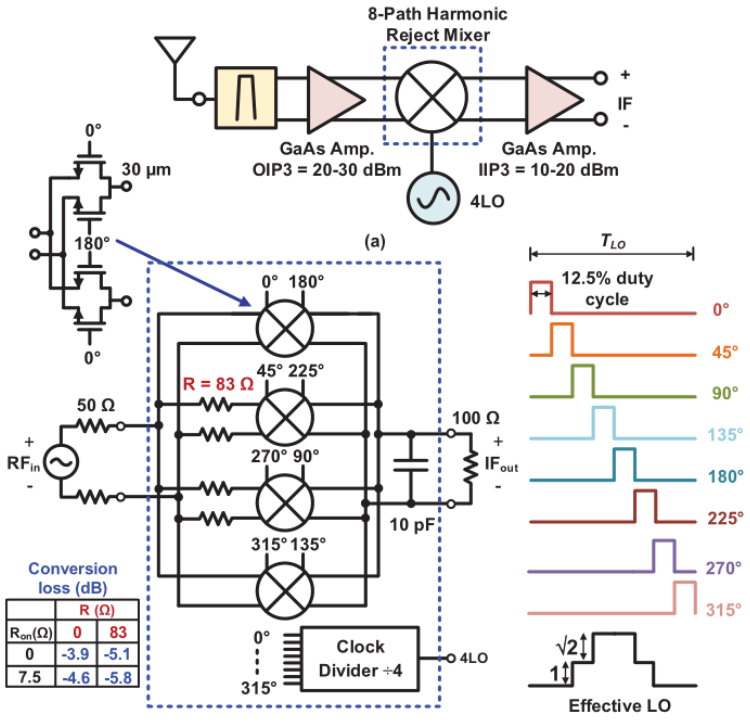

Figure 3.22: Harmonic rejection implemented by resistive scaling [23]

To improve the isolation, Kibaroglu [23] proposes to use non-overlapping clocks of 12.5% duty cycle.

With 12.5% duty cycle clocks, the same effective Harmonic rejection waveform can be implemented as shown in Fig. 3.14. Consequently, in theory, a constant input impedance can be achieved. Interestingly, the paper does not show a combined I-Q mixer and therefore, the mixer does not have a constant input impedance.

The work has been extended by El-Aassar [22], into a 16 phase version reaching harmonic rejection up until the 13^{th} harmonic. However, the proposed 16-phase harmonic rejection waveform cannot be used to present a constant input-impedance, even when combining the I and Q waveforms. Most other specifications are similar to the 8-phase version of Kibaroglu [23]. An IIP3 of 30dBm and an input-refered 1dB gain compression point(IP1dB) of 13dBm, with an IF bandwidth of 100-200MHZ.

Simulations of the mixer proposed in this thesis, including designed TIA, show an IIP3 of 49dBm, a IP1dB of 21dBm, with an IF bandwidth of over 1GHz. More detailed simulation results are presented in section 3.4.

Of course, the use of an amplifier in our system does not come for free. When requiring a large bandwidth, the open-loop gain of the TIA will be limited, leading to an inaccurate closed-loop gain. Consequently, the mixer's gain must be calibrated, leading to increased system complexity.

3.2.3 RFDAC-Mixer interface

So far, the mixer was shown with an ideal voltage source at its input. In reality, the input is coming from an high power RFDAC. The RFDAC can be modeled as an current source that supplies a current of 2.8A peak to peak through a load resistor of 10Ω, leading to an output voltage of 28V peak to peak. Such high voltages would potentially break the thin-oxide devices used in the mixer. Consequently, a voltage attenuator is needed.

The voltage attenuator has the following requirements:

- Provide a voltage attenuation of factor N
- Be highly linear.
- Provide a high input impedance to avoid loading the RFDAC.

An obvious candidate would be a transformer, but a transformer is avoided in this project because it could pick up electromagnetic interference from the high voltage switching in the transmitter. Additionally, a transformer takes chip area. However, when the final implementation of the RFDAC is single-ended, a balun with good common-mode rejection will still be necessary.

The proposed solution in this project is a simple resistive divider. This is undoubtedly linear and the input impedance can be chosen freely. The situation is modeled in Fig. 3.23. The figure shows the RFDAC, attenuator and mixer. The RFDAC is modeled as an AC current source with an amplitude of 14V and a load resistor of 10Ω. The mixer is modeled as a resister with input impedance R_{mixer}, similar to Fig. 3.17. The output voltage of the RFDAC (V_{RFDAC}), is attenuated by the voltage divider of R_3 with the parallel combination of R_4 and R_{mixer}. One might argue that R_4 is redundant. The voltage attenuation could be implemented with only R_3 and R_{mixer}. However, the R_4 is there for robustness, it prevents the voltage at the input of the mixer from jumping up violently when R_{mixer} might temporarily be high. A sensible choice would be to choose R_4 equal to R_{mixer}. Consequently, the parallel combination of R_4 and R_{mixer} is given by Eq. 3.3. The voltage attenuation of N leads to Eq. 3.4 and an expression for R_3 given by Eq. 3.6. The input impedance of the attenuator can be expressed in terms of R_{mixer}, given by Eq. 3.7. The total power tapped from the RFDAC is expressed in Eq. 3.9. Equation 3.10 gives how much consumed power is used by the mixer.

The thin oxide devices can tolerate a voltage up to 1.1V, so the peak to peak voltage swing on the terminals can be $2.2V_{pp}$. The total input voltage swing is divided over the positive and negative inputs, so the total allowed differential peak to peak swing is $4.4V_{pp}$. Consequently, the voltage attenuator must have an attenuation of $N = \frac{28}{4.4} \approx 6.36$. Substituting this into Eq. 3.10 and we find an efficiency of roughly 10%. The total consumed power is directly dependant on R_{mixer}, so a high input impedance benefits the systems power dissipation. The low efficiency makes the resistive divider costly in terms of power-dissipation. However, the power dissipation can be deemed acceptable when considering the whole system.

For robustness, R_4 is chosen such that:

$$R_4||R_{mixer} = \frac{R_{mixer}}{2} \tag{3.3}$$

The voltage attenuator must implement an attenuation of N:

$$\frac{V_{RFDAC}}{V_{In_{mixer}}} = \frac{R_4||R_{mixer} + R_3}{R_4||R_{mixer}} = \frac{\frac{R_{mixer}}{2} + R_3}{\frac{R_{Mixer}}{2}} = N \tag{3.4}$$

Now everything can be expressed in terms of R_{mixer}:

$$R_3 = \frac{N+1}{2} \cdot R_{mixer} \tag{3.5}$$

$$R_4 = R_{mixer} \tag{3.6}$$

$$R_{in} = R_3 + R_4||R_{mixer} = \frac{N+2}{2} \cdot R_{mixer} \tag{3.7}$$

Expressing P_{tapped} and P_{mixer} in the same variables:

$$P_{mixer} = \frac{V^2_{In_{mixer,rms}}}{2R_{mixer}} \tag{3.8}$$

$$P_{tapped} = \frac{V^2_{RFDAC,rms}}{2R_{in}} = \frac{N^2 \cdot V^2_{In_{mixer,rms}}}{\frac{N+2}{2} \cdot 2R_{mixer}} = \frac{2 \cdot N^2}{N+2} \cdot \frac{V^2_{In_{mixer,rms}}}{2R_{mixer}} = \frac{2 \cdot N^2}{N+2} \cdot P_{mixer} \tag{3.9}$$

$$\frac{P_{mixer}}{P_{tapped}} = \frac{N+2}{2 \cdot N^2} \tag{3.10}$$

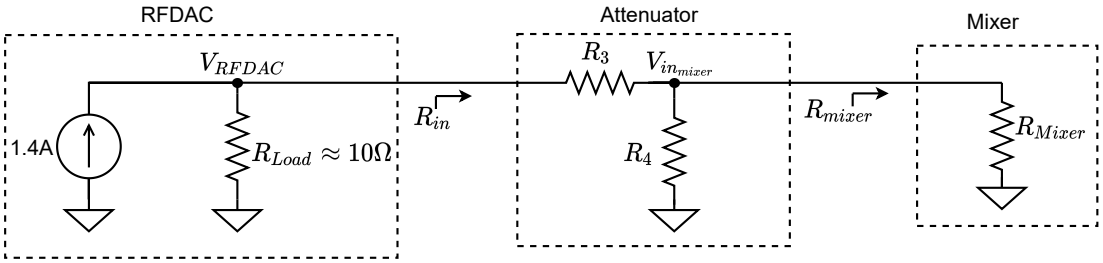

Figure 3.23: RFDAC-mixer interface, a resistive divider connects the RFDAC to the mixer.

3.2.4 Choosing the design parameters

This subsection will go deeper into the proposed mixer of Fig. 3.18. The essential metrics of the mixer will be discussed together with the relevant design parameters. Simulation results support the discussion. Relevant metrics for the mixer are: harmonic rejection, linearity and output swing. The design parameters are the sizing of the switches, the resistors and the specifications of the TIA. To obtain more insight, the mixer can be modeled as in Fig. 3.24. In this model, the mixer is modeled as just one branch with a resistor R_{mixer}. The R_{mixer} is in series with a transistor operating in triode mode, presenting an impedance of R_{on}. The model can be seen as all the branches of the mixer combined into one. The model assumes that the transistor is always on, no switching occurs. This model will especially be helpful when considering the trade-offs between linearity, input impedance, and output swing.

The TIA is shown as an opamp with a feedback resistor R_{FB}. In this subsection, the mixer simulations were done with an ideal TIA. Ideal in the sense that the TIA does not introduce bandwidth or linearity limitations. Section 3.3 addresses the design of the TIA. Section 3.4 will show simulations of the mixer with a non-ideal TIA.

The model of Fig. 3.24 also shows a shunt capacitor C_{shunt} at the input of the TIA. This capacitor filters out higher harmonics in the current domain, before the current is injected into the TIA. Another way of looking at it is shown in Fig. 3.25. The figure shows a simplified 50% duty cycle mixer. Commutating switches up-convert the lowpass characteristic at the input of the TIA, to a bandpass characteristic at the input of the mixer. Consequently, the input signal is filtered already at the RF side. The C_{shunt} can be chosen to get the proper bandwidth of the filter. Another function of the C_{shunt} is to filter out the charge and discharging currents needed to open and close the switches. Circuit level simulations show that the addition of C_{shunt} improves the linearity and harmonic rejection significantly. The C_{shunt} and $R_{in_{TIA}}$ will determine the bandwidth of the mixer.

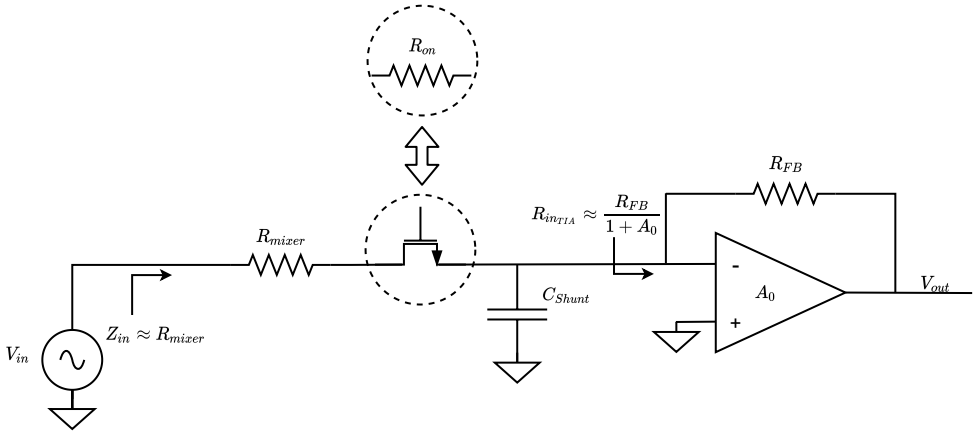

Figure 3.24: Mixer model used to obtain insight into the design parameters.

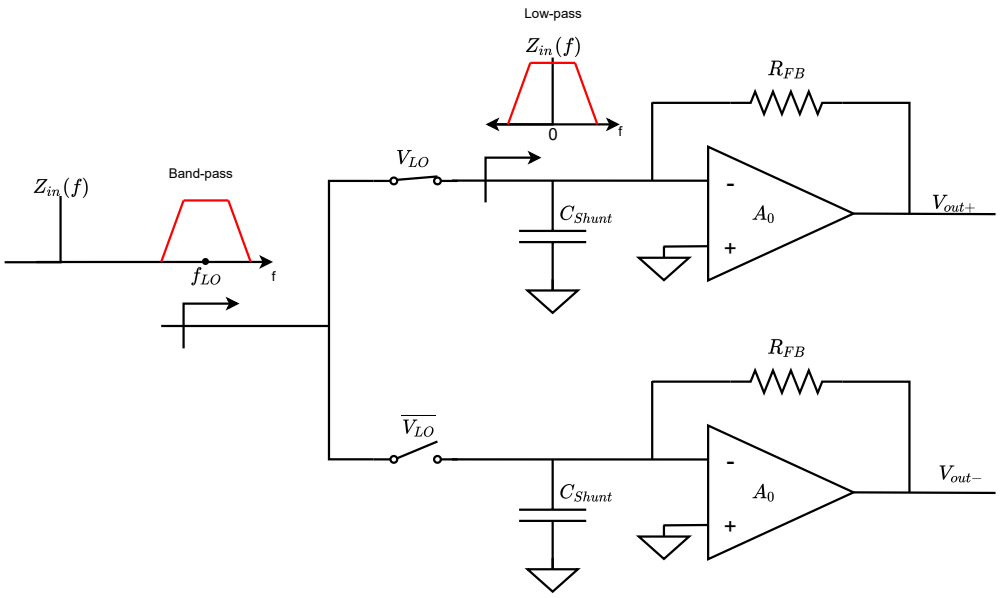

Figure 3.25: Commutating switches upconvert a low pass filter to a bandpass filter.

Linearity and output swing

For the discussion of linearity and output swing, the model of Fig. 3.24 is useful. To achieve maximum linearity, the switching transistors should have low voltage swing on their terminals. A large swing at the terminals of the transistors cause modulation of their on-resistance, which causes non-linearities. The swing on the source depends on the input impedance of the TIA ($R_{in_{TIA}}$) and the amount of current that is injected into the TIA. Figure 3.26 shows a simulation that demonstrates the dependence of the IM3 on the input impedance of the TIA.

The swing on the drain depends mainly on the resistive divider of R_{mixer} and R_{on}. It seems sensible to choose R_{mixer} at least 10 times larger than R_{on}. Figure 3.26 shows the dependence of IM3 on R_{on}. Notice that in both simulations the voltage swing at the output of the TIA did not change much. The large R_1 dominated the amount of current injected. The linearity of the switch can be further improved by shorting the bulk-source junction, avoiding the modulation of the threshold voltage by the source-bulk voltage. This requires for each transistor to be located in a separate well.

The optimal solution for linearity is to choose R_{mixer} large, R_{on} small and $R_{in_{TIA}}$ small. The $R_{in_{TIA}}$ can be reduced by reducing R_{FB} or by increasing the open-loop gain of the amplifier. The open-loop gain is constrained, it trades off with bandwidth as will be explained in more detail in the next section. Therefore, we can choose to reduce $R_{in_{TIA}}$ by reducing R_{FB}. However, the mixer's output swing benefits from a small R_{mixer} and large R_{FB}. Consequently, the choice of R_{mixer} and R_{FB} result in a trade-off of linearity and output swing. Note that a low $R_{in_{TIA}}$ not only benefits the linearity, it also improves the isolation between branches because of the reduced voltage swing at the output of the mixing core. Likewise, a large R_{mixer} benefits not only the linearity but also the power-dissipation of the system, as was made clear in subsection 3.2.3.

The R_{on} can be reduced without significantly influencing the output swing. However, a very small R_{on} will result in large parasitics and a relatively low off-impedance. This can limit the harmonic rejection and reduce isolation of the baseband signals between branches. The latter effects are not as significant as the dependence of the linearity on R_{on}.

One can argue that output swing can be traded for linearity. Because there can always be another gain stage added after the TIA to increase the output swing. Whereas it is not possible to improve the linearity later. To make the optimal choice, the whole system has to be taken into account.

Because a low $R_{in_{TIA}}$ has multiple important benefits, this will be a priority in the design. When the $R_{in_{TIA}}$ is known, the R_{mixer} and R_{on} can be chosen. Using some iterations of this process, the mixer is designed such that it just meets the linearity and harmonic rejection specifications at the maximum output swing for the given input swing.

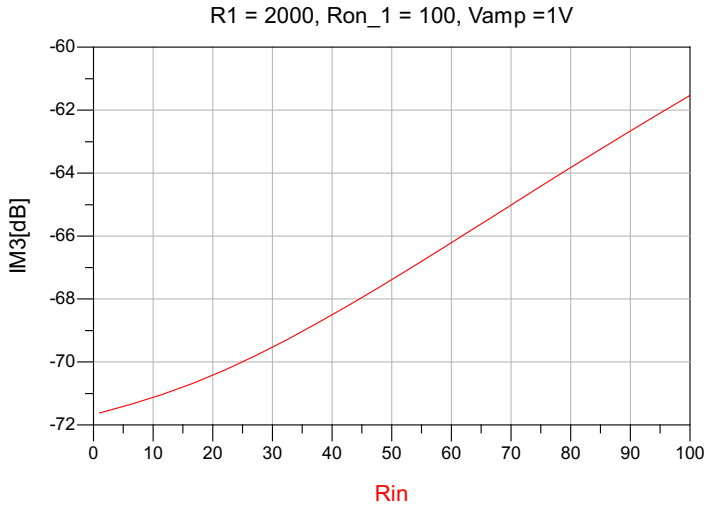

Figure 3.26: IM3 vs $R_{in_{TIA}}$

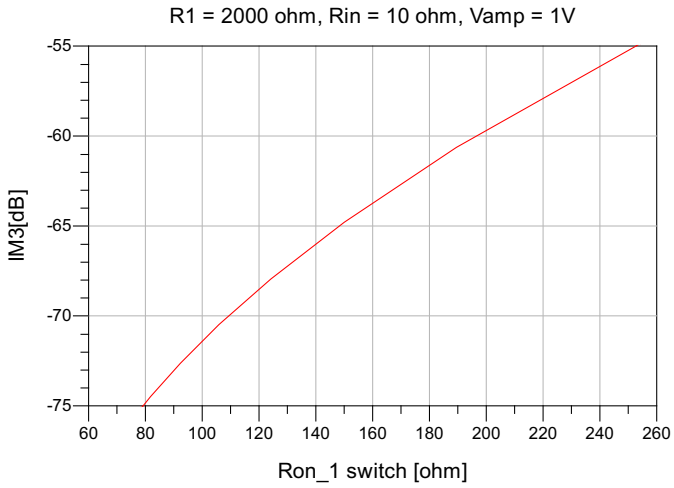

Figure 3.27: IM3 vs R_{on_1}

Harmonic rejection

The harmonic rejection is implemented by the resistors. When $R_2 = \frac{R_1}{\sqrt{2}}$, the harmonic rejection is ideally infinite for the third and fifth harmonic. However, in practise the harmonic rejection will be limited. For example, the irrational factor of $\sqrt{2}$ is impossible to implement. Additionally, the resistors are subject to random variations. When the resistors's values deviate from the intended value, the harmonic rejection will be reduced. One benefit of implementing a resistor ratio is that absolute errors are not important, only relative errors. Relative errors can be made smaller than absolute errors with careful layout design. Random errors can be lowered by increasing the size of the components.

Specific layout design is not the topic of this thesis. To still get an idea of the allowed variation in resistor ratio, a MATLAB simulation was done. In this simulation the R_2 was defined as in Eq. 3.11. The deviation was swept, resulting in the plot of Fig. 3.28. The simulation shows the aimed harmonic rejection of 40dB is still reached when R_2 is 5.5% smaller than intended. This simulation only applies to the accuracy with which the ratio of $\sqrt{2}$ needs to be implemented. A Monte-Carlo simulation can be done to account for random variation of all components.

$$R_2 = (1 - \frac{deviation[\%]}{100}) \cdot \frac{R_1}{\sqrt{2}} \tag{3.11}$$

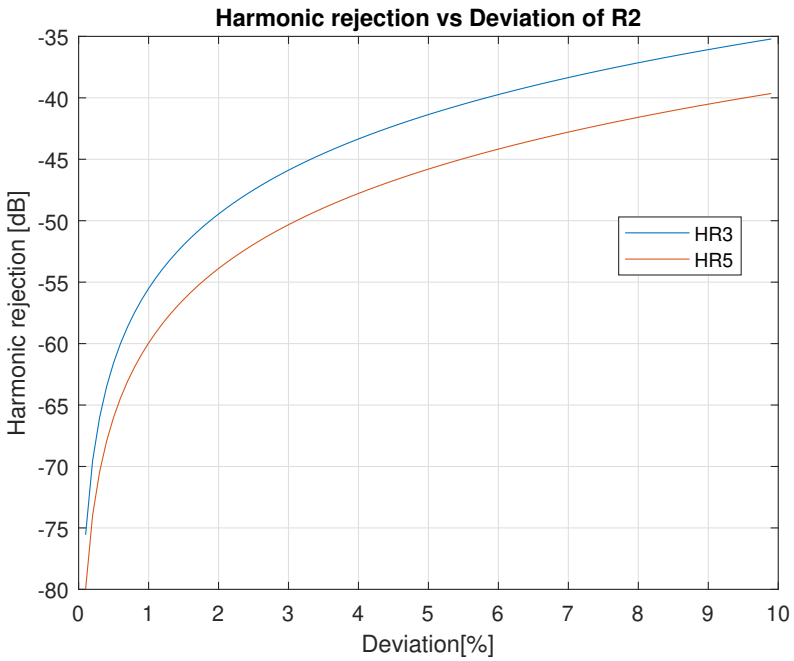

Figure 3.28: Harmonic rejection versus relative deviation of R_2

Until now, only the variation of R_2 with respect to R_1 was taken into account. Other factors to consider are the R_{on} of the switch and the $R_{in_{TIA}}$ of the TIA. Figure 3.29 shows a model that can be used to determine the proper scaling when taking R_{on} and $R_{in_{TIA}}$ into account. From Fig. 3.18 one can observe that at any moment in time, a branch with R_1 will be in parallel with a branch with R_2. For example when ϕ_1 is high, θ_1 is also high and both branches will connect to the positive side of the In-phase path(I_p). The leftover branch with R_1 will connect to the Quadrature path. At any other moment in time a similar situation occurs. The situation can be modeled as in Fig. 3.29. To implement the harmonic rejection the I_1 should be $(1 + \sqrt{2})$ times bigger than I_2 as given in Eq. 3.12. The resistors R_{on_i} model the switch resistor when a switch is on. To simplify the mixer model, the R_{on_i} is chosen to be a fraction of R_i, as is shown

in Fig. 3.29. Another way of looking at it is that $\frac{R_2}{R_1} = \frac{R_{on_2}}{R_{on_1}}$. The expressions for the currents are given in Eq. 3.14 and Eq. 3.15. Those expressions can be divided and set equal to $(1+\sqrt{2})$, as is done in Eq. 3.16. Using Eq. 3.16, R_2 can be expressed in R_1, given by Eq. 3.17. Scaling R_2 as given by Eq. 3.17 will result in perfect harmonic rejection, even for a non-zero input impedance of the TIA. When $R_{in_{TIA}} = 0$, the relation reduces to $R_2 = \frac{R_1}{\sqrt{2}}$.

There are more circuit non-idealities that can reduce the harmonic rejection, but simulations show that the aimed harmonic rejection of 40dB can be reached. Figure 3.30 shows the result of a frequency sweep at the input of the mixer. The red line indicates the frequencies around from 2.5GHz to 4.5GHz that were mixed with the fundamental of the mixing waveform and mixed back to the baseband. The blue line indicates the frequencies from 9.5GHz to 11.5GHz that were mixed with the third harmonic of the mixing waveform and mixed back to the baseband. Both lines are normalized such that the mixing with the fundamental of the mixing waveform resulted in a gain of 0dB. The plot shows that the harmonic rejection is more than 40dB for all frequencies. The simulation was performed using: $R_1 = 2000\Omega$, $R_{on_1} = 100\Omega$ and $R_{in_{TIA}} = 10$. Another observation from this plot is that the red line is almost flat within the baseband bandwidth of 1GHz.

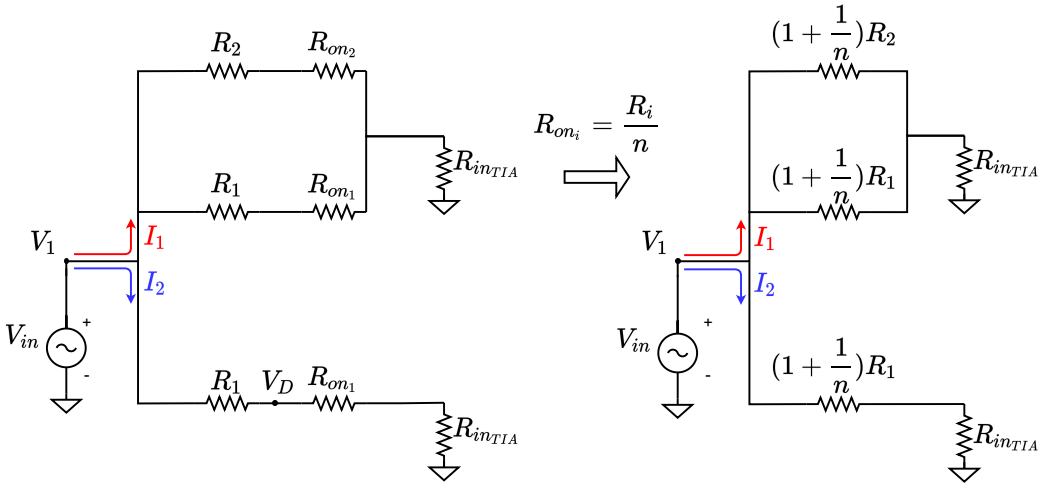

Figure 3.29: Mixer model used to choose values for R_1 and R_2, that implement the harmonic rejection.

To implement the harmonic rejection the currents must be:

$$I_1 = (1+\sqrt{2})I_2 \tag{3.12}$$

When the switches are sized such that:

$$R_{on_i} = \frac{R_i}{n}, \text{ or: } \frac{R_{on_2}}{R_{on_1}} = \frac{R_2}{R_1} \tag{3.13}$$

The currents can be expressed as:

$$I_1 = \frac{V_1}{(1+\frac{1}{n})R_1 || (1+\frac{1}{n})R_2 + R_{in_{TIA}}} \tag{3.14}$$

$$I_2 = \frac{V_1}{(1+\frac{1}{n})R_1 + R_{in_{TIA}}} \tag{3.15}$$

$$\frac{I_1}{I_2} = \frac{(1+\frac{1}{n})R_1 + R_{in_{TIA}}}{(1+\frac{1}{n})\frac{R_1 R_2}{R_1+R_2} + R_{in_{TIA}}} = 1+\sqrt{2} \tag{3.16}$$

Now R_2 can be expressed in terms of R_1 and $R_{in_{TIA}}$:

$$R_2 = \frac{(1+\frac{1}{n})\frac{R_1}{\sqrt{2}} - R_{in_{TIA}}}{1+\frac{1}{n}+\frac{R_{in_{TIA}}}{R_1}} \approx \frac{R_1}{\sqrt{2}} \tag{3.17}$$

In a final implementation the $R_{in_{TIA}}$ might deviate from the expected value. To see the sensitivity of the harmonic rejection to variation of $R_{in_{TIA}}$, a simulation was done where first R_2 was calculated with Eq. 3.17 using $R_{in_{TIA}} = 25\Omega$ and $R_1 = 2000\Omega$. Then the $R_{in_{TIA}}$ was varied without updating R_2. The result is shown in Fig. 3.31. The simulation shows that the harmonic rejection is not very sensitive to variations of $R_{in_{TIA}}$. The reason is that $R_{in_{TIA}}$ is much smaller than R_1, so R_1 dominates the expression. Most likely, the harmonic rejection is limited by more complex mechanisms, such as RC times and switch parasitics, instead of small variations in R_1. Since the harmonic rejection target could be met without problems, most of the focus in the design has been on improving the linearity.

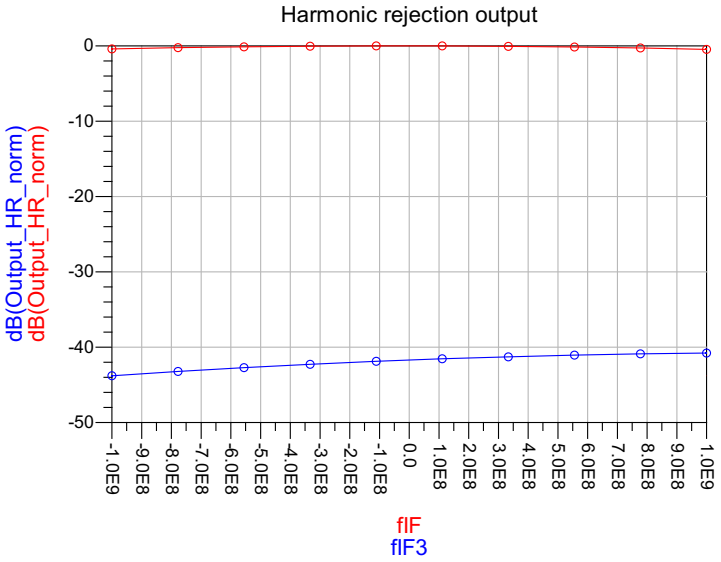

Figure 3.30: Harmonic rejection versus frequency.

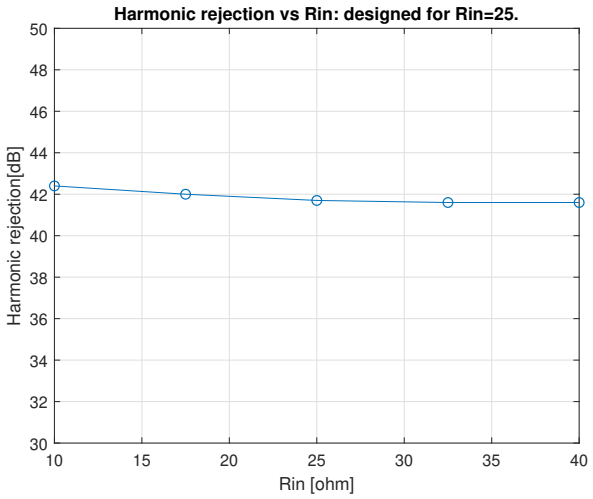

Figure 3.31: HR vs Rin. R1 much bigger than Rin, so no strong dependance.

3.3 Transimpedance amplifier

This section will go over the design of a TIA. The most essential function of the TIA is to offer a low input impedance to the mixer. The TIA will limit the bandwidth and linearity of the overall system. Therefore, the focus in the design of the TIA is on bandwidth and linearity. Furthermore, the TIA needs to offer a reasonable output swing, to take advantage of the full input range of the ADC.

3.3.1 TIA topology

A short discussion of different TIA's is given. For each TIA the R_{in}(input impedance) and R_T(Transimpedance) is given.

A simple resistor can function as a TIA, shown in Fig. 3.32. However, using just a resistor, the input impedance and transimpedance are directly coupled. Figure 3.33 shows a common-gate used as a TIA. The figure shows that the bias current is in the signal path. The advantage of the common-gate is that the input impedance and transimpedance are on approximation decoupled. The input impedance can be approximated as $\frac{1}{g_m}$ and the transimpedance is given by R_D. When the R_D is not much smaller than r_o, the input impedance and transimpedance are no longer decoupled. The g_m must be large to get a low input-impedance, but a large g_m will result in a large device and therefore, a small r_o.

Another way to implement a TIA is with a feedback amplifier, shown in Fig. 3.34. When the gain of the amplifier is large, the transimpedance and input impedance are decoupled. The use of feedback improves the linearity and makes the amplifier less prone to PVT variations. Within the same technology and comparable bandwidth, a feedback TIA will have a higher transimpedance than the common-gate approach [24]. Therefore, the feedback TIA is the preferred configuration in our system. The disadvantage of the feedback configuration is that it can potentially be in-stable, particularly when the amplifier consists of multiple stages.

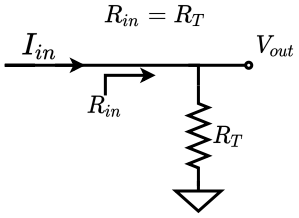

Figure 3.32: Resistor TIA

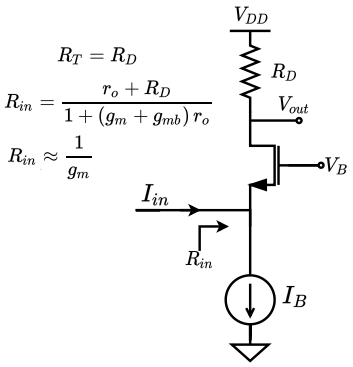

Figure 3.33: Common-gate TIA

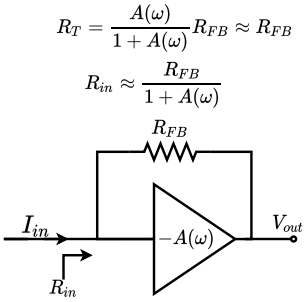

Figure 3.34: Feedback TIA

3.3.2 High-bandwidth TIA design

The last subsection concluded that the feedback setup was the most suitable in this project. The goal of this project is to design a high bandwidth TIA. This subsection explains how high bandwidth can be achieved for an amplifier. A simple common source amplifier is used as an example.

Figure 3.35 shows a common source amplifier with an ideal current source load. Figure 3.36 shows a small-signal model of the common-source amplifier. In this example, only the capacitor at the output is shown. Later subsections will discus the effect of all other parasitic capacitances.

The gain from input to output is the product of its transconductance and its output impedance. The gain does not depend on the device's width; when the device is made wider, g_m goes up but r_o goes down proportionally. The output capacitance will result in a pole at the output, the pole frequency depends on the output capacitance and the output impedance. When the load capacitance dominates the output capacitance, the bandwidth can be increased by sizing up the device. However, when the device's parasitics dominate

the output capacitance, the output pole is approximately constant. When the device is made wider, the r_o goes down but the C_{out} goes up proportionally.

The remaining design parameters are the channel length and overdrive voltage. By increasing the channel length, the r_o goes up, and therefore the intrinsic gain will increase. However, increasing r_o will decrease the frequency of the output pole. By increasing the overdrive voltage, g_m goes up. Increasing g_m, increases the gain and does not influence the bandwidth, breaking the gain-bandwidth trade-off. However, increasing the overdrive voltages costs power.

This gain-bandwidth trade-off can be formalized by considering the gain-bandwidth (GBW) product. The GBW can be found by multiplying the gain and bandwidth, shown in Eq. 3.18. For a one-pole system, GBW is equivalent to the unity-gain frequency, the frequency where the amplifier has a gain of one. Consequently, the GBW gives an upper limit for the -3dB frequency of an amplifier. When the output capacitance is dominated by the parasitic capacitance the GBW can be approximated with Eq. 3.19. Observe that the GBW improves with overdrive voltage and deteriorates with channel length. These equations are approximations. In a short channel device in velocity saturation, the L^2 becomes L. Furthermore, the mobility μ becomes a function of the overdrive voltage.

To conclude, when one wants to increase the gain, increasing the channel length is more power efficient than increasing the overdrive voltage. But when designing for high bandwidth, one might have no other choice than to increase the overdrive voltage.

One can also use a cascode structure to increase the output impedance. Cascoding does not lower the GBW, but it also does not break the GBW trade-off. Consequently, cascoding trades gain for bandwidth. Furthermore, when the amplifier has a resistive load, boosting the intrinsic output impedance of the amplifier is not effective. A cascode structure would be beneficial when one wants to reduce the miller effect, but that is unnecessary for this project.

Another way of increasing the gain is by cascading multiple stages. The output stage can be used as a buffer, such that the gain is not lowered by a resistive load. However, a multistage approach requires stabilization techniques that compromise the bandwidth. Consequently, in this project the focus is one a one-stage approach.

The GBW of a device can we approximated as:

$$GBW = A_0 BW = g_m r_o \cdot \frac{1}{r_o C_{out}} = \frac{g_m}{C_{out}} = \mu C_{ox} \frac{W}{C_{out}} \frac{V_{gs} - V_T}{L} \tag{3.18}$$

When the output capacitance is dominated by the device's capacitance:

$$GBW \approx \mu C_{ox} \frac{W}{\frac{2}{3} W \cdot L C_{ox}} \frac{V_{gs} - V_T}{L} = \mu \frac{3}{2} \frac{V_{gs} - V_T}{L^2} \tag{3.19}$$

After choosing the overdrive voltage, the L can be used to compromise between gain and bandwidth (λ' is a technology parameter):

$$A_0 = g_m r_o = \frac{2L}{\lambda'(V_{gs} - V_T)} \tag{3.20}$$

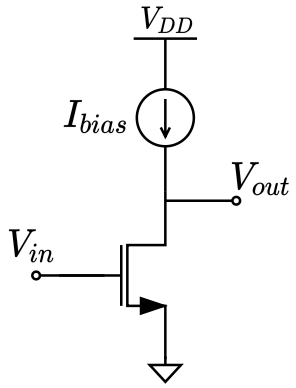

Figure 3.35: Common-source amplifier

$$A_o = g_m r_o \qquad \omega_{p_{out}} = \frac{1}{r_o C_{out}}$$

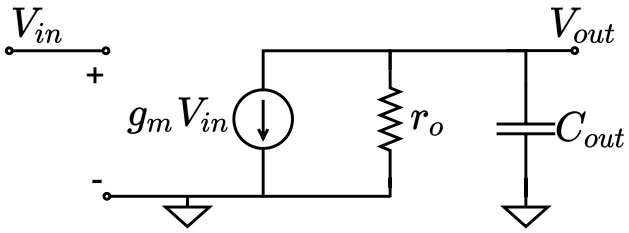

Figure 3.36: Small signal model CS

3.3.3 Inverter based TIA

The last subsection demonstrated that the GBW of an amplifier directly depends on its transconductance. An efficient way of getting a high transconductance is by using an inverter as an amplifier. The inverter's gain benefits from the transconductance of both the NMOS and the PMOS input devices. Therefore, this project will make use of an inverter-based TIA.

Figure 3.38 shows a TIA based on an inverter, the DC level can conveniently be set with the feedback resistor. The feedback will bias the inverter in the middle of its voltage range, where it has the maximum gain. A disadvantage of the inverter-based amplifier is that it is sensitive to power supply noise. To understand this, please observe Fig. 3.37. The V_{gs} of the PMOS device is between V_{in} and V_{DD}. Unfortunately, this means that the power supply noise is amplified. The power supply rejection can be improved by moving to a fully differential design. Figure 3.39 shows a fully-differential design. Such a fully-differential setup needs a common-mode-feedback(CMFB). This fully-differential amplifier has been confirmed to work in simulations both separate and in combination with the mixer. However, due to time constraints the simulation results in this thesis were created by using a pseudo-differential setup consisting of two single-ended amplifiers.

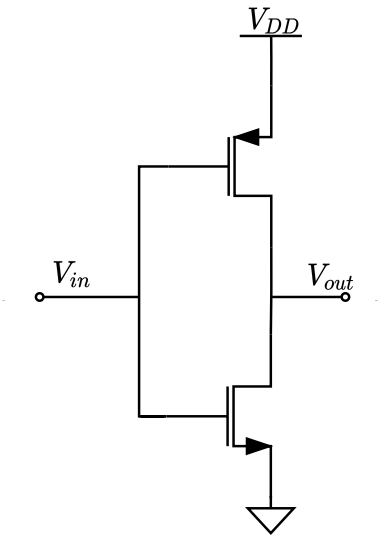

Figure 3.37: Inverter

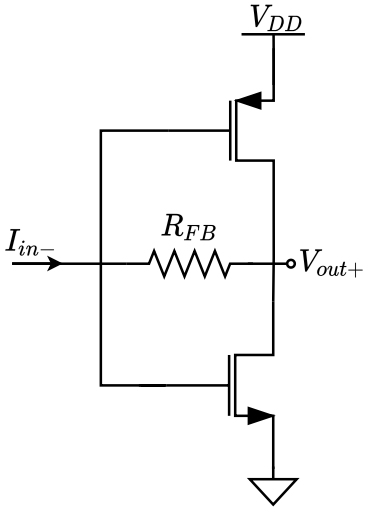

Figure 3.38: Inverter based TIA

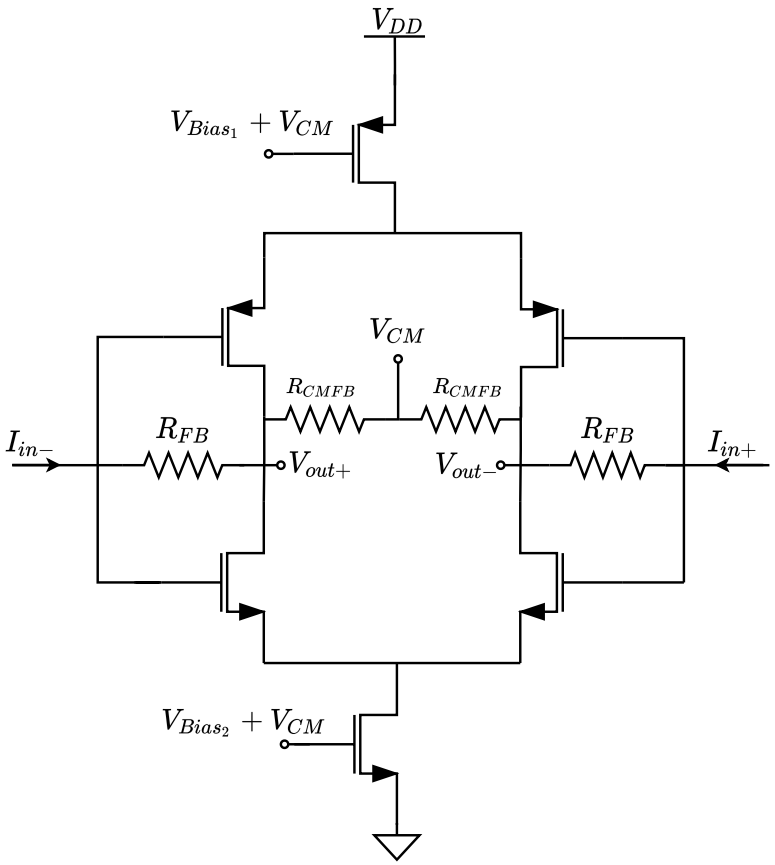

Figure 3.39: Fully differential inverter based TIA

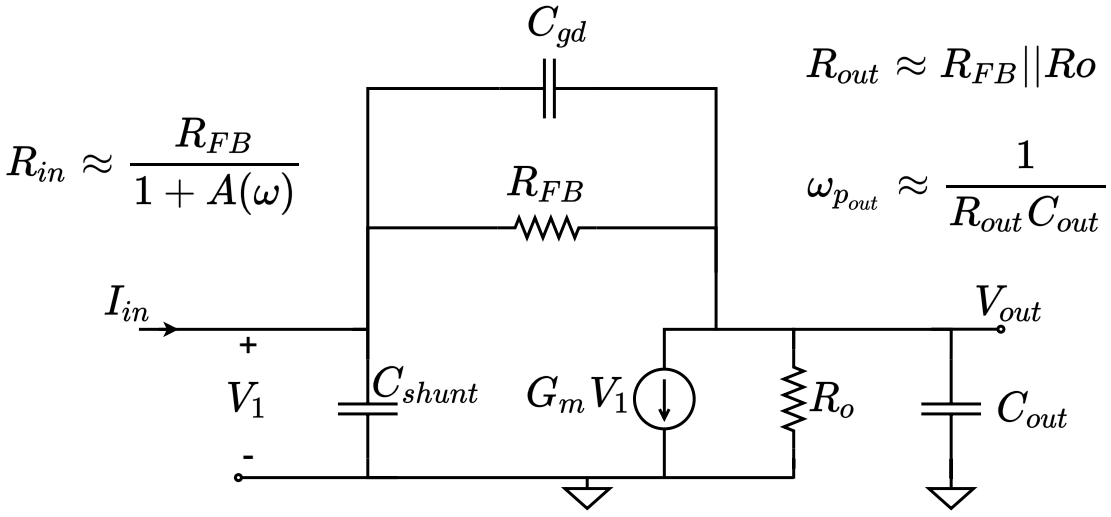

Figure 3.40: Small signal model TIA

Figure 3.40 shows a small-signal model of an inverter-based TIA. The capital G_m and R_o refer to the combined transconductance and output impedance of the PMOS and NMOS devices. The model includes the capacitor at the input C_{shunt}. This capacitor is needed in the mixer. Furthermore, the parasitic feedback capacitance C_{gd} is shown. This capacitor, though relatively small, will cause a significant input capacitance

due to the miller effect. The feedback capacitance can be converted to an input capacitance by multiplying by (1+A) to simplify the small-signal model. This miller capacitance can then be lumped together with C_{shunt} and parastics such as C_{gs}, to get a total input capacitance C_{in}. The resulting small-signal model is shown in Fig. 3.41.

The relatively large C_{in} causes a second pole at the input. The input pole is limiting the bandwidth. A two pole transfer, with the input pole determining the bandwidth, is shown in Fig. 3.42. In case of an two-pole system in feedback, one has to be careful of instability. The second pole must lie sufficiently far beyond the point of 0dB gain, to have enough phase-margin. The maximum frequency of the output pole depends on the GBW of the amplifier. Consequently, the input pole is indirectly limited by the GBW of the amplifier. The simplified small-signal model does not explicitly show C_{gd}, however it is still there and introduces a zero in the TIA's transfer function. This zero will make it easier to achieve enough phase margin.

$$C_{in} \approx C_{shunt} + C_{gs} + (1+A)C_{gd}$$

$$R_{in} \approx \frac{R_{FB}}{1+A} \qquad A_o = G_m R_{out} \qquad R_{out} \approx R_{FB} || Ro$$

$$\omega_{p_{in}} \approx \frac{1}{R_{in} C_{in}} \qquad \omega_{p_{out}} \approx \frac{1}{R_{out} C_{out}}$$

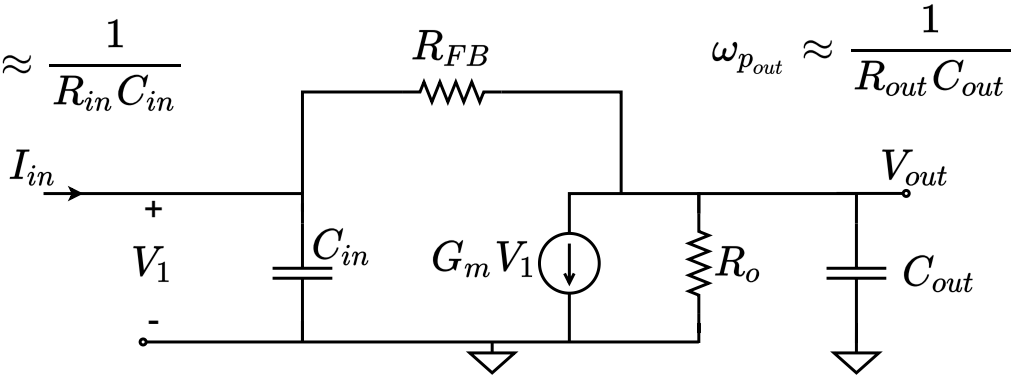

Figure 3.41: Simplified small signal model TIA

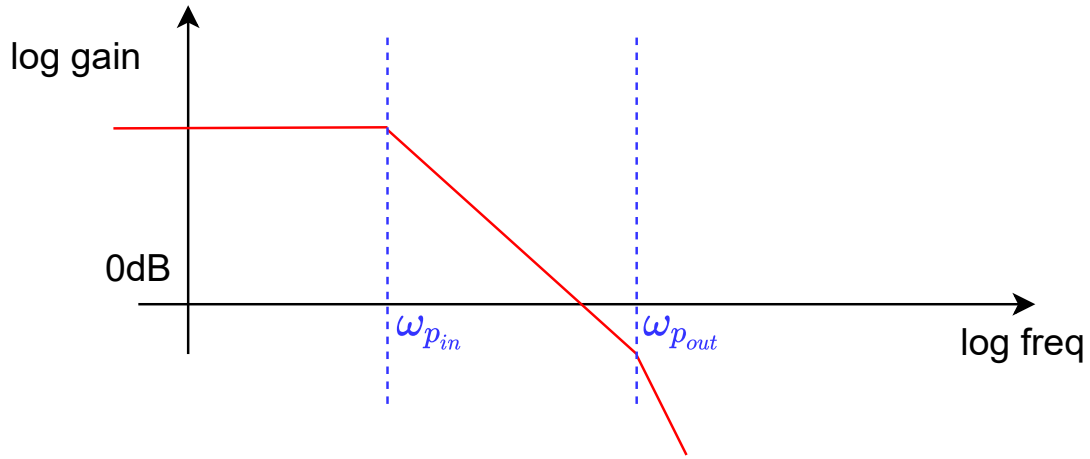

Figure 3.42: Two pole system, the bandwidth is limited by the input pole. To guarantee stability, the output pole must lie beyond the 0dB point

3.3.4 Design

The last subsection introduced the topology of the inverter-based amplifier. This subsection will go over the design. The input bandwidth of the amplifier must be 1GHz, given by the requirements of the mixer. The design strategy is to put the input pole at 1GHz, and choose the GBW such that the output pole lies far enough beyond 1GHz. Effectively, this boils down to choosing the transconductance high enough.

In this thesis, the M factor is used to scale devices, to simplify the initial design. The starting point is an NMOS of 2um width and 80nm channel length. This device is characterized using DC simulations. The transconductance trades with power efficiency, as is shown in Fig. 3.43. The red line shows the g_m and the blue line shows $\frac{g_m}{I_d}$. Observe that a higher g_m results in a decreased $\frac{g_m}{I_d}$, and therefore, lower power efficiency. Another factor to consider is linearity. Figure 3.44 shows the second and third derivative of the current vs V_{gs}. The graph shows that the third-order non-linearity can be minimized by choosing V_{gs} approximately equal to 650mV. The graphs look similar for the NMOS and PMOS. The bias point of 650mV is high enough to meet the GBW requirement, so this will be the bias point in this thesis. If the bias point of 650mV was not high enough to meet the GBW requirement, the channel-length could have been reduced. The PMOS is chosen 2.52 wider to match the current of the NMOS. The resulting amplifier' transconductance and output impedance are 1.5mS and 11.7kΩ respectively, resulting in an open-loop gain of 17.6. Note that this open-loop gain is too low to guarantee an accurate closed loop gain. Consequently, the closed-loop gain must be calibrated, which could be achieved by tuning the feedback resistor.

The feedback resistor in the TIA is chosen 250Ω, this choice is made by considering all requirements; such as input impedance, transimpedance, and power-dissipation. The resistive load lowers the output impedance of the TIA, to counter this, the amplifier is sized up with a factor 75, resulting in a quiescent current of 5.6mA per branch. Consequently, the power dissipation of a branch is $5.6mA \cdot 1.3V = 7.3mW$. In the fully-differential implementation of Fig. 3.39, another 160mV is needed to fit a current source. Consequently, the total power dissipation becomes $2 \cdot 5.6mA \cdot (1.3V + 2 \cdot 160mV) = 18.1mW$.

Note that if we wanted to decrease the input impedance by a factor two, the feedback resistor must be reduced by a factor of two. Now the power dissipation must be doubled to get approximately the same open-loop gain. Additionally, the trans-impedance, and therefore the output swing, would be reduced with a factor of two. Various linearization techniques were considered to improve the TIA's output linearity. However, these techniques lead to a reduction of the open-loop gain, which ultimately was not worth the trade-off.

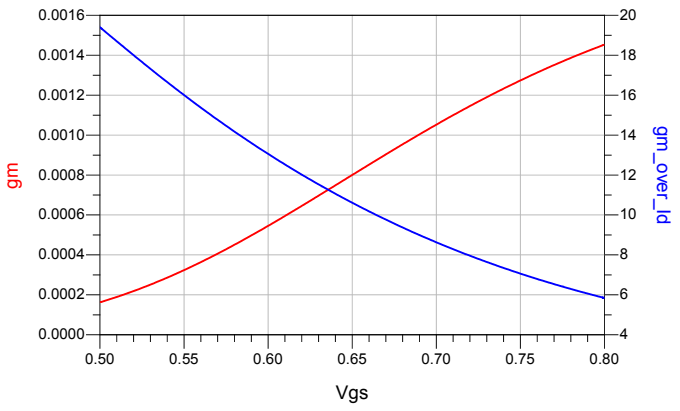

Figure 3.43: g_m and $\frac{g_m}{I_d}$ vs V_{gs}

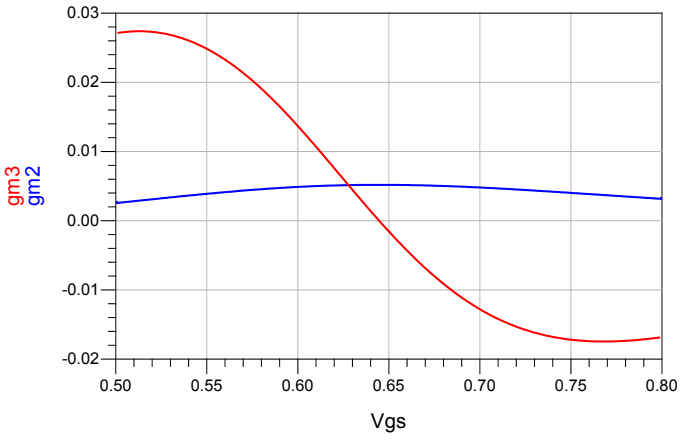

Figure 3.44: g_{m2} and g_{m3} vs V_{gs}

3.3.5 TIA simulations

Now, the simulation results of an inverter-based TIA will be presented. Figure 3.24 showed a mixer model that combines all branches of the mixer into a single branch, the resulting model looks like a feedback amplifier. The mixer can be viewed as a feedback amplifier, with a time-varying feedback network. Simulations of the final mixer show that the mixer has a voltage gain of $\frac{1}{3}$, from input of the mixer to the output of the TIA. Therefore, in this section the designed amplifier is simulated as a feedback amplifier with a feedback factor of $\frac{1}{3}$. The setup is shown in Fig. 3.45.

Figure 3.46 shows the closed-loop transfer. A C_{shunt} of 1pF placed the -1dB point at 1GHz and the -3dB frequency at 1.86GHz. Figure 3.47 shows the input impedance versus frequency. The input impedance is 22Ω and decays when the input capacitance becomes dominant. To check the stability, a step function is applied in transient. Figure 3.48 shows the step did not result in any ringing. This design leaves some room to increase the load capacitor without it causing instability. Alternatively, the channel length could be slightly increased to achieve a higher open-loop gain.

Finally, the linearity is tested by applying a two-tone. The amplitudes of the input tones were chosen such that the TIA has a $1V_{pp}$ differential output swing. Figure 3.49 shows the resulting normalized output spectrum, a linearity of 63.2dB is achieved. Interestingly, the current injected into the TIA has a linearity of over 79.5dB, shown in Fig. 3.50. Indicating that the linearity is limited at the output of the TIA.

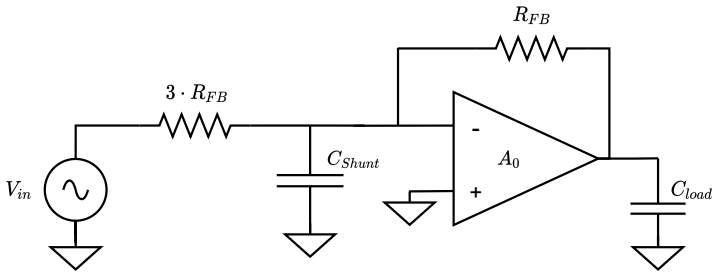

Figure 3.45: Simulation setup of designed TIA

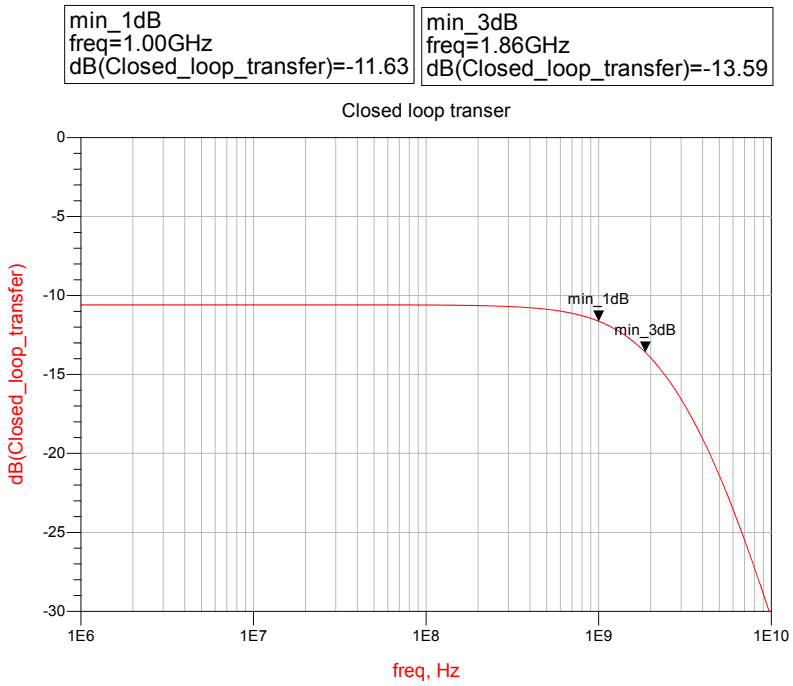

Figure 3.46: Closed loop simulation

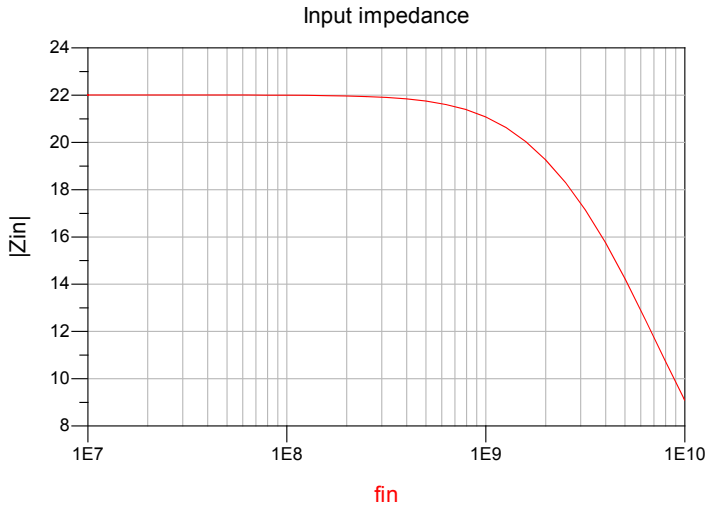

Figure 3.47: Input impedance simulation

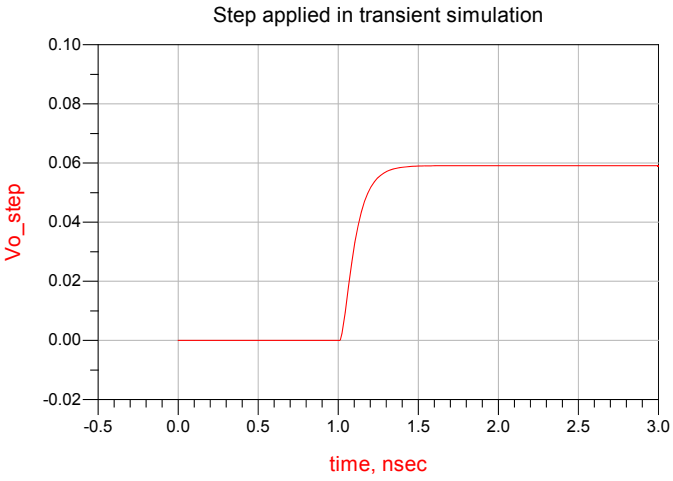

Figure 3.48: Step function applied in transient sim

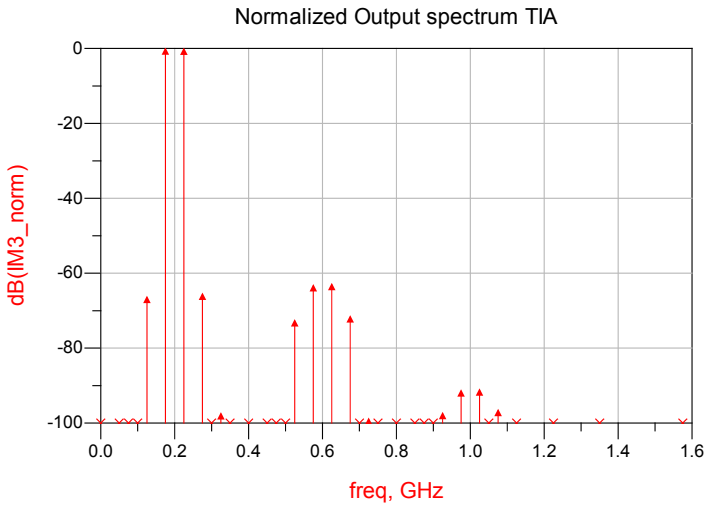

Figure 3.49: Output spectrum TIA

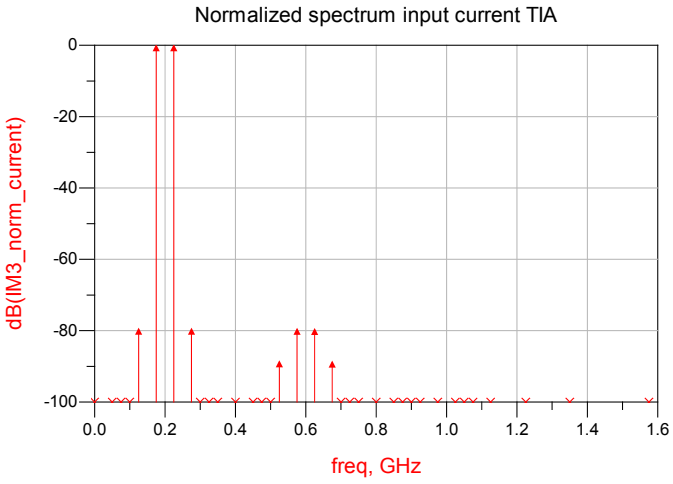

Figure 3.50: Spectrum input current TIA

3.4 Mixer simulations with designed TIA

Now, the simulations of the mixer using the designed TIA of section 3.3 are presented. Section 3.3.5 mentioned the R_{FB} was chosen to be 250Ω, this choice was made by taking the whole system into account. The R_1 is chosen to be 1500Ω and the R_{on_1} is 50Ω. Consequently, the input impedance of the mixer is roughly 470Ω. Simulations of the final mixer show that the mixer has a voltage gain of $\frac{1}{3}$.

Figure 3.51 shows the result of a frequency sweep at the input of the mixer. The red line indicates the signals from 2.5GHz to 4.5GHz, that were mixed with the fundamental of the mixing waveform back to the baseband. The bandwidth specification of 1GHz is met. The blue line indicates the signals from 9.5GHz to 11.5GHz, that were mixed with the third harmonic of the mixing waveform back to the baseband. Both lines are normalized such that the mixing with the fundamental corresponds to 0dB in the plot. The plot shows that the harmonic rejection is 40dB.

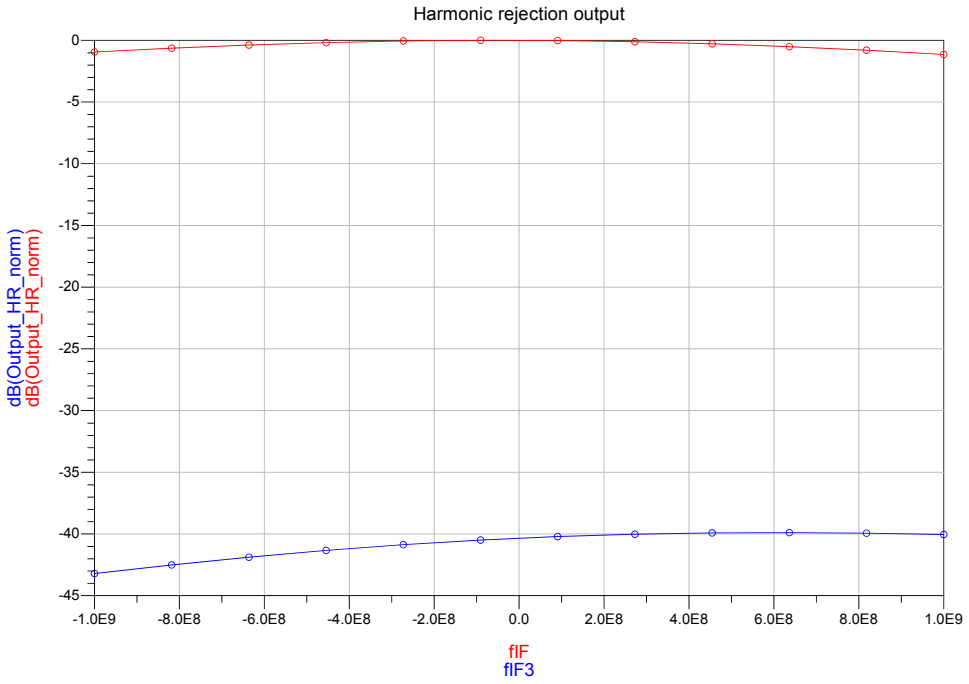

Figure 3.51: Harmonic rejection vs frequency

Figure 3.52 shows the normalized output spectrum of the mixer, this figure shows that the linearity specification of 65dB is met. However, this linearity was not achieved at $1V_{pp}$ output swing. Figure 3.54 shows the magnitude of the output spectrum. It shows that both tones have 179mV amplitude at the output. This results in a total output amplitude of 358mV and consequently, 716mV_{pp}. Again, the current injected into the TIA has a better linearity, shown in Fig. 3.53. The mixer almost achieves the aimed 65dB at $1V_{pp}$. Therefore, with a slight concession this mixer could be used in the conventional direct downconversion architecture of Fig. 2.4.

When the ADC has an input range of $1V_{pp}$, it must have an SFDR of $65dB + 2.9dB = 67.9dB$, to sample the output of the TIA with an SFDR of 65dB. The additional 2.9dB is calculated as follows: $20log(\frac{0.716}{1}) = 2.9$.

To compare the linearity to other work, the (In-Band)IIP3 and IP1dB were simulated. These simulations calculate the IIP3 and IP1dB in dBm by using the voltage swing and assuming a 50Ω impedance. Figure 3.56 shows the simulation done to find the IIP3 and Fig. 3.57 shows a zoomed in view to find the IP1dB. The mixer achieves an IIP3 of 49dBm and an IP1dB of 22dBm. These specifications are a significant improvement over the IIP3 of 30dBm and IP1dB of 10dBm reported by Kibaroglu [23] and El-Aassar [22]. Figure 3.56 shows that for high power the IM3 increases more rapidly versus input power. This can be

explained by noting that for very high power the switches in the mixer no longer behave as switches. For low input power the linearity is limited by the TIA, whereas for high power the linearity is limited by the mixing core.

Figure 3.55 shows the normalized output spectrum, now for a much wider frequency range. One can observe a strong tone present at 7.175GHz. This can be explained by remembering that the mixer works as a multiplier. This multiplication will result in downconversion, but also upconversion. This upconverted signal is filtered at the input of the TIA. However, 7GHz is only 2 octaves higher than the filter cutoff of 1.8GHz. Consequently, additional anti-aliasing is needed.

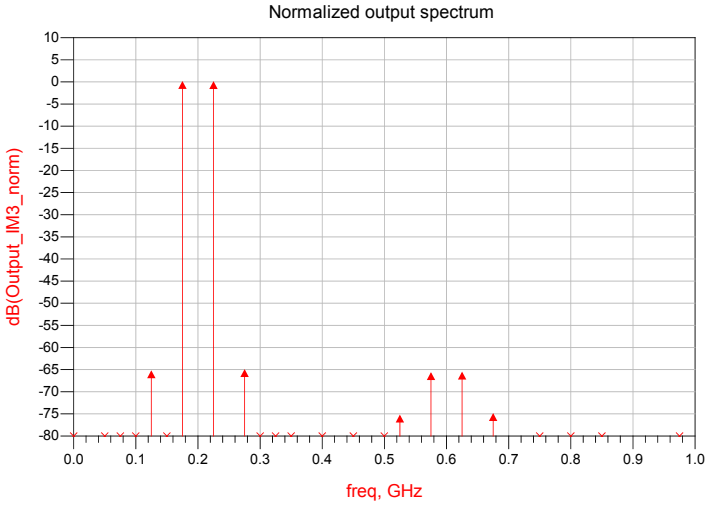

Figure 3.52: Output spectrum TIA

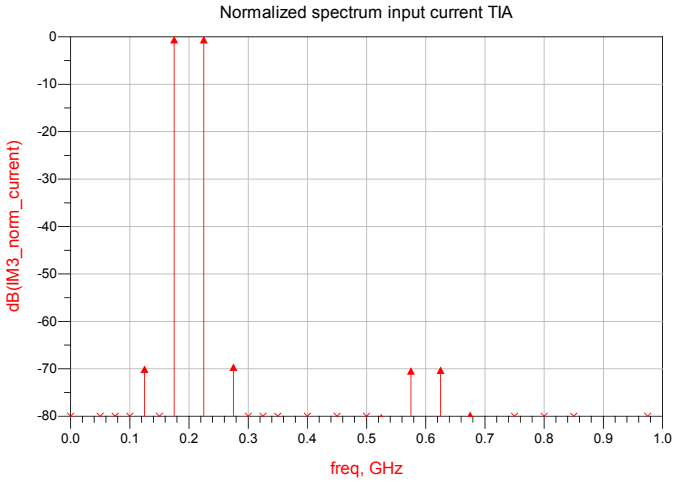

Figure 3.53: Spectrum input current TIA

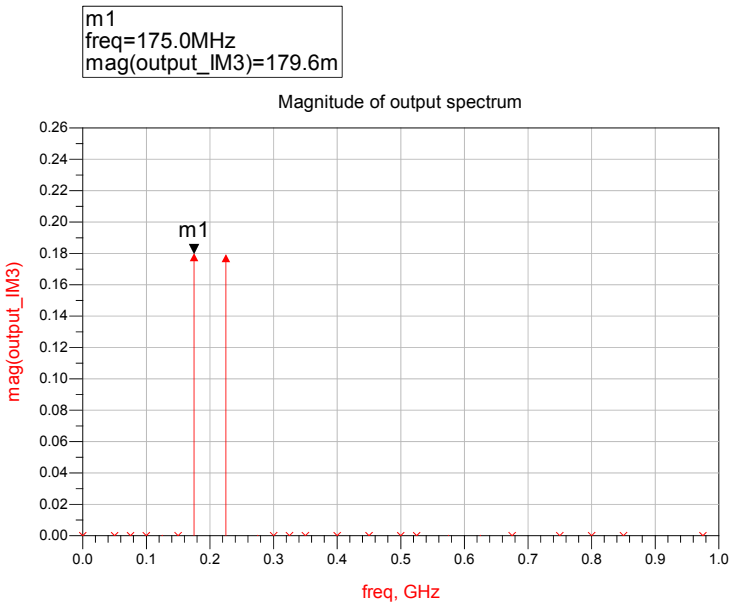

Figure 3.54: Magnitude of output spectrum mixer

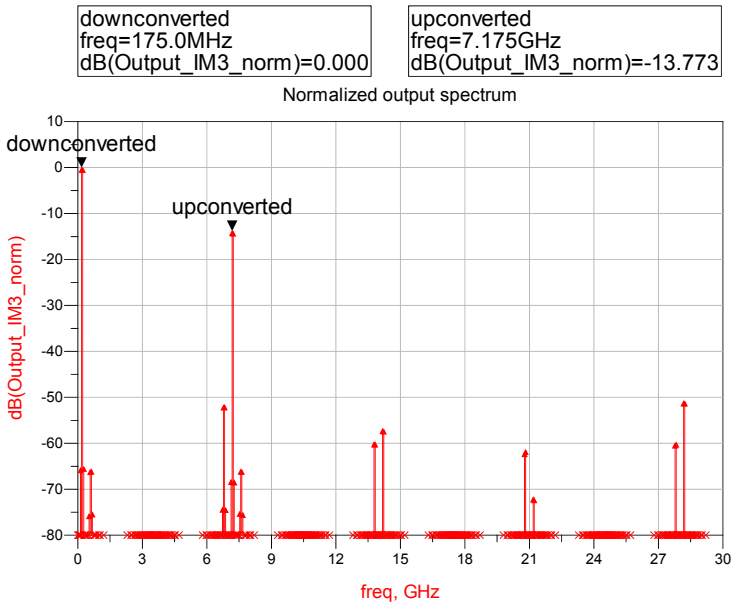

Figure 3.55: Output spectrum, up to 30GHz

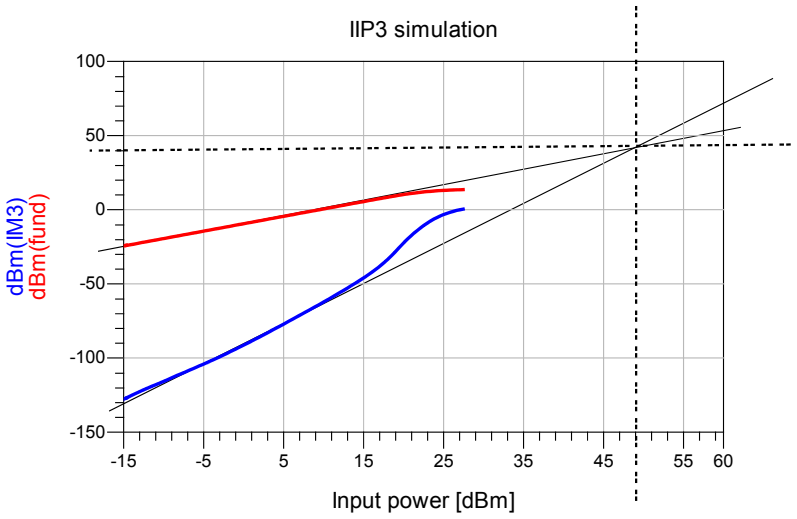

Figure 3.56: IIP3 simulation

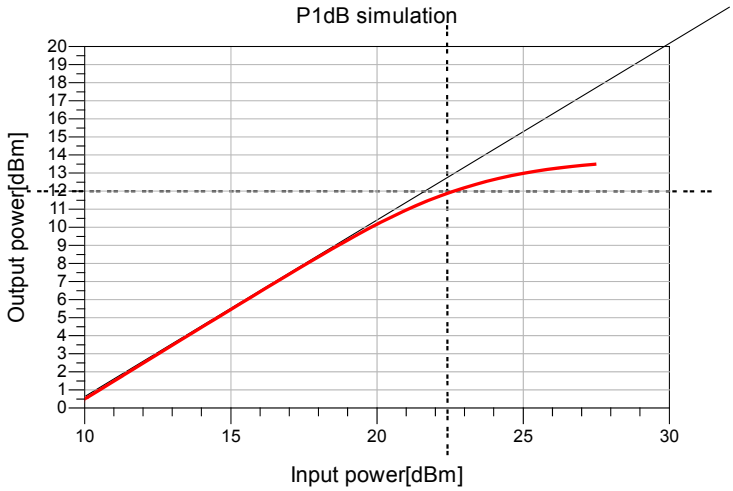

Figure 3.57: P1dB simulation

3.5 Conclusion

A highly linear harmonic rejection mixer was presented. The mixer rejects up until the 7^{th} harmonic with 40dB, and its continuous-time operation avoids aliasing. The presented mixer achieves 65dB linearity at 716 mV_{pp} differential output swing with a bandwidth of over 1GHz. The simulated IIP3 is 49dBm, a significant improvement over any published work. The mixer implements linear harmonic rejection by scaling the input current with resistors. The presented design combines the In-phase and Quadrature parts to present a constant input impedance. Additionally, the smart combination of branches with complementary clocks further improves linearity and harmonic rejection. As part of the passive mixer, a TIA was designed. The low input impedance presented by the TIA decreases the swing on the switches, increasing the linearity. Furthermore, constant input impedance and low swing at the input of the TIA largely prevents interaction of the downconverted signals between different branches. The TIA is implemented with an inverter to benefit from the transconductance of both the NMOS and PMOS. The TIA is biased for optimal linearity and reaches 1.8GHz of bandwidth. The relatively limited open-loop gain results in a limited accuracy of the closed loop gain. Consequently, the closed-loop gain must be calibrated. A fully-differential implementation of the TIA uses 18.1mW of power.

4 Circuit level implementation of the error-measurement architecture

The error measurement architecture has been introduced in section 2.3. This chapter will present the circuit level implementation of the error-measurement architecture. First, a short recap is given of the architecture. Section 4.1 will show a circuit-level implementation of the architecture, while section 4.2 its simulation results, using the mixer designed earlier in this thesis. Sections 4.3 and 4.4 will discuss BBDAC and ADC resolution requirements, taking into account various circuit-level issues in the error-measurement architecture. Section 4.5 will give the conclusions for the proposed architecture.

The RFDAC's linearity is estimated to be between 30dB and 65dB. This knowledge of a minimum linearity of 30dB can be used to design a measurement system with a 30dB reduced dynamic range. The 30dB reduction can be achieved by subtracting the output of the RFDAC from an ideal reference DAC. The error-measurement system therefore needs a $65dB - 30dB = 35dB$ dynamic range after subtracting. Next, a circuit implementation is presented.

4.1 Implementation of the error-measurement architecture

Chapter 3 showed that the TIA is the limiting factor when requiring high linearity and bandwidth at an output swing of $1V_{pp}$. Simulations showed that the linearity at the input of the TIA was significantly better than at the output. The TIA has a trade-off between input-impedance, output swing, bandwidth and linearity. The error-measurement architecture can improve the trade-off because it only requires high linearity before subtraction. After subtraction, the linearity requirement is only 35dB.

A simplified circuit-level implementation of the error-measurement architecture is shown in Fig. 4.1. The passive mixer topology consists of a mixing core that produces a baseband current and a TIA that converts the current to an output voltage. Similarly, a BBDAC can be created with switched current sources and a TIA that converts the current to an output voltage. The proposed error-measurement architecture performs the subtraction in the current domain and shares the TIA between the passive mixer and the BBDAC. After subtraction, a small I_{error} current will be injected into the TIA. Because the RFDAC has a minimum linearity of 30dB, the I_{error} will be at least 30dB smaller than I_{BB}. Consequently, the input and output voltage swing of the TIA will be reduced by 30dB. The low input swing will benefit the linearity of the mixer, and importantly, the linearity of the BBDAC. Also the isolation between branches will benefit from the reduced voltage swing of baseband signals in the mixing core. The small output swing of the TIA must be amplified to be brought up to a reasonable voltage swing. Fortunately, since this amplification happens after the subtraction, the amplification can happen with a reduced linearity. The additional gain stage can be combined with an active anti-aliasing filter.

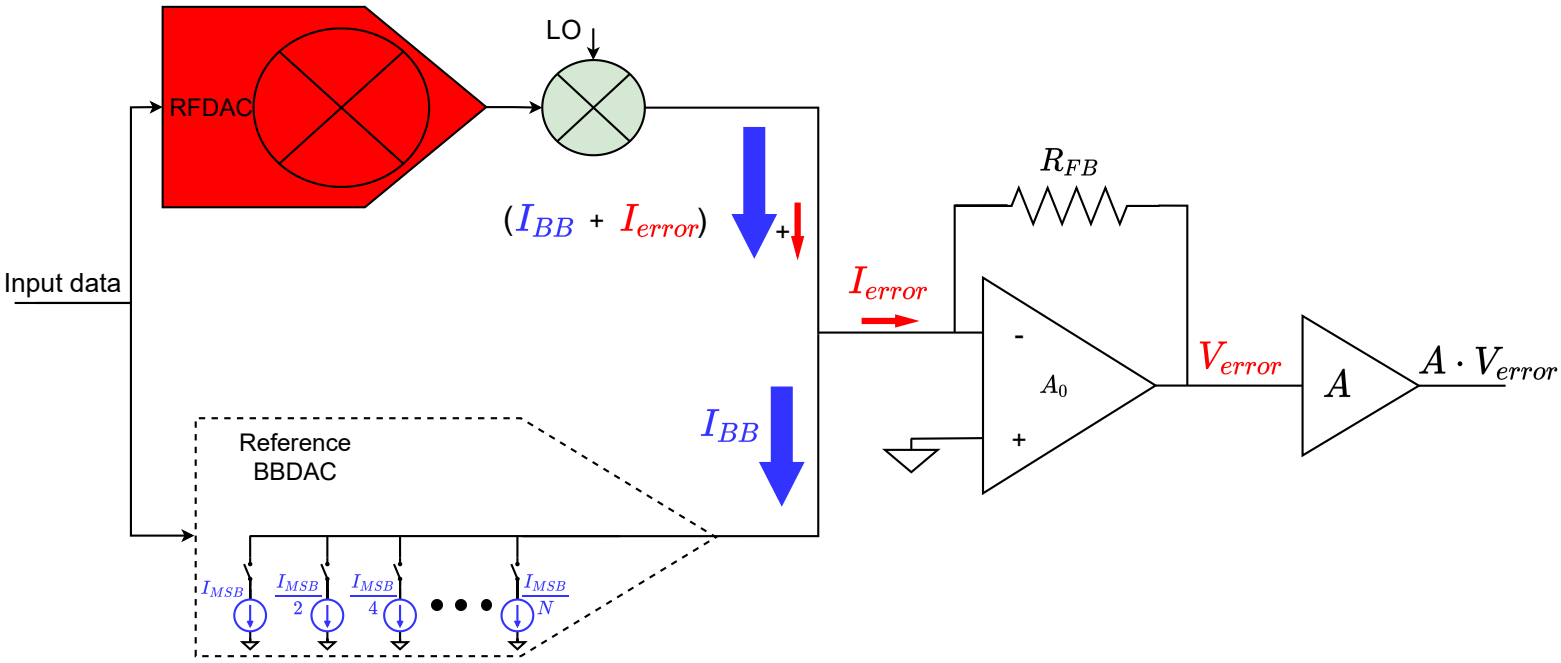

Figure 4.1: Error-measurement architecture, the subtraction is performed before the TIA

4.2 Demonstration error subtraction in the circuit simulator

To demonstrate the concept on the circuit level, a simulation has been performed in ADS. This simulation aims to be very similar to the MATLAB simulation presented in subsection 2.3.2. But in this case, the actual mixer is used, and the subtraction is done on the circuit level. Analog sources create the input signals in the simulation because they are practical in a harmonic balance simulation. Analog sources can model the RFDAC and BBDAC because the assumption is that the quantization error is negligible.

Similar to the MATLAB simulation, a signal is defined that models the output of the RFDAC. This RFDAC signal is then downconverted to the baseband. After downconversion, the signal of the BBDAC is subtracted in the current domain. The resulting current signal is injected into the TIA, which converts it to an output voltage. The RFDAC signal is created in ADS by upconverting a baseband tone with an ideal multiplier. After the multiplication, a non-linearity is applied. The resulting RFDAC signal is shown in Fig. 4.2. This RFDAC signal is used as the input to the mixer that is designed for thesis. The mixing core produces an output current, shown in Fig. 4.3. At the output of the mixing core, a current signal supplied by the BBDAC is substracted, the output current of the BBDAC is shown in Fig. 4.4. After subtraction, the remaining current is injected into the TIA. In Fig. 4.5 the output of the TIA is shown. An ideal TIA(with 22Ω input impedance) is used in this simulation, so the output voltage has the same linearity as the input current.

The simulation results look similar to the results of the MATLAB simulation. The output of the mixer shows a downconverted signal with the main tone at 100MHz, and an intermodulation tone at 300MHz that is about 50dB weaker. After subtraction the tone at 300MHz is more than 25dB stronger than the tone at 100MHz. Assuming the subtraction did not affect the tone at 300MHz, the subtraction reduced the power of the tone at 100MHz by more than 70dB. In a final implementation, the BBDAC and output of the mixer must be matched in amplitude and phase, to perform the subtraction. A complicating factor is that the non-linearity of the RFDAC, will influence its output power. Since the non-linearity of the RFAC is not known beforehand, the amplitudes must be matched by iterating. In the MATLAB simulation, an iterative procedure was implemented, that adjusted the gain of the BBDAC until the signal after subtraction was minimized. In the circuit level simulation, no such automated procedure was implemented. The phase and amplitude of the BBDAC were tuned manually, until the presented results were reached. The simulation

results show that the mixer designed in this thesis can be used in the error-measurement architecture.

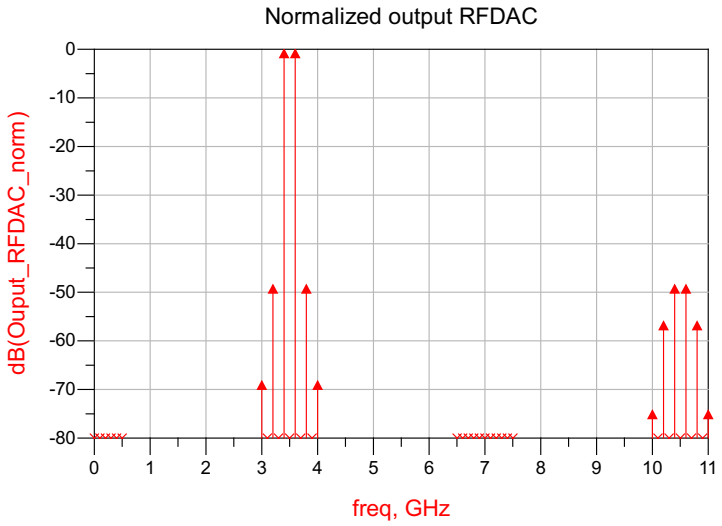

Figure 4.2: Normalized signal that models the RFDAC

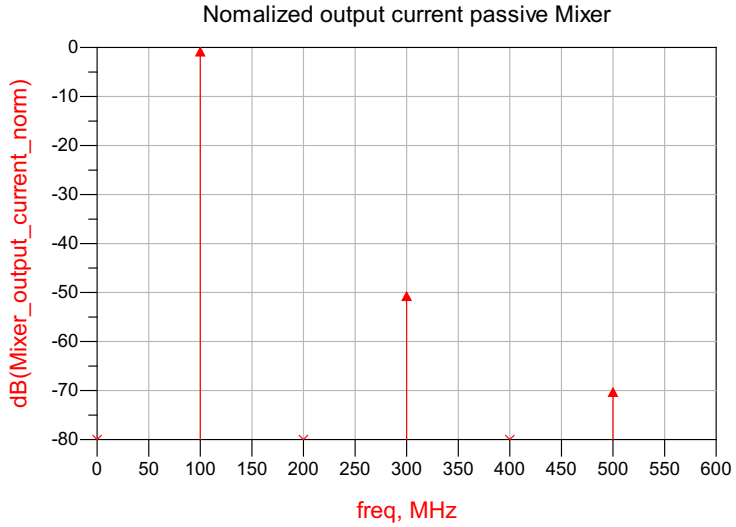

Figure 4.3: Normalized output current of mixing core

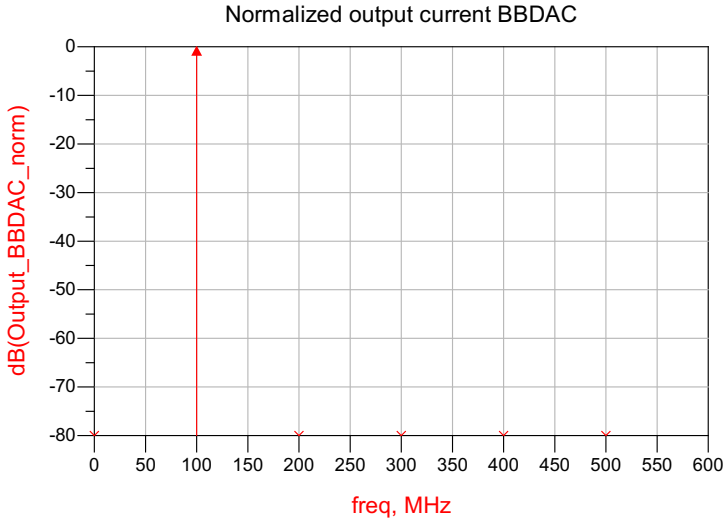

Figure 4.4: Normalized output current BBDAC

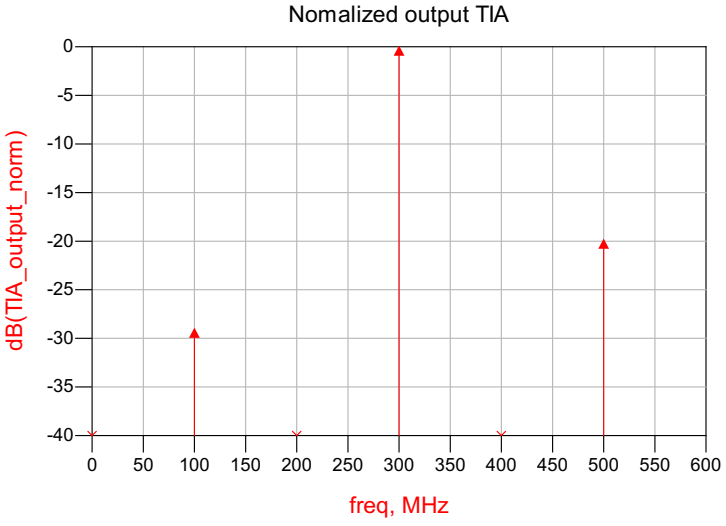

Figure 4.5: Normalized output TIA

4.3 Required resolution of BBDAC

The function of the BBDAC is to produce an ideal reference signal. The intermodulation must be negligible, compared to the linearity of the overall system. The BBDAC benefits from the low voltage swing at its output, enabling high linearity.

The spurs that the BBDAC produces are caused by errors in the differential-non-linearity(DNL). One might wonder, if the ADC that measures the error has a dynamic range of over 35dB. Then perhaps the BBDAC does not need to have a very high resolution, as long its DNL is very good and as long as the quantization error is not bigger than the error caused by the non-linearity of the RFDAC.

However, this way of thinking is flawed for multiple reasons. Firstly, when the error signal consists of two components, a quantization error, and a non-linearity error, the two cannot be distinguished. Secondly,

a quantization error signal will significantly expand the bandwidth of the error signal.

Based on this, the conclusion is that the BBDAC must have at least the same resolution as the RFDAC. The system's overall complexity will be more manageable when the BBDAC can be considered an ideal reference. The benefit of designing a DAC with a low resolution is also not very large since the matching of the current sources must still be comparable to a high-resolution DAC.

4.4 Required resolution ADC

The dynamic range of the error signal is estimated to be around 35dB. Therefore, the ADC must have 35dB SFDR. However, there are some motivations to increase the dynamic range of the ADC. Firstly, when the phase and amplitude of the RFDAC and BBDAC are not yet matched, the error signal will increase in amplitude. Secondly, PVT variation will cause gain variation in the baseband amplifiers. An increased ADC dynamic range will allow a margin of error and the possibility to correct for gain errors.

Over-designing the ADC is also not very expensive, when the initial target SFDR was relatively low. For example, Zhu [17] reaches an SFDR of 48dB and a bandwidth of 2GHz, while using $0.08mm^2$ of area and 21mW of power.

4.5 Conclusion

A circuit-level implementation of the error-measurement architecture has been presented. The error is found by subtracting the output current of the mixing core from the output of a BBDAC. The subtraction is performed in the current domain before the TIA. This approach reduces the voltage swing at the input of the TIA, benefiting the linearity of the mixer and the BBDAC.

Simulations show that the mixer designed in this thesis is suited to this application. The error-measurement architecture lowers the requirement on the ADC by 30dB, resulting in decreased power dissipation, increased integration potential. The architecture leaves room for an increase in bandwidth and the dynamic range of future wireless standards.

5 Conclusion

This work presents a highly linear downconverter to be used for the linearization of high power RFDAC's. A novel subtraction architecture is presented that measures the non-linearity of the power RFDAC by comparing it to a highly linear reference. This architecture reduces the SFDR of the ADC by 30dB. It demands accurate time alignment of the RFDAC and the reference baseband DAC (BBDAC). Note that the time alignment is significantly relaxed by doing this signal subtraction after the downconversion.

As part of the work, a highly linear harmonic rejection mixer was designed. The proposed mixer scales input current with resistors to implement linear harmonic rejection. The mixer's performance is further enhanced by the smart combinations of branches with complementary clocks. As part of the passive mixer, a TIA was designed. The TIA is biased for optimal linearity and has an input bandwidth of 1.8GHz. The use of a TIA increased isolation between branches and linearity by reducing the swing on the terminals of the switching devices. The simulated IIP3 of the mixer is 49dBm, to the best the author's knowledge, the best reported for high bandwidth applications. This mixer can be used for a conventional direct-downconversion architecture. However, the required ADC for that architecture will be challenging to integrate with the transmitter.

In the proposed error-measurement architecture, the outputs of the mixer and BBDAC are subtracted in the current domain before the TIA. As such, the TIA is shared between the BBDAC and the passive mixing core. This approach drastically reduces the voltage swing at the input of the TIA, benefiting the linearity of both the mixer and the BBDAC. Simulations show that the designed mixer is suited for use in this subtraction architecture. The proposed architecture brings the integration of a complete high-power transmitter closer to reality. Additionally, the reduced requirements on the ADC enables the use of the architecture for future wireless standards that will use higher bandwidth and will demand higher dynamic range.

5.1 Future work

The presented TX error detection system in this thesis is the first step. The system consists of two parts. A novel error-measurement architecture that needs accurate phase and amplitude matching of two paths. Within this architecture we proposed a new type of HR mixer that offers improved linearity. Multiple parts of this system will need calibration. Since these parts are relatively new, it would be good to test their functionality separately before testing the overall system performance.

5.1.1 Error-measurement architecture

The accurate time alignment of the RFDAC and BBDAC requires further work. Ideally, the phase matching of the output of the mixing core and the BBDAC would be implemented in the digital domain. The idea is to estimate a slightly phase-shifted signal of the BB data, and feed this to BBDAC. Future work will have to determine if this is feasible. If not, an adjustable analog delay has to be implemented. One approach could be to adjust the clock delays that control the BBDAC with the use of current-starved inverters. The risk of this analog approach is undesired cross-modulation of the delay by electrical interference of the close-by high power transmit signal

In addition, the amplitudes have to be matched. A MATLAB simulation showed that this amplitude matching could happen iteratively. To test the idea on the circuit level, one could use a setup such as shown in Fig. 5.1. The goal is to automate the gain adjustment based on the output of the ADC. A similar setup can be used to test the phase alignment, shown in Fig. 5.2. This setup includes a circuit implementation of a programmable delay, used to adjust the phase of the clocks.

After confirming that the amplitude and phase alignment using a non-linear DAC works, the system can be extended with the RFDAC and mixer.

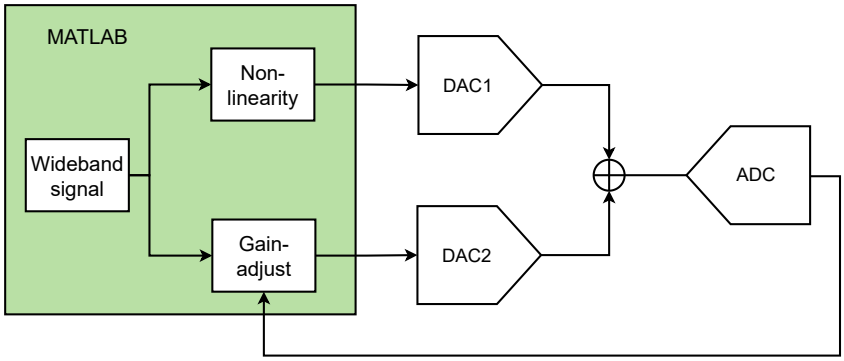

Figure 5.1: Setup used to test amplitude matching

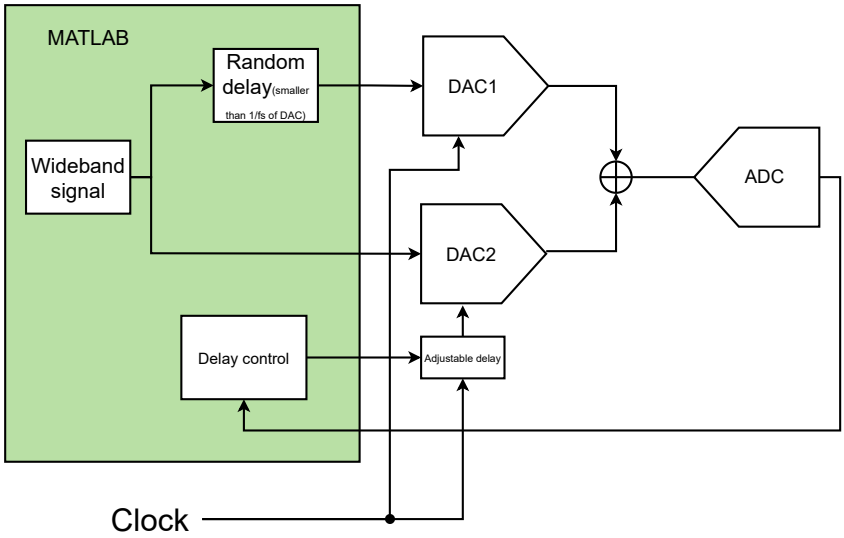

Figure 5.2: Setup used to test phase matching

5.1.2 Mixer

All circuits have been tested on the transistor level. The next step is to develop a lay-out for the mixer. A careful lay-out is needed to get the expected harmonic rejection. The high bandwidth requirement of the TIA resulted in a limited open-loop gain. The limited open-loop gain results in an inaccurate closed-loop gain. Consequently, the mixer needs gain calibration, which could be implemented by tuning the feedback resistor of the TIA. Alternatively, we could over-design the ADC and compensate for a possible gain deviation in the digital domain. The high-bandwidth requirement also motivated the choice of a direct-conversion mixer. However a direct-conversion architecture is prone to DC-offset and spurs due to the IM2. Though the IM2 should also benefit from the focus on linearity in the proposed mixer, these effects can be reduced by designing a symmetric lay-out spending attention to matching and clocking. Clock generation has not been a part of this thesis, but the clocks can have a large influence on the IM2. The clocks must have an equal rise and fall time to avoid duty cycle distortion [22]. Calibration can be used to improve the IM2 and offset if needed [11].

It would also be interesting to try an implementation using thick-oxide switching devices. These can tolerate a higher input voltage so will require less attenuation of the RFDAC's signal. The resistive attenuators(subsection 3.2.3) efficiency is dependent on its attenuation, so a thick-oxide implementation can be more power efficient.

IQ-crosstalk

A potential problem in the proposed mixer is IQ-crosstalk. IQ-crosstalk refers to leakage of for example the Q_{BB} signal to the I_{output}. Equation 5.1 shows the output of the I path. If α is non-zero there exists IQ-crosstalk. This is not the same as IQ-inbalance, IQ-inbalance refers to a gain difference of the I and Q paths, but not in an interaction. Passive mixers can suffer from IQ-crosstalk because the commutating switches are bi-directional, the input signal is downconverted tot the output, but the output signal can also be upconverted back to the input. Additionally, there can be direct leakage through switches that are meant to be "off", or through circuit parasitics.

Section 3.2.2 argued that IQ-crosstalk in the mixer of this thesis is greatly improved over the implementation of Kibaroglu [23] because the baseband signal swing is reduced in the mixing core. Additionally, the constant input impedance and low voltage swing at the drain of each device further improves the isolation. Furthermore, much smaller-sized switches reduce the leaking of baseband currents through switches meant to be open. Leakage currents can be a valid concern, as was shown in Fig. 3.21. One can also add series capacitor in each branch to filter out Baseband leakage currents, such as proposed in passive mixers with overlapping clocks [25]. The assumption here is that the IQ-crosstalk is caused by leakage of the baseband signals. Ideally this assumption would be checked.

Kibaroglu proposes non-overlapping clocks to isolate the different branches. Interestingly, the design of Kibaroglu [23] is not an IQ mixer. It only shows one path. If you only have one output, there can be no isolation problem since the path can only interact with itself. Consequently, it is not clear to me why they are mentioning the isolation problem. It could be that they identified the isolation problem and therefore did not propose an IQ mixer.

In any case, it is essential to confirm that our mixer does not suffer from IQ-crosstalk. The isolation is expected to be improved a lot in our mixer, but the high dynamic range specification still makes IQ-crosstalk a topic of interest. To understand this, observe Eq. 5.2. In this definition of the I_{output}, both the $IM3_{spurs}$ and $\alpha \cdot Q_{BB}$ are unwanted additions that limit the dynamic range. The SFDR can be calculated as in Eq. 5.3.

The difficulty with determining the amount of IQ-crosstalk is that any Q_{BB} signal leaking to the I_{output} could also be caused by the mixing waveforms not being precisely synchronized with the input signal. To still get good simulation results. An ideal IQ signal was defined and fed to the mixer. Then, manually the phase of the input signal was tuned until the amount Q_{BB} signal was minimized in the I_{output}. This procedure was repeated for different input signals and different mixer parameters. Remember that the phase has to be re-optimized when impedance levels in the mixer are changed, so automated sweeps cannot be used without further corrective actions. Using this manual approach, the following conclusions were obtained:

- The proposed mixers dynamic range is not limited by IQ-crosstalk.
- IQ-crosstalk can be improved by reducing baseband signal swing in the mixing core
- IQ-crosstalk can be improved by increasing the switches devices' width.

Ideally, we find a better way of simulating IQ-crosstalk and use this simulation to check the conclusions presented above.

Note that the error-measurement architecture reduces the baseband signal swing in the mixing core with at least 30dB. Consequently, the error-measurement architecture will improve the IQ-crosstalk.

$$I_{output} = I_{BB} + \alpha \cdot Q_{BB} \tag{5.1}$$

$$I_{output} = I_{BB} + IM3_{spurs} + \alpha \cdot Q_{BB} \tag{5.2}$$

$$SFDR = 20log(\frac{I_{BB}}{IM3_{spurs} + \alpha \cdot Q_{BB}}) \tag{5.3}$$

Appendices

.1 A low-noise mixer using capacitors

Noise has not been the focus of the thesis. The aimed application is to estimate the transfer function of the RFDAC. This transfer function does not change quickly over time. Allowing for the averaging of the output signal to filter out noise. For low-noise applications the use of resistors to scale currents and relatively low conversion gain can be a concern. The resistors used to scale the input currents will add noise. The design of Kibaroglu [23] has a Noise figure of 10dB, mostly caused by its gain of -10dB. The noise-folding of higher harmonics is negligible due to the harmonic rejection. As the design of this thesis is similar, the mixer of this thesis is expected to have similar noise figure. The addition of the TIA will add noise, but given the high g_m, the noise contribution of the TIA is not expected to be dominant.

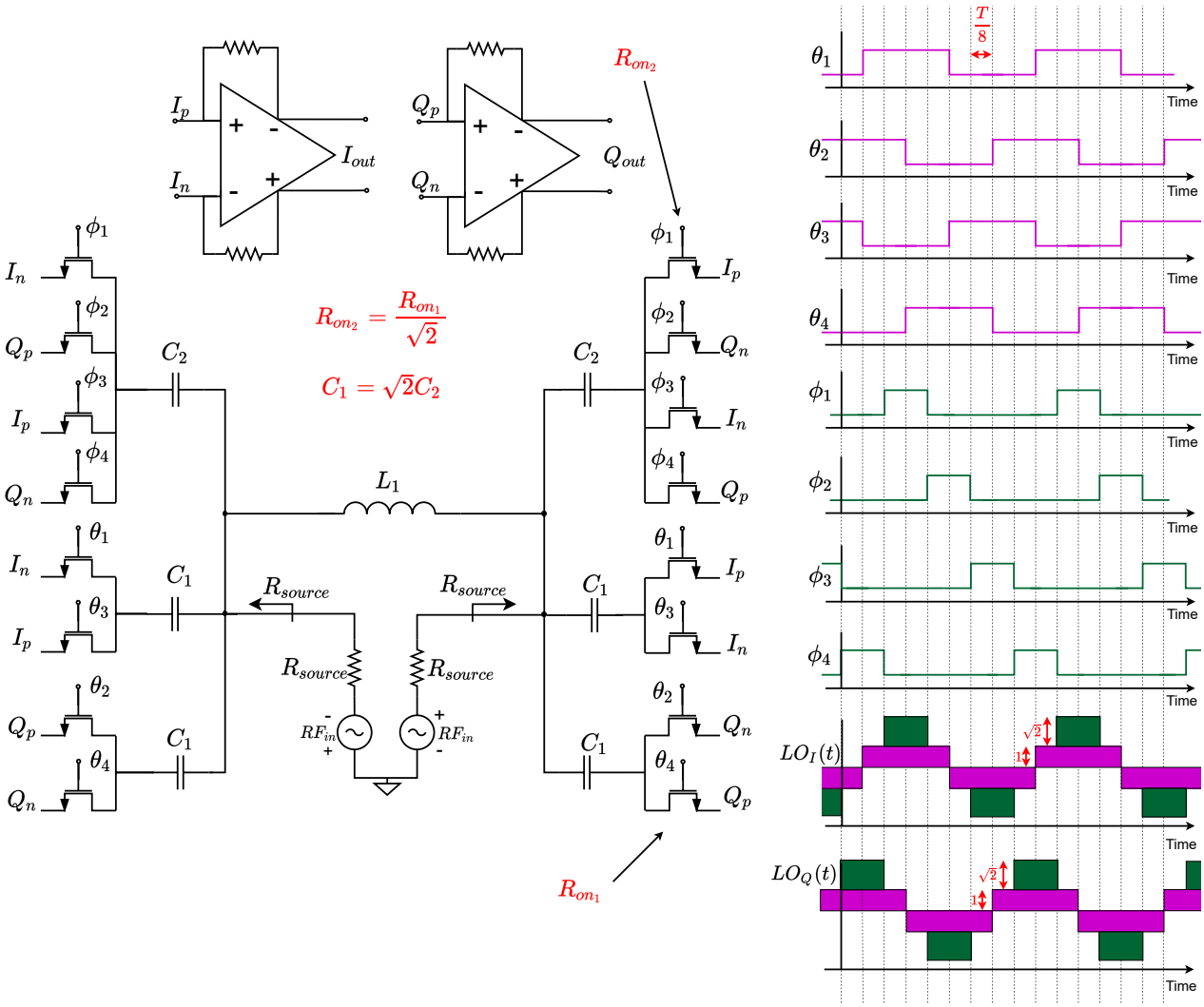

Figure 3: Mixer using capacitors to scale input currents.

Instead of using resistors to scale the input currents, one can also use capacitors. Such a configuration is shown in Fig. 3. Capacitors do not add noise, consequently, this approach has an improved noise performance. The capacitors have two functions. The first is to scale the input currents. For this purpose the impedance of the capacitor must dominate the on-impedance of a switch. The second function is to form a matching network together with the inductor at the input. The mixer can be modeled as a matching network such as shown in Fig. 4. This model assumes an ideal TIA presenting a virtual ground at the source of each

switch. The matching network uses the on-resistance of the switch and converts it to a higher impedance to match the source impedance. The combinations of branches as proposed in subsection 3.2.1 is even more important here. Because a low impedance at the drain of each transistor reduces the needed charging and discharging of the scaling capacitors during switching.

The mixer using scaling capacitors can also reach harmonic rejection, simulation results are shown in Fig. 5. For this result, ideal switches were used, but the concept has also been confirmed to work with real switches. Notice that this result is plotted from minus 250MHz to plus 250MHz, within this bandwidth a relatively flat transfer is realized. However, compared to the resistive scaling, the bandwidth is reduced. This can be explained by noting that any matching network has a limited bandwidth. Additionally, the capacitors impedance is frequency dependant, but the TIA's feedback resistor is not. Consequently, the mixer's gain is frequency dependent. The limited bandwidth becomes more apparent when looking at the groupdelay, shown in Fig. 6. The groupdelay is calculated by taking the derivative of the phase transfer. For the resisitive mixer the groupdelay was flat over frequency, but the capacitive mixer shows a frequency dependent groupdelay.

Nevertheless, the capacitive mixer could be of interest to more narrow-band applications. In a narrow-band application, the TIA's gain can be increased, allowing an increased mixer gain.

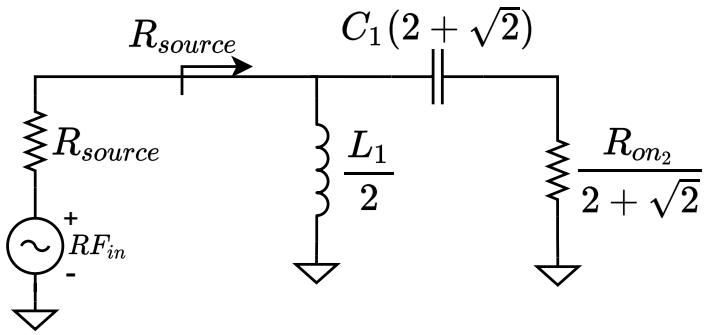

Figure 4: Model of mixer using capacitors to scale input currents

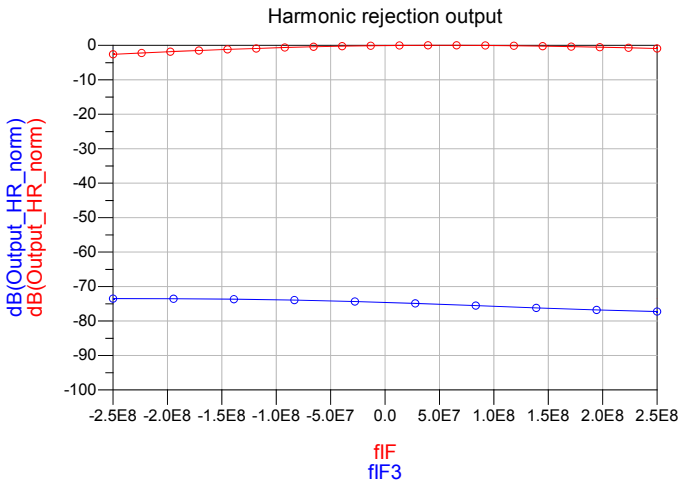

Figure 5: Harmonic rejection capacitive mixer

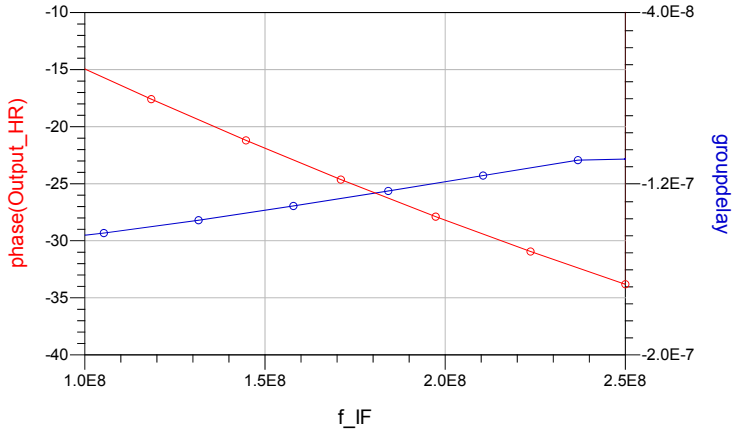

Figure 6: Phase response and groupdelay of capacitive mixer

.2 Alternative clocking schemes

The harmonic rejection waveform in the proposed mixer uses 25% and 50% duty cycle clocks. The mixer can also be implemented using 12.5% duty cycle clocks. However, there are no advantages to this approach. Interestingly, the harmonic rejection waveform can also be implemented with only 50% duty cycle clocks. Though there are some complications, there will be current flowing in the mixer that does not serve a direct purpose. Figure 7 and Fig. 8 show two different phases of an implementation using only 50% duty cycle clocks. In these figures, the flow of current used by the In-phase part is explicitly shown with coloured arrows. Other currents are flowing for the Quadrature part, but those are not explicitly shown. Figure 7 shows a snapshot of the mixer at a specific moment in time. At that moment in time, the effective mixing waveform of the In-phase part is at its maximum amplitude. There are currents injected through a R_1 and an R_2 branch. These currents are both injected into the TIA. The current will flow through the load and return to the other terminal of the differential input. In this phase, the mixer operates the same way as the proposed mixer with 25% and 50% duty cycle clocks. However, in Fig. 8 something different happens. In this case the current I_2 does not flow to the TIA, but directly returns to the other terminal of the differential input. One such path is shown with the dotted line. As a result only the current I_1 is flowing into the TIA.

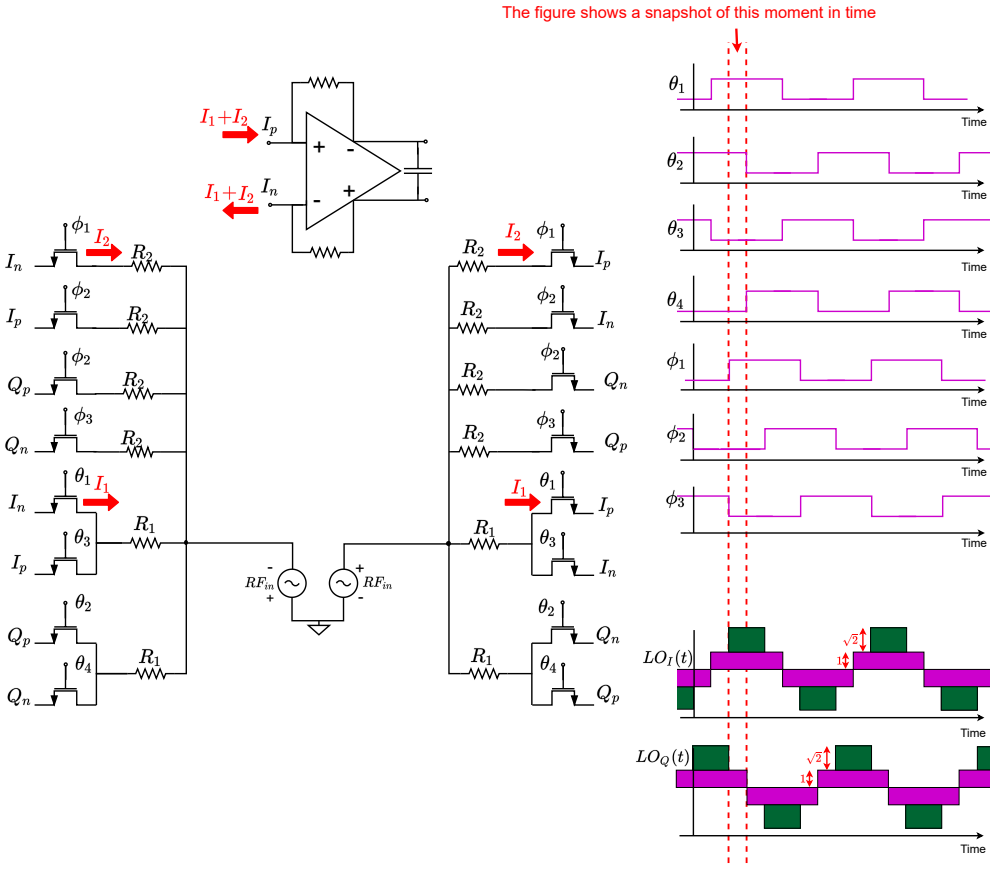

Figure 7: phase 1 of 50% clocking scheme

Notice that in the phase right before the one of Fig. 7, the same current was injected in the TIA as in the phase of Fig. 8. But only in Fig. 8 was there the need for the direct return path. As a result, the input impedance of the mixer is not constant in time. There are multiple ways to implement the harmonic rejection waveform with 50% duty cycle clocks, but I have not been able to find one that implements a constant input impedance. Another disadvantage is that this clocking scheme causes a lowered input impedance. A high input impedance is desired to limit the power dissipation, explained in subsection 3.2.3.

Additionally, the branches with theΦ_2 clock cannot be combined with another branch to share resistor

R_2. Consequently, this configuration will have a lowered linearity and harmonic rejection, as was demonstrated in Fig. 3.19. Furthermore, the 50% duty cycle clocks still need a high timing accuracy.

The conclusion is that 25% and 50% duty-cycle clocks are the most suited for this project. The 25% duty cycle clocks are already available because the RFDAC uses multi-phase operation, which also needs 25% duty-cycle clocks.

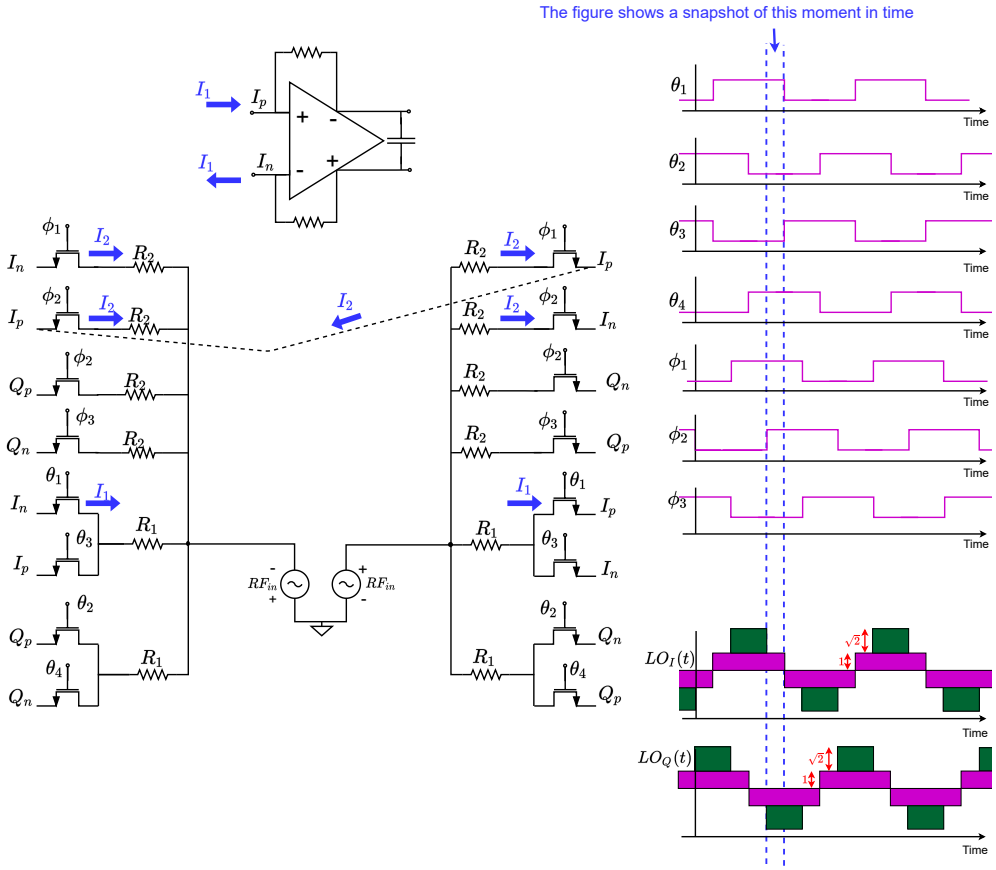

Figure 8: phase 3: $2*\frac{T}{8}$ after the situation of Fig. 7

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