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An Amplitude-Programmable Energy-Recycling High-Voltage Resonant Pulser for Battery-Powered Ultrasound Devices

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***Abstract*— This article presents an application-specific integrated circuit (ASIC) for battery-powered ultrasound (US) devices. The ASIC implements a novel energy-efficient high-voltage (HV) pulser that generates HV transmit (TX) pulses directly from a low-voltage (LV) battery supply. By means of a single off-chip inductor, energy is supplied to a US transducer in a resonant fashion, directly generating half-period sinusoidal HV pulses on the transducer, while consuming substantially less energy than a conventional class-D pulser. By recycling residual reactive energy from the transducer back to the input, the energy consumption is further reduced by more than 50%. The autocalibration techniques are leveraged to deal with tolerances of the inductor, transducer, and battery supply and thus maximize the energy efficiency. A prototype chip was fabricated in TSMC 0.18-μm HV BCD technology and used to drive external 120-pF capacitive micromachined US transducers (CMUTs) with a center frequency of approximately 2.5 MHz. Electrical measurements show that the prototype can generate pulses with a peak amplitude between 10 and 30 V accurate to within ±1 V. Acoustic measurements demonstrate successful ultrasonic pulse transmission and pulse-echo measurements. The prototype reaches a peak efficiency of 0.23 fCV2, which is the highest reported to date for HV pulsers targeting US imaging.**

***Index Terms*— Battery-powered operation, energy recycling, high-voltage (HV) pulser, resonant pulser, ultrasound (US) application-specific integrated circuit (ASIC), US imaging, wearable US.**

I. Introduction

ULTRASOUND (US) imaging is a popular medical imaging modality in medical diagnosis and treatment guidance due to its safety, cost-effectiveness, and compatibility with minimally invasive interventions [1]. An emerging class of US imaging devices are battery-powered US monitoring devices, such as US patches [2], [3]. These devices have the potential to enable impactful medical monitoring. Fig. 1(a) shows possible applications, which include blood-pressure, cardiac, bladder, and respiratory monitoring. Research in this area to date has focused mainly on the realization of flexible patch-based US transducers, while the significant challenges associated with the required battery-powered miniaturized electronics have been largely unaddressed [4]. Fig. 1(b) shows an artist's impression of an envisioned US patch, which includes an application-specific integrated circuit (ASIC) with a US transducer array powered from a low-voltage (LV) battery. The ASIC interfaces with a microcontroller (MCU) and a wireless link, for processing, storage, and transmission of measurement data. The ASIC drives the transducer elements for US pulse transmit (TX) and processes the received echo signals (RX) [5]. The TX part is particularly challenging, because US transducers typically need to be driven with high-voltage (HV) pulses (tens of volts) to generate enough signal-to-noise ratio in the presence of propagation attenuation in tissue [5]. The efficient generation of such pulses in a battery-powered context is the focus of this work.

Most prior US transceiver ASICs employ class-D pulsers driven by an external HV supply to generate the required HV pulses, e.g., [5], [6]. Various techniques have been reported to reduce the fCV^2 losses associated with the charging and discharging of the transducer capacitance, such as multi-level pulsing [7], [8] and inductive energy replenishing [9]. These techniques will be reviewed in more detail in Section II-B.

Irrespective of the efficiency of the pulsing, these approaches require the generation of a dedicated HV supply. Fig. 1(c) summarizes the downsides of this conventional approach. To generate an HV supply, dc–dc conversion is required, introducing conversion losses [6]. To stabilize this HV supply, a large HV off-chip decoupling capacitor is required, which needs to be orders of magnitude larger than the total transducer array capacitance if class-D pulsers are used. Due to the long measurement intervals of the targeted monitoring patches (in the order of minutes), most of the charge on these decoupling capacitors will leak away between measurements, requiring the dc–dc converter to resupply that charge before each acquisition, thus significantly increasing the energy consumption per measurement.

Therefore, an HV TX circuit that omits the need for large off-chip capacitors is desirable. Some HV waveform generators have been reported that employ either charge-pump techniques [10], [11] or buck–boost-conversion techniques [12], [13] to directly generate HV pulses from an LV supply. However, these solutions, which will be

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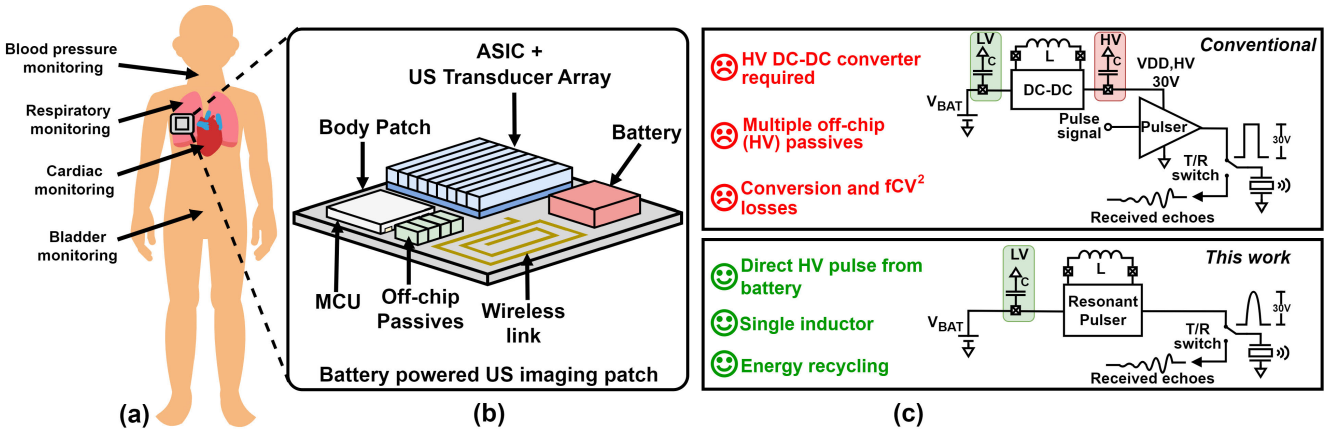

Fig. 1. (a) Possible wearable US monitoring patch application scenarios. (b) Artist's impression of the envisioned battery-powered US patch. (c) Overview of a traditional approach for an HV pulser targeting battery-powered US devices and the proposed resonant pulser.

reviewed in more detail in Section II-C, require many off-chip components or run at clock frequencies that are an order of magnitude higher than the frequency of the pulses being generated, making them impractical for megahertz-range medical US wearables.

This article presents a resonant HV pulser that addresses the aforementioned shortcomings. This work extends on our previous work presented in [14]. Here, we provide a detailed description of the architectural choices and circuit implementation of the HV pulser. Furthermore, we present extended electrical and acoustic measurements, which also show higher energy efficiency. The latter is mainly achieved by employing higher performing inductors and optimizing the field-programmable gate array (FPGA) logic to better optimize the accuracy of the different calibration steps. Fig. 1(c) summarizes the key advantages of the resonant pulser. A prototype ASIC is described that drives two 2.5-MHz capacitive micromachined US transducer (CMUT) transducers, each with an electrical capacitance of 120 pF, using a single low-cost off-chip inductor. It operates from a 3.6-V battery supply and generates sinusoidal pulses with a peak amplitude up to 30 V. The amplitude is programmable, allowing it to be adapted to the desired imaging depth of the US patch to optimize the transmitter for its different application scenarios. The autocalibration techniques are presented that control the pulse amplitude to within ±1 V in the presence of tolerances of ±20% on the inductance and transducer capacitance and ±10% on the supply voltage, representing the variation of a battery voltage as a function of its depth of charge [15].

This article is organized as follows. A review of the prior art on techniques for reducing fCV^2 losses and generating HV pulses without an HV supply is discussed in Section II. The operating principle of the resonant pulser, including the design tradeoffs and the required circuitry around the pulser to make the design functional, is discussed in Section III. Section IV provides implementation details on the circuit design. The fabricated prototype, measurement setup, and electrical and acoustic measurements are discussed in Section V. This article concludes with a comparison to the prior art and a conclusion in Section VI.

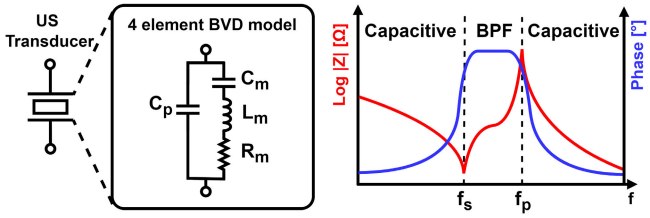

Fig. 2. Four-element BVD model and its impedance characteristics.

II. Review of the Prior Art

A. Transducer Characteristics

Fig. 2 presents the four-element Butterworth–Van Dyke (BVD) model for the US transducer and its impedance characteristics. Its center frequency f_s is defined by the resonance in its mechanical branch due to C_m and L_m. The energy dissipated in R_m models the acoustic dissipation. The impedance of these transducers is often dominated by their (parasitic) capacitance C_p [20]; hence, we treat it as a capacitive load. The approximation made by the BVD model equally applies to CMUT, piezoelectric micromachined US transducers (PMUTs), and bulk piezo transducers.

B. Techniques for Reducing fCV^2 Losses

Different techniques have been introduced in prior art to reduce the losses associated with the charging and discharging of C_p. Multi-level pulsing reduces the dynamic power consumption in a class-D pulser by driving the transducer not using a unipolar rectangular pulse but by charging the transducer in multiple steps. For an N-level pulser, the power consumption ideally reduces with a factor of $N - 1$ [16]. However, this requires multiple HV levels to be available to the transmitter or be generated on-chip, which incurs additional losses [6]. In [8], the intermediate voltage levels are implicitly generated by employing multiple large off-chip reservoir capacitors. However, this requires continuous pulsing or a very high pulse repetition frequency (PRF) to function. Alternatively, capacitive charge redistribution has been leveraged to reduce C_p losses for transducers that do not require to be driven in a single-ended fashion, such as PMUTs [17].

Finally, one could also reduce energy losses in an HV pulser by leveraging a series inductor to avoid C_p losses.

The work presented in [9] shows a US HV pulser design targeted at capsule endoscopy that charges and discharges the transducer's C_p through a series inductor. This minimizes the energy dissipation in the switches and the energy stored on C_p can be recycled back to the supply via the inductor. The design utilizes conduction through the body diodes of the HV transistors during the energy recycling phase while being fabricated in a BCD technology, which could lead to latch-up-related problems in the circuit [18].

However, all of these approaches still require a dedicated HV supply. If only an LV supply is available to the ASIC, one would need to generate and regulate this supply. Fig. 1(c) summarizes the downsides of using this traditional approach for a US transmitter targeting wearable devices. To generate an HV supply, dc–dc conversion is required, introducing conversion losses [6]. To stabilize the HV supply, large HV off-chip decoupling capacitors are required. These should provide the transient current drawn by the pulsers and, hence, should be much larger than the total transducer array capacitance driven by the pulsers. Due to the long measurement intervals in the operation of the targeted monitoring patches, all charge on these decoupling capacitors will likely leak away, requiring the ASIC to resupply that charge during each acquisition, inevitably dominating power consumption. Therefore, besides achieving high efficiency during pulsing, an efficient method to drive the US transducer from an LV supply is crucial.

C. HV Pulsing Without an HV Supply

In prior art, various techniques have already been proposed. One is charge-pump-based waveform generation [10], where voltage-multiplier-like circuitry is used to generate an HV square wave pulse on a capacitive load. In [11], multi-level pulsing is also adopted to increase the efficiency of the design. In these designs, however, multiple large off-chip HV capacitors and a long start-up settling time are required.

Buck–boost-converter-based waveform generation has also been leveraged to obtain continuous pulsing of US transducers. Methods implementing inductive boost converters [12], possibly with reverse-buck functionality [13], present an energy-efficient method to excite US PZT transducers. While these converters generate an HV excitation waveform on a transducer directly from an LV input, they require an off-chip inductor, filter capacitor, and sense resistor. Moreover, these converters run at a switching frequency order of magnitude higher than the frequency of the generated waveform. Consequently, since medical US imaging requires pulses in the megahertz range, this method becomes unfeasible to implement.

Another variation of the previously described buck–boost converter-based driver is using a fly-back converter-based driver [19]. However, these also suffer from requiring bulky off-chip components, such as a fly-back transformer.

III. Operating Principle

A. Basic Architecture

Fig. 3 shows a simplified model of the proposed resonant pulser, assuming, for now, an ideal capacitive load C_p. The

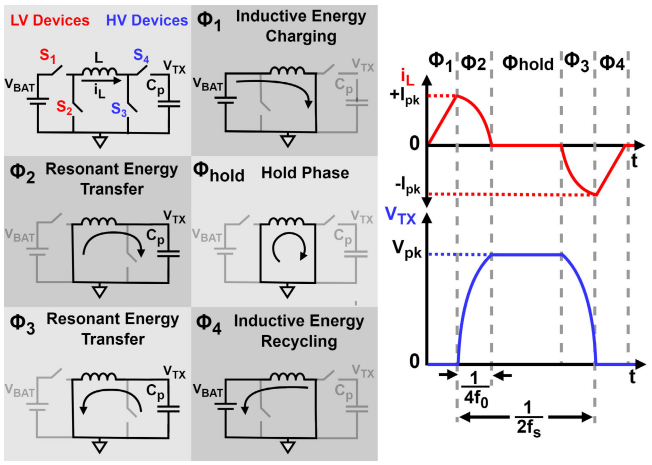

Fig. 3. Simplified operation principle of the resonant pulser.

generic operation of the pulser consists of five phases. In the first phase, Φ_1, the inductor is connected to the battery supply charging the inductor to a peak current $+I_{\text{pk}}$. In the second phase, Φ_2, the inductor is connected in parallel to the load capacitor, leading to resonant energy transfer at a frequency f_0 given by

$$f_0 = \frac{1}{2\pi\sqrt{L \cdot C_p}}. \tag{1}$$

The resulting sinusoidal oscillation forms both the rising and falling edges of the HV pulse in Φ_2 and Φ_3, respectively, where ideally

$$T_{\phi 2} = T_{\phi 3} = \frac{1}{4 f_0} = \frac{\pi}{2}\sqrt{L{\cdot}C_p}. \tag{2}$$

If all inductive energy is completely transferred to the load capacitor, this leads to a peak TX voltage V_{pk} of

$$V_{\text{pk}} = \frac{T_{\phi 1}}{\sqrt{L{\cdot}C_p}} \cdot V_{\text{bat}} = 2\pi T_{\phi 1} f_0 V_{\text{bat}}. \tag{3}$$

To generate a pulse whose frequency matches the transducer's center frequency, f_s, a hold phase Φ_{hold} can be inserted between phases Φ_2 and Φ_3. During this hold phase, the transducer is left floating to obtain the proper pulsewidth. After the residual energy on C_p is returned to the inductor in resonance in Φ_3, the residual inductor energy is recycled during Φ_4.

This shows some important properties of the resonant pulser. First, the TX amplitude can be controlled by controlling the timing of the circuit. Second, the TX amplitude can exceed the low input voltage of the circuit and create a much higher TX pulse without requiring a dedicated HV supply. Typically, the transducer is driven with pulses near or at its resonance frequency. The time period of Φ_{hold} is limited in the extreme case, where $T_{\Phi\text{hold}} = 0$. In this case, the resonant energy transfer frequency f_0 equals the transducer resonance frequency f_s, which leads to a limit on L given C_p.

B. Efficiency Analysis

Given a switch ON-resistance R_{on}, a battery voltage V_{bat}, and a target pulse amplitude V_{pk}, the achievable efficiency of

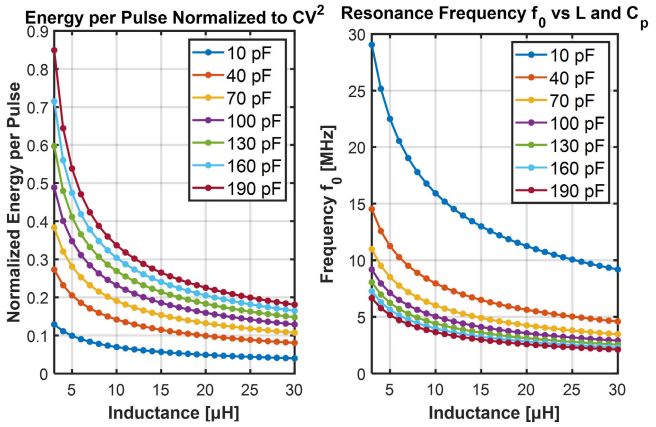

Fig. 4. Calculated losses and f_0 in the simplified resonant pulser model, $V_{\text{bat}} = 3.6$ V, $V_{\text{pk}} = 30$ V, and $R_{\text{on}} = 5\ \Omega$.

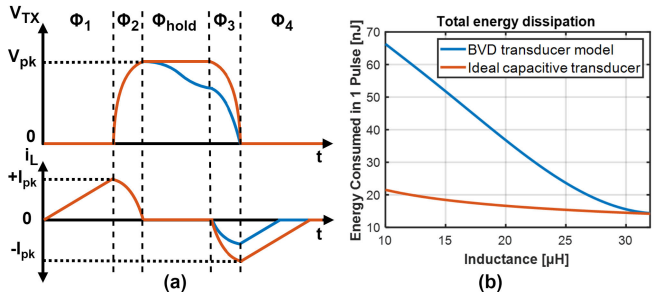

Fig. 5. (a) More realistic transient voltage and current when a US transducer is driven rather than an ideal capacitive load. (b) Calculated energy dissipation increase.

the resonant pulser is determined. Fig. 4 shows the energy dissipation per pulse due to ohmic losses in the switches, normalized to that of a class-D pulser, for the example case of generating 30-V pulses from a 3.6-V battery, using 5-Ω R_{on} and a range of inductances L and capacitances C_p. Also shown is the resonance frequency f_0 corresponding to these values.

These results show a few important characteristics. The efficiency of the pulser increases with both lower f_0 and lower C_p. This is because a lower peak inductor current is required to achieve the required TX amplitude. The lower peak current, in turn, reduces the dissipation losses due to the finite R_{on} of the switches. As a result, the resonant pulser is best suited toward low frequency (few megahertz) pulsing ideally with an electric capacitance that is not very large.

Different loss mechanisms play a role in the total achievable power efficiency of the pulser. Besides ohmic dissipation losses in the four switches of the pulser and gate drive losses of these same switches, non-idealities in the inductor can dominate the power efficiency. A real inductor has a non-zero dc resistance, R_{dc}, which adds resistance to the current path during the entire operation of the pulser. Additionally, a self-resonance frequency, f_{SRF}, is required that is at least higher than f_s. The capacitance associated with f_{SRF} is placed in parallel to C_p during resonant energy transfer, leading to an increased capacitive load and hence higher losses. This is twofold since besides the larger load that has to be driven, the maximum allowable inductance decreases. Finally, non-ohmic losses associated with the inductor (non-linear) quality factor, Q, increase the impedance of the inductor, further increasing the power consumption as a result.

C. Operation With and Without Hold Phase

The resulting architectural choices are split into two cases, which are as follows: first is a resonant pulser having a hold phase (i.e., $f_0 > f_s$) and the second is the extreme case, where the hold phase is reduced to zero (i.e., $f_0 = f_s$). In the latter case, the resulting HV pulse is a half-period sinusoidal pulse rather than a square wave-like pulse. Fig. 5(a) shows how the US transducer influences the operation of the resonant pulser in case a hold phase is present. During the time the transducer is left floating, the energy left on C_p will cause a parallel oscillation resulting in imperfect recycling of the residual energy in Φ_4. This behavior can be modeled analytically for the target CMUT transducer and is shown in Fig. 5(b), noting that losses in R_m are excluded from this calculation. Here, it was found that maximizing L provides optimal power efficiency. Another reason to design the resonant pulser with a maximized inductance is the resulting simplicity of the circuitry. If the resulting f_0 is matched accurately to f_s, the whole operation of the pulser is synchronously timed based on a 50-MHz system clock, which will be further elaborated in Section IV.

The half-sinusoidal architecture does pose some limitations to the resulting US ASICs imaging capabilities. Since the inductor is in use during the generation of the pulse, there is no direct possibility of driving multiple transducer elements using the same inductor in order to implement TX beamforming on a transducer array. Even generating pulse trains, which increase the resulting peak pressure, is limited depending on the choice of f_s, C_p, V_{bat}, and V_{pk}, because the required charge and discharge periods of the inductor are too long compared to the pulse interval. This could be remedied by using two or more inductors in a ping-pong-like configuration. However, in this work, we limit the design to a single off-chip inductor. The target application does not necessarily require the ability to beamform or generate pulse trains. Imaging schemes, such as synthetic aperture [21], in which array elements are pulsed one at a time, would be suitable for monitoring patches. Hence, this architecture has been chosen for the prototype. Note that, while the charge and discharge periods are too long for generating pulse trains, they are still much shorter than the receive period for practical imaging depths and hence do not limit the PRF that can be achieved.

D. Calibration

The half-sinusoidal pulser requires f_0 to accurately match f_s. Since both L and C_p can vary by ±20%, an initial calibration on each of the transducer elements is required. Fig. 6 presents a simplified architecture overview of the resonant pulser with the three required calibration steps. For the half-sinusoidal pulser, phase Φ_{2+3} represents the resonant energy transfer phase, which combines the previously depicted Φ_2 and Φ_3 for the pulser implementing the hold phase.

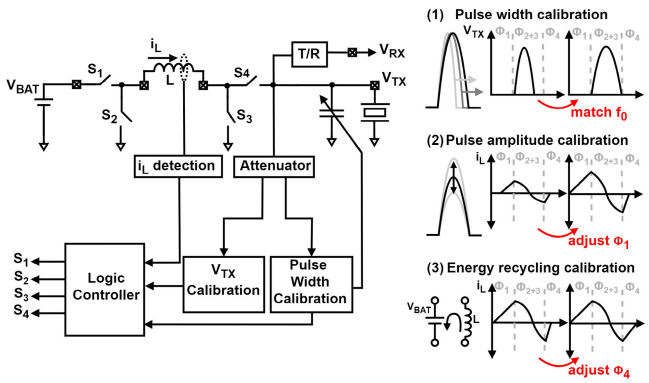

Fig. 6. Simplified architecture overview of the resonant pulser showing the three autocalibration steps.

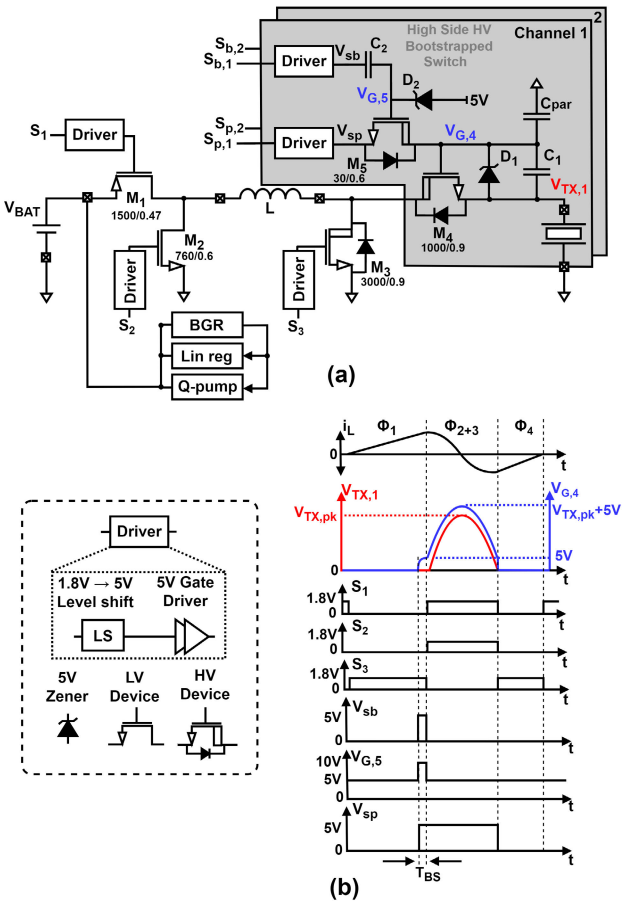

Fig. 7. (a) Circuit implementation of the core of the resonant pulser, including the high-side HV bootstrapped switch; device sizes are in μm. (b) Timing diagram of the pulser.

Note that the resulting pulsewidth remains the same and equals $1/2\,f_s$.

After calibration of the pulsewidth to 200 ns (half of the resonance period of the targeted 2.5-MHz transducer), the programmable pulse amplitude V_{pk} is calibrated by adjusting $T_{\Phi 1}$. This is necessary since V_{TX} is a function of L, C_p, V_{bat}, and parasitics present in the pulser. Finally, the energy recycling timing is calibrated to maximize the pulser's efficiency. All three calibration steps are performed automatically at start-up and are orthogonal to each other if performed in this order. After fixing the total capacitive load by performing the pulsewidth calibration, the resulting V_{pk} is only influenced by adjusting $T_{\Phi 1}$, and the same holds for adjusting $T_{\Phi 4}$.

Besides the core of the resonant pulser, which consists of the four switches, additional circuitry is required to implement the different calibrations. For the LV electronics to interface with the HV TX pulse, an attenuator is added to the output of each TX channel. The attenuated pulse is used to measure the pulsewidth and adjust f_0 by adjusting the total load capacitance to match f_0 to f_s. That same attenuated pulse is used to measure the peak TX amplitude and adjust the timing provided by a logic controller. Finally, a circuit is used to measure the residual energy on the inductor and adjusts the timing of the pulser accordingly.

IV. Circuit Design

A. High-Side Switch Implementation

Fig. 7(a) shows the core of the resonant pulser. The four main switches in the core of the resonant pulser are implemented using two LV transistors (M_{1-2}) and two HV transistors (M_{3-4}). The prototype contains two copies of M_4 to allow two transducers to be driven by the same inductor. This can readily be extended to more copies, at the expense of increased parasitic capacitance. Switches M_{1-3} are driven directly from the LV electronics using a cross-coupled dynamic level shifter and gate drivers. The gate drivers are sized to trade off their power consumption against the dissipation losses through the switches for the targeted pulse amplitude range and other sources of losses.

One of the challenges in the design of the pulser is controlling the high-side HV transistor M_4. Driving the switch from logic supply levels is not directly possible, given that the gate–source voltage of the HV devices used is limited to 5 V. In prior art, the voltage gap is bridged by a level-shifter using either HV transistors and resistors [22], [23] or capacitors [24]. However, due to the lack of an HV supply in the system, these options are not suitable. Bootstrapped structures circumvent this limitation and have been applied in designs, where external pulses are passed from an imaging system to a transducer [25], [26].

Fig. 7(a) shows the proposed high-side HV bootstrapped switch, and Fig. 7(b) shows the timing diagram and the resulting TX output voltage. The design takes advantage of pulsing without a hold phase to ensure that only the high-side switch M_4 turns on and off when V_{TX} is low. In time interval T_{BS}, before Φ_1 is completed, M_4 is turned on by charging the bootstrap capacitor C_1 to 5 V through transistor M_5 Capacitor C_1 is sized, such that M_4 remains on while V_{TX} rises, in spite of the attenuation due to parasitic capacitance C_{par}. After completion of the pulse, C_1 is discharged through M_5, to turn off M_4. Zener diode D_1 protects the gate of M_4 by preventing the gate–source voltage of M_4 from exceeding 5 V. Transistor M_5 is controlled by a voltage doubler, consisting of a capacitor C_2 and Zener diode D_2. Transistor M_5 is sized, such that a sufficient 5-V overdrive is created during T_{BS}, which lasts one clock cycle ($T_{\text{BS}} = 20$ ns). Even though there is a single clock period where both M_4 and M_3 are turned on,

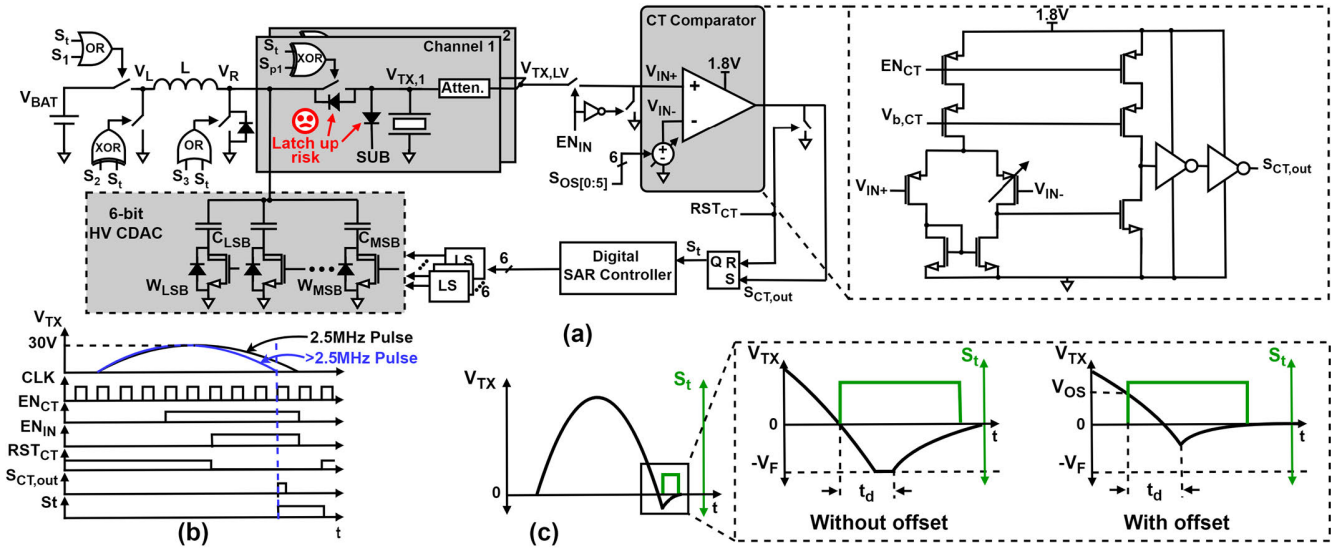

Fig. 8. (a) Circuit implementation of the pulsewidth calibration circuit, with a CT comparator and 6-bit HV CDAC. (b) Timing diagram showing the operation of the circuit. (c) Diagram showing the resulting offset due to delay at the output of the pulser.

the high-voltage node of the inductor is kept firmly grounded through M_3, avoiding charging of the transducer. In order to avoid short-circuiting the battery supply through ground by switching M_1 and M_2 simultaneously, a non-overlap circuit is implemented, which controls S_1 and S_2.

In order to allow the pulser to drive multiple transducer elements in a synthetic aperture fashion, only the high-side switch needs to be duplicated for each transducer element. The HV low-side switch M_3 can be shared, decreasing the required area. Furthermore, all the high-side HV transistors can be sized much smaller compared to M_3 since the resulting dissipation losses through these switches are much smaller compared to M_1 and M_3, which charge and discharge the inductor. All HV transistors used in this design are rated at a 40-V breakdown voltage to guarantee safe operation during pulsing and pulse amplitude calibration.

To bias the pulser core, a bandgap reference (BGR), 5-V charge pump, and a 1.8-V linear regulator are implemented. The 5-V supply is generated by a two-stage regulated charge pump using feed-forward control from the digital controller. The output is regulated by an on-chip 200-pF MOS capacitor. The 1.8-V supply is generated by a capacitorless NMOS linear regulator, which is internally compensated. Its output is also regulated by an on-chip 200-pF MOS capacitor.

B. Pulsewidth Calibration

Due to tolerances in L and C_p, the pulser requires an initial calibration for f_0 for each TX channel. After this initial calibration, the entire operation of the resonant pulser consumes only dynamic power due to its timed nature. The prototype uses a 50-MHz system clock as the time reference. Fig. 8(a) shows the implementation of the pulsewidth calibration circuit. A continuous time (CT) comparator is used to detect the zero crossing of the attenuated TX voltage $V_{\mathrm{TX,LV}}$. Depending on whether the zero crossing occurs before or after the intended time moment, i.e., $1/2\,f_s$, the total load capacitance is adjusted by means of a 6-bit capacitive DAC (CDAC) through a successive approximation process.

Operating the circuit introduces a latch-up risk in case the TX output becomes negative and falls below the forward voltage drop V_F of the HV transistor's parasitic body and substrate diodes. The use of the CT comparator prevents this. Its latched output S_t controls the pulser switches together with the synchronously timed control signals S_{1-3} and S_{p1} through a set of XOR and OR gates to start the recycling phase Φ_4 earlier if V_{TX} drops too far, as shown in Fig. 8(b).

To ensure the CT comparator triggers early enough, an adjustable offset is added. Due to finite propagation delays in the comparator, level shifters, and gate drivers (t_d), V_{TX} could still drop below V_F. Adding an appropriate offset prevents this, as shown in Fig. 8(c). The adjustable offset is realized by skewing the current through the input pair of the comparator's PMOS input stage, as shown in Fig. 8(a). The CT comparator consumes a total current of 100 μA and is turned off after the calibration has been completed.

In order to adjust f_0, the load capacitance can be increased by adding capacitance in parallel to the transducer or decreased by adding capacitance in series. The latter, however, is undesirable, as it would attenuate the pulse. Therefore, a parallel CDAC is used, implying that load capacitance is always adjusted upward toward a target capacitance. The inductance L is reduced to compensate for this. To allow the CDAC to be shared by all TX channels, it is connected to the high-voltage node of the inductor, V_R, rather than the output, where it has the same effect on the resulting pulse.

The CDAC consists of a set of binary-scaled MOM capacitors with HV switches connected to their bottom plates. This makes controlling the CDAC easier since it prevents the CDAC switches from requiring an HV bootstrap circuit. Now, the top plate parasitics of the entire CDAC are connected in parallel to the transducer during pulsing. The resulting increase of the load capacitance does not decrease the efficiency of the pulser much, since all charge on these parasitics will get recycled.

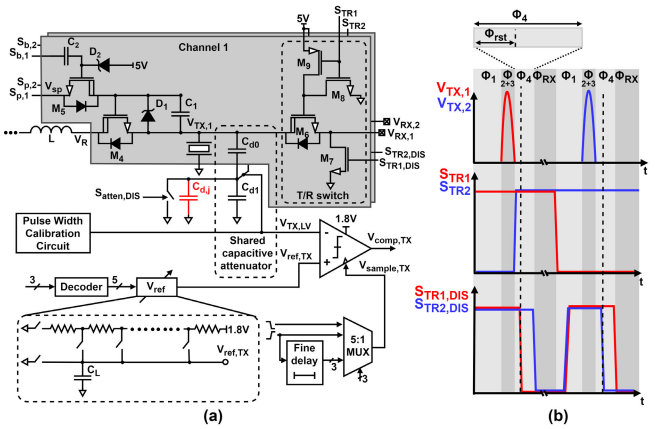

Fig. 9. (a) Circuit implementation of the shared capacitive attenuator, the T/R switches, and the TX amplitude calibration. (b) Shared attenuator operation.

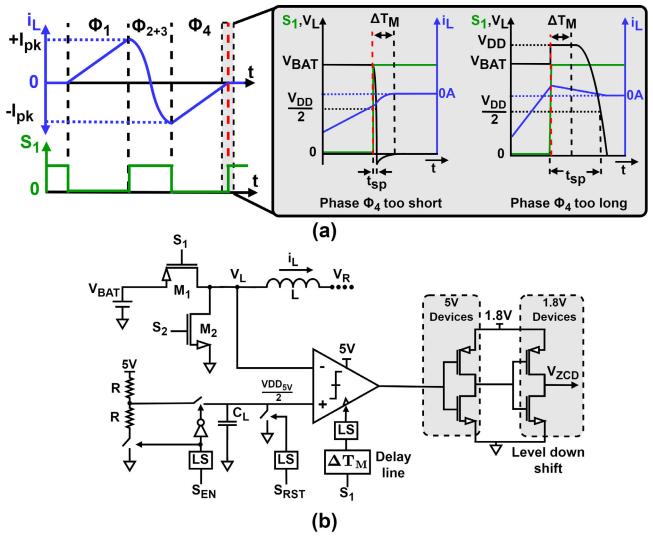

Fig. 10. (a) Operation principle of the energy recycling calibration. (b) Circuit implementation.

The LSB size of the CDAC is based on the resolution of the pulsewidth calibration required in order to avoid forward biasing of the parasitic diodes during normal pulsing. This is determined by the case of the highest TX amplitude since it has the highest slope at 0 V, and thus, the available time before $-V_F$ is reached is shortest. Based on simulations, an LSB of 1.1 pF is used for this design. The range of the CDAC is determined by the total tolerance on L and C_p, which has been determined to be 6-bit.

Due to large bias-voltage dependent junction capacitors originating from the drain of the HV transistors connected to node V_R, f_0 is a slight function of V_{TX}. The resulting f_0 is slightly higher at the maximum V_{pk}, i.e., 30 V. Therefore, the pulse with calibration is always performed at maximum V_{pk}.

C. Pulse Amplitude Calibration

Fig. 9(a) shows the circuit used for the TX amplitude calibration. The amplitude calibration is performed after the pulsewidth has been calibrated. By using a capacitive attenuator, an attenuated version of the pulse $V_{\mathrm{TX,LV}}$ is compared with a reference voltage, which is derived from the 1.8-V regulator using a resistive divider and corresponds to a pulse amplitude of 10, 15, 20, 25, or 30 V. To calibrate the peak value of the pulse, the comparison is taken halfway through the pulse. To correct for propagation delay in the switches, the sample moment is made adjustable. The inductor charging time $T_{\Phi 1}$ is adjusted using a successive-approximation algorithm to obtain the required TX amplitude.

The required number of calibration steps is determined by the sensitivity of the amplitude calibration, i.e., the charge time required to obtain a 1 V increase on V_{TX}. This sensitivity is lowest in the case of the lowest V_{bat} and highest C_p. To obtain the required $\pm$1-V accuracy, eight calibration cycles are used, six coarse and two fine steps. The coarse timing is derived from the 50-MHz clock and the final two fine steps are generated using an on-chip delay element of 5 ns. If the resonant pulser was to be designed targeting a higher frequency transducer, one would require either a higher system clock or a higher order of clock interpolation.

The T/R switches not only serve to connect the transducers to the RX circuitry after pulse transmission but fulfill two additional purposes. First, as shown in Fig. 9(b), they discharge any residual charge on C_p during Φ_4 before RX starts for a period of Φ_{rst}. Second, they allow the capacitive attenuator to share capacitor C_{d1}, by connecting the top capacitor C_{d0} of the inactive channel(s) to ground. Thus, area is saved, while the attenuation factor is set by the ratio of C_{d0} of the active channel, and C_{d1} plus C_{d0} of the inactive channel(s). While this comes at the cost of capacitive coupling between the different channels during TX, this is designed to be negligible.

Different error sources limit the achievable accuracy of the amplitude calibration. Bias-voltage-dependent transistor junction capacitance $C_{d,j}$ connected to the attenuator leads to a nonlinear attenuation ratio for different TX amplitudes. Introducing a static error and mismatch in the attenuator leads to a gain error voltage, and the combined error increases for increasing TX amplitudes. The dynamic comparator employs a dual-tail single-clock-phase architecture [27]. Its input-referred offset and noise also contribute to the total error budget. Finally, the error due to finite accuracy and load regulation of the 1.8-V regulator contributes to the total achievable accuracy of this calibration step.

D. Energy Recycling Calibration

Instead of continuously monitoring the inductor current and ending the recycling phase Φ_4 when it returns to zero, $T_{\Phi 4}$ is calibrated instead, thus also making the recycling phase free of static power dissipation. Residual inductor energy is initially dissipated during the RX period in the first two calibration steps. After pulse amplitude calibration, pulse-echo acquisitions can start and the energy recycling timing is calibrated in the background. The calibration is performed by measuring voltage spiking on the LV node of the inductor V_L due to residual inductor energy when the 5-V PMOS transistor M_1 is turned off. In low-power boost converter designs, similar techniques have been utilized to optimize switching timing [28].

Fig. 10(a) shows the operation principle. Before the inductor is discharged during RX, all switches connected to node V_L

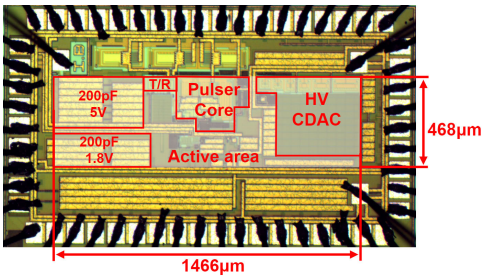

Fig. 11. Chip micrograph.

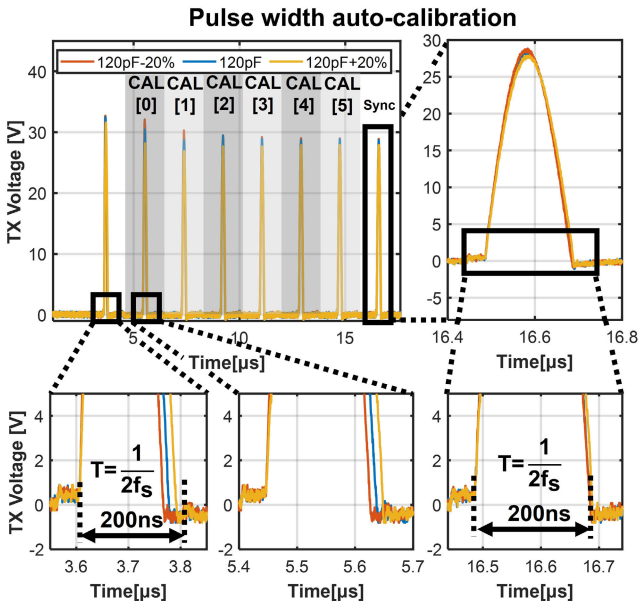

Fig. 12. Measurement of the pulsewidth autocalibration for varying C_p between ±20%.

are briefly open, allowing the residual inductor current to develop a voltage spike across the high OFF-resistance of the switches. Node V_L will either quickly fall to ground when phase Φ_4 was too short or exhibit a positive voltage spike when phase Φ_4 was too long. In case residual energy is left on the inductor, the inductor current discharges through the high OFF-resistance of the switch, generating an overshoot at node V_L. The voltage overshoot lasts until the inductor is completely discharged. This is detected by a clocked comparator in order to adjust $T_{\Phi 4}$. Four pulse-echo cycles are required to find the 4-bit adjustment of $T_{\Phi 4}$ in a successive-approximation fashion. Two steps for coarse adjustment derived from the 50-MHz clock and two for 5-ns fine adjustments generated using a similar delay element as used in the amplitude calibration circuit.

Fig. 10(b) shows the circuit implementation of the calibration circuit. The dynamic comparator employs a dual-tail single-clock-phase architecture, similar to what is used in the amplitude calibration circuit [27], but now implemented in the 5-V domain. It compares V_L to a 2.5-V reference voltage derived from the 5-V internal supply using a resistive divider and sample-and-hold circuit. The comparator is clocked at a delay ΔT_M relative to the opening of M_1, in order to minimize false negative and false positive comparisons. In case ΔT_M is omitted or chosen too short, a false positive output would be detected when $T_{\Phi 4}$ is too short. Vice versa, in case ΔT_M is chosen too long, a false negative output would be detected when $T_{\Phi 4}$ is too long. Therefore, ΔT_M is designed close to the propagation delay t_{SP} in case the residual inductor current is exactly 0 A [29].

Like the pulse amplitude calibration, different error sources limit the final accuracy of the energy recycling calibration. Now, the timing skew from the ΔT_M delay cell and 5-V level shifter also becomes an important limiting factor in the final accuracy of this calibration step. The chosen 5-ns resolution in the adjustment of $T_{\Phi 4}$ leads to a simulated error of <1.5% of the initial inductor current in Φ_4 being left on the inductor. Note that given the inductor and other parasitics, the resulting transients on node V_L due to the current switching show negligible effect on the calibration performance.

V. Experimental Results

A. Electrical Measurements

The prototype ASIC has been fabricated in a 180-nm HV BCD technology. Fig. 11 shows a die micrograph. The ASIC has an active area of approximately 0.69 mm^2. For flexibility and debugging purposes, the control logic is implemented on an FPGA, which also generates the ASIC's 50-MHz clock. For the electrical measurements, external capacitive loads of nominally 120 pF were connected to the ASIC's two TX channels. An inexpensive 27 μH ± 20% inductor with a Q factor of 16 is used. Fig. 12 shows the pulsewidth autocalibration on one of the TX channels, for ±20% variation in the load capacitance. To show the uncalibrated spread in the pulsewidth, an initial pulse is generated with the CT circuit active and the CDAC set to 0. In the subsequent six successive-approximation calibration cycles, the pulsewidth is accurately set to 200 ns. After calibration, a single synchronously timed pulse is generated (i.e., without employing the CT circuit), showing proper operation of the resonant pulser. In this measurement, $T_{\Phi 1}$ is kept constant in order to perform the calibration at approximately 30 V, leading to a small decrease in amplitude during calibration due to the added CDAC capacitance. This is addressed by subsequent amplitude calibration. The results also show that the CT circuit correctly prevents negative output voltages during the calibration steps, which could forward bias the body diode of the high-side HV transistor, as discussed in Section IV-B.

Fig. 13(a) shows the measured peak TX amplitude as a function of the inductor charging time $T_{\Phi 1}$ for different values of the input voltage V_{bat}. As expected, the dependence on $T_{\Phi 1}$ is approximately linear, and variations on V_{bat} lead to significant variation in the amplitude. Fig. 13(b) shows the measured amplitude autocalibration. It demonstrates how the circuit successfully generates five different TX amplitudes ranging from 10 to 30 V within eight successive approximation cycles, for the nominal V_{bat} of 3.6 V. Fig. 14 shows the amplitude calibration for varying V_{bat} and the resulting error voltage. At the nominal V_{bat} of 3.6 V, the ASIC achieves ±350-mV accuracy, while for V_{bat} ranging

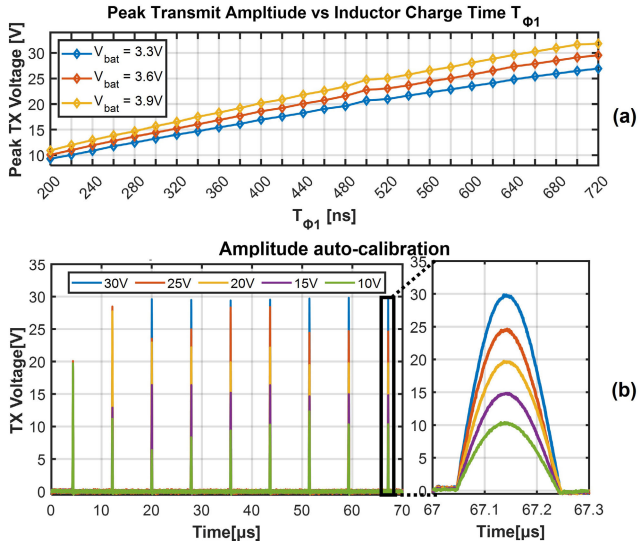

Fig. 13. (a) Measurement of the (uncalibrated) peak TX amplitude for varying $T_{\Phi1}$ and V_{bat}. (b) Measurement of the pulse amplitude calibration.

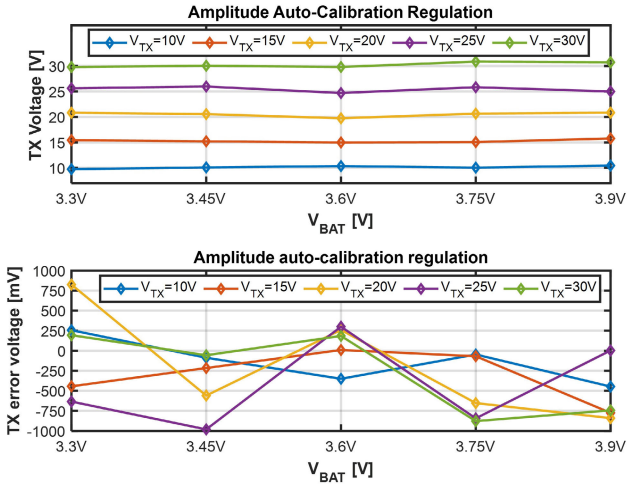

Fig. 14. Measurement of the calibrated TX voltage regulation for varying V_{bat}.

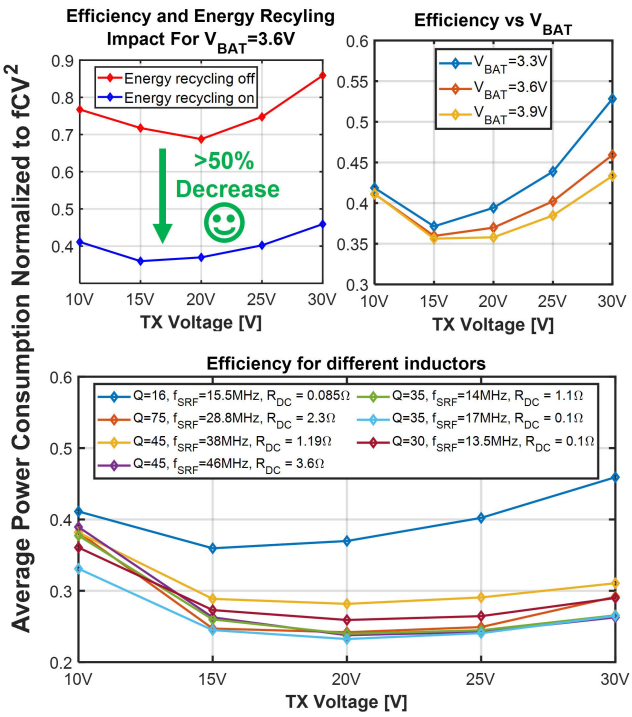

Fig. 15. Measured average power consumption of the resonant pulser ASIC, showing the impact of energy recycling for the low Q inductor, and the efficiency for varying V_{bat}, and for different inductors.

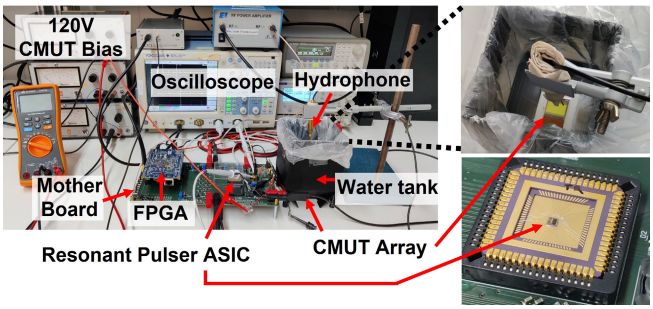

Fig. 16. Measurement setup for electrical and acoustic verification.

from 3.3 to 3.9 V, the error increases to ±1 V, corresponding to a maximum error of 5.2% relative to the targeted pulse amplitude.

Fig. 15 shows the measured efficiency of the ASIC. The total average power consumption is measured for a 120-pF capacitive load after calibration. This was measured directly at the battery input and thus includes the power consumed for generating and regulating the internal 1.8- and 5-V supplies and all circuitry powered from these supplies.

By dissipating all energy after pulsing instead of returning it to the input, the impact of the energy recycling operation is measured. Recycling reduces the average power consumption by more than 50%. Note that this is for a capacitive load. The benefit of recycling will be less for a transducer that dissipates part of the pulse energy.

Fig. 15 also shows the measured efficiency for different inductors, demonstrating that the choice of the inductor heavily impacts the efficiency of the pulser. Choosing a more expensive inductor, with a higher f_{SRF} and Q factor, further reduces the average power consumption considerably.

B. Acoustic Measurements

Fig. 16 shows the measurement setup used for acoustic verification of the prototype. For these measurements, an external 32-element CMUT array was connected through a flex PCB. The two channels of the prototype ASIC were connected to two elements of the array. A hydrophone was used inside of a water tank to measure the pressure waves produced by the CMUT elements. Fig. 17 shows a comparison of the recorded pressure waves produced by the resonant pulser and an external pulser. The results are very similar. The slight differences can be explained by the difference in the frequency content of the two pulses. Rectangular-like pulses have more energy falling inside the passband of the US transducer.

Fig. 18 shows the recorded pressure waves for increasing inductor charge time $T_{\Phi1}$. Both the measured peak TX voltage and peak pressure show, as expected, a linear relation with

TABLE I
COMPARISON WITH THE PRIOR ART

	This work	TBCAS'16[6]	JSSC'13[7]	ISSCC'21[9]	JSSC'21[17]	ISSCC'24[31]	TCSII'21[32]	SSCL'23 [33]	ESSCIRC'21[8]	JSSC'21[34]
Target application	Imaging					Stimulation	General		Haptics	
Transducer	**CMUT**	PMUT	CMUT	PZT	PMUT	PMUT	PMUT	PZT	CMUT	PMUT
Operating Frequency	**2.5MHz**	8MHz	3.3MHz	5kHz	5MHz	7.8MHz	1MHz	40kHz	250kHz	250kHz
TX voltage	**10-30V**	32V	30V	30V	13.2V	4.8V	28.7V	7.2V	32V	24V
Technology	**180nm BCD**	180nm BCD	180nm BCD	180nm BCD	180nm BCD	65nm CMOS	180nm BCD	180nm CMOS	180nm BCD	800nm IGZO
Load Capacitance	**120pF**	17.5pF	40pF	470pF	15.4pF	2.5pF	1nF	2.7nF	235pF	36pF
Theoretical C_p loss reduction	**100%**	N/A	50%	100%	50%	75%	N/A	90%	83.3%	N/A
Measured Cp loss reduction	**Low Q[1]: 64.0%** / **High Q[2]: 76.8%**	N/A	38%	73.1%	42.2	46%	64.9%	87.2%	80%	22%
# off-chip components[3]	**1**	2	2	N/A	N/A	N/A	5	8	5	N/A
External supply voltage(s)	**3.6V**	1.8V	1.8V, 3.3V, 30V	1.8V, 5V, 30V	3.3V (13.2V)	1.2V, 4.8V	1.2V, 5V	3.6V	1.8V, 32V	6V, 12V
HV supply	**Not Needed**	Charge Pump	External	External	3x Voltage Doubler or External	No HV TX	Supply Multiplier	No HV TX	External	External

[1] Inductor characteristics: L=27µH, Q=16 (@2.5MHz), R_{DC} = 85mΩ, f_{SRF} = 15.5MHz
[2] Inductor characteristics: L=27µH, Q=35 (@2.5MHz), R_{DC} = 100mΩ, f_{SRF} = 17MHz
[3] Number of off-chip (HV) components required for the pulser, omitting LV off-chip decoupling

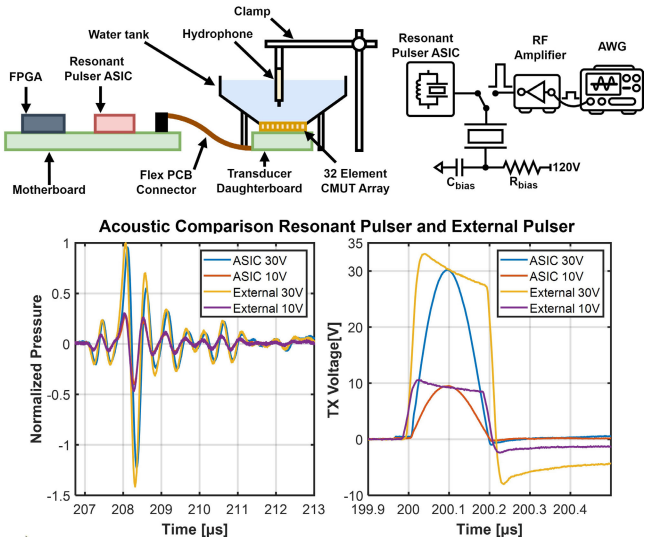

Fig. 17. Overview of the acoustic measurement setup and comparison of the measured pressure generated when the transducer is driven by the resonant pulser and by an externally generated HV pulse.

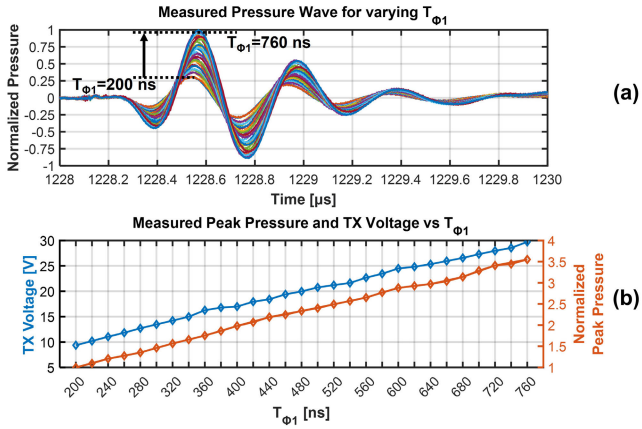

Fig. 18. Measured pressure wave for increasing $T_{\Phi1}$ and corresponding peak CMUT TX voltage and peak pressure.

$T_{\Phi1}$. Fig. 19 shows two pulse-echo experiments that have been performed. In the first experiment, the reflected echo signals from the water surface are measured for different water levels. In the second experiment, a waterbag is placed inside the water tank mimicking a bladder. The reflections of the two layers from the waterbag are visible together with the echo reflection from the water surface. The resulting time of flight closely corresponds to the diameter of the water bag. It demonstrates the ability of the resonant pulser to receive echo signals through its T/R switches. Note that CMUT transducers require an HV bias to properly operate. In this case, an external 120-V bias voltage was applied. For the wearable US application, this HV bias would decrease the system power efficiency for the same reason that generating an HV supply for the pulser does. Hence, PMUT or charge-trapped CMUT transducers [30] that do not require this HV bias are the preferred option.

Table I gives a comparison with the prior art in energy-efficient and battery-powered US TX solutions. The resonant pulser presents a novel TX solution able to achieve the highest reported reduction in C_p losses for pulsers targeting US imaging. Furthermore, it presents the first HV US transmitter able to generate HV pulses directly from a single LV battery supply, without requiring the need to generate and regulate an HV supply on chip.

While the design presented in [32] also generates HV pulses from an LV input, it requires two LV supplies of 1.2 and 5 V and five 60-nF off-chip capacitors to achieve the efficiency listed in Table I. Furthermore, its charge-pump-like operation does not allow direct generation of HV pulses after start-up.

The design presented in [8] and [33] achieves higher efficiency, however at much lower transducer frequencies of 40 and 250 kHz, respectively, targeting haptics and other

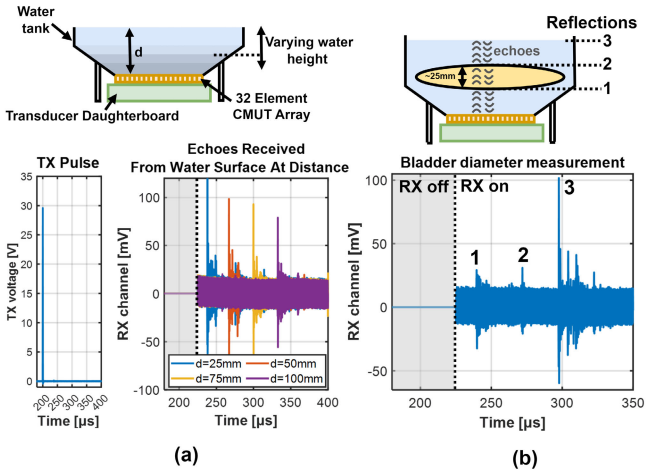

Fig. 19. Pulse-echo experiments. (a) Measurement of the reflection of the water surface. (b) Measurement of a bladder phantom.

low-frequency applications. Some of these works also require a very high PRF or continuous-wave pulsing to operate, such as [8] and [32], making them incompatible with the pulse-echo acquisitions required for imaging.

Furthermore, our work relies only on a single off-chip inductor and does not require any additional passive components for the transmitter to operate. The resonant pulser also has the added benefit of achieving programmable TX amplitudes.

VI. Conclusion

A prototype US ASIC implementing the resonant pulser for battery-powered wearable US devices has been presented. It employs a novel technique to directly generate a half-period sinusoidal HV excitation voltage on a US transducer without relying on a dedicated HV supply. The resulting architecture leads to a compact design that can be expanded to drive a full transducer array. By means of three autocalibration loops, the pulser deals with component and transducer tolerances, while only requiring 14 TX calibration cycles to be operational. After this initial calibration, the pulser operates synchronously and is free of static power dissipation. The timed nature of the resonant pulser provides a programmable TX amplitude between 10 and 30 V.

To the best of our knowledge, the prototype is the first reported US pulser capable of generating HV pulses directly from a single LV battery supply. It does so without relying on an HV supply, thus avoiding the overhead, conversion losses, and settling time associated with generating such a supply. Furthermore, it presents the lowest average power consumption among HV pulsers targeting US imaging. These features make the solution promising for future wearable US devices.

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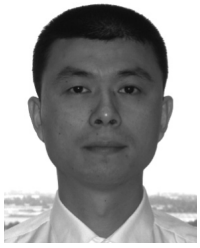

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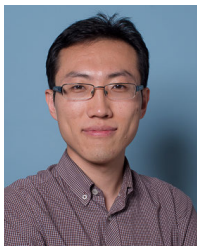

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