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DOI
10.1109/JSSC.2023.3279235

Publication date
2023

Document Version
Final published version

Published in
IEEE Journal of Solid-State Circuits

A Wideband Digital-Intensive Current-Mode Transmitter Line-Up

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***Abstract*— A current-mode direct-digital RF modulator (DDRM)-based transmitter (TX) architecture is proposed in this article for energy-efficient wireless applications. To demonstrate its key principles, a 2 × 13 bit demonstrator is implemented in a 40-nm CMOS technology. This DDRM can operate standalone or as a driver for a common-gate (CG)/common-base (CB) power amplifier (PA). The proposed DDRM is based on current-steering radio frequency digital-to-analog converters (RFDACs) that feature an extra current division path to allow the generation of the optimum current-mode class-B drive profile for the final CG/CB PA, facilitating energy-efficient TX operation without compromising linearity. For this purpose, the DDRM uses signed-IQ mapping combined with a class-B harmonic rejection (HR) technique. In addition, an advanced dynamic biasing technique is introduced to further enhance the TX line-up efficiency in deep power back-off (PBO) region. The DDRM driver standalone can provide 19.6-dBm RF peak output power. It supports a "160-MHz 256-QAM" signal at 2.4 GHz with an adjacent channel leakage ratio (ACLR) of −40.3 dBc and an error vector magnitude (EVM) of −33 dB, without using any digital pre-distortion (DPD). When connected to a CB SiGe PA, the overall TX line-up achieves an output power of 27 dBm and an overall TX system efficiency of 20%. This DPD-free TX line-up achieves an ACLR of −37.7 dBc and an EVM of −30 dB, respectively, when operating with an "80-MHz 64-QAM" signal at 2.2 GHz.**

***Index Terms*— Common-gate (CG)/common-base (CB) power amplifier (PA), current division path, digital pre-distortion (DPD)-free, direct-digital RF modulator (DDRM), dynamic biasing, harmonic rejection (HR), IQ-mapping, quadrature up-converter, radio frequency digital-to-analog converter (RFDAC), TX line-up.**

I. Introduction

RADIO FREQUENCY (RF) transmitters (TXs) used in modern wireless networks must deliver sufficient RF power, operate efficiently, and provide high integration while handling signals with large modulation bandwidth. Traditionally, analog-intensive TX architectures use a quadrature up-converter, comprising in-phase (I) and quadrature (Q) paths, and a following power amplifier (PA) as key building blocks [1], [2], [3], [4], [5], [6], [7]. Nonetheless, in these systems, their linearity–efficiency tradeoff typically entails low system efficiency. To address this challenge, over the past few years, digital TXs (DTXs) [8], [9], [10], [11], [12], [13], [14], [15], [16], [17], [18], [19], [20], [21], [22], [23], [24], [25], [26], [27], [28], [29], [30], which benefit from nanoscale CMOS technologies, have emerged as favorable alternative architectures. These architectures exploit RF digital-to-analog converters (RFDACs) or mixing-DACs. A pair of RFDACs with quadrature local oscillator (LO) input is often used to form an I/Q up-converter, which is referred to as a direct-digital RF modulator (DDRM) [11], [12], [13], [14], [15], [16]. Among them, current-steering DDRMs are well-known for their superior spectral purity due to their accurate and always-on current sources, making them excellent candidates for driving external PAs.

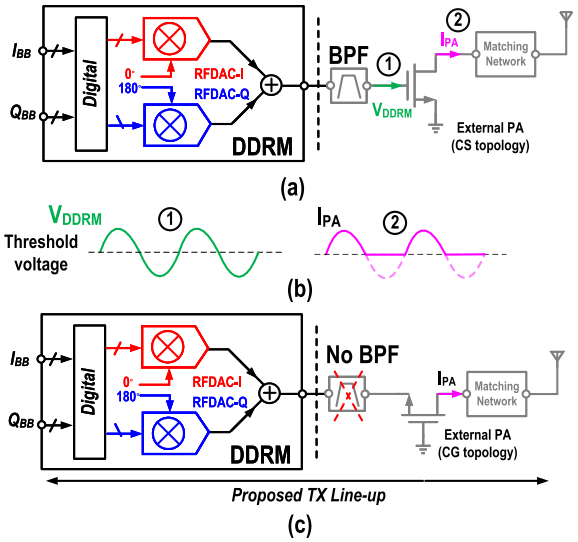

Fig. 1. (a) Conceptual diagram of DDRM drivers to drive a CS/CE PA. (b) Its corresponding voltage/current waveforms. (c) Conceptual diagram of the proposed current-mode DDRM to drive a CG/CB PA.

As depicted in Fig. 1(a), such an external PA is typically a common-source (CS)/common-emitter (CE) output stage biased in class-AB/B region. When the PA operates in class-AB/B, the drain current is clipped by the nonlinear I_d/V_{gs} or I_c/V_{be} relation of the output current responding on its driving input voltage, yielding the (distorted) class-AB/B waveform

Manuscript received 26 June 2022; revised 18 March 2023; accepted 10 May 2023. Date of publication 8 June 2023; date of current version 25 August 2023. This article was approved by Associate Editor Arun Natarajan. This work was supported by the Dutch Research Council (NWO) under Project 13315 "SEEDCOM" (Smart Energy Efficient Digital Communication) and Project 16336 "DIPLOMAT" (Highly Integrated Digital-Intensive Massive MIMO Transceivers). *(Corresponding author: Yiyu Shen.)*

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Color versions of one or more figures in this article are available at https://doi.org/10.1109/JSSC.2023.3279235.

Digital Object Identifier 10.1109/JSSC.2023.3279235

shown in Fig. 1(b). At first sight, one might conclude that this distortion only affects the higher harmonics of the TX signal. However, this non-linear I–V curve of the CS/CE device also contributes to counter-intermodulation distortions (C-IMDs) [31], degrading the spectral purity within the desired TX band. Practical m-MIMO systems use linearization techniques such as digital pre-distortion (DPD) to correct this distortion [1]. However, modern wireless systems use many TX line-ups, making DPD costly and power-hungry. In contrast, common-gate (CG)/common-base (CB) PAs provide an inherently linear current transfer function. In addition, the low input impedance of CG/CB PAs can improve linearity performance by increasing their immunity to the parasitic capacitors at the interconnection node. While some passive devices, e.g., in literature [32], can transform the typical 50-Ω load to a lower impedance, they cannot achieve the same low level as CG/CB PAs. Consequently, when aiming for such a current-mode scenario, the driver itself must implement the current clipping action needed for efficient output stage operation [e.g., class-B waveform in Fig. 1(b)]. Failing to do so will degrade the achievable TX efficiency.

In view of this, a current clamping technique was proposed recently in [33] to boost the efficiency of a millimeter-wave PA. It uses an inductor at the input of the CG/CB PA to clamp the output current envelope. In other words, this technique applies the adaptive biasing technique to a class-A PA, and thus, elevates the efficiency from class-A to a deep class-AB. However, this technique fails to provide the optimum "class-B" current waveform to the output stage, and therefore, its efficiency enhancement and linearity remain limited. In [34], the current of a class-E PA was modulated using a baseband DAC with a transconductor. While this polar approach improves the system efficiency, it requires a dedicated phase modulator and the alignment between the AM and PM signal paths, which all become increasingly more complicated with large modulation bandwidth signals.

This article focuses on a DDRM that directly provides the optimum (current-mode) drive signal for CG/CB PA, which features a linear current transfer [35]. In this way, the notorious linearity–efficiency tradeoff that characterizes analog-intensive solutions can be overcome. Such an approach is expected to avoid the need for DPD even when operating with broadband signals. The conceptual diagram of such a TX line-up is shown in Fig. 1(c).

This article is organized as follows. Section II first evaluates the two popular wideband DTX architectures for their capability to drive CG/CB PAs, namely, Cartesian digital PAs (DPAs) [23], [24], [25], [26], [27] and Cartesian DDRMs. Section III adds a current division path to the DDRM architecture to allow the generation of the optimum current-mode class-B drive signal. It also introduces three additional techniques to enhance linearity and efficiency: signed IQ-mapping, class-B-compatible harmonic rejection (HR), and dynamic biasing. The detailed design considerations of the resulting CMOS driver are given in Section IV. Section V discusses the CG/CB PA implementation, while Section VI gives results of both the DDRM standalone and embedded in a current-mode CB TX line-up. Finally, Section VII concludes this article.

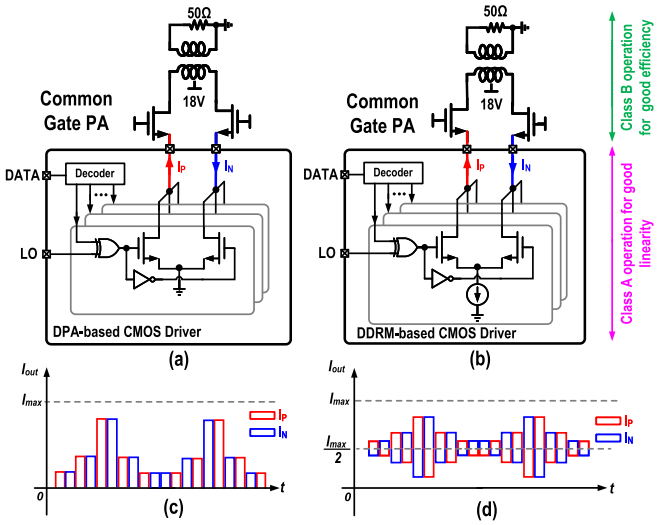

Fig. 2. Block diagram of (a) DPA ([36]) and (b) current-steering RFDAC/DDRM as a driver of CG/CB PA stages. Responding current waveforms for (c) DPA and (d) RFDAC/DDRM when applied a two-tone signal, respectively.

TABLE I
COMPARISON BETWEEN CARTESIAN DPA AND DDRM AS CURRENT-MODE DRIVERS

	Data Format	Operation Class	Linearity Performance	Efficiency Performance
DDRM	Unsigned	Class-A	High	Low
DPA	Signed	Class-B	Low	High
Proposed DDRM	Signed	Class-B	High	Medium

II. OVERVIEW OF DPA AND DDRM AS A DRIVER FOR CG/CB PA

Fig. 2(a) and (b) conceptually shows the circuit architecture of CG/CB PA driven by a simplified DPA and a DDRM, respectively. Note that only a single branch is shown in Fig. 2 instead of the complete quadrature configuration. Their current waveforms for a two-tone scenario are given in Fig. 2(c) and (d), respectively. To improve energy efficiency when DPA acts as a driver, it is common to use a signed data format for class-B operation [36], [37]. This configuration enables its dc current to scale down in proportion to the output amplitude, resulting in improved power efficiency [see Fig. 2(c)]. The driver's relatively low output impedance limits the linearity. Depending on the implementation, this can degrade the TX line-up linearity [38]. A current-steering RFDAC-based DDRM has a much higher output impedance and more accurate amplitude control word (ACW)-to-output current transfer. However, a DDRM normally relies on unsigned data and operates in class-A, yielding a high dc-current independent of output amplitude [see Fig. 2(d)] and degrading its efficiency. For example, at 6-dB power back-off (PBO), the achievable efficiency for a regular DDRM is only a quarter (12.5%) of the achievable ideal (class-A) peak efficiency (50%). In contrast, a DPA driver at 6-dB PBO provides still half (39.25%) of its class-B

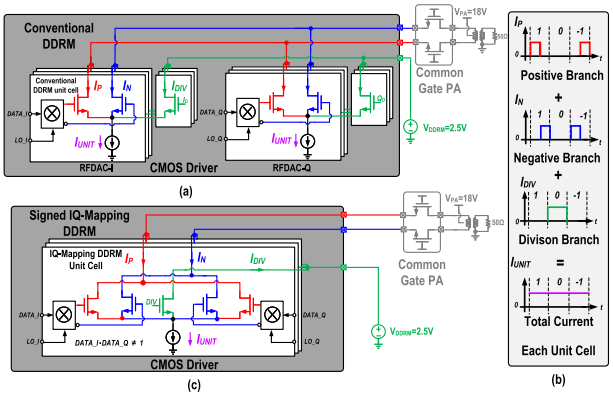

Fig. 3. (a) Conventional DDRM with current division paths. (b) Its unit cell up-converted current waveform. (c) Proposed DDRM architecture with the signed IQ-mapping technique [35].

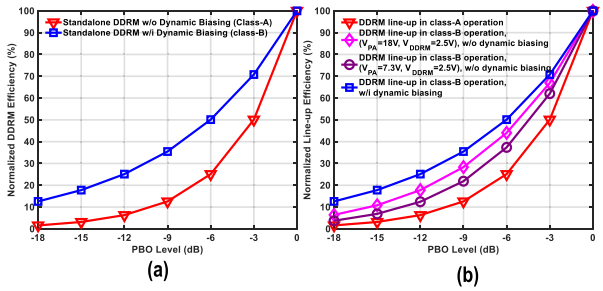

Fig. 4. Normalized drain efficiencies curve of (a) proposed standalone DDRM and (b) TX line-up.

peak efficiency (78.5%). The linearity–efficiency tradeoff of the Cartesian DPA and DDRM topologies driving a CG/CB is summarized in Table I. Meanwhile, other challenges deserve attention, namely, conventional (unsigned) DDRM topologies use two separate RFDACs leading to IQ mismatch, which degrades the in-band linearity. Furthermore, the use of a passive bandpass filter (BPF) between the (CMOS) driver and external PA is preferably avoided to extend the RF bandwidth [see Fig. 1(c)]. However, the absence of this network yields unfiltered harmonics (mainly the third and fifth) of the DDRM at the input of the CG/CB stage giving rise to C-IMDs, which deteriorates the spectral purity [31]. Last but even more important, modern wireless standards use higher order modulation schemes with a high peak-to-average power ratio (PAPR), yielding low average system efficiency. Therefore, the DDRM driver should adjust its dc power consumption to the RF signal envelope to alleviate this issue especially in the PBO region. The proposed DDRM architecture discussed in this article addresses all the above challenges.

III. DDRM Driver With Improved Efficiency and Spectral Purity

This section introduces an improved DDRM driver, which features a current division path, signed IQ-mapping, class-B HR, and dynamic biasing techniques. Each of these techniques enhances the energy efficiency while maintaining the signal purity.

A. Current Division Path

The efficiency–linearity tradeoff in current-mode DDRM-based TX line-ups can be overcome by introducing an additional current division path facilitating the generation of the ideal clipped current drive signal for the (external) CG/CB stage while keeping the tail current sources "always-on." The currents in the differential and division branches are shown in Fig. 3(a). The sum of the current in the differential and division branches is shown in Fig. 3(b). As can be observed, the total current in all the branches ($I_P + I_N + I_{\text{DIV}}$) remains constant and equal to the corresponding unary cell current source (I_{UNIT}). Due to this current division path, each unit cell can generate three different logical states, namely, $+1$, 0, and -1, as such, supporting the signed operation. Consequently, a close to ideal class-B (pre-)clipped current waveform can be provided to a CG/CB PA input, driving it in "ideal" class-B operation with related efficiency performance. The current-mode class-B operation of the CG/CB PA stage can provide high linearity, which benefits from the "always-on" operation of the unit cell current sources.

The efficiency penalty in the TX line-up due to the "always-on" DDRM current sources can be made very small. When considering the standalone DDRM, its normalized efficiency using "always-on" current sources is identical to the class-A case given in Fig. 4(a) (red curve).

When considering the TX line-up, at peak power, when all the DDRM current (I_{DDRM}) goes to the PA stage, the push–pull output signal has an amplitude of

$$V_{\text{out}} = I_{\text{DDRM}} \times R_L. \tag{1}$$

We assume that $V_{\text{out}} \leq V_{\text{PA}}$, where V_{PA} is the supply voltage of CG/CB PA. Next, for reasons of simplicity, we consider I_{DDRM} to be a square wave (here ignoring any possible use of HR techniques). In this case, the RF output power can be written as

$$P_{\text{RF,peak}} = \frac{8}{\pi^2} I_{\text{DDRM}}^2 R_L \tag{2}$$

with the peak efficiency given by

$$\eta_{\text{peak}} = \frac{8}{\pi^2} \frac{I_{\text{DDRM}}^2 R_L}{I_{\text{DDRM}} V_{\text{PA}}} = \frac{8}{\pi^2} \frac{I_{\text{DDRM}} R_L}{V_{\text{PA}}}. \tag{3}$$

In the PBO region, however, only a fraction of I_{DDRM} goes to PA, i.e.,

$$I_{\text{PA,PBO}} = m I_{\text{DDRM}}. \tag{4}$$

And the remaining part $(1-m)I_{\text{DDRM}}$ is supplied by DDRM supply voltage V_{DDRM}. Therefore, the output power is scaled by m^2

$$P_{\text{RF,PBO}} = \frac{8}{\pi^2} m^2 I_{\text{DDRM}}^2 R_L. \tag{5}$$

And the efficiency in PBO is

$$\eta_{\text{PBO}} = \frac{8}{\pi^2} \frac{m^2 I_{\text{DDRM}}^2 R_L}{m I_{\text{DDRM}} V_{\text{PA}} + (1-m) I_{\text{DDRM}} V_{\text{DDRM}}} = \frac{8}{\pi^2} \frac{m^2 I_{\text{DDRM}} R_L}{m V_{\text{PA}} + (1-m) V_{\text{DDRM}}}. \tag{6}$$

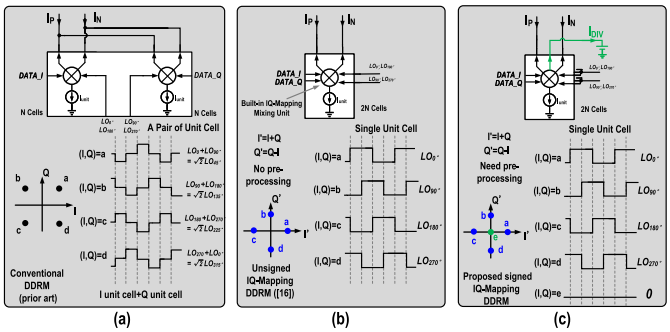

Fig. 5. DDRM evolution. (a) Conventional DDRM. (b) Unsigned IQ-mapping DDRM [16]. (c) Proposed signed IQ-mapping DDRM.

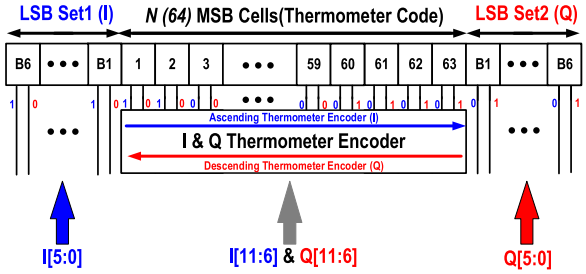

Fig. 6. I/Q complementary decoding scheme.

As shown in (6), if V_{PA} (e.g., >18 V) is much higher than V_{DDRM} (e.g., 2.5 V in this design), the dc power/efficiency penalty from "always-on" current sources in PBO region is minimal. Fig. 4(b) shows the normalized drain efficiency curves of the whole line-up for different values of V_{PA}. Due to the square waveform of the current, the efficiency for class-A and class-B operation will be the same at peak power. The overall dc power consumption scales down with output power, as such, approximating class-B operation. And with higher V_{PA}, the overall efficiency–PBO curve is closer to ideal class-B curve. Nevertheless, in the deep PBO region (e.g., $\geq$ 12 dB), since most of I_{DDRM} is supplied by V_{DDRM}, the efficiency penalty is no longer negligible. Therefore, a dynamic biasing technique was added to this concept to boost its system efficiency also in deep PBO operation [blue curve in Fig. 4(b)]. For the standalone DDRM driver, when including the dynamic biasing technique, the normalized efficiency of the standalone DDRM will closely approximate to the blue curve in Fig. 4(a). The dynamic biasing technique will be discussed in detail later in this section.

B. Signed IQ-Mapping Technique

The DDRM topology in Fig. 3(a) enables signed-IQ operation but still relies on two standalone RFDACs with separate current sources in their unit cell pairs to implement the IQ operation, yielding IQ mismatch. In [16], an *unsigned* IQ-mapping technique was proposed to cancel the IQ image and boost the DDRM output power. In this work, we extend the concept of [16] to *signed* IQ-mapping operation. The newly proposed DDRM topology provides bitwise current-mode up-conversion while featuring only one current source per IQ-unit-cell [see Fig. 3(c)]. Fig. 5 gives the DDRM evolution from the conventional DDRM topology [see Fig. 5(a)] through the unsigned IQ-mapping technique [see Fig. 5(b)], to the proposed signed IQ-mapping technique [see Fig. 5(c)]. Both the unsigned and signed IQ-mapping DDRMs use their dc-current budget more energy-efficiently by mapping the square constellation diagram to a diamond-shaped one, as such avoiding (complex) analog IQ vector summation within the unit cells.

1) Unsigned DDRM Operation: The unit cells of the unsigned DDRM shown in Fig. 5(a) support two independent states for I and Q, namely, +1 and −1, yielding four constellation points. Using a single current source unit cell [see Fig. 5(b)], the four constellation points in conventional DDRM unit cells can be directly hardware mapped to the four phases of the LO, resulting in the diamond-shaped constellation diagram [16].

2) Signed DDRM Operation: The signed DDRM of Fig. 3(a) has two current sources and can, due to the extra current division path(s), support three independent states: +1, −1, and 0 for both I and Q, yielding nine combinations. When using a single current source for the signed IQ unit cell [see Fig. 5(c)], only five of the original nine constellation points can be supported, which satisfies the orthogonality requirement related to IQ operation

$$|I_{\text{unit}}| \cdot |Q_{\text{unit}}| = 0. \tag{7}$$

In contrast to the unsigned case where the mapping can be implemented directly in the hardware of the unit cell [16], pre-processing of the baseband data is required in the signed IQ-mapping operation

$$\begin{cases} I' = I + Q \\ Q' = Q - I. \end{cases} \tag{8}$$

To achieve the signed operation in each unit cell, when both the DI and DQ are zero, regardless of the sign bits (SI and SQ), the division path will be activated. When one of SI and SQ is 1 (and assume DI = 1), the output phase is either 0° or 180°, which will be determined by the sign bit (SI).

Besides the pre-processing given in (8), a custom decoding scheme is required to implement the signed IQ-mapping DDRM. An adapted version of [24] is used in Fig. 6. For the most significant bit (MSB) cells, the I decoding scheme is in ascending order, while the Q decoding scheme is in descending order. For the LSB cells, since the values of binary bits are not constrained by (7), the I/Q overlap cannot be systematically avoided [24]. Therefore, LSB banks for I and Q are kept separate to handle the situation when I and Q LSB are both 1. A combination of 6-bit MSB unary cells and 6-bit LSB binary cells is selected as the best compromise in the chip area, design complexity, and power consumption [39].

Similar to [16], this technique doubles the RF output power for a given current budget since (8) can be transformed to

$$||(I', Q')||^2 = 2||(I, Q)||^2. \tag{9}$$

Therefore, compared with conventional DDRM, the proposed architecture can provide 3 dB more output power for the same dc-current budget.

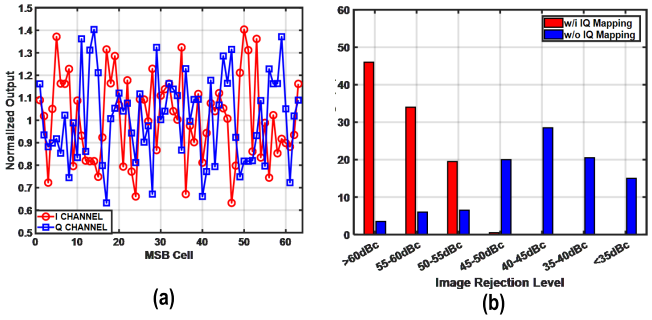

Fig. 7. (a) DNL pattern of MSB cells in the proposed decoder pattern (the DNL pattern of I and Q is inverse to each other). (b) IRR distribution with $\sigma = 1$ LSB with and without signed IQ-mapping technique in MC simulations.

In [24], the applied decoder scheme was used to relax the DPD. Here, the modified version of this decoder is used to suppress the IQ image. Namely, the I and Q branches share the same MSB cells (although with opposite decoding schemes). Consequently, the resulting IQ mismatches and their DNL are strongly correlated but have a reversed dependency. An example of such a reversed DNL pattern is shown in Fig. 7(a). It is this correlation that suppresses the IQ image. The Monte Carlo (MC) simulations with a single-sideband signal demonstrate the effectiveness of this approach [see Fig. 7(b)]. For this purpose, DDRMs with 6-bit MSB unary cells and 6-bit LSB binary cells are evaluated. Without the proposed signed IQ-mapping technique, the image rejection ratio (IRR) is worse than 50 dBc, when simulating with a deviation of $\sigma = 1$ LSB. In contrast, the IRR is better than 55 dBc when the signed IQ-mapping technique is applied. Note that the IQ image is not perfectly canceled, as is the case in the unsigned IQ-mapping technique [40]. There are two reasons for this: first, the DNL curves of MSB cells in the I and Q paths are flipped instead of perfectly equal, so their distortion is correlated, although not identical. Second, the LSB banks for I and Q are kept separate in the signed IQ-mapping DDRM, while in unsigned IQ-mapping DDRM, the LSB bank is shared. Thus, any mismatch in the LSB cells is independent in the signed DDRM. Both the sources contribute to the residue IQ image.

C. Class-B HR Technique

HR techniques are typically introduced to suppress the third and fifth harmonics in class-A operated circuits [41]. The principle of class-A HR is shown in Fig. 8(a) and (b) [41]. It consists of three RFDACs of which their LO signals have a progressive phase shift of 45°. In addition, they have to be scaled in amplitude with a factor of 1, $\sqrt{2}$ and 1, respectively. However, this HR scheme cannot be directly applied in the proposed class-B DDRM since in Fig. 8(c), the duty cycle after IQ summation is 100%. Therefore, for class-B HR, the waveform of $\mathrm{LO}_{\mathrm{total}}$ in Fig. 8(b) must be clipped by half. Fig. 8(d) and (e) shows, respectively, the class-B HR block diagram and the related time-domain waveform. The resulting individual I and Q class-B HR waveforms will have a 50% duty cycle. Moreover, after IQ summing, we obtain the waveform in Fig. 8(f), having a 75% duty cycle. Meanwhile, the resulting class-B waveform still suppresses the third and fifth harmonics, but now also contains even harmonics [see Fig. 8(g)]. The impact of these even harmonics can be eliminated by applying a differential output stage.

A similar class-B-like HR technique was earlier introduced in [42] for RX design. In [30], class-B HR was applied to a polar DTX to cancel the third harmonic. However, it is rather challenging to accurately generate the required 25% and 50% phase-modulated signals in a polar system. The Cartesian architectures, which use fixed clocks, are more naturally suited for applying class-B HR techniques.

D. Dynamic Biasing Technique

As proved in (6), in the deep PBO region, the dc power consumption of division path is no longer negligible. Therefore, in the proposed signed IQ DDRM, the unused current can be independently scaled down using the current division path in the 50% and 25% duty-cycle RFDACs. Fig. 9 demonstrates the principle of this proposed dynamic biasing technique, where I_{DIV} is the current that goes to the current division path. The current sources not needed for generating the output signal in PBO can be (pre-)turned on/off, shift from gray to green, or vice versa (see Fig. 9), to improve the system efficiency.

The detailed schematic of the current source switch is shown in Fig. 10(a). The current re-direction technique pre-activates the current sources so that their turn-on time does not degrade the linearity. When the current sources are off, the dummy diode is pre-charged, accelerating the turning-on process. Note that the current source turn-on process still takes more than 50 ns due to the large device size (needed for the matching of the current sources), which limits the signal bandwidth when applying this technique. To tackle this issue, independent current control allows the pre-activating of the current sources (see Fig. 9) to preserve the linearity. The turn-off process is not critical since the current is already re-directed to the current division path before the current source is off entirely.

Fig. 10(b) shows the decoder topology for dynamic biasing, which is similar to the previous IQ RFDAC design in Fig. 6. Two thermometer decoders are used with the reversed order. The IQ signal goes through an OR gate to control the on/off state for the current source. In this design, only unary MSB cells can be turned on/off since the majority of the RF power is generated there. The switches in LSB cells are only dummies for matching purposes.

IV. Design of CMOS Driver: System Architecture and Implementation Details

A. System Architecture of CMOS Driver

The block diagram of the proposed DDRM driver is shown in Fig. 11 and includes all the features mentioned earlier. The overall system consists of two RFDACs with a resolution of 13 bits (including SI). The eight phases needed by the HR technique are generated ON-chip. For this purpose, a $4 \times f_{\mathrm{LO}}$ sinusoid signal is provided by an external signal source. As depicted in Fig. 11, the IQ baseband data are fed to SRAMs through an SPI. Four ON-chip SRAMs are time-multiplexed to create a bit-stream throughput equal to half of the center

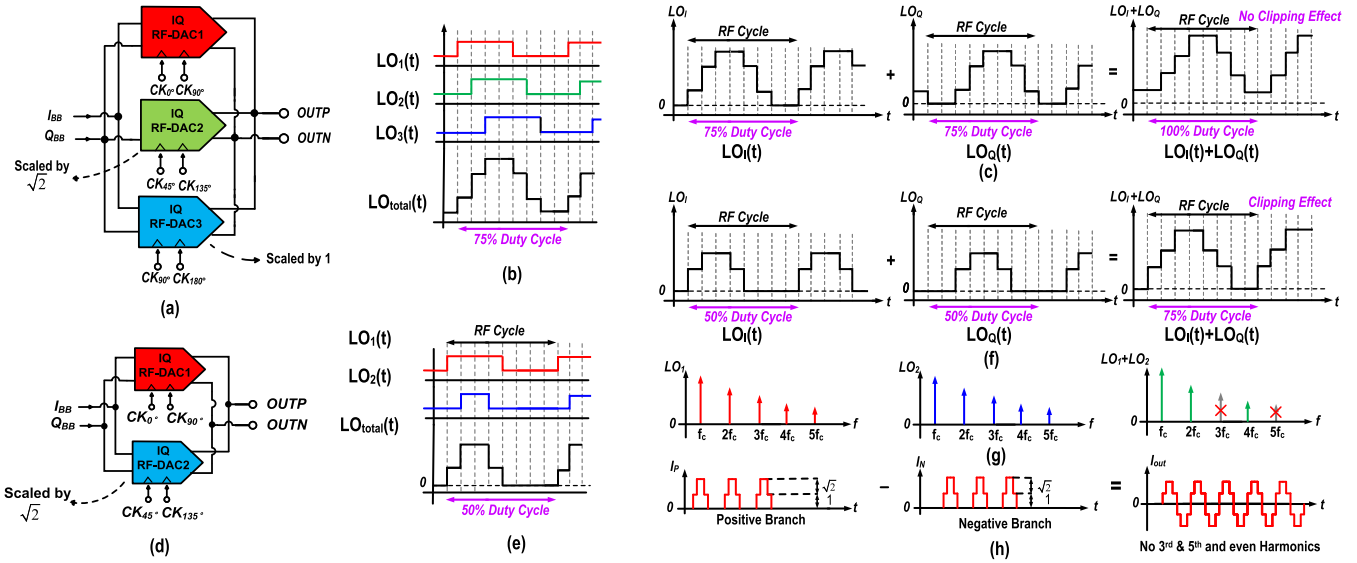

Fig. 8. Principle of class-A HR technique: (a) block diagram, (b) timing diagram, and (c) waveform after IQ summing. Principle of the proposed class-B HR technique: (d) block diagram, (e) timing diagram, and (f) waveform after IQ summing. (g) Spectrum of class-B HR and (h) push–pull output to cancel even harmonics.

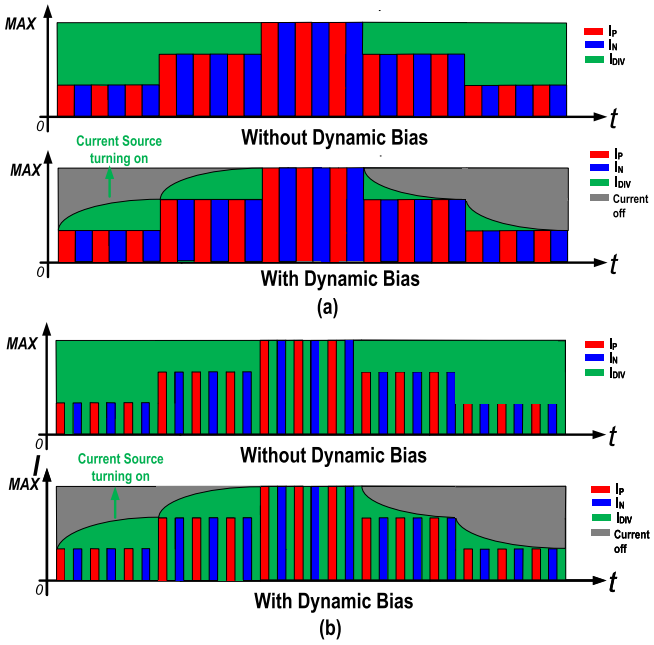

Fig. 9. Concept of dynamic biasing technique: (a) with 50% duty-cycle RFDAC and (b) with 25% duty-cycle RFDAC.

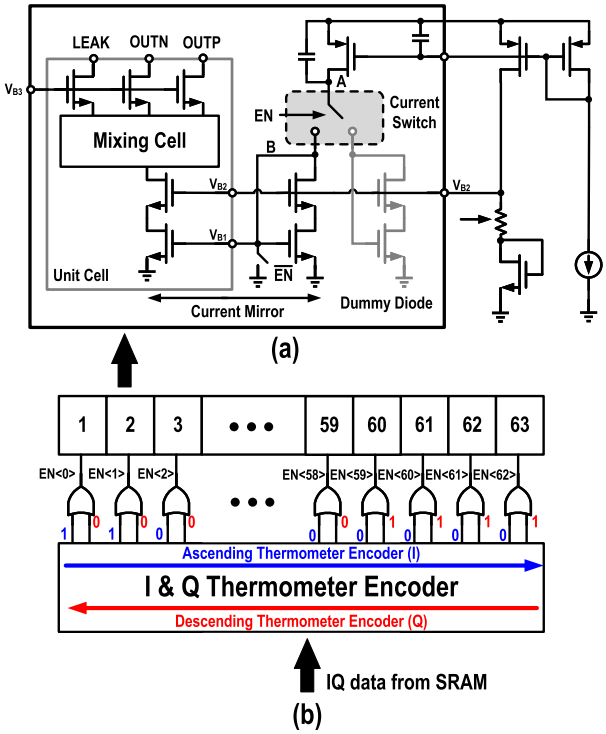

Fig. 10. (a) Topology of current source switch in unit cells and (b) thermometer decoding scheme for dynamic biasing.

frequency, f_{LO}. Such a high data rate supports modulation bandwidths up to 160 MHz, pushing the sampling spectral replica far away from the main signal.

B. Unit Cell Implementation

The top-level current-steering unit cell with the current division path is shown in Fig. 12. The implementation of the 50% and 25% duty-cycle RFDAC is similar, except for the mixing cell. In each unit cell, using an appropriate bitwise operation, the IQ baseband data are up-converted using the corresponding quadrature LO clocks. Thick-oxide cascode transistors are placed in all the three paths to enhance the linearity performance. To enlarge the current capability, the mixing cell and top cascode transistors are put inside a deep n-well (DNW), with an elevated bulk voltage of 0.6 V. The related LO and data signals are shifted to the 0.6–1.7-V domain in advance.

The mixing cell differs significantly from [40] due to the introduction of the current division path and signed operation. The mixing cell schematics for the 50% and 25% duty-cycle operation are depicted in Fig. 12.

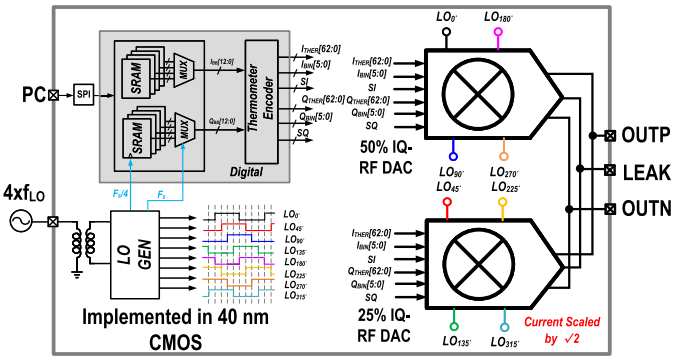

Fig. 11. Proposed DDRM driver's block diagram with standalone testing output circuitry.

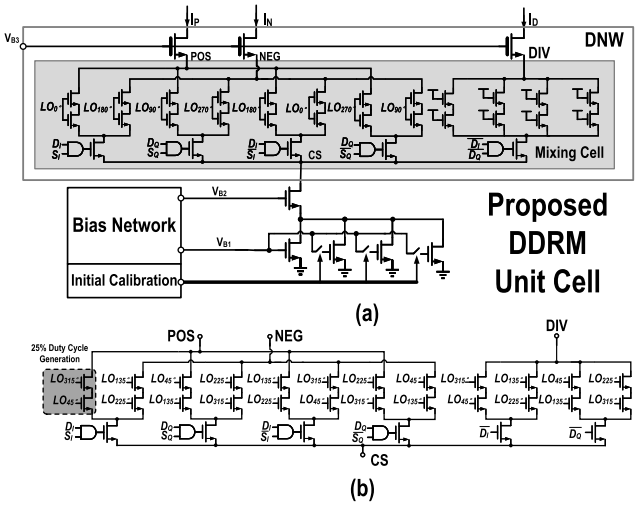

Fig. 12. (a) Schematic of the proposed unit cell with mixing cell of 50% duty-cycle RFDAC and (b) schematic of mixing cell of 25% duty-cycle RFDAC.

The decoded data are generated by the bitwise and operation of the I/Q data and SIs: $DI \cdot SI$, $DQ \cdot SQ$, $DI \cdot \overline{SI}$, and $DQ \cdot \overline{SQ}$. Subsequently, the up-conversion is performed using bitwise multiplication of the quadrature LO clocks with the related decoded data by the current-mode XOR/XNOR. The decoding logic for positive and negative branches is identical for both the 50% and 25% duty-cycle IQ RFDACs. However, their local decoding schemes are different for the current division path. The latter can be understood by considering Fig. 9. Namely, for the 25% duty-cycle RFDAC unit cell, even when the IQ data are active, the current division path still carries current for a part of the RF cycle. In the 50% duty-cycle RFDAC unit cells, however, the current division path only turns on when both I and Q are inactive.

Furthermore, the proposed 25% duty-cycle RFDAC topology generates its low duty-cycle signals locally at the unit cell level in Fig. 12(b). Using an AND of two 50% duty-cycle and 90°-shift quadrature clock signals, the impact of delay and duty-cycle mismatch between the two LO distribution networks of the 25% and 50% RFDACs can be minimized.

C. LO Generator

The schematic of the LO generator is shown in Fig. 13. The eight phases needed for the HR are generated by dividing the external $4 \times f_{LO}$ clock signal ON-chip after going through ON-chip transformer balun and phase alignment. The two-stage quadrature divider uses current-mode logic (CML) and clocked CMOS (C^2MOS) latches. Then resulting eight phases are re-timed by C^2MOS D-flip-flops (DFFs) before being fed to LO distribution networks. The eight LO signals are shifted from 0 to 1.1 V to the 0.6–1.7-V voltage domain using ON-chip "bias-Tees." The higher voltage domain is use to maximize the current handling and output power capability of the output stages.

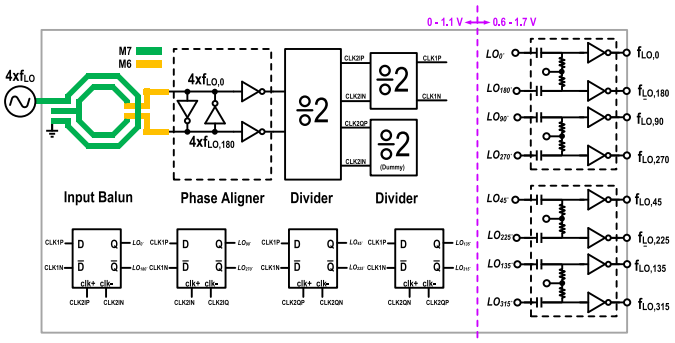

Fig. 13. Schematic of the LO generator.

V. Design of CG/CB PA

In the proposed TX line-up, the voltage gain of CG/CB PA is essential in achieving high efficiency. This section focuses on the design considerations of the CG/CB PA used in the TX line-up. NXP's SiGe technology QuBiC was selected for this demonstrator. The schematic of the CB PA with the CMOS driver is shown in Fig. 14. The CB PA collector voltage was limited to 7.3 V to avoid the device breakdown, while its base was biased at 2.9 V in view of the CMOS current-mode driver. Two design aspects require special attention, namely, limiting the series impedance in the CMOS driver-CB stage connection and enabling an adjustable bleeding current by the driver to maintain the CG/CB PA linearity.

In Fig. 14, the CB input voltage $V_{PA,in}$ can be expressed as

$$V_{PA,in} \approx \frac{1/g_m}{Z_{Series} + 1/g_m} V_{Driver} \tag{10}$$

where V_{Driver} is the output voltage of DDRM driver, g_m is the transconductance of the PA, and Z_{Series} is the series inductive impedance. Based on (10), Z_{Series} can corrupt the voltage gain, and thus, the output power. Therefore, flip-chip is the best candidate to minimize the connection inductance. However, due to process limitation, wire-bonding is used for this demonstrator. To lower the bonding wire inductance, multiple-parallel bondwires can be used. However, when placing them simply in parallel, their mutual coupling still puts a higher bound on the effective inductance of the overall bondwire structure. Therefore, in this demonstrator, the bonding wires for positive and negative branches are placed alternately such that their magnetic fields cancel each other, yielding a strong reduction of the effective inductance of this structure.

Furthermore, since the signed DDRM driver provides a "clipped" current waveform, the CG/CB transistors are forced

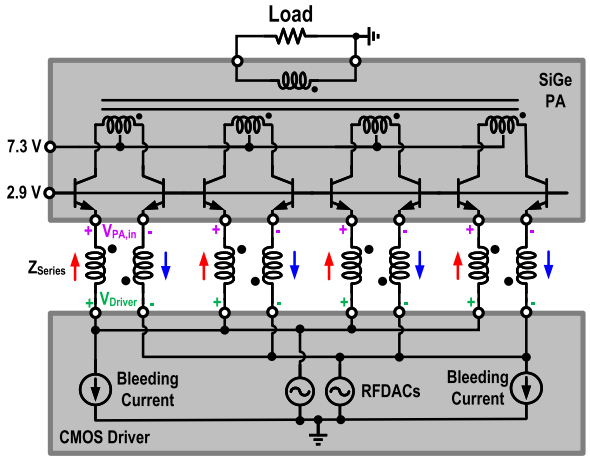

Fig. 14. Conceptual diagram of CB PA with connection to CMOS driver.

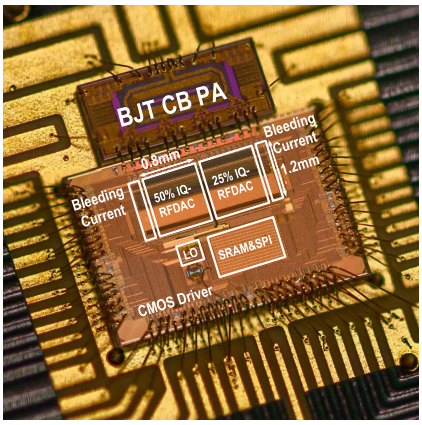

Fig. 15. Chip micrograph of the proposed TX line-up.

to switch between the triode/linear region and the saturation/active region, which corrupts their linearity performance. Therefore, it is beneficial to keep the CG/CB PA in its saturation/active region. This can be achieved by adding a pair of static bleeding current sources to the CMOS driver (see Fig. 14), which is popular in the high-speed baseband DAC designs [43] and [44]. Such bleeding current sources can boost the linearity at a small power penalty. In this design, the bleeding current can be set between 0 and 100 mA.

VI. Measurement Results

The proposed CMOS driver is fabricated in a bulk 40-nm CMOS process, and the core design, excluding the SRAMs, occupies an area of 2.4 mm^2. As mentioned earlier, the CB PA is fabricated in NXP's QuBiC SiGe technology. Fig. 15 shows the micrograph of the proposed TX line-up.

The measurement results are presented in two parts: one on the standalone CMOS driver and one on the overall TX line-up. In the measurement for the standalone driver, to imitate the low input impedance level of CG/CB PA, an OFF-chip balun at output node, which is shown in Fig. 11, is adopted from [45] to transfer the 50–7.5-Ω differential load. In TX line-up measurement, the output directly goes to $50-\Omega$ load since there is already a balun inside the CB PA die. Note that the dc power consumed by SRAMs is excluded from the total power consumption since the SRAMs are used only for measurement purposes. In practice, high-speed interfaces or local up-sampling circuits can be exploited at a much lower power budget. Most importantly, no DPD is applied in both the measurements.

A. Measurement Results: Standalone CMOS Driver

Fig. 16(a) shows the measured peak RF output power versus carrier frequency, i.e., P_{out} versus f_{LO}, and the third and fifth harmonics level of f_{LO} from 1 to 3 GHz in continuous-wave (CW) measurements. Note that the operational range is limited by the OFF-chip balun. At 2.4 GHz, the peak P_{out} reaches 19.6 dBm, and the dc power consumption, i.e., P_{dc}, is 505 mW without the testing SRAMs, achieving an efficiency of about 18%. The third and fifth harmonic levels

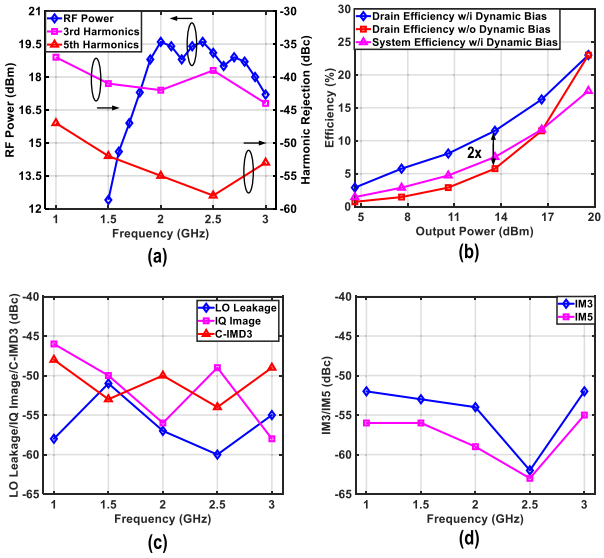

Fig. 16. (a) Measured peak output power, HR ratio versus f_{LO}. (b) Efficiency versus output power with/without dynamic biasing at 2.4 GHz. (c) LO leakage, IQ image, and C-IMD3 in single-tone test versus f_{LO}. (d) IM3 and IM5 in two-tone test versus f_{LO}.

shown in Fig. 16(a) are better than −36 and −46 dBc, respectively. The drain/system efficiency with/without dynamic biasing versus in normalized input power P_{in} is shown in Fig. 16(b), showing that the drain efficiency is doubled at 6-dB PBO which is predicted in Fig. 4(a).

Fig. 16(c) shows the LO leakage, IQ image, and third-order C-IMD (C-IMD3) versus f_{LO} in a single-tone test with maximum output power. At 2.5 GHz, the LO leakage, IQ image, and C-IMD3 are lower than −60, −49, and −54 dBc, respectively. Fig. 16(d) presents the IM3 and IM5 in the two-tone tests with maximum output power, demonstrating that IM3 and IM5 are lower than −60 dBc at 2.5 GHz.

The performance of the standalone DDRM driver is also verified using complex modulated signals. Due to the limited ON-chip SRAM memory depth, we did not measure with standard complex-modulated communication signals. Fig. 17(a) depicts the spectral purity of a 20-MHz bandwidth single-carrier 256-QAM signal at 2.4 GHz when the dynamic biasing is enabled. It yields an adjacent channel leakage ratio (ACLR)

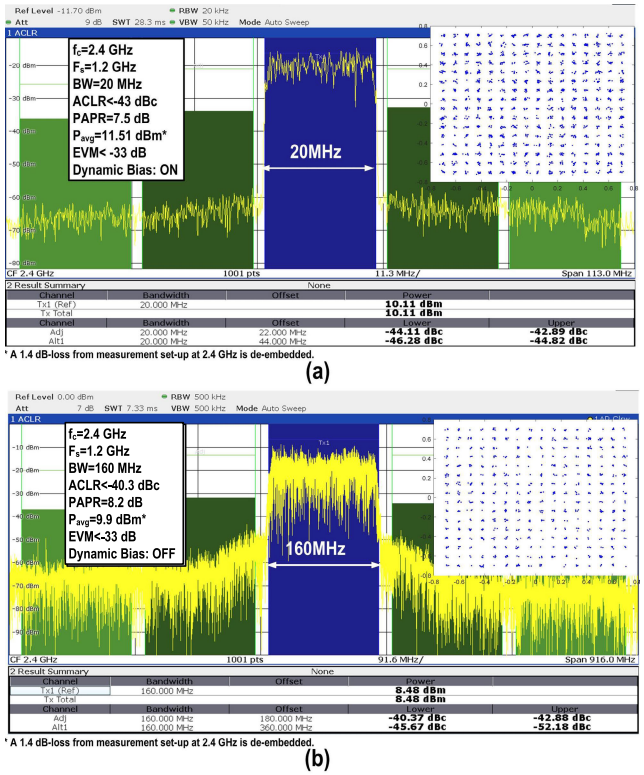

Fig. 17. Measured spectrum and constellation diagram of the (a) "20-MHz 256-QAM" signal with dynamic biasing and (b) "160-MHz 256-QAM" signal without dynamic biasing at 2.4 GHz.

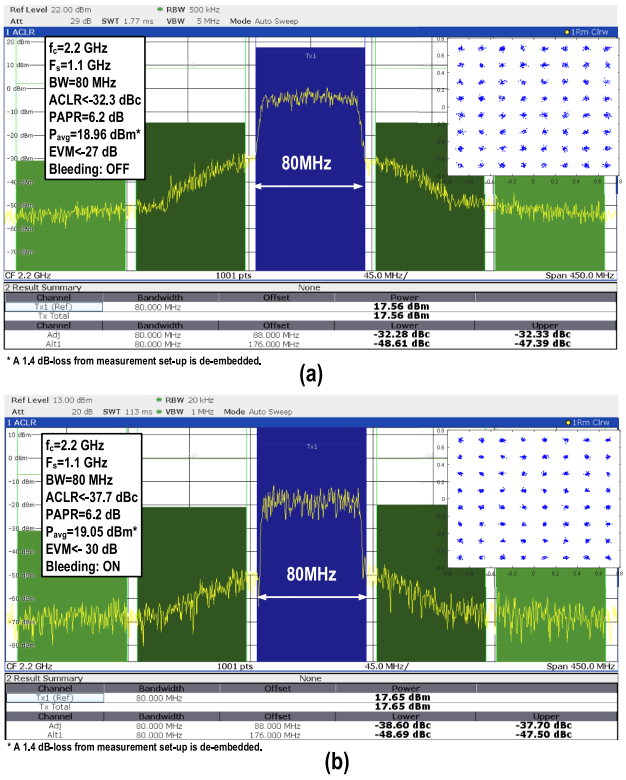

Fig. 19. Measured spectrum and constellation diagram of the "80-MHz 64-QAM" signal (a) without and (b) with 100-mA bleeding current, respectively.

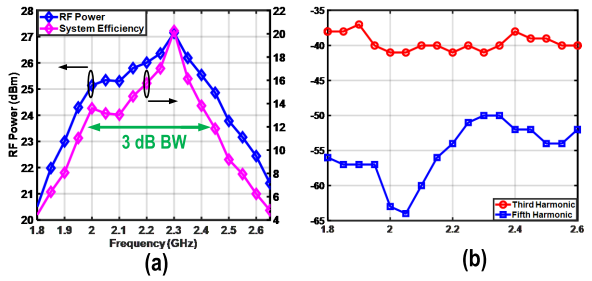

Fig. 18. CW measurement with whole system. (a) Peak power and system efficiency versus f_{LO}. (b) Third and fifth harmonic levels versus f_{LO}.

of −43 dBc and an error vector magnitude (EVM) of −33 dB, respectively. As discussed, for a larger modulation bandwidth, the dynamic biasing technique becomes less effective and is thus switched off. The measured spectrum of a 160-MHz bandwidth single-carrier 256-QAM signal with 1-dB extra PBO is shown in Fig. 17(b). The resulting out-of-band spectral purity is better than −40.3 dBc, while its EVM is better than −33 dB.

B. Measurement Results: CMOS Driver-CB Stage TX Line-Up

This part focuses on the measurement results of the complete TX line-up. First, CW measurement results are given in Fig. 18(a), and the third and fifth harmonic levels are shown in Fig. 18(b). The achieved 3-dB bandwidth is 2–2.45 GHz, indicating a relative bandwidth of 20%. The maximum peak power is more than 27 dBm, with a peak system efficiency of 20%. This somewhat low system efficiency is mainly caused by the relative low collector voltage used for the SiGe CB PA (7.3 V). As discussed in (6), the collector voltage needs to be much higher than the DDRM supply to maximize the RF power and, consequently, the overall efficiency.

In addition, modulated signals are used to test the TX line-up linearity. Fig. 19 shows the measured spectrum with an "80-MHz 64-QAM" signal at 2.2 GHz, with and without bleeding current, respectively. With 100-mA bleeding current, the proposed system achieves an ACLR of better than −37.7 dBc and an EVM of better than −30 dB, respectively.

C. Comparison With State-of-the-Art Drivers and Line-Ups

The performance of the proposed CMOS driver standalone is summarized in Table II and compared with other state-of-the-art DDRMs, Cartesian DTXs, and analog modulators. Our standalone signed-Cartesian CMOS driver can support a bandwidth as high as 160 MHz, which is only exceeded by our previous work focusing on unsigned operation [40]. When comparing the system efficiency, this work provides competitive result among the reported DDRMs without compromising the linearity performance. The peak efficiency comparison of this work, which provides high modulation bandwidth while omitting the need for DPD, with narrowband DPAs requiring DPD is less straightforward. Namely, the power consumption needed for performing the DPD in these works is not given.

TABLE II
PERFORMANCE SUMMARY AND COMPARISON WITH STATE-OF-THE-ART QUADRATURE MODULATORS AND PA DRIVERS

Specification		This Work		[15] ISSCC20	[11] JSSC18	[14] JSSC21	[40] JSSC22	[17] ISSCC20	[38] CSICS15	[24] ISSCC16	[26] ISSCC21	[25] ISSCC20	[6] ISSCC20
Architecture		DDRM		DDRM	DDRM	DDRM	DDRM	CDAC	DPA	DPA	DPA	DPA	Analog
Matching Network		Off-Chip		On-Chip	Off-Chip	Off-Chip	Off-Chip	On-chip	Off-Chip	Off-Chip	On-Chip	On-Chip	On-Chip
Technology	[nm]	40		65	40	65	40	65	180 SOI	40	40	55	28
Frequency	[GHz]	1-3		1.4-3	0.9-3.1	0.9-5.2	0.5-3	2.2	0.9	2.4	2.4	0.85	1.4-2.7
Peak P_{out}	[dBm]	19.6@2.4GHz		22	9.2	15	18.2	13	31.6	27	30.3	29.3	3[5]
DC Power	[mW]	505@2.4GHz		1350	146[3]	900	540	N.A.	2140	2230	2950	1974	70.5[6]
Peak η	%	18.1		11.7	9.2	3.5	12.2	N.A.	66	22.4	36.5	43	N.A.
f_{LO}	[GHz]	2.4		2.2	3	2.4	2.4	2.2	0.9	2.4	2.4	0.85	2.5
Bandwidth	[MHz]	20[1]	160[2]	20	57	20	320	40	5	40	60	10	20
Modulation Type		256 QAM	256 QAM	256 QAM	64 QAM	256 QAM	256 QAM	1024 QAM OFDM	LTE	64 QAM OFDM	64 QAM	64 QAM	64 QAM
ACLR1	dBc	-43[1]	-40.3[2]	-45	-44	-42	-43	<-45[4]	-36	<-40	-32	-32	-44
EVM	dB	-33[1]	-33[2]	-40	-30	-42	-32	-42[7]	N.A.	<-30	-31.7	-25.6	-34.4
PAPR+PBO	dB	7.5	9.2	4.6	5.5	4	8	16	6.7	8	7	5.7	N.A.
Avg. Sys. η	%	4.7[1,8]	1.8[2,8]	4.5	N.A.	1.05	N.A.	N.A.	35	14.5	30.7	24.4	3.6
DPD	Y/N	No		Yes	No	No	No	No	Yes	Yes	Yes	No	IQ Cal

[1]Dynamic biasing enabled; [2] dynamic biasing disabled; [3] LO generation power is not included; [4] estimated from figure; [5] average power; [6] not including baseband DAC; [7] measured at the output of -3dBm.
[8] without calibrating the return loss of the instrument.

TABLE III
PERFORMANCE SUMMARY AND COMPARISON WITH STATE-OF-THE-ART DIGITAL-INTENSIVE CMOS-MMIC LINE-UPS

Specification		This Work	[36] Diddi' RFIC16	[47] Bootsman' TMTT22
Architecture		DDRM+PA	DPA+PA	DPA+PA
Connection Mode to PA		Current (CB)	Current (CG)	Voltage (CS)
Technology: CMOS+MMIC		40nm+SiGe	180nm SOI+GaN	40nm+LDMOS
Output Matching Network		On-Chip	Off-Chip	Off-Chip
On Chip Modulator	Y/N	Yes	No	No
Supply Voltage	[V]	1.1/2.5/7.3	1.5/4.1/15	1.1/2.5/20
Frequency	[GHz]	2.2	0.9	2.1
Peak P_{out}	[dBm]	27	34.5	43.7
Peak Efficiency	%	20	57.7[3]	58.1
Bandwidth	[MHz]	80	5	10
Modulation Type		64 QAM	16 QAM	256 QAM
ACLR1	dBc	-32.3[1]/-37.7[2]	-36.6	-46.1
EVM	dB	-27[1]/-30[2]	N.A.	-38
DPD	Y/N	No	Yes	Yes

[1] Without bleeding current; [2] with bleeding current; [3] drain efficiency.

Furthermore, the required power for DPD increases rapidly with the modulation bandwidth.

Although the proposed architecture demonstrates superior linearity performance, it faces challenges in extending to higher frequency bands, such as FR2 [46], due to the escalating impact of parasitic capacitors. An active mixer approach can be used to overcome this challenge which handles the input capacitance of the output stage. It is worth noting that this active mixer approach remains compatible with the techniques proposed in this work.

Table III shows comparison of the system performance with other TX line-ups. This work covers a DPD-free linear, wideband DTX line-up with ON-chip modulator and matching network. As such, it achieves the highest modulation bandwidth and best linearity performance in the table. However, its power efficiency is lower than other works, mainly due to the low supply voltage used for the CB PA, which constrained by breakdown limitations. When combining the high-power CG GaN PA (drain voltage 15 V) of [36] with the proposed driver, output power and system efficiency will be boosted dramatically. Meanwhile, since in Table III the works of [36] and [47] do not include the power of RF (phase) modulator or DPD blocks, their overall system efficiency is positively affected. Nevertheless, the provided comparison demonstrates that the proposed TX line-up presents a good linearity and large modulation bandwidth without DPD, while having the potential to obtain a high system efficiency is very well feasible.

VII. CONCLUSION

This article presents a novel TX line-up based on a current-mode CMOS driver-CG/CB PA architecture to gain high output power, efficiency, spectral purity, and modulation bandwidth simultaneously, without requiring any DPD. The proposed CMOS driver features a current division path, signed IQ-mapping, dynamic biasing, and class-B HR techniques to boost its efficiency and linearity. In addition, additional design considerations are provided for the CG/CB PA design. The proposed driver operates over a frequency range of 1–3 GHz while generating 19.6-dBm peak RF power at 2.4 GHz. For a "160-MHz 256-QAM" signal, the measured ACLR and EVM is better than −40.3 dBc and −33 dB, respectively. Together with a CB PA implemented in a SiGe technology, the peak output power of this TX line-up is 27 dBm. The overall system achieves an ACLR of −37.7 dBc and an EVM of −30 dB without any DPD while handling an "80-MHz 64-QAM" signal. The proposed DPD-free TX line-up is an interesting candidate for future pico-cell base stations in 5G cellular network or WLAN systems.

ACKNOWLEDGMENT

The authors would like to thank Dutch Research Council (NWO) for financial support, and Ampleon B.V and NXP.

Inc. for their technical support. They want to acknowledge the contribution of A. Akhnoukh, M. Pelk, and Z. Chang, all with TU Delft, for their support, and IMEC-Leuven for tape-out support. They would like to pay tribute to the late Prof. McCune, with TU Delft, for his invaluable and enlightening technical discussion.

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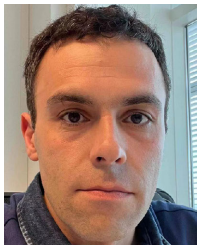

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