Life Expectancy of DC Fast Charger

Effect of load profile on thermal degradation of semiconductors

Sustainable Energy Technology

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by

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Preface

This thesis represents my learning of electrical and electronic engineering during my brief time at TU Delft. It combines both my passions for sustainability and automotive engineering. Looking back, I remember how challenging and intense this course in Sustainable Energy Technology was. Coming to a different country, and adapting to a different cultural and educational system, especially during COVID is not easy. Moreover, I chose to follow a track of studies that was barely covered during my bachelor's. However, with the help of family, friends, and teachers (Faezeh Kardan Halvaei and Aditya Shekhar), I managed to overcome what previously felt like an insurmountable challenge. Additionally, I would also like to thank Pavol Bauer and Milos Cvetnovic for assessing my thesis, and giving valuable feedback on it.

Abheek Bhadury
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Summary

There will soon be a huge influx of EV chargers required in the coming years. Therefore it is important to find out the lifetime of EV chargers like the DC Fast Charger for business cases. These chargers are a combination of multiple power converters to help regulate the grid AC voltage to something that can be used to charge the battery. Multiple Industrial surveys have shown that the most vulnerable parts of power converters are the power semiconductors used inside them. Moreover, research shows that most of the failure in these EV chargers is due to thermal cycling which causes thermo-mechanical fatigue. While there are studies that estimate the lifetime of these semiconductors, it is seldom done in the context of EV charging load profiles. These EV charging load profiles are responsible for long-term power cycling contrary to short-term power cycling which is generally done to estimate the lifetime of the semiconductors. This thesis shall thus choose a popular DC Fast Charger power converter, feed in a load profile and analyse the effects of thermal degradation of the switches and rectifier diodes present in the circuit. This data will then be used to make an estimate of how long the whole power converter will last thus leading to the lifetime of the DC Fast Charger.

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Nomenclature

Abbreviations

Abbreviation	Definition
AC	Alternating Current
CC	Constant Current
CCM	Continuos Conduction Mode
CDF	Cumulative Distribution Function
CFM	Cubic Feet per Minute
CTE	Coefficient of Thermal Expansion
CV	Constant Voltage
DAB	Dual Active Bridge
DC	Direct Current
DCFC	Direct Current Fast Charger
EOL	End of Life
EV	Electric Vehicle
FB	Full Bridge
FEM	Finite Element Method
FWD	Free Wheeling Diode
HB	Half Bridge
IGBT	Insulated Gate Bipolar Transistor
MOSFET	Metal Oxide Semiconductor Field-Effect Transistor
PCB	Printed Circuit Boards
PDF	Probability Distribution Function
PFC	Power Factor Correction
PSFB	Phase Shifted Full Bridge
PWM	Pulse Width Modulation
RBD	Reliability Body Diagram
RMS	Root Mean Squared
SMD	Surface Mount Devices
SoC	State of Charge
V2G	Vehicle to Grid
ZCS	Zero Current Switching
ZVS	Zero Voltage Switching

Variables

Symbol	Definition	Unit
ΔI	Current ripple	[A]
ΔQ	Charge Accumulated in Capacitor	[C]
τ	Thermal time constnat	[s]
ΔV	Voltage ripple	[V]
C_{of}	Output Filter Capacitance	[F]
C_{th}	Thermal Capacitance	[J/K]
D	Duty Ratio	-
D_{max}	Maximum Duty Ratio	-
E_a	Activation Energy	[J/mol]

Symbol	Definition	Unit
E_{off}	Switch off Energy Loss	[J]
E_{on}	Switch on Energy Loss	[J]
E_{rr}	Reverse Recover Energy Loss	[J]
f_{sw}	Switching Frequency	[Hz]
I_{ce}	Collector-Emitter Current	[A]
I_F	Forward Current	[A]
I_{in}	Input Current	[A]
I_{out}	Output Current	[A]
I_{ref}	Reference Current	[A]
I_{rr}	Reverse Recovery Current	[A]
I_{RRM}	Maximum Reverse Recovery Current	[A]
I_{RMS}	Root Mean Square Current	[A]
I_{Switch}	Switch Current	[A]
k_B	Boltzman's constant	[J/K]
L_{of}	Output Filter Inductance	[H]
N_f	Number of cycles to failure	-
N_p	Number of turns on Primary Side of Transformer	-
N_s	Number of turns on Secondary Side of Transformer / Turns Ratio	-
P_{cond}	Conduction Power Losses	[W]
P_{loss}	Total Power Losses	[W]
$P_{loss,max}$	Maximum total power lost in full load cycle	[W]
P_{sw}	Switching Power Losses	[W]
R_c	IGBT Internal Resistance	[Ω]
R_D	Diode Internal Resistance	[Ω]
R_{diode}	Reliability of the Diode	-
$R_{DS,on}$	MOSFET Internal Resistance	[Ω]
R_{IGBT}	Reliability of the IGBT	-
R_{out}	Load Resistance	[Ω]
R_{par}	Reliability of components in parallel	-
R_{ser}	Reliability of components in series	-
R_{sys}	Reliability of the System	-
$R_{th(j-c)}$	Thermal Resistance Junction to Case	[K/W]
$R_{th(c-h)}$	Thermal Resistance Case to Heat Sink	[K/W]
$R_{th(h-a)}$	Thermal Resistance Heat Sink to Ambient	[K/W]
T_{amb}	Ambient Temperature	[K or degC]
T_j	Junction Temperature	[K or degC]
$T_{j,max}$	Maximum Operating Junction Temperature	[K or degC]
t_{on}	Rise time of current in switch	[s]
t_{on}	Cycling time of heat for semiconductors	[s]
t_{off}	Fall time of current in switch	[s]
t_{rr}	Reverse Recovery time of diode	[s]
T_s	Switching Time Period	[s]
U_r	Unreliability of component	-
$V_{ce(sat)}$	Saturated Collector-Emitter Voltage	[V]
V_F	Forward Voltage	[V]
V_{in}	Input Voltage	[V]
V_L	Voltage drop across inductor	[V]
V_{out}	Output Voltage	[V]
V_{ref}	Reference Voltage	[V]
$Z_{th(c-h)}$	Thermal Impedance Case to Heat Sink	[K/W]
$Z_{th(h-a)}$	Thermal Impedance Heat Sink to Ambient	[K/W]
$Z_{th(j-c)}$	Thermal Impedance Junction to Case	[K/W]

1

Introduction

The world is currently seeing a huge increase in the number of electric vehicles used by consumers. It is predicted that by 2035 the number of electric vehicles will increase to 130,000,000 units [1]. However, one of the most common concerns of consumers regarding electric vehicles is the availability of the charging infrastructure and the time it takes to charge electric vehicles. The time taken to charge an electric vehicle depends on the level of charging of the charging station which corresponds to the power rating/output of the charger. It is broadly categorised into 3 levels. Level 1 charging deals with powers up to 2.2kW. Level 2 is related to stations with an output of above 2.2kW to about 22kW. Finally, DC fast charging (level 3) deals with power levels from 50kW to 350kW.

Level 3 charging stations can charge a car within 1 or 2 hours depending on the battery capacity and power capabilities. However, to do this, the charging station requires more components. In level 1 and level 2 charging, the car is supplied with AC power. An onboard charger then converts this AC power to DC power that is compatible with the battery to charge it. This can be seen in Figure 1.1. However, with the power levels of level 3 charging, it is not feasible to integrate a sizeable onboard charger in the car. Hence, the AC-DC rectification is done in the charging station itself which leads to the name "DC-Fast Charging" as the car is directly being supplied DC power.

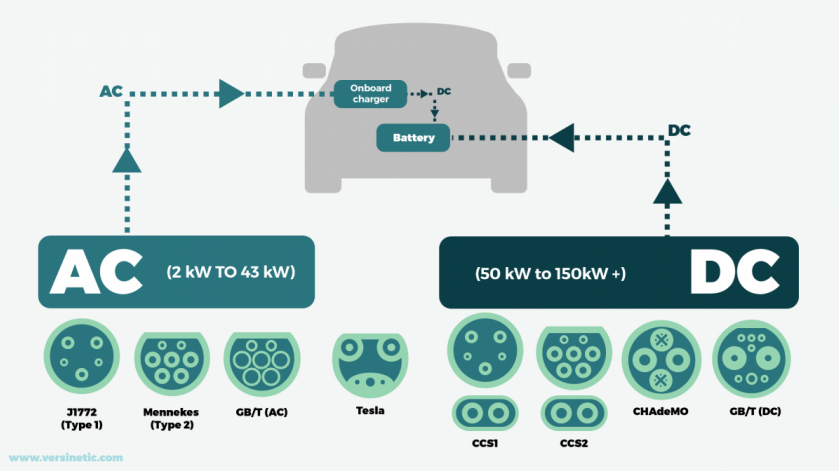


Figure 1.1: AC versus DC charging [2]

However, due to this fact, the components in the charging station also increase leading to an increase in the cost. Hence, from a business perspective, it is quite important to know the lifetime of these EV chargers to help develop a cost-benefit analysis for various operators.

1.1. Research Objective and Methodology

The objective of this thesis would thus be to explore the life expectancy of DC Fast Chargers given the thermal degradation that various semiconductors undergo in the power converters for a given charging profile. While there are a lot of papers that exist on the thermal degradation of semiconductors, research on the effects of an electric vehicle's load profile on the thermal degradation of semiconductors is relatively scarce. Thus this thesis will attempt to determine the lifetime of the semiconductor components present in DCFCs and therefore the charger as a whole when under the influence of an EV charging load profile.

To do this, first various power converter topologies will be studied that are used in the DC fast chargers. The DC-DC converter topologies are of particular interest as they are directly impacted by the load profiles of EVs. While a step down can be performed by controlling the rectification of the AC power, this is not being considered in the scope of this thesis. After studying various topologies mentioned in [3], one of them will be simulated to determine the power losses that occur system-wide and also across every individual component during the duration of the load cycle.

These power loss values can then be used to determine the junction temperature of various components. Once this is achieved, lifetime estimation models can be used to determine the damage that occurs to individual components. With the help of this data, the most critical component (with the lowest life) can be identified. A Monte Carlo study will then be performed to test the reliability of the power converter and extrapolate the results thereafter.

1.2. Research Questions

The main question this thesis shall aim to answer is **how many years can a power converter in a DCFC last before failure**?
Based on this question, few sub-questions can be formulated whose answers may be required to reach this final objective.

- **Question 1** - What kind of power converter topologies are used in the DC Fast Chargers and how do they differ?
- **Question 2** - How to simulate a power converter which can meet the requirements of the EV charger and verify the working of such a model?
- **Question 3** - What are the power losses that are occurring in the semiconductor devices in the power converter? Are they uniform?
- **Question 4** - How to model the thermal network of a power module and how this thermal network affects the junction temperature?
- **Question 5** - How does the junction temperature affect the cycles to failure and the damage occurring to the device?
- **Question 6** - Which semiconductor device is the most vulnerable and how does it limit the lifetime of the converter?

1.3. Thesis Outline

This thesis will follow the following outline after this chapter. In Chapter 2, a literature survey has been done. It reviews the concepts researched to create a methodology and perform this thesis project. Chapter 3 talks about the research method used in this thesis and also finalizes the design of the model. In Chapter 4, the findings of the base case, or the results of the IGBTs are discussed along with the validation of the model. Chapter 5 then moves on to discussing the losses, junction temperatures and the lifetimes of the diode. Then Chapter 6 determines the overall lifetime of the converter. Once that is done, the same chapter further explores the results of switching the existing diode with ones with lower voltage and current ratings. Chapter 7 presents a brief conclusion, the answers to the sub-questions asked above and even future recommendations on research in this topic.

2

Literature Review

This chapter shall detail the literature survey conducted before this project was initiated. Section 2.1 will give an introduction about the topic and the motivation for the research being conducted. After that, Section 2.2 will discuss the types of power converters that are used in the DC Fast Chargers. Section 2.3 will then illustrate how the power losses can be calculated for various components used inside the power converters. Using these power losses, Section 2.4 will go over how the thermal network can be drawn for any component and how the junction temperature can then be determined. Section 2.5 talks about the various lifetime models that currently exist for semiconductors and their advantages/limitations. In Section 2.6 different methods of reliability estimation can be seen. Finally, the chapter will be concluded by discussing the research gaps identified and the aim thus derived in sections 2.7 and 2.8 respectively.

2.1. Background

As declared by the European Commission, gasoline passenger cars and vans will slowly be phased out by 2035. This will be done in two steps. In the first step, the emissions limits will be reduced by 55% by 2030 for all passenger cars and vans. This includes luxury car brands like Ferrari and Lamborghini. Essentially, it provides them with a buffer time to prepare for EVs. After this, by 2035, all the cars and vans sold need to be zero-emission vehicles [4].

At the current growth of electric vehicles, which is about 65% every year, there would be around 130 million EVs on the roads by 2035. This raises concerns on the consumer side because some of their most common doubts regarding EVs are related to range anxiety and charging infrastructure. Reuters estimates it is going to take about 65 million chargers to power these cars. 56 million of these will be residential chargers while the other 9 million will be public chargers such as destination chargers or highway chargers [1].

Even with the presence of chargers, another concern of consumers is the speed of charging. Conventional gasoline or diesel vehicles can get a full tank in a matter of minutes. On the other hand, the charging speed of an EV depends vastly on the type of charger used. Level 1 chargers can charge the car in 40-50 hours depending on the battery capacity. The same car may take 4-10 hours using a level 2 charger which is normally available in public spaces. On the other hand, Level 3 chargers can charge a car in 20 minutes to an hour [5]. While this charging speed is relatively slower than conventional gasoline cars, it is a significant improvement over the previous two technologies.

This speed of charging is made possible in level 3 chargers as the charging station directly supplies high-powered DC voltage to the battery of the car. A schematic of both DC fast chargers and level 1/2 chargers is shown in Figure 1.1. Since the power supplied by the grid is in AC, it is important to convert this power to the first DC type and then drop down its voltage to one that matches the battery's voltage. To do this, every EV charger has 2 main components - an AC-DC rectifier and a DC-DC converter. Figure 2.1 shows a flow chart of the difference in architecture for DC fast charging and AC charging for EVs. The EVSE shown in the diagram stands for Electric Vehicle Supply Equipment. It is essentially a control mechanism to help charge the battery to the correct output levels. In AC chargers (Level 1

and Level 2 chargers), the function of rectification and conversion is performed by the onboard charger. However, due to the high-power levels of level 3 chargers, the packaging for such converters is harder and cannot be fitted onboard a car easily. Thus, DC fast chargers use an off-board rectifier and a DC-DC converter to step down the voltage as required.

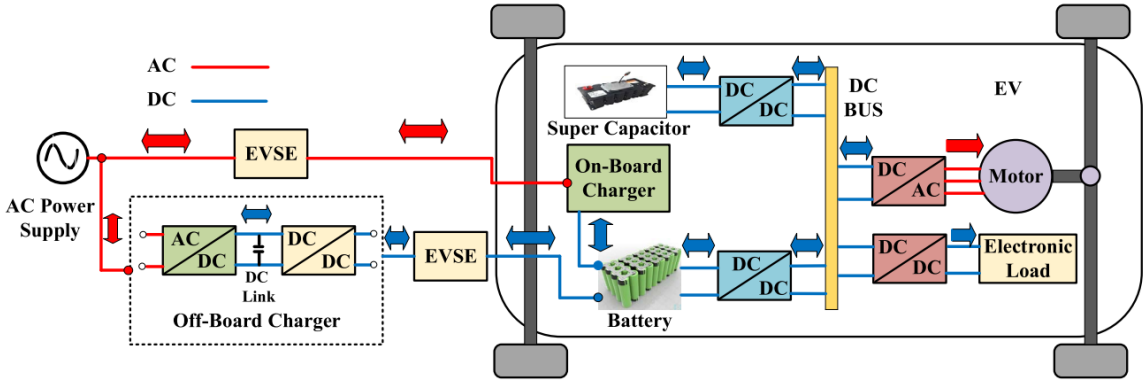


Figure 2.1: Charging Flowchart for EVs [3]

Due to these high voltage and current requirements, high power rating transistors and diodes have to be used in the power converters. This raises the cost of an EV charger. For context, the cost of a Level 2 charger is around $3000, but the cost of DC Fast charger ranges anywhere from $28,000 to $140,000 depending on the power capacity of the station [6]. Now, one of the main failure modes inside any electrical or electronic system is the power converters present inside them [7]. Thus, from a business point of view, it is extremely important to determine the lifetime of these chargers and the converters present inside them. It would help determine important cost-benefit analyses for setting up and installing charging stations.

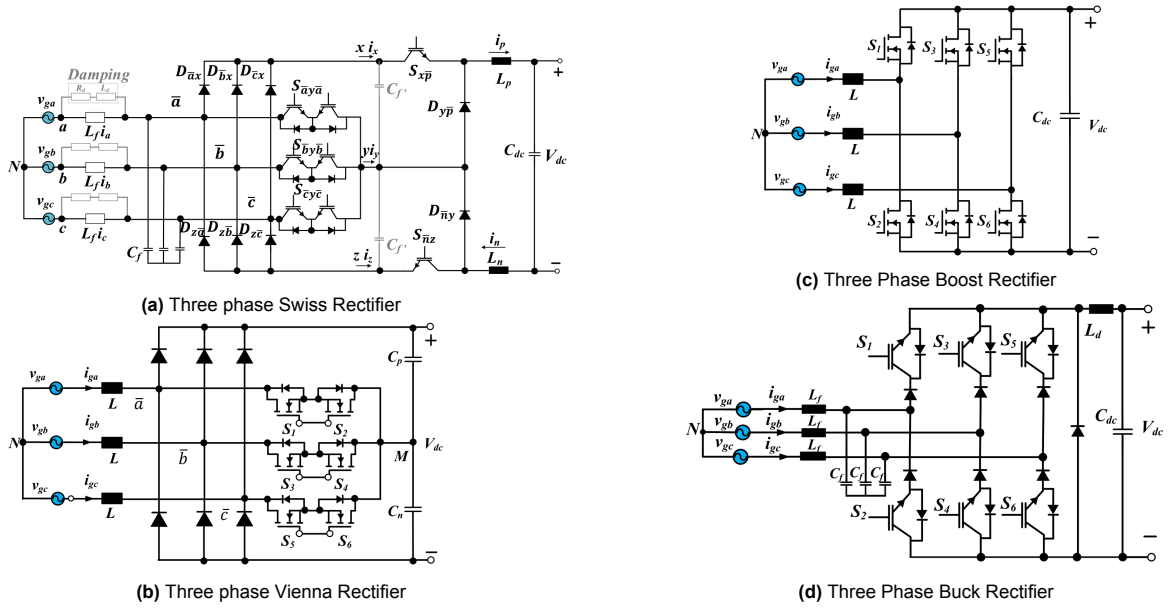
2.2. Power Converters Used in DC Fast Chargers

As mentioned above, DC Fast chargers have two stages of converters inside them. The first one is an AC-DC rectifier which converts the power from the supply lines to DC voltage. The second stage is a DC-DC converter which changes the voltage and current of the output as required by the car battery. The review paper by Safayatullah et al. gives a good overview of various topologies used for both the AC-DC and DC-DC converters [3].

2.2.1. Introduction to types of Power Converters

For AC-DC rectifiers, there are multiple topologies possible. The most common ones used are Vienna and Swiss Rectifiers and their various modifications. However, simpler circuits like the Three-Phase Buck and Three-Phase Boost Rectifiers can also be used. The main advantage of the Vienna rectifiers is that these topologies can also be optimised to be bi-directional for use cases such as V2G charging applications. On the other hand, the three-phase buck and boost rectifier provide an additional advantage of regulating the voltage after rectification [3]. This can be done by using active switches or thyristors on the rectification side instead of diodes. By controlling the switch timings, the output voltage pulse can be changed and thus reduced or increased depending on the rectifier topology. This can help mitigate the voltage and current stresses on the DC-DC converter that is placed after it in the charging process. Some of these topologies can be seen in Figure 2.2.

After the AC-DC rectification is done, then the voltage might need to be stepped down further to match the voltage of the battery. This is done with the help of DC-DC converters and these converters shall be the primary focus of this thesis. The DC-DC converter topologies mentioned in the paper [3] can be broadly categorised as isolated or non-isolated converters. This refers to the presence of galvanic isola-



(a) Three phase Swiss Rectifier

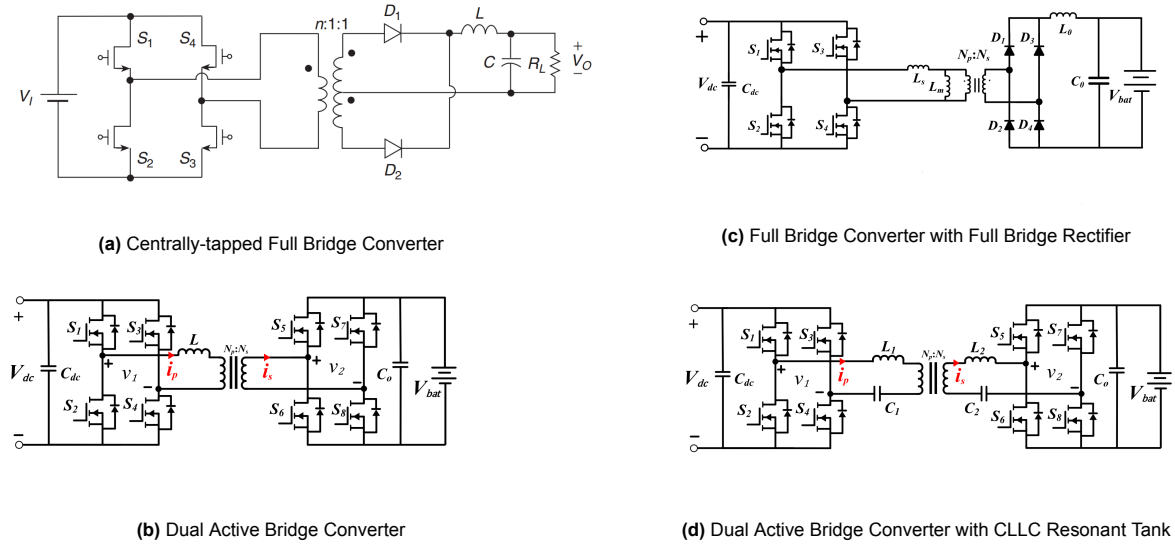
(c) Three Phase Boost Rectifier

(b) Three phase Vienna Rectifier

(d) Three Phase Buck Rectifier

Figure 2.2: AC-DC Rectifier Topologies used in DC Fast Chargers [3]

tion within the circuit. Galvanic isolation is provided for safety purposes. While research is going on for non-isolated converters (also mentioned in this review paper), isolated converters are more popular due to their inherent safety characteristics. Among the isolated converters, there are two topologies that are widely used. They are the Dual Active Bridge (DAB) Converter or the Full Bridge (FB) Converter. There are multiple variations and optimisations of these that exist. Most commonly the variations include a resonant tank or other passive and active components that help improve the efficiency of the circuit. Some of the popular topologies can be seen in Figure 2.3. These converted have been discussed in detail below in Section 2.2.3



(a) Centrally-tapped Full Bridge Converter

(c) Full Bridge Converter with Full Bridge Rectifier

(b) Dual Active Bridge Converter

(d) Dual Active Bridge Converter with CLLC Resonant Tank

Figure 2.3: DC-DC Converter Topologies used in DC Fast Chargers [3][8]

2.2.2. Soft Switching vs. Hard Switching

Before discussing the functioning of these two types of circuits, it is important to understand the difference between soft and hard switching. They refer to the behaviour of a switch's voltage and current

during their turn-on and turn-off times. Hard switching relies on the device's own ability, while soft switching relies on the control logic used for the circuit.

(a) Hard Switching **(b)** Soft Switching

Figure 2.4: Switching Techniques used in Converters [9]

When a switch is sent the signal to turn on, it does not happen instantly unless it is an ideal switch. This happens due to the parasitic capacitances present inside a switch. The blocking voltage takes some time to drop to zero and the drain (or collector-emitter) current takes some time to reach the steady state values. During this interval, the switch is not conducting fully and thus the power transmitted during this period contributes to switching losses. This can be seen in Figure 2.4a . However, if these periods of waveforms were to have some form of lag or phase difference between them, the losses can be reduced. This is the principle followed in Soft Switching. Here inductors and capacitors (collectively known as resonant tanks) are used to delay the switching on/off of the switches to minimize the losses of the circuit. Even in soft switching, there are two techniques that are prevalent. These are Zero Voltage Switching (ZVS) and Zero Current Switching (ZCS). In ZVS, as the name suggests, the blocking voltage is allowed to reach zero before the current passes through the switch. In ZCS, the opposite happens, where the current value is allowed to drop to zero before the blocking voltage rises again. This can be seen in Figure 2.4b. In practice, ZVS is used more than ZCS as the implementation is easier. However, ideally, both should be implemented to minimize switching losses. Switching losses occur for every switching period and thus depend on the switching frequency. Therefore, for higher power or high switching frequency applications, soft switching is preferred [9]

2.2.3. DC-DC Converters in Detail

With the information shared above, two common DC-DC converters can be studied further - the Full Bridge (FB) Converter and the DAB Converter. The DAB has bidirectional capability and inherent soft switching capabilities. However, it also has a higher cost, along with lower power density and more complex control algorithms. The FB converter on the other hand is known for its simple control, high power density and low EMI. But, they also do not support bidirectional power flow and often have hard-switching on the secondary side [3].

The Full-Bridge converter has a full H bridge on the primary side and a half or full-bridge rectifier on the secondary side of the converter. The primary and secondary sides are separated from each other by means of galvanic isolation or a transformer between them. This transformer can help the converter either step-up or step-down the voltage according to requirements. Further, the power transfer in the FB converter can be controlled in two common ways. The first method involves introducing a phase difference between the two switches of the same active leg. This type of converter is called a Phase Shifted Full Bridge (PSFB) Converter. All the switches operate on the same duty cycle with a dead time introduced between the two legs. This dead time is essential to help prevent transformation saturation and discharge the parasitic capacitances. The amount of phase delay controls the amount of power that can be transferred from the primary to the secondary side of the converter. The gate signals for such a type of converter can be found in Figure 2.5a. The phase difference is highlighted in purple. Since power is not transmitted during this period, this period is often called the loss of duty cycle or D_{loss}. To aid in this, there exists an inductor on the primary side that helps the current keep going during dead times and discharges the capacitances. It also helps in ZVS operation which reduces the switching losses in the converter.

The second method controls the output voltage by just varying the duty cycle of the switches. When the transformation turns ratio is known, the duty cycle can easily be calculated based on the input and output and voltage requirements as seen in Section 3.3. The gate signals of this type of modulation can be seen in Figure 2.5b. This method of switching is far simpler than the PSFB converter. The transformer waveforms as a result of this switching strategy can be seen in Figure 4.6. However, due to the hard switching of the IGBTs/MOSFETs, there are higher power losses compared to the phase-shifted control. The switch layout for both the phase-shifted modulation and the simple PWM modulation can be seen in Figure 2.3c

(a) DC-DC Phase Shifted Full Bridge Converter

(b) DC-DC PWM - Full Bridge Converter [8]

Figure 2.5: Full Bridge Converter Gate Signal Waveforms

On the other hand, the DAB converters consist of two active H bridges on both sides of the transformer. Thus, this converter has a total of 8 switches in the simplest configuration. Similar to the FB converter, the transformer can be used to either step up or step down the voltage depending on the requirement. Like the PSFB converter, the DAB converter also works on a phase-shifted control. However, the phase shift is introduced between the primary and the secondary side of the transformer. The two switches of the same active leg are switched on in sync. This can be seen in Figure 2.6, which represents the gate signals for a circuit as shown in Figure 2.3b. The orange highlighted portion is the phase shift introduced between the primary and the secondary parts of the circuit.

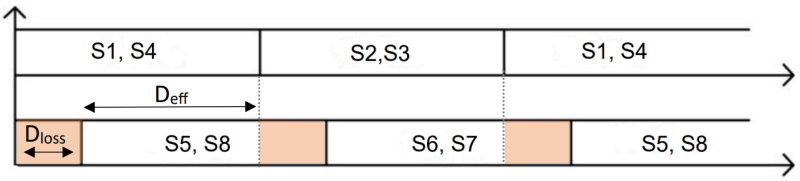


Figure 2.6: DAB Gate Input Signals [10]

There are several variations that exist for both these converters in terms of hardware and control techniques as well. For example, one of the common variations of the PSFB converter is to control the switching in ZVS or ZCS range. This can reduce the switching losses of the switch and consequentially improve the efficiency of the converter. For this purpose, the inductors towards the transformer need to be adequately sized. Another option is to run the PSFB converter with a half-bridge rectifier on the secondary side with a centrally tapped transformer [11]. Finally, another modulation technique used for the PSFB converter implements changing the duty cycle of the second switch in the active leg rather than phase shifting it. This is known as trailing edge modulation or rising edge modulation depending on the turn-on and turn-off times of the switch. This type of configuration can help reduce the losses as well since the semiconductor is switched on for a lower duration of time.

For the DAB converter, there are various versions that exist based on modulation techniques. The simple version relies on a single-phase shift modulation technique. This means the secondary side of the transformer is phase shifted compared to the primary side. However, there are other modulation techniques such as dual or triple-phase shifting. In dual-phase shift, an additional phase shift is imple-

mented between the working of the active legs in the H bridge converter, essentially reducing the duty cycle [12]. In the triple phase shift, not only is there this duty cycle reduction but also a phase shift is introduced between the two switches of the same active leg [13]. Such multiple-phase modulation techniques enable a multi-step conversion process. Moreover, they also help in increasing efficiency over a wider load range while preventing transformer saturation.

Therefore, both varieties of isolated converters show great promise to be used for this scope. A final comparison has been made in Section 3.1.

2.3. Power Losses

The sources of power losses in a power converter can be the transformer, switches, diodes, inductors, capacitors, and resistors. However, the failure points are primarily the switches and the diodes [14] [15] [16] [17]. Thus, the focus of power losses in this thesis shall be the switches and the diodes.

2.3.1. Switches (IGBTs or MOSFETs)

The most common type of switches used in power converters are either MOSFETs or IGBTs. Each has its own advantages and disadvantages. In switches, there are multiple sources of power losses that occur. These are -

- Conduction losses
- Switching losses
- Gate losses

In addition to these losses, there are additional losses that are related to the presence of the body diode. Moreover, the share of these losses depends on the application of switches. In the case of power converters, the MOSFETS and IGBTs are used as switches. During switching applications with a constant current output, the conduction and the switching losses are primarily much greater than the gate driver losses. Moreover, the gate driver losses depend a lot on the type of gate driver chosen for controlling the switches. Thus, in the scope of this thesis, only the switching and the conduction losses will be focused on.

Switching Losses

The switching losses in a switch are a result of the inherent parasitic capacitances present inside it. Due to this, there is a delay in the time it takes for the switch to completely switch on, and allow the current through completely while also maintaining zero voltage drop across its terminals. During this delay, since the required amount of power is not being transmitted across the terminals, the power is lost for this duration. A representation of this can be found in Figure 2.7. The time delay depends on several factors including the gate voltage and current. The leakage inductance of the transformer also plays a role. The power lost during this period is thus a function of the instantaneous voltage and current across the switch during these switching delays. An integral over this time period can give the energy lost while switching the device on or off for a cycle. Thus, to calculate the power lost in a second, it has to be multiplied by the switching frequency [18] [19]. Hence, the switching losses increase as the switching frequency increases. This can be seen in (2.1).

$$P_{sw} = (E_{on} + E_{off}).f_{sw} \tag{2.1}$$

Here P_{sw} are the switching losses (W)
E_{on} is the switching energy loss during switch turn-on (J)
E_{off} is the switching energy loss during switch turn-off (J)
f_{sw} is the switching frequency of the switches (Hz)

The variables E_{on} and E_{off} are available in the datasheet of a switch. However, the values listed are those measured for a particular current and voltage. A rough estimate can be made by scaling the voltage and current [20]. (2.2) illustrates this method. It is important to note that this equation only

takes into account the reference voltage and not the reference temperature that was used to measure these readings. To take the temperature into account as well, the equation will need to be modified further as shown in [20].

$$P_{sw} = (E_{on} + E_{off}).f_{sw}.\frac{V}{V_{ref}}.\frac{I}{I_{ref}} \tag{2.2}$$

Here V_{ref} is the reference voltage at which the switching losses were measured in the datasheet (V)
V is the blocking voltage at which the switching losses need to be measured (V)
I_{ref} is the reference current at which the switching losses were measured in the datasheet (A)
I is the current through the switch at which the switching losses need to be measured (A)

Conduction Losses
Conduction losses in a switch are the result of internal resistances. Another way to determine this is to calculate the product of the voltage across the switch depending on the current flowing through the switch and add the ohmic losses to this [18] [19]. This can be seen in (2.3). In switches, the voltage drop across the switch is determined by the amount of current flowing through it. Manufacturers thus give tabulated data about the voltage drop at different temperatures and different values of current. This provides a more accurate way to calculate the power losses across the switch. Since these losses do not depend on the switching frequency, they stay constant even as the switching frequency is changed.

$$P_{cond} = V_{ce}.I_{ce,avg} + I^2_{ce,rms}.R_c \tag{2.3}$$

Here P_{cond} are the conduction losses measured in Watts (W)
V_{ce} is the forward voltage drop measured in Volts (V)
$I_{ce,avg}$ is the average forward current or the current through the switch (A)
$I_{ce,rms}$ is the RMS current through the switch (A)
R_c is the on-time resistance of the switch (Ω)

It is important to note that the conduction losses in the case of MOSFETs, are not the same as that of the IGBTS. In this case, only the ohmic losses exist. Therefore, (2.3) changes for the MOSFETs into (2.4).

$$P_{cond} = I^2_d.R_{DS,on} \tag{2.4}$$

Where $R_{DS,on}$ is the drain to source on-time resistance of the MOSFET (Ω)
I_d is the drain current through the MOSFET

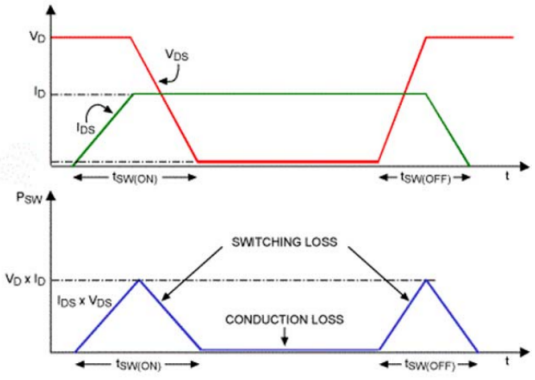


Figure 2.7: Losses in a Switch [21]

2.3.2. Diodes

Diodes experience losses similar to switches. There are generally two types of diodes that can be found in a power converter circuit. The first one is the Body Diode which helps in continuing a freewheeling action of current in the circuit to dissipate the energy stored in the inductor and reduce transformer saturation. The second type of diodes generally found (mostly in the case of DC-DC FB converters) are the rectifier diodes. These diodes are used to rectify the current back to DC after it has passed through the transformer. The rectifier diodes will be the focus of the investigation. There are two main types of losses in diodes -

- Conduction Losses
- Reverse Recovery (Switching Losses)

Conduction Losses

The conduction losses in a diode are similar to that of switches. They are also calculated as products of voltage and current passing through the diode with the addition of the ohmic losses [22]. These voltage values are also tabulated and stated by the manufacturer at different temperatures and currents in their PLECS models. The datasheets on the other hand, generally just have a single value of the forward voltage. This value is denoted for some standard testing conditions and thus cannot be used everywhere. Alternatively, a scaling law like the one used in (2.2) can be used. (2.5) shows the relationship between the diode conduction losses and the current passing through them. A graphical representation of these losses can also be seen in Figure 2.8.

$$P_{cond} = V_F.I_{F,avg} + I^2_{F,rms}.R_d \tag{2.5}$$

Here P_{cond} are the conduction losses measured in Watts (W)
V_f is the forward voltage drop measured in Volts (V)
$I_{F,avg}$ is the average forward current or the current through the diode (A)
$I_{F,rms}$ is the RMS current through the diode (A)
R_d is the on-time resistance of the diode (Ω)

Reverse Recovery Losses

The reverse recovery losses in a diode are similar to the switching losses of switches. However, unlike them, there are no turn-on losses considered. There are only turn-off losses when the diode has to switch from conducting to blocking function. In reality, there are very slight turn-on losses that are negligible and thus usually ignored. During this switching, the current does not immediately stop flowing. Instead, it flows in the reverse direction for some time to get rid of the residual charges. This leads to a peak reverse current following which the current slowly goes back to 0. The time duration it takes for this to happen is known as the reverse recovery time. The amount of power lost during this period is known as the reverse recovery loss. Like the switching loss, it is calculated as the product of current and voltage during this period. (2.6) shows one of the ways to determine these losses [23]. Figure 2.8 illustrates the switching losses along with the peak reverse recovery current.

$$P_{sw} = \frac{1}{2} t_{rr}.I_{RRM}.V_R.f_{sw} \tag{2.6}$$

Here P_{sw} is the reverse recovery losses (or switching losses) measured in Watts (W)
I_{RRM} is the peak reverse recovery current mentioned in datasheet (A)
V_R is the reverse or blocking voltage of the diode (V)

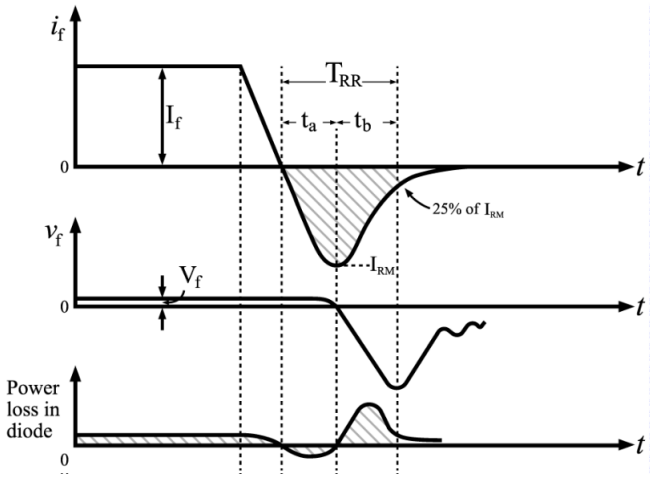


Figure 2.8: Losses in a Diode [24]

2.4. Thermal Network and Junction Temperature

As the focus of this thesis is to investigate the thermal degradation of a power converter under the loading of an electric vehicle load profile, modelling the thermal network accurately is very important. Thermal networks are crucial to be modelled correctly as they affect the junction temperature of the semiconductors which in turn affect the power losses of the semiconductor continuing the loop. With respect to the power converter, there are two networks that need to be considered. First, the internal thermal network of the junction and secondly the exterior thermal network of the module.

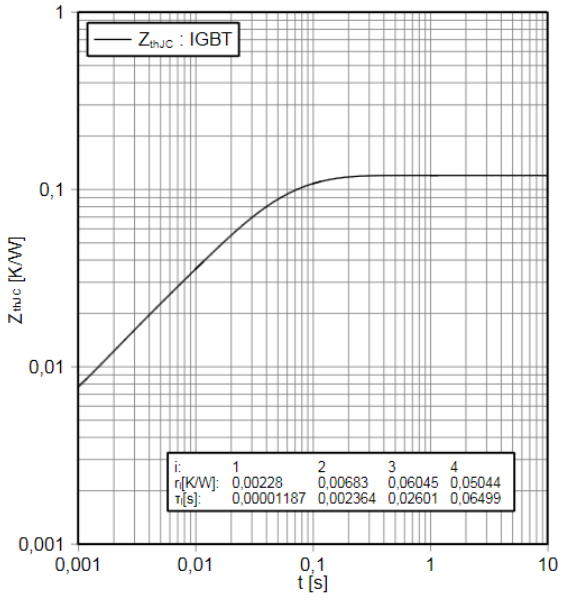


Figure 2.9: Internal Thermal Impedance Graph of IGBT Module [25]

The internal thermal network can be obtained easily by looking at the datasheet of any MOSFET, IGBT or diode. There are graphs given to show how the thermal impedance of the junction varies with respect to time as seen in Figure 2.9. Additionally, there is a table given of thermal resistances and time constants. The thermal time constant is defined as the time taken for the system to reach 69% of the final steady-state temperature once the power transmitted is changed. Generally it takes 4-5 thermal time constants to reach a steady state from this point. Mathematically, it is the product of thermal capacitance and thermal resistance at that point as can be seen in (2.7).

$$\tau_{th} = R_{th} * C_{th} \tag{2.7}$$

Here τ_{th} is the thermal time constant (s)
R_{th} is the thermal resistance (K/W)
C_{th} is the thermal capacitance (J/K)

The external thermal network then needs to be modelled according to how the module is connected to the circuit board and thereafter the heat sink. Figure 2.10 below gives a rough overview of how these switches are mounted onto the power converter and heat sinks. The casing is highlighted by the dark black outline. However, in most cases, the baseplate is considered to be a part of the casing. The thermal resistance for the junction to the casing is generally provided in the data sheet. Thus, it can be considered that all the layers including the base plate are considered in determining the thermal resistance up to that point. The thermal capacitance or time constant for this is generally not included in the data sheets. This is primarily because thermal capacitances are a function of the material properties (its specific heat capacity) and the mass of the layer. In the case of these power modules, the mass of the materials is so low that the resultant capacitances are often negligible. Nevertheless, the capacitance or the time constant affects the dynamics of the system and thus is important to be considered where provided like the graph of internal thermal impedance. Thus, the thermal components that need to be modelled are just the thermal grease and heat sink.

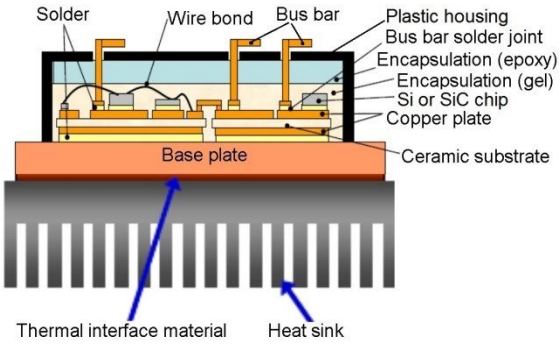
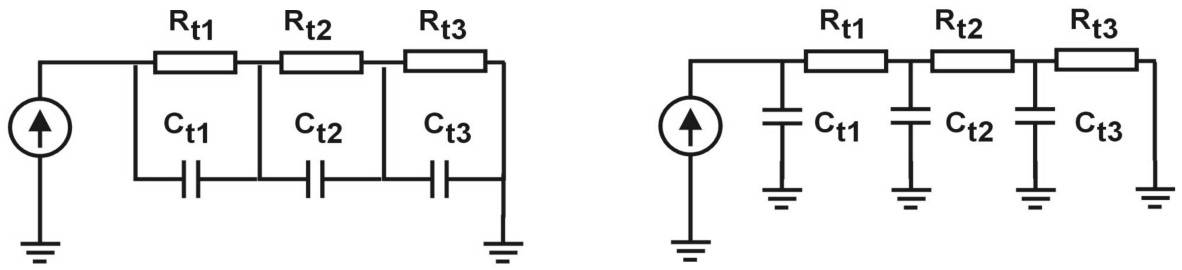


Figure 2.10: Cross section of a Power Module [26]

There are multiple ways of modelling these layers. Some of the common ones are the Foster and the Cauer Thermal Networks. The Foster network considers a ladder structure for the thermal resistances and capacitances as seen in Figure 2.11a. This also leads to the model working on the parameters of thermal time constants (τ_{th})and resistances (R_{th}) where the thermal time constant can be derived from (2.7). Cauer network on the other hand uses thermal resistances (R_{th}) and capacitances (C_{th}) as seen in Figure 2.11b. The capacitances in the Cauer network are all grounded individually. They can be used interchangeably based on the data available at hand. While Foster network has no physical significance, it is easy to derive it empirically through experiments. [27].



(a) Foster Network

(b) Cauer Network

Figure 2.11: Thermal Networks used for semiconductors [28]

The total thermal impedance of such a network is given by (2.8) [29]. Thus, looking at the data sheets, and the material properties, the total thermal impedance of any Foster or Cauer Network can be calculated using (2.7) and (2.8). This total thermal impedance can then be used to calculate the junction temperature of the component.

$$Z_{th}(t) = \sum_{i=1}^{n} R_i(1 - e^{\frac{-t}{\tau_i}}) \tag{2.8}$$

Here Z_{th} is the thermal impedance (K/W)
R_i is the thermal resistance of the i-th element (K/W)
t is the total time elapsed (s)
τ_i is the time constant of the i-th element (s)
n is the number of elements present in the thermal network

To calculate the junction temperature, the power losses occurring at the component will be required along with the total time-varying thermal impedance. It should be noted that (2.8) follows a graph as seen in Figure 2.9. Thus, as time goes on, the system reaches a steady state. At this point, the exponential term present in the thermal impedance (that depends on the elapsed time) tends to zero due to the very high negative exponent. Thereafter, the impedance of the thermal network no longer depends on time or even the thermal capacitance present in the circuit for that matter. Therefore, just the thermal resistances in the network can be used to calculate the junction temperature of the component. This can be done by following (2.9) [29].

$$T_j = P_{loss}.Z_{th} + T_{amb} \tag{2.9}$$

Here P_{loss} is the total power losses of the component measured in Watts (W)
Z_{th} is the total thermal impedance of the thermal network (K/W)
T_{amb} is the ambient temperature (K)
T_j is the junction temperature of the component (K)

In the equation shown above, it is good to note that the thermal impedance mentioned is the combined one of the heat sink, the thermal grease/paste, and the internal thermal network of the component. This equation will change slightly depending on how the thermal network is designed. This will be covered in detail in sections 4.4.2 and 5.2.2.

2.5. Lifetime estimation

Lifetime estimation is an important process in the development of any product. It helps understand how long a particular product will last or when it will fail. Thus, it is a very important tool in terms of financial decisions as often the capital cost of a product is amortised over the span of its lifetime. As mentioned in Section 2.1, with the requirement of several new chargers by 2050, it is becoming increasingly important to know the lifetime of chargers.

2.5.1. Background

There are typically two times of vulnerability in the life cycle of the product. These are the early stages of the lifecycle and the end stages. This can be seen depicted in the bathtub curve of products (see Figure 2.12). The early-stage failures occur mainly due to the manufacturing defects of various components, or their assembly. This period is generally known as the Infant Mortality section of the graph. On the other hand, late-stage failures generally occur due to wear and fatigue. The final lifetime of the component thus depends on the design of the product and the selection of the components within it (their ratings). The part in the middle is known as the random failure region as the reasons for failure in this region for the device are unknown. Generally, it is caused by external stress factors. For example, if the device was used in an operating temperature way beyond its limits or if the rate voltage/current was exceeded due to a short [30]. This thesis will be focusing on the wear-out region of the bathtub curve as it wants to predict the end of life of the power converters inside DC Fast Chargers.

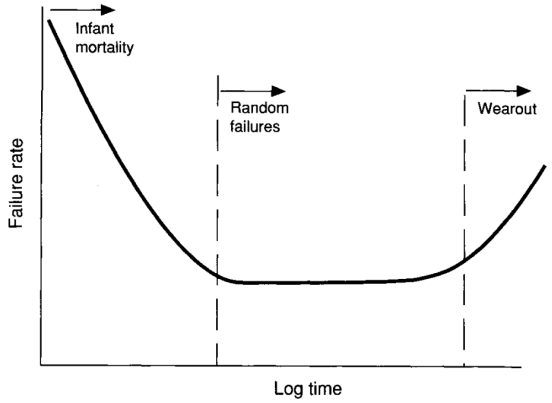


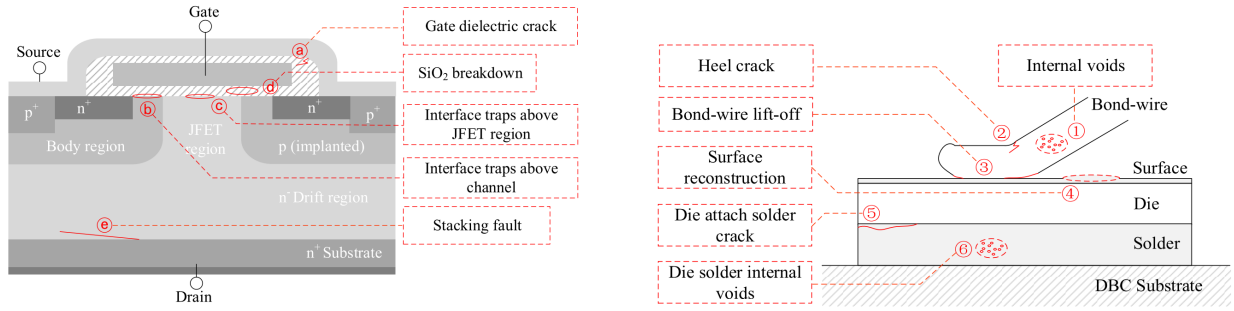
Figure 2.12: Bathtub Curve for Reliability [30]

However, power converters have several components used inside of them. It is important to narrow down the field of study to truly identify the vulnerable components and then focus on them. A paper by Wang et al. shows that the most common failures in these components are the capacitors, semiconductors and the PCBs [14]. Other industry surveys such as that of Yang et al. show that the number one cause of failures in power converters is due to the fragility of IGBTs, MOSFETs, and diodes used in them [15]. Similarly, in PV Grid connected systems, the transistors and diodes were responsible for more than 90% of the failures that occurred within the power converter in another study [16]. Even in PFC systems, it was found that the switches, the diodes and the capacitors are responsible for higher failure rates in the power converters [31]. In [17], a push-pull converter was tested for PV systems where the majority of failures came from the diodes used in the circuit followed by the MOSFETs. From these studies, it can be concluded that some of the most vulnerable components in power converters are the semiconductors - the switches and diodes used in the circuit. Thus, this thesis shall focus on these devices in determining the lifetime of the power converters and thus the EV Fast Charger.

As discussed previously, failure in various products can occur due to a variety of reasons. In the case of electronics, it can be mechanical or thermal stresses, short circuits due to moisture/corrosion, other contaminants, or even shocks/vibration. The same survey conducted by Wang et al. shows that the number one reason for electronic components' failure was cyclical and steady-state thermal stresses [14]. The idea of thermal cycling causing damage to a part is due to the cyclic thermal expansion and contraction causing mechanical stress on the components. This occurs as there are several layers of various materials used in the power module each with their own separate CTE (Coefficients of Thermal Expansion). Due to this difference in CTEs, some of the layers tend to expand more than others causing mechanical stresses in the system. These mechanical stresses can lead to multiple failure modes in the semiconductor. Some of these are -

- Heel Crack
- Bond Wire Lift Off
- Die attach solder crack
- Die solder internal voids
- Surface reconstruction

This can be seen below in Figure 2.13.



(a) Chip level **(b)** Package level

Figure 2.13: Failures modes inside MOSFETS [32]

2.5.2. Empirical Models

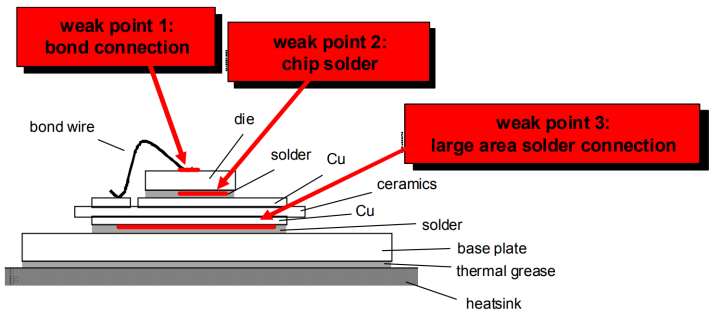


Figure 2.14: Prominent Failure Modes in IGBTs [33]

The simplest empirical model to exist is called the Coffin-Manson Model. This model is based on the fact that solely the temperature swing (ΔT_j) is the only factor influencing the lifetime of the power module. The Coffin Mason law is noted down in (2.10). In this equation α and n are constants that depend on the type of power module being used [34].

$$N_f = a\Delta T^{-n} \tag{2.10}$$

Here N_f is the number of cycles to failure
ΔT is the temperature swing (K)
a and n are empirical parameters that are based on module design

However, numerous power cycling tests revealed that there were more factors that affected the lifetime of the module other than the temperature swing. This led to the creation of the LESIT model in the 1990s [35] . It assumes that the main failure mode is that of the bond wire lift-off. This model is applicable to modules with an Aluminium Oxide substrate and a copper base plate. The mean junction temperature was thus added to the equation along with the temperature swing. The number of cycles to failure using this module could now be calculated using (2.11).

$$N_f = a\Delta T_j^{-n} e^{\left(\frac{E_a}{k_B T_{j,m}}\right)} \tag{2.11}$$

Here a and n are model parameters that are determined experimentally
k_B is the Boltzmann constant (J/K)
E_a is the activation energy required (eV)
ΔT_j is the junction temperature swing (K)
$T_{j,m}$ is the mean junction temperature (K)

However, when power cycling was done to other power modules under high voltages, there were two different failure modes that were observed. One was bond wire lift-off which was already considered in

the LESIT model. However, the base plate solder fatigue seemed to accelerate the fatigue. The factor that affected this the most was the on-time of the thermal cycle (t_{on}). Figure 2.14 shows the vulnerable parts detected in the cross-section of a power module. Thus, Bayerer et. al proposed a new model that has been defined in (2.12). In literature, this relationship has come to be known as the CIPS2008 model [36]. This particular model was more robust as it took into consideration the bond wire diameter (D), chip thickness, and the current allowed per bond wire (I). As one can see there is no variable related to the Chip Thickness. However, the blocking voltage or voltage class (V) is directly related to the chip thickness. Moreover, this data is more easily available in datasheets compared to the chip thickness. Thus, this model shows how the geometry of the module affects life. (2.12) can be used to thus determine life.

$$N_f = A\Delta T_j^{\beta_1} t_{on}^{\beta_3} I^{\beta_4} V^{\beta_5} D^{\beta_6} e^{\left(\frac{\beta_2}{T_{jmin}}\right)} \tag{2.12}$$

Here t_{on} is the on time of the power cycle during which the power was supplied to the system (s)
I is the maximum current allowed per Bond Wire Stitch (A)
V is the Voltage class of the chip or the blocking voltage (V/100)
D is the bond wire diameter (μm)
β_1, β_2 β_3... β_6 are fitting constants used based on experimental data
A is the Coffin Manson Term
$T_{j,min}$ is the minimum junction temperature throughout the load cycling process (K)

As Figure 2.14 shows, solders are one of the weakest links in the power module. Therefore Semikron engineers created a power module that was sodler free to try and improve the lifetime. However, the CIPS model was based on the theory that solder fatigue was one of the contributing factors to the power module failure. Therefore, a new lifetime model called the SKiM63 was developed in [37]. This model is specifically meant for solder-free modules, but it was based on the LESIT model with some variations. This model took into consideration various other factors that could affect the failure rate of devices including the aspect ratio of bond wires (ar) and a derating factor for freewheeling diodes (f_{diode}). The equation was thus modified into (2.13).

$$N_f = A\Delta T_j^{\alpha} ar^{\beta_1 T_j + \beta_0} \left(\frac{C + t_{on}^{\gamma}}{C+1}\right) e^{\left(\frac{E_a}{k_B T_{jm}}\right)} f_{Diode} \tag{2.13}$$

Here ar is aspect ratio of the bondwire
f_{diode} is diode derating factor
β_0 and β_1 are fitting constants
C is a time coefficient
γ is a time exponent factor
T_{jm} is the medium junction temperature (K)

As one of the primary failure modes for diodes is also bond-wire liftoffs, the same models can thus be applied to the diodes to calculate their junction temperatures as well. This is especially valid for free-wheeling diodes [38].

2.5.3. Physics-Based Models

The lifetime models described in previous sections are empirical models which were derived by conducting several experiments on different power modules to failure and monitoring different physical parameters for each of them. Fitting constants were then added so graphs resembled real-life data as well. However, there also exist some physics-based models that can help determine the lifetime of semiconductors too. A paper by Kovacevic et. al reviews some of them in detail [34].

First, the model developed in ETH Zurich, known as the ETHZ-PES lifetime model will be discussed. The primary failure mode considered in this model is Solder Fatigue. Thus, the main assumption used to derive this relation is that the strain occurring inside the solder as a result of thermal cycling follows a hysteresis loop. The number of cycles to failure thus follows Morrow's law of Fatigue as stated in (2.14). However, it was noted that this was valid only for solder joints used in Surface Mount Devices

(SMDs). But, in the case of power modules, the geometry of the solder joints varied which affected the stress accumulation inside of them. Thus, this model was not valid everywhere. To use this equation it is critical to know a lot about the material properties used in the power module. Numerous other models also consider that the solder joint is the vulnerable part of the power module. These models however focus on the crack propagation of soldier joints [39] [40].

$$N_f = W_{crit}.(\Delta w_{hys})^{-n} \tag{2.14}$$

W_{crit} is Critical Energy required for failure (J)
Δw_{hys} is the accumulated deformation energy per cycle (J)
n is a constant that depends on the solder type

Another interesting Physics-Based Model is that of O. Schilling et al. as it considers that the primary failure mode here is the failure of aluminium bond wires [41]. However, this model also follows Morrow's law like the equation above as seen in (2.15). However, here the deformation energy (Δw_{hys}) is not for the solder joint but for the bond wire. This was calculated using a 2D FEM model after Young's Modulus of the material was known. The results from this model were compared to the Coffin Manson Model for failure described earlier in 2.5.2 where the number of cycles to failure was determined by the temperature swing. The authors thus stated that the difference in measurements was within expectations between the empirical measurements and the values determined from 2D FEM calculations.

$$N_f = c_1.(\Delta w_{hys})^{c_2} \tag{2.15}$$

c_1 is a value that depends on the geometry of the module
c_2 is a constant derived from previous experiments ($c_2 < 0$)

Depending on the information available, either the empirical models can be used or even the physics-based model. It is important to note that since the empirical models are a result of several experiments conducted on a specific type of power module, the fitting constants may vary from one set-up to another. Therefore, to get accurate values in the case of empirical models, it is important to replicate the test conditions and use the correct fitting constants to calculate the lifetimes for the power modules. Based on this information, the choice of lifetime model has been made in Section 3.7

2.5.4. Damage and Lifetime Estimation

Once the Nf is calculated, one can then proceed to calculate the damage estimation. This can be done by (2.16). This will be done over the period of one charge cycle. This can thus give the damage accumulated over a single cycle.

$$D = \sum_{i}^{n} \frac{n_{f,i}}{N_f} \tag{2.16}$$

Here D is the damage accumulated overtime
$n_{f,i}$ is the number of cycles run during that time period of type i
n is the total number of types of cycles

Alternatively, the same formula can be used to calculate the accumulated damage over a year. For this purpose, it can be assumed that the converter is undergoing the same type of charge profile a certain number of times each day. Once this is done, the static lifetime of the converter in years can be calculated using (2.17).

$$L = \frac{1}{D} \tag{2.17}$$

Here L is the lifetime of the component (years)

The lifetime and damage derived in the cases above are applicable to each of the devices. However, in reality, the components in a power converter are bound to interact with one another and change the lifetime slightly. Thus, a weighted average can be considered as shown in [42] to calculate the average damages occurring in the entire converter. This can be done by using (2.18).

$$D_{avg} = \frac{1}{\sum M^{(X)}} \cdot \sum \sum_{i}^{M} D_{i,X} \tag{2.18}$$

Where X is the type of the component (this can be capacitors, diodes, or switches)
$M^{(X)}$ is the number of that specific type of component
$D_{i,X}$ is the damage for that specific component

Thus, the formula essentially adds the up the damage of all the components present in the circuit and divides it by the number of components being considered thereby calculating the average damage. This average damage can then be used to calculate the lifetime of the converter by using (2.17).

The static life thus derived refers to the lifetime of the converter considering that none of the variables change for any of the cycles. While this is slightly unrealistic in a real-world scenario, it provides a good benchmark to compare multiple lifetimes. The variance of different variables is however taken into account in the B10 lifetime. This can also be calculated using the equations given above with some minor tweaks.

2.6. Reliability

In the previous section, the lifetime of the diode or the IGBT can be found in terms of years. However, this static lifetime derived above provides no indication of the reliability of the components at this time period. Thus, a more in-depth analysis needs to be performed. One of the ways to do so is with a B10 lifetime estimation. B10 lifetime is the time by which at least 10% of a population of devices is expected to fail. This also means that the components thus have 90% reliability up until that age. It is a common tool used in industries to predict the lifetime of products and their reliabilities. It can also be represented in other ways like the Bx lifetime where 'x' represents the failure probability at that time. Many manufacturers often base their warranties on these lifetime numbers.

In practice, this is done by experimentally testing a certain number of components and checking when x% of the population of test samples start failing. However, this is not always a possibility as testing components towards failure is destructive testing and ultimately leads to an increase in costs. Thus, it is often a better idea to calculate these lifetimes from statistical tools like using the Monte Carlo method. It is a method to randomly draw samples from a population and predict a deterministic outcome. Essentially, it can simulate the concept of randomly selecting a number of components and testing them to give a wide range of data available for the whole population. It can do this by changing different variables up to a certain magnitude if the probability distribution function for that variable is known in nature. In the case of estimating lifetimes, the independent variables in the equations discussed in the previous section can be varied to a certain extent and the lifetime for each of those cases can be determined. it is known that in the case of thermo-mechanical cycling, the lifetimes generally follow a Normal or Weibull distribution [43]. A larger value would be a more inclusive population, however, it may not be a realistic scenario. At the same time, it is important to select a vast number of samples to be tested. The higher the number of samples being tested, the better will be the accuracy of the model. Thus, knowledge of the following factors is necessary for the simulation -

- The independent variables that can be varied
- The sample size
- The extent of variation in the mean data points

These factors will be discussed in Section 4.5.2 for this thesis.

Once these factors are known, a CDF (Cumulative Distribution Function) graph is generated for the lifetime of the component. Through this graph, it can be identified at what point in time 10% of the population is expected to fail. In other words, at this point, the reliability is achieved to be 90%. Alternatively, the failure rate can be observed at the static lifetime predicted above to get reliability at that point. This can be done with (2.19).

$$R_{sys} = 1 - U_r \tag{2.19}$$

Here R_{sys} is the Reliability of the system
U_r is the Unreliability

An alternative method to measure the reliability of a system or component is to use the Reliability Body Diagram Method (RBD). This method calculates the individual reliability of the various components in the system at a given point in time. The reliability is then calculated according to the layout of the system whose reliability is being measured. If multiple components are in series (their actions rely on one another), the overall reliabilities are reduced and hence they are multiplied by each other. On the contrary, if multiple components are in parallel (their functions are independent of each other, like a redundancy), then the overall reliability of the system increases. The reliability of the system can be calculated with (2.20a) for components in series and (2.20b) for components in parallel.

$$R_{ser} = R_1.R_2.R_3...R_n \tag{2.20a}$$

$$R_{par} = 1 - (U_{r1}.U_{r2}.U_{r3}...U_{rn}) \tag{2.20b}$$

Where R_{ser} is the Reliability of a system of components in series
R_{par} is the Reliability of a system of components in parallel

In such scenarios, it is vital to know how the working of the system to understand which components are in parallel with another and which are in series.

2.7. Research Aspects

Several papers look into the lifetime estimation of semiconductors including diodes, IGBTs and MOSFETs individually when the power is cycled for short durations [44] [45] [46] [37]. However, these papers often do not take into consideration how the presence of other components in the circuit might affect the power cycling happening in these semiconductors. For example, the presence of a transformer can increase or decrease the voltage stresses on these components. Hence, a holistic approach is important to measure the lifetime of these semiconductors in real-world scenarios.

In some studies, the failure rates of various components inside different converters have also been studied, This provided a more holistic approach as mentioned above. However, these papers look into converters that are often used in wind turbines or solar PV [47] [48] [16] [31] [49]. These systems operate in lower voltage and current settings compared to DC Fast chargers and therefore these studies cannot be used to estimate the lifetime of EV chargers. Moreover, these studies generally take into consideration short power cycling where the heating current exists for only 1-2 seconds.

When it comes to the field of EVs, limited knowledge on the lifetime of the overall EV charger is available. This is mostly due to the fact that most of the lifetime analysis for semiconductors is generally done on the basis of extensive experimental testing to failure. Since the technology of DC Fast chargers is fairly new, there exists limited on-field test data to determine the lifetime of such chargers. Some experts predict this can be around 10 years [50]. Other studies discuss the effect of different charging strategies has been seen on power converters [51]. However, the effect studied is the efficiency of the power converters and not the junction temperatures or their lifetimes [52]. While the efficiencies are closely related to the power losses in the system and therefore related to the junction temperature and lifetime, it is hard to specify which parts suffer the most amount of damage solely based on the efficiency and power loss data. This is because while a component has higher power losses it may also have lower internal thermal resistance leading to lower junction temperatures. Moreover, the junction temperature (that is affected by the thermal network of the module) also, in turn, affects the power losses of the component. Thus, it is important to not only look at the efficiencies of the system but also at the thermal network within it which ends up affecting the lifetime ultimately.

Therefore this thesis shall aim to look into the following research aspects -

- Find out the lifetime of the IGBTs/Diodes in a converter environment
- Determine the lifetime of the IGBTs/Diodes used in EV charging applications
- Discuss the effect of the EV charging profile on the lifetime of the converter

2.8. Aim of this thesis

The aim of this thesis is to get an in-depth understanding of EV Charging systems and their lifetimes. More importantly, it shall attempt to determine the lifetime of a DC Fast charger operating under a particular load profile. This process can be further divided into the following points.

- Study various converters and their topologies used in DC Fast Chargers
- Learn the working and model of a DC-DC converter that can vary the voltage and current according to a given load profile
- Study the losses occurring at various semi-conductor components
- Study the structure of the components and model them in a thermal environment to determine the junction temperature when the power losses are known
- Use the junction temperatures and determine the number of cycles to failure for the components
- Apply various statistical tools to find the individual and the overall converter lifetime and reliability
- Propose a standard approach to calculate the lifetime of such EV chargers

3
Methodology

This chapter shall discuss the methodology through which the damage and the lifetime of the power converter shall be obtained. First, the choice of power converter topology will be discussed in Section 3.1 and how the model will be simulated in Section 3.2. Section 3.3 will talk about the process of designing the power converter and determining the various parameters of the circuit. The Load profile is discussed in Section 3.4. Power Loss calculation and validation are discussed in 3.5. The thermal network, junction temperature, and heat sink design are further explored in Section 3.6. Finally, 3.7 talks about the lifetime estimation and cumulative damage calculation based on the junction temperature.

3.1. Choosing a Power Converter

The first objective is to choose a suitable power converter for EV chargers that can handle the power levels of a DC fast charger. Numerous power converter topologies are reviewed in [3]. The review paper focuses on topologies that can be used for DC Fast Charging. It specifies various AC-DC rectification topologies as well as the DC-DC conversion topologies. Since the DC-DC converter is mainly responsible for stepping up or down the voltage from the rectifier, a voltage load profile will primarily affect this DC-DC converter side. Numerous AC-DC rectification topologies can be used to control the voltage output on the DC side of the converter. This can be done with the help of rectifiers that use resonant tanks and thyristors or switches instead of diodes to rectify the AC waveforms as seen in Section 2.2.1. However, this is out of this project's scope.

Thus, the focus of this thesis will be to look into the DC-DC converter topologies. The two main topologies covered in the review paper for DC fast chargers are Full Bridge (FB) Converters and Dual Active Bridge (DAB) Converters. The other converters mentioned in the paper are a variation of them with a resonant tank involved to facilitate ZV (Zero Voltage) or ZC (Zero Current) switching in order to minimize the switching losses. In this project, it will be assumed that the EV charger being studied does not support V2G charging. Thus, the bidirectionally of the power converter is not important in this application.

To choose between these topologies, it is important to compare their merits and demerits. The working of these converters in their simplest forms has been covered in Section 2.2. Table 3.1 shows a summary of the comparison between DAB Converters and FB Converters.

From the table, it can be seen that the greatest advantage that the DAB converter has over the FB converter is the ability to control bi-directional power flow easily. However, since it is assumed that the DC fast charger does not currently support V2G applications, bidirectionality is not required. Moreover, the FB converter offers simple control and is comparatively less expensive due to the lesser number of components. Therefore, the full bridge converter topology was selected.

However, even among the DC-DC Full Bridge converters, there are numerous topologies which included resonant banks and some that do not. Thus, it is important to pin down the exact topology of the circuit. For such converters, the converter topology and the modulation strategy are interrelated. For example, a ZVS modulation technique in a PSFB requires an adequately sized leakage inductance

Table 3.1: Summary of differences between DC-DC FB and DAB Converters [3]

Dual Active Bridge (DAB) Converter	Full Bridge (FB) Converter
Bidirectionality possible for V2G charging	Unidirectional charging
Complex control methods required	Simple PWM control is used
High frequency current ripples	Lower Current stresses on switches
High Efficiency	Lower Efficiency due to more diodes

present on the primary side [53]. This helps the energy be stored and reduces the sharp drop/rise in currents passing through the switches. It is also required for achieving ZVS modulation. However, in the case of a simple PWM modulation, the switching losses are greater and thus have lower efficiency. The advantage of this modulation is that the output voltage can be controlled easily by varying the duty cycle. This leads to much simpler control and a lower requirement of components. The waveforms of these modulation techniques can be found in Figures 2.5a and 2.5b respectively.

Due to the simplicity of design and the focus of the project being on the losses rather than the topology of the converter, the chosen modulation technique and design was the DC-DC Full Bridge Converter without a phase shift (simple PWM modulation).

3.2. Modelling the power Converter

Once the power converter was chosen to be a DC-DC PWM-FB converter, it was then important to decide where the power converter will be modelled. Simulink in MATLAB provides a robust toolbox in the form of Simscape that helps one accurately model electrical and electronic circuits. In particular, it is important to use the Simscape toolbox since it has the option to combine with other toolboxes in the system. For the purpose of this project, it would be helpful to measure the power lost in the semiconductors in the form of heat to calculate the junction temperature. Simscape semiconductor blocks also have the ability to monitor the junction temperature of a circuit. Moreover, it can be combined with external thermal circuits to accurately represent the other layers of the module and the packaging of the power converter.

This allows MATLAB Simulink to simulate multiple physical domains (electrical and thermal) at the same time. Unfortunately, the DAESSC solver present in MATLAB Simulink was one of the only solvers that could handle multi-domain simulations. This solver is built particularly for solving differential-algebraic equations. for multi-domain simulations. While this solver is robust it compensates with a large computational load. Therefore, running the simulation was too time-consuming and hence other options needed to be explored.

One such option was PLECS. PLECS is a software designed by PLEXIM that is made especially for designing electronic circuits. The solvers included in the software are suited specifically for these applications. Moreover, their components also have features to model external thermal circuits and measure the power loss of the semiconductor components in the circuits. This software turned out to be much faster than using MATLAB Simulink. However, the flexibility of control algorithms in PLECS proved to be much lower than that of MATLAB Simulink.

Fortunately, PLECS is cross-compatible with MATLAB. This allows one to simulate the control part of the circuit in MATLAB Simulink, while the circuit can still be simulated in PLECS only. This hybrid simulation method increased the simulation speed compared to MATLAB Simulink while the decrease compared to PLECS standalone was negligible. Thus, this was chosen as the way to model the circuit.

3.3. Design Parameters Used in the Circuit

This section shall discuss how the design parameters were determined for the DC-DC PWM FB model. Section 3.3.1 will discuss the initial input parameters. In Section 3.3.2, the duty ratio is chosen. Further, in Section 3.3.3, the design of the transformer will be explored. Primarily, the turns ratio will be considered. After that, the design of the output filter will be discussed in 3.3.4. The design process used in this thesis is similar to that used in the paper by Sabate et. al [53]. However, that paper discusses a design procedure for phase shifted converters. Thus, certain aspects were modified by obtaining design principles from [8]. The design procedure consists of mainly 3 steps -

1. Choosing the maximum duty ratio
2. Determining the turns ratio
3. Designing the output filter inductance and capacitance

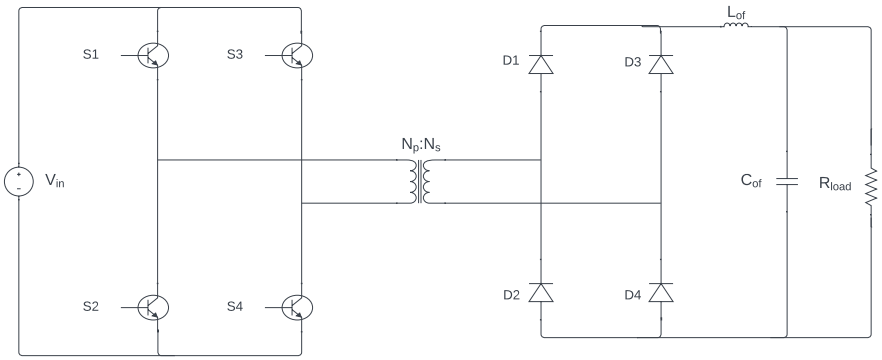


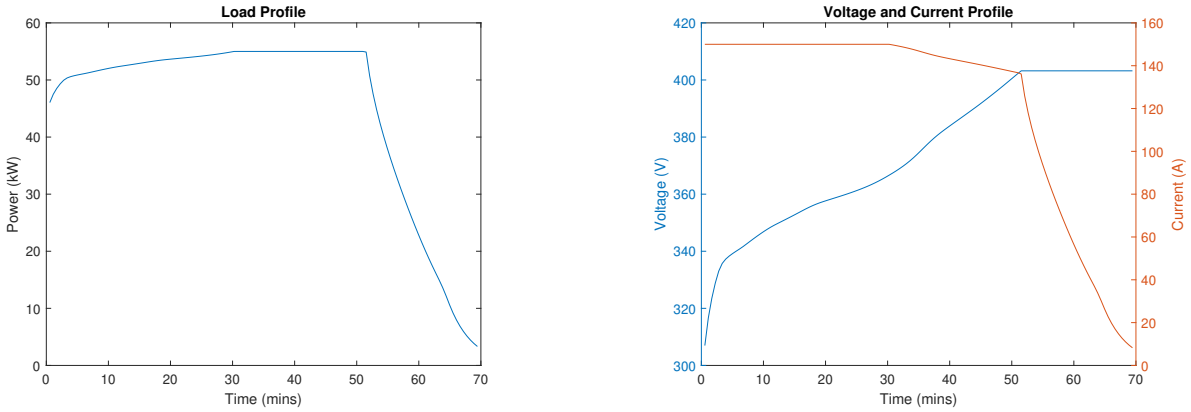
Figure 3.1: Schematic of DC-DC PWM Full Bridge Converter used in this project

3.3.1. Initial Design Parameters

As the converter that is being focused on is the DC-DC converter, it can be assumed that the rectifier is supplying a constant DC voltage as an input. This is assumed to be 600V. From the load profile that is currently being studied, it can be seen that the output voltage ranges from 307V to 403V. Thus, this range shall be used as the output voltage. At the same time, the power varies from 44kW at the start to 3kW at the last time step. A summary of these input parameters is provided in Table 3.2. The voltage and power profile can be seen in 3.2a and 3.2b respectively. Thus, the total current output shall be considered accordingly. The switching frequency for this converter is initially chosen to be 10kHz for the IGBTs. The IGBT chosen for this purpose was the FF200R12KE3 produced by Infineon [25].

Table 3.2: Initial Design Parameters

Input Parameter	Value
Input Voltage	600 V
Output Power	3.34 kW - 46.04 kW
Output Voltage	307 - 403 V
Switching Frequency	10 kHz
Allowable Current Ripple	20%
Allowable Voltage Ripple	1%



(a) Power Profile

(b) Voltage and Current Profile

Figure 3.2: Load Profiles for the EV

3.3.2. Choosing Duty Ratio

In a DC-DC PWM Full Bridge converter, one switch pair is active for one-half of the switching period while the other switch pair is active for the other half. Therefore, a 50% duty cycle means that the switch on the inactive leg is switched on as soon as the active leg switch is turned off. In ideal cases, this causes a momentary short circuit (especially if the switch is considered to be ideal with no internal resistance). In practical cases, this is much longer. Moreover, the simulation shows a switching error in these cases where the circuit appears to be short-circuited. Choosing a lower maximum duty cycle would require an increase in the turn ratio to match the required output voltage. This can increase the voltage stress on the diodes. Thus, the maximum duty ratio will be chosen as 0.45 for each active switch pair.

3.3.3. Determining Turns Ratio

For this project, the transformer is considered to be an ideal one. Thus, the only other parameter to be selected is the turns ratio of the transformer. Since the turns ratio decides the voltage output on the secondary side, it is important to take a look at the input and the output voltages. The input voltage is above the output voltage at all operating points in the load profile being considered. Thus, a bucking operation is important. Moreover, it is important that the secondary side voltage is not higher than the rectifier's diode's breakdown voltage.

Another important consideration is the duty cycle of the switches. Once the max duty cycle is decided, the transformer turns ratio can then be estimated using (3.1). Since the input voltage is always higher than the output voltage, a turns ratio lower than 1 is required for the entire range of operation. The minimum allowable turns ratio can be determined after looking at the max output voltage required. In this case it is about 403V.

Therefore, by inputting the above values in (3.1), one gets $N = N_s/N_p$ = 0.746 which is the turns ratio. For the purpose of this project, 0.8 will be assumed as the turns ratio since $N_{min} < 0.8 < N_{max}(1)$. Other values between this range can also be selected. With the turns ratio selected, the duty cycle at every individual point can be determined with the help of the same equation [53] [8]. To do this, however, the output voltage will be changed to the required output voltage at that point.

$$\frac{V_{out}}{V_{in}} = 2.\frac{N_s}{N_p}.D_{max} \tag{3.1}$$

Here V_{out} is the Output Voltage (V)
V_{in} is the Input Voltage (V)
N_s is the Number of secondary turns of the transformer
N_p is the Number of primary turns of the transformer
N is the turns ratio (N_s/N_p)

D_{max} is the Max Allowable Duty Ratio for each switch leg (maximum can be 50%)

3.3.4. Filter Design

As the switches generate a square wave through their modulation technique, there are bound to be ripples in the output waveforms of the load current and voltage. Thus, an LC filter is proposed to reduce the oscillations and smooth out the waveforms. This has been done by calculating the allowable voltage and current ripple percentages. For EV charging, about a 1% voltage ripple is allowed and a 20% current ripple is allowable. The inductance of the filter can be calculated by (3.2) [54] [8].

$$L_{of} = \frac{V_L}{\Delta I_{ripple}} DT_s \tag{3.2}$$

Here L_{of} is the Inductance of the output filter (H)
V_L is the voltage across the output filter inductor (V)
T_s is the switching period of the system (s)
D here is the Duty Ratio of the switch leg at that operating condition
ΔI_{ripple} is the current ripple experiences across the inductor and here $\Delta I_{ripple} = 0.2 * I_{out}$ since the allowable output current ripple is 20%

It is important to note that there are two versions of (3.2). They are based on the same principle but vary depending on the time duration during which the inductor is being analysed, that is, whether it is being analysed while the switch is turned on, or while it is turned off. These variations can be seen in (3.3a) and (3.3b) respectively.

$$L_{of} = \frac{V_{out}}{\Delta I_{ripple}} (0.5 - D)T_s \quad \text{When switch is off} \tag{3.3a}$$

$$L_{of} = \frac{(NV_{in} - V_{out})}{\Delta I_{ripple}} DT_s \quad \text{When switch is on} \tag{3.3b}$$

Here V_{in} is the Input Voltage (V)
V_{out} is the Output Voltage (V)
N is the turns ratio

However, due to the nature of the load profile, the output current keeps varying. To account for this, the minimum output current is taken into consideration. This will allow the design to be robust and the inductor will be able to smoothen out ripples of higher current values too. In the load profile this point is that of the 8.4A output current and 403V output voltage. Thus, assuming the lower boundary for current, using (3.3a), a value of **1.6 mH** is calculated for the inductor.

Now, the voltage ripple of a converter is closely related to the capacitance and the change in charge using as shown in (3.4a), where ΔQ is the change in charge when compared to the mean output current and ΔV is the allowable output voltage ripple [54]. Here, ΔQ is essentially the amount of charge accumulated over time or the area under the triangle. Thus it can be calculated using (3.4b). Thus, substituting this value in the previous equation, one gets the resultant equation for the output capacitance in (3.4c).

$$C_{of} = \frac{\Delta Q}{\Delta V} \tag{3.4a}$$

$$\Delta Q = \frac{1}{2} \frac{\Delta I_{ripple}}{2} \frac{T_s}{2} \tag{3.4b}$$

$$C_{of} = \frac{1}{8} \frac{\Delta I_{ripple}.T_s}{\Delta V} \tag{3.4c}$$

However, the output voltage would keep varying. Thus, the lowest voltage boundary (307V) and the highest current boundary (150A) are assumed for a robust design as that would help smoothen out the

output voltage ripple even at higher voltage values. Therefore, going for the allowable ripple voltages and currents of 20% and 1% respectively, the required capacitance value is **122.15 μF**.

A summary of the results of the circuit design has been presented below in Table 3.3

Table 3.3: Output Parameters

Output Parameters	Value
Turns Ratio (N_s/N_p)	0.8
Duty Ratio	0.3198 - 0.4198
Inductor Rating	1.6 mH
Capacitor Rating	122.15 μF

3.4. Load Profile

The load profile shown in Figure 3.2 is an artificial EV charging load profile derived by employing a physics model of a lithium-ion cell [55]. This cell data was then used to generate a voltage and current profile (and thus a power profile too) for the charging of an EV Battery. It was used to test the efficiency of a PSFB converter in [51] under an EV load profile. The load profile thus used can be compared to the load profile of Nissan Leaf derived from Fastned [56]. They closely resemble each other, especially in the case of the 40kWh battery profile as seen in Figure 3.3. This thesis shall use the same load profile to estimate the thermal degradation of the semiconductors present in the circuit and thus predict their lifetimes.

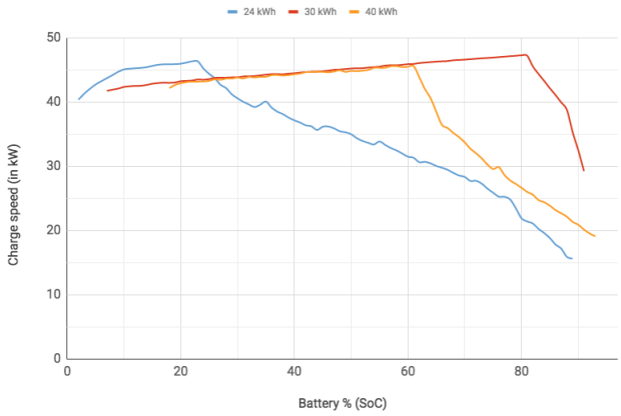


Figure 3.3: Fastned Charging Profile for a Nissan Leaf [56]

As mentioned in earlier sections, the focus of this project is to check the lifetime of EV chargers by seeing the effect that an EV charging load profile has on the thermal degradation of the power converters. For this purpose, a load profile was obtained which can be seen in Figure 3.2b. It lasts for 4167 seconds in steps of 33.6 seconds. Hence, there were a total of 124 load points.

Since the data points in between these ones were unknown, there were two possibilities for interpolating the data. The first way was to assume linear interpolation. However, since the variation in the load profile parameters is around the scale of a few minutes to an hour, it is much slower than the switching time of the converter switches Thus, the second way was used. In this method, the power, voltage, and current can be assumed constant at that point for the whole of 33.6 seconds before moving on to the next one.

The resultant load profile was in the shape of a staircase with every horizontal step representing the data point at that time. This meant that the load profile still had to be run for 4167 seconds which is

very costly computationally. Thus, to simplify this further and reduce the computational load, all these points were assumed to be steady states. Moreover, the simulation was used to only derive the power losses that occurred at the semiconductors. This helped reduce the computational time further as the thermal circuit didn't have to be completely modelled. The junction temperature could then be derived from the power losses given as described in Section 3.6.2. However, for validation purposes, the whole circuit was run as well including the thermal circuit to check the functioning of the PLECS Simulation.

3.5. Calculating Power Losses

In PLECS, the power loss of different components can be calculated based on inbuilt or imported component models. Moreover, the distinction between power loss due to conduction and switching loss is easier to distinguish. The power loss determined from these simulations will also thus be used to calculate the junction temperatures. Hence, it is imperative to validate these values as well.

The validation will be performed by comparing the values simulated by PLECS and the ones derived manually by using empirical formulae of power losses. Depending on the type of component, the switching and conduction losses can be calculated by the equations presented in Section 2.3. Once the switching and conduction losses are determined, the total losses can be calculated using (3.5). However, it is important to note that another crucial value required while calculating the losses is the current passing through the switch. The simple way to calculate this would be to accept the current measurements of the simulations. However, this feeds back to the assumption that the circuit has been modelled correctly. Thus, the second method to analytically derive the current is the preferred method. This has been explored in detail in sections 4.3 and 5.1.

$$P_{loss} = P_{cond} + P_{sw} \tag{3.5}$$

Here P_{loss} is the total power loss experienced by the component.
P_{cond} is the conduction power loss.
P_{sw} is the switch power loss.

It is important to note that as mentioned in Section 2.3, the gate driver losses have been ignored in this equation.

3.6. Junction Temperature Calculations

This section shall focus on three topics. Firstly, the actual layout of the thermal circuit will be focused on in 3.6.1. In Section 3.6.2, the junction temperature calculation method will be discussed. Finally Section 3.6.3 will focus on calculating the heat sink thermal resistance in such a way that the semiconductors can stay within safe operating temperatures.

3.6.1. Designing the Thermal Network

As mentioned in the sections above, the thermal network is crucial for getting accurate junction temperatures. Moreover, there are two thermal circuits to consider in this model - the internal thermal circuit and the external circuit. The internal thermal circuit is often mentioned in the datasheet of the component used. An example of this can be found in Figure 2.9. This can be fed into the simulation model to reflect practical experimental results. In the case of PLECS, most manufacturers like Infineon provide PLECS data files that can be imported into the software. These models reflect the voltage drops and the collector/drain current at different temperatures and even the turn-on/off power losses experienced by the device at different operating points. Moreover, they feed in the internal thermal network parameters to accurately represent the losses and the junction temperatures. Other parameters like the thermal interface resistance must be added which reflects the solder or the thermal grease. Thus, the task after that is to connect it to the external thermal network or the heat sink. This can then be connected to an ambient temperature source to model real-life conditions. The assumption here is that the other side of the semiconductor is a perfect insulator and thus there is heat flow only via the surface exposed to the heatsink. A schematic of the thermal network can be found in Figure 3.4.

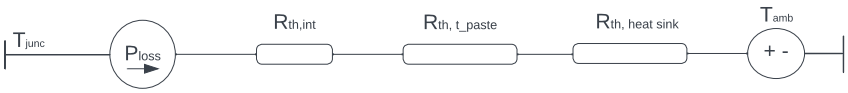


Figure 3.4: Thermal Network of Semiconductors

3.6.2. Finding the Junction Temperature

Once the power losses have been determined and validated, they can be used to determine the junction temperatures at various load points. This data can then be used to generate a temperature profile throughout the charging profile of the car to determine the thermal cycling load that the power semiconductor underwent. This data is then used to calculate the damage to the power semiconductor in question. This is explored further in Section 3.7.

To calculate the junction temperature, the thermal impedance of the network is required. As mentioned in Section3.6.1, these values can either be found in the semiconductor datasheet or in the literature. Thus, by combining the internal thermal impedance (junction to case), the interface thermal impedance (case to heatsink), and the heat sink thermal impedance (heatsink to air), a thermal model like in Figure 3.4 is obtained. Given all this data, the junction temperature can be calculated using (3.6) [29].

$$T_j = T_{amb} + (Z_{th(j-c)} + Z_{th(c-h)} + Z_{th(h-a)}) * P_{loss} \tag{3.6}$$

Here T_j is the junction temperature (K)
T_{amb} is the ambient temperature (K)
P_{loss} is the maximum total power in the component (W)
$Z_{th,(j-c)}$ is the thermal impedance between the junction and the case (K/W)
$Z_{th,(c-h)}$ is the thermal impedance between the junction case the heatsink (K/W)
$Z_{th,(h-a)}$ is the thermal impedance between the heatsink and the air or ambient conditions(K/W)

3.6.3. Designing the Heat Sink

As mentioned in the previous sections, there are primarily two thermal networks to be considered - the internal one and the external one. The external one consists of the heatsinks and the thermal paste. The thermal interface or thermal paste resistance is generally mentioned along with the IGBT/Diode datasheets. This is because the interface thermal resistance is decided based on the area of the power module and the thickness of the paste is determined by the rated tightening force. However, the heatsink thermal resistance/impedance is something that needs to be determined. This is generally based on the operating temperature of the power module and the power loss generated by it. Therefore, (3.6) can be rearranged to derive the heat sink thermal resistance as shown in (3.7).

$$Z_{th(h-a)} = \frac{T_{j,max} - T_{amb} - P_{loss,max}.(Z_{th(j-c)} + Z_{th(c-h)})}{P_{loss,max}} \tag{3.7}$$

Here $T_{j,max}$ is maximum allowable operating junction temperature (K)
$P_{loss,max}$ is the maximum amount of power loss throughout the load profile (W)

It is important to note that this equation can change depending on the thermal network created. For example, this equation can be modified depending on the number of intended devices to be planted on the heat sink. Since the semiconductor devices considered in this thesis are both modules with 2 devices (diodes, IGBTS) inside each of them, a factor of 2 must be used for the powerloss term. If required, 4 devices can also be mounted on the same heat sink depending on the powerloss figures. For a robust design, the max allowable junction temperature used can be slightly lower than specified in the data sheet and the ambient temperature can be raised too.

The power losses in semiconductors are affected by the junction temperature which is an effect of the heat sink design. Nevertheless, the power loss values calculated in previous sections can be used as a rough estimate to design the heatsink with suitable approximations. These numbers can then be used to find real-world heat sinks that have similar or lower thermal resistance values to minimise the junction temperature. This has been done in sections 4.4.1 and 5.2.1 for IGBTs and Diodes respectively.

3.7. Life Estimation and Damage Calculation

With the thermal profile, the next step is to determine the damage to the switch. As detailed in Section 2.5, there are several lifetime models that can be used to determine the lifetime of semiconductors. For the purpose of this project, the chosen lifetime model is the CIPS08 model [57]. This model predicts the Number of Cycles to Failure based on the assumption that bond wire lift-off and solder fatigue is the main cause of failure in such devices. It is to be noted that this formula is only valid for modules which contain an aluminium oxide substrate.

The CIPS08 model as listed in (2.12) has 6 fitting constants, namely β_1 , β_2, ... β_6 and A as Coffin-Manson term. These values depend on the type of circuit being used and vary accordingly. Their values were determined after experimental testing of several semiconductors. For the purposes of this thesis, the generic model values listed in reference shall be used which can be found in Table 3.4. Other than these there are a number of variables that depend on the device, or rather the bond wire being used inside the device. Namely, these are the Bond wire diameter (D), the device voltage class (V) and the max current allowed per bond wire stitch (I). Since these values are generally not provided in the data sheets, a possible solution is to use the bond wire specifications used by the semiconductor manufacturers. Their specifications will be mentioned while calculating the individual component lifetimes.

Table 3.4: CIPS08 model coefficients [57]

Constant	Value
A	9.3E14
β_1	-4.416
β_2	1285
β_3	-0.463
β_4	-0.716
β_5	-0.761
β_6	-0.5

There are then 3 different independent variables that need to be considered which are a result of the load profile being simulated. These are the junction temperature fluctuations (ΔT_j), the minimum junction temperature ($T_{j,min}$), and the thermal cycle time duration (t_{on}). Now, the first two variables can be derived from the results of the simulation while the cycling time can vary in multiple ways. In such cases, two kinds of cycle times can be considered. The first type is short-term cycling. This is caused by the device being turned on and then turned off. This would lead to small temperature fluctuations. The second type is long-term temperature fluctuations. This would be the rise and fall of the junction temperature as a result of the entire load profile and not just the switching on or off of the devices. Since the aim of this project is to calculate the lifetime of the EV charger based on the load profile, the temperature fluctuation due to the load profile is considered and not the switch directly. Moreover, due to the very small junction temperature swing caused due to the switching behaviour of the semiconductor, the damage accumulated will be lower too. This can be seen in detail later in sections 4.5.2 and 5.3.2 where the significant effect of the junction temperature swing on the lifetime is studied with the Monte Carlo method.

However, the CIPS08 model takes into account only short-term power cycling [36] [57]. Numerous papers indicate a variety of methods that approximate the cycling time based on conditions when the cycling time is over 1.5 seconds. (3.8a) is one of them which considers that the lifetime for a cycling time greater than 15 seconds remains unchanged as at this point, the system reaches a steady state with regards to temperature and thermal expansion [57]. On the other hand, (3.8b) considers that this steady state point is reached only after 60 seconds [58] [36].

$$N_f(t_{on}) = \begin{cases} N_f(t_{on}) & \text{for} \quad t_{on} \leq 15s \\ N_f(15) & \text{for} \quad t_{on} > 15s \end{cases} \tag{3.8a}$$

$$N_f(t_{on}) = \begin{cases} N_f(t_{on}) & \text{for} \quad t_{on} \leq 1.5s \\ N_f(1.5) * \left(\frac{t_{on}}{1.5}\right)^{-0.3} & \text{for} \quad 1.5s < t_{on} \leq 60s \\ 0.33 * N_f(1.5) & \text{for} \quad t_{on} > 60s \end{cases} \tag{3.8b}$$

Where $N_f(t_{on})$ is the Number of cycles to failure at a particular t_{on} duration
t_{on} is the power/thermal cycling time (s)

Since both formulae are from reputable sources, it is important to choose between the two. To help with this decision, for varying values of ΔT_j, the number of cycles to failure was plotted for both these approximations. Since the load profile is in excess of an hour, the constant values were considered in both approximations. All the other constants were kept the same. The comparison is shown in Figure 3.5. As one can see, there is barely any difference between the two methods used. Therefore, the approximation mentioned in (3.8a) will be considered. This is because the steady state of the system is generally within a magnitude of five to six-time constants (of the system). As the time constant of power semiconductors is within 1 second usually, the 15-second approximation is closer to a real-world scenario and is thus used.

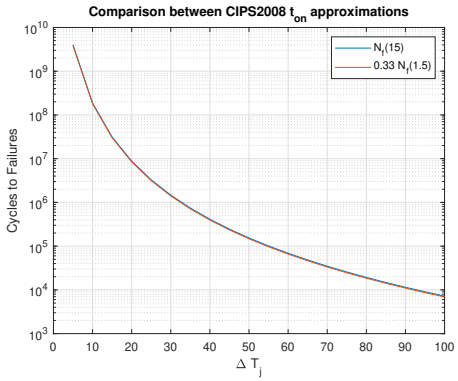


Figure 3.5: Comparison between different t_{on} approximations

Two methods of lifetime calculation will be focused on in this thesis. For one, the static lifetime assumes that there are no deviations from said values and the same car is being charged at the station with the same load profile every day for a number of times. While this gives a good baseline to compare two or more semiconductor devices, the lifetime value obtained from it is not realistic. Thus, the second-lifetime estimation strategy - the B10 lifetime estimation is used. The lifetime proposed by using this method accounts for variations in the input by means of a Monte Carlo simulation. This lifetime is the B10 lifetime which states that by this time, 10% of the devices in the population can fail.

3.7.1. Static Lifetime

The static lifetime can be calculated by first measuring the temperature fluctuations. Then the CIPS08 model can be used with the cycling time approximation mentioned in the (3.8a) to determine the number of cycles to failure. The number of cars that are being charged daily needs to be assumed to determine the damage accumulated over a year using Miner's rule that is stated in (2.16). With this, the damage

over a year can be calculated. Thus to calculate the number of years as the lifetime, a simple reciprocal is required as seen in (2.17). This will then output the number of years the semiconductor can last.

3.7.2. B10 lifetime

In the case of B10 lifetimes, the unknown deviations in various independent variables are considered. In the case of the CIPS08 model, there are three independent variables -

- Temperature fluctuation (ΔT_j)
- Minimum Junction Temperature ($T_{j,min}$)
- Thermal Cycling Time (t_{on})

As mentioned earlier, deviations to the cycling time are immaterial as it is assumed to be a certain value post the 15-second mark. Thus, the choice to vary the first two was made. Once the independent variables are selected, sample size and variance need to be determined. A large sample size will lead to a more accurate model and more variance will create a robust model. Thus, for this purpose, a sample size of 1000 and a variation of 10% was selected. Finally, a type of distribution needs to be selected for the randomly generated values. In most cases of thermomechanical failures, the function tends to be a Weibull distribution function or a Normal distribution function distribution. For simplicity, the Normal distribution function shall be chosen for this project.

Once the above factors are decided, the same process flow can be followed as it was for the static lifetime estimation. First, the number of cycles to failure shall be calculated, then the accumulated damage and finally the lifetime in years. However, in this case, the calculations will be made for 1000 of the data points that were randomly generated. Once this is done, the probability distribution function (PDF) of lifetimes will need to be converted into a Cumulative Distribution Function (CDF). This curve would then give the unreliability on the y-axis and the lifetime (in years) on the x-axis. Since the focus is to determine the B_{10} lifetime, the unreliability of 0.1 is of concern. The x coordinate of this value on the CDF will then provide the B10 lifetime of the device. When the B10 lifetimes of both the diodes and the switches have been determined, then it can be easier to point out which of them is the bottleneck/root cause for the lifetimes. Accordingly, efforts can be focused on that part of the circuit to improve the lifetime of the entire converter and ultimately the DC Fast Charger.

Moreover, the overall converter lifetime can also be calculated either by means of the averaged damage method or the Reliability Body Diagram (RBD) method. It is important to do so as the individual component lifetimes derived earlier will always be higher than the system level lifetime/reliability. Therefore, these methods will be studied further in Section 6.1.

3.8. Summary

This chapter discussed how the model was derived and how numerous parameters were calculated for the model for the scope of this thesis. Then it was discussed how the power loss calculations will be verified along with the junction temperature values from the simulation. Finally, various methods of deriving the lifetimes for the semiconductors were explored. An important note to be made is the assumptions that were made during the simulation of this converter. These have been enumerated below -

1. V2G is not required for this type of charger.
2. The Voltage and Current stay constant for a period of 33.6 seconds before being changed to the next operating point.
3. External layers of the power module were assumed to be similar to other modules that currently exist.
4. Failure mechanisms do not interact with each other.

4

Base Case Results and Validation

This chapter will discuss the results of the base case scenario and try to validate the simulation outputs. To clarify, the base case is the assumption that the most vulnerable semiconductor in the DC-DC full bridge converter topology is the switch. In the base case, it is considered to be the IGBT whose specifications are listed in Table 4.1. This chapter will start discussing the initial results of the converter in Section 4.1. This includes the output voltage and current. Following this, a more thorough verification of the results will be performed by observing the output waveforms. They shall be compared with the expected waveforms as seen in the literature in Section 4.2. Post this, Section 4.3 will highlight the power loss values of the IGBT derived from PLECS. They will then be compared with the calculated power loss values from empirical formulae to validate these numbers. Finally, a temperature calculation will be performed in Section 4.4 and then accordingly compared with the junction temperature derived from the PLECS simulation. In the end, the number of cycles to failure, the damage and the lifetime will be calculated in Section 4.5 to establish a base comparison for further iterations. Furthermore, a Monte Carlo simulation will also be performed to derive the B10 lifetime by varying various parameters in the lifetime model chosen.

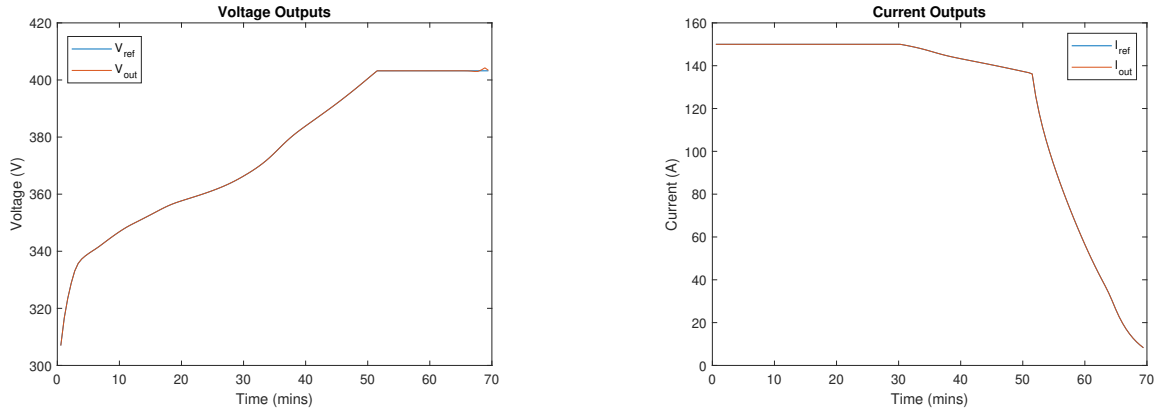
Table 4.1: Properties of IGBT FF200R12KE3 [25]

Property	**Value**
Max. Voltage Drop (V_{ce})	1.7 V
Max. Current Rating (I_{ce})	200 A
Internal Resistance (R_c)	0.7 mΩ

As discussed in Chapter 3, the load profile was divided into several load points instead of a continuous load profile to reduce the computational load on the system. Thus, each load point was simulated individually and the steady state values were used to plot the necessary graphs. These load points can then be used to make comparisons based on their voltages, currents, waveforms, power losses and even temperatures obtained at these points. When these load points are arranged chronologically they exhibit a similar power loss and temperature profile to that of the load profile. This graph can then be used to find the extremities of the temperature profile and accordingly determine the lifetimes.

4.1. Initial Comparison

This section discusses the initial model verification where the output voltage and the current (or power) are compared to the expected/required output voltages and power. A difference between the output voltage and currents can be seen in the graphs displayed in Figures 4.1a and 4.1b respectively.



(a) Voltage Outputs

(b) Current Outputs

Figure 4.1: Output Waveforms

As one can see, the PLECS values show little to no deviation from the expected values of the circuit. Numerically, all the deviations are lower than 1% in terms of error. Therefore it is reasonable to assume that the converter is working sufficiently. These findings show that the design parameters selected for the circuit are correct. However, it is equally important to check the waveforms and compare them to the literature to see if the current and voltage is behaving as expected for this type of topology.

4.2. Waveform Comparison

This section shall compare the waveforms obtained from PLECS at a particular load point and compare them to waveforms expected from the literature. For reference, the load point simulated in this case was 46.04 kW power output and 307V voltage (150A) output. There are six key component waveforms that are going to be studied-

- Gate Signals
- Output Waveforms
- Switch Waveforms
- Transformer Waveforms
- Diode Waveforms
- Inductor Waveforms

Before analyzing the waveforms, it is important to analyse the circuit it is being compared to. The circuit found in literature [8] implements full bridge inverter on the primary side but just a half-bridge rectifier on the secondary side. Moreover, the orientation of the switches is slightly different. Another notable difference is how the turns ratio is structured. In the thesis, the turns ratio (N) is defined as N_s/N_p. However, in the reference circuit, the opposite is used where (n) is defined as N_p/N_s. Thus, it is important to note the differences between the circuits used in this thesis versus the ones found in the literature. This can be seen in Figure 4.2.

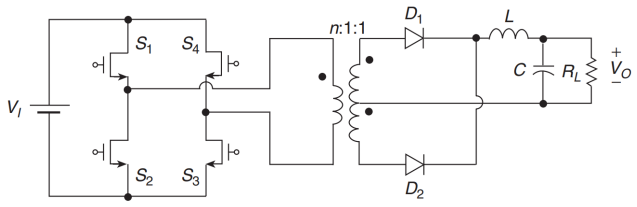
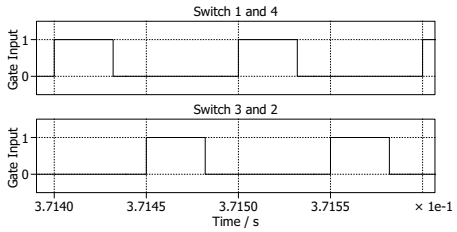
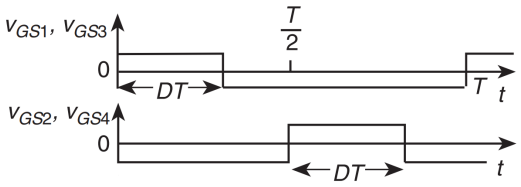


Figure 4.2: Reference DC-DC Full Bridge Converter Circuit [8]

Firstly, the gate signals are compared with each other. This can be seen in Figure 4.3. Here the only notable difference is that there is a negative gate impulse (shown in Figure 4.3b) instead of a 0 signal when the switch is being turned off. This is an optional control strategy used for practical purposes to drain the parasitic capacitances faster and enable faster switching (thereby reducing the switching losses). Otherwise, it can be seen that the control strategies used are the same.



(a) Simulated Gate Signals



(b) Reference Gate Signals [8]

Figure 4.3: Switch Gate Signals

Along with these, the output current and voltage waveforms will also be analysed. At the reference load point, the output current measures 150A. Figure 4.4 shows the output current and voltage waveforms. It can be seen that initially when the simulation is started, there is a slight overshoot. However, the system quickly reaches a steady state condition within 0.1s. The overshoot is caused due to the initialisation of the simulation and the LC oscillation.

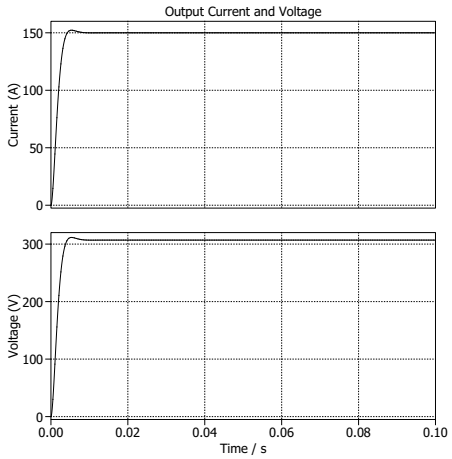
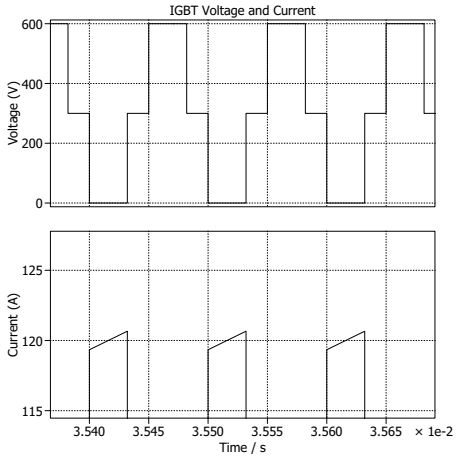


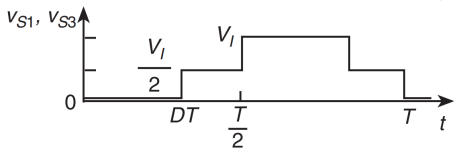
Figure 4.4: Output Current and Voltage

Next, the switch waveforms are analysed. This can be seen in Figure 4.5. In the case of the voltage waveforms, it can be seen that there are 3 distinct stages. In the first stage, the voltage is 0V. At this point, the switch has been switched on and the current can pass through the switch easily. Correspondingly, the current shows a positive value in the same duration. While it is minor, it can be seen that the current value slowly increases. This is due to the presence of the inductor. However, the average current value is maintained at 120A. The average current value for the switch would be the output current reflected back onto the input side when the switch is turned on.

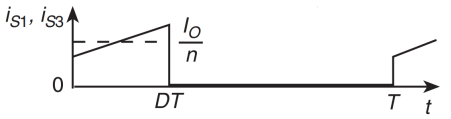
Since the turns ratio is 0.8 and the output current is 150A, the input current can thus be calculated to be 120A. The second stage of the IGBT is when it is switched off. At this interval, even the second arm of the full bridge converter is switched off. Therefore, the voltage is equally divided between both arms of the switches and thus the voltage across the switch is half the input voltage or 300V in this case. Finally, the last stage is where the switches from the other arm are active. In this case, the input voltage is blocked completely by this switch and thus the voltage is at 600V. This behaviour can be confirmed from the literature [8].



(a) Simulated Values



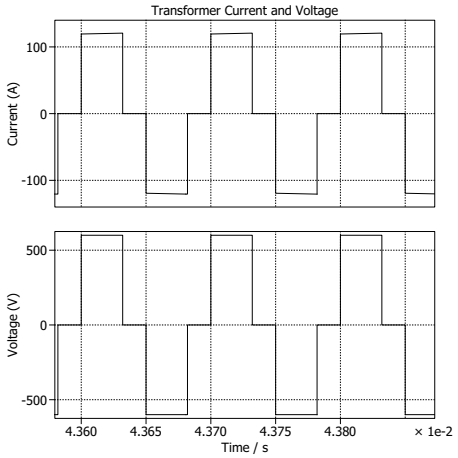
(b) Voltage Reference [8]



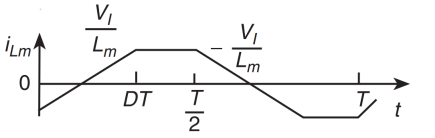
(c) Current Reference [8]

Figure 4.5: IGBT Waveforms

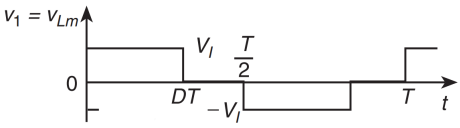
The transformer waveforms will be looked at next in Figure 4.6. In the case of the transformer, the voltage waveforms will be similar to the IGBT ones. However, the three stages would be Input Voltage, 0 Voltage, and Negative Input Voltage. This is because the full bridge on the primary side converts the input DC power into an alternating AC power square wave with the same amplitude. The width of the pulse is determined by the duty ratio. The current would show a similar waveform as well with the current oscillating between the 120A, 0A, and -120A. This can be verified by looking at the waveforms listed in the literature below in Figures 4.6c and 4.6b. The only difference that can be observed is the slopes in the current waveforms. This is due to the presence of a magnetising inductor placed on the primary side of the circuit used in the literature. Nevertheless, the waveforms can be used to validate this current model.



(a) Simulated Waveforms



(b) Current Reference [8]

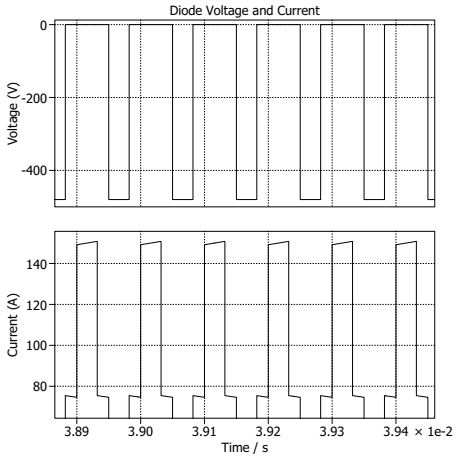


(c) Voltage Reference [8]

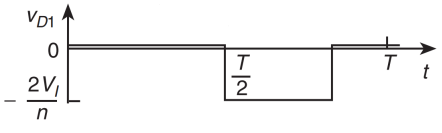
Figure 4.6: Transformer waveforms

Moving on to the diode side, the waveforms change a little bit as seen in Figure 4.7. The voltage applied across the diode is a negative bias and it is of the magnitude of 480V. This is because, on the secondary side, the transformer converts the 600V input voltage to 480V secondary side voltage due to the 0.8 turns ratio. However, in the case of the reference, as seen in Figure 4.7b, the output voltage value is shown differently. This difference can be attributed to the presence of only 2 diodes instead of 4 present in the case of the converter used in the circuit. Thus, when this negative voltage is applied across the diode, the diode does not conduct as can be seen in the current graph where the current is 0. This state is only achieved when the opposite pair of diodes are conducting. The rest of the period can be divided into two sections. One in which the diodes of that leg are conducting and the second in

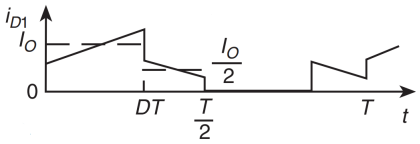
which the diodes are dissipating the energy stored in the inductor. In the first case, it can be seen that the current reaches around 140A and keeps increasing. This is when the corresponding switch legs are turned on. As the energy is stored in the inductor, the current keeps increasing while maintaining an average output current of about 150A. The other section is during the dead times when all the switches are turned off. During this time, the inductor on the secondary side releases its energy and the current is divided equally among the diodes. This is why a degrading current is seen with roughly half the average output current. Similar behaviour can be observed in graphs from the literature.



(a) Simulated Waveforms



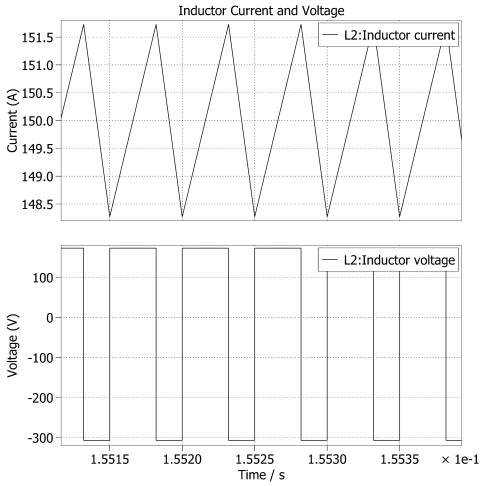
(b) Voltage Reference [8]



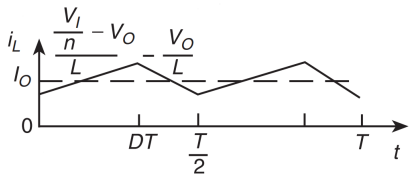
(c) Current Reference [8]

Figure 4.7: Diode Waveforms

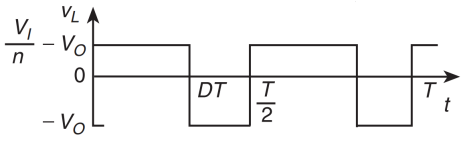
Finally, the inductor waveforms shall be discussed. The inductor current waveforms are simple where the current increases when either of the switch legs is turned on. During the dead times when all of the switches are turned off, the current decreases as the inductor begins to dissipate the stored energy into the circuit. Since the switch is operating in CCM (Continuous Conduction Mode), the current never drops to 0. In the voltage waveforms, the behaviour is also as expected. When the switches are turned on, the voltage would be $V_L = N_s.V_{in} - V_{out}$, which in this case is about 173V. When the switches are turned off, the voltage is equal to the negative output voltage, or -307V. This can be seen in Figure 4.8 and validated by Figures 4.8b and 4.8c respectively in the literature. The working of the inductor as a filter is further verified in Appendix A.



(a) Simulated Waveforms



(b) Current Reference [8]



(c) Voltage Reference [8]

Figure 4.8: Inductor Waveforms

With the waveforms explained above and the initial verification, the general circuit can be considered

to be valid. However, the purpose of this project is to explore the losses of the device and then predict its lifetime. Thus, it is important to verify if the losses simulated by the model are within calculated expectations or not. This shall be explored in the next section.

4.3. Power loss Comparison

This section is concerned with calculating the power loss occurring in the model and comparing it with the values that were derived from the simulation. Moreover, the results of the power losses will also be looked into at various load points. Before looking into the verification of the results, first, the results are presented in Figure 4.9. It can be seen that the absolute losses closely mirror the load profile.

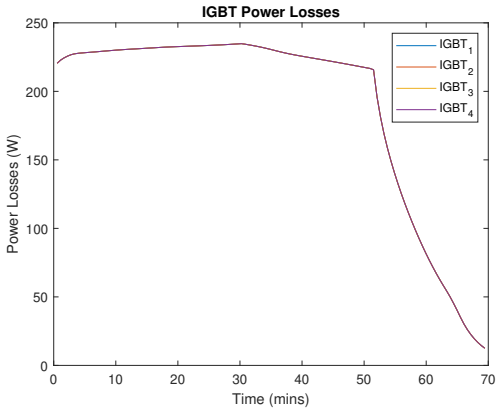


Figure 4.9: Absolute Power Losses of IGBTs

An important observation is that at all load points, the losses are identically the same up to the second decimal. This is because the current passing through them is the same in both cases. Moreover, the voltages applied across them are the same during each switching cycle. Thus, the switching losses and the conduction losses coincide for both arms of the DC-DC full bridge converter.

A second observation is that when the output voltage is increased, the losses increase marginally. This is because at these times, though the current passing through them is the same, the output voltages increase the duty ratios which increase the conduction losses. Consequently, when the current starts dropping (the power starts decreasing at a constant voltage output), it can be observed that the losses start dropping significantly. This is due to the decrease in the switching and conduction losses. Thus, the trends exhibited by the losses are within expectations.

To then verify these losses, just a single IGBT will be considered as the IGBTs exhibit identical losses among all the other parts. As the current flowing through the circuit was already verified in the previous sections, this section is looking into the actual validity of the IGBT thermal model specified in the simulation. As mentioned before, PLECS allows the user to program an inbuilt library coded by the manufacturer for specific components. This allows the software to model the circuit and its losses as accurately as possible. In this case, the thermal model file for the FF200R12KE3 IGBT from Infineon was fed into the model. This contains the following information in the form of lookup tables and/or formulae -

- Conduction Losses
- Turn On Losses
- Turn Off Losses
- Internal Thermal Circuit

While the data sheets often have similar information available, the number of data points is relatively less and thus this thermal model file is a more accurate model that can be used. The objective of this section will be to verify the conduction and switching power loss values obtained by PLECS at various

load points and compare them to calculations performed with the help of empirical calculations.

Before determining the power losses, it is important to calculate the current through the switches. As discussed before in (2.3), the conduction losses of the IGBT require two values of the current. This is the average current $I_{ce,avg}$ and the RMS current $I_{ce,rms}$. To derive these values, it is important to know how the switch current behaves during a single cycle. This can be seen in (4.1) and even in Figure 4.5.

$$I_{ce} = \begin{cases} I_{out}.N & \text{for} \quad 0 < t \leq DT_s \\ 0 & \text{for} \quad DT_s < t \leq T_s \end{cases} \tag{4.1}$$

Here D is the duty cycle of the switch
I_{out} is the output current (A)
I_{ce} is the collector-emitter current through the IGBT (A)
N is the Turns Ratio

The average can then be calculated using the following formula

$$I_{ce,avg} = \frac{1}{T_s}\int_0^{T_s} I_{ce}dt \tag{4.2}$$

Here, T_s is the switching period of the IGBT. After implications from (4.1), and further calculations, this leads to the following answer

$$I_{ce,avg} = D.I_{out}.N \tag{4.3}$$

The next step would to be determine the RMS value of the current, this can be done by using the following formula

$$I_{ce,rms} = \sqrt{\frac{1}{T_s}\int_0^{T_s} I_{ce}^2 dt} \tag{4.4}$$

After implications from (4.1), and further calculations, this leads to the following answer

$$I_{ce,rms} = \sqrt{D}.I_{out}.N \tag{4.5}$$

These values can then be used to find the conduction losses in an IGBT by using (2.3). However, it is important to note that the voltage drop does not vary linearly based on the current flowing through it. Thus, the lookup tables can be used for such circumstances. While the datasheet does give information about the voltage drop across the IGBT, it is important to note that this was achieved under specific conditions including load voltage and current. Thus, to use datasheet values, one would have to apply a crude scaling rule to determine the actual voltage drop at that load point. Also as mentioned previously, the scaling rule is applicable with the assumption that the power losses are linear which they generally are not. Thus, the best way to verify the power losses would be to look at the lookup tables and use the current derived from calculations.

The switching losses can be calculated using two different formulae. The first formula was mentioned in Section 2.3. Even this formula can be used in various forms. One of them is to use the scaling factor as mentioned above to account for the deviation from the measuring conditions. The other form is to look at the look-up tables and accordingly use the E_{off} and E_{on} on values for those operating points. While these values vary according to temperature, an estimate can be taken.

The other formula relies on the values directly from the datasheet as shown in (4.6).

$$P_{sw} = \frac{1}{2} I_{ce} V.(t_{on} + t_{off}).f_{sw} \tag{4.6}$$

Where I_{ce} is the current through the switch (A)
V is the amount of voltage at the output (V)
t_{on} is the rise time of the current during switch-on of the switch (s)
t_{off} is the fall time of the current during switch-off of the switch (s)

f_{sw} is the switching frequency of the switch

The t_{on} and t_{off} can be derived from the datasheet. The other factors will vary depending on the load point and the constant switching frequency used. Theoretically, the rise and fall times are also affected by external conditions like temperatures and gate voltages. However, this formula can be used to also get a close estimate of the switching losses occurring inside an IGBT. Thus, using these three formulae ((4.6) , (2.3), (3.5)), the power losses from the PLECS simulation were compared. The results can be seen below in Figure 4.10.

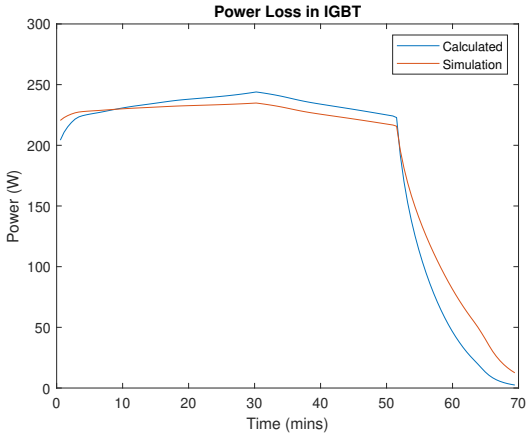


Figure 4.10: Comparison between calculated and simulated power loss values for IGBTs

As one can see the results do deviate by a bit. There are a couple of reasons for this. Firstly, the losses are affected by the component temperatures. While the interpolation between different data points of the currents was accounted for, it is not as simple to do the same with temperatures. The temperatures affect the voltage drops, which in turn affect the losses, affecting the temperatures again. This cycle continues for a while before reaching a steady state value. Thus this might cause a slight difference in values. The difference is impacted by the initial assumption of temperature. If the assumed value is higher than the steady-state temperature value, then the calculated losses will be higher than the simulated ones. Moreover, in the calculations, the mean current is assumed to determine the voltage drops and the switching losses. The presence of the inductor means that the current changes with time as can be seen in the waveforms in Section 4.2. Each of these current values has a corresponding voltage drop. Since they may not always be linear, using the average current value may lead to some inaccuracies. Given these reasons and the difference observed between the calculations and the PLECS values, it can thus be assumed that the results are within expectations and thus valid.

4.4. Validating Junction Temperatures

The previous section validated the thermal loss modelled by PLECS. However, it is also important to validate the junction temperatures obtained through PLECS. To reduce the mismatch in values, the power losses determined by PLECS will be used to determine the temperature differences and the junction temperatures. First, using the power loss values determined above, a suitable heatsink shall be designed. Then, this heat sink shall be included in the thermal network model of the simulation. An initial analysis will be done of the junction temperatures thus obtained from the simulation. These values will then be compared to the junction temperatures obtained by using empirical formulae.

4.4.1. Heat Sink Design

Based on the power loss values derived above, the thermal network for the IGBT can be designed. In this case, an attempt was made to mount all 4 IGBTs (or both the IGBT modules) on the same heatsink. This led to a thermal network whose visual representation can be found in Figure 4.11. It is important to note that an assumption was made that the internal thermal resistances specified in the data sheets

referred to each individual IGBT whereas the thermal interface resistance specified was for the whole module.

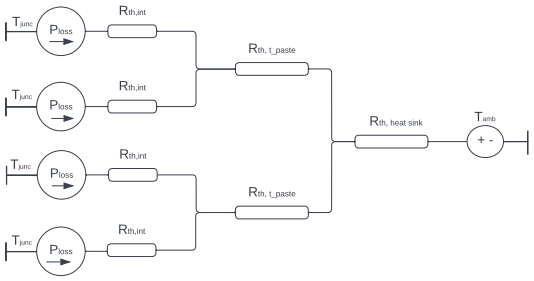


Figure 4.11: Thermal Network Representation for the IGBTs

Thus, the thermal systems are combined wherein they share the same heat sink thermal resistances. Therefore, (3.7) shown in Section 3.6.3 can be modified to (4.7) to determine the required heat sink thermal resistance.

$$R_{th,(h-a)} = \frac{T_{j,max} - T_{amb} - 2.P_{loss,max}.R_{th,(c-h)} - P_{loss,max}.R_{th,(j-c)}}{4.P_{loss,max}} \tag{4.7}$$

Here $T_{j,max}$ is maximum operating junction temperature of the IGBT (K)
$P_{loss,max}$ is the maximum amount of power loss throughout the load profile (W)
$R_{th,(j-c)}$ is the thermal resistance between the junction and the case (K/W)
$R_{th,(c-h)}$ is the thermal resistance between the junction case the heatsink (K/W)
$R_{th,(h-a)}$ is the thermal resistance between the heatsink and the air or ambient conditions (K/W)

For a more robust design, it has been assumed that the maximum allowable junction temperature is 110 degrees C and the ambient temperature is 40 degrees C. In reality, these values are 125 degrees C and 25 degrees C respectively. Substituting these values, the required heat sink thermal resistance is 0.04 K/W. This value is quite difficult to achieve via air cooling which is how the chargers are generally cooled. While there are some cooling fans present in the system, it is important to know that these will also be a source of parasitic losses. On the contrary, it is easier to achieve such thermal resistance via liquid cooling. In this case, a commercially available heat sink with a thermal resistance value of 0.045 K/W shall be used. This is a 512-12M series heatsink from Wakefield-Vette operating under an airflow of 100 CFM (cubic feet per minute) [59]. This thermal resistance value will thus be used to simulate the junction temperature values for the IGBTs. A summary of the thermal resistances used can be found in Table 4.2.

4.4.2. Junction Temperature Values and Validation

Since the previous section showed that the power loss values are very similar for every IGBT, it can thus be assumed that the temperature drop for them will also be the same. This can also be seen in the Figure 4.12a. However, in practical situations, the design of the heat sink, the mounting point of the IGBTs and the orientation of the heatsink (along with the direction of airflow) will play a crucial role in the temperature distribution along the heat sink. But, for the purpose of this project, the geometry of the heat sink is ignored and the focus is on the thermal impedance of it.

As shown by (2.8) in Section 2.4, it can be seen that the thermal impedance is a time-varying quantity. This is primarily due to the presence of the thermal capacitance. However, at steady state conditions, only the thermal resistance can be considered. In reality, as can be seen from the datasheet of the IGBT, this condition is achieved at a time interval between $t = 0.1$s to 1s. According to the load profile, each of the load points is maintained for a total of 33.6 seconds. Thus, it can be assumed that the system is allowed to reach a steady state before moving on to the next load point. Hence, to calculate

the temperature, only the thermal resistances can be considered while the capacitances can be ignored.

Also as mentioned earlier, the thermal system is a combined one. Thus, to calculate the junction temperature, each IGBT cannot be considered individually. The heat from the other IGBTs will have an impact on the total heat dissipation capacity of the heat sink. First, the temperature of the heat sink and thermal paste interface will need to be determined. To find this, the thermal resistances of the thermal interface and the heat sink will be required. The thermal paste parameters are taken from the IGBT data sheet. On the other hand, the heat sink value was determined in Section 4.4.1. Their specifications have been noted in Table 4.2.

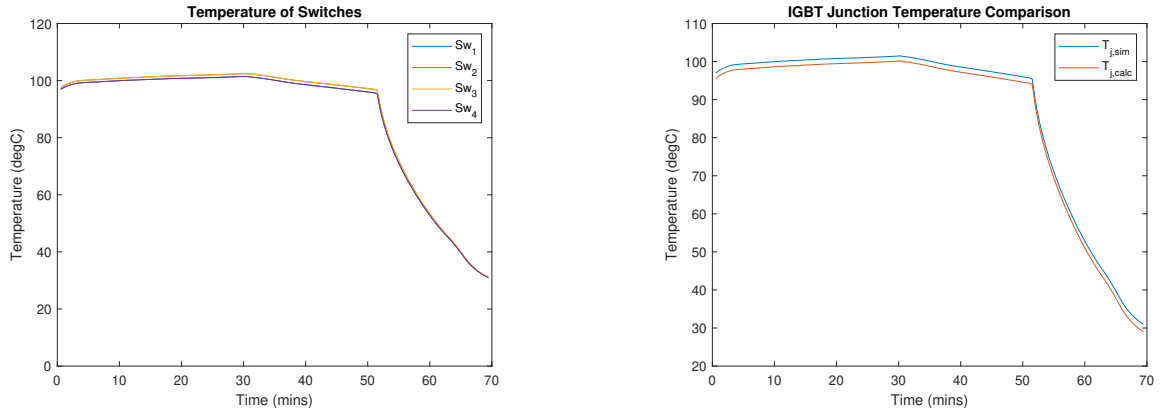
Table 4.2: Internal and External Thermal Circuit Parameters of IGBT

Layer	**Thermal Resistance (K/W)**
Internal Resistance ($R_{th,(j-c)}$)	0.12
Thermal Paste ($R_{th,(c-h)}$)	0.01
Heat Sink ($R_{th,(h-a)}$)	0.045

Using these values, and the combined power loss of all the IGBTs, the temperatures at these interfaces can be determined with the help of (4.8).

$$T_j = ((4.P_{loss}R_{th,(h-a)}) + (2.P_{loss}R_{th,(c-h)}) + T_{amb}) + (P_{loss}.R_{th,(j-c)}) \tag{4.8}$$

Then, each IGBT can then be treated individually to determine the junction temperature. Figure 4.12b shows a comparison between the calculated temperatures and the simulated ones.



(a) Simulated Temperatures of all IGBTs

(b) Temperature Comparison

Figure 4.12: IGBT Temperature Outputs

Figure 4.12b shows that there is still some difference between the temperatures that are obtained from the PLECS versus those of the calculations. This is mostly due to the constant switching nature of the circuit. The temperature begins to rise when the switch is conducting and falls again when it is not conducting. Thus, the final temperature received by the PLECS simulation depends on when the simulation ended and where the temperature was in its cycle when the simulation stopped. This problem can be rectified by increasing the thermal capacitance in the circuit. This would however lead to an increase in the simulation times. Hence the low error margins were accepted for the time being. Due to this low error, it can then be assumed that the model is working and thus the temperature fluctuations derived from PLECS are correct.

From Figure 4.12a, the minimum and maximum junction temperatures can be obtained. Moreover, that data can be used to calculate the temperature fluctuation during the complete thermal cycle which

corresponds to the entire load profile. This data can then be used to determine the lifetime in Section 4.5.

4.5. Lifetime Estimation

As mentioned in Section 3.7, this project shall focus on two types of lifetimes - the static lifetime and the Monte Carlo-derived B10 lifetime. As mentioned in the Chapter 3, the lifetime model used in this project's scope will be the CIPS2008 model. This model considers that the primary failure mode for semiconductors is bond wire lift-off .

4.5.1. Static Lifetime

To calculate the static lifetime using the CIPS2008 model, it is important to have the bond wire specifications on hand. As discussed in Section 3.7, the bond wire specifications used for this purpose will be from the same manufacturer as the IGBT. In this case, a Semikron bond wire is selected for calculations. Its specifications have been listed below in Table 4.3 [60].

Table 4.3: Semikron bond wire Characteristics

Parameter	Value
Max Current per Bond Wire Stitch	20A
Diameter of bond wire	500 um

Apart from these values, the voltage class of the IGBT needs to be considered. In this case, it is 12, since the blocking voltage is 1200V. Using these values, the number of cycles to failure for this IGBT was determined to be 99008 cycles. This value can then be used to calculate the damage occurring every year given the number of charge cycles that are occurring in a day. The assumption here is that the same type of car is being charged at the fast charger every time. While this assumption is not entirely realistic, it provides a good base to compare multiple power converters devices. Given the damage occurring in a year for the IGBT (2.16), it can then be used to determine the lifetime in years of the IGBT (2.17).

Furthermore, the lifetime of the IGBT can thus be determined under various conditions. In each of these conditions, a different number of cars is assumed to be charging every day. This would then accordingly reduce the lifetime of the IGBT. The different results can be seen in Figure 4.13. As a baseline, the average will be considered to be 10 cars being charged every day. According to the load profile, this should take about 12 hours which is plausible. Thus, in this case, the static lifetime of the IGBT turns out to be 27.1 years.

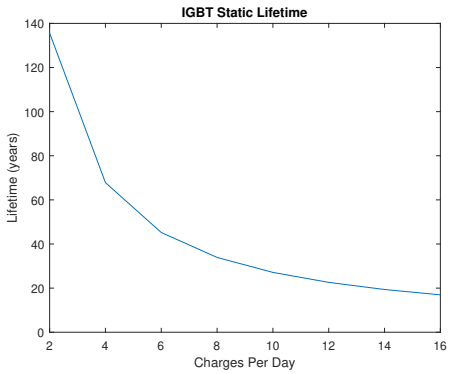
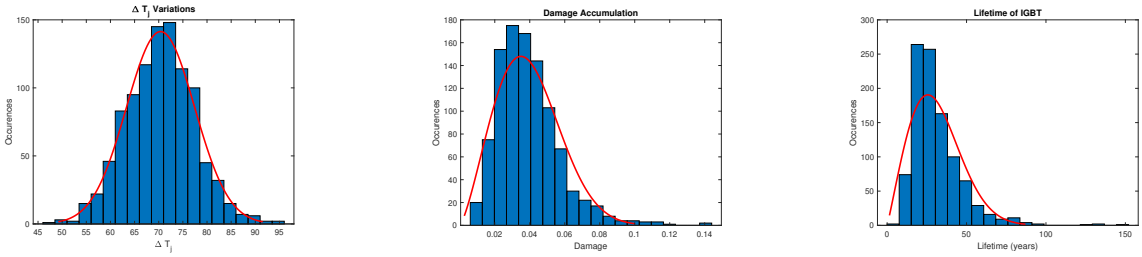


Figure 4.13: IGBT Static Lifetime

4.5.2. B10 lifetime

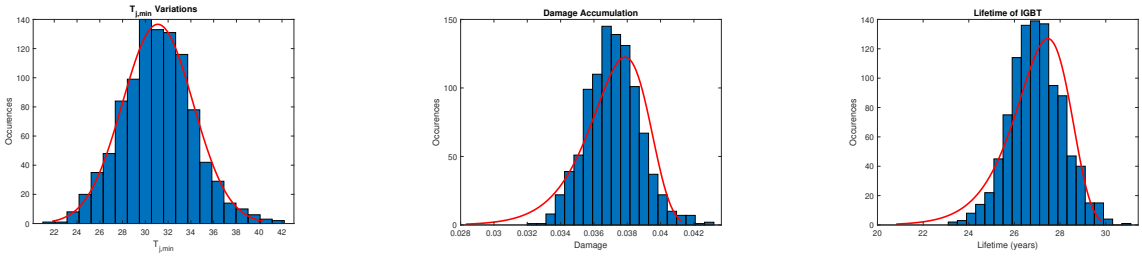
As discussed in Section 3.7, the B10 lifetime is a more realistic estimate of the lifetime of a component as it will take into account discrepancies in different values such as the temperature fluctuation and minimum junction temperature. Changes in both these parameters can be caused by the initial battery SoC and the final battery SoC. For example, if a car comes in with a 20% charge and only charges up to a maximum of 80% to preserve battery lifetime, only 60% of the load profile will be covered. In such cases, the minimum junction temperature can change and so can the temperature fluctuation as a result. Other factors such as the ambient temperature being lower or higher than the standard room temperature considered in the simulations of 25 degrees C or 298K could also affect these parameters that affect the lifetime.

Hence it is important to do this analysis as well. Therefore, a Monte Carlo simulation was performed with a 10% variation from the values derived in Sections 4.4 to calculate the B10 lifetimes. A sample size of 1000 was considered. Finally, the same assumption is being used where 10 cars are being charged in a single day. This can then help calculate the damage and the lifetime in terms of years. The resultant graphs are shown below for each of the following cases.



(a) Junction Temperature Fluctuation **(b)** Damage Accumulation **(c)** Lifetime in Years

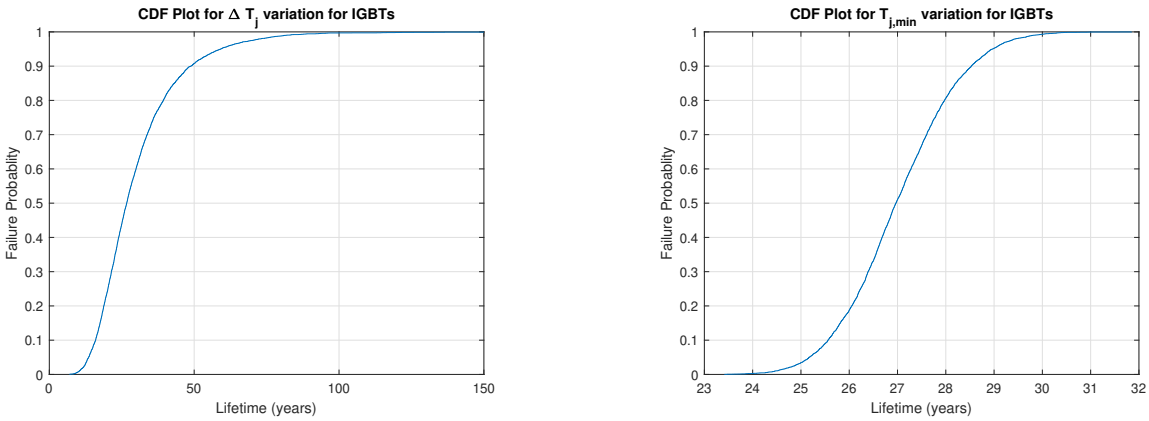
Figure 4.14: Histogram Plots for Variations in IGBT Junction Temperature Fluctuations



(a) Minimum Junction Temperature **(b)** Damage Accumulation **(c)** Lifetime in Years

Figure 4.15: Histogram Plots for Variations in IGBT Minimum Junction Temperatures

Using the graphs derived above and the probability distribution function for the lifetime in years in both cases, a cumulative distribution function can be derived with all the various possibilities adding up. These figures can be seen below in 4.16. The CDF plots thus derived closely resemble the expectations as seen in literature [43] [61] [49]. To derive the B10 lifetime from these graphs, one has to simply identify the 10% failure rate or 0.1 points on the plot. This would give the corresponding B10 lifetime in years on the x-axis.

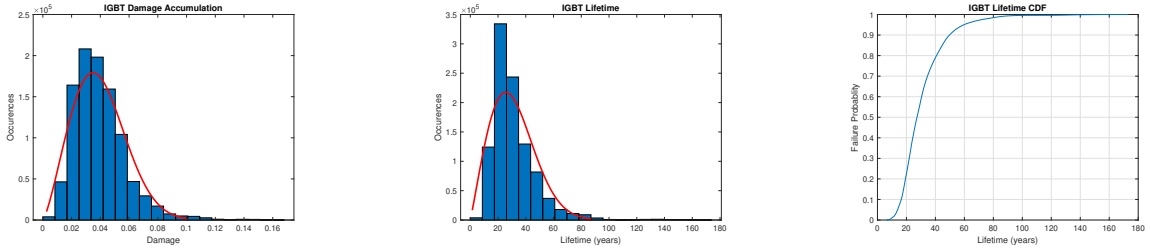


(a) CDF for ΔT_j **(b)** CDF for $T_{j,min}$

Figure 4.16: Cumulative Distributive Function for IGBTs

As one can see, the B10 lifetime derived from the temperature fluctuations results in a lifetime of 16.6 years while that of the minimum junction temperature is about 25.6 years. The difference in the reduction of lifetimes is to do with the exponential constants associated with those variables in the CIPS2008 equation. Thus, the Monte Carlo simulation is also an excellent tool to do a sensitivity analysis of any given model.

While the above cases listed are good ways of performing a sensitivity analysis, in reality, it is not a very realistic case as discussed previously. Thus, it is important not only to vary these two parameters (ΔT_j and $T_{j.min}$) individually but together as well. Thus, the Monte Carlo simulation will be performed again where each change in one of the variables has 1000 corresponding changes in the other variable. This led to a subset of 1,000,000 possibilities. These results have been graphed in Figure 4.17.



(a) Yearly Damage Accumulation **(b)** Lifetime in years **(c)** CDF Plot for IGBTs

Figure 4.17: Histogram Plots for IGBT Monte Carlo Simulation

The B10 lifetime has now changed to 16.5 years. This is practically the same value that is derived from the Monte Carlo Simulations where only ΔT_j was varied. This further shows how sensitive the equation is to a change in the difference of temperatures rather than minimum junction temperature. However, as these graphs represent a more realistic scenario, these data points will thus be used to derive an overall converter lifetime in Section 6.1.

4.6. Summary

In this chapter, the results of the base case scenario of the power converter were discussed. Moreover, the overall PLECS model was validated according to basic current and voltage values, waveforms, power loss values, and even junction temperatures. The latter two are a function of the component being measured and their own thermal circuits. After validation, the thermal profile was used to determine the lifetime of the IGBT in years which gave a result of 27.1 years. This static lifetime derived was then compared to the B10 lifetime derived using Monte Carlo simulations. The B10 lifetime proved to be 16.5 years when both independent variables were changed simultaneously for Monte Carlo simulations.

5

Secondary-Side Diodes Lifetime Estimation

The previous chapter discussed the lifetime of the IGBTs used in the full bridge DC-DC converter. However, this was based on the assumption that the IGBTs were the vulnerable part of the circuit. Another essential part of the power converters is the rectifier diodes used in the secondary side of the transformer. This chapter will focus on the lifetime estimation of the rectifier diodes. The previous chapter verified that the primary circuit is working including the waveforms in sections 4.1 and 4.2 respectively. Since that remains unchanged, there is no need to re-verify those aspects in this chapter. However, it is important to re-verify the power losses of the diode (Section 5.1) and the junction temperatures (Section 5.2) that occur as a result of them. These junction temperatures can then be used to derive the lifetime of the diodes in Section 5.3.

The Diode used for rectification is the DFM200PXM33 rectifier diode from Dynex Semiconductors with a rating of 3300V and 400A [62]. This diode was chosen as it met the requirements of the secondary side of the converter. Some key ratings of this diode can be seen in Table 5.1. This shows that the diode selected for this circuit has a much higher rating than required. However, the supplier had PLECS thermal models which can be used for simulation purposes to derive accurate losses. The internal thermal network provided by the manufacturer also helps generate accurate junction temperature values. Therefore this diode was ultimately chosen.

Table 5.1: Properties of Diode DFM200PXM33 [62]

Property	**Value**
Max. Voltage Drop (V_F)	2.9 V
Max. Current Rating (I_F)	400 A
Max. Reverse Voltage (V_R)	3300V

5.1. Power Losses

The output from the simulations shows that the power losses for all the diodes are more or less identical. Also, like the IGBTs, the power losses closely follow the load profile curve. The reason for this is that the currents passing through them are all the same. Also, the voltage applied across them is the same too at all instances. Moreover, their turn-on and turn-off times are the same. Thus, the switching and conduction losses can be expected to be the same. This can be seen in Figure 5.1. Hence, either one of these diodes can be selected to validate the power losses in all the diodes.

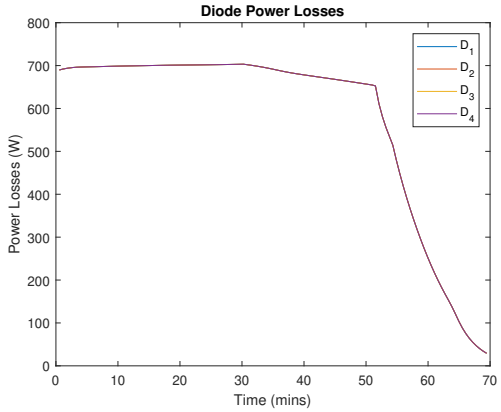


Figure 5.1: Absolute Power Losses of Diodes

In Chapter 2, Section 2.3.2 the power losses of a diode are discussed in brief. However, it is important to understand the power losses mentioned are primarily for a diode under standard operation. In the case of a DC-DC PWM full bridge converter, the rectifier diodes act a bit differently. Instead of the usual on and off stage, there is an additional intermediate stage introduced between them. This occurs when both the switch arms on the primary side are switched off and the current is circulating inside the secondary side of the circuit. At this stage, as discussed in Section 4.2, the current value of the diode is halved. The detailed breakdown can be seen in (5.1).

$$I_F = \begin{cases} I_{out} & \text{for} \quad 0 < t \leq DT_s \\ 0.5I_{out} & \text{for} \quad DT_s < t \leq 0.5T_s \\ 0 & \text{for} \quad 0.5T_s < t \leq (0.5+D)T_s \\ 0.5I_{out} & \text{for} \quad (0.5+D)T_s < t \leq T_s \end{cases} \tag{5.1}$$

Here I_F is the forward current through the diode (A)
I_{out} is the output current to the load (A)
D is the duty cycle of the switch (Which is lower than 0.5*T_s)
T_s is the switching period (s)

To find the conduction losses of the diode it is important to first find the average current through the diode as stated in (2.5). This can be done by using the following formula

$$I_{F,avg} = \frac{1}{T_s}\int_0^{T_s} I_F \, dt \tag{5.2}$$

Using the conditions mentioned in (5.1), the derived value for the average forward current comes out to be -

$$I_{F,avg} = 0.5I_{out} \tag{5.3}$$

While this is a valid result, this average value cannot be used in (2.5) as the forward voltage also changes with the changed current. The variation in current needs to be accounted for. Therefore, the average currents at every time period need to be considered. This leads to (5.4).

$$I_{F,avg} = \begin{cases} DI_{out} & \text{for} \quad 0 < t \leq DT_s \\ (0.5-D)*0.5I_{out} & \text{for} \quad DT_s < t < 0.5T_s \\ (0.5-D)*0.5I_{out} & \text{for} \quad (0.5+D)T_s < t < T_s \end{cases} \tag{5.4}$$

Thus, the forward voltages need to be determined for both these time periods. This leads to the formation of (5.5).

$$P_{cond} = 2(0.5-D)\frac{I_{out}}{2}.V_{F,0.5Iout} + DI_{out}.V_{F,Iout} \tag{5.5}$$

Here $V_{F,Iout}$ is the forward voltage measured at I_{out} (V)
$V_{F,0.5Iout}$ is the forward voltage measured at half the current value or at $0.5I_{out}$ (V)

The first part of the term represents the losses that occur during the secondary side freewheeling period (during the dead time of the switches). Since there are two of them, a factor of 2 is introduced. Moreover, the time duration for this is during the switch-off times for each arm leg. Since each switch arm can be active for a maximum period of half the switching time, the dead time can be calculated as $0.5 - D$. The second term represents the power loss during the time when the opposite switch arm is switched off only. This allows the diode current to reach peak value with the average current hovering around the average output current. It is also important to note while (2.5) shows an ohmic losses term ($I_F^2.R_d$), the diode used in this project does not have an internal resistance listed. Thus, these losses shall be ignored.

For the switching losses, the same (2.6) can be used. However, in the case of the diode used, the reverse recovery time (t_{rr}) has not been mentioned in the datasheet. Thus, another calculation method can be used for this. This is seen in (5.6).

$$P_{sw} = E_{rr}.f_{sw} \tag{5.6}$$

Here E_{rr} is the energy lost during the reverse recovery process (J)

In the case of diodes, the turn-on losses are considered to be negligible. However, there are considerable turn-off or reverse recovery losses. In (5.6), E_{rr} varies with the current passing through the diode and the temperature of the diode. After analysing the waveforms presented in Section 4.2, it is evident that there is a period of dead time before the switch has to completely switch off. As discussed previously, this means, the current levels before turn-off are half that of the average output current. Thus, it is important to interpolate the values of turn-off loss at these half-current values to accurately calculate the switching losses.

The total power loss values can then be calculated by adding the switching and conduction losses as seen in (3.5). These power loss values can then be compared to the power loss values derived from PLECS. Figure 5.2 shows a comparison between these two power loss values - the calculated ones and the simulated ones.

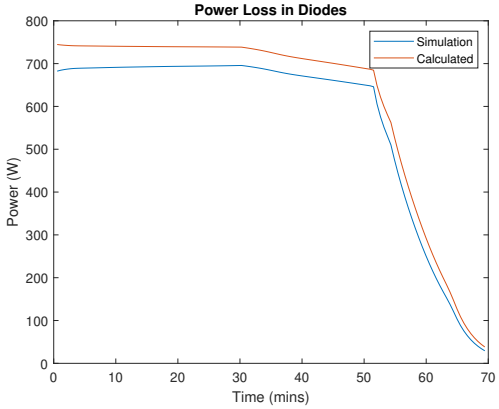


Figure 5.2: Powerloss comparison between simulation and calculations for diodes

There is a slight difference that can be seen between these values. This is mostly because the power loss values have been calculated at a certain assumed temperature. In reality, the power loss values affect the temperatures, which in turn affects the power loss values again. This process goes on until a steady state is reached where the temperature and the power loss values do not change more than a certain number of decimal digits where it is considered to be a steady state system. The difference in most cases of power loss is less than 10% and thus it can be considered that the power loss values determined above are correct for all the diodes.

5.2. Junction Temperatures and their Validation

This section shall discuss the design of a suitable heat sink for the increased power losses of diodes (compared to IGBTs). Once the design of the heatsink is finalised, it can then be used to generate a suitable thermal network for the diodes to help them maintain their junction temperatures below the maximum operating temperatures throughout the load profile. The initial results of the junction temperatures will then be analysed and finally validated with the help of calculations from empirical formulae.

5.2.1. Heat Sink Design

As seen in the previous section, the power loss values for these diodes are much higher than that of IGBTs. Thus, the same thermal network and heatsink used for the IGBTs will not work for the diodes. Therefore, it is important to derive a new required thermal resistance for the heatsink. In this case, it will be assumed that 2 diodes (or only one module) will be mounted to its own heat sink. This will allow for better heat dissipation. A thermal network of such a configuration can be found below. Similar to the case of the IGBTs, in this model, it is assumed that the internal thermal resistance mentioned in the data-sheet is for each diode but the thermal interface resistance is for the entire module. The figure shows the thermal network attached to just one of the heat sinks. In reality, there shall be two of these networks for the entire rectifier side of the converter.

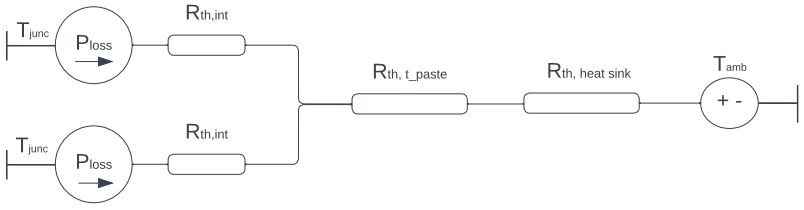


Figure 5.3: Diode Thermal Network for a single module

Again, due to a change in the thermal network, the equation will have to be modified to take this into consideration. This can be seen in (5.7).

$$R_{th,(h-a)} = \frac{T_{j,max} - T_{amb} - 2.P_{loss,max}.R_{th,(c-h)} - P_{loss,max}.R_{th,(j-c)}}{2.P_{loss,max}} \tag{5.7}$$

Here $T_{j,max}$ is maximum operating junction temperature of the Diode (K)
$P_{loss,max}$ is the maximum amount of power loss throughout the load profile (W)
$R_{th,(j-c)}$ is the thermal resistance between the junction and the case (K/W)
$R_{th,(c-h)}$ is the thermal resistance between the junction case the heatsink (K/W)
$R_{th,(h-a)}$ is the thermal resistance between the heatsink and the air or ambient conditions(K/W)

First, an attempt was made to use a lowered maximum allowable junction temperature (110 degrees C) and a higher ambient temperature (40 degrees C) for a robust design. However, this gave thermal resistance values as low as 0.0002 K/W. Such values are very hard to achieve unless liquid cooling is used. But since the IGBTs used a heat sink with forced convection, a similar attempt shall be made here. Then, the maximum operating junction temperature and standard ambient temperature conditions were considered. Substituting these values, one gets a heat sink value of 0.007 K/W. Certain heat sinks from Fischer Elektronik can generate up to 0.01 K/W thermal resistance under forced convection conditions of 5 m/s [63]. Thus, if the airflow is increased slightly above that, 0.007 K/W or even lower can be achieved. Therefore, under that assumption, the heat sink thermal resistance value was chosen to be 0.005 K/W as it would allow the system to stay just below max operating temperature even at maximum loading conditions. A breakdown of the thermal resistances considered is given in Table 5.2.

Table 5.2: Internal and External Thermal Circuit Parameters of Diode

Layer	Thermal Resistance (K/W)
Internal Resistance ($R_{th,(j-c)}$)	0.096
Thermal Paste ($R_{th,(c-h)}$)	0.016
Heat Sink ($R_{th,(h-a)}$)	0.005

5.2.2. Junction Temperature Values and Validation

Similar to Section 4.4, the junction temperatures for the diodes shall be presented and validated in this section. Since the power losses for the diodes are also identical, their junction temperatures should also be similar. As discussed earlier, there are other factors in play here, however, they shall be ignored for simplicity in the scope of this project. Figure 5.4 shows a graph of all the temperatures for the diodes along the load profile. As can be confirmed from the figure, the junction temperature values of all the diodes are the same. Thus, either one of the diodes can be validated by empirical calculations, and it would hold true for all of the diodes. More importantly, it can be seen that the maximum diode junction temperature is just below 125 degrees C (at 121 degrees C). Thus, the heat sink design chosen earlier works for this diode in an ideal scenario.

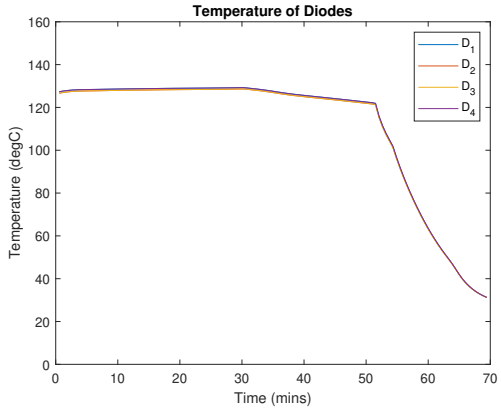


Figure 5.4: Temperature of all the rectifier diodes along the load profile

In Section 3.6.2, the basic formula for determining the junction temperature was discussed if the power loss values and the thermal resistances were given along with thermal capacitances. To reiterate, the values of the thermal capacitance only affect the dynamics of the system but not the temperature at a steady state. Thus, for steady-state calculations, the capacitances can be ignored. Therefore, due to the modification of the thermal network, (5.8) can be used to determine the junction temperature of each diode.

$$T_j = (2.P_{loss}.(R_{th,(h-a)} + R_{th,(c-h)}) + T_{amb}) + (P_{loss}.R_{th,(j-c)}) \tag{5.8}$$

Using this equation and the profile of the power losses, the calculated temperature profile can be determined. Figure 5.5 shows the difference between calculated and simulated temperature profile values.

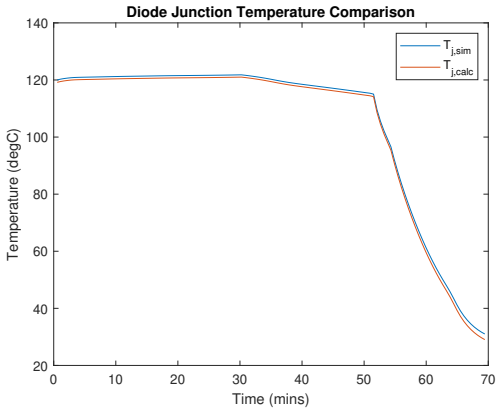


Figure 5.5: Diode Junction Temperature Comparison Between Simulation and Calculations

The slight discrepancy observed in the numbers is due to the fluctuation of temperature of a few degrees Celsius. This occurs due to the cycling nature of the switches and the diodes being turned on and off. This fluctuation can be reduced by simply increasing the size of capacitances. However, that would increase the time constant and thus the time taken to reach a steady state by a lot. In percentage terms, this fluctuation is less than 5% initially. However, since the fluctuation temperature is constant, at low temperatures (near low power loss values), the percentage difference increases as the absolute value in temperature difference remains the same. Therefore, the thermal network can also be considered validated for the diode and either of the temperature profiles can be used for determining the lifetime of the diode.

5.3. Lifetime Estimation

This section will look into the lifetime estimation of the diode using the thermal profile derived from PLECS. Again, even in this case, two forms of lifetimes will be considered. The static lifetime and the Monte Carlo B10 lifetime. Like with the IGBTs, there will be two variables whose effect on the lifetime will be observed - ΔT_j and $T_{j,min}$. These will first be varied individually and then together to see the combined effect on the lifetime.

5.3.1. Static Lifetime

First, the static lifetime will be determined based on the CIPS2008 formula again. In this case it will be assumed that the bond wire used for the diode is also the Semikron bon wire [60]. Thus, the wire ratings can be taken from Table 4.3 as well. An important thing to note though is that the voltage class in this case (V) in this case is much higher as the blocking voltage is much higher too. Here, it is assumed to be 33 as the blocking voltage of the diode is 3300V. For the case of the static lifetime, it will again be assumed that the same car charges at the station with the same load profile. Varying the number of times the car charges at the spot daily, the accumulated damage (2.16) and hence the lifetime in years (2.17) can be determined. This leads to the graph as can be seen in Figure 5.6

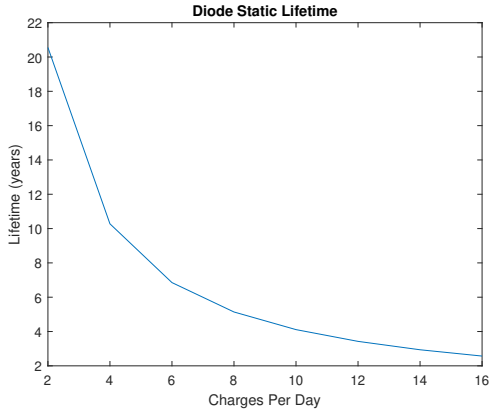


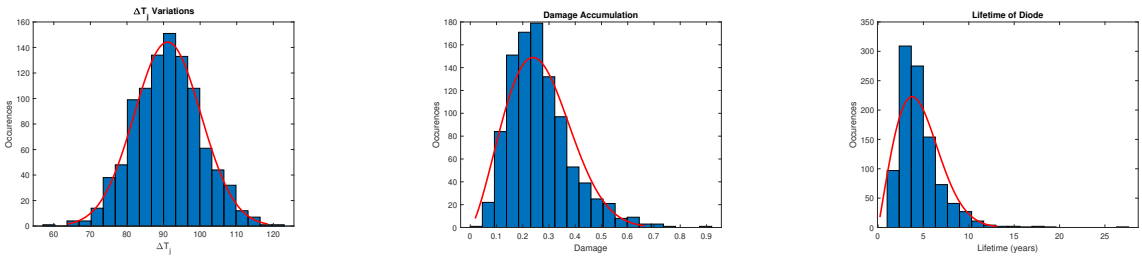
Figure 5.6: Diode Static Lifetime

The graph shows that assuming a total number of 10 charges per day, the lifetime is around 4.11 years. This is much lower than the IGBT and thus it can be stated that the rectifier diode (in this circuit) is the vulnerable component. It will thus be limiting the lifetime of the overall converter.

5.3.2. B10 Lifetime

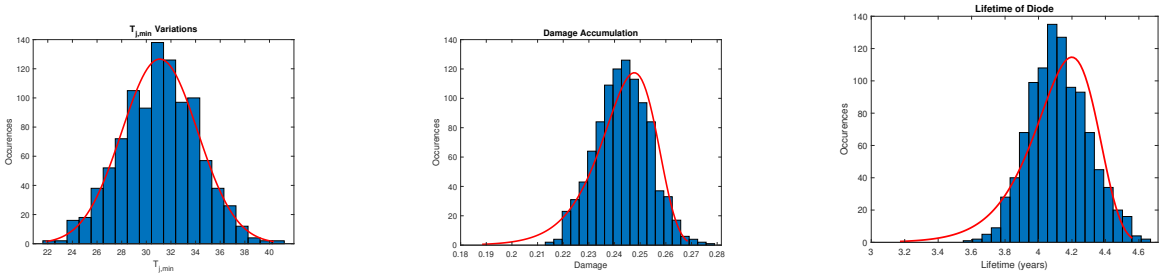
Now that the static lifetime values are known, it is also important to see how sensitive this lifetime is to a change in variables. Namely, the junction temperature fluctuation and change in minimum junction temperature shall be checked. It is important to note that each of these variables will be modified one at a time. However, in a real-life scenario, there is a high chance that a change in one of the variables will often result in a change in the other variable too. This has been illustrated before in Section 4.5.2 with the example of a charging car.

A similar process will be followed as it was performed for IGBTs. There would be 1000 variations taken within a normal distribution of the values achieved in the previous section with a 10% variance. These temperature values will then be used to calculate the accumulated damages and overall lifetime in years using (2.16) and (2.17) respectively. The results of these Monte Carlo simulations can be seen in Figures 5.7 and 5.8.



(a) Junction Temperature Fluctuation **(b)** Damage Accumulation **(c)** Lifetime in Years

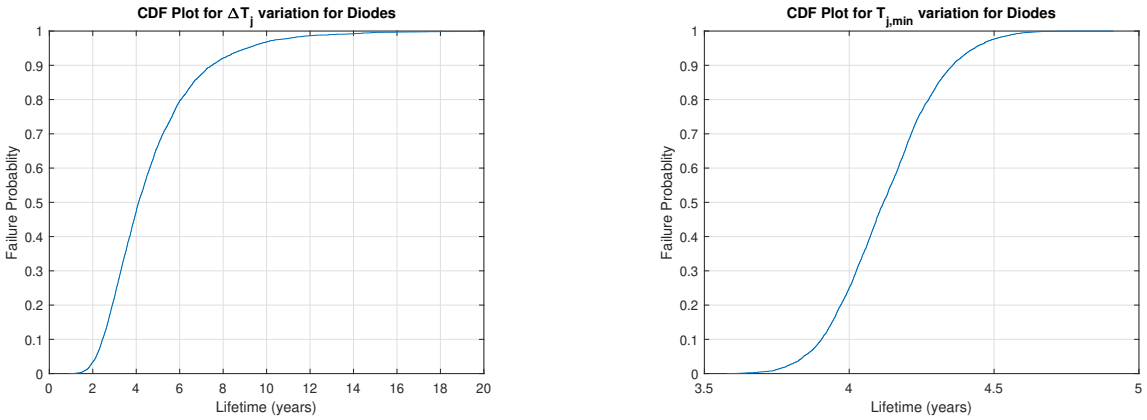
Figure 5.7: Histogram Plots for Variations in Diode Junction Temperature Fluctuations



(a) Minimum Junction Temperature **(b)** Damage Accumulation **(c)** Lifetime in Years

Figure 5.8: Histogram Plots for Variations in Diode Minimum Junction Temperatures

Using the graphs derived above and the probability distribution function for the lifetime in years in both cases, a Cumulative Distribution Function (CDF) can be derived with all the various possibilities adding up. These figures can be seen below. To derive the B10 lifetime from these graphs, one has to simply identify the 10% failure rate or 0.1 point on the plot. This would give the corresponding B10 lifetime in years on the x-axis.

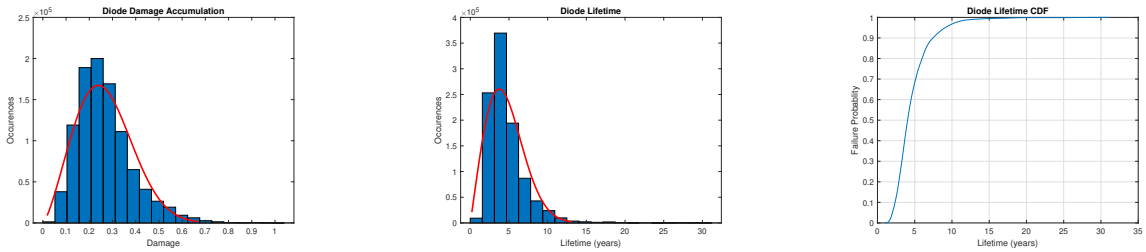


(a) CDF for ΔT_j **(b)** CDF for $T_{j,min}$

Figure 5.9: Cumulative Distributive Function for Diodes

As one can see, the B10 lifetime derived from the temperature fluctuations results in a lifetime of 2.3 years while that of the minimum junction temperature is about 3.8 years. The difference in the reduction of lifetimes is to do with the exponential constants associated with these independent variables in the CIPS2008 equation. Similar to the case of the IGBTs, it shows that the CIPS08 equation is more sensitive to a change in the difference between maximum and minimum temperatures in the cycle than changes in the minimum junction temperatures.

Once this was determined, it was important to also see the effect of varying both these parameters together and then calculate the B10 lifetime. Thus, multiplying both the variations with each other, a superset of 1,000,000 data points was achieved which was then used to calculate the B10 lifetime. The resultant graphs from the Monte Carlo Simulation can be seen in 5.10.



(a) Damage Accumulation **(b)** Lifetime in years **(c)** Lifetime in Years

Figure 5.10: Histogram Plots for Diode Monte Carlo Simulation

From the CDF graph in Figure 5.10c, it can be seen that the B10 lifetime, in this case, is 2.3 years. Again showing that the model is very sensitive to changes in temperature fluctuations over the load profile as this value is closer to the value determined previously for ΔT_j fluctuations.

5.4. Summary

This chapter focused on validating the diode's power loss model and thermal model. Once validated, it then discussed the lifetime estimation of this diode. As seen in the case with IGBTs in Chapter 4, the diode's static lifetime and B10 lifetime were calculated. The static lifetime of the diode was calculated to be 4.1 years whereas the B10 lifetime changed depending on which variable was being varied. In the case where the temperature swing of the diode was varied, a lifetime of 2.3 years was achieved. Whereas while varying the minimum junction temperature, the lifetime was estimated to be 3.8 years. When both the variables were varied simultaneously, the lifetime was found to be 2.3 years, closer to the temperature swing variation. Thus proving once again that the temperature swing exerts a significant influence on the lifetime of a component. The next chapter will now attempt to calculate the lifetime of the overall converter, and possibly improve it.

6

Converter Lifetime

In chapters 4 and 5, the lifetimes of individual components were discussed. However, when these components are combined in a system, they interact with each other thus affecting the overall system reliability. This chapter shall thus look into the overall converter lifetime. Initially, the converter lifetime will be measured considering that the IGBT and the diode discussed in the previous chapters are used in Section 6.1. Then, in Section 6.2, an attempt will be made to improve the lifetime of the converter by changing the diode to one with lower losses.

6.1. Original Converter Lifetime

The previous chapters discussed the possible lifetimes of the diodes and IGBTs under different circumstances. However, the objective of this thesis is to determine the lifetime of the entire converter. The simplest way to look at it would be to focus on the more vulnerable component in the circuit. In this case, it was found to be the diode. That would mean that the lifetime of the converter would be limited to about 2.3 years. However, in a system, the diodes and the IGBTs interact with each other. Thus, the combined lifetime of the entire converter is something that needs to be taken into account.

Therefore, to find the lifetime of the converter the reliability body diagram method will be used. A Reliability Body Diagram (RBD) is created to see how components interact with each other to change the system's reliability. In all the cases, the standard assumption that 10 cars are being charged in a day will be considered. A reliability body diagram is something that is often used in the world of reliability analysis. It is especially useful if the reliability of a system needs to be calculated which has multiple components in the system. In this technique, a flow chart is made where it is tracked how one component affects the other one. Then the reliabilities are calculated at different points and depending on the RBD, the system reliability can be calculated. This is explained more in detail in Section 2.6.

The Reliability Body Diagram (RBD) for this converter has been shown in Figure 6.1. It is to be noted that this RBD contains only the IGBTs and the rectifier diodes. In a practical scenario, one should consider all the components present in the circuit, including any redundancies that are built in. For this purpose, it has been assumed that all the IGBTs are connected in series while the diodes are also connected in series with them. This assumption is being made because if one of the IGBTs stops functioning, the entire system fails unless the modulation is changed significantly. Similarly, if one of the diodes stops functioning, then the system may not work properly and thus the entire converter is affected.

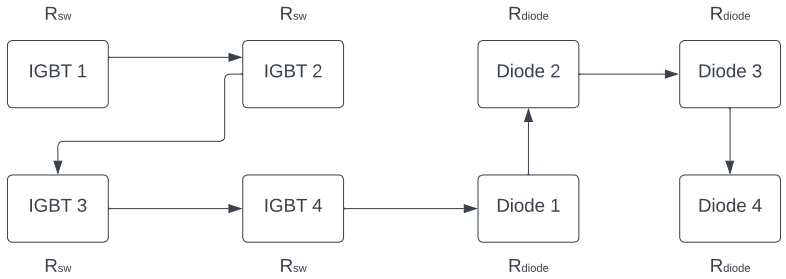


Figure 6.1: Reliability Body Diagram for the Converter

More research is required into the level and mode of failure of the IGBTs and the diodes and how the system can continue functioning in a robust manner despite such shortcomings. However, that will require feedback loops and the consideration of multiple scenarios and has thus been excluded from the scope of this project. Therefore, given the assumption that each of the components is critical to the system's functions, the reliability of the system can be derived using (6.1).

$$.R_{sys} = R_{IGBT}^4 . R_{diode}^4 \tag{6.1}$$

Here R_{IGBT} is the reliability of the IGBT at determined at a particular time period
Here R_{diode} is the reliability of the Diode at determined at a particular time period

Therefore the reliability of the entire system can be calculated. However, it is first important to calculate the reliability function of the respective components. This can be done by observing the lifetime graphs shown in previous sections. In this case, the lifetime follows a Weibull distribution as also observed in the literature. The reliability of a product following the Weibull distribution is given by (6.2).

$$R = e^{-\left(\frac{t}{\theta}\right)^{\beta}} \tag{6.2}$$

Where θ is the scale factor of the distribution
β is the shape factor
t is the time at which the reliability is being measured.

The terms θ and β are determined from the lifetime curve of the diodes and IGBTs individually. They are then fed into the reliability formula shown in (6.2) to create the reliability functions R_{IGBT} and R_{diode} respectively. These functions were fed back into (6.1) to generate a system-level reliability curve. This can then be used to plot a graph similar to CDF with the unreliability and the lifetime in years as seen in Figure 6.2.

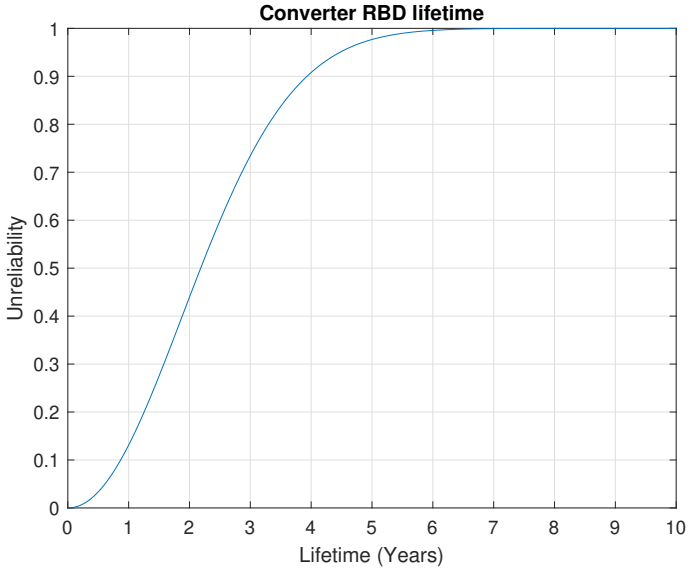


Figure 6.2: Resultant RBD Cumulative Distribution Function

Then the B10 lifetime can be determined again from this graph by identifying the point of lifetime where the overall converter reliability is 0.9 or the failure rate is 0.1. In this case, it is identified to be 0.86 years. While this is quite low, it is expected as the B10 lifetime of the converter would be limited by the diode whose B10 lifetime is around 2.3 years. Thus the addition of more such diodes leads to a decrease in lifetime.

6.2. Changing The Diode

The previous sections determined the lifetime of the converter considering that all the components (semiconductors) were connected in series. That is, if either of the components stopped working then the whole converter will stop working. It was observed that though the IGBT had a B10 lifetime of 16.5 years, and the Diode had a B10 lifetime of 2.3 years, the overall converter had a lifetime of only 0.86 years with a reliability of 0.9. This is quite low when compared to the lifetime of a car. Thus, it was clearly seen that the bottleneck or the heart of the issue was the low lifetime of the diode.

The reason for the low lifetimes of the diode wasn't the external thermal circuits but the high power losses and internal thermal resistances that cannot be altered after selecting the module. As seen before in earlier sections, it is hard to reduce the thermal resistance of the heatsink further without delving into the territory of liquid cooling. Hence, it can be concluded that the external thermal circuit has reached the limit of its capabilities to remove heat. Thus, one of the only solutions to improve the diode lifetime (and thereby the entire converter) is to change the diode. This will have two benefits. Firstly a diode with a lower internal thermal resistance can be selected. Secondly, the diode characteristics can be chosen such that the losses are minimised.

As seen in Chapter 5, the reason for the high losses on the side of the diode was the high reverse recovery current (leading to high switching losses) and high forward voltage (leading to high conduction losses). In retrospect, one of the reasons such a diode was chosen was because the PLECS model of that diode was readily available. However, that cannot be a limitation when choosing a component for design purposes. In Section 5.1 when the diode power losses were validated using the equations, it can also be stated that PLECS models validated that the theoretical empirical formulae used closely resembled the practical scenarios. Therefore, the same theoretical calculations can be used to calculate the losses of a diode that has a detailed datasheet but not a PLECS thermal model. As it was noted earlier, there were slight deviations between the simulated power losses and the calculated power losses. This might lead to further discrepancies when the temperature is calculated. However, it should be noted that ultimately a Monte Carlo simulation will be carried out where the temperature values will be varied

to get a better picture of the randomisation of events occurring in real life. Therefore, the simulation will cover a range of possibilities that could have been the temperature swing or minimum temperature had the actual thermal model been used in the simulation.

Therefore to improve the lifetime of the converter, the following process will be followed. First, a number of alternative diodes will be looked into that match the requirements of the secondary side of the converter. In this case, it is a minimum of 480V and a current rating of 150A. While in reality, the current required might be lowered since the RMS current is what damages the component. However, to be on the safer side, an average of 150A is assumed while choosing new diodes. Similarly, considering a small factor of safety, the minimum blocking voltage explored would be 600V and not 480V.

When new diodes are chosen, the power losses will be calculated from the parameters given in the datasheet. However, the junction temperature also depends on the internal (and external interface) thermal resistance. Therefore, once the losses are calculated, their junction temperatures will also be derived. Thereafter, the diodes with the lowest junction temperature swing and minimum junction temperature will be considered for further calculations. However, priority will be given to the junction temperature swing value as it was seen before in Section 4.5.2 that the lifetime is more sensitive to the junction temperature swing rather than the minimum junction temperature.

The lifetime of this diode will then be calculated using the Monte Carlo method and compared with the lifetime of the previously selected diode in Chapter 5.

6.2.1. Choosing the Diodes

As mentioned above, the first step was to select the necessary diodes that could substitute the existing ones. In this case, it was not important for the diode to have an existing PLECS model. However, their datasheets need some key information like the peak reverse recovery current (I_{RRM}) and the reverse recovery time (t_{rr}). This information is crucial for calculating the switching losses.

Another important piece of information required was a graph between the voltage drop (V_F) versus the current applied (I_F). This graph is important in determining the conduction losses of the diode. Fortunately, most of the data sheets have this information present in them. Using these criteria, three diodes were selected from DigiKey [64]. A summary of their attributes has been mentioned in Table 6.1. Their properties have been compared with the existing Dynex diode used in the base case.

Table 6.1: Diode Loss and Thermal Properties

Part Number	MF300K06F3 [65]	DSEK300-06A [66]	VS-UFB250FA60 [67]	DFM200PXM33-F000 [62]
Manufacturer	MCC	IXYS	Vishay Semiconductors	Dynex
Max Blocking Voltage (V)	600	600	600	3300
Average Forward Current (A)	150	150	168	200
Max Forward Voltage Drop (V)	1.4	1.4	1.19	3
Peak Reverse Recovery Current (A)	22	50	64	160
Reverse Recovery Time (ns)	220 (I_F = 150A; T_j = 125 C; V_R = 300V)	180 (I_F = 150A; T_j = 125 C; V_R = 300V)	291 (I_F = 50A; T_j = 150 C; V_R = 200V)	1562 (I_F = 200A; T_j = 125 C; V_R = 1800V)
Max Operating Temperature (degC)	150	150	175	125
Thermal Resistance (J-C) (K/W)	0.06	0.2	0.215	0.096
Thermal Resistance (C-H) (K/W)	-	0.1	0.05	0.016

6.2.2. Power Loss and Junction Temperature Calculations

In Section 2.3, the switching losses were calculated using the graphs or lookup tables provided by the thermal model of the component. However, in this case, a lookup table is not available for the switching losses, and neither is a graph. Therefore the method to calculate the switching losses needs to be changed slightly. In this instance, (2.6) can be used. Although, in this equation, the reverse recovery

time (t_{rr}) changes with the current applied. Since the value given in the data-sheet is presented at specific test conditions, it is important to apply a scaling factor that helps determine the correct switching losses at that load point. Therefore the equation can be modified into (6.3). This equation has been further validated in Appendix B.

$$P_{sw} = \frac{1}{2} I_{RRM} V_R t_{rr} . \frac{I_F}{I_{ref}} \tag{6.3}$$

Here I_{RRM} is the maximum reverse recovery current (A)
V_R is the blocking voltage (V)
t_{rr} is the reverse recovery time (s)
I_F is the forward current through the diode (A)
I_{ref} is the forward current at which the reverse recovery time was measured (A)

Therefore the switching losses can be calculated by using those parameters. These parameters for the selected diodes have been listed in Table 6.1. While the scaling factor only provides an approximation, as discussed earlier, the Monte Carlo simulation conducted later on should take care of the discrepancies. On the other hand, for the conduction losses, the forward current versus forward voltage graph can be used to accurately determine the conduction losses.

One limitation of this method is that it does not take into account the fluctuation of parameters like reverse recovery time and forward voltage drop with respect to junction temperature. As the general temperature levels of the diode are known to be around 100 degrees C, the upper bound data will be used from the datasheets. While this value may not be valid for lower currents (where the junction temperature is much lower), it is important to note that the lifetime calculation is highly dependent on the max temperature achieved during the load cycle. This is achieved during the high current part of the load cycle where the junction temperatures are much closer to the upper bound mentioned in the data sheets and thus closer to the accurate values. This is why this method can be considered to be a suitable approximation of the power losses derived. Using this data, the power losses at different points in the load profile were derived and compared to the base case. This can be seen in Figure 6.3.

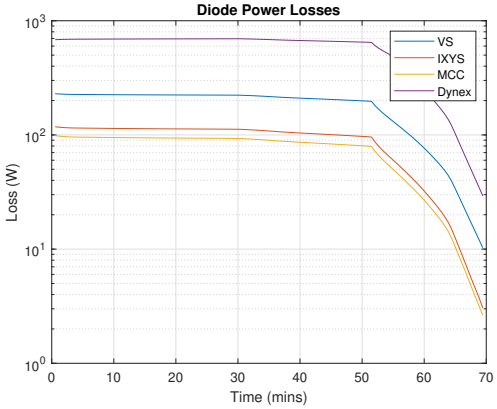


Figure 6.3: Losses of all Rectifier Diodes

As expected, all three new diodes chosen exhibit lower power losses compared to the base case diode (Dynex). The losses derived above can then be used to calculate the junction temperature of the diodes. The method to calculate the junction temperature will remain unchanged from the previous sections because the diodes currently being considered are also two-diode modules. Thus, the thermal network design for each of them will be the same. Therefore, the only thing changing would be the internal thermal resistance of the diodes and the thermal interface resistances. These have also been mentioned in Table 6.1. The heat sink for this purpose will be kept the same for a fair comparison with the diodes

used in the base case.

Using the data given in the table, and the losses determined earlier, the calculated temperature profiles of the different diodes can be seen in Figure 6.4. The temperature profile of the base case is also included in this graph.

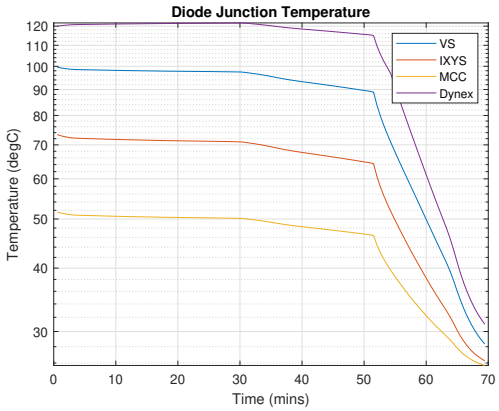


Figure 6.4: Junction Temperatures of all the rectifier diodes

As can be seen from the figure, the MCC and IXYS diodes show the lowest swing in junction temperature. This was expected due to both of them having lower losses as observed previously in Figure 6.3. The MCC diode in particular had even lower power losses (due to a lower I_{RRM}) and also a lower internal thermal resistance. Therefore it performed the best. However, even the VS diode performed significantly better than the Dynex diode in terms of junction temperature swings. Hence, all three diodes will be considered for further lifetime estimation calculation including the overall converter lifetime. It is expected that the lifetimes of the individual diodes would follow a similar trend since all of them have the same voltage class. Moreover, it is assumed that all the diodes are using the same bond wire.

6.2.3. New Diodes Lifetime Estimation

This section shall explore the lifetime estimation of the diodes chosen in the previous section. To do so, the B10 lifetime of the respective diodes will be calculated directly while varying the temperature swing values and the minimum junction temperature values simultaneously as previously performed in Section 5.3.2. Again, the same assumption shall be made that 10 cars are being charged in a day. This assumption will be used to calculate the damage to the diode and the lifetime of it in years. The CDF graph for these diodes along with the base case Dynex Diode is seen in Figure 6.5.

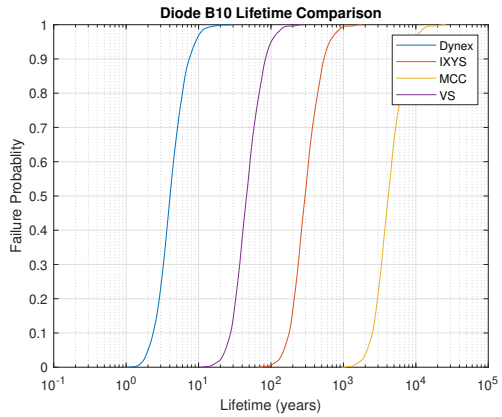


Figure 6.5: CDF of all four diodes

The CDF plot shows a large difference in the lifetime of the three didoes being considered. Firstly, the Dynex diode which was originally considered seems to have only 2.3 years as the B10 lifetime. The VS diode performs slightly better than that with a B10 lifetime of 27 years. This value is quite close to the value of the IGBT B10 lifetime derived in Section 4.5.2. On the other hand, the IXYS diode shows a much higher B10 lifetime of 177 years. Finally, the MCC diode is more than a magnitude higher at 2512 years of B10 lifetime. This can be attributed to the very low-temperature fluctuation at the junction. Clearly, both these systems (IXYS and MCC) can be modified to use more compact heatsinks that don't need forced convection.

6.2.4. Revised Converter Lifetime

The overall lifetime of the converter will be calculated using the RBD method. This is because it provides the most holistic approach to calculating the lifetime of a system and determining its reliability at a given point in time. In the case of the new diode, the RBD remains unchanged (Figure 6.1). Therefore, the equation to calculate the system reliability (6.1) also remains unchanged. The only things to be changed are the shape and scale factors in (6.2) for the diode as the Monte Carlo method generated different data sets for the diodes under consideration. Thus, once this is calculated, the unreliability graph can be generated for the new diodes. A comparison has been made with the old diode too. This is seen in Figure 6.6.

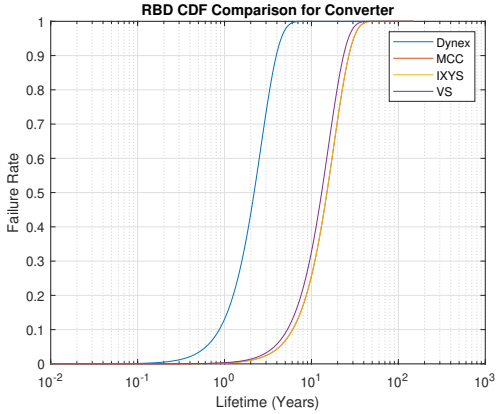


Figure 6.6: RBD CDF of the Overall Converter for all cases

There is a distinct difference spotted between the CDFs of the new diodes and that of the Dynex diode. However, there is very little difference between the new ones. While there is a small difference between the VS diode and that of IXYS and MCC, there is practically no difference between the IXYS converter lifetime and the MCC converter lifetime. Numerically, the B10 lifetime of the converter with the IXYS diode is 6.06 years and that of the MCC diode is 6.08 years. THE VS diode is slightly lower with 5.3 years. While these values are much higher than the lifetime with the Dynex Diode (0.86 years), they are much lower than the B10 lifetimes of their own respective diodes estimated earlier. This shows that at this point when the diode lifetime exceeds a certain threshold, the limiting factor then becomes the IGBT. Therefore, the lifetime of the entire converter is now limited by the IGBT and not the Diode as seen earlier.

This process can be repeated multiple times, where the vulnerable part of the system (either the diode or the IGBT) is replaced with a better one till an optimal lifetime of the converter is reached. However, the scope of this project was not to design an optimal converter for a DCFC. It was to determine the lifetime of the DCFC and explore if it can be improved to a certain extent. Both of these objectives have been met thus far. Therefore, the lifetime of the converter (and therefore the DCFC) in this case can be determined to be around 6 years. Till this point in time, 90% reliability is assured. This means that either 10% of the population of certain converters will fail by this time, or there is a 10% chance that a particular converter (or DCFC) will fail within 6 years.

6.3. Summary

This chapter discussed the overall converter's lifetime under two scenarios. In one scenario, the original diode was used. While in the other scenario, new diodes were explored and their effect on the lifetime was observed. It was seen that with the old diode, the B10 lifetime (using the RBD method) of the entire converter was only around 0.86 years. In this case, the low lifetime of the diode limited the converter's lifetime. However, when new diodes with lower losses were used in place of the old ones, then the B10 lifetime of the converter jumped to around 5-6 years irrespective of the diode. This was because, with the higher lifetime of the new diodes, the limiting factor in the converter's lifetime was now the IGBT. To further increase the overall lifetime of the converter, the IGBTs can also be switched out for ones which have lower losses.

7

Conclusion and Future Work

This chapter shall discuss the conclusions determined from the simulations conducted in the scope of this project. First, a brief conclusion will be discussed in Section 7.1. This will be in regard to the main research question posed at the beginning - the lifetime of the charger. Then in Section 7.2 the answers to the sub-questions will be discussed that were set out as the research objectives of this project. Finally, Section 7.3 goes over some of the future recommendations for research on this topic.

7.1. Conclusions

As stated in the beginning, this thesis aimed to estimate the lifetime of a DC Fast Charger based on the lifetime of the power converters inside them. Therefore, first, a study was performed about the types of power converters used in DC Fast chargers, their advantages and disadvantages. The lifetime of these power converters is in turn dependent on the lifetime of the components present inside them. Hence, it was important to determine the type, topology, and components of the power converter being studied. Moreover, research was conducted into the types of failures that can occur in semiconductor devices. Different lifetime models that took various failure modes into consideration were also studied. This information was presented in Chapter 2.

This thesis considered the DC-DC converter of an off-board DC Fast Charger, particularly one that used a full bridge converter topology. This converter was then modelled in PLECS and validated to prove that the simulated model works according to expectations in various scenarios. This model was validated using a multi-faceted approach as seen in Chapter 4. The effect of a load profile on various components inside the power converter like the IGBTs and the diodes (Chapter 5) was studied. Their power losses were measured and then used to design suitable heat sinks. With these simulations, the junction temperature variations could be measured. Finally, using the junction temperature variation data, the lifetime of the diodes and the IGBTs were calculated. These lifetimes could then be used to derive the overall lifetime of the converter (Chapter 6). At the same time, the reliability of the converter could be determined at different periods of time. The results are as follows -

- The B10 lifetime of the IGBT is 16.5 years considering 10 cars are being charged in a day.
- Under similar conditions, the B10 lifetime of the diode was found to be 2.3 years.
- Using the RBD method, the B10 lifetime of the converter was revealed to be 0.86 years with the Dynex diode.
- Changing the diode, it was found that the overall converter's B10 lifetime can be increased to 5-6 years depending on the choice of the diode.

Thus, the DC Fast charger is expected to last around 5-6 years with a 90% reliability given that 10 cars similar to the load profile considered are charged every day. It is important to note that this is only considering the DC-DC converter as the one that will fail and not the AC-DC rectifier. Moreover, this lifetime and reliability are specifically for this type of load profile, the semiconductor devices considered, and the topology they are used in. For other types of converters and devices, Section 7.3 explains a robust method to calculate this.

Another important thing to note is that the lifetime of 5-6 years mentioned above is the point of time at which any of the 8 components used in the topology (either diodes or IGBTs) is expected to fail. Rather, there is a 10% chance that either of these parts fails. Therefore, this does not indicate the absolute end of life of the converter but rather the time at which a single component may need to be replaced. Therefore, the lifetime of 5-6 years indicated the time at which some breakdown maintenance may be required for the DCFC.

7.2. Answers to Research Sub-Questions

This section will answer the sub-research questions that were set out when the thesis was started.

What kind of power converter topologies are used in DC Fast Chargers and how do they differ?

It was found in the course of this thesis that there are two main types of power converters used in DC Fast chargers. These are AC-DC converters and DC-DC converters.

There are several possible topologies for each of these converters. The main topologies used for the AC-DC rectifiers were the Swiss and Vienna rectifiers. However, other topologies such as the three-phase buck or the three-phase boost converters are also used in some applications as they provide the added benefit of stepping up or down the voltage a step before it reaches the DC-DC converter.

The DC-DC converters used in fast chargers are mostly of the Full Bridge or the Dual Active Bridge type. The main difference between these converters is the presence of diodes or switches on the secondary side of the converter. Additionally, resonant tanks (with capacitors and inductors) can be added to the topology to introduce new modulation strategies and improve the overall efficiency of the converters.

For the purpose of this thesis, the focus was on the DC-DC converter that uses a full bridge topology without a resonant tank for the purpose of simplicity.

How to simulate a power converter which can meet the requirements of the EV charger and verify the working of such a model?

This project considered various methods to simulate the power converter. One of the first methods attempted was to simulate the model in MATLAB Simulink. However, the simulations were time-consuming and prone to some simulation errors. Therefore, PLECS by PLEXIM was considered. This removed the simulation errors and also sped up the simulation by a lot. However, PLECS interface was unfamiliar and also didn't allow similar customization as MATLAB and Simulink. Fortunately, PLECS was cross-compatible with MATLAB and thus a hybrid mode called PLECS Blockset was used. This allowed the circuit to be simulated in the PLECS environment while the input and output were controlled by MATLAB/Simulink. The output then could be fed back to MATLAB to perform Monte Carlo Analysis, determine lifetimes, and generate neat graphs automatically.

The verification was performed with a multi-pronged approach. It can be seen in detail in Chapter 4. In short, first an initial comparison was made to see if the output voltage and current followed the voltage and current of the load profile. Next waveforms were compared with the literature to see if they followed the expected values. After this, the power loss values were compared from the simulation to empirical formulae from the literature. This was done to verify the semiconductor model being used by the simulation. Finally, the thermal network was validated by deriving the expected junction temperatures given the power losses and comparing them with the temperatures derived from the simulation.

What are the power losses that are occurring in the semiconductor devices in the power converter? Are they uniform?

There are multiple devices in the circuit where power may be lost in the circuit. These include capacitors, inductors, resistors, transformers, and other semiconductor devices. As seen in the literature

survey, semiconductors are prone to failure in power converters and thus they were focused on for this thesis. Other components were considered to be ideal in this case.

There are two main types of power losses occurring in semiconductors. These are the switching losses and the conduction losses. Gate losses may also play a part, however, they depend a lot on the gate driver used and thus were not considered within the scope of this thesis. Even switching losses can be further divided into turn-on and turn-off losses. However, the turn-on losses of the diode are negligible and thus neglected usually. For the IGBTs, both the switching losses (turn-on and turn-off) and the conduction losses are considered.

The switching losses depend on the switching frequency used in the circuit. The conduction losses on the other hand depend on the duty cycle of the switch. Since the current passing through the IGBTs and the diodes differ, the losses observed in them are different. Moreover, the on-times of both these devices are also different as seen in Section 4.2. Overall, the switching losses account for anywhere from 65% to 75% of the total losses occurring in the device. This depends on the load (the output voltage and current required).

How to model the thermal network of a power module and how this thermal network affects the junction temperature?

There are primarily two parts to the thermal network for any of the power devices used in the model. They are the internal thermal network and the external thermal network. The internal thermal network depends on the materials used to make the diode/IGBT and the other materials present inside the casing including the baseplate and substrate amongst others. Everything between the case and the junction. A cross-section of this can be seen in Figure 2.10. The external network on the other hand consists of the thermal paste and the heat sink.

The internal thermal network is generally modelled either as a Cauer or Foster network which is a set of thermal resistances and capacitances (or time constants) in series. They help determine the dynamic behaviour of the device when heated. This information is generally available on the data sheets of the devices. The external model can be added easily in PLECS via a series of thermal resistances and capacitances as well. This can also be added directly to the PLECS semiconductor model if the thermal file requires it. Finally, the heat sink can be modelled simply as a thermal resistance as it interacts with the air.

The thermal network does in fact affect the losses in the system. Primarily, the thermal network affects the junction temperature. However, the voltage drop across the semiconductor is generally a function of temperature. Moreover, the rise and fall times of the current also depend on the temperature of the device. Hence, both the switching and the conduction losses depend on the junction temperature. Thus, when the power losses increase, the junction temperatures increase with them. These increased device temperatures increase the losses occurring in the system by increasing the respective parameters as well. Therefore this leads to cyclic nature where the power losses and the junction temperature finally stabilize at a point where there is minimal change after every iteration in the calculation.

How does the junction temperature affect the cycles to failure and the damage occurring to the device?

The cyclic change in junction temperature causes thermo-mechanical stress inside the devices. This is because the power devices are made up of many different materials. Each of these materials has its own CTE (Coefficient of Thermal Expansion). Therefore some layers expand more than others. This leads to internal stresses in the devices leading to multiple failure modes. The mode of failure considered in this thesis for the semiconductor devices is that of bond-wire lift-off and solder fatigue/crack. A crack in the solder also leads to an increase in thermal resistance, thereby increasing junction temperatures and accelerating failure mechanisms.

The lifetime estimation method used in this project is the CIPS2008 model developed by Bayerer et al.

This equation is an empirical model developed after collecting reliability test data from several converters. It considers bond wire lift-off and solder fatigue as one of the main failure modes in power devices. The main determining factors are those of the junction temperatures that the device is exposed to. However, the equation also takes into account other factors such as the bond wire diameter, chip thickness (as a virtue of the voltage class of the device), current per bond wire stitch and finally the power cycling time.

A Monte Carlo simulation was performed by individually varying the independent variables of the CIPS2008 model (ΔT_j and $T_{j,min}$). It revealed that the equation is more sensitive to a change in the temperature swing rather than a change in the minimum junction temperature. The cycling time is also an independent variable. However, due to correction factors, adding a realistic variation to the cycling times will not change the constant value used in the equation. This is explained further in Section 3.7. Therefore, higher temperature swings lead to lower lifetimes and consequently more damage accumulated over a period of time.

Which semiconductor device is the most vulnerable in the Power Converter and how does it limit the lifetime of the converter?

An important objective of this thesis was to determine which power semiconductor in this converter was the most vulnerable. This would ultimately be the determining factor in the overall converter's lifetime. As seen in Chapters 4 and 5, the static lifetime of the IGBT comes out to be around 27.1 years and that of the diode to be 4.11 years. This means that the most vulnerable component in this converter is the rectifier diode. However, it is to be noted that the rectifier diode chosen for this purpose is an overrated one with a very high peak reverse recovery current (I_{RRM}) and high forward Voltage (V_F). This is because it was the only PLECS model available which met the converter requirements. Due to this, the losses were bound to be higher than in a conventional setup.

Therefore, if a better rectifier diode is used, the losses will be lower and in that case, the IGBT might very well become the vulnerable component. This can be seen in Section 6.2 where the diode is changed and the lifetime of the converter then is limited by the IGBT being used. In the case where the diode was limiting the converter's lifetime, the lifetime of the DCFC was found to be 0.86 years with a reliability of 90%. In contrast, when the IGBT was the limiting factor, the lifetime of the converter increased to 5-6 years with the same reliability.

7.3. Future Work

The aim of this project was to determine the lifetime of a DC Fast Charger operating under a comparable EV load and that goal was achieved. However, in the pursuit of that goal, a lot of assumptions were made. These assumptions make the lifetime that was derived in this thesis a lifetime valid for a very specific case. Moreover, a lot of the conditions were assumed to be ideal. Thus, for future work, the method implemented in this thesis can be expanded to different conditions to more closely resemble practical operating conditions thereby generating more realistic lifetimes for the power converter. Some of the ideas have been mentioned below.

One of the primary assumptions made in this project is that only the DC-DC converter is used to step up or down the voltage. However, in reality, as seen in previous sections, the AC-DC rectifier can also be used to control the voltage output. Thus, to truly determine the lifetime of the converter, it is important to take into account the effect that the AC-DC converter has on the whole system. Moreover, as the complexity of the devices increases, the overall system reliability will also be decreased. Therefore, it is important to consider both the converters required for the DC Fast Chargers.

Another assumption that was made was that only the semiconductors are the vulnerable parts of the system. Therefore the other components were assumed to be ideal. However, in practical conditions, it is not so. Hence, it is important to calculate the losses and lifetimes of various components in the entire system. Not only will this affect the efficiency of the converter but the heat generated from the

losses might also interact with other devices leading to higher junction temperatures than previously predicted. Moreover, a different type of component, for example, a capacitor's lifetime might limit the overall life of the converter and ultimately the charger.

The selection criteria of the diodes can be improved too. Initially, for this thesis, a diode was selected based on the availability of the PLECS model. This allowed for more accurate results due to the amount of data that was present in the PLECS model (but not in the datasheet). It also permitted the verification of the switching loss formula used in Section 6.2.2. However, this decision also led to the selection of a diode that was overrated and had loss parameters not suitable to this use case. In retrospect, the verification method could have been changed from software to hardware (experimental testing). Alternatively, the software could also be changed to LT-Spice which also housed a number of diode models that could have been better suited for this purpose. Selecting the appropriate semiconductors will lead to more accurate real-life comparable results.

This thesis also focuses on a particular type of converter. However, depending on the permutation and combination of AC-DC rectification and DC-DC converter, the losses for the same (semiconductor) device might vary thereby altering the lifetimes due to various modulation techniques and current/voltage stresses. Thus, an optimum configuration can be determined to maximize the lifetime of such chargers. Alternatively, to take these variations into consideration, the fitting parameters used in the CIPS2008 equation could also be varied. These parameters are determined by the type of circuit being tested. Therefore, conducting a Monte Carlo simulation for all these fitting constants might help as well, provided that the constants don't vary too much for different circuits.

While calculating the lifetime, only the long-term temperature fluctuations were considered. However, while minimal, there is still damage caused by the short-term temperature fluctuation generated by the switching behaviour of the IGBTs/MOSFETs. While the damage per cycle might be lower, the damage accumulated over a year may be significant since the number of cycles is multiple orders higher than the long-term temperature fluctuations. Thus, these two damages need to be added up to calculate the lifetime in a more accurate manner.

Implementing these changes in future research models will help generate a more robust way to calculate the lifetime of any EV charger being used in the industry. While there still might be some differences when compared to real-life scenarios, the method could be further fine-tuned to come as close to the real result as possible.

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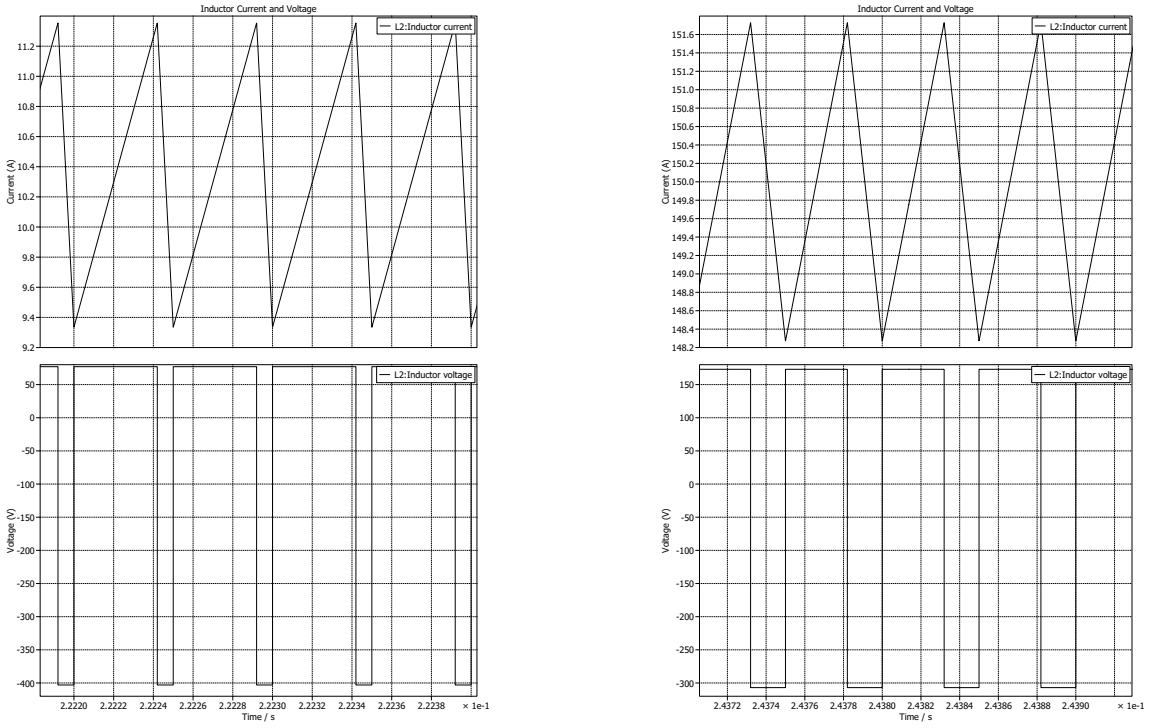
A

Output Filter Validation

This appendix chapter will focus on the validation of the output filter inductance that was designed in Section 3.3. The filter inductor was designed considering the worst-case scenario that occurs for the inductor in the load profile. In this case, that was the last point of the load profile with a current of around 10A and a voltage of 403V. Using these values, the inductance of the filter was determined to be 1.6 mH. Thus, the working of this inductor will be verified using (3.2). To do this, the inductor current ripple will be measured at two points - firstly the point that the inductor was designed for and secondly a point where the current ripple should be lower than the 20% allowed.

Figure A.1a shows the inductors waveforms at the 10.3375A and 403.2V load point. Whereas, in Figure A.1a, the graphs for 150A and 307V can be seen.



(a) 10A and 403V

(b) 150A and 307V

Figure A.1: Inductor Waveforms at various load points

The allowable inductor current ripples and the simulated ripples have been summarised in Table A.1. It

can be seen clearly in the table that at the low current load point, the inductor ripple is very close to the 20% desired value. On the other hand, for the 150A load point, the current ripple is much lower than 20% as expected due to the inductor size. Instead, the ripple value matches closely with the predicted value using (3.2). The values are found to be lower than the 20% allowable ripple due to the inductor value being rounded off during calculations.

Table A.1: Inductor Current Ripple Summary

Current Value (A)	Voltage Value (V)	Calculated Current Ripple (A)	Simulated Current Ripple (A)	20% Current Ripple (A)
10.3375	403.2A	2.02	2.01	2.06
150	307A	3.45	3.45	30

With these values, it can be considered the the output filter inductance was appropriately designed for use.

B

Power Loss Verification

This chapter shall look into verifying the power loss equation used in Section 6.2.2. This has to be done since the loss verification performed in Section 5.1 used a different formula (Equation B.1a) compared to the one used in the other Equation (B.1b). There are two reasons for this. Firstly, the lookup table for the losses was available in the case of the Dynex diode and their corresponding power loss graphs. Secondly, the reverse recovery time (t_{rr}) variable was not given in the Dynex Datasheet for this formula to be used.

$$P_{sw} = E_{rr}.f_{sw} \tag{B.1a}$$

$$P_{sw} = \frac{1}{2} I_{RRM} t_{rr} V_R. \left(\frac{I_F}{I_{ref}} \right) .f_{sw} \tag{B.1b}$$

However, the new diodes that were being used did not have any PLECS models available. Their data sheets had a graph for the forward voltage drop (V_F) but not the Switching losses (E_{rr}). Therefore the switching losses had to be calculated from (t_{rr}) value mentioned in their data sheets. But, the reverse recovery time mentioned in the data sheets is calculated under specific conditions mentioned in the datasheet. To be precise, the conditions specified are the forward current (I_F), the blocking voltage (V_R), and the junction temperature at which the measurement was made. Therefore, to account for the varying conditions in the load profile, a scaling factor has to be added to the equation that considers the ratio of the forward current and the reference current at which the reverse recovery time was measured. This scaling law can only be treated as an approximation since the change in reverse recovery time may not be linear with a change in forward current. Thus, this scaling law has been compared to the simulation results of the Dynex diode.

To do this, first the Dynex diode's reverse recovery time (t_{rr}) had to be calculated since it was not mentioned in the datasheet. However, the reverse recovery charge (Q_{rr}) and the peak reverse recovery current (I_{RRM}) have been mentioned in the datasheet. Using these two pieces of information, an approximation of t_{rr} can be made using Equation B.2.

$$Q_{rr} = \frac{1}{2} I_{RRM} t_{rr} \tag{B.2}$$

Therefore the value of t_{rr} derived from using this equation was substituted in Equation B.1b to derive the switching losses for the dynex diode. The conduction losses were calculated in the same as shown in 5.1 using Equation 5.5. The comparison with the simulated results is given below in Figure B.1.

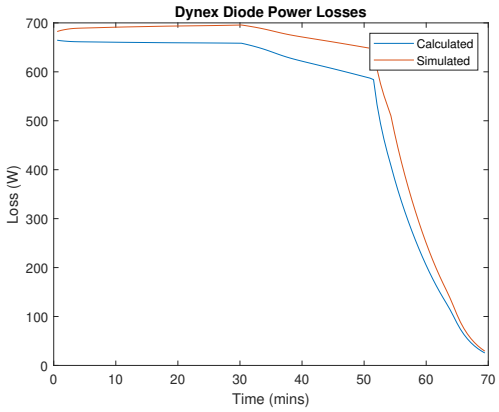


Figure B.1: Comparison of Power Losses in the Dynex Diode

As one can see, there is a slight difference in both curves. This can be explained by three primary reasons. Firstly, the calculated value of t_{rr} assumes that the area under the current curve is a perfect triangle. However, in reality, it is not and a curve is seen. Therefore, the t_{rr} is generally slightly different than what can be derived from Equation B.2. Secondly, the scaling law used assumed a linear relationship between the forward current and t_{rr}, which is only an approximation. Finally, the effect of temperature is not taken into account here. Despite these reasons, the discrepancies are lower than 10% throughout the load cycle. Thus, this Equation can be considered to be a valid approximation of switching losses in the new diodes.