A 1.2mW/channel 100m-Pitch-Matched Transceiver ASIC with Boxcar-Integration-Based RX Micro-Beamformer for High-Resolution 3D Ultrasound Imaging

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32.3 A 1.2mW/channel 100μm-Pitch-Matched Transceiver ASIC with Boxcar-Integration-Based RX Micro-Beamformer for High-Resolution 3D Ultrasound Imaging

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The integration of 2D ultrasonic transducer arrays and pitch-matched ASICs has enabled the realization of various 3D ultrasound imaging devices in recent years [1-3]. As applications such as 3D intravascular ultrasonography, intra-cardiac echocardiography, and trans-fontanelle ultrasonography call for miniaturization and improved spatial resolution, higher-frequency transducers (>5MHz) with a correspondingly smaller array pitch (<150□m) are needed. Such devices generally employ a large number of transducer elements, calling for channel-count reduction in the ASIC while meeting stringent restrictions on per-element power consumption and die area. Micro-beamforming (μBF) is an effective way of reducing channel count by performing a delay-and-sum operation on the echo signals received within a sub-array [1]. However, prior μBF implementations employ per-element capacitive memory to realize the delay [1,2], making it increasingly difficult to apply μBF in smaller-pitch arrays.

This paper presents a μBF architecture that employs current-mode summation and boxcar integration to realize delay-and-sum on an *N*-element sub-array using *N*□ fewer capacitive memory elements than conventional μBF implementations. This facilitates the use of μBF in smaller-pitch applications, as demonstrated by a prototype transceiver ASIC targeting a wearable ultrasound device that monitors brain perfusion in preterm infants via the fontanel (Fig. 32.3.1). To meet its strict spatial resolution requirements, a 10MHz 100μm-pitch piezoelectric transducer array is employed, leading to a per-element die area >2□ smaller than prior designs employing μBF [1-3].

Conventional μBF implementations [1,2] sample the echo signals $V_{1..N}$ from the sub-array elements and store the last *K* samples for each element, thus requiring *K* capacitive memory cells per element (Fig. 32.3.1). These stored values are then read out after a programmable time delay and added in the voltage- or charge-domain to implement the delay-and-sum operation. The proposed μBF, in contrast, operates on current-mode input signals $I_{1..N}$, and successively connects these to a set of *K* memory cells. These collect charge representing the upcoming *K* output samples, allowing summation to take place in the current domain at their input. The delay associated with an individual input is set by the delay between the connection of that input to a memory cell, and the moment that the memory cell connects to the output. This architecture reduces the number of memory cells by a factor of *N* compared to conventional μBFs [1,2]. In contrast with prior current-mode μBFs, which either employ per-channel delay lines [4] or explicit per-channel S/H stages [5], the signal currents are directly integrated on the memory capacitors, realizing boxcar integration that provides inherent anti-alias filtering and obviates the need for such filtering in the analog front-end (AFE), thus further reducing die size.

Figure 32.3.2 shows a block diagram of the prototype ASIC interfacing with an 8×8 transducer array. Element-level high-voltage (HV) pulsers allow all elements to contribute to acoustic pulse transmission (TX), with the ability to define time delays at the row- or column-level to steer the resulting TX beam to different angles. For echo reception (RX), the array is divided into sub-arrays of 2×2 elements. After TX, HV T/R switches and multiplexers connect two of these sub-arrays to the receive (RX) circuitry. The signal currents from the elements of the selected sub-arrays are amplified by 4 AFEs and then fed, via multiplexers that set the element delays, to 4 memory cells, implemented as active boxcar integrators to improve linearity compared to a passive integrator. Output sample-and-hold (S/H) stages drive the μBF outputs off chip.

The AFEs are based on the design presented in [6] and consist of a capacitive-feedback transimpedance amplifier (TIA), the output of which is capacitively coupled to the input of a current amplifier (CA). The CA provides a high-Z output to drive the boxcar integrator in the μBF with an amplified version of the transducer's signal current. The AFE's gain can be continuously controlled in a range of 36dB by an external voltage V_{TGC} to provide time-gain compensation, i.e., to compensate for the stronger attenuation of echoes that arrive later. The AFE provides less than ±0.4dB gain error and has a 1.31pA/√Hz input-referred noise density within 6 to 14MHz bandwidth at its maximum gain (V_{TGC} = 1.1V).

Figure 32.3.3 shows the detailed implementation of the μBF. To set the delay profile, each of the input currents $I_{1..4}$ is connected to one of 6 summation nodes, which correspond to 6 possible delay steps. These 6 summation nodes are cyclically connected to the 4 boxcar integrators, orchestrated by an 80MHz delay clock CLK_{delay}. The active boxcar integrators alternate between integration (R_i = 0) and readout (R_i = 1) phases. During the latter, the accumulated charge is transferred to one of two S/H stages, which operate in a ping-pong fashion and alternately drive the output, controlled by a 40MHz clock CLK_{SH}. While CLK_{delay} sets the minimum delay step to 12.5ns and the delay range to 62.5ns, CLK_{SH}, independently, sets the output sampling period to 25ns. The boxcar integration time is 25ns to provide effective anti-alias filtering.

The OTAs in the boxcar integrators and S/H stages are implemented using inverter-based amplifiers (Fig. 32.3.4) with current-reuse supply- and ground-regulators that suppress interference and are shared at the sub-array level to save area. Two capacitive level shifters (C_1/C_2) are used to enlarge the dynamic range of the OTAs. These are reset during the TX period (Φ_{TX}) and hold the DC bias points during the RX period (Φ_{RX}).

The ASIC has been fabricated in a 180nm BCD process (Fig. 32.3.7) and consumes 1.2mW/channel, of which 0.8mW is consumed by the AFE and 0.33mW by the μBF, while the 30V TX consumes 32μW/channel at a pulse repetition frequency of 10kHz. Figure 32.3.4 shows the input-referred noise at the μBF's output (Fig. 32.3.4) for different TGC control voltages (V_{TGC}). At the highest gain, it achieves 0.67pA/√Hz, which is close to half of the input-referred noise (1.31pA/√Hz) of a single-channel AFE measured at CA's output. This factor is in line with the $\sqrt{N} = 2$ noise reduction expected from a μBF without noticeable noise-folding effects and is maintained across the full gain range (Fig. 32.3.4). The gain of the full signal chain at 7 different TGC levels (Fig. 32.3.5) shows a minimum -3dB bandwidth of 14.7MHz at V_c = 1.1V. A measurement of SNR vs. input current shows a peak SNR of 54dB, and an 82dB dynamic range. An accurate delay-and-sum operation is demonstrated by applying time-shifted sinusoidal inputs to the chip, thus emulating acoustic inputs arriving at different angles, and comparing the μBF response with the ideal expected directivity for different μBF delay settings. The HV pulsers successfully produce 30V pulses with a delay resolution of 12.5ns.

Acoustic characterization is done on a prototype with transducer array built on top as shown in Fig. 32.3.7. A small water tank was mounted on top of the chip, with 3 needle reflectors positioned at about 8mm from the transducer surface (Fig. 32.3.6). For TX, 3-cycle 30V pulses were used. The μBFs were steered to different angles and the amplitude of the received echo signals increases as the μBF steered towards the reflectors. A B-mode image clearly shows the needles positions even with the small aperture size (0.8×0.8mm²).

A comparison with prior μBF ASIC designs with pitch-matched 2D arrays (Fig. 32.3.7) shows that this work achieves the smallest array pitch, the highest center frequency, and the smallest μBF area per channel, making the μBF architecture a promising solution for channel-count reduction in next-generation small-pitch 3D ultrasound imaging devices.

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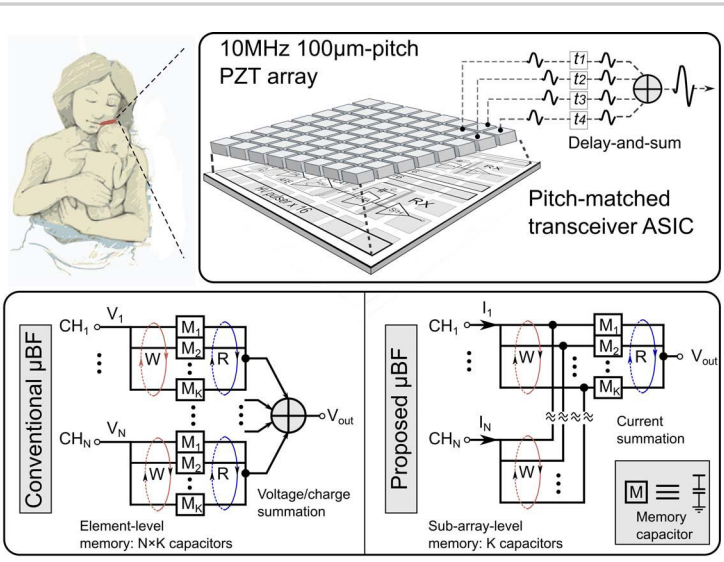


Figure 32.3.1: Overview of the ASIC for trans-fontanelle echography and comparison between conventional and proposed micro-beamforming.

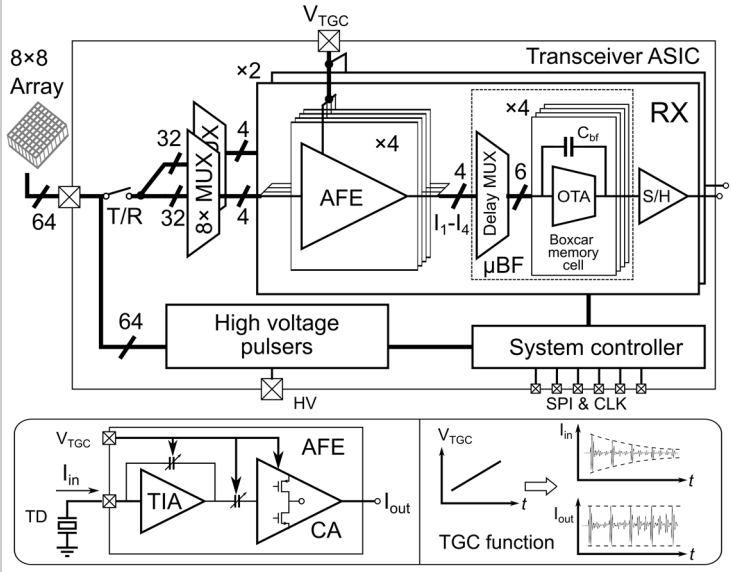


Figure 32.3.2: ASIC architecture with an inset showing the continuous-time time-gain-compensation AFE.

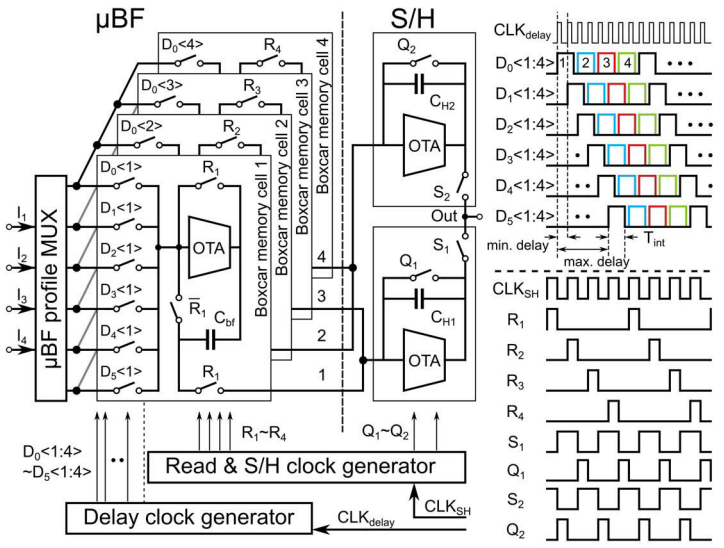


Figure 32.3.3: Circuit diagram of the boxcar-integration μ-beamformer, the ping-pong S/H and their timing details.

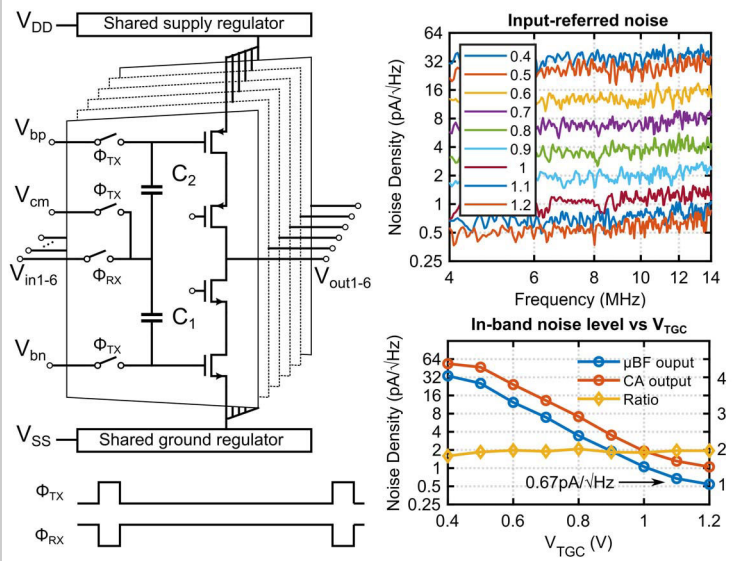


Figure 32.3.4: Inverter-based amplifiers, measured input-referred noise of the μBF,

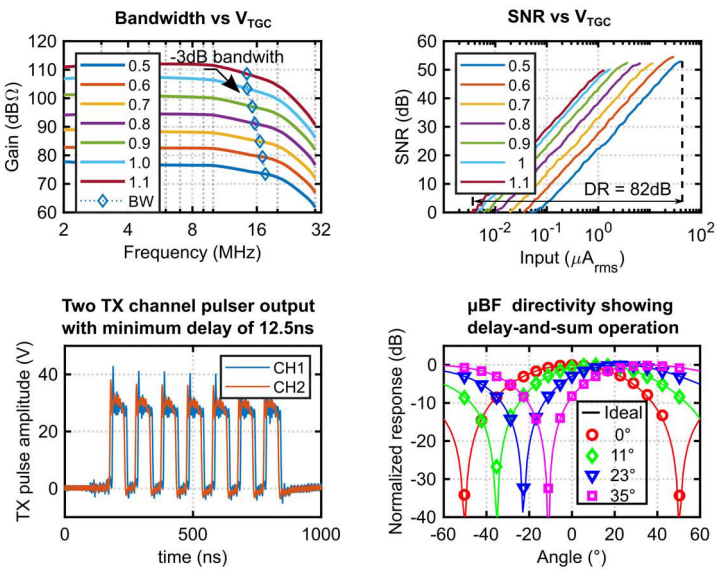


Figure 32.3.5: Measured signal-chain bandwidth, signal-to-noise ratio, high-voltage TX pulser and μ-beamforming directivity.

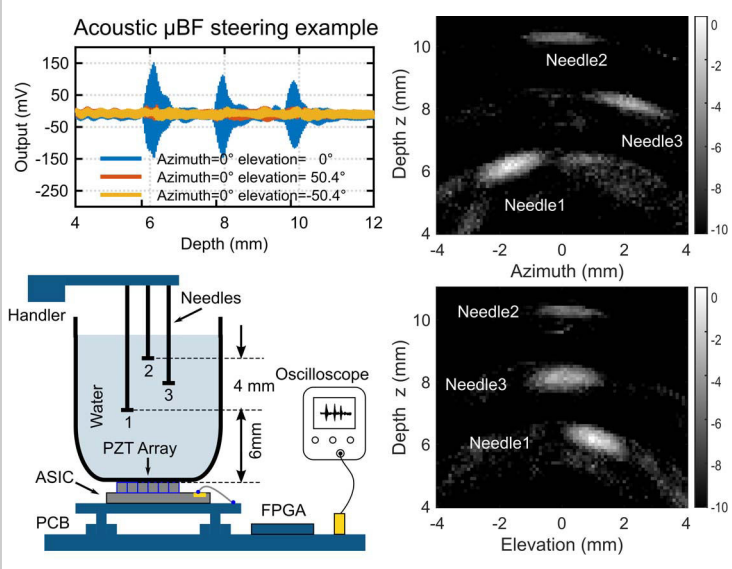
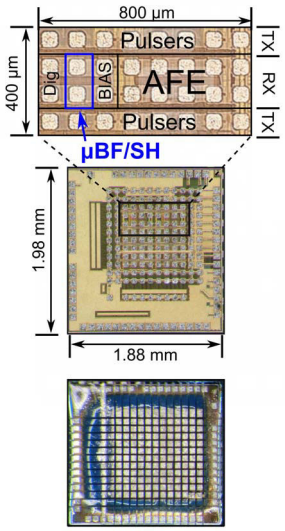


Figure 32.3.6: Acoustic beam-steering example, acoustic measurement setup and B-mode images.



Comparison with state-of-the-art pitch-matched micro-beamformer circuits for 2D arrays

	This work	[1]	[2]	[3]
uBF type	**Boxcar Int.**	Voltage S/H	Voltage S/H	ADC+FIFO
Process	**180nm BCD**	180nm	180nm SOI	28nm
Sub-array size	**2 × 2**	3 × 3	4 × 6	4 × 4
Transducer type	**PZT**	PZT	PZT	CMUT
Pitch	**100 µm**	150 µm	300 µm	250 µm
Center freq.	**10 MHz**	5 MHz	< 5 MHz	5 MHz
Sampling rate	**40 MS/s**	30 MS/s	40 MS/s	20 MS/s
Delay resolution	**12.5 ns**	33 ns	25 ns	8.33 ns
uBF area/ch.	**0.005 mm² ***	0.011 mm² †	0.03 mm²	0.041 mm² §
uBF power/ch.	**0.33 mW ***	0.17 mW †	0.19 mW	17.5 mW §
AFE type	**LNA with TGC**	LNA + PGA	LNA + PGA	LNA + PGA
RX area/ch.	**0.04 mm²**	0.026 mm²	0.09 mm²	0.088 mm²
RX power/ch.	**1.17 mW**	0.91 mW †	0.43 mW	33 mW §
Peak SNR	**54 dB**	51.8 dB	n/a	59.9 dB
Input DR	**82 dB**	85 dB	85 dB	n/a
Includes TX	**Y**	N	Y	N
TX voltage	**30 V**	-	138 V	-

*includes S/H stage; † includes sub-array ADC;
§includes element-level ADC

Figure 32.3.7: Micrograph of the ASIC and prototype with transducers on top, and comparison with the state of the art.

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