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Switching Algebra Noninterference Based Spin Wave Computing

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***Abstract*—In recent years, Spin Waves (SWs) have emerged as a promising avenue for beyond-CMOS computing, offering potential advantages in terms of energy efficiency, scalability, and opening avenues towards novel computation paradigms. Until now, SW interference-based gates, for example, the 3 input majority gate (MAJ3), have been proposed and experimentally demonstrated, and an alternative computing paradigm, which relies on SW phase manipulation instead of SW interference has been proposed. However, state-of-the-art SW-based devices suffer from challenges that hinder the realization of larger-scale SW circuits. In this paper, we explore a different computing avenue that relies on Boolean algebra and introduce a SW Switch that makes use of the Voltage Controlled Magnetic Anisotropy (VCMA) effect to allow/block SW propagation. We introduce the device concept, verify its functionality by means of micromagnetic simulations, and perform a circuit-level analysis on EPFL Combinational Benchmarking Suite circuits. As no SW generation and SW read transducers energy consumption experimental data is available we evaluate their upper bound values for which SW implementations can outperform CMOS counterparts. We implement the circuits by means of state-of-the-art SW technologies and the proposed method, compute the upper bound values, and our results indicate that on average the proposal is increasing the upper bound by about $1.2\times$. Subsequently, we consider SW read transducers energy consumption estimates reported in the literature and argue that while they seem appropriate for evaluating SW Boolean switching gates they have to be multiplied with a factor $m > 1$ to capture the extra complexity of generating the output value for SW interference and Phase manipulation SW gates. Our evaluations indicate that the SW Switch-based approach reduces the energy consumption by $1.2504\times$, $1.4973\times$, $1.7443\times$, and $1.9912\times$, when compared to the interference approach, and by $1.2478\times$, $1.4947\times$, $1.7416\times$, and $1.9886\times$, when compared to the phase shifting approach, for $m = 1.25, 1.5, 1.75, 2$, respectively. We finally highlight system level advantages of our proposal and conclude that SW Boolean switching gates are opening the most promising avenue towards energy effective SW computing.**

I. Introduction

In recent years, Complementary Metal Oxide Semiconductor (CMOS) technology has made considerable progress [1]. However, as CMOS technology continues to evolve, the need for a higher transistor density per chip, to increase computing capabilities, continues to drive device miniaturization [2]. However, increasing complexity [3] and power consumption [4] hinder the realization of scaled-down transistors. As a result, the Dennard scaling is approaching its physical and practical limits [5]. To this end, various fields have been investigated as potential CMOS technology successors [6], aiming to surpass its performance in the near future. One particularly promising beyond-CMOS avenue involves exploiting the inherently unique properties of Spin Waves (SWs) for computation [7], [8]. SWs correspond to propagating disturbances in magnetic materials spin alignment, which are enabling data encoding, transmission, and processing. Their intrinsic properties [9], including, but not limited to, a broad operating frequency range (GHz - THz), nonlinear dynamics and energy-free data transmission, offer significant advantages for the development of SW-based devices, facilitating the potential realization of ultra-low power circuits and systems.

State-of-the-art SW devices rely on relative phase data encoding and SW interference [10] for computation. Within such a framework, input data are represented by the phase difference between the respective SW and a reference signal: a relative phase of $0°$ (in-phase) represents a logic 0 while $180°$ (out-of-phase) denotes a logic 1. This encoding scheme leverages the SW wave-like nature and enables logic operations by means of SWs interference, where in-phase SWs interfere constructively and out-of-phase destructively. For proper functionality, SW-generating antennas must be placed at distances $n \times \lambda$ from each other, where λ is the SW wavelength and n an integer constant. As such, a 3-input Majority gate (MAJ3) has been proposed [11] and experimentally demonstrated [12], [13], where 3 SWs are excited by means of Radio Frequency (RF) antennas and propagate through a magnetic conduit, while interacting according to their phase relationships. Therefore, the relative phase of the resulting SW, i.e., the gate output, is determined by means of a majority voting process. Note that, MAJ3 and inverter (INV), realized by shifting the MAJ3 readout port position within $\pm\frac{\lambda}{2}$, form a universal gate set, thus any Boolean function can be implemented withing this computation paradigm.

In spite of its great potential, interference-based SW computing faces significant challenges, e.g., gate cascading [14], fan-out achievement [15], [16], rendering the transition from the gate to circuit level rather complex. State-of-the-art

technology addresses these issues by employing SW to/from CMOS domain converters, which are rather power-hungry and are diminishing the inherent SW technology low-power advantage. In view of this, a new SW computing avenue, Spin Wave Threshold Logic (SWTL), that relies on SW phase manipulation instead of SWs interference have been proposed [17]. This approach involves exciting and propagating a single SW carrier through a waveguide, while computations are performed by inducing input-dependent phase shifts by means of DC-controlled transducers, Phase Shifters (PSs), that can modulate an incoming SW carrier phase. The gate output is determined based on the SW carrier net phase shift by following the Threshold Logic (TL) principles [18]. Based on this concept, the Phase Shifting MAJ3 (PSMAJ3) gate was introduced [19], which exhibits clear advantages over its interference-based counterpart by requiring less RF circuitry and relaxing the SW synchronization constraints. However, PS-based SW computing still falls short of fully realizing larger-scale circuits as PSMAJ3 gates cascading still requires domain conversions.

In view of the above, in this paper, we propose a Boolean Algebra SW-based computing alternative. Our proposal builds upon Boolean Algebra synthesis procedure and makes use of the Voltage Controlled Magnetic Anisotropy (VCMA) effect to implement SW-VCMA Switches able to block/allow SW propagation. As such, for a given function $f(x_1, x_2, ..., x_n)$, we create a waveguide maze on which SW carriers propagation is controlled by $x_1, x_2, ..., x_n$ values, such that SW absence/presence at the output port indicates $f = 0/1$.

This paper is organized as follows: In Section II, we briefly present the Voltage Controlled Magnetic Anisotropy effect and introduce the SW-VCMA Switch concept. In Section III, we proceed to present the verification of the proposed device, and in Section IV, a circuit-level analysis of a collection of representative logic circuits utilizing SW computation technologies, i.e., Interference, Phase Shifting, and Boolean Switching, and compare them with CMOS counterparts. We conclude the paper by discussing circuit and system level advantages of our proposal over other SW counterparts.

II. SW-VCMA Switch Concept

While state-of-the-art SW computation is relying on SWs interaction or SW phase manipulation we propose to pursue a Boolean Algebra inspired avenue. As such, to evaluate a given Boolean function $f(x_1, x_2, ..., x_n)$ we rely on a waveguide maze where SW carriers propagation is controlled by means of SW switches. Within such a framework, the absence/presence of a SW at the output determines the logic value $f = 0/1$. As such, circuit topology and switch control are determined by means of Boolean function synthesis principles and tools, while traditional switches need to be realized in the SW domain.

For the implementation of the Boolean switches within the SW domain, we make use of the Voltage Controlled Magnetic Anisotropy (VCMA) effect [20], which relies on controlling the Perpendicular Magnetic Anisotropy (PMA) field intensity by means of an external voltage [21]. Voltage application is performed through a material stack locally embedding the waveguide, an example of which is presented in Figure 1, where the voltage application electrodes are connected to the top gold layer and the bottom heavy metal layer. The voltage, V, creates an electric field, E, in the oxide layer, which in turn increases or decreases, depending on the sign, the PMA field in the region of the waveguide where the stack is located. Consequently, the interfacial anisotropy constant, K_S, is increased as per (1), where β is the VCMA coefficient obtained through material selection and stack engineering.

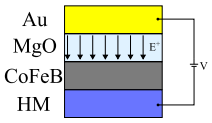


Fig. 1: Material stack for VCMA effect realization

$$\Delta K_S = \beta \cdot E \tag{1}$$

By increasing the PMA field, the SW dispersion relation in the waveguide region where the stack is placed is shifted upwards to a point where, at the original SW excitation frequency, no propagating SW mode exists, thus, blocking the SW propagation. As such, a SW-VCMA switch can be realized, as graphically depicted in Figure 2, where an RF transducer is utilized to excite a carrier SW and the VCMA material stack is employed to allow/block its propagation. By implementing such SW Boolean switches, SW circuits able to evaluate any given Boolean function $f(x_1, x_2, ..., x_n)$ can be realized by following the Boolean algebra principles.

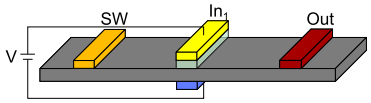


Fig. 2: Voltage Controlled Magnetic Anisotropy SW Switch

III. SW Switch Design and Verification

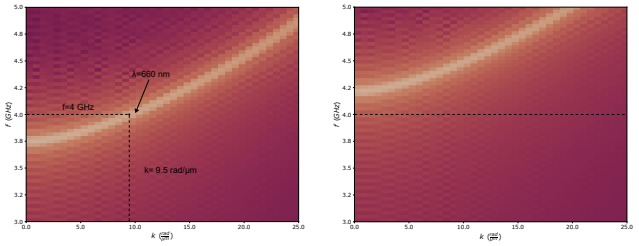
Having presented the SW-VCMA switch concept, we proceed to verify its correct behavior. To do so, we perform mumax^3 [22] micromagnetic simulations, by utilizing the following setup. A single RF antenna was placed on top of the waveguide, to create the carrier SW, and we varied the PMA field in the middle region of the waveguide to obtain "open" and "closed" state of the switch. As, mumax^3 does not inherently support the implementation of the interfacial anisotropy K_S, we utilized the uniaxial anisotropy K_u instead. For the starting value, we set $K_u = 0.92\,\mathrm{MJ\,m^{-3}}$, which translates to $K_S = t \cdot K_u = 3.68\,\mathrm{mJ\,m^{-2}}$, where $t = 4\,\mathrm{nm}$ is the waveguide thickness. The rest of the simulation parameters are presented in Table I. For the SW carrier generation, we chose an excitation frequency $f_{exc} = 4\,\mathrm{GHz}$, which, according to the dispersion relation presented in Figure 3a, induces a SW with an wavelength $\lambda = 600\,\mathrm{nm}$.

For the application of the VCMA effect, we consider the creation of an electric field $E = 0.225\,\mathrm{V\,nm^{-1}}$ at the oxide

TABLE I: SW-VCMA switch simulation parameters

Material	Length	Width	Thickness	Bext
CoFeB	10 µm	200 nm	4 nm	60 mT

layer, which results in an increased $K'_S = K_S + \beta \cdot E = 3.854\,\mathrm{mJ\,m^{-2}}$ with $\beta = 174\,\mathrm{fJ\,V^{-1}\,m^{-1}}$ chosen to accommodate experimental values [23], at the respective region of the waveguide. Accordingly, the uniaxial anisotropy increases to $K'_u = 0.924\,35\,\mathrm{MJ\,m^{-3}}$. From the performed simulations, we obtain the dispersion relations for both anisotropy values, as graphically depicted in Figure 3, where one can clearly observe that the dispersion shifts upward when K'_u is utilized, and no propagating SW mode exists at the original excitation frequency, thus, blocking the carrier wave when the voltage is applied.



(a) V not applied (b) V applied

Fig. 3: Dispersion relation modulation

Thus, to verify the correct behavior of the SW-VCMA switch, we simulate both switching states: when V is not applied and hence the switch is 'closed' and when V is applied and the switch is 'open'. By appropriately modulating the anisotropy values in each case, we demonstrated the expected functionality as depicted in Figure 4.

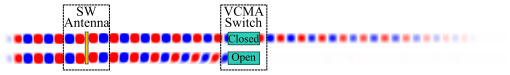


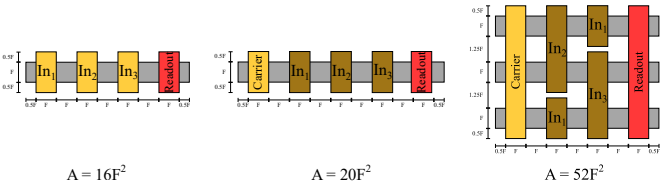
Fig. 4: SW-VCMA Switch simulated behavior

IV. Circuit Level Analysis

Having demonstrated the correct behavior of the SW-VCMA switch, it is of interest to examine the impact of our proposal at the circuit level. To do so, we consider the collection of representative logic circuits from the EPFL Combinational Benchmarking Suite [24] presented in Table II, and derived estimates of energy and area for their implementations in CMOS and SW-based technologies, i.e., Interference-based, Phase Shifting-based, and Boolean Switching-based. The CMOS circuits are synthesized by means of commercially available tools and a 7 nm CMOS technology node, while for the SW implementations, we utilized Majority Inverter Graph (MIG) synthesis [25]. While MIG netlists include majority gates only, some of them have one input connected to $0/1$ to obtain an AND (OR) gate behavior. Thus, as Boolean Switching (BS) provides direct support for AND (OR) gate implementations we replace underutilized MAJ3 gates with the equivalent Boolean Switching AND (BSAND) and OR (BSOR) gates. We note that circuits implemented solely employing BSAND/BSOR gates wouldn't provide optimized designs since the Boolean Switching MAJ3 (BSMAJ3) gate requires only 4 SW-VCMA switches, as depicted in Figure 5c, instead of 10 in case it is implemented with BSAND/BSOR gates. For Interference- and Phase Shifting-based technologies, the building blocks are MAJ3 and PSMAJ3 gates, respectively.

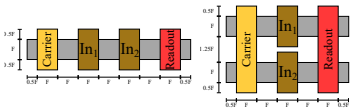
TABLE II: Implemented circuits' names and descriptions

Circuit Name	Description
'ctrl'	Simple control unit for an arithmetic logic unit
'router'	Look-ahead XY routing function
'int2float'	11-bit integer to 4-bit mantissa/3-bit exponent float
'dec'	Standard decoder function
'priority'	Priority encoder
'cavlc'	Context-adaptive variable-length coding
'i2c'	Controller (serial bus)
'arbiter'	Blind Round Robin arbiter
'bar'	Barrel shifter
'adder'	128-bit adder
'mem'	Memory controller
'max'	Maximum finder in 4 x 128-bit in uts
'sin'	Boolean function approximating the sinus trigonometric function
'voter'	Majority voting of 1001 bits
'square'	64-bit square ($b = a^2$)
'log2'	32-bit logarithm with base 2
'mult'	64-bit combinational multiplication of unsigned integers
'sqrt'	128-bit square-root integer approximation



A = 16F² A = 20F² A = 52F²

(a) MAJ3 (b) PSMAJ3 (c) BSMAJ3



A = 16F² A = 25.5F²

(d) BSAND (e) BSOR

Fig. 5: SW building blocks layouts and area estimates

For circuit area estimations, we consider that each gate embeds a number of RF and DC transducers. Assuming that each transducer occupies an area of F^2, with F being the transducer feature size, area estimations are deduced based on the gate layouts depicted in Figure 5. Consequently, MAJ3, PSMAJ3, BSMAJ3, BSAND, and BSOR require $16F^2$, $20F^2$, $52F^2$, $16F^2$, and $25.5F^2$, respectively, which for $F = 20\,\mathrm{nm}$ translate to $0.0064\,\mu\mathrm{m}^2$, $0.008\,\mu\mathrm{m}^2$, $0.0208\,\mu\mathrm{m}^2$, $0.0064\,\mu\mathrm{m}^2$, and $0.022\,95\,\mu\mathrm{m}^2$, respectively.

For evaluating SW circuit implementations energy consumption, we only consider the energy consumed by RF and DC transducers, as SW propagation can be considered as inducing no power consumption. As, for the time being, no experimental data are available for the practical realization of the RF and DC transducers, no realistic energy consumption values can be estimated for the SW circuit implementations. Thus, instead of providing energy consumption figures for

TABLE III: Area estimations and RF and DC transducers energy consumption upper bounds

Circuit Name	CMOS		Interference				Phase Shifting					Boolean Switching						
	Area (μm^2)	Energy (fJ)	Gates	Area (μm^2)		Energy (aJ)	Gates	Area (μm^2)		Energy (aJ)		Gates			Area (μm^2)		Energy (aJ)	
			MAJ3	F =20.000 nm	F =30.000 nm	E_{RF}	PSMAJ3	F =20.000 nm	F =30.000 nm	E_{RF}	E_{DC}	BSOR	BSAND	BSMAJ3	F =20.000 nm	F =30.000 nm	E_{RF}	E_{DC}
'ctrl'	4.00	0.234	86	0.619	1.393	0.680	86	0.688	1.548	0.680	0.453	9	47	30	1.017	2.287	0.812	0.406
'router'	3.92	0.278	218	1.570	3.532	0.318	218	1.744	3.924	0.318	0.212	40	92	86	2.786	6.268	0.375	0.188
'int2float'	6.47	0.721	203	1.462	3.289	0.888	203	1.624	3.654	0.888	0.592	44	108	51	2.201	4.952	1.092	0.546
'dec'	12.43	0.268	304	2.189	4.925	0.220	304	2.432	5.472	0.220	0.147	7	297	0	1.972	4.437	0.294	0.147
'priority'	20.39	7.505	818	5.890	13.252	2.294	818	6.544	14.724	2.294	1.529	361	275	182	9.228	20.763	2.847	1.423
'cavlc'	21.00	2.879	577	4.154	9.347	1.247	577	4.616	10.386	1.247	0.832	122	296	159	6.446	14.504	1.523	0.762
'i2c'	33.78	3.269	1116	8.035	18.079	0.732	1116	8.928	20.088	0.732	0.488	291	567	258	11.963	26.918	0.907	0.453
'arbiter'	191.50	24.005	6827	49.154	110.579	0.879	6827	54.616	122.886	0.879	0.586	572	876	5379	123.324	277.479	0.928	0.464
'bar'	81.50	46.208	2819	20.297	45.668	4.098	2819	22.552	50.742	4.098	2.732	946	1541	332	26.417	59.439	5.257	2.629
'adder'	76.40	82.432	384	2.765	6.221	53.667	384	3.072	6.912	53.667	35.778	1	2	381	7.948	17.883	53.772	26.886
'mem'	1074.80	990.792	40582	292.190	657.428	6.104	40582	324.656	730.476	6.104	4.069	8702	21155	10725	447.232	1006.278	7.479	3.740
'max'	111.60	194.020	2386	17.179	38.653	20.329	2386	19.088	42.948	20.329	13.553	703	1397	286	22.060	49.635	26.064	13.032
'sin'	185.23	850.664	4164	29.981	67.457	51.073	4164	33.312	74.952	51.073	34.048	1902	1200	1062	49.170	110.633	62.761	31.381
'voter'	410.59	574.434	5527	39.794	89.537	25.983	5527	44.216	99.486	25.983	17.322	868	1764	2895	80.359	180.808	29.494	14.747
'square'	702.46	2699.328	10795	77.724	174.879	62.513	10795	86.360	194.310	62.513	41.676	1487	4530	4778	143.542	322.969	72.635	36.317
'log2'	1161.98	14 256.956	24038	173.074	389.416	148.275	24038	192.304	432.684	148.275	98.850	10069	7370	6599	287.131	646.045	181.126	90.563
'mult'	1023.41	7437.999	18881	135.943	305.872	98.485	18881	151.048	339.858	98.485	65.657	4988	7364	6529	233.810	526.073	117.742	58.871
'sqrt'	1237.23	153 216.240	18983	136.678	307.525	2017.809	18983	151.864	341.694	2017.809	1345.206	5939	8900	4144	203.733	458.399	2507.918	1253.959

each implementation, we are seeking RF and DC transducers' energy consumption theoretical upper bound estimations for which SW implementations can still outperform their CMOS counterparts in terms of energy consumption.

From the area and upper bound energy consumption estimations, presented analytically in Table III, we can conclude that, when compared to the other SW implementations, the proposed Boolean Switching approach is less effective in terms of area, but it outperforms its counterparts in terms of energy consumption, i.e., it can outperform CMOS at a more relaxed RF transducer energy consumption upper bound. While the actual improvement is circuit specific, Boolean Switching provides an average increase of $1.20395\times$ in terms of RF transducer energy consumption upper bound. This is quite significant as it relaxes the RF transducers design constraints while still enabling the proposed approach to produce SW implementations that outperform their CMOS counterparts.

To further evaluate our concept, we compute the SW circuits energy consumptions when utilizing the theoretical transducers energy consumption estimates reported in [26], i.e., $14.4\,\mathrm{aJ}$ for a SW generating antenna and $2.7\,\mathrm{fJ}$ for a SW readout. While these are enough for the evaluation of MAJ3 based implementations, the other SW schemes require DC transducers, for which no estimates are available. Therefore, we assume that a DC transducer consumes a fraction of the RF transducer energy, expressed as $E_{DC} = k \cdot E_{RF}$, $k \leq 1$.

The energy consumptions under these assumptions are presented in Table IV, and we observe that while our is in the leading position, the improvement remains relatively small. For instance, in the case of the 'ctrl' circuit with $k = 0.0625$, our approach lowers the total energy consumption by $23.39\,\mathrm{aJ}$ and $2.26\,\mathrm{fJ}$, when compared to the phase

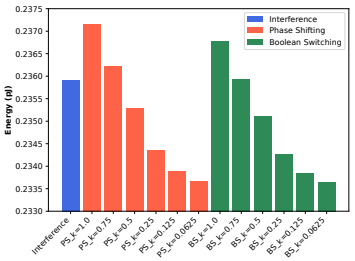


Fig. 6: 'ctrl' circuit energy consumption comparison

shifting and interference approaches, respectively, as depicted in Figure 6. This rather small difference is related to the fact that readout transducers are operating into fJ regime while the SW generating transducers into aJ regime and, while having different architectures, the implementations require the same (similar) number of gates (SW readout transducers), thus the overall energy consumption is dominated by the readout component.

However, the estimate in [26] only covers the energy consumption of the Sense Amplifier (SA) utilized to generate a voltage, to be further processed by the CMOS circuitry in order to detect the SW phase difference and produce the gate output value $0/1$, but completely disregard the energy consumption related to this output value detection process. This simplification is appropriate for Boolean switching, where we can tell the gate output value by sensing the presence/absence of an output SW. However, it is rather inaccurate for interference and phase shifting gates, which in order to provide the gate output value should embed additional circuitry for the computation of the phase difference between the obtained signal and a reference.

While the design of phase difference detection circuits [27], [28] is out of the scope we are interested to evaluate their impact on the overall energy consumption for the three considered avenues, i.e., Interference, Phase Shifting, and Boolean Switching. In view of the previous discussion the read energy for Boolean Switch $E_{read_{BS}}$ is the one estimated in [26] while the read energy for Interference and Phase Shifting is $E_{read_{Inter/PS}} = m \cdot E_{read_{BS}}$, where $m > 1$ captures the overhead associated with the phase difference detection circuitry. By assuming again that the DC transducer energy consumption $E_{DC} = 0.5 \cdot E_{RF}$ and $m = 1.25, 1.5, 1.75, 2$, we computed the total energy consumptions of the circuits presented in Table V. From the obtained results, we note that for $m = 1.25, 1.5, 1.75, 2$, our approach significantly reduces the energy consumption, achieving average reductions of $1.2504\times$, $1.4973\times$, $1.7443\times$, and $1.9912\times$, respectively, when compared to the interference approach, and $1.2478\times$, $1.4947\times$, $1.7416\times$, and $1.9886\times$, respectively when compared to the phase shifting approach.

Aside from the energy efficiency improvements, our approach offers additional advantages at the system level. While SW interference-based gates necessitate precise input SW synchronization to maintain phase relationships between inputs and ensure proper interference, our approach is free

TABLE IV: SW circuits energy consumptions (transducer energy consumption estimates [26] and $E_{DC} = k \cdot E_{RF}$)

Circuit Name	E_{Inter} (pJ)	E_{PS} (pJ)						E_{BS} (pJ)					
		$k=1$	$k=0.75$	$k=0.5$	$k=0.25$	$k=0.125$	$k=0.0625$	$k=1$	$k=0.75$	$k=0.5$	$k=0.25$	$k=0.125$	$k=0.0625$
'ctrl'	0.23592	0.2372	0.2362	0.2353	0.2344	0.2339	0.2337	0.2368	0.2359	0.2351	0.2343	0.2339	0.2337
'router'	0.59802	0.6012	0.5988	0.5965	0.5941	0.5929	0.5923	0.6005	0.5983	0.5961	0.5939	0.5928	0.5923
'int2float'	0.55687	0.5598	0.5576	0.5554	0.5532	0.5521	0.5516	0.5583	0.5565	0.5547	0.5529	0.5519	0.5515
'dec'	0.83393	0.8383	0.8350	0.8317	0.8285	0.8268	0.8260	0.8339	0.8317	0.8296	0.8274	0.8263	0.8257
'priority'	2.24394	2.2557	2.2469	2.2381	2.2292	2.2248	2.2226	2.2492	2.2420	2.2348	2.2276	2.2240	2.2222
'cavlv'	1.58283	1.5911	1.5849	1.5787	1.5724	1.5693	1.5678	1.5874	1.5821	1.5768	1.5715	1.5689	1.5675
'i2c'	3.06141	3.0775	3.0654	3.0534	3.0413	3.0353	3.0323	3.0688	3.0590	3.0491	3.0392	3.0342	3.0317
'arbiter'	18.72783	18.8261	18.7524	18.6787	18.6049	18.5681	18.5496	18.8827	18.7949	18.7070	18.6191	18.5752	18.5532
'bar'	7.73308	7.7737	7.7432	7.7128	7.6823	7.6671	7.6595	7.7426	7.7200	7.6973	7.6746	7.6632	7.6576
'adder'	1.05339	1.0589	1.0548	1.0506	1.0465	1.0444	1.0434	1.0644	1.0589	1.0534	1.0478	1.0451	1.0437
'mem'	111.32454	111.9089	111.4706	111.0324	110.5941	110.3749	110.2654	111.6334	111.2640	110.8946	110.5252	110.3405	110.2481
'max'	6.54528	6.5796	6.5539	6.5281	6.5023	6.4894	6.4830	6.5535	6.5343	6.5150	6.4958	6.4862	6.4814
'sin'	11.42268	11.4827	11.4377	11.3927	11.3477	11.3253	11.3140	11.4533	11.4156	11.3780	11.3404	11.3216	11.3122
'voter'	15.16167	15.2413	15.1816	15.1219	15.0622	15.0323	15.0174	15.2450	15.1844	15.1238	15.0631	15.0328	15.0177
'square'	29.61284	29.7683	29.6517	29.5351	29.4185	29.3602	29.3311	29.7505	29.6383	29.5262	29.4141	29.3580	29.3300
'log2'	65.94104	66.2872	66.0276	65.7680	65.5084	65.3786	65.3137	66.1311	65.9105	65.6899	65.4693	65.3590	65.3039
'mult'	51.79436	52.0663	51.8623	51.6584	51.4545	51.3525	51.3016	51.9824	51.7994	51.6165	51.4335	51.3421	51.2963
'sqrt'	52.07417	52.3475	52.1425	51.9375	51.7325	51.6300	51.5787	52.1935	52.0270	51.8605	51.6940	51.6107	51.5691

TABLE V: Energy consumptions assuming that $E_{DC} = 0.5 \cdot E_{RF}$ and $E_{read_{Inter,PS}} = m \cdot E_{read_{BS}}$

Circuit Name	E_{BS} (pJ)	E_{Inter} (pJ)					E_{PS} (pJ)				
		$m=1$	$m=1.25$	$m=1.5$	$m=1.75$	$m=2$	$m=1$	$m=1.25$	$m=1.5$	$m=1.75$	$m=2$
'ctrl'	0.2351	0.2359	0.2940	0.3520	0.4101	0.4681	0.2353	0.2933	0.3514	0.4094	0.4675
'router'	0.5961	0.5980	0.7452	0.8923	1.0395	1.1866	0.5964	0.7436	0.8907	1.0379	1.1850
'int2float'	0.5547	0.5569	0.6939	0.8309	0.9679	1.1097	0.5554	0.6924	0.8295	0.9665	1.1035
'dec'	0.8296	0.8339	1.0391	1.2443	1.4495	1.6547	0.8317	1.0369	1.2421	1.4473	1.6525
'priority'	2.2348	2.2439	2.7961	3.3482	3.9004	4.4525	2.2380	2.7902	3.3423	3.8945	4.4466
'cavlc'	1.5768	1.5828	1.9723	2.3618	2.7513	3.1407	1.5787	1.9681	2.3576	2.7471	3.1366
'i2c'	3.0491	3.0614	3.8415	4.5680	5.3213	6.0746	3.0534	3.8067	4.5600	5.3133	6.0666
'arbiter'	18.7070	18.7278	23.3361	27.9443	32.5525	37.1607	18.6787	23.2869	27.8951	32.5033	37.1120
'bar'	7.6973	7.7331	9.6359	11.5387	13.4416	15.3444	7.7128	9.6156	11.5184	13.4213	15.3240
'adder'	1.0533	1.0534	1.3126	1.5718	1.8310	2.0902	1.0506	1.3098	1.5690	1.8282	2.0874
'mem'	110.8946	111.3245	138.7174	166.1100	193.5031	220.8959	111.0324	138.4252	165.8181	193.2109	220.6000
'max'	6.5150	6.5453	8.1558	9.7664	11.3769	12.9875	6.5281	8.1386	9.7492	11.3597	12.9700
'sin'	11.3780	11.4227	14.2334	17.0441	19.8548	22.6655	11.3970	14.2034	17.0141	19.8248	22.3630
'voter'	15.1238	15.1617	18.8924	22.6231	26.3538	30.0846	15.1219	18.8526	22.5833	26.3140	30.0450
'square'	29.5262	29.6128	36.8995	44.1861	51.4727	58.7593	29.5351	36.8217	44.1084	51.3950	58.6820
'log2'	65.6899	65.9410	82.1667	98.3923	114.6180	130.8436	65.7680	81.9936	98.2193	114.4449	130.6700
'mult'	51.6165	51.7944	64.5390	77.2837	90.0284	102.7731	51.6584	64.4031	77.1478	89.8924	102.6400
'sqrt'	51.8605	52.0742	64.8877	77.7012	90.5147	103.3287	51.9375	64.7510	77.5645	90.3781	103.1900
Average $E_{approach}/E_{BS}$		1.0035	1.2504	1.4973	1.7443	1.9912	1.0009	1.2478	1.4947	1.7416	1.9886

of this constraint. Furthermore, both interference and phase shifting paradigms rely on the availability of a reference signal for acquiring the logic value of gate outputs. Therefore, additional circuitry is required for the reference signals generation and for the output readout transducers, which indicates that interference and phase shifting implementations may present even greater area and energy footprints. Based on the above, we conclude that the Boolean switching paradigm is the most promising SW-based avenue towards ultra-low power SW-based computing.

V. Conclusions

We initially discussed state-of-the-art SW-based devices and the challenges, which are hindering the realization of larger-scale SW circuits. Subsequently, we proposed a different computing avenue that relies on Boolean algebra and introduced a SW switch that makes use of Voltage Controlled Magnetic Anisotropy (VCMA) effect to allow/block SW propagation. We introduced the device concept, verified its functionality by means of micromagnetic simulations, and performed a circuit-level analysis on EPFL Combinational Benchmarking Suite circuits. As no experimental data related to SW generation and SW read transducers energy consumption are available we evaluated their upper bound values for which SW implementations can outperform CMOS counterparts. We implemented the circuits by means of state-of-the-art SW technologies and the proposed method, computed the upper bound values, and our results indicated that on average the SW Switch based approach allows for a $1.2\times$ upper bound increase. Subsequently, we considered SW read transducers energy consumption estimates reported in the literature and argued that they seem appropriate for evaluating SW Boolean switching gates, but they have to be multiplied with a factor $m > 1$ to capture the extra complexity of generating the output value for SW interference and Phase manipulation gates. Our evaluations indicated that our approach reduced the energy consumption by $1.2504\times$, $1.4973\times$, $1.7443\times$, and $1.9912\times$, when compared to the interference approach, and by $1.2478\times$, $1.4947\times$, $1.7416\times$, and $1.9886\times$, when compared to the phase shifting approach, for $m = 1.25, 1.5, 1.75, 2$, respectively. We finally highlighted system level advantages of our proposal and concluded that SW Boolean switching gates are opening the most promising avenue towards energy effective SW computing.

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REFERENCES

[1] H. H. Radamson, J. Luo, E. Simoen, and C. Zhao, *CMOS Past, Present and Future*. Elsevier, 2018. [Online]. Available: https://linkinghub.elsevier.com/retrieve/pii/C20160034629

[2] M. T. Bohr and I. A. Young, "CMOS Scaling Trends and Beyond," *IEEE Micro*, vol. 37, no. 6, pp. 20–29, Nov. 2017. [Online]. Available: http://ieeexplore.ieee.org/document/8119702/

[3] B. Calhoun, Yu Cao, Xin Li, Ken Mai, L. Pileggi, R. Rutenbar, and K. Shepard, "Digital Circuit Design Challenges and Opportunities in the Era of Nanoscale CMOS," *Proceedings of the IEEE*, vol. 96, no. 2, pp. 343–365, Feb. 2008. [Online]. Available: http://ieeexplore.ieee.org/document/4403891/

[4] M. Horowitz, E. Alon, D. Patil, S. Naffziger, R. Kumar, and K. Bernstein, "Scaling, power, and the future of CMOS," in *IEEE InternationalElectron Devices Meeting, 2005. IEDM Technical Digest.* Tempe, Arizon, USA: IEEE, 2005, pp. 9–15. [Online]. Available: http://ieeexplore.ieee.org/document/1609253/

[5] T. N. Theis and H.-S. P. Wong, "The End of Moore's Law: A New Beginning for Information Technology," *Computing in Science & Engineering*, vol. 19, no. 2, pp. 41–50, Mar. 2017. [Online]. Available: http://ieeexplore.ieee.org/document/7878935/

[6] D. E. Nikonov and I. A. Young, "Overview of Beyond-CMOS Devices and a Uniform Methodology for Their Benchmarking," *Proceedings of the IEEE*, vol. 101, no. 12, pp. 2498–2533, Dec. 2013. [Online]. Available: http://ieeexplore.ieee.org/document/6527325/

[7] G. Csaba, A. Papp, and W. Porod, "Perspectives of using spin waves for computing and signal processing," *Physics Letters A*, vol. 381, no. 17, pp. 1471–1476, May 2017. [Online]. Available: https://linkinghub.elsevier.com/retrieve/pii/S0375960116316486

[8] A. V. Chumak, "Fundamentals of magnon-based computing," 2019. [Online]. Available: https://arxiv.org/abs/1901.08934

[9] D. D. Stancil and A. Prabhakar, *Spin Waves: Theory and Applications*. Boston, MA: Springer US, 2009. [Online]. Available: https://link.springer.com/10.1007/978-0-387-77865-5

[10] A. Mahmoud, F. Ciubotaru, F. Vanderveken, A. V. Chumak, S. Hamdioui, C. Adelmann, and S. Cotofana, "Introduction to spin wave computing," *Journal of Applied Physics*, vol. 128, no. 16, p. 161101, Oct. 2020. [Online]. Available: https://pubs.aip.org/jap/article/128/16/161101/568458/Introduction-to-spin-wave-computing

[11] S. Klingler, P. Pirro, T. Brächer, B. Leven, B. Hillebrands, and A. V. Chumak, "Design of a spin-wave majority gate employing mode selection," *Applied Physics Letters*, vol. 105, no. 15, p. 152410, Oct. 2014. [Online]. Available: https://pubs.aip.org/apl/article/105/15/152410/385199/Design-of-a-spin-wave-majority-gate-employing-mode

[12] T. Fischer, M. Kewenig, D. A. Bozhko, A. A. Serga, I. I. Syvorotka, F. Ciubotaru, C. Adelmann, B. Hillebrands, and A. V. Chumak, "Experimental prototype of a spin-wave majority gate," *Applied Physics Letters*, vol. 110, no. 15, p. 152401, Apr. 2017. [Online]. Available: https://pubs.aip.org/apl/article/110/15/152401/32983/Experimental-prototype-of-a-spin-wave-majority

[13] F. Ciubotaru, G. Talmelli, T. Devolder, O. Zografos, M. Heyns, C. Adelmann, and I. P. Radu, "First experimental demonstration of a scalable linear majority gate based on spin waves," in *2018 IEEE International Electron Devices Meeting (IEDM)*. San Francisco, CA: IEEE, Dec. 2018, pp. 36.1.1–36.1.4. [Online]. Available: https://ieeexplore.ieee.org/document/8614488/

[14] A. N. Mahmoud, F. Vanderveken, C. Adelmann, F. Ciubotaru, S. Cotofana, and S. Hamdioui, "Spin Wave Normalization Toward All Magnonic Circuits," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 68, no. 1, pp. 536–549, Jan. 2021. [Online]. Available: https://ieeexplore.ieee.org/document/9226456/

[15] A. Mahmoud, F. Vanderveken, C. Adelmann, F. Ciubotaru, S. Hamdioui, and S. Cotofana, "Fan-out enabled spin wave majority gate," *AIP Advances*, vol. 10, no. 3, p. 035119, Mar. 2020. [Online]. Available: https://pubs.aip.org/adv/article/10/3/035119/1037239/Fan-out-enabled-spin-wave-majority-gate

[16] A. Mahmoud, C. Adelmann, F. Vanderveken, S. Cotofana, F. Ciubotaru, and S. Hamdioui, "Fan-out of 2 Triangle Shape Spin Wave Logic Gates," in *2021 Design, Automation & Test in Europe Conference & Exhibition (DATE)*. Grenoble, France: IEEE, Feb. 2021, pp. 948–953. [Online]. Available: https://ieeexplore.ieee.org/document/9474089/

[17] A. Van Zegbroeck, P. Anagnostou, S. Hamdioui, C. Adelmann, F. Ciubotaru, and S. Cotofana, "Spin Wave Threshold Logic Gates," in *Proceedings of the 18th ACM International Symposium on Nanoscale Architectures*. Dresden Germany: ACM, Dec. 2023, pp. 1–6. [Online]. Available: https://dl.acm.org/doi/10.1145/3611315.3633269

[18] S. Muroga, *Threshold logic and its applications*. New York: Wiley-Interscience, 1971.

[19] A. Van Zegbroeck, F. Ciubotaru, P. Anagnostou, F. Meng, C. Adelmann, S. Hamdioui, and S. Cotofana, "Spin Wave Threshold Majority Gate," in *2024 IEEE 24th International Conference on Nanotechnology (NANO)*. Gijon, Spain: IEEE, Jul. 2024, pp. 615–619. [Online]. Available: https://ieeexplore.ieee.org/document/10628869/

[20] T. Nozaki, J. Okabayashi, S. Tamaru, M. Konoto, T. Nozaki, and S. Yuasa, "Understanding voltage-controlled magnetic anisotropy effect at Co/oxide interface," *Scientific Reports*, vol. 13, no. 1, p. 10640, Jun. 2023. [Online]. Available: https://www.nature.com/articles/s41598-023-37422-4

[21] S. Miwa, M. Suzuki, M. Tsujikawa, T. Nozaki, T. Nakamura, M. Shirai, S. Yuasa, and Y. Suzuki, "Perpendicular magnetic anisotropy and its electric-field-induced change at metal-dielectric interfaces," *Journal of Physics D: Applied Physics*, vol. 52, no. 6, p. 063001, Feb. 2019. [Online]. Available: https://iopscience.iop.org/article/10.1088/1361-6463/aaef18

[22] A. Vansteenkiste, J. Leliaert, M. Dvornik, M. Helsen, F. Garcia-Sanchez, and B. Van Waeyenberge, "The design and verification of MuMax3," *AIP Advances*, vol. 4, no. 10, p. 107133, Oct. 2014. [Online]. Available: https://pubs.aip.org/adv/article/4/10/107133/584191/The-design-and-verification-of-MuMax3

[23] F. Xue, N. Sato, C. Bi, J. Hu, J. He, and S. X. Wang, "Large voltage control of magnetic anisotropy in CoFeB/MgO/OX structures at room temperature," *APL Materials*, vol. 7, no. 10, p. 101112, Oct. 2019. [Online]. Available: https://pubs.aip.org/apm/article/7/10/101112/149106/Large-voltage-control-of-magnetic-anisotropy-in

[24] L. Amarù, P.-E. Gaillardon, and G. De Micheli, "The EPFL Combinational Benchmark Suite," in *Proceedings of the 24th International Workshop on Logic & Synthesis (IWLS)*, 2015. [Online]. Available: https://infoscience.epfl.ch/handle/20.500.14299/113476

[25] L. Amaru, P.-E. Gaillardon, and G. De Micheli, "Majority-Inverter Graph: A New Paradigm for Logic Optimization," *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, vol. 35, no. 5, pp. 806–819, May 2016. [Online]. Available: http://ieeexplore.ieee.org/document/7293649/

[26] O. Zografos, A. Vaysset, B. Sorée, and P. Raghavan, "Spin-Based Majority Computation," in *Beyond-CMOS Technologies for Next Generation Computer Design*, R. O. Topaloglu and H.-S. P. Wong, Eds. Cham: Springer International Publishing, 2019, pp. 231–262.

[27] P. Horowitz and W. Hill, *The art of electronics*, 2nd ed. Cambridge: Cambridge Univ. Press, 1989.

[28] P. E. Allen, *CMOS analog circuit design*, third edition ed., ser. The Oxford series in electrical and computer engineering. New York: Oxford University Press, USA, 2012.