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Testing STT-MRAMs: Do We Need Magnets in our Automated Test Equipment?

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***Abstract*—The Spin-Transfer Torque Magnetic Random Access Memory (STT-MRAM) is on its way to commercialization. However, the development of high-quality test solutions for STT-MRAMs poses challenges due to the specific working mechanism of the core element of the STT-MRAM bit cells, i.e., the magnetic tunnel junction (MTJ), which involves both a magnetic field and spin-transfer torque. This property can introduce defects unique to MTJs which may escape from test programs that consist solely of functional write and read operations, like march tests. Hence, it is important to develop test solutions that go beyond conventional march tests. This paper explores the effect of applying an external magnetic field (H_{ext}) on the test quality and test time of STT-MRAMs, which could be achieved by integrating one or more magnets in the Automated Test Equipment (ATE) setup. A framework for these so-called H_{ext}-assisted tests is presented and implemented for all known conventional and unique defects. The paper demonstrates that the H_{ext}-assisted tests offer superior coverage and/or lower test time compared to regular functional tests, like march tests. The effectiveness of these tests are validated through silicon measurements.**

***Index Terms*—STT-MRAM, test development, design for test, defect, magnetic field, MTJ, spin-transfer torque.**

I. Introduction

The Spin-Transfer Torque Magnetic Random Access Memory (STT-MRAM) is on the way to commercialization, thanks to its competitive write performance, endurance, retention, and low power consumption [1]. Since the initial product in 2006, world-leading foundries have entered the MRAM market, and STT-MRAMs are applied in a wide range of applications, like embedded systems, computing-in-memory systems, and are considered potential replacements for SRAMs [1–3]. However, the further development of STT-MRAMs' practical usage still faces critical challenges, one of which is to develop short, high-quality tests to enable high-volume production.

Prior work on STT-MRAM testing can be classified according to the different defect types into two categories: (1) the conventional defects outside MTJs, like opens and shorts [4–9]; (2) the unique defects inside MTJs, like pinholes and back-hopping [10,11]. To detect conventional defects, researchers extend what has been done on traditional memories, like DRAMs and SRAMs [12,13], to STT-MRAMs [4–9]; they inject defects modeled as resistors, and perform fault modeling by observing MRAM's faulty behavior in SPICE simulations. However, this conventional approach fails to deliver high-quality tests as it does not properly consider the specific working mechanism of MTJs, which may cause unique defects that cannot be modeled as linear resistors [11,14]. To solve this challenge, the Device-Aware Test (DAT) is introduced, in which compact models for defective MTJs are designed by incorporating the impact of physical (manufacturing) defects on electrical and magnetic behavior [10,15,16]. Both approaches have obtained accurate defect and fault models, however, they primarily rely on functional tests (e.g., march tests) or design-for-test (DfT) [5,10,17,18]. functional tests exhibit low defect coverage [5,10,18], since they fail to extract non-linear MTJ faulty behaviors (e.g., in the presence of pinholes [19]). Besides, DfT incurs extra costs as it requires additional chip area for circuits [5,18]. Further improvement of STT-MRAM manufacturing requires better test solutions with a low escape rate and low test cost.

This paper investigates the effect of applying the external magnetic field (H_{ext}) on the test coverage and test time for STT-MRAMs; applying H_{ext} in tests can be realized by integrating magnets into the Automated Test Equipment (ATE). We first conduct a physical analysis to elucidate the role of H_{ext} and Spin Transfer Torque (STT) in MTJ switching, the insights of which serve as the foundation of the following so-called H_{ext}-assisted test development. Then, practical implementations of H_{ext}-assisted tests are presented for both conventional and unique defects, whose effectiveness is validated through silicon measurements. The results demonstrate that H_{ext}-assisted tests can effectively lower the escape rate and/or expedite tests for multiple defects. The contributions of the paper are the following:

- Perform a physical analysis of the impact of H_{ext} on MTJ switching.
- Define a framework of H_{ext}-assisted test development for both conventional and unique defects.
- Design H_{ext}-assisted tests for all known defects, and, as examples, detail the process for two unique defects.
- Validate H_{ext}-assisted tests by silicon measurements.
- Discuss merits and shortcomings of H_{ext}-assisted tests.

The rest of this paper is organized as follows. Section II introduces the basics of STT-MRAMs. Section III presents the framework for H_{ext}-assisted test development. Section IV and Section V design H_{ext}-assisted tests for Synthetic Anti-Ferromagnet Flip (SAFF) and Back-Hopping (BH) respectively. Section VI shows the merits, shortcomings, and costs of H_{ext}-assisted tests. Section VII concludes this paper.

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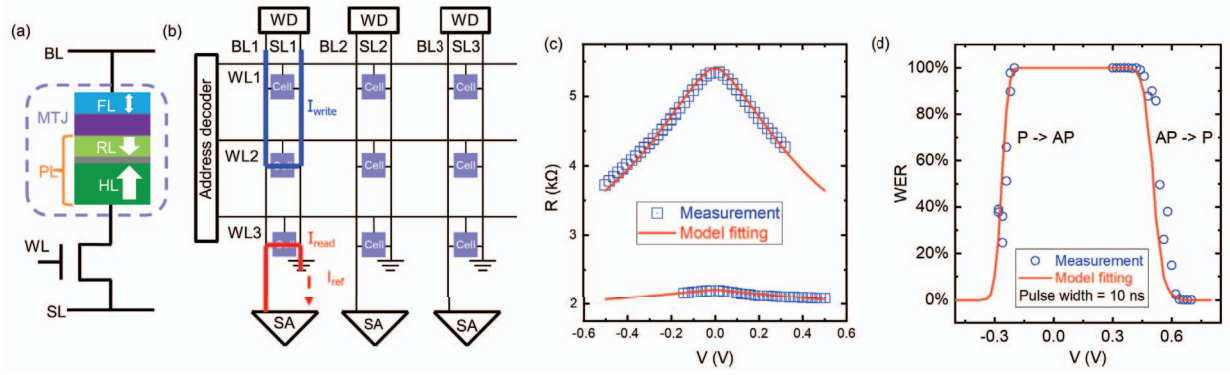

Fig. 1. (a) Simplified MTJ stack and 1T-1M cell, (b) 3×3 STT-MRAM array, (c) R-V measurement, (d) WER measurement

II. Background

A. MTJ device

The fundamental data-recording element in STT-MRAMs is the MTJ; it demonstrates one-bit data storage by encoding two bi-stable resistance states. Fig. 1(a) presents a simplified schematic of an MTJ [20]. Typically, the MTJ consists of an ultra-thin dielectric Tunnel Barrier (TB) sandwiched between the Free Layer (FL) and the Pinned Layer (PL). The FL is a thin ferromagnetic layer (e.g., $1\,\mathrm{nm}$). The TB is a thin insulator made of MgO with the thickness of $1\,\mathrm{nm}$ in this work. The PL is a multi-layer stack composed of a Reference Layer (RL), a thin metal spacer, and a thick Hard Layer (HL). The RL is a thin ferromagnetic layer that is anti-ferromagnetically coupled to the HL through the spacer, resulting in opposite magnetization directions between the two layers. The HL is a thick and stable ferromagnetic layer.

When a current flows through the device, it offers STT to the FL, which may switch magnetization of the FL to be either parallel (P) or anti-parallel (AP) to that of the RL. The MTJ resistance is determined by the FL magnetization direction: when magnetization of the FL and the RL are in parallel, the MTJ presents low resistance (R_P), described as P state or '0' state; otherwise, when the magnetization of the FL and the RL are anti-parallel, the MTJ is in high resistance (R_{AP}), described as AP state or '1' state.

B. 1T-1M STT-MRAM cell

Fig. 1(a) illustrates the structure and write/read operations of a bottom-pinned 1 Transistor-1 Magnetic Tunnel Junction (1T-1M) bit cell. The cell comprises an N-type Metal-Oxide-Semiconductor Field-Effect Transistor (MOSFET) selector and an MTJ, with three terminals connecting to the Bit Line (BL), Source Line (SL), and Word Line (WL), respectively. During write operations, the voltage of the WL selects the cell and the voltage between the BL and the SL controls the operation type. For instance, the $1w0$ operation refers to connecting BL to V_{DD}, and SL to ground, generating a write current I_{w0} flowing through the MTJ device from the FL to the PL, and switching the MTJ state from AP to P. The tunneling electrons provide STT that switches the FL magnetization from parallel to anti-parallel to that of the RL. On the contrary, a $0w1$ operation refers to offering an opposite current I_{w1} by connecting the BL to ground and the SL to V_{DD}. The MTJ state is switched from P→AP by the reversed STT. For write operations, a write current I_{w} larger than the critical current (I_{c}) is necessary to achieve a high write success rate, and the switching time t_{w} is inversely proportional to $I_{\mathrm{w}}-I_{\mathrm{c}}$ [21]. In read operations, a read current I_{read} being much smaller than I_{c} is offered to detect the MTJ resistance while avoiding unwanted state switches. The sense amplifier is employed to detect the device state, leading to a short read time t_{rd} (e.g., $5\,\mathrm{ns}$) [22].

C. STT-MRAM array

Fig. 1 (b) presents a 3×3 1T-1M STT-MRAM array [23]. In the array, cells in the same row share the same WL, and cells in the same column share the same BL and SL. The peripheral circuit consists of the Write Driver (WD), the address decoder, and the Sense Amplifier (SA). In write operations, the WD offers a write current flowing through the STT-MRAM cell, and switches the MTJ state, represented by the blue line in the figure. In read operations, the SA applies a read pulse to the STT-MRAM cell, and compares the read current (I_{read}, the current through the MJT) with a reference current (I_{ref}), represented by the red line in the figure. If $I_{read}>I_{ref}$, the MTJ is in state '0', otherwise the MTJ is in state '1'.

D. Defect-free MTJ measurement data

In this work, we perform measurements on the MTJs with a critical diameter (i.e., the diameter of the round MTJs) of $60\,\mathrm{nm}$, and the pitch (i.e., the distance between neighboring MTJs) of $90\,\mathrm{nm}$. The pulse width of both write and read operations is $10\,\mathrm{ns}$. The read pulse height is $0.01\,\mathrm{V}$, and the write pulse height is adjustable, which will be described in later sections. Fig. 1 (c) and (d) show the R-V and Write Error Rate (WER) measurement data for defect-free MTJs [24], the details of the measurements are explained in [18] and [10]. The MTJ model [25] is calibrated with the data from the measurements, as presented in the figures.

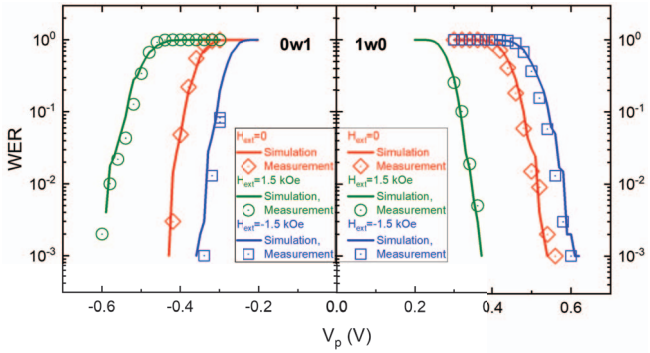

Fig. 2. H_{ext} impact on MTJ switching

III. Why H_{ext} matters in STT-MRAM testing

In this section, we introduce the framework of H_{ext}-assisted tests for STT-MRAM. Firstly, we present the H_{ext} impact on defect-free MTJ performance, conducting a comprehensive analysis of its effects alongside STT on MTJ switching. Subsequently, we extend this physical analysis to explore how H_{ext} influences the behaviors of defective MTJs. The insights gleaned from these analyses serve as the foundation for developing the H_{ext}-assisted test framework.

A. Impact of H_{ext} on defect-free MTJ switching

The MTJ switching mode is classified into three regimes according to the average switching time (t_w): the precessional regime (t_w<10 ns), the dynamic regime (10 ns<t_w<100 ns), and the thermal activation regime (t_w>100 ns) [25]. Next, we perform the physical analysis only in the precessional regime. A similar process can be conducted to the other following two regimes [21], which will not be shown here.

In the precessional regime, the MTJ compact model is designed through the calculation of key electrical parameters, viz. 'I_c' and 't_w', presented as follows [25]:

$$t_w = \frac{\left(C + \ln\left(\frac{\pi^2}{4}\cdot\Delta\right)\right)\cdot e\cdot m}{4\cdot\mu_B\cdot\eta\cdot(I-I_c)} \quad (a)$$
$$I_c = \frac{1}{\eta}\cdot\frac{\alpha\cdot e}{\hbar}\cdot V\cdot M_s\cdot(H_k + H_{ext} + H_s) \quad (b) \qquad (1)$$

C	Euler constant	Δ	Thermal stability
e	unit charge	m	FL magnetization
μ_B	Bohr magneton	η	STT efficiency
I	Current through the MTJ	α	Damping factor
$\hbar$	Reduced Planck constant	V	Volume of the FL
M_s	Saturation magnetization	H_k	Anisotropy magnetic field
H_{ext}	External magnetic field H_{ext}	H_s	Stray field

The MTJ switching process is based on the initial MTJ state and a comparison between the actual write pulse width (t_p) and t_w. For example, in the $1w0$ operation, the initial MTJ state is '1'; when the write pulse is applied with t_p>t_w, the MTJ is switched to '0'.

Fig. 2 presents both the measurements and simulation data for H_{ext} impact on MTJ switching. Clearly external magnetic field favors $1w0$ operations when H_{ext}>0, and it favors $0w1$ operations when H_{ext}<0.

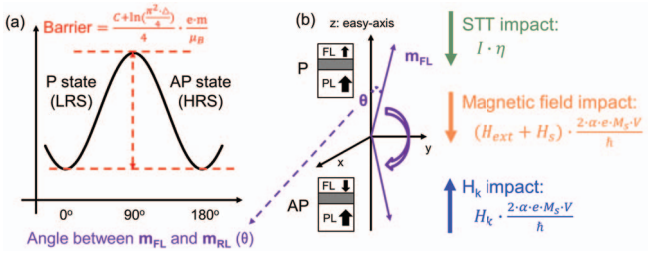

Fig. 3. Impact of the STT and external magnetic field on MTJ switching

B. Analysis of STT and magnetic field in MTJ switching

Although the MTJ model has been proven high-accuracy in circuit simulations [25], it fails to directly present the role of STT effect and magnetic field impact on MTJ switching. Next, we view the MTJ switching process from an alternative perspective. Notice that the new perspective does not change the calculation of the original MTJ model in Eq. 1.

Firstly, we extract the energy barrier E_B between P and AP states [26], presented as follows:

$$E_B = \frac{\left(C + \ln\left(\frac{\pi^2}{4}\cdot\Delta\right)\right)}{4}\cdot\frac{e\cdot m}{\mu_b} \qquad (2)$$

As presented in Fig. 3 (a), E_B from P to AP switching is the same as that of AP to P switching (i.e., P and AP states are asymmetric for FL) [21]. Secondly, we calculate the total input energy E during a write operation with a pulse duration of t_p based on [] and by by substituting Eq. 1 (b) to (a) as:

$$E = t_p\cdot(I\cdot\eta + (H_{ext}+H_s)\cdot\epsilon - H_k\cdot\epsilon)$$
$$\text{where}\quad \epsilon = \frac{2\cdot\alpha\cdot e\cdot M_s\cdot V}{\hbar} \qquad (3)$$

The equation determines MTJ switching by comparing the actual input energy (E) and the barrier E_B. To achieve a successful switching, enough energy E>E_B must be provided. Three components are involved in Eq. 3:

- **STT effect:** $I\cdot\eta$ [26]. The STT is provided by the current (i.e. the electrons) through MTJs.
- **Magnetic field impact:** $(H_{ext}+H_s)\cdot\epsilon$. Here, H_{ext} refers to magnetic fields from all possible external resources, like the equipment. H_{ext} can be either positive or negative. Notice that $H_{ext}=0$ when MTJs work in an ideal environment. H_s is the stray field originating from the ferromagnetic layers (i.e., FL, RL, and HL) of both the MTJ itself and neighboring MTJs [27].
- **Anisotropy magnetic field impact:** $H_k\cdot\epsilon$. H_k is the anisotropy magnetic field (i.e., a constant material parameter aligned with the easy-axis [26], it is an equivalent magnetic field), and it always impedes the switching.

Fig. 3 (b) presents an example of the MTJ switching process, in which the three components either accelerate or impede the switching. The initial angle θ between m_{FL} and

easy-axis (a material cognition, see [28]) is around $0°$ (not equaling $0°$ due to thermal energy of electrons). If the total impact of STT and magnetic field exceeds that of the H_k (i.e., $E>0$), then the MTJ switches in the precessional regime [21]; θ alters from closing $0°$ to closing $180°$ [26].

In the original model (Eq. 1), the impact of the magnetic field is integrated into the calculation of I_c and t_w. Although this integration simplifies the model design, it complicates assessing the magnetic field or STT impact on MTJ switching. In this alternative perspective, however, the role of STT effect and magnetic field impact are disentangled, which favors the following H_{ext}-assisted test design, as we can analyze the contributions of STT and the magnetic field to E independently.

C. H_{ext} impact in presence of a defect

Eq. 3 is valid for both defective and defect-free MTJs, providing valuable insights into understanding and comparing their behaviors under H_{ext}. For example, when applying one write operation to defect-free MTJs, $E>E_B$ and MTJs are switched. However, in the presence of defects, one or several components in Eq. 3 and Eq. 2 (i.e., E_B, STT effect, H_s impact, H_k impact, or H_{ext} impact) are affected, potentially causing faulty behaviors.

In the presence of some defects, logic errors occur and strong faults are sensitized [29]. For instance, a strong spot defect between BL and MTJ, like an unexpectedly high contact resistivity [30], causes a much lowered STT effect [12,31] (i.e., '$I \cdot \eta$' is reduced), which further results in $E \ll E_B$ and sensitizes strong write faults. Functional tests, such as march tests, guarantee the detection of these faults. On the other hand, in the presence of some other defects, logic errors may occur irregularly. For example, in the presence of a weak spot defect between BL and MTJ, E will be disturbed [19]. Consequently, a higher WER is induced and weak faults (i.e., intermittent faults) are sensitized [29]; applying functional tests to detect such faults results in a high escape rate. To obtain a high coverage of the second defect type, DfT methods with specific circuits [7,31,32] are usually applied, which require an additional area on the chip.

In this work, we focus on the H_{ext}-assisted tests for STT-MRAMs, which can improve the defect coverage and/or reduce the test time without additional costs of the chip area, since applying H_{ext} can be realized by integrating magnets into ATE. For example, to improve the coverage of detecting the weak spot defect described above, we can apply a certain H_{ext} to guarantee E less than E_B, and sensitize strong faults. Hence, applying functional tests, like march tests, with H_{ext} can improve the defect coverage of this spot defect.

Here, we only combine H_{ext} with regular functional tests; no DfTs with specific circuits are involved. Although it is possible to further explore the combination of H_{ext}-assisted tests with DfTs to further improve the test quality, it is beyond the scope of this paper.

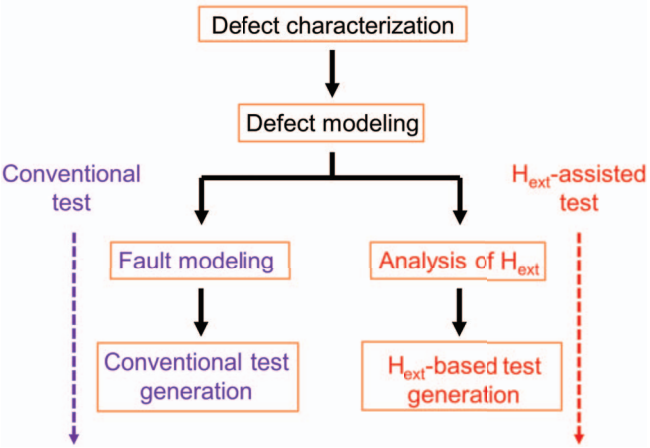

Fig. 4. Comparison of conventional and H_{ext}-assisted test development

D. Framework of H_{ext}-assisted test development

Fig. 4 presents a generic framework of both conventional test (utilizing the DAT method as an example [24]) and H_{ext}-assisted test development [33]. The first two steps are the same for the two test types. The first step 'defect characterization' measures defective MTJ behaviors and studies the physical mechanism of the defect. The second step 'defect modeling' incorporates the impact of physical defects into the technology parameters of the MTJ device and thereafter in the electrical parameters, then develops a compact model of the defective MTJ. For conventional tests, the third step 'fault modeling' describes the STT-MRAM faulty behaviors in the presence of defects through circuit simulations; the fourth step 'conventional test generation' generates test solutions to sensitize faults (here, we only consider functional tests, like march tests). For H_{ext}-assisted test development, the third step 'analysis of H_{ext}' performs the physical analysis on how H_{ext} impacts the components in Eq. 2 and Eq. 3 for defective MTJs; the fourth step 'H_{ext}-assisted test generation' generates H_{ext}-assisted test solutions to detect defects.

E. Targeted defects

In this work, we follow the framework in Fig. 4 to design function and H_{ext}-assisted tests for all known defects in the public domain, and compare these two approaches for each defect type. The results are summarized in TABLE I (see the last section), in which H_{ext}-assisted tests are advantageous in defect coverage and/or time-efficiency for most defects. In the presence of some strong interconnect and contact defects, $E<E_B$ must occur, implying functional tests present full coverage and high time-efficiency in detecting these defects [6,23]. For Pinholes, the defect mechanism (i.e., MgO breaking-down process) is not fully understood, hence the third step in the H_{ext}-assisted test framework cannot be performed.

Next, we will design H_{ext}-assisted tests to detect two defects 'SAFF' [24] and 'BH' [18] as illustrative examples. The framework can be applied to other defects, which this paper will not discuss.

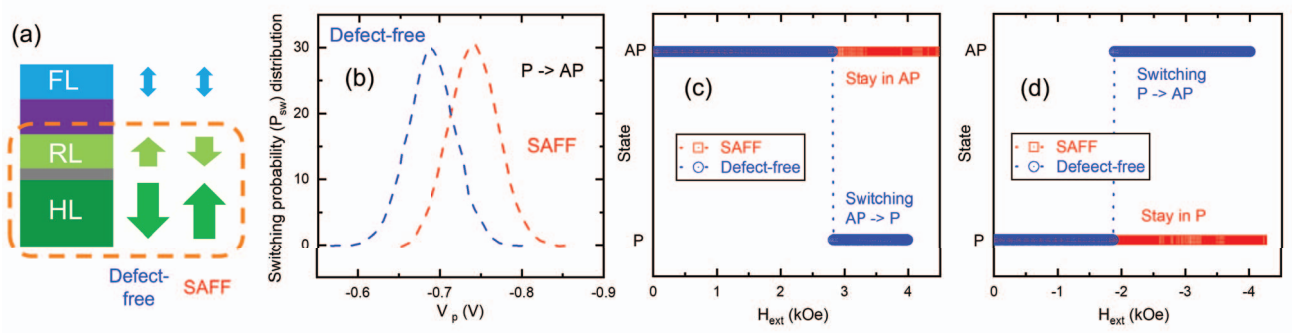

Fig. 5. (a) SAFF mechanism; (b) P_{sw} distribution for SAFF-defective and defect-free MTJs; (c) Validation for the march algorithm Eq. 9; (d) Validation for the march algorithm Eq. 10.

IV. Conventional vs H_{ext}-assisted test for SAFF

In this section, we review the mechanism of the defect 'SAFF', and follow the flow chart in Fig. 4 to design both function and H_{ext}-assisted tests for this defect. Notably, the H_{ext}-assisted test demonstrates superior defect coverage and shorter test time compared to functional tests.

A. Defect mechanism, characterization, and model

Fig. 5 (a) presents the mechanism of SAFF, in which symbols of '↑' and '↓' are applied to reflect the magnetization direction of each ferromagnetic layer. SAFF signifies the unexpected magnetization flipping of HL [17]. Given the strong anti-ferromagnetic coupling strength between HL and RL ($>10\,\mathrm{kOe}$ for our devices), the RL magnetization also flips. Consequently, the magnetization polarity of the FL is reversed between SAFF-defective and defect-free MTJs in either the '1' or 0' state. For example, in the '0' state, the FL magnetization is '↑' for defect-free devices yet '↓' for defective devices (see Fig. 5 (a)).

SAFF has little impact on the MTJ resistance or TMR, since it does not affect the FL of MgO properties [17]. Furthermore, the write operation type is not affected despite that the magnetization of all ferromagnetic layers is flipped in certain states. For example, when the write current flows from FL to RL in defect-free MTJs, the electrons flow from RL to FL, offering the STT and switching the FL magnetization from anti-parallel to parallel (i.e., '↓' to '↑'); it is the $1w0$ operation, the MTJ resistance switches from high to low. On the other hand, when the same current flows in SAFF-defective MTJs, it still offers the STT from RL to FL, yet switches the FL magnetization from '↑' to '↓'; although this switching is reversed from that of defect-free MTJs, it is still the same $1w0$ operation which turns the MTJ resistance from high to low.

However, the flip of FL magnetization implies that the stray field has a reversed impact on it, which impacts the MTJ switching performance. Fig, 5 (b) compares the switching probability (P_{sw}) behaviors between a SAFF-defective and a defect-free MTJ, where the V_p-P_{sw} curve of the defective MTJ is shifted negatively along the V_p axis. This P_{sw} deviation results in an unexpectedly high WER [17].

The SAFF defect model is designed and calibrated with measurements in [17], which will be directly applied in this work. The model reverses all the magnetic field impacts on the FL for the SAFF-defective MTJ.

B. functional test for SAFF

The details of 'fault modeling' and 'conventional test generation' are described in [17], which will not be extended here. The march algorithm to detect SAFF is presented as follows [17]:

$$\text{March-SAFF} = \left\{ \Updownarrow (\mathrm{w1}) ; \Updownarrow (\mathrm{w0}, \mathrm{r0}, \mathrm{w1})^i \right\} . \tag{4}$$

The first element initializes MTJs to be '1'. The second element repeats the three operations of $w0$, $r0$, and $w1$ for 'i' times. It extracts the WER of $1w0$ operations; if the extracted WER is higher than the WER spec (WER_{spec}), SAFF is detected. The march length is $(1 + 3 \cdot i) \cdot N$, where 'i' is determined by WER_{spec} and 'N' is the memory size.

Given the stochasticity in write error occurring, it is very hard, if not impossible, to guarantee 100% detection of SAFF with a reasonable i. For example, if WER_{spec}=10^{-6}, the probability of detecting at least one write error (P_d) with a certain 'i' can be described as:

$$P_d = 1 - (1 - WER)^i \tag{5}$$

When $WER = WER_{spec}$ and $i = 10^6$, $P_d = 63\%$. To guarantee a high defect coverage, 'i' is required to be even larger to distinguish the WER between SAFF-defective and defect-free MTJs (i.e., detect if $WER{>}WER_{spec}$). Besides, P_d can never reach 100% when $WER{<}100\%$. As a result, applying the march algorithm to detect SAFF results in a low defect coverage and low time-efficiency.

C. H_{ext}-assisted test for SAFF

Next, we follow the steps in Fig. 4 to design the H_{ext}-assisted test for SAFF. First, we analyze the defect impact on the four components in Eq. 2 and Eq.3. Since the FL magnetization is flipped in the presence of SAFF, the effect of the magnetic field on the FL is reversed as compared with

defect-free MTJs. Hence, components relating to magnetic fields (i.e., H_s and H_{ext}) become opposite to their original directions (see Eq. 3), yet other components of (i.e., E_B, $H_k \cdot \epsilon$, and $I \cdot \eta$)) remain unchanged, since the FL property is not affected by the defect. Notice that H_k is a material parameter, not the real magnetic field.

If we apply the same $1w0$ operation on both SAFF-defective and defect-free MTJs, the total input energy can be presented as follows:

$$\begin{aligned} \mathrm{E}_{\mathrm{defect-free}} &= t_p \cdot (-H_k \cdot \epsilon + I \cdot \eta + (+H_{ext} + H_s) \cdot \epsilon) \\ \mathrm{E}_{\mathrm{SAFF}} &= t_p \cdot (-H_k \cdot \epsilon + I \cdot \eta + (-H_{ext} - H_s) \cdot \epsilon) \end{aligned} \tag{6}$$

The differences between the two formulas above are the reversed H_s and H_{ext}. If $H_{ext} = 0$, H_s is the only origin of the gap between the input energy, which results in the different P_{sw} behavior in Fig. 5. Subtracting the two formulas in Eq. 6 results into the gap of the input energy (E_{gap}), presented as:

$$E_{gap} = |2 \cdot (H_{ext} + H_s) \cdot \epsilon \cdot t_p| \tag{7}$$

To distinguish SAFF-defective MTJs from defect-free ones, it is critical to enlarge E_{gap} to guarantee switching only occurs in one device type (i.e., only defective MTJs or only defect-free MTJs switch). A preferable way to realize this is by increasing the input energy for the defect-free case while decreasing it for the defective case. Given the fact that H_{ext} has opposite impacts on defect-free and defective case (increasing versus decreasing the input energy), it can be easily used to realize the purpose. For example, by applying a large positive H_{ext}, it achieves $E_{SAFF} \ll E_B$ while $E_{defect-free} \gg E_B$. Thus, defect-free MTJs switch while defective ones stay constant.

Furthermore, if we keep $I = 0$ (i.e., do not perform any write operation) and try to switch the MTJ purely by H_{ext}, the total energy input for defective and defect-free devices can be presented as:

$$\begin{aligned} \mathrm{E}_{\mathrm{defect-free}} &= t_p \cdot (-H_k \cdot + H_{ext} + H_s) \cdot \epsilon > E_B \\ \mathrm{E}_{\mathrm{SAFF}} &= t_p \cdot (-H_k - H_{ext} - H_s) \cdot \epsilon < E_B \end{aligned} \tag{8}$$

To guarantee a successful switching for defect-free MTJs, it requires $E{>}E_B{>}0$, meaning $H_{ext}{>}(H_k - H_s)$. On the other hand, the positive H_{ext} actually stabilizes the FL state for the SAFF-defective MTJ (i.e. it guarantees $E{<}0$), and the device will never switch. Therefore, we can apply a positive H_{ext} and keep it for several microseconds; the actual value of H_{ext} is inconsequential as long as it exceeds a certain threshold, ensuring only defect-free MTJs switch.

The H_{ext}-assisted test for the SAFF defect can be described by the following three steps:

- Perform $\{\Updownarrow (w1)\}$.
- Apply a positive $H_{ext} = H_{1+}$ to the whole chip for several microseconds, then remove H_{ext}.
- Perform $\{\Updownarrow (r0)\}$.

The first step initializes all MTJs to '1' state. The second step applies the H_{ext}, which tries to switch the defect-free MTJ to state '0' while stabilizing the SAFF-defective MTJ state in '1'. Notice that the H_{ext} can be applied to devices on the whole chip simultaneously. The third step checks the final state of MTJs, and the SAFF is detected if MTJs stay in '1'. Here, the H_{ext}-assisted test is presented by the following march algorithm:

$$\{\Updownarrow (w1), H_{1+}, \Updownarrow (r0)\} \tag{9}$$

Fig. 5 (c) presents the R-H loop measurement data for both defective and defect-free MTJs with the initial state '1'. When $H_{1+}{>}2.8\,\mathrm{kOe}$, the defect-free device is switched to '0', yet the defective device still stays in '1'.

A similar test can be applied by initializing MTJ state to '0' and performing a large negative $H_{ext} = H_{1-}$. The march algorithm is presented as:

$$\{\Updownarrow (w0), H_{1-}, \Updownarrow (r1)\} \tag{10}$$

Fig. 5 (d) validates this algorithm. Devices are initialized to '0'. When $H_{1-}{<}{-}1.9\,\mathrm{kOe}$ is applied for several microseconds, the defect-free device is switched to '1', yet the defective device still stays in '0'.

D. Comparison of function and H_{ext}-assisted tests

The march algorithm based on the conventional approach is presented in Eq. 4; the march algorithm of the H_{ext}-assisted approach is presented in Eq. 9 or Eq. 10. Next, we compare the two test methods on the aspect of defect coverage and test time.

1) Defect coverage: The conventional functional tests in Eq. 4 can never guarantee 100% coverage of the SAFF defects. It relies on comparing the difference of WER between defective and defect-free MTJs; this difference is caused by E_{gap} in Eq. 7, which can be small at H_{ext}=0. Besides, the write error occurs stochastically. Consequently, testing SAFF purely by conventional approach results in escapes. On the other hand, the H_{ext}-assisted test applies H_{ext} to enlarge E_{gap}; it switches defect-free MTJs while stabilizing the defective ones. Hence, this approach can guarantee 100% coverage of the SAFF defect.

2) Test time: Eq. 4 only performs read and write operations, and the conventional march test has a length of $(1 + 3i) \cdot N$, where 'i' can be very large considering the low WER_{spec}. The test time of Eq. 9 or Eq. 10 can be divided into two parts: 1) the time for performing write/read operations, with a longer length of which is $2N$; and 2) the time of applying H_{ext}, which takes several microseconds (e.g. $10\,\mathrm{us}$ in our experiments). Here we compare the test time of the two tests by an example: when the pulse width of read and write operation is both $10\,\mathrm{ns}$, the test time applying Eq. 4 to a 256×256 STT-MRAM array is calculated as:

$$256 \cdot 256 \cdot 4 \cdot 10\,\mathrm{ns} \approx 2621\,\mathrm{us}, \quad \text{when} \quad i = 1 \tag{11}$$

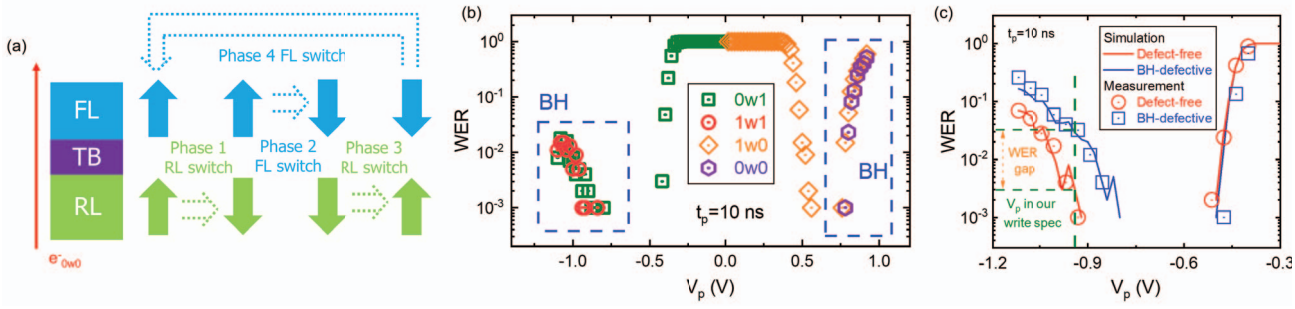

Fig. 6. (a) BH mechanism in $0w0$ (b) Pulse I-V measurement of BH (c) Comparison of BH-defective and defect-free MTJs

The test time applying Eq. 10 is calculated as:

$$256 \cdot 256 \cdot 2 \cdot 10\,\text{ns} + 10\,\text{us} \approx 1321\,\text{us} \tag{12}$$

Since 'i' is much larger in reality, the H_{ext}-assisted test realizes much higher time-efficiency than the regular functional test.

V. Conventional vs H_{ext}-assisted test for BH

In this section, we review the mechanism of the defect 'BH', and follow the flow chart in Fig. 4 to design both function and H_{ext}-assisted tests for this defect. The results demonstrate that the H_{ext}-assisted test achieves a reduced test time while maintaining equivalent defect coverage compared to the functional test.

A. Defect mechanism, characterization, and model

Fig. 6 (a) presents the mechanism of BH occurring in $0w0$ operations (i.e., P to P switching) [11], in which the current flows from FL to RL, and the electrons tunnel from RL to FL (see the arrow of e^-_{0w0} in the figure). The magnetization of both FL and RL is '↑' before writing, and BH occurs following the Four-Phase loop. In each Phase, either FL or RL magnetization switches, and the other layer is stable, described as follows:

- **In Phase 1**, the FL is stable, and the RL is switchable. Two issues are involved in the RL magnetization switching process: 1) the STT effect from the FL, 2) the pinning effect from the HL. The pinning effect means that the RL magnetization direction is forced to keep the same as that of HL through the ferromagnetic coupling [34]. A specific parameter 'equivalent pinning magnetic field' (H_p) is introduced to the strength of the pinning effect to design the BH defect model [18]. This pinning effect is strong for defect-free MTJs (i.e., a large H_p), but weak in BH-defective MTJs. Under strong stress (i.e., high $|V_p|$), the STT switches the RL magnetization from '↑' to '↓'.
- **In Phase 2**, the FL is switchable, and the RL is stable. The FL switches from'↑' to '↓' by the STT from RL.
- **In Phase 3**, the FL is stable, and the RL is switchable. The RL switches from '↓' to '↑' by the STT from FL.
- **In Phase 4**, the FL is switchable, and the RL is stable. Compared with Phase 2, the magnetization of both FL and RL is flipped; hence the STT offered by the RL is also reversed. The STT form RL switches the FL magnetization from '↓' to '↑'. The end of Phase 4 indicates a new start of Phase 1, hence the four phases form a complete loop, and the MTJ state oscillates permanently in this loop.

During the whole write operation, the MTJ state oscillates within this loop. The occurrence of write errors depends on the final phase the MTJ stays at the end of write operations. If it stops at Phase 3 or 4, the FL is switched to '↓' and the write error occurs; conversely, if it stops at Phase 1 or 2, the FL remains (or be switched back to) '↑', preventing write errors. Hence, a high, albeit never reaching 100% WER is observed in the presence of BH. The physical mechanism of BH occurring in other write operations (i.e., $1w0$, $1w1$, and $0w0$) are similar, which will not be discussed here.

Fig. 6 (b) presents the WER behavior in different write operations. In $0w1$ and $1w0$ operations, first the normal switching occurs under weak stress (i.e., at low $|V_p|$ where WER decreases with $|V_p|$ increasing), then BH occurs and the BH-induced WER is observed under strong stress (i.e., at high $|V_p|$ where WER increases with $|V_p|$ increasing). With $1w1$ and $0w0$ operations, no normal switching occurs, and all write errors are BH-induced. The BH-induced WER behavior is the same between $1w1$ and $0w1$ operations, and the same between $0w0$ and $1w0$ operations, implying the write operation type, rather than the initial MTJ state, plays the critical role in BH occurring.

Due to the limited strength of the pinning effect between RL and HL (i.e., H_p cannot be infinite), the RL can never be completely stable, implying BH exists in all MTJs as long as $|V_p|$ large enough. However, only MTJs with a weak pinning effect are considered BH-defective, where a high BH-induced WER exceeding WER_{spec} is observed in the write spec. Fig. 6 (c) compares the WER behavior between BH-defective and defect-free MTJs under $0w1$. While both devices exhibit similar performance in normal switching, the defect-free MTJ demonstrates a BH-induced WER approximately one order of magnitude lower than that of the defective one at a proper $|V_p|$ (e.g., $V_p = -0.95V$ in the picture).

Details of the BH defect model are described in [18], which forms the four-phase loop by calculating the key parameters I_c and t_w for the switching layer in each Phase; it iterates through the MTJ state within this loop one by one. The model is fitted with measurement data for both defective and defect-

free MTJs, as presented in Fig. 6 (c).

B. functional test for BH

The steps of 'fault modeling' and 'conventional test generation' are described in [18]. The march algorithm for detecting BH is presented as follows:

$$\begin{aligned} &\text{March} - \text{BH} = \left\{ \Updownarrow (\text{w0}, \text{r0})^i \right\} \quad (a) \\ &\qquad \text{or} \\ &\text{March} - \text{BH} = \left\{ \Updownarrow (\text{w1}, \text{r1})^i \right\} \quad (b) \end{aligned} \tag{13}$$

The two march algorithms extract the WER in $1w1$ or $0w0$ operations, and the BH is detected if the extracted $WER{>}WER_{spec}$. The march length is $(2 \cdot i) \cdot N$, where 'i' is determined by WER_{spec}. $1w0$ and $0w1$ operations are not selected to avoid write errors due to normal switching failing affecting the test.

Given the stochasticity of the BH mechanism, the same process as Eq. 4 can be applied to evaluate the defect coverage and test time of applying Eq. 5 to detect BH. Similar to the test of SAFF, 'i' can be large due to the low WER_{spec}.

C. H_{ext}-assisted test for BH

Next, we follow the steps in Fig. 4, to design H_{ext}-assisted test for BH. First, we analyze the BH impact on four components in Eq. 2 and Eq.3. Since the defect does not affect the material property of either FL or RL, it does not affect the four components. However, due to the four-phase loop of BH occurring, we must consider the input energy E for RL and FL switching in each phase separately to analyze the H_{ext} impact on BH-induced WER (see Fig. 6 (a)). Here, we apply Eq. 3 to each phase in the $0w0$ operation, presented as follows:

$$\begin{aligned} &P1 : t_{w\_1} \cdot (I \cdot \eta + (-H_{ext} - H_s - H_{k\_RL} - H_p) \cdot \epsilon_{RL}) = E_{B\_RL} \\ &P2 : t_{w\_2} \cdot (I \cdot \eta + (-H_{ext} - H_s - H_{k\_FL}) \cdot \epsilon_{FL}) = E_{B\_FL} \\ &P3 : t_{w\_3} \cdot (I \cdot \eta + (+H_{ext} + H_s - H_{k\_RL}) \cdot \epsilon_{RL}) = E_{B\_RL} \\ &P4 : t_{w\_4} \cdot (I \cdot \eta + (+H_{ext} + H_s - H_{k\_FL}) \cdot \epsilon_{FL}) = E_{B\_FL} \end{aligned} \tag{14}$$

Here, H_{k_FL} & H_{k_RL}, E_{B_FL} & E_{B_RL}, ϵ_{FL} & ϵ_{RL} refer to H_k, E_B, and ϵ of FL and RL separately; H_p is introduced in the model, which is the only parameter affected by BH (i.e., represents the defect strength) $t_{w\_i}, i = (1, 2, 3, 4)$ indicates the t_w for each phase in Fig. 6 (a), which will occur sequentially to form the loop. For example, the MTJ state is initially in 'P', and the RL is switched after t_{w_1}. Subsequently, the FL is switched further after t_{w_2}, and so forth. After t_{w_4}, the MTJ returns to the initial 'P' state, and the loop is restarted. In a single write operation, each phase may occur multiple times. To improve the time-efficiency of detecting BH, it is critical to increase the BH-induced WER, which is determined by the distribution of t_{w_i}. For example, if t_{w_1} and t_{w_2} become larger, t_{w_3} and t_{w_4} become smaller, BH-induced WER is reduced.

For the convenience of the following analysis, we define:

$$\gamma_i = \frac{E_{B\_RL\ or\ B\_FL}}{t_{w\_i}}, i = (1, 2, 3, 4) \tag{15}$$

$$\Gamma = \gamma_1 + \gamma_2 - \gamma_3 - \gamma_4 \tag{16}$$

Increasing BH-induced WER implies enlarging Γ, which can be achieved by applying the H_{ext} with a certain direction. When we apply a certain $H_{ext} = H_1$, the impact of H_{ext} on Γ is defined as $\Delta\Gamma(H_1) = \Gamma(H_{ext} = H_1) - \Gamma(H_{ext} = 0)$:

$$\Delta\Gamma(H_1) = -2 \cdot H_1 \cdot (\epsilon_{FL} + \epsilon_{RL}) \tag{17}$$

For the $0w0$ operation, if $H_1{<}0$, $\Delta\Gamma(H_1){>}0$, Γ increases, and BH-induced WER increases. Fig. 7 (a) presents the H_{ext} impact on BH-induced WER in the $0w0$ operation. With the same V_p, a higher BH-induced WER is observed with the negative H_{ext}; BH-induced WER increases with the $|H_{ext}|$ increasing. Notice that when we apply a large positive H_{ext}, few BH-induced write errors occur because the H_{ext} stabilizes the RL and avoids Phase 1 taking place; hence related lines are not shown in the figure. A similar analysis can be performed on the BH occurring in the $1w1$ operation. Fig. 7 (b) presents the H_{ext} impact on BH-induced WER in the $1w1$ operation, where a positive H_{ext} inciting a higher WER at the same V_p.

Fig. 7 (c) compares the H_{ext} impact between the BH-defective and defect-free MTJs in the $0w0$ operation. At the same V_p, BH-induced WER of both MTJs increases under the same negative H_{ext}. A large gap is observed between the two MTJs with or without H_{ext} at a proper V_p. For example, the BH-induced WER of defective MTJ is one order of magnitude higher than that of the defect-free one at $V_p = 0.8V$ either with or without H_{ext}. A similar phenomenon is presented in Fig. 7 (d) with the $1w1$ operation. The simulation result fitted with the measurement data is also presented in figures.

Based on the analysis above, the H_{ext}-assisted test for BH follows three steps:

- Pre-calibration:
  - Find the threshold between defect-free and BH-defective MTJs, i.e., BH-induced WER = WER_{spec} in the $0w0$ operation.
  - Select the proper H_{ext}. Here, a negative $H_{ext} = H_{1-}$ is applied.
  - Find the new threshold between defect-free and BH-defective MTJs under H_{1-}, i.e., BH-induced WER = WER'_{spec} in $0w0$ operations with H_{1-}.
- Perform $\left\{ \Updownarrow (w0r0)^i \right\}$ with H_{1-}.

The first step selects the proper H_{1-} with associated WER'_{spec}, which can be achieved by simulations. For example, here we select $H_{1-} = -0.5\,\text{kOe}$ and $WER'_{spec} = 30\%$, as presented in Fig. 7 (c). The second step extracts the BH-induced WER under H_{1-}, and compares it with WER'_{spec}; if the extracted WER $>WER'_{spec}$, BH is detected. A simplified march algorithm is presented as follows:

$$\{ \Updownarrow (w0, r0)^i_{H1-} \} \tag{18}$$

The march length of the march algorithms is $(2 \cdot i) \cdot N$, where 'i' is determined by WER'_{spec}. A similar process can

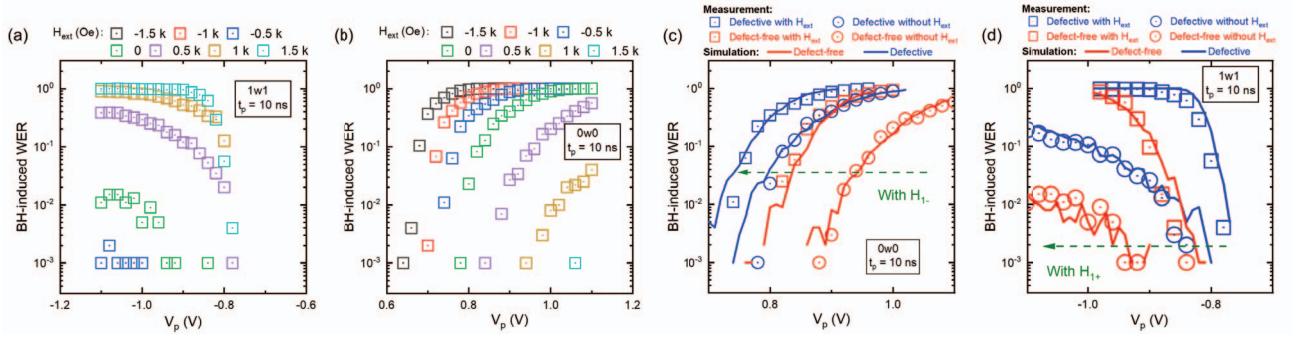

Fig. 7. H_{ext} impact on BH-induced WER with the (a) $0w0$ operation; (b) $1w1$ operation; (c) Comparison of H_{ext} impact on BH-induced WER between BH-defective and defect-free MTJs with the (c) $0w0$ operation; (d) $1w1$ operation

TABLE I. H_{ext}-ASSISTED TESTS FOR DIFFERENT DEFECT TYPES IN STT-MRAM TESTING

Defect	functional tests	H_{ext}-assisted tests	Advantages of H_{ext}-assisted test
Strong interconnect and contact defects [33]	$\{\Updownarrow(w1);\Updownarrow(w0,r0,w1);\Updownarrow(r1)\}$ [33]	Unnecessary	\
Weak interconnect and contact defects [35]	Repeating march algorithm in [33]	$\{\Updownarrow(w1);\Updownarrow(w0,r0)_{H1-};\Updownarrow(w1,r1)_{H1+}\}$	Improve defect coverage
Pinhole [36]	$\left\{\Updownarrow(w1)^i;\Updownarrow(w0,r0)\right\}$ [37]	Unavailable	\
SAFF [17]	$\left\{\Updownarrow(w1);\Updownarrow(w0,r0,w1)^i\right\}$ [17]	$\{\Updownarrow(w1),H_{1+},\Updownarrow(r0)\}$	Improve defect coverage and reduce test time
Intermediate States [38]	$\left\{\Updownarrow(w0,r0,w1,r1)^i\right\}$ [39]	$\left\{\Updownarrow(w0,r0,w1,r1)^i_{H1-}\right\}$	Reduce test time
BH [11]	$\left\{\Updownarrow(w1,r1)^i\right\}$ [33]	$\{\Updownarrow(w0,r0)^i_{H1-}\}$	Reduce test time

be performed with $1w1$ operations. A positive $H_{ext} = H_{1+}$ is applied, and the march algorithm is presented as follows:

$$\{\Updownarrow(w1,r1)^i_{H1+}\} \tag{19}$$

D. Comparison of function and H_{ext}-assisted tests

The march algorithm of the conventional test is presented in Eq. 13; the march algorithm of the H_{ext}-assisted test is presented in Eq. 18 and Eq. 19. Next, we compare the two test methods regarding defect coverage and test time.

1) Defect coverage: Due to the intrinsic stochastic mechanism of write errors, both two methods cannot guarantee 100% coverage of the BH defect.

2) Test time: The march length of the march algorithms in both two methods is $(2\cdot i)\cdot N$, where 'i' is determined by either WER_{spec} or WER'_{spec}, as presented in Eq. 5. Assuming both two testing methods are required to reach the same defect coverage (e.g., the same P_d in Eq. 5), due that WER'_{spec}>WER_{spec}, a much shorter test time can be realized by H_{ext}-assisted tests. For example, if $WER_{spec} = 10^{-4}$, $WER'_{spec} = 0.3$, to guarantee $P_d = 99.9\%$, $i = 70000$ by functional tests, and $i = 13$ is required by H_{ext}-assisted tests. The test time is reduced by 99.98% by H_{ext}-assisted tests.

VI. DISCUSSION

The comparison of functional tests and H_{ext}-assisted tests for each defect is demonstrated in TABLE I, where two examples are presented in Sec. IV and Sec. V. H_{ext}-assisted tests for other defects can also be designed by flowing steps in Fig. 4, which will not be extended here. Next, we discuss advantages, shortcomings, and costs of H_{ext}-assisted tests.

A. Advantages

Advantages of H_{ext}-assisted tests are stated as follows:

1) Improve defect coverage and/or reduce test time without costs of chip area: TABLE I demonstrates that H_{ext}-assisted tests can realize a high defect coverage and a short test time without costs of additional chip area. Especially, since H_{ext} can be applied to devices in the whole chip simultaneously, which further reduces the test time (see the case of detecting SAFF). To realize the same defect coverage or time-efficiency, DfTs with specific circuit designs are usually applied [7,18,31,32], which requires additional chip area. For example, the DfT for BH in [18] requires an additional current mirror and a NOR gate for each column. Notice that, in large-scale manufacturing, a small saving on each chip (e.g., saving chip area) suggests a significant overall cost saving.

2) Flexible in test design: The H_{ext} can be continuously applied by Automated Testing Equipment (ATE) [40], which offers high flexibility in the test design; any H_{ext} value (not exceeding the maximum) can be applied in tests for STT-MRAM. On the other hand, DfTs with specific circuits have relatively low flexibility [41,42]. For example, the DfT 'weak write' can offer only a few choices of different write pulse heights [42].

B. Shortcomings and costs

Shortcomings and costs of H_{ext}-assisted tests are stated as follows:

1) Cost of equipment: To perform write/read operations and apply H_{ext} simultaneously, specific ATE is required [40], implying additional cost for the test equipment.

2) Time-compatibility: Switching between different magnetic fields requires a longer time (e.g., several microseconds for current ATE [40]) than applying operations (e.g., $10\,\mathrm{ns}$ in this work), hence some H_{ext}-assisted tests may cause low time-efficiency. For example, the march algorithm $\{\Updownarrow (w0_{H1}, w1_{H2})\}$ applies $w0$ with $H_{ext} = H_1$, then immediately applies $w1$ under $H_{ext} = H_2$. This algorithm necessitates a long waiting period of several microseconds for switching H_1 to H_2, despite the write operation requiring only $10\,\mathrm{ns}$; hence indicates low time efficiency. On the other hand, the march algorithm $\{\Updownarrow (w0_{H1}, w1_{H1})\}$ applies both write operations with the same H_1, avoiding switching H_{ext} in the whole test process, hence with higher time-efficiency.

VII. Conclusion

In this work, we investigate the effect of applying H_{ext} on the test coverage and test time for STT-MRAMs. The framework of so-called H_{ext}-assisted tests is proposed and applied to all defects we know in the public domain. Although H_{ext}-assisted tests require extra magnets in ATE, they present a higher defect coverage and/or lower test time compared with regular functional tests, like march tests. The effectiveness of H_{ext}-assisted tests is validated through silicon measurements.

To address the question posed in the title - whether magnets are needed in ATE - various factors must be considered, including the nature of targeted defects and the cost-benefit balancing. Following the framework of this paper, H_{ext}-assisted tests can be designed for each defect, with a thorough analysis of their advantages, drawbacks, and costs. This comprehensive evaluation will assist in deciding the necessity of magnets in ATE.

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