# A New Low-Noise 100-MHz Balanced Relaxation Oscillator

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*Abstract*—**A new fully balanced architecture for high-frequency, low-noise relaxation oscillators is presented. Differential operation is achieved with the use of two grounded capacitors utilizing the circuit parasitics. Bypassing of the regenerative memory function in the oscillator benefits both high-speed and low-noise operation. In addition a detailed analysis of phase noise in relaxation oscillators is performed. Results obtained from a test chip have verified both the viability of the new oscillator concept and the developed phase-noise theory. The oscillator circuit has been realized in a medium-frequency ($f_\tau = 3$ GHz) bipolar process. The tuning range extends to 150 MHz. At an oscillation frequency of 115 MHz, measured phase noise was −118 dBc/Hz at 1-MHz distance from the carrier.**

## I. INTRODUCTION

THE availability of high-performance high-frequency integrated oscillators would be a big step forward in analog integrated circuit design. However, the known integrated relaxation oscillators suffer from bad noise behavior and excessive temperature drift. When the oscillator is used in a PLL, which is often the case, drift is no longer a problem. The remaining bad noise behavior excludes the use of integrated relaxation oscillators in a lot of telecommunication applications. In order to design relaxation oscillators with lower phase noise, insight into the origins of phase noise is a prerequisite.

Using the method described by Abidi and Meyer [1], an indication of the time jitter of a relaxation oscillator can be obtained. However, because time correlations are not included in this method, it is not easy also to predict the phase-noise spectrum as measured with a spectrum analyzer. Therefore, prior to the design of the oscillator, an analysis of the origins of phase noise was performed. Expressions predicting the phase-noise spectrum due to different noise sources are presented.

Another problem in traditional relaxation oscillators, based on the well-known emitter-coupled multivibrator (Fig. 1), is the presence of parasitic capacitors at each side of the floating timing capacitor. As the parasitics are not used as a part of the timing capacitor $C$, this capacitor has to be considerably larger than the parasitics in order assure proper functioning of the oscillator. This might cause problems in the design of high-frequency oscillators with small on-chip timing capacitors, especially because integrated floating capacitors have relatively large parasitic capacitors to the substrate. For high-frequency oscillators a topology that uses the parasitics as a part of the timing capacitors is therefore preferable [2]–[4].

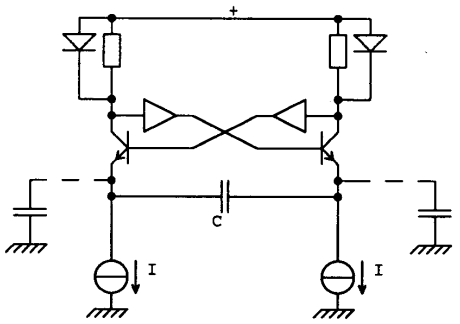


Fig. 1. Emitter-coupled multivibrator.

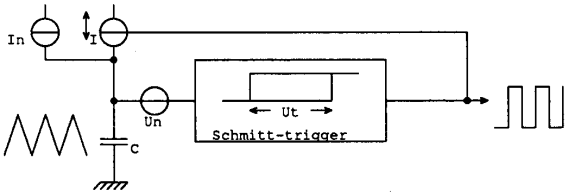


Fig. 2. Basic relaxation oscillator with noise sources.

The mentioned problem with the emitter-coupled multivibrator architecture is that it is not really a balanced version of the basic relaxation or Schmitt-trigger oscillator with grounded capacitor, as depicted in Fig. 2. As a differential architecture is desired, in order to reduce the sensitivity to power-supply variations, a new fully balanced relaxation oscillator with two grounded timing capacitors has been designed. The absence of a floating capacitor and the possibility of much smaller timing capacitors are important advantages of such a new oscillator topology. A 100-MHz low-noise version of this new oscillator has been realized in a medium-frequency bipolar

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process ($f_\tau = 3$ GHz). Measurement results on the integrated oscillator will be presented.

## II. Phase Noise in Relaxation Oscillators

For the analysis of phase noise the basic diagram of a relaxation oscillator, depicted in Fig. 2, is used. The fundamental oscillation frequency is

$$f_0 = \frac{I}{2U_t C}. \tag{1}$$

Sources of phase noise are a noise current $i_n$, parallel to current $I$, and a noise voltage $u_n$ in series with the timing capacitor. Depending on the frequency of the noise sources, different methods will be used to calculate the resulting phase noise. If the noise frequency is much smaller than the oscillation frequency $f_0$, there is only normal frequency modulation of the oscillator. For higher noise frequencies the influence of the switching action will also become significant. Due to the switching action, high-frequency noise will be folded back. These aliased noise sources will also modulate the oscillation frequency.

### A. Low-Frequency Noise

First, the influence of a small low-frequency sine-wave component of a noise current $i_n$ with frequency $f_m$ ($f_m \ll f_0$) will be calculated. The peak frequency deviation $\Delta f_0$ due to this current is readily obtained from (1):

$$\Delta f_0 = \frac{i_n(f_m)}{2U_t C}. \tag{2}$$

The ratio between the carrier power and the power of a sideband at a distance $f_m$ from the carrier can be expressed in terms of $\Delta f_0$ and $f_m$ using modulation theory [5]. Substitution of (1) and (2) in this expression yields

$$\frac{P_{\text{carrier}}}{P_{\text{noise}}(f_0 + f_m)} = \left(\frac{\Delta f_0}{2f_m}\right)^2 = \frac{i_n^2(f_m)}{4I^2}\left(\frac{f_0}{f_m}\right)^2. \tag{3}$$

Applying this method to all the spectral components of a noise current $i_n$ yields an expression for the resulting single-sided spectral phase-noise density $\mathcal{L}(f_m)$ of $i_n$ by simply summing all of the individual contributions. Assuming a white-noise current with spectral density $S(i_n)$ equal to $4kT/R_i$, the resulting phase-noise density is

$$\mathcal{L}(f_m) = \frac{S(i_n)}{2I^2}\left(\frac{f_0}{f_m}\right)^2 = \frac{2kT}{I^2 R_i}\left(\frac{f_0}{f_m}\right)^2 \tag{4}$$

where $R_i$ is the equivalent output noise resistance of the controlled current source $I$. The maximum value of $R_i$ for an integrated current source can be obtained if a large emitter resistor $R$ is used [6]. In that case the output noise is approximately $4kT/R$. The product $I^2R$ that would appear in (4) is exactly the power dissipation in the resistor $R$. In order to obtain a certain value of $\mathcal{L}(f_m)$ a certain minimum power consumption in the current sources is unavoidable.

Besides a noise current there will unavoidably be a noise voltage $u_n$ in series with the timing capacitor $C$. Starting with a small sine-wave low-frequency component with frequency $f_m$ of a noise voltage source $u_n$ with a spectral density $4kTR_u$, the same method as stated above can be applied. $R_u$ is the equivalent noise resistance of the noise sources in series with $C$. The approximated expression for the resulting phase-noise density is

$$\mathcal{L}(f_m) = \frac{2kTR_u}{U_t^2}\left(\frac{f_0}{f_m}\right)^2. \tag{5}$$

The lowest possible value of $R_u$ for a given $U_t$ will depend on the used technology. For a bipolar realization this might usually be the base resistance of the transistors.

### B. High-Frequency Noise

The switching action, inherent in relaxation oscillators, will fold back high-frequency noise. The result of this sampling process is low-frequency modulation of the oscillation signal. In case of high-frequency current noise, the resulting phase noise may be neglected because of the integrating action of the timing capacitor. Therefore, the total phase-noise density due to a white current noise $i_n$ is given by (4).

Aliased high-frequency noise components from $u_n$, however, will dominate the influence of the low-frequency components of $u_n$. Boon *et al.* [7] have investigated the phase noise that results from this sampling process. If the spectral density $S(u_n)$ of the white-noise source $u_n$ is again $4kTR_u$, the resulting phase-noise density has been calculated to be

$$\mathcal{L}(f_m) = \alpha\frac{16kTR_u}{U_t^2}\left(\frac{f_0}{f_m}\right)^2. \tag{6}$$

The factor $\alpha$ represents the number of aliased spectra and is given by

$$\alpha = \frac{B_{conv}}{2f_0}. \tag{7}$$

In this expression $B_{conv}$ is the effective noise conversion bandwidth. In case of high-frequency oscillators $B_{conv}$ will usually be determined by a dominant pole in the threshold detector. This is a result of the fact that the threshold detector will not be able to react on noise sources with frequencies above the frequency of this pole. The factor $2f_0$ in (7) is a consequence of the fact that only noise components at odd multiples of $f_0$ seriously harm the oscillation stability [7].

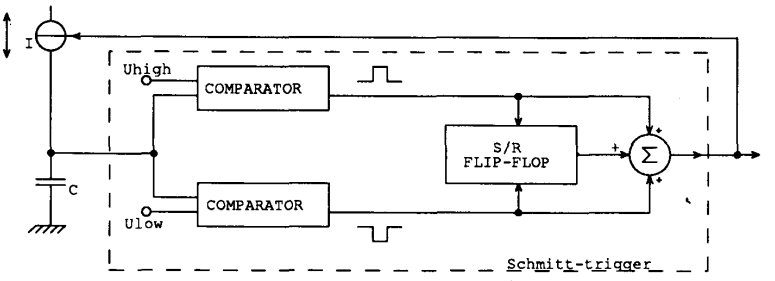



Fig. 3. Relaxation oscillator with bypassed memory function for low-noise, high-speed operation.

Therefore, besides a large $U_t$ and a small $u_n$, a small value of $\alpha$ is also necessary for a low-noise oscillator. But the low-pass action needed for a small value of $\alpha$ will also introduce time delay in the oscillator. This will harm the linearity of the oscillator tuning curve. High linearity and low noise are therefore conflicting demands made on a relaxation oscillator unless linearizing circuitry is added.

## III. Low-Noise, High-Speed Architecture

In the introduction we have pointed out our preference for a relaxation oscillator with a grounded timing capacitor. The architecture of a high-frequency low-noise oscillator with grounded capacitor is depicted in Fig. 3. The Schmitt-trigger function has been divided into a threshold comparator and a memory function ($S/R$ flip-flop). The $S/R$ flip-flop is bypassed by the outputs of the voltage comparators. The voltage comparators immediately switch the current switch. The only demand made on the speed of the $S/R$ flip-flop is that it takes over the comparator output state before the comparator is switched off.

The removal of the $S/R$ flip-flop from the signal path is firstly advantageous for high-speed operation. Secondly, it is also advantageous for low-noise operation. From earlier work it is known that, depending on the slope of the driving signal, the switching delay of a Schmitt trigger or flip-flop can be very sensitive to noise [8]. This is a consequence of the regenerative action. The influence of noise on the flip-flop switching time is decreased by means of the insertion of slope amplifiers in front of the flip-flop. The already available voltage comparators can be used for this purpose. Known low-noise oscillators are based on this principle [1], [9]. For very high-frequency oscillators the driving slope of the flip-flop can hardly be amplified anymore by the comparators. Bypassing the memory function will therefore be the only way to further decrease the influence of the flip-flop noise.

In order to reduce the sensitivity to power-supply variations a fully differential architecture is desired. Fig. 4 depicts a diagram of the balanced version of the basic architecture of Fig. 3. Apart from their implementation the operation of both architectures is essentially the same. Supposing equal charging currents $I$ and equal timing capacitors ($C_1 = C_2 = C$), the oscillation frequency of the balanced oscillator is

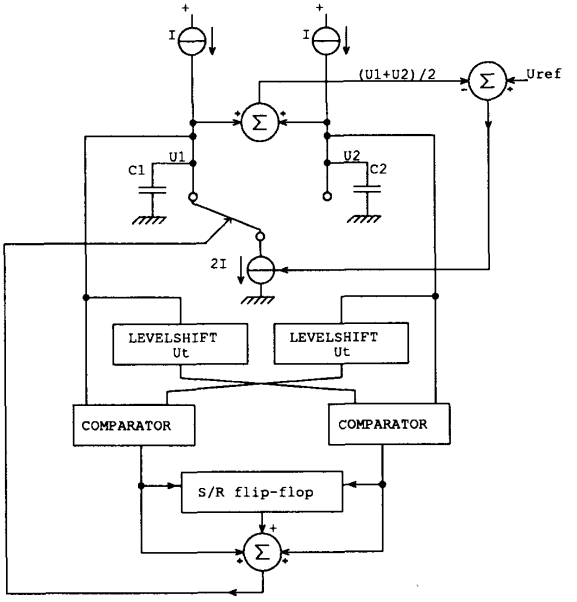



Fig. 4. New balanced relaxation oscillator architecture.

$$f_0 = \frac{I}{2U_t C}. \tag{8}$$

Threshold levels in the balanced architecture are floating instead of related to ground. The voltages at $C_1$ and $C_2$ are now balanced with respect to $U_{\text{ref}}$. Any disturbance between $U_{\text{ref}}$ and the common-mode signal $(U_1 + U_2)/2$ will lead to a correction current in the discharging current source, which will cancel the disturbance. A result of the common-mode feedback loop is the equality of the sum of the charging current sources to the discharging source. Whenever the voltage difference $U_1 - U_2$ is equal to $U_t$, one of the voltage comparators switches. Subsequently, the $S/R$ flip-flop and the current sources will be switched. The results of this operation scheme are opposite triangular waveforms at $C_1$ and $C_2$.

The essential new features of this architecture compared to an earlier reported differential relaxation oscillator [9] are the bypassed memory function and the applied

common-mode feedback. The use of this common-mode feedback is the reason why grounded capacitors still can be used in a differential architecture.

## IV. Circuit

The circuit diagram of an oscillator based on the new proposed architecture has been depicted in Fig. 5(a). As we intended to use the oscillator in a PLL over the frequency range 100–130 MHz, some demands on linearity of the oscillator were made.

### A. Switching Part

The voltages at the timing capacitors are level shifted by $Q2a$, $Q3a$ and $Q2b$, $Q3b$. The threshold $U_t$ is realized by means of the diodes $Q4a$ and $Q4b$. Thus $U_t$ is about 0.7 V. The differential stages $Q5a$, $Q5b$ and $Q6a$, $Q6b$ are used as voltage comparators. The output current of these stages is transformed into a pulse voltage by means of $R2a$ and $R2b$. This pulse voltage switches a next differential stage $Q1a, Q1b$—used as a current switch—and the S/R flip-flop $Q7a, Q7b$. The simulated waveform of the differential voltage $V_s$ across the current switch, as well as the voltage $V_c$ across the timing capacitors, are depicted in Fig. 5(b). It is seen that $V_s$ quickly rises after one of the voltage comparators has been switched on. When the comparator has been switched off again, $V_s$ decreases to a level determined by the flip-flop. This level has been chosen large enough to keep the current switch $Q1a, Q1b$ in the right position. The voltage $V_s$ across the current switch is also used to drive an output buffer.

### B. Common-Mode Loop

The common-mode voltage of the two timing capacitors is obtained by means of $R1a$ and $R1b$. The common-mode signal is level shifted by means of $Q12$–$Q14$. Subsequently, it is transformed into a current by means of a series stage ($Q16$ and $R3$). Neglecting high-frequency poles, the open-loop common-mode transfer function $G(p)$ is thus

$$G(p) = \frac{1}{2pR_3C}. \tag{9}$$

If $C = 2.5$ pF (inclusive parasitics) and $R3 = 400\ \Omega$ the predicted common-mode bandwidth is 80 MHz. Simulations show that other poles in the common-mode loop are nondominant, such that stability of the common-mode loop is assured.

Instead of being fixed to a reference voltage $U_{\text{ref}}$, the common-mode voltage is now determined by the sum of the base–emitter voltages of $Q12$–$Q14$ and $Q16$ and the voltage across $R3$. As the voltage across $R3$ changes proportional to the tuning current $I$, the common-mode voltage will also slightly depend on the tuning current. This construction of the common-mode loop saves an extra voltage reference and avoids the use of p-n-p transistors in the loop. Low-frequency poles due to lateral p-n-p's in the common-mode loop would cause stability problems.

The voltage at $U_r$ has to be approximately equal to the emitter voltage of $Q12$ in order to avoid saturation of either the voltage comparator or the current switch. This can easily be realized by means of the insertion of a transistor between the base of $Q12$ and $U_r$. In a later version of this oscillator we have successfully applied this method to bias $U_r$.

### C. Current Sources

The depicted construction of the low-noise current sources (Fig. 5(a)), with the available low-current lateral p-n-p transistors and emitter resistors, would cause problems due to the very low and unpredictable current gain of the p-n-p's when biased at the required current of about 1 mA. Besides tuning inaccuracies, this would also cause a high equivalent output noise current $i_n$. This noise could easily dominate the phase-noise performance. In order not to be troubled by the bad performance of the p-n-p's, external current sources were used in the first version of the oscillator.

## V. Semicustom Realization

The circuit from Fig. 5(a) has been realized on a semicustom chip containing 3-GHz n-p-n transistors, various resistors, and low-current lateral p-n-p's. For reasons explained in the preceding section, it was decided to construct a first test version of the new oscillator without employing the lateral p-n-p's as charging current sources. A photograph of a part of the semicustom chip containing the oscillator circuit is shown in Fig. 6. A successive version of the oscillator, working at half the tuning current, contained the on-chip p-n-p current sources. The measured phase noise of this oscillator was 3 dB higher than in the first version due to the high output noise of the applied on-chip current sources.

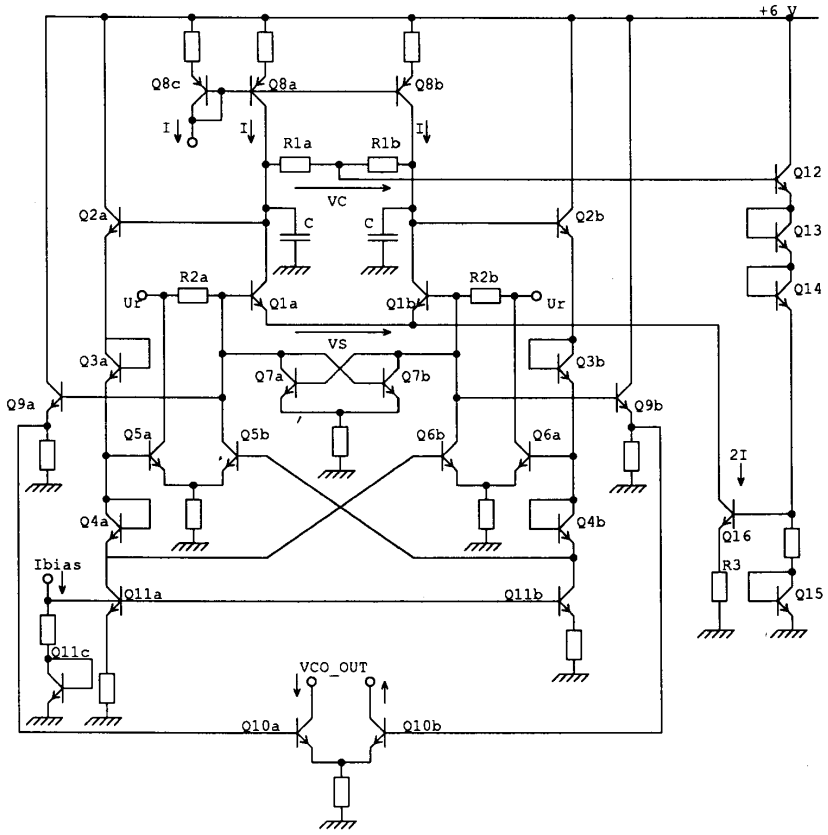
## VI. Experimental Results

### A. Current – Frequency Transfer Function

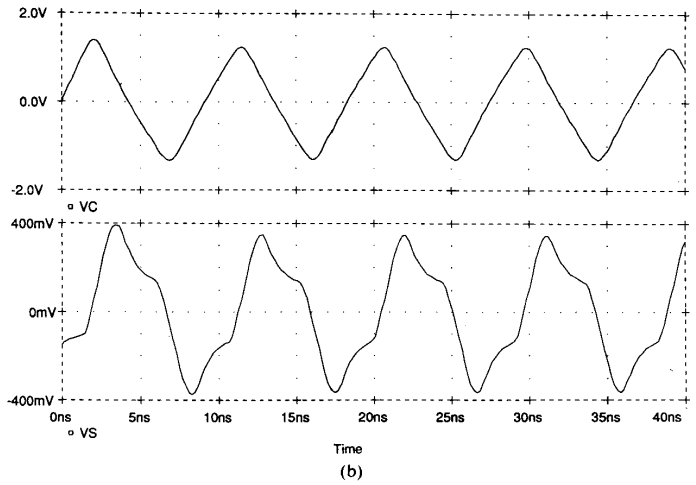
The realized oscillator functions well from very low frequencies up to about 150 MHz. The measured current–frequency transfer function is depicted in Fig. 7. The nonlinearity at high frequencies is a consequence of the switching time delay in the oscillator.

### B. Phase Noise

The phase-noise spectrum, measured using the HP3048A phase-noise measurement system, at an oscillation frequency of 115 MHz is depicted in Fig. 8. The




(a)




(b)

Fig. 5. (a) Schematic of the new balanced relaxation oscillator. (b) Simulated waveforms for the circuit of (a).

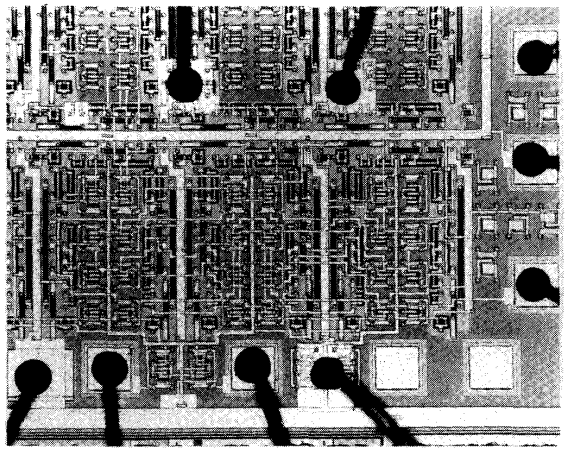


Fig. 6. Photograph of the part of the semicustom chip containing the oscillator circuit.

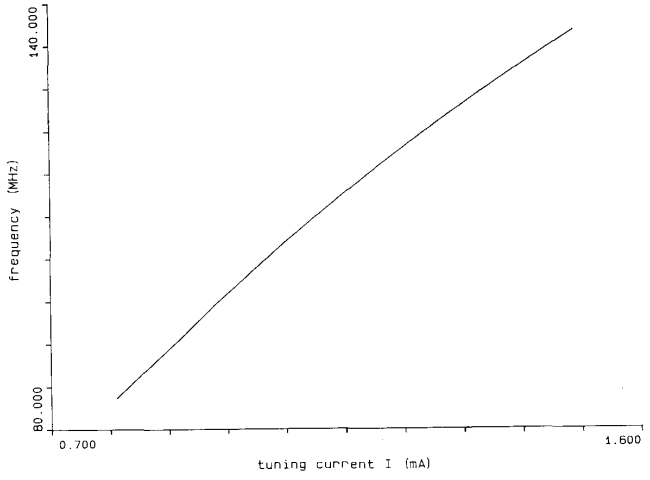



Fig. 7. Measured current–frequency transfer function.

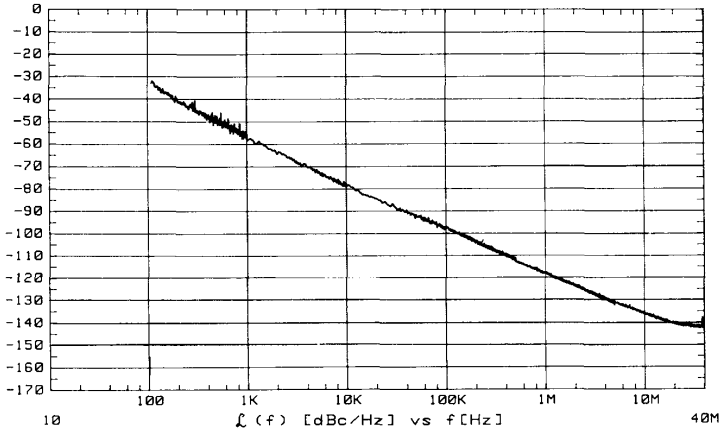



Fig. 8. Measured single-sided phase-noise spectrum ($f_0 = 115$ MHz).

phase-noise spectrum decreases exactly $-20$ dB per decade over a large frequency range, which is in accordance with the term $(f_0/f_m)^2$ in all the derived phase-noise expressions. The noise floor of $-142$ dBc/Hz at 40 MHz is caused by the 50-Ω load resistor of the output buffer.

The absolute value of the phase noise is $-118$ dBc/Hz at 1-MHz distance from the carrier. Because low-noise current sources were used, there is a dominating influence of the sampled high-frequency voltage noise. Analysis of the oscillator circuit reveals that there are effectively seven transistors in series with the switching threshold. The total equivalent noise resistance $R_u$ is 2300 Ω, mainly due to the base noise resistance ($r_b = 300$ Ω) of the transistors. The noise conversion bandwidth $B_{conv}$ is about 400 MHz. Because of the switching time delay the effective value of $U_t$ at $f_0 = 115$ MHz is 1 V, which is somewhat larger than the 0.7 V for low-frequency operation. Using (6) and (7) a value of $-120$ dBc/Hz is calculated if $f_m = 1$ MHz and $f_0 = 115$ MHz. This value differs only 2 dB from the measured phase noise.

### C. Power Consumption and Temperature Behavior

The complete circuit, inclusive of output buffer circuitry (3 mA), consumes about 8 mA at a supply voltage of 6 V. Lower power consumption in the oscillator core with the same tuning linearity and noise performance would be possible if very small on-chip timing capacitors could be used. However, this also requires the availability of low-noise p-type charging current sources.

The temperature coefficient of the oscillator at 100 MHz was measured to be about $-1000$ ppm/°C.

## VII. Conclusion

The analysis and realization of a new balanced fully integratable relaxation oscillator has been described. By means of an on-chip common-mode feedback loop it is possible to use two grounded timing capacitors in a fully differential architecture. The implicit use of parasitics as a part of the timing capacitor and speed-up techniques in the switching part offer an attractive new concept for high-frequency oscillators. The realized circuit functions well over a large frequency range up to 150 MHz. The measured phase noise is close to the theoretical value obtained from a detailed analysis of phase noise in relaxation oscillators. The actual realization in a bipolar process is only one of the possible implementations of the new oscillator architecture. Further work will concentrate on implementations in other technologies (CMOS, BiCMOS) as well.

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