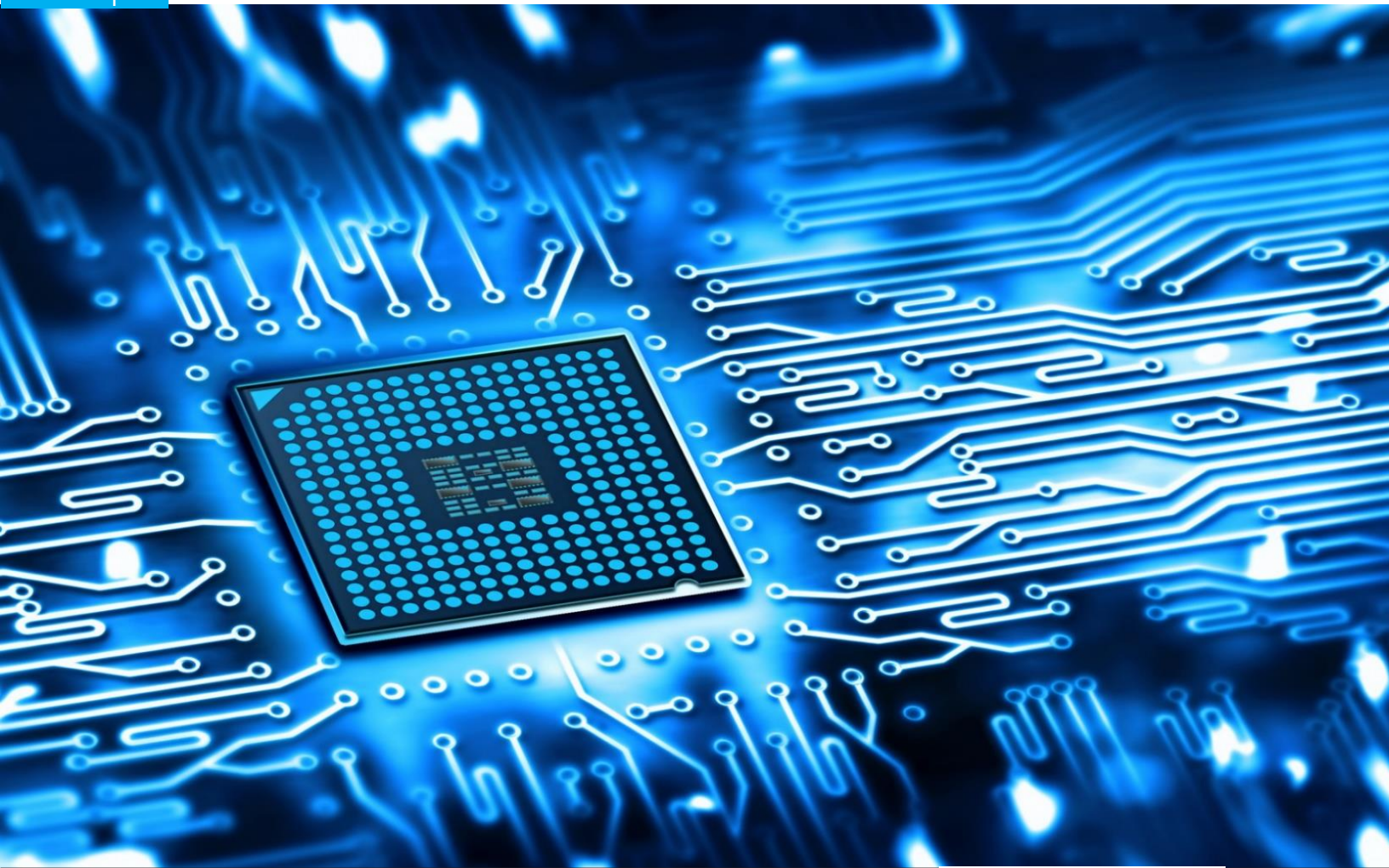


# Void Formation in Cu/Sn Interconnections in Flip Chip Package

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# Abstract

The sporadic occurrence of voids within intermetallic compounds during microelectronic soldering is a key factor affecting the reliability of electronic solder joints. This study aims to understand the void formation mechanisms and investigate different soldering effects. Cu/Sn solder joints in flip chip packages were examined at 190°C after zero to four weeks thermal aging. Experimental approach included ion milling and plasma focused ion beam (PFIB) cross sectional examination, while simulation approach such as finite element modeling (FEM) was used to support the results.

Results showed voids presence at  $\text{Cu}_6\text{Sn}_5$ /solder interface after three weeks aging due to the large local tensile stress induced by volume shrinkage associated with intermetallic compounds formation. These voids have tendency to self-heal after four weeks aging by a compressive stress that originates from the solder ball shrinkage. Compressive stress of 59 MPa was found sufficient to close the 3  $\mu\text{m}$  void.

Moreover, higher level of carbon and organic additives during the electroplating of Cu substrates showed a remarkable effect on the impurities incorporation, which in turn has led to more Kirkendall voids at  $\text{Cu}_3\text{Sn}/\text{Cu}$  interfaces. This suggests that by avoiding C and O impurities on Cu substrates, there will be less voids and thus more reliable joints.

Furthermore, solder joints in Cu/Sn/Cu sandwich structure without underfill were found to release volume shrinkage stress by height reduction and thus resulting in no voids formation. On the contrary, in structures that have underfill filled in between the solder joints, stress will accumulate to a higher level when the volume intends to shrink and stimulates voids to form. The simulated strain in solder joints with the underfill can be as high as 60 % while it can only be 25 % without the underfill. Both experimental results and FEM suggest that voids have higher forming tendency when subjected to the underfill. Last but not the least, cracks will generate due to large mismatch of coefficient of thermal expansion (CTE) when solder joints undergo multiple reflows. Underfill can compensate the large difference and suppress the cracks formation. Consequently, the application of underfill is very crucial for voids formation and solder joints reliability.

# Acknowledgement

I was offered the chance to work on this interesting topic by NXP last summer. It was a strange feeling which combined a little bit of excitement and anxiety on the first day of this journey. Luckily, packaging in semiconductor industry isn't as lame as it sounded like. It actually requires a lot of knowledge and experience to overcome all the obstacles that show up continuously. All of these have given me a lot of chance to learn and grow up. Voids, small holes in a material that couldn't even be seen by bare eyes. I spent almost a year trying to understand why and how they form. This paper is a report for the "life" of these holes. It cannot express the sweat and blood of mine that were taken away in the labs, consulting and disturbing all the brilliant and friendly colleagues, the hope for good results and the tiredness with failures. Despite all the exhausting days, I never regret it. In fact, I love it. I am more than grateful to have such chance to develop myself in a way that I never thought I could.

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*Wei-En  
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# Acronym

Flip chip technology (FCT)

Input/output counts (I/O)

Intermetallic compounds (IMC)

Finite element analysis (FEA)

Finite element model (FEM)

Capillary underfill (CUF)

Molded underfill (MUF)

Ball grid array (BGA)

Printed circuit board (PCB)

Scanning electron microscopy (SEM)

Energy dispersive X-ray spectrometer (EDX)

X-ray photoelectron spectroscopy (XPS)

Plasma focused ion beam (PFIB)

Coefficient of thermal expansion (CTE)

# 1

## Introduction

Packaging Technology has become more challenging and complicated than ever before. Developments in smaller copper (Cu) pillar, finer bump pitch attach process and finer line width and spacing substrate (LW/LS) to satisfy the increasing requirements in the semiconductor industry has become a hot topic. As increasing input/output (I/O) counts in a package are needed in electronic devices, packaging solutions are migrating from traditional wire bond packages to flip chip interconnect to meet these requirements. See Figure 1 for flip chip demonstration. Flip chip technology (FCT) is viewed as an attractive solution for complicated and highly integrated systems. It provides several advantages: a high number of I/O connection, cost effective for manufacturing and the capability to reduce the size of chips. Flip chip interconnect system consists of essentially three basic elements: the chip, the solder bump, and the substrate, see figure 2.

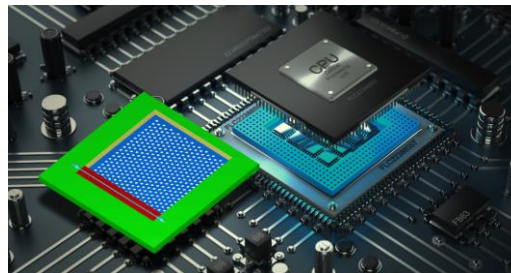


Figure 1 Flip chip demonstration [1]

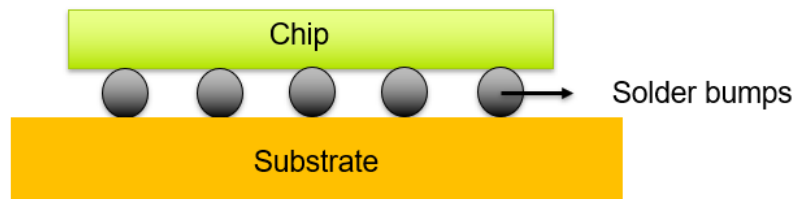
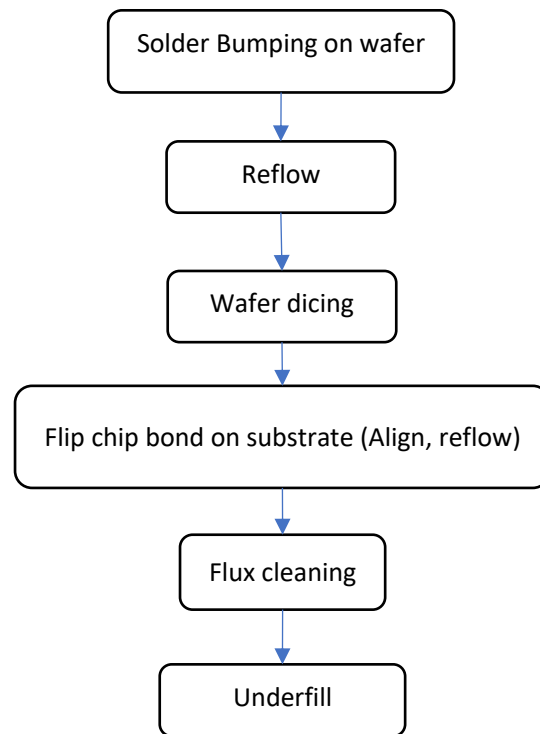


Figure 2 Three essential elements in flip chips: chip, solder bumps, substrate

The bumps are first deposited on a wafer and reflowed. Then they will be diced into small pieces called dies. The dies are flipped over, align to a substrate with flux and reflowed to create a connection. The flux is used to clean the oxidation layer on the substrate. Flux should be cleaned after reflowing. Finally, an underfill is often filled into the gaps between bumps to improve the reliability of the interconnects. Figure

3 shows the process of flip chip manufacturing. The solder bumps in a flip-chip interconnect system provide two main functions. First, the solder joint is the electrical connection between the chip and the substrate. Secondly, the solder joint provides the structural link between the chip and the substrate. These connections are constructed by the reaction of molten solder bumps with conductive metal substrates to form intermetallic compounds (IMC). As the structural integrity of the solder joint affects both the electrical and thermal performance of the flip chip interconnection system, a degradation in the structural integrity can be a reliability concern. This degradation can become more serious when voids start to form in the joints. The interfacial void formation has remained a critical issue that affects the long-term bond reliability. Considerable attention has been paid to this reliability issue in order to find a solution. Some researchers propose voids form because of volume change induced during IMC forming while the others suggested it is attributed to the impurities of electroplating Cu. Nevertheless, previous studies do not account for factors such as stress induced by volume shrinkage, underfill, different reflow time, and additive level in plating.



*Figure 3 Typical process flow for manufacturing solder flip chip interconnect system*

In this thesis report, the aim is to include these factors and understand how they correlate to void formation and investigate it in a broader perspective. The remainder of the report is organized into five chapters. In chapter 2, background knowledge and related literature will be reviewed. Chapter 3 discuss the tested materials and methods that were applied to investigate these materials. Results and discussion will be presented in chapter 4. The conclusions are reported in chapter 5. Finally, chapter 6 shows recommendations for further research.

# 2

## Literature Review

In this chapter the available literature and background knowledge concerning flip chip technology and the void formation, IMC formation in flip-chip packaging will be discussed and reviewed.

### 2.1. Kinetics and thermodynamics of IMC formation

The presence of IMC between solders and metal substrates is desirable because it provides good and solid metallurgical bonding. A continuous, uniform IMC layer is an essential requirement for excellent bonding. Without the metallurgical interaction at the solder/metal substrate interface, IMC will not be formed, and the joint will not be strong enough. This can be disastrous to electronic packaging and raise serious reliability issues. On the other hand, a thick IMC may degrade the reliability of the solder joints as well due to their inherent brittle nature and their tendency to generate structural defects caused by mismatches of the physical properties (such as elastic modulus and coefficient of thermal expansion). The growth mechanism of IMC layer is important in order to avoid weak connections. In addition, void formation is inherently related to the IMC growth. These voids appear in the solder joints while IMC is forming. As a result, knowledge of the solder/metal substrate interactions and phase evolution in the solder interconnections is essential to understand the reliability of solder interconnections and void formation from a metallurgical, kinetic and thermodynamic viewpoint [2].

In Cu–Sn soldering systems, two IMC i.e.,  $\text{Cu}_6\text{Sn}_5$  ( $\eta$  phase) and  $\text{Cu}_3\text{Sn}$  ( $\epsilon$  phase) have been experimentally observed at Cu/Sn interfaces [3]. The typical morphology reported for the IMC layer is a two-phase structure:  $\text{Cu}_3\text{Sn}$  near the Cu substrate and  $\text{Cu}_6\text{Sn}_5$  near the solder. Most of the literature only cover discussion concerning IMC formation either during reflowing or thermal aging. Nevertheless, in this chapter both reflowing process and subsequent thermal aging process will be reviewed. Since reflowing process is a solid/liquid reaction while isothermal aging process is a solid/solid reaction, these two reactions will be discussed separately in the following two sections.



### 2.1.1. IMC formation during reflowing solid/liquid reaction

Figure 4 shows the temperature profile of the reflow process that is used in this thesis. The aim of reflow process is to form acceptable solder joints by first pre-heating the solder and then melting the solder without causing damage by overheating. Take Sn1.8Ag, the solder material used in this thesis as an example. According to the Ag-Sn phase diagram shown in Figure 5a the melting temperature of Sn1.8Ag solder is estimated to be around 225°C [4]. In addition, according to Cu-Sn phase diagram Figure 5b, only two possible IMC,  $\text{Cu}_6\text{Sn}_5$  and  $\text{Cu}_3\text{Sn}$  [5], will be formed during reflowing solder and subsequent isothermal aging provided that the temperature range lies in region A throughout the whole process (thermal aging temperature is 190°C in this report). This is consistent with experimental results done in many researches [6-10]. The two formed IMC,  $\text{Cu}_6\text{Sn}_5$  and  $\text{Cu}_3\text{Sn}$ , tend to have rather high melting temperatures, 415°C and 640°C respectively. As a result, the reflowing process is a solid/liquid reaction between solid IMC and liquid solder from 225°C to 260°C, melting temperature of Sn1.8Ag to the peak temperature of reflowing.

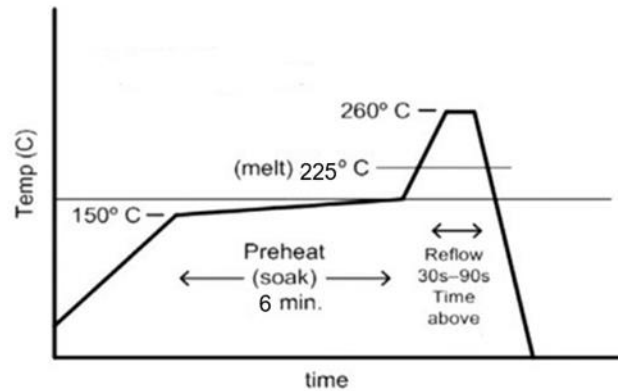


Figure 4 Temperature profile for reflow

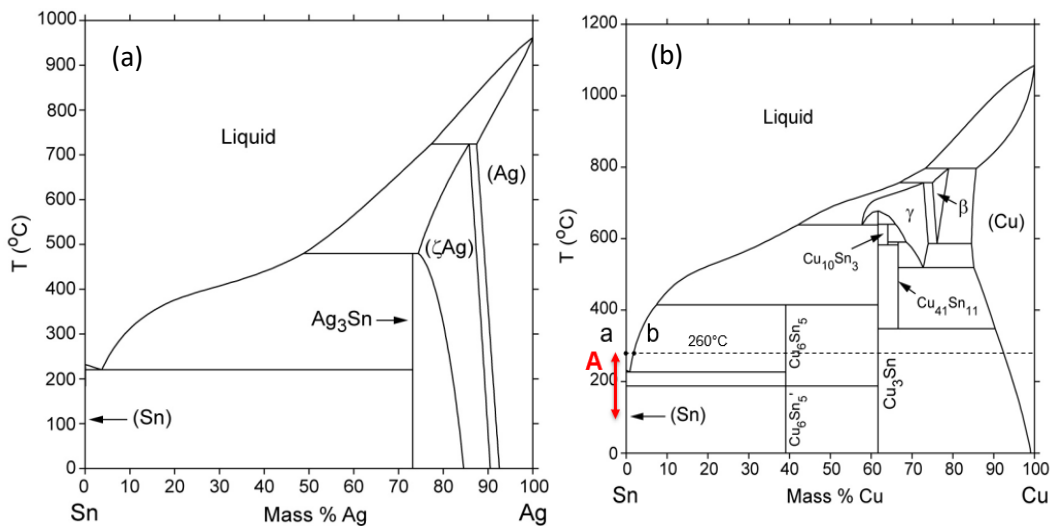


Figure 5 (a) Ag-Sn phase diagram [4]. (b) Cu-Sn phase diagram. Region A is the temperature range during reflowing and aging. Point a to b is solubility of Cu in Sn at 260°C [5].

Experiments have found that the  $\text{Cu}_6\text{Sn}_5$  phase precipitates first at the solder/Cu substrate interface, followed by the precipitation of  $\text{Cu}_3\text{Sn}$  at the  $\text{Cu}_6\text{Sn}_5$ /Cu substrate interface after a certain period of incubation. During the soldering of the Sn1.8Ag solder on the Cu substrate, the Cu starts to dissolve instantaneously in the molten solder after the flux removed the oxides and permitted metallurgical contact between the solder and contacted Cu [11]. The initial rate of dissolution is very high. The dissolution is a nonequilibrium process, and a very high concentration of Cu could be locally found in the Cu/liquid interface. After a short duration of time, molten solder adjacent to the contacted Cu becomes supersaturated with the dissolved Cu and precipitation of  $\text{Cu}_6\text{Sn}_5$  will take place. After  $\text{Cu}_6\text{Sn}_5$  grains nucleate, they tend to grow laterally since the mass transport mechanism leading to the formation of  $\text{Cu}_6\text{Sn}_5$  is most efficient at the substrate–IMC–liquid triple points. As  $\text{Cu}_6\text{Sn}_5$  grains impinge upon one another, a continuous IMC layer forms, completely covering the Cu substrate in a fraction of a second. As the reaction progresses, diffusion of Cu from the substrate leads to the thickening of the  $\text{Cu}_6\text{Sn}_5$  layer by reaction (1).



From a thermodynamics viewpoint, the solid IMC starts to form in the layer of the solder adjacent to the contacted metal at the local equilibrium solubility. The phenomena above can be better interpreted with help of Cu-Sn phase diagram Figure 5b. The liquid solder has solubility of Cu from point a to point b at  $260^\circ$ , the peak temperature of reflowing. When the local region becomes supersaturated with Cu (%Cu goes beyond point b), Liquid  $\rightarrow$  Liquid +  $\text{Cu}_6\text{Sn}_5$  reaction will take place as can be seen in the phase diagram. In sum,  $\text{Cu}_6\text{Sn}_5$  was formed by the dissolution of Cu, followed by a chemical reaction during reflowing. Unlike  $\text{Cu}_6\text{Sn}_5$ ,  $\text{Cu}_3\text{Sn}$  formation is a solid-state diffusion controlled reaction that takes place after an incubation time. After the nucleation of the  $\text{Cu}_6\text{Sn}_5$  phase is complete, the newly formed Cu substrate/ $\text{Cu}_6\text{Sn}_5$  interface becomes metastable with respect to the precipitation of  $\text{Cu}_3\text{Sn}$ . Sn from the Sn1.8Ag solder will slowly diffuse through  $\text{Cu}_6\text{Sn}_5$  and react with the copper substrate to form  $\text{Cu}_3\text{Sn}$ . The reaction is shown below in reaction (2).



In contrast to the  $\text{Cu}_6\text{Sn}_5$  phase, the formation and growth of  $\text{Cu}_3\text{Sn}$  IMC has not been investigated as extensively since it usually requires considerable incubation times and its growth during the early stages of soldering is rather slow, which makes it extremely thin in this early phase. Therefore, it is difficult to detect such thin layer using conventional characterization techniques. As mentioned above,  $\text{Cu}_6\text{Sn}_5$  is the first phase to precipitate at the solder/Cu substrate interface during the earliest stages of the reflowing solder reaction. While thermodynamics alone suggests that nucleation of  $\text{Cu}_3\text{Sn}$  can occur immediately after the formation of the metastable Cu substrate/  $\text{Cu}_6\text{Sn}_5$  interface, an incubation time is usually required for the onset of  $\text{Cu}_3\text{Sn}$  precipitation. In order to understand why this incubation happens, driving force for nucleation needs to be taken into account.  $\text{Cu}_6\text{Sn}_5$  has a larger thermodynamic driving force for precipitation, compared to that of  $\text{Cu}_3\text{Sn}$  under the solder/Cu substrate metastable equilibrium conditions [12]. A local equilibrium is assumed to build up at the interface before the interface compound is formed. In the case of Cu-Sn system, the compositions that are going to form can be predicted by calculating the metastable equilibrium between the Cu-rich FCC phase (Cu substrate) and the liquid phase. Then, the phase with the highest driving force of formation is selected as the compound that would form first during the soldering process. In Figure 6, Gibbs free energy curve of FCC Cu and liquid are drawn. When equilibrium, the metastable phases would have same chemical potential. This can be done by drawing a

common tangent line. The vertical distances between the common tangent and the Gibbs energies of  $\text{Cu}_3\text{Sn}$  and  $\text{Cu}_6\text{Sn}_5$  correspond to the driving forces of formation for the two phases, the Gibbs energies of  $\text{Cu}_6\text{Sn}_5$  and  $\text{Cu}_3\text{Sn}$  are denoted by star sign in Figure 6 [3, 13]. Hence, due to the fact that  $\text{Cu}_6\text{Sn}_5$  has higher driving force for precipitate than  $\text{Cu}_3\text{Sn}$ ;  $\text{Cu}_6\text{Sn}_5$  will form first. It should not be concluded that the phase with the highest driving force of formation always forms first because kinetics and interfacial properties affect the expected value of nucleation rates too. However, since experiments and theoretical analyses [13] suggest that thermodynamics plays the dominant role, it can be a good approximation as has been used to explain the formation of an unstable phase at the beginning of phase transformation.

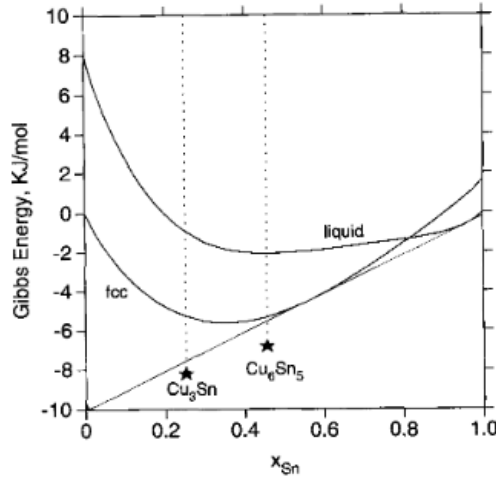


Figure 6 Illustration of driving forces of formation for  $\text{Cu}_6\text{Sn}_5$  and  $\text{Cu}_3\text{Sn}$  under metastable equilibrium between f.c.c. and liquid in Cu-Sn binary system. [13].

One of the characteristics of IMC is the formation of a scallop-type or groove-type morphology as shown in Figure 7a. During early phase of reflowing process,  $\text{Cu}_6\text{Sn}_5$  appears to be a scallop-shape IMC. This groove morphology of  $\text{Cu}_6\text{Sn}_5$  is a result of the force equilibrium between the interfacial tensions of solid (IMC)/liquid (solder) and grain boundary of the IMC as depicted in Figure 7b. The equilibrium reaction is shown in reaction (3),

$$\gamma_{gb} = 2\gamma_{il} \cos \varphi_{il} \quad (3)$$

where  $\gamma_{gb}$  is the grain boundary energy,  $\gamma_{il}$  is the interfacial energy between IMC and liquid solder,  $\varphi_{il}$  is the equilibrium semi-dihedral angle at the IMC/liquid solder interface. Another group proposed that “freezing” of the boundaries from the groove parallel to the growth direction, in this case  $\text{Cu}_6\text{Sn}_5/\text{Cu}_6\text{Sn}_5$  boundaries, would increase the total surface area and would require additional work into the system. Thus, the grooves serve to constrain the boundaries from moving during intermetallic formation, and the  $\text{Cu}_6\text{Sn}_5$  grain will grow faster at the  $\text{Cu}_6\text{Sn}_5$  /solder interface, yielding the scalloped morphology [14].

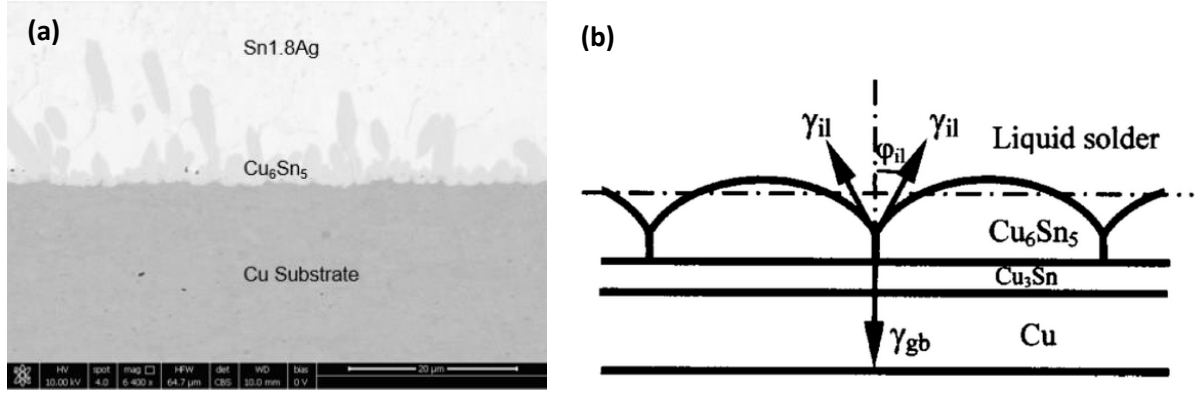


Figure 7 (a) Scallop-type  $\text{Cu}_6\text{Sn}_5$  (b) The schematic of equilibrium condition at liquid solder/  $\text{Cu}_6\text{Sn}_5$  grain boundaries [14].

### 2.1.2. IMC formation during thermal aging solid/solid reaction

Thermal aging process is usually performed after reflowing to investigate the IMC growth and related issues. Since the aging temperature used in this thesis report is  $190^\circ\text{C}$ , much lower than melting temperature of solder materials (in this case  $225^\circ\text{C}$  for Sn1.8Ag) and IMC ( $415^\circ\text{C}$  for  $\text{Cu}_6\text{Sn}_5$  and  $640^\circ\text{C}$  for  $\text{Cu}_3\text{Sn}$  from the phase diagram), the reaction between IMC and the solder is a solid to solid reaction. During thermal aging,  $\text{Cu}_3\text{Sn}$  and  $\text{Cu}_6\text{Sn}_5$  both grow by solid state diffusion mechanism. The phase formation and evolution in the interfacial region involve the diffusion of Sn and Cu atoms. The growth of the  $\text{Cu}_6\text{Sn}_5$  IMC is mainly attributed to the reaction between Cu atoms from the Cu substrate and Sn atoms from the solder, as expressed in reaction (4). This reaction grows  $\text{Cu}_6\text{Sn}_5$  pushing the interphase boundary toward the solder direction.



With a prolonged aging time,  $\text{Cu}_3\text{Sn}$  will have an obvious growth at both Cu substrate/ $\text{Cu}_3\text{Sn}$  interface and  $\text{Cu}_3\text{Sn}/\text{Cu}_6\text{Sn}_5$  interface. For the Cu substrate/ $\text{Cu}_3\text{Sn}$  interface, Sn from the solder will slowly diffuse through IMC and react with Cu to form  $\text{Cu}_3\text{Sn}$ . The reaction is identical to  $\text{Cu}_3\text{Sn}$  formation during reflowing, as they both are driven by solid state diffusion interaction between Sn and Cu. See reaction 2. Despite  $\text{Cu}_3\text{Sn}$  growing at this interface appears to be straightforward, growing can be very complicated at the  $\text{Cu}_3\text{Sn}/\text{Cu}_6\text{Sn}_5$  interface. The  $\text{Cu}_6\text{Sn}_5$  phase is thermodynamically unstable with Cu [15]. Upon the formation of the  $\text{Cu}_3\text{Sn}$  phase, the  $\text{Cu}_3\text{Sn}$  phase will form by consuming the  $\text{Cu}_6\text{Sn}_5$  phase. This growth consists of two steps. Firstly, the diffusion of Cu from the Cu substrate and  $\text{Cu}_3\text{Sn}$  through the existing  $\text{Cu}_3\text{Sn}$  layer, followed by the conversion of  $\text{Cu}_6\text{Sn}_5$  into  $\text{Cu}_3\text{Sn}$  at the  $\text{Cu}_3\text{Sn}/\text{Cu}_6\text{Sn}_5$  interface as described in equation 5 below.



To sum up, the whole reaction can be seen as  $\text{Cu}_3\text{Sn}$  grows rapidly with temperature at the expense of  $\text{Cu}_6\text{Sn}_5$  at  $\text{Cu}_6\text{Sn}_5/\text{Cu}_3\text{Sn}$  interface. Because of the reaction in reaction 2, the amount of Cu atoms that diffuses from the Cu substrate to the  $\text{Cu}_6\text{Sn}_5$ /solder interface is remarkably reduced when the thickness of the  $\text{Cu}_3\text{Sn}$  layer increases with increasing ageing time. Therefore, in the absence of excess Sn from the solder,  $\text{Cu}_6\text{Sn}_5$  formation toward the solder direction is limited (reaction in reaction 4 is retarded by limited Sn.) In the meantime, the  $\text{Cu}_3\text{Sn}$  phase keeps growing at the expense of the  $\text{Cu}_6\text{Sn}_5$  phase until the latter

phase is fully consumed, making the growth of  $\text{Cu}_3\text{Sn}$  layer more significant than that of the  $\text{Cu}_6\text{Sn}_5$  layer under this circumstance [16]. On the other hand, under normal soldering conditions, there is sufficient Sn for reaction 4 to continue. In this case, the thickness of the  $\text{Cu}_3\text{Sn}$  layer is much thinner than  $\text{Cu}_6\text{Sn}_5$  [17]. Moreover, the initial scalloped  $\text{Cu}_6\text{Sn}_5$  IMC formed during reflowing will become planar after a short time period during thermal aging. The planarization process is attributed to the shorter diffusion distance between the scallop valleys and the Cu substrate, compared with the distance between scallop peaks and the Cu substrate. Thus, Cu will diffuse faster to the scallop valley than to the scallop peak, leading to a faster growth rate at the valley and subsequent planarization of the layer.

Researches have shown that at the early stage of  $\text{Cu}_6\text{Sn}_5$  formation, the growth is controlled by massive grain boundary diffusion [18, 19]. However, after a certain amount of time, the controlling growth mechanism will transit to volume diffusion controlled. It should be noted that the transition can be regarded as a range rather than a distinct transition point because the dominant growth mechanism of the intermetallic changed gradually but not suddenly. This transition from grain boundary diffusion to volume diffusion is attributed to the coarsening effect of  $\text{Cu}_6\text{Sn}_5$  grain. The coarsening process is governed by Gibbs-Thomson effect which causes the flux of Cu atoms going from the small grain to the large grains and thus the diminishing of the small grains. There are two types of atoms diffusion fluxes, interfacial reaction flux and ripening flux. In the interfacial reactions between Sn-rich solder and Cu substrate, the growth of  $\text{Cu}_6\text{Sn}_5$  grains is controlled by both fluxes, as shown in Figure 8, where  $J^I$  is interfacial reaction flux and  $J^R$  is ripening flux. The interfacial reaction flux is due to the chemical reaction of Cu and Sn atoms diffused to each other, and it is responsible for the total thickness of  $\text{Cu}_6\text{Sn}_5$  IMC formed at the interface. On the other hand, the ripening flux is due to the Gibbs-Thomson effect accompanied by volume diffusion between  $\text{Cu}_6\text{Sn}_5$  grains with different grain size, and it is naturally related to the grain size of the  $\text{Cu}_6\text{Sn}_5$  IMC. The expression of Gibbs-Thomson effect is shown below [20].

$$J_R = \frac{2\gamma\Omega DC_0}{3\delta RT} \cdot \frac{1}{r} \quad (6)$$

where  $\gamma$  is the interfacial energy per unit area between  $\text{Cu}_6\text{Sn}_5$  and molten solder,  $\Omega$  is the molar volume of  $\text{Cu}_6\text{Sn}_5$ ,  $D$  is the diffusion coefficient of Cu in the liquid Sn,  $C_0$  is the equilibrium concentration of Cu in Sn,  $\delta$  is the average grain separation distance,  $R$  is a gas constant,  $T$  is the absolute temperature, and  $r$  is the average radius of the  $\text{Cu}_6\text{Sn}_5$  grains. By the ripening flux of Cu atoms between  $\text{Cu}_6\text{Sn}_5$  grains, the large grains continue growing, while the small grains shrink or disappear. Hence, the  $\text{Cu}_6\text{Sn}_5$  grains will gradually grow larger and end up with fewer grain boundaries causing the growth mechanism transit from a grain boundary diffusion-controlled mechanism to a volume diffusion-controlled mechanism. Unlike  $\text{Cu}_6\text{Sn}_5$  that experiences a transition of diffusion mechanism, researches have shown  $\text{Cu}_3\text{Sn}$  phase is more likely to be grain boundary diffusion-controlled during the entire thermal aging process.  $\text{Cu}_3\text{Sn}$  phase naturally exhibits a relatively fine grain size with columnar structure. Furthermore, the same ripening effect is not apparent in  $\text{Cu}_3\text{Sn}$  growth. Thus, the fine grain size coupled with lack of obvious ripening effect likely contributed to grain-boundary diffusion as a predominant mechanism.

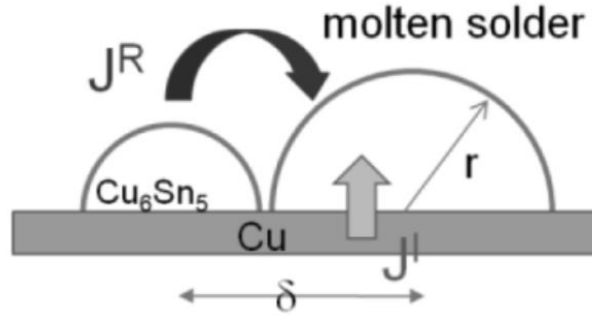


Figure 8 Two fluxes account for  $\text{Cu}_6\text{Sn}_5$  growing.  $J^I$  is interfacial reaction flux and  $J^R$  is ripening flux [20].

The kinetics concerning the IMC growth at a Cu-Sn system can be adequately modeled with the empirical power law as follows

$$h = h_0 + kt^n \quad (7)$$

where  $h$  is the total thickness of interfacial IMC,  $h_0$  is the initial thickness of IMC,  $k$  is the coefficient of IMC growth rate which is strongly related to the diffusivity of atoms in IMC,  $t$  is the reaction time and  $n$  is the time exponent. The  $n$  value is strongly dependent on which mechanism is dominating. When  $n = 1/3$ , the interfacial IMC growth is grain boundary diffusion-controlled; when  $n = 1/2$ , the interfacial IMC growth is volume diffusion-controlled [19]. As mentioned above, grain boundary diffusion is the dominant transport path  $\text{Cu}_6\text{Sn}_5$  in the early stages of the interfacial reaction. This leads to a  $n=1/3$ , thus  $h_1 = kt^{1/3}$  growth law. In the later stages when the  $\text{Cu}_6\text{Sn}_5$  grains become large enough the grain boundary transport is negligible, diffusion of the atoms through the solid IMC to the interfaces where reactions take place dominates thickening kinetics of  $\text{Cu}_6\text{Sn}_5$  leading to a total thickness of  $h_{\text{total}} = h_1 + kt^{1/2}$ . In contrary, there is no coarsening effect for  $\text{Cu}_3\text{Sn}$  phase, the fine grain sizes remain, leading to a  $h = kt^{1/3}$  growth law [18].

## 2.2. Possible root causes of void formation

The voiding effect has been the subject of many studies and speculation, however the root cause remains unidentified. The complexity lies in that voids can appear in several places in a solder joint and they seem to have different mechanisms. Some voids exist at Cu substrate/ $\text{Cu}_3\text{Sn}$  interfaces, while some appear at  $\text{Cu}_6\text{Sn}_5$ /solder interfaces. The hypotheses proposed to explain these void formations are very diverse. However, there are three main theories that have caught the most attention: Kirkendall effect, voids induced by plating impurities and IMC volume shrinkage-accounted voids. In this section, these theories will be reviewed.

### 2.2.1. Kirkendall effect-induced voids

Frequently, microscopic voids within  $\text{Cu}_3\text{Sn}$  have been observed to develop during extended thermal aging. This phenomenon is commonly referred to as Kirkendall voiding or diffusion porosity [21]. It is commonly believed that these small voids arise from the agglomeration of excess vacancies, as a result of the intrinsic diffusivity difference between the two diffusion species, Cu and Sn [22]. In reactive interdiffusion system, reaction product formation at the interfaces is accompanied by a divergence of vacancy fluxes, reports have shown Cu is the faster diffusive specie in  $\text{Cu}_3\text{Sn}$  [23]. This leads to a larger Cu diffusion flux than Sn diffusion flux and thus producing vacancies. When the vacancies start to aggregate, coalescence begins and voids will form. The vacancy flux ( $J_v$ ) by the Sn/Cu reaction couple can be expressed as follows [24].

$$J_v = J_{\text{Cu}} - J_{\text{Sn}} \quad (8)$$

where  $J_{\text{Cu}}$  refers to the Cu atoms diffuse out of the Cu/IMC toward the Sn matrix and  $J_{\text{Sn}}$  refers to the Sn atoms that migrate from the Sn matrix to the IMC/Cu interface. Again, it is well known that the formation of Kirkendall voids was partly attributed to the unbalanced diffusion of component elements, that is, Cu and Sn. However, an intriguing observation is that Kirkendall voids do not always occur in every Cu-Sn system. If this effect of an asymmetry between the fluxes of two interdiffusing species, i.e. voids grow because more material is moving out of a local region than is coming in is true, it should appear in every case. A high voiding level in  $\text{Cu}_3\text{Sn}$  has so far only been observed on electroplated Cu substrates. On high purity Cu substrates, negligible voiding was shown in solder joints under the same aging conditions. Accordingly, it suggests that diffusion flux imbalance is not enough to lead to high level voiding and some other reasons might play a role in it as well.

### 2.2.2. Co-deposition of impurities during Cu electroplating

As section 2-2-1 pointed out, Kirkendall effect cannot explain the voids entirely; hence there should be other mechanism elevating voids to form. The co-deposition of impurities during Cu electroplating has raised much attention. The incorporation of impurities in the Cu deposit originating from the Cu plating formula significantly affects the evolution of the interfacial microstructure of Sn/Cu joints. On one hand, the impurities will segregate at the interface, thus can reduce the activation energy barrier of the void nucleation, and accelerate the formation of voids [25]. On the other hand, vacancy super-saturation, necessary for void formation, may result from vacancy sinks being blocked by impurity molecules. Such sinks could be dislocations, interfaces and grain boundaries [22]. Although impurities introduced during electroplated Cu have been suspected to be responsible for the voiding phenomenon, it has previously not been clear what properties of electroplated Cu are responsible for the voiding in  $\text{Cu}_3\text{Sn}$ . Some group speculated co-deposited H might agglomerate into voids during thermal aging, it was suggested that H segregating atoms would pin the interfacial, misfit, dislocations whose climb otherwise severed to absorb (sink) Cu vacancies [26] while some conjectured that the voiding phenomenon was caused by organic and inorganic impurities incorporated in electroplated Cu films [27]. Other group attributed the voiding to residual sulfur from an organic plating additive. Segregation of S to the Cu/ $\text{Cu}_3\text{Sn}$  interface lowered interface energy and thereby the free energy barrier for Kirkendall void nucleation[28]. Several other researches like above-mentioned have done to understand which element is responsible for the voiding. Some have found that even elements in solder material i.e. Bi in SnBi solder can serve as segregating

atoms to block vacancy sink [29]. Nevertheless, there is still no consensus on which element and what mechanism is controlling the behavior by far. In this study, the influence of impurities level on void formation will be discussed first. For the second step, elements that haven't been included in previous research will be added into discussion.

### 2.2.3. IMC volume shrinkage-introduced voids

Not only Kirkendall effects combined with impurities during plating can cause voids that mainly locate at Cu/Cu<sub>3</sub>Sn interface. Bigger voids locate at Cu<sub>6</sub>Sn<sub>5</sub>/solder occur to form during thermal aging as well. Volume shrinkage is a highly suspected reason in this case. In the reaction of Cu and Sn system, Cu<sub>6</sub>Sn<sub>5</sub> and Cu<sub>3</sub>Sn are the only two IMC that will form during reflowing and thermal aging at 190°C. When forming Cu<sub>6</sub>Sn<sub>5</sub> and Cu<sub>3</sub>Sn, because of the nature of IMC structure, the formation of IMC will cause a significant volume shrinkage which can be estimated by the structural data [30, 31]. A 4.1% contraction of volume will happen when Cu reacts with Sn forming Cu<sub>6</sub>Sn<sub>5</sub>, and a contraction of 8.1% in volume when forming Cu<sub>3</sub>Sn. These calculated numbers will be used in the finite element analysis (FEA) model in chapter 3. The change of volume may result in the generation of inner stress in the solder joints. Although yield strains of materials, including IMC and solder can suppress the volume shrinkage, it is still difficult to compensate this volume loss entirely. Consequently, the solder joints will be in a highly stressed state and prone to form voids. However, more details and research with regards to IMC volume shrinkage-induced voids are lacking. Very limited research has been done on the volume shrinkage that comes accompanied with IMC formation. In addition, no research was found describing this type of bigger voids in Cu<sub>6</sub>Sn<sub>5</sub> and solder interface. As a result, studies and research on volume shrinkage-induced voids can be valuable and provide a new perspective to void formation.

## 2.3. Underfill

One key factor which has drastically increased the reliability of flip chip structures against temperature variations is the use of underfill between the chip and the substrate which, when properly selected and applied, may increase the reliability by more than one decade. The underfill materials, usually thermoset epoxies, are stiff enough to take part of the forces developed by different thermal expansion coefficients of the chip and substrate. An underfill material also protects the face of the chip against moisture and impurities and makes the structure mechanically stronger [32]. There are several requirements for underfill materials such as: good adhesion to the solder and chip; compatible coefficient of thermal expansion (CTE) value with chip, solder and substrate; high transition temperature  $T_g$ , good flow property, low moisture absorption rate, and negligible interaction with flux residues etc. Since this report will include the underfill influence on void formation, knowing how to apply underfill is crucial. Currently, there are two main application methods for underfill. One is capillary underfill (CUF), shown in Figure 9a and the other is molded underfill (MUF) shown in Figure 9b [33]. CUF is applied by injecting the epoxy at a targeted corner point, which allows the injected epoxy from the tip of the dispensing needle to flow down along the sidewall of the chip to the edge of the lower surface of the chip and subsequently fill into the gap through capillary action. After completely filling into the gaps, heating up the thermoset epoxy



for curing is necessary. The last optional step is to cover the whole package and underfill with a molding compound to provide further protection. See Figure 10 for the procedure [34, 35]. Unlike CUF, MUF is a one step process combining molding compound and underfill together. MUF assembly concept uses a single step approach to both underfill and over mold the die during the same mold shot thus making the process a lot simpler and faster than that with CUF. These two techniques have different advantages and disadvantages, it is important to choose a better underfilling procedure based on the purpose and the requirements of the chips. Based on the facts that underfill can largely change the stress field around solder joints and mechanically support them. Underfill seems to be a crucial factor that would be influential to void formation.

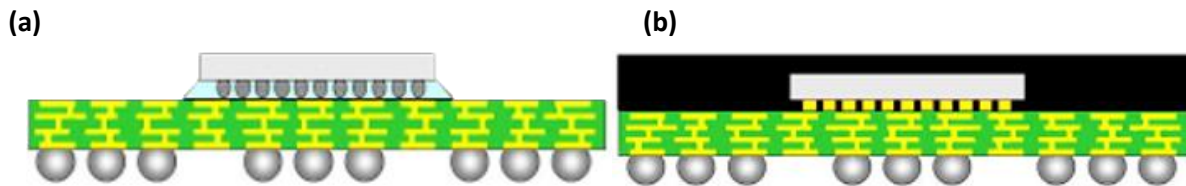


Figure 9 (a) Illustration of CUF (b) MUF [33]

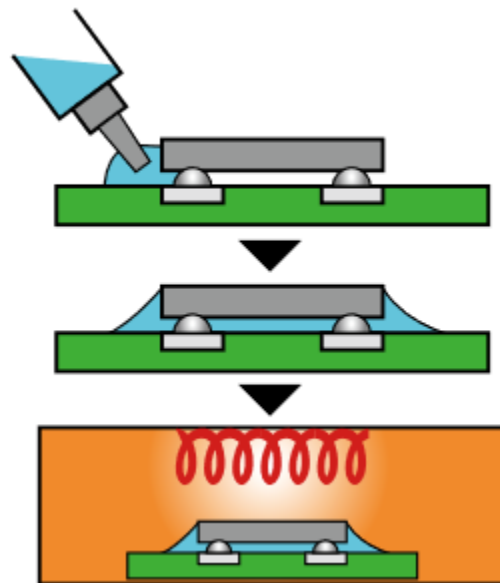


Figure 10 CUF procedure. Dispense underfill material at the edge of the chips. Underfill fill in by capillary action. Finally, curing the underfill [35].

## 2.4. Reflow

During the reflow process the solder is heated to a temperature above the melting point of the solder. When the solder melts, it forms a metallurgical IMC bond with the Cu bond pad. The reflow temperature profile can influence the kinetics of the reaction of the solder composition with the Cu pad, especially at the final phase of reflowing, different cooling rate can end up with different IMC bonding. Different cooling rate influences the bonding by forming IMC with different initial thickness and morphology. These initial intermetallic characteristics had a profound impact on the growth kinetics of the intermetallic layer and, primarily, the  $\text{Cu}_6\text{Sn}_5$  phase. Faster cooling rate such as water quenching and air cooling produced a relatively thin and planar  $\text{Cu}_6\text{Sn}_5$  layer, while slower cooling such as furnace cooling produced a scalloped  $\text{Cu}_6\text{Sn}_5$  layer. Besides the initial morphology and thickness, another significant difference between faster cooling rate and slower cooling rate is the growth rate of  $\text{Cu}_6\text{Sn}_5$ . As mentioned,  $\text{Cu}_6\text{Sn}_5$  appears to be a scalloped-type for slow cooling while faster cooling resulting in planar  $\text{Cu}_6\text{Sn}_5$ . This grooving shape caused by slow cooling can contribute more surface area for bulk diffusion than planar shape caused by faster cooling [36]. Hence, the growth rate of  $\text{Cu}_6\text{Sn}_5$  occurs to be higher if the reflowing profile has a slowing cooling rate. Note that this effect only exists before the planarization. Once the planarization process begins,  $\text{Cu}_6\text{Sn}_5$  no longer has a scallop shape and this effect will be eliminated. In a reflow oven, typically a peak temperature between 10 and 50 °C above the melting point is used. At low temperatures the rate of melting of the solder can be slow, resulting in poor IMC formation and solder ball height nonuniformity. At very high temperature, the solder might react extensively with the Cu bond pad, resulting in IMC dewetting [37]. So far, the study regarding to reflowing impact on void formation has been very limited. However, since the reflowing cooling rate can influence the initial IMC wildly, and chips typically undergo more than one time reflow during manufacturing. It is reasonable to include the effect of reflow time into the study.

## 2.5. Flux

Flux coating is one of the key processes during flip-chip packaging. Flux is applied on the solder bumps or substrate to remove oxides by chemically dissolving metal oxides that inhibit the flow of solder and pre-bonding flip chip on the substrate before reflow [32]. Flux can also facilitate solder wetting during reflow. Flux commonly contain three constituents: a solvent such as alcohol, a vehicle which is a solvent with a high boiling point and an activator which contain acids. The solvent facilitates uniform spreading of the flux on the metal bond pads and will vaporize during the pre-heat process of reflow. This promotes a uniform coating of the flux on the solder and metal bond pad. The flux also becomes more viscous and tackier. Further increase in temperature causes the vehicle to flow along with the activator. The activator reduces the oxides, while both the vehicle and the activator volatilize. Flux residues commonly contain residues from the reaction by-products. However, flux residues sometimes present after reflow process and can seriously affect the performance of surface mount and reliability. One of the detrimental influences is its corrosive behavior of acidic activators on solder materials. Another downside of residue flux is it can sometimes cause a premature failure of the solder connections between solder and metal pad substrate, as shown in Figure 11. Last but not the least, the flux normally will vaporize during reflowing. This vaporized residue flux can sometimes be trapped in the solder and cause a disconnection while IMC grow, see Figure 12. Hence, cleaning the flux after reflowing is necessarily important. The cleaning can be

done by using organic or inorganic solvent liquid aided by ultrasonic vibration. Unfortunately, the shrinking size of all electronic components and bonding pad has made cleaning of flux increasingly difficult. The small gaps between assembled parts, and solidification cavities in solder joints are very resistive to penetration by cleaning liquids. Nevertheless, the cleaning procedure can still clean out the flux to some extent and thus is a mandatory step.

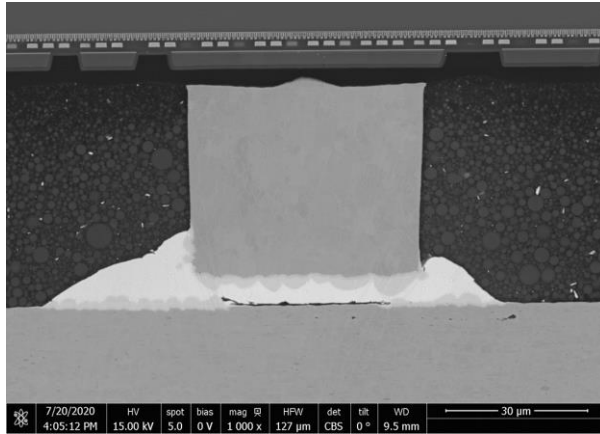


Figure 11 Premature failure of the solder connections between solder and metal pad substrate

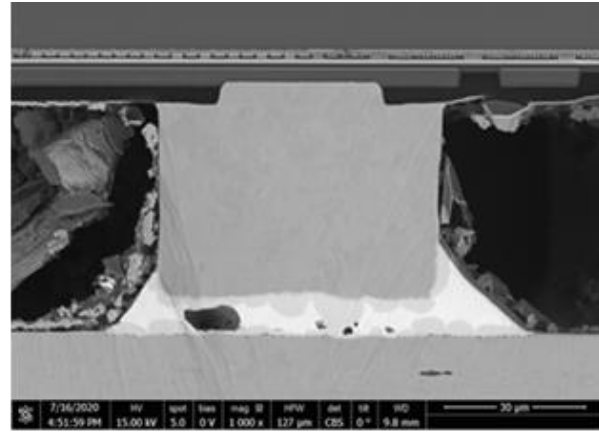


Figure 12 Trapped residue flux

## 2.6. Conclusions

The IMC formation has been reviewed from both thermodynamic and kinetic perspectives. Three main hypotheses for the root-causes of void formation were found:

- (i) the imbalance of diffusion rates between Cu and Sn during the formation of Cu–Sn IMC.
- (ii) the co-deposition of impurities during Cu electroplating to void formation.
- (iii) volume shrinkage during IMC phase transformation.

Although these hypotheses have been widely researched, most researchers studied only one of the theories above. Considerations and crosslinks with other important factors during packaging process such as stress induced by volume shrinkage, underfill involvement, cycles of reflow time, impurities level and other possible element that cause Kirkendall voids are still missing. Hence, has the following research objectives are set for this thesis:

1. Understand the formation mechanism of voids in zero to four weeks of thermal aging and obtain the critical stress for either voids formation or self-healing.
2. Develop finite element model demonstrating the strain at interfaces with and without underfill.
3. Develop a comprehensive model on void formation in Cu/Sn/Cu sandwich structure to understand the relation between the void formation, volume shrinkage and underfill involvement.

4. Acquire knowledge on how to create void-free solder joints by controlling the impurities of Cu substrates.

5. Include effect of multiple reflow times to the tested samples and determine how to overcome the cracks induced by multiple reflow times.

# 3

## Materials and methods

In this chapter, materials and methods used will be discussed in detail. Materials section will be split up into two subsections: a packaged chip (an actual chip) and the bare die model system (only the bare die from the actual chip). In the methods section, methods for the whole integrated chip such as cross section preparation and finite element simulation will be introduced in the first two subsections. The procedure of how to build up the bare die model system will be discussed afterwards. In the last part, the cross-section preparation and surface analysis on this model system will be discussed.

### 3.1 Materials

This section will be split into two subsections. The first subsection introduces an integrated test chip containing Cu-Sn system that will be studied. The second subsection introduces a Cu/Sn/Cu sandwich structure that was constructed by placing the die of the integrated test chip on electroplating Cu substrates.

#### 3.1.1. Packaged test chip

The material that is studied in this thesis report is a packaged test chip as shown in Figure 13. To have a better understanding of the test chip, Figure 14a shows the schematic illustration of the elements in typical flip-chip technology. Here, the chip is attached to the ball grid array (BGA) substrate which is normally a metal pad through an array of solder joint (flip-chip joints) with a diameter around tens of micrometers. The BGA substrate is then connected to the printed circuit board (PCB) through another array of solder joints (BGA). This later BGA is a package, in operation, conduct electrical signals between the integrated circuit and the PCB on which it is placed. This array of solder joints are ten times larger in diameter than the BGA between chip and metal pad.

In comparison, the silver dots on the back side of the test chip in Figure 13 correspond to the bigger BGA that is attached to PCB in Figure 14a. However, the focus solder joint in this thesis report is the smaller BGA attached to the chip and Cu metal pad substrate. Figure 14b shows a brief optical microscope cross section image of the test chip. The zoom-in area is the target area where the solder joints are. In the magnifying image, the top layer is the chip substrate. Beneath the chip substrate are Cu pillars (pink color, square shape). Each Cu pillar has a dimension of  $60\text{ }\mu\text{m} \times 40\text{ }\mu\text{m}$ . The Cu pillar is surrounded by Sn1.8Ag

solder (silver) which has a 30  $\mu\text{m}$  height. Normally, Cu pillars are wrapped and covered by solder balls before cross sectioning. That is why we can only see the silver solder balls until cross sections are made. Underneath the Cu pillars and Sn1.8Ag solder there is a Cu pad substrate. From one Cu pillar to another Cu pillar, there is underfill (black) filling up the gaps.

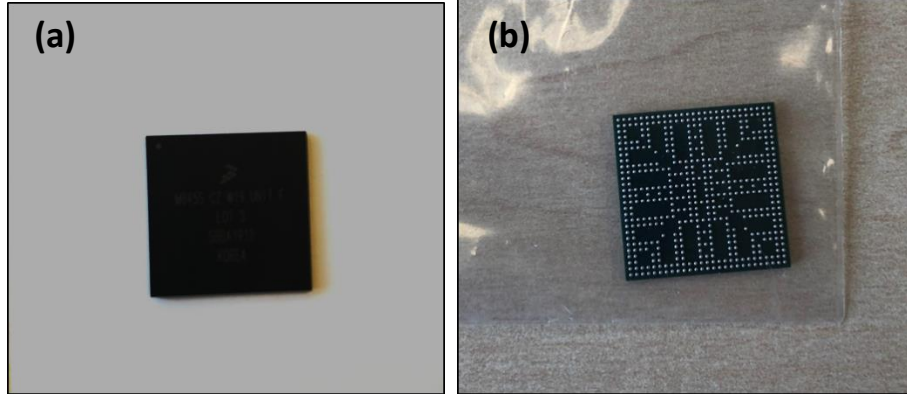


Figure 13 Test Chip (a) Back side (b) BGA side

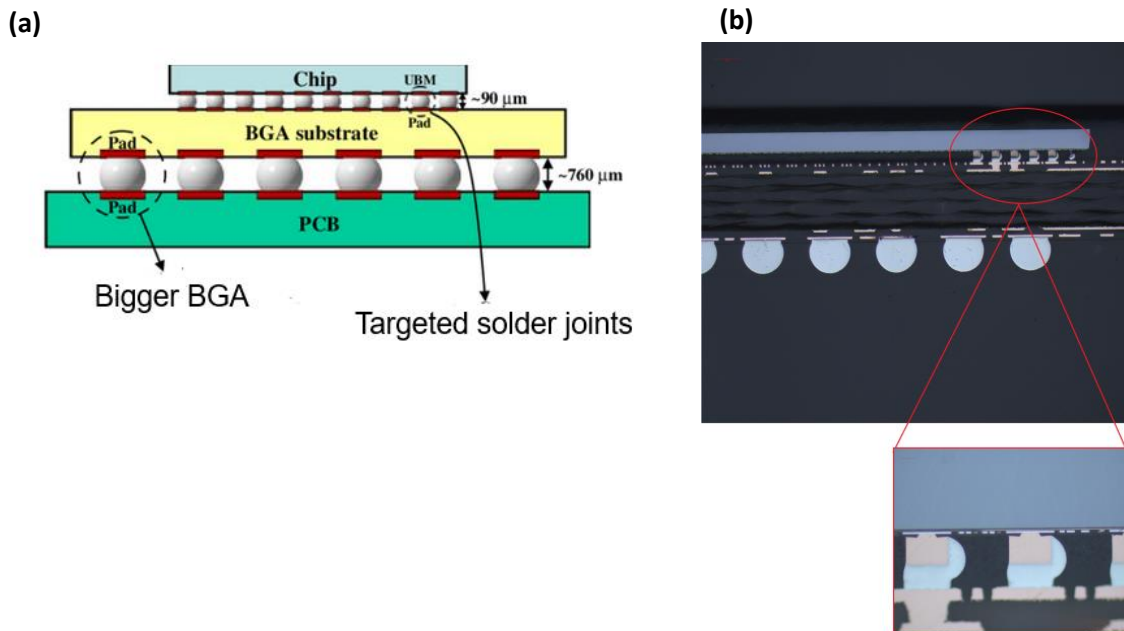


Figure 14 (a) Schematic illustration of a typical flip chip device (b) Optical Microscope image of test chip. The zoom-in area is the focus solder joints

The core chip (bare die) is located in the center position of the test chip, pointed out by the red square in Figure 15. As mentioned and illustrated in Figure 14a, Cu pillars are attached to this chip; therefore, this square region is where we can find Cu pillars. The zoom-in image shows the X-ray image of the center position where the chip is located. The black dots are the bigger BGA and the grey smaller dots are the Cu pillars and solder joints where we will be focusing on. Knowing the position of the Cu pillars is extremely important for the purpose of performing experiment such as polishing, ion milling and focused ion beam

cross sectioning on the precise position. Hence, the X-Ray image is helpful and can facilitate experimental work tremendously.

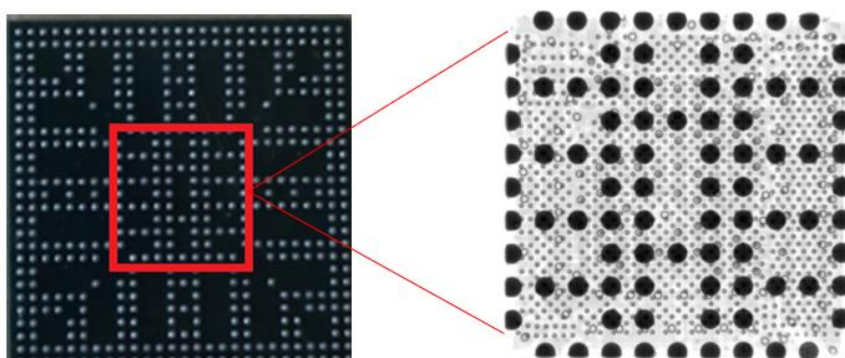


Figure 15 Picture of test chip. Red rectangle area represents the bare die location, the magnifying picture is the X-ray image of the bare die.

### 3.1.2. Bare Die Model System: Cu/Sn/Cu sandwich structure

In this thesis report, not only the full package of a test chip was studied, a “bare die only” model system was also designed and set up to include different factors to this study. See Figure 16 for the bare die of the test chip. The bare die only consists of a chip substrate and Sn1.8Ag solder bumps. It does not have underfill in between solder joints nor Cu substrates attached to them, as shown in Figure 17. Thus, several factors such as underfill involvement, different impurities level on Cu substrate, and different reflow times can be taken into consideration because we can manually include or exclude underfill, attach the dies to different electroplating Cu substrates and reflow them for multiple cycles. In sum, by using the bare dies, this study won’t be restricted to the original design of the test chip.

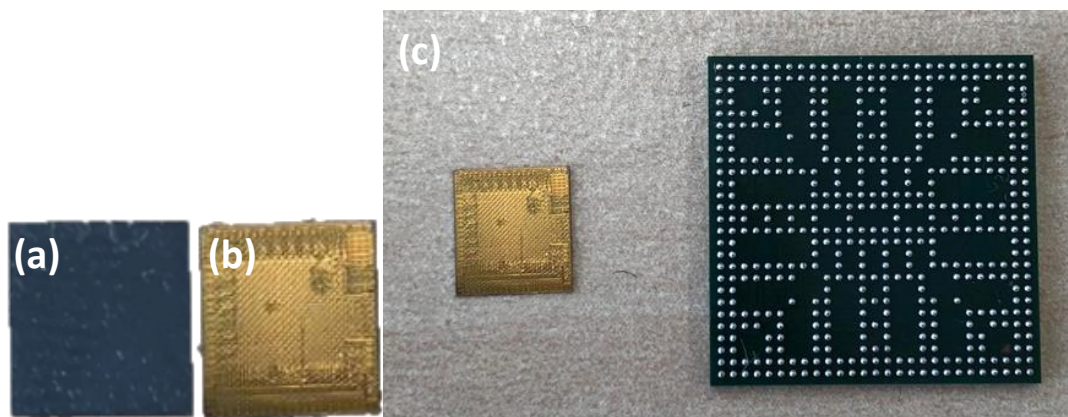


Figure 16 (a) Silicon chip side of bare die (b) Solder side of bare die (c) bare die and the chip



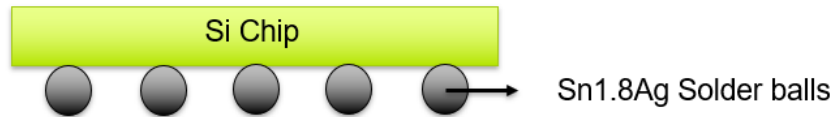


Figure 17 Schematic illustration of a bare die.

As already mentioned, bare dies comprise only chip substrate and solder joints, they need to attach to Cu substrates in order to create Cu/Sn/Cu reaction systems. In semiconductor industry, lead frame, a thin layer of Cu strip, is usually served as Cu substrate. In this study, four types of lead frames (Cu substrates) with different surface compositions resulting from various additive level added into electroplating bath were prepared to study the impact of impurities on void formation. The first reference lead frame is the commercial rolled Cu lead frame that has very high purity of Cu. In addition to the rolled Cu lead frame, three rolled Cu lead frames were electroplated with 15  $\mu\text{m}$  Cu layers using different additives in plating bath. In the plating bath, copper sulfate ( $\text{CuSO}_4$ ) provides a source of copper ions. Sulfuric acid ( $\text{H}_2\text{SO}_4$ ) makes the bath conductive and acts as a charge carrier. Three various additive formulas were added into bath separately; hence these three plated frames present different impurities level on the surface. The one using the most additives while electroplating is called Shiny Cu. It contained a variety of organic additives in the plating bath. Followed by Matt Cu that used only one commercial additive ended up with much fewer impurities than Shiny Cu. Finally, Virgin Cu which has no additives presented in the bath was prepared as well. More details and information on these frames will be discussed in chapter 4. Figure 18 shows all four different lead frames.

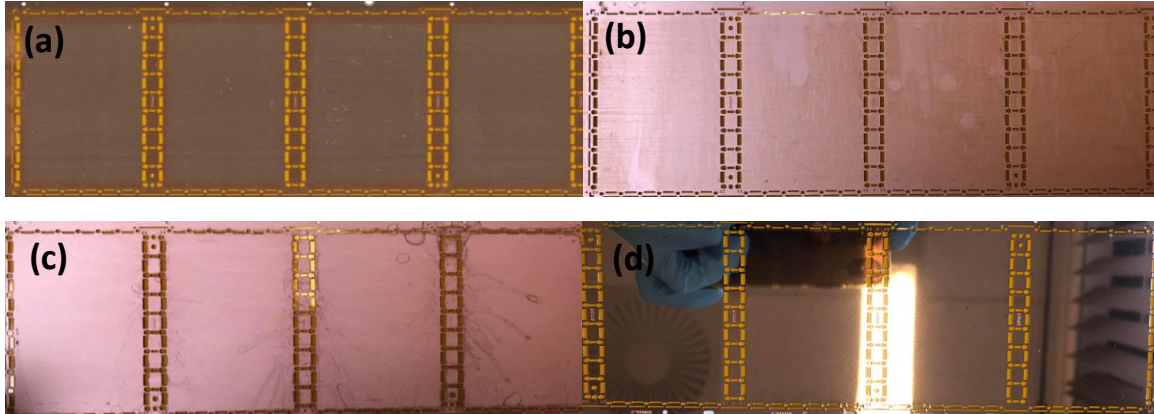


Figure 18 Four reference lead frames (a) Rolled Cu (b) Virgin Cu (c) Matt Cu (d) Shin Cu

## 3.2. Methods

This section includes both detail experimental procedures and finite element simulation on materials introduced in section 3.1.1. The second part of this chapter will focus on the set-up progress and experimental methods of the bare die system.

### 3.2.1. Thermal aging and cross section preparation for SEM: packaged test chip

There is one major requirement needs to be fulfilled when choosing a suitable thermal aging temperature. That is the temperature needs to be high enough to accelerate the void formation, yet it shouldn't exceed



the melting temperature of solder materials nor too high to sabotage the test chip. Experiments were carried out at 150°C and 175°C first. However, these temperatures were too low to expose voids within a reasonable time. On the other hand, 190°C shows an excellent result within appropriate time period. Hence, the thermal aging temperature was set to be 190°C in this study. Several pieces of test chips were placed in the oven and thermal aged for one to four weeks. One unit was taken out from the oven every week. Since the copper pillars and the solder joints are located in the center position of the test chip, diamond wire sawing the chip to the close center part was necessary. Firstly, the chip was mounted to the sample holder of the diamond wire cutting machine. Note that in order to mount the chip on the holder, heating up the holder with epoxy on it was needed. After the chip was fully attached to the holder, the holder and the chip were placed to the desired position with respect to the diamond wire. In this case, they were targeted to the position close to the die position. When one side of the chip was completely sawed through, the chip was rotated 90 degrees to another side and then the procedure was repeated again. Finally, after all four sides are sawed out, the remaining part was the desirable die. Wire sawing was a method to reach the close-center part of the test chip where the die and Cu pillars are. However, Cu pillars exist and distribute within the die in a very fine scale. A more sophisticated method such as ion milling was needed after sawing to desired positions of the Cu pillars. Some pre-polishing steps was performed before ion milling. The goal was to polish it to the edge of Cu pillars so the subsequent ion milling could expose a perfect cross section of Cu pillars for microstructural observation using a scanning electron microscopy (SEM). The steps involved were: (i) The die was released from the holder and mounted to the ion milling holder. (ii) Die was polished by SiC sandpaper from sandpaper number p240 to p2500. The cross-section surface was frequently checked by optical microscope during every step of polishing in order to keep track on the polishing position of dies. The X-ray picture shown in Figure 15 can serve as a blueprint while polishing. Keep reading the X-ray picture and choose a suitable sandpaper can massively increase the efficiency of polishing.

After all the polishing was done, the last step was ion milling. The concept of ion milling is to remove the part of sample that is not covered by mask with  $\text{Ar}^+$  beam, illustration shown in Figure 19 [38]. Thus, accurately place the mask is important in order to ion mill through the Cu pillars. One of its most powerful function is to create a smooth cross section while largely minimizing mechanical defects such as large residual stress, cracks etc.

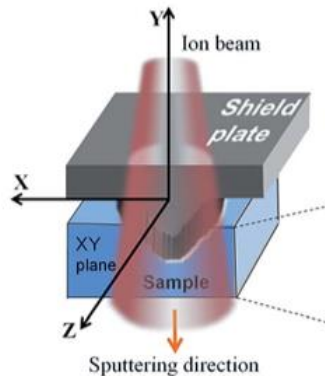


Figure 19 Schematic view of the cross-section ion milling process. The sample not protected by mask is polished with  $\text{Ar}^+$  beam [38].

Due to the existence of non-conductive material such as underfill in the test chip, coating an ultrathin layer of Pt on samples was required for SEM to enable or improve the imaging of the test chip. Creating a conductive layer of metal on the sample inhibits charging, reduces thermal damage and improves the secondary electron signal required for topographic examination in the SEM. Coating a roughly 5nm thick Pt layer is ideal. This layer is not thick enough to mask surface morphology but enough to provide a conductive coating to dissipate charging artifacts, any resultant heat buildup and minimize beam damage. The SEM used was Quanta FEG 250. The charge setting was generally 15kV and spot used was 4.0 to 5.0. The thicknesses of the intermetallic compounds and angle between  $\text{Cu}_6\text{Sn}_5$  grains were measured from the SEM images of the metallographic cross-sections using the image analysis method. The elemental compositions were determined using an energy dispersive X-ray spectrometer (EDX) equipped with Quanta.

### 3.2.2. Finite Element Analysis

Finite element simulations were used to assess the strain in the solder joint induced by IMC volume change under different conditions and circumstances. . Only half of the solder joint was constructed because the model was axisymmetric, as shown in Figure 20. The copper substrate thickness was 20  $\mu\text{m}$ , while the Cu pillar has a 30  $\mu\text{m}$  x 40  $\mu\text{m}$  (width x length) dimension. The total height of the Sn1.8Ag solder ball was 70  $\mu\text{m}$  from top to bottom, and the width was 45  $\mu\text{m}$ . A very fine mesh was used to ensure accuracy of the numerical simulation. The mesh size in the IMC region was 0.1  $\mu\text{m}$ , square elements while the size elsewhere was 1-3  $\mu\text{m}$ . There was one fixed point as indicated in Figure 20 while other edges could move freely. Plastic strain is related to the volume changes associated with the formation of Cu-Sn IMC,  $\text{Cu}_6\text{Sn}_5$  and  $\text{Cu}_3\text{Sn}$ . The IMC growth mechanism has been detailly discussed in chapter 2 already. In the model we only consider IMC growth into the solder direction, and neglect the small amount of  $\text{Cu}_3\text{Sn}$  growing into the Cu substrate, which we believe is reasonable approxiamtion. The measured IMC thickness data after different aging hours was then input to the model to simulate the actual IMC growth with aging time increasing. The IMC formation was applied by a moving front into the solder. Material factors such as Possion ratio, yield stress and Young's modulus of Cu, solder,  $\text{Cu}_6\text{Sn}_5$  and  $\text{Cu}_3\text{Sn}$  were assigned to their coresponding regions in the model. Their values are listed in table 1. The net volume change associated with IMC growth was simutaneously taken into account when the phase change occurs. In this model, the net volume change is -4.1 % for  $\text{Cu}_6\text{Sn}_5$  and -8.1 % for  $\text{Cu}_3\text{Sn}$  by calculation. These calculation on shrinkages have been proven experimentally by optical profilometer measuring the solder balls height before and after IMC formation. The simulations were split into two parts. The first part includes underfill, and the second part excludes underfill by omitting the underfill material from the model.

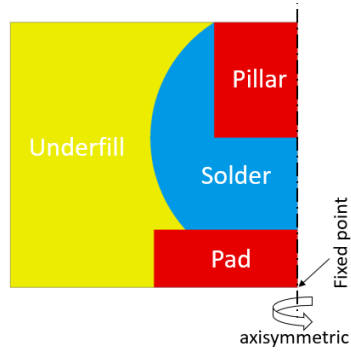


Figure 20 The initial structure of solder joint used in finite element simulation.

Table 1 Mechanical properties of solder, Cu, IMC used in FEA simulation

Parameters used in the simulations		
Parameter	Value	Ref
Young's Modulus of Solder	4.5 GPa	[31]
Possion ratio of Solder	0.45	[31]
Yield stress of Solder	10 MPa	[31]
Young's Modulus of Cu	128 GPa	[31]
Possion ratio of Cu	0.35	[31]
Young's Modulus of $\text{Cu}_6\text{Sn}_5$	117 GPa	[30]
Possion ratio of $\text{Cu}_6\text{Sn}_5$	0.309	[30]
Yield stress of $\text{Cu}_6\text{Sn}_5$	$10^5$	
Young's Modulus of $\text{Cu}_3\text{Sn}$	133 GPa	[30]
Possion ratio of $\text{Cu}_3\text{Sn}$	0.299	[30]
Yield stress of $\text{Cu}_6\text{Sn}_5$	$10^5$	

Note. The yield stress of two IMC were set to be extremely high deliberately to isolate the plastic behaviors of solder where voids form.

### 3.2.3. Samples preparation for Bare Die Model System

Table 2 *Design of experiments*

Design of Experiment		
Underfill	Lead frames	Reflow times
Without Underfill	Rolled Cu	1x
		5x
	Virgin Cu	1x
	Shiny Cu	1x
	Matt Cu	1x
With Underfill	Rolled Cu	1x

*Note. The aging time are four weeks for every variation.*

The design of experiments is shown in table 2. This experiment included factors such as whether or not there is underfill between the Cu pillar gaps, different Cu lead frames, and different reflow times. First of all, bare dies were flipped and attached to four lead frames as shown in Figure 21. Before attaching bare dies on lead frames, a thin layer of flux was smeared on the lead frames in order to clean the oxidation layer during reflowing. There are several choices of fluxes available in semiconductor packaging. Sticky flux was chosen here because of its non-corrosive characteristics. After attaching, the frames with dies on them were reflowed in reflow oven. The reflow temperature profile was already shown in Figure 4. Flux cleaning was performed right after reflow. Since sticky flux is water soluble, demi water was used to clean the flux. The cleaning was done by immersing the lead frames and dies into demi water at 50°C aided by ultrasonic vibration for 20 minutes. Flux cleaning is especially important if underfill will be filled into the gaps between solder joints. Extra rinsing time for those samples was needed. After flux cleaning, some samples were reflowed four more times to prepare for 5-times-reflow samples. So far, samples without underfill were ready.

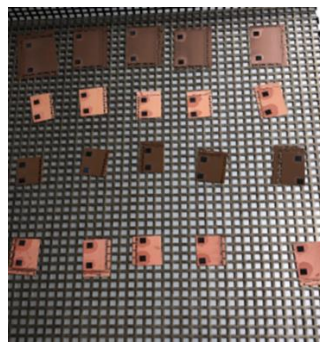
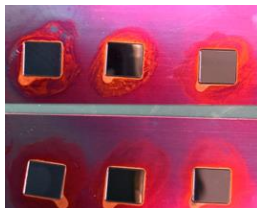


Figure 21 *Demonstration of flipped bare dies on four lead frames*

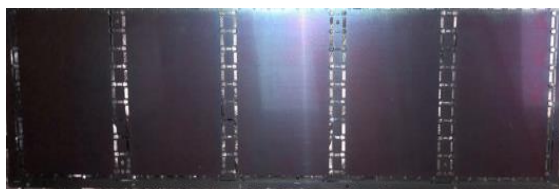
The last step was to fill in underfill to prepare for with-underfill samples in table 2. First step was to pre-heat the samples at 125°C for 30 minutes before underfilling to prevent liquid or moisture from flux cleaning. This made sure the quality of underfilling would be stable. Then, underfill was applied manually along the edges of the dies. It would flow into the gaps in the die viscously by capillary reaction. Lastly, two hours of curing at 100°C was performed in order to solidified the underfill. Figure 22 shows sample with underfill when all the steps were completed. Until then, all the tested samples were created and were ready for thermal aging.



*Figure 22 Bare dies on rolled Cu with underfill*

#### **3.2.4. Thermal aging and cross section preparation for SEM: bare die model**

Owing to the fact that Cu pillars in bare dies are exposed to the air directly without any protection from underfill or molding compound; thermal aging in a low oxygen atmosphere is highly recommended. The aging oven used was nitrogen oven that can reduce the oxygen level to lower than 20 ppm. A pre experiment was done to check the effect of nitrogen oven. Cu lead frame shows excessive oxidation when it was aged in atmosphere oven, as shown in Figure 23. In contrast, when it was aged by Nitrogen oven, there was no severe color change introduced by oxidation layer. Thereby, nitrogen oven was a better environment for bare dies aging.



*Figure 23 Lead frame after 1 hour aging in normal atmosphere oven*

Concerned that organic underfill might outgas and contaminate other samples during thermal aging; all the samples were wrapped with Al foil separately to minimize their influence on others. The aging temperature was 190°C. Took one unit of each variable out every week for four weeks. Overall, we would have zero to four weeks aging time for every variable in table 2.

Having discussed how the samples were prepared and aged, how the cross sections were made for SEM will be addressed next. Similar to the cross-section preparation procedure of the packaged test chip, the sample was firstly mounted to ion mill holder by epoxy and then polished by SiC sandpaper. The cross-section surfaces were constantly checked during polishing. The polishing wasn't finished until the cross-section surfaces were ground to the edge of Cu pillars. The ion milling mask was precisely adjusted to

suitable position with respect to the polished dies. Some samples with weaker connections between solder joints and lead frames could not be mechanically polished without peeling off from the lead frames or generating cracks into the joints. Hence, these samples were polished using a plasma focused ion beam (Plasma FIB, JEOL). The ion source is focused on the sample to obtain a small beam that can etch the surface with material removing. For bare die with this thickness, it is time consuming to make cross section with normal FIB. However, plasma FIB provides a faster etching rate and a bigger cover area making this technique a perfect match for this experiment.

### 3.2.5. Surface analysis

Surface analysis on four different lead frames was carried out by X-ray photoelectron spectroscopy (XPS). XPS is typically accomplished by exciting the surface with mono-energetic Al  $K_{\alpha}$  X-rays causing photoelectrons to be emitted from the sample surface. An electron energy analyzer is used to measure the energy of the emitted photoelectrons. From the binding energy and intensity of a photoelectron peak which is recorded as spectrum, the elemental identity, chemical state and quantity of an element can be determined. Depth information can be obtained by combining XPS spectroscopy measurements with ion milling (sputtering) to characterize the film composition and structure. See Figure 24 for XPS illustration [39]. The analyzed frames were firstly reflowed with flux on them to clean the oxidation layer. Residue flux was then cleaned by demi water. These frames were then subjected to XPS testing. Lead frames without flux cleaning were tested too to check the effectivity of flux. The result will be discussed in chapter 4.

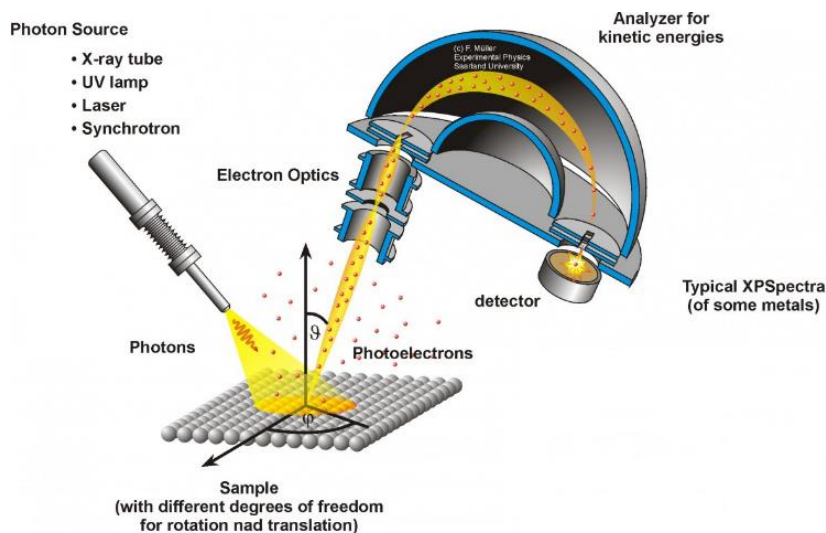


Figure 24 XPS functional illustration [39]

# 4

## Results and discussion

In this chapter, all concerning factors that can influence the IMC/void formation will be discussed and studied.

### 4.1. Growth of IMC

The two IMC phases formed in the packaged test chip during thermal aging have been identified to be  $\text{Cu}_6\text{Sn}_5$  and  $\text{Cu}_3\text{Sn}$  by EDX. The EDX results can be found in Appendix A. The growth kinetics of the IMC layer in a solid-state reaction is generally considered to follow an empirical power-law relation shown in equation 9 below [40].

$$h = h_0 + Kt^n \quad (9)$$

where  $h$  is the total thickness of interfacial IMC,  $h_0$  is the initial thickness of IMC,  $K$  is the coefficient of IMC growth rate which is strongly related to the diffusivity of atoms in IMC,  $t$  is the reaction time and  $n$  is the time exponent. As already discussed, the  $n$  value can be used to determine which mechanism is controlling the growth of IMC. As a result, calculating the  $n$  value is the first step to understand how IMC are formed. The value  $n$  can be derived from equation 10 below.

$$\log(h - h_0) = \log K + n \log t \quad (10)$$

Figure 25a shows the thickness of  $\text{Cu}_6\text{Sn}_5$  and  $\text{Cu}_3\text{Sn}$  as a function of aging time at  $190^\circ\text{C}$ . Figure 25b shows the thickness of IMC as a function of aging time in log–log format. It can be seen that the thickness of  $\text{Cu}_6\text{Sn}_5$  and  $\text{Cu}_3\text{Sn}$  layer are linearly related to the aging time on a log scale. According to the linear fitting results, the values of the time exponent was 0.55 and 0.39 for  $\text{Cu}_6\text{Sn}_5$  and  $\text{Cu}_3\text{Sn}$  respectively. Thus, the growth of  $\text{Cu}_6\text{Sn}_5$  during thermal aging at  $190^\circ\text{C}$  is controlled by volume diffusion while  $\text{Cu}_3\text{Sn}$  is controlled by grain boundary diffusion.

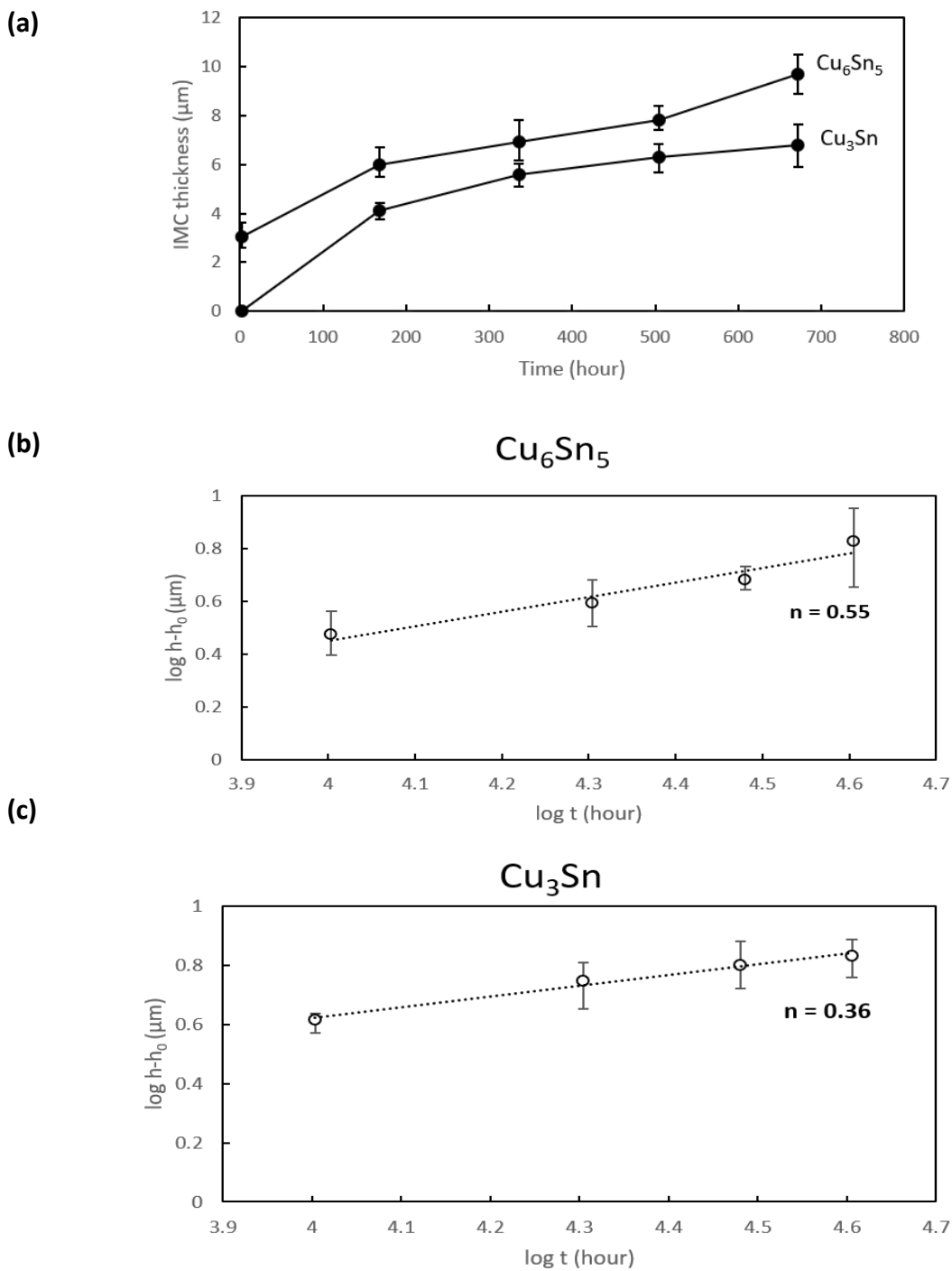


Figure 25 (a) IMC thickness vs. Aging time (b) Thickness of  $\text{Cu}_6\text{Sn}_5$  as a function of aging time in logarithmic scale (c) Thickness of  $\text{Cu}_3\text{Sn}$  as a function of aging time in logarithmic scale  $\text{Cu}_3\text{Sn}$



## 4.2. Void formation and self-healing mechanism in packaged test chips

Figure 26 shows typical cross-sectional SEM micrographs of test chips solder joints, where samples were aged at 190°C from zero to four weeks.

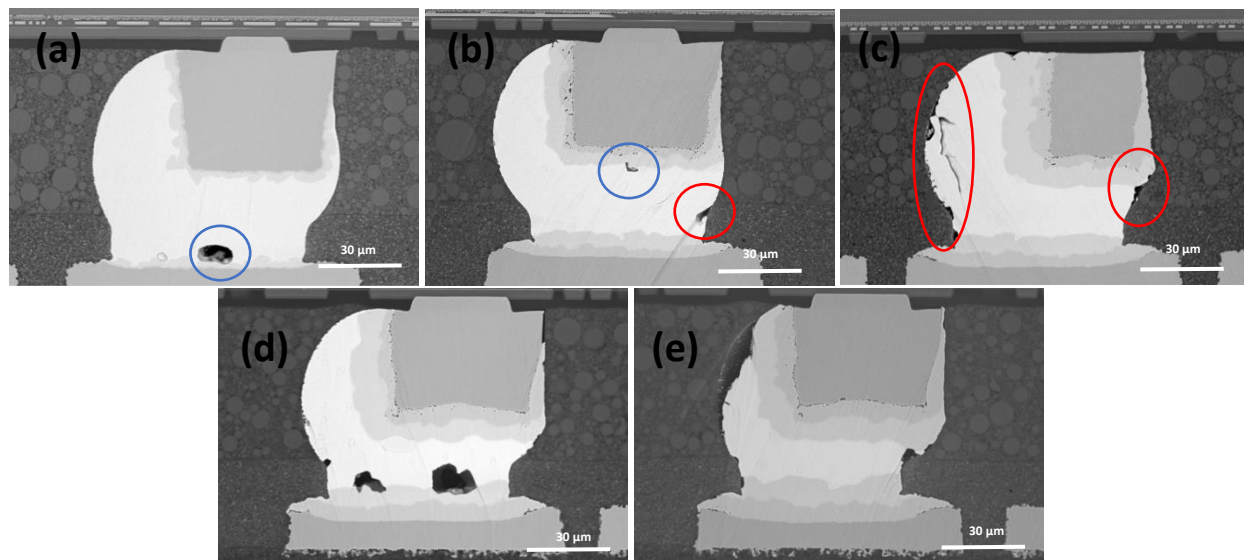


Figure 26 SEM micrographs of test chips. Thermal aged for (a) non-aged (b) one week (c) two weeks (d) three weeks (e) four weeks

Before aging, the  $\text{Cu}_6\text{Sn}_5$  phase shows a scalloped-type shape and only a very thin  $\text{Cu}_3\text{Sn}$  layer was formed as shown in Figure 26a. The circled area is essentially a gas bubble produced by the evaporation of the solvent in the flux residue during the heating process of reflow [41, 42]. This indicates that the use of flux in the reflowing process may also cause voids to form inside the solder matrix. This type of voids can be eliminated by better processing parameters and better quality of flux. Eliminating them hasn't been an issue; hence, they are relatively less significant and won't be focused in this report. As aging time increases to one week,  $\text{Cu}_3\text{Sn}$  layer grows and becomes visible. In addition, a small quantity of volume shrinkage takes place in the solder outcurve as can be seen in the red circle in Figure 26b. This shrinkage is attributed to the volume shrinkage when IMC are formed. During IMC formation,  $\text{Cu}_6\text{Sn}_5$  undergoes a 4.1% volume shrinkage while the shrinkage for  $\text{Cu}_3\text{Sn}$  is 8.1%. The volume shrinkage exerts a high tensile stress at the solder/underfill connection region. These shrinkages could be accommodated by strain of solder materials to some extent. However, when it exceeds yield strain of the solder, solder starts to shrink in order to compensate these volumes lose. Note that a small flux residue-induced void remains in here as well, see the blue circle. The solder experiences an even larger volume shrinkage around the solder ball when it is aged for two weeks, see Figure 26c. After aging for three weeks, further IMC formation leads to a high local stress state at the interface of  $\text{Cu}_6\text{Sn}_5$  and solder. When this local tensile stress exceeds the critical stress of void formation, voids will start to form, as shown in Figure 26d. However, after aging for four weeks, the voids show abnormal disappearing behavior, as shown in Figure 26e. A self-healing mechanism seems to facilitate voids to annihilate themselves. In order to understand the mechanism better, a theory is postulated here to demonstrate how voids self-heal themselves. Firstly, the surface tension of  $\text{Cu}_6\text{Sn}_5$ /solder is calculated by equation 10.

$$\gamma_{gb} = 2\gamma_{il} \cos \varphi_{il} \quad (10)$$

The angles of two neighboring  $\text{Cu}_6\text{Sn}_5$  grains  $\varphi_{il}$  are measured and averaged to be  $21^\circ$ , see Figure 27. Taking grain boundary energy of Sn  $\gamma_{gb}=164 \text{ (mJ/m}^2\text{)}$  to represent  $\text{Cu}_6\text{Sn}_5$  due to the lack of value for  $\text{Cu}_6\text{Sn}_5$  [43]. The interfacial surface tension at  $\text{Cu}_6\text{Sn}_5/\text{solder}$  is then calculated to be  $88 \text{ (mJ/m}^2\text{)}$ . Secondly, in order for a void to be stable the concentrated tensile stress at the void tip must exceed the surface curvature induced back stress described by equation 11,

$$\sigma = \frac{2\gamma}{R} \quad (11)$$

where  $R$  is the radius of curvature and  $\gamma$  is the surface tension [44]. This barrier may be lower at interfaces between layers or with impurities, but in general voids below a certain critical size will tend to annihilate. In this case, the average curvature of the voids in Figure 26d is  $3 \text{ }\mu\text{m}$  measured by SEM image analysis method. Applying surface tension at  $\text{Cu}_6\text{Sn}_5/\text{solder}$ :  $88 \text{ (mJ/m}^2\text{)}$  and average curvature:  $3 \text{ }\mu\text{m}$ ; the tensile stress needed to sustain voids is estimated to be  $59 \text{ MPa}$ . This suggests that a local tensile stress higher than  $59 \text{ MPa}$  will generate because of the IMC formation from both Cu pillar side and Cu substrate side. However, after aging for four weeks voids tend to self-annihilate as can be seen in Figure 26e suggesting that the compressive stress in the tip of voids will compensate this  $59 \text{ MPa}$  tension stress and cause the voids to close themselves. This compressive stress can originate from the volume shrinkage in solder balls. When the solder ball shrinks, it exerts a compressive stress to “squeeze” the inner part of the solder ball and locally close the voids. That is why voids do not exist when there is a lot of volume shrinkage at the outcurve of solder ball after four weeks aging (Figure 26e) while voids appear to form where there isn't shrinkage in the solder outcurve after three weeks aging (Figure 26d). In the next section, a finite element model will be built to demonstrate the shrinkage of solder ball after aging. One thing should be kept in mind while calculating the stress is that the surface energy would decrease with increasing temperature. Hence, the grain boundary energy  $\gamma_{gb}$  would be slightly lower than  $164 \text{ mJ/m}^2$  at  $190^\circ\text{C}$  causing a critical tensile stress even lower than  $59 \text{ MPa}$  for voids formation.

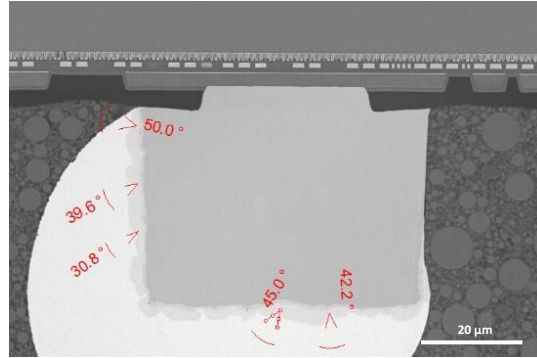
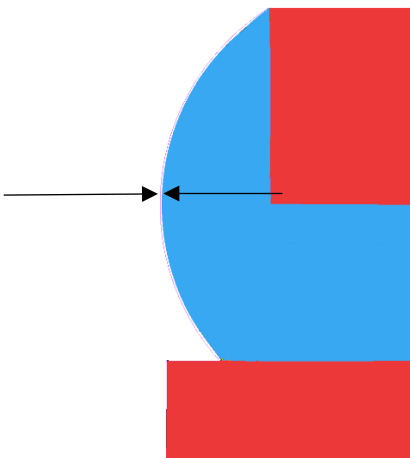


Figure 27 Angle measurement of  $\text{Cu}_6\text{Sn}_5$  grains by SEM

### 4.3. Finite element simulation

Figure 28 shows the solder shape after four weeks aging at 190°C. The thin line right adjacent to the solder ball is the original shape of the solder ball before aging (the gap is indicated by arrows in the Figure 28.) This implies the solder will shrink after four weeks aging to accommodate the volume shrinkage originating from IMC formation. This corroborates the experimental results shown in Figure 26e. Furthermore, the FEA model results in Figure 29 shows the strain in vertical direction of solder joints thermal aged at 190°C after certain amount of time. Two conditions were considered in Figure 29a and Figure 29b: with and without underfill. With underfill, an ununiform large strain deformation occurs, which might cause voids in the solder. This is in agreement with the irregular voids occurrence in Figure 26d. The non-uniform feature of strain can be traced back to the different geometry of upper Cu pillar and lower Cu substrate causing IMC from both ends grow differently. Clearly, the strain in solder joints with underfill is higher than the ones without underfill. The local strain can be as high as 60% with underfill and can only be 25% without underfill. It is because the underfill is a rigid boundary constraining solder ball to move apart from after IMC formation. As a result, the constraint would lead to a higher stress state and higher strain. This result implies voids have higher forming tendency when they are subjected to underfill. It is consistent with experimental results that will be discussed in section 4.4 and section 4.5. Note that a lot of assumptions were made in these models. These assumptions have large influences on strain development which might cause the simulated strain to deviate from actual strain. Despite the simulated strain value does not necessarily represent the actual strain; this model does give a fairly clear first insight into how voids are formed concerning IMC volume shrinkage and it does strongly support the experimental results.



*Figure 28 Shape of solder joint after four weeks thermal aging at 190°C. The thin line outside solder ball area is the original shape of solder joint before aging. The gap indicated by arrows is the shape shrinkage after aging.*

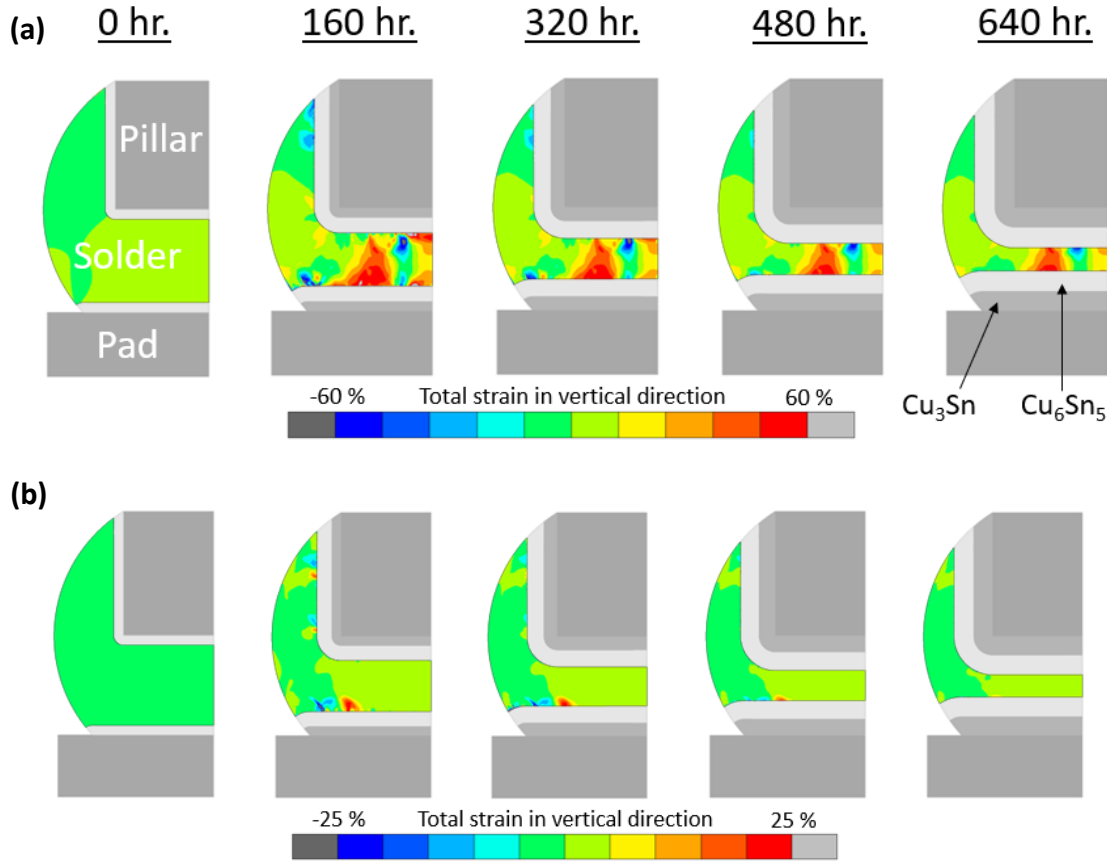


Figure 29 Strain in vertical direction of solder joints at 190°C (a) With underfill (b) Without underfill

#### 4.4. Effect of thermal aging time in bare die system

Figure 30 shows the cross section of bare die system, rolled Cu 1x reflow samples that were subjected to thermal aging from zero to four weeks. The EDX results have confirmed that two phases formed in this sandwich structure are  $\text{Cu}_6\text{Sn}_5$  and  $\text{Cu}_3\text{Sn}$ , as shown in Appendix A. As can be seen in Figure 30, there is still flux remaining besides the Cu pillars and the solder. However, research has shown organic flux has minimum corrosive effect on solder joints [45]. Hence, the existence of flux does not influence the results presented here. Before the sample was aged, only one cycle of reflowing had been conducted. The typical scallop-typed  $\text{Cu}_6\text{Sn}_5$  is found in this sample. After one-week aging,  $\text{Cu}_3\text{Sn}$  grows to a visible amount by consuming  $\text{Cu}_6\text{Sn}_5$  while the latter continues to grow until almost all solder materials are transformed. Some solder will remain in  $\text{Cu}_6\text{Sn}_5$  in forms of “islands” due to scallop-typed  $\text{Cu}_6\text{Sn}_5$  impingement, see red circles in Figure 30b. When upper  $\text{Cu}_6\text{Sn}_5$  grains from Cu pillars side start to impinge on the lower ones from Cu substrate at certain locations due to scallop shape; solder will be isolated into many small islands. When aging time increases to two weeks,  $\text{Cu}_6\text{Sn}_5$  phase is almost consumed entirely by  $\text{Cu}_3\text{Sn}$ . After three weeks aging, there is only  $\text{Cu}_3\text{Sn}$  phase present because  $\text{Cu}_6\text{Sn}_5$  continuously transformed into  $\text{Cu}_3\text{Sn}$  while no new  $\text{Cu}_6\text{Sn}_5$  can be grown because of insufficient solder. In addition, the solder islands will slowly transform into  $\text{Cu}_6\text{Sn}_5$  once Cu atoms reach them and further transform into  $\text{Cu}_3\text{Sn}$  eventually making samples contain only  $\text{Cu}_3\text{Sn}$  after three- and four-weeks aging

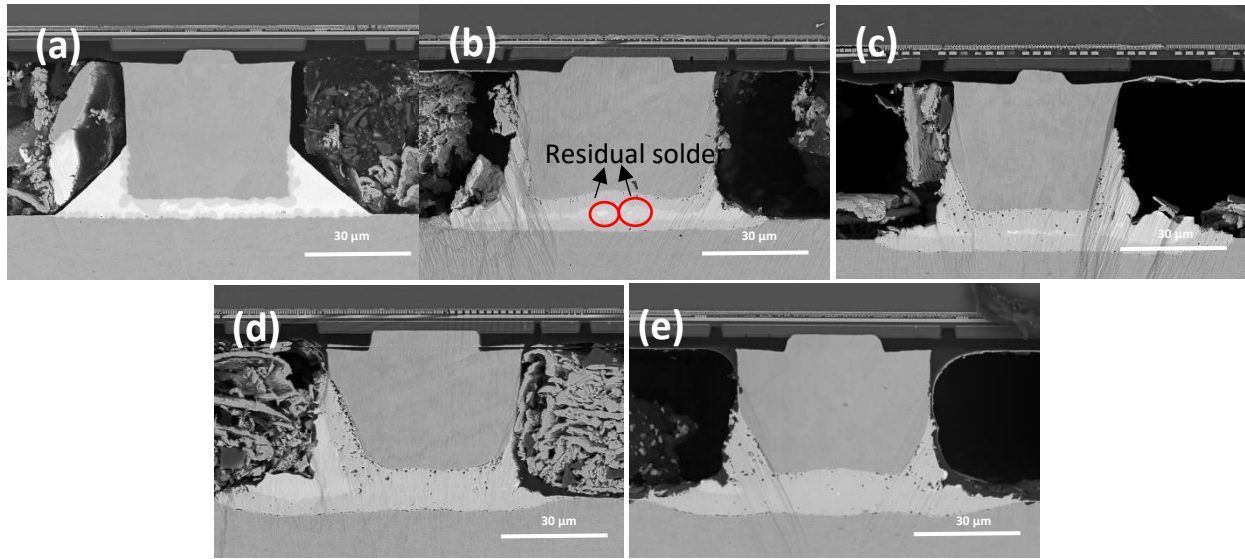


Figure 30 SEM micrographs of rolled Cu 1x reflow Thermal aged for (a) non-aged (b) one week (c) two weeks (d) three weeks (e) four weeks

However, in some units (different Cu pillars units but undergo the same thermal aging time, i.e., zero to four weeks), we occasionally found voids appear in the positions where the solder islands originally were, as shown in Figure 31. These samples were thermal aged for one week and four weeks respectively. This leads to a speculation that the stress generated with volume shrinkage cannot be fully dissipated by this volume shrinkage. Sometimes the volume shrinkage during IMC formation will generate a high local stress state and cause voids.

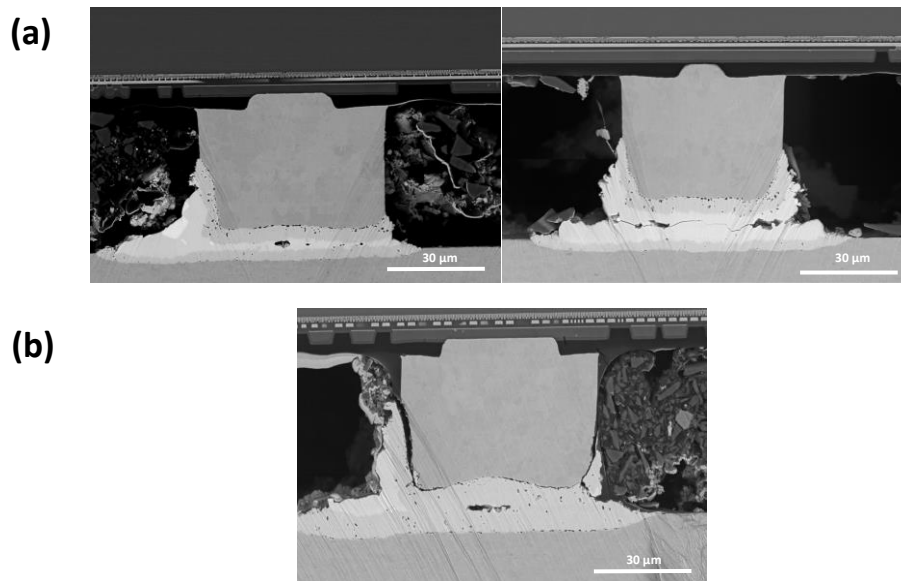


Figure 31 Voids found in rolled Cu 1x reflow thermal aged for (a) one week (b) four weeks

Therefore, a model is built and proposed to demonstrate this void formation. The sequence of events for volume shrinkage and void formation are illustrated in Figure 32. Firstly, a non-aging solder joint is shown in Figure 32a. Secondly, volume shrinks when  $\text{Cu}_6\text{Sn}_5$  phase forms during thermal aging as shown in Figure 32b. After an incubation time,  $\text{Cu}_3\text{Sn}$  begins to form while  $\text{Cu}_6\text{Sn}_5$  keeps growing, see Figure 32c. The growths of these IMC further contribute volume shrinkage. In general, the further the IMC grow, the more volume shrinks. When upper  $\text{Cu}_6\text{Sn}_5$  grains impinge with lower ones, the system will stop shrinking in volume and leave many Sn islands at the same time due to their scallop-shape nature, see Figure 32c. The volume shrinkage from both ends exerts a tensile stress in the center, as plastic deformation is very difficult in brittle IMC, when this tensile stress reaches critical stress value of void formation, voids will form at the solder islands in order to dissipate the shrinkage stress, as shown in Figure 32d. Finally,  $\text{Cu}_3\text{Sn}$  will keep consuming  $\text{Cu}_6\text{Sn}_5$  until it covers the whole joint, as shown in Figure 32e.

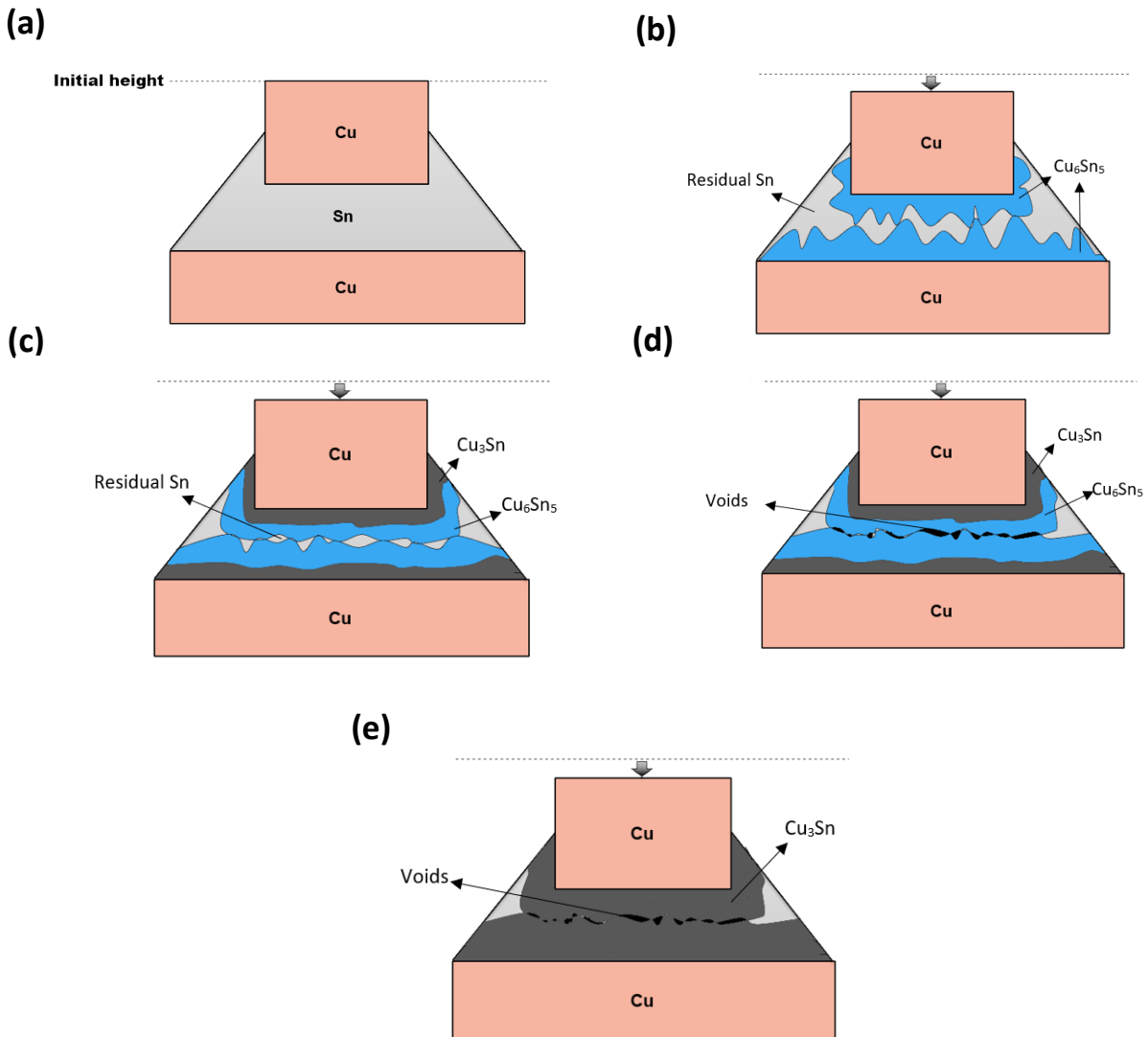


Figure 32 Illustration of how voids related to volume shrinkage during thermal aging. (a) Initial Cu/Sn/Cu sandwich structure (b) Volume (Height) shrinkage after  $\text{Cu}_6\text{Sn}_5$  formation (c)  $\text{Cu}_3\text{Sn}$  formation and impingement of  $\text{Cu}_6\text{Sn}_5$  grains (d) Void formation (e)  $\text{Cu}_6\text{Sn}_5$  fully transform into  $\text{Cu}_3\text{Sn}$



#### 4.5. Effect of underfill in bare die system

Figure 33 shows the cross-section SEM images of rolled Cu 1x reflow with underfill samples that were thermal aged from zero to four weeks. As stated last section, when the volume shrinkage is not enough to compensate the shrinkage stress; a high tensile stress will be generated locally and will cause voids to form. However, unlike samples without underfill can freely conduct volume shrinkage without any constraint; underfill prohibits volume shrinkage because it is firm enough to stop the height from decreasing when IMC starts to form. Hence, without height shrinkage contributes to the release of the stress, the stress tends to become higher for those samples with underfill. That is to say, voids will form more easily and frequently under this condition. This is consistent with the FEM result. In last section, we have already discussed that voids were found occasionally in some units. In contrast, voids were found in every unit in this set of samples with underfill. In Figure 33a, before thermal aging,  $\text{Cu}_6\text{Sn}_5$  appears in scalloped type. The underfill surrounding the Cu pillars and solder perfectly attach to them. This implies the inorganic sticky flux does not influence the wetting of underfill and shows a promising outcome. After one-week aging, voids begin to form in the solder island positions and will remain in there for all four weeks aging, see Figure 33b to Figure 33e. Another interesting thing worth to point out is that after four weeks aging, not only do the voids form in the solder islands positions, but they also form in the corner region where solder attach to underfill, see the circle in Figure 33e. They are normally called fillets. The existence of fillets can be attributed to the underfill act as a stiff material that continuously pulling the solder when it tries to shrink. This pulling can further generate a large stress and cause fillets. The geometry (height and width) of fillets was proven to have influential effect on interfacial stress field of solder joint [46]. This explains why the corner triangle-shaped fillets only exist in bare die model system (Figure 33) but not present in test chips (Figure26). In section 4.2, we discussed the self-healing of voids in test chips. However, the self-healing of voids does not appear here. It might be because of the different geometry of the solder joints causing the different stress field distribution. In the bare die model system, the shrinkage of fillets has limited influence on stress around voids tips due to fillets only exist in the triangle corner. On the other hand, for test chips, the solder has a round shape and can possibly have a more direct influence on voids when it shrinks (apply a compressive stress on voids when it shrinks).

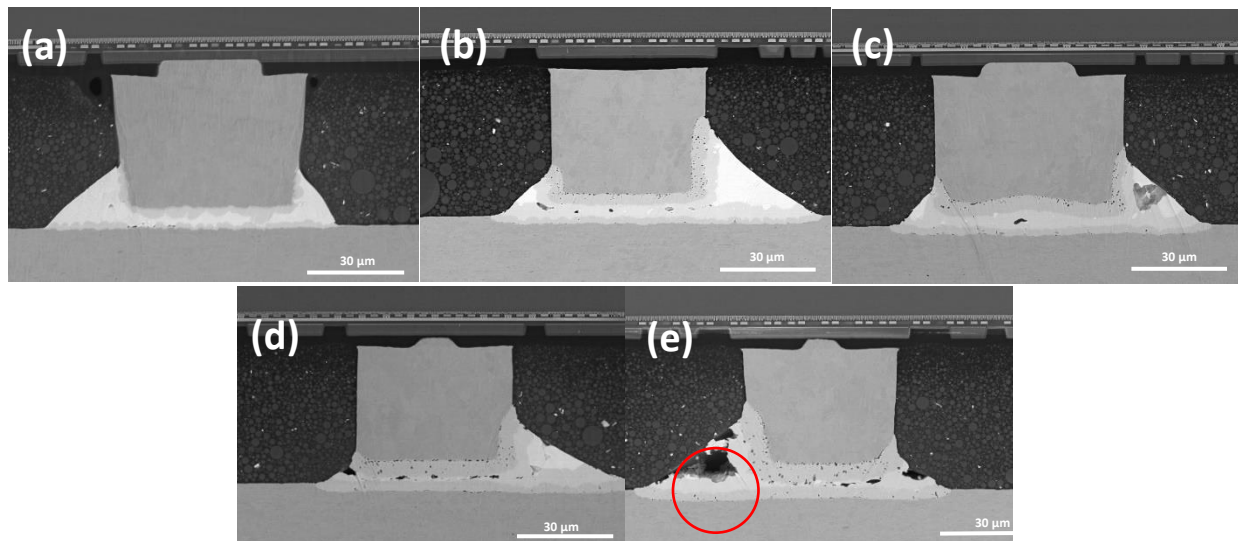


Figure 33 SEM micrographs of rolled Cu 1x reflow with underfill thermal aged for (a) non-aged (b) one week (c) two weeks (d) three weeks (e) four weeks

## 4.6. Effect of different reflow times in bare die system

Figure 34 shows cross section images of rolled Cu 5x reflows without underfill samples. Before aging, the scalloped  $\text{Cu}_6\text{Sn}_5$  has grown very thick already. This can be originated from the longer period of time the samples experienced at high temperature. The higher reflow times resulted in enhanced reaction and diffusion, which contributed to a thicker IMC before aging. Comparing to one time reflow samples, samples prepared by five times reflows show more cracks in the IMC. See Figure 34d, not only do the delamination layer exists between two IMC, IMC itself also shows large cracks within it. This might be due to the Si chip, the solder, the substrate and the IMC thermally expand in different rate when reflowing at high temperature [47]. This difference of CTE put the solder joint under stress since they expand at different rates creating high mismatches between materials. These mismatches put the joints under a stress that the solder cannot absorb, therefore leading to fractures in the solder connections.

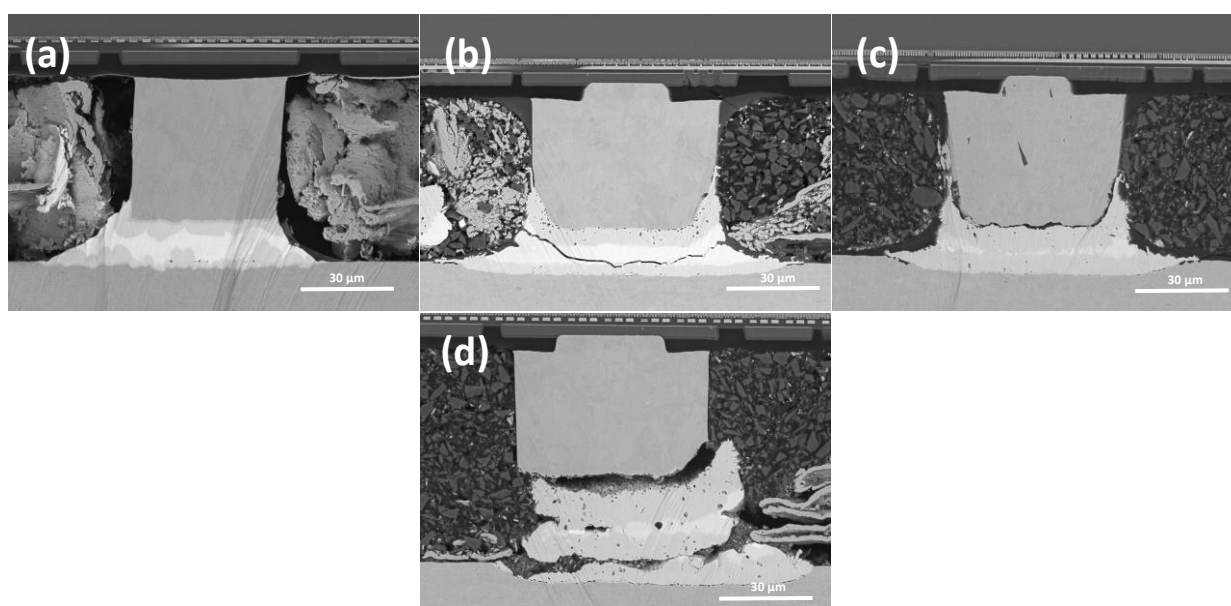


Figure 34 SEM micrographs of rolled Cu 5x reflow thermal aged for (a) non-aged (b) one week (c) two weeks (d) three weeks

On the other hand, if underfill was applied to 5x reflows sample the cracks would no longer present. See Figure 35. The reason is that underfill can compensate the large thermal expansion mismatch between the silicon chip, the solder ball, and the substrate. The CTE of silicon is approximately 3.5 ppm/K, and typical copper substrate has a CTE of 17 ppm/K. Large cracks are observed in the solder joints due to this thermal expansion mismatch. To compensate for this mismatch, a underfill with a CTE close to that of the solder bumps ( $\sim 23$  ppm/K) is deposited and cured in the gap between the chip and substrate [48]. The use of underfill enables structural coupling of the chip and substrate, effectively decreasing the high CTE difference and thus lowering the probability of cracks in solder joints.



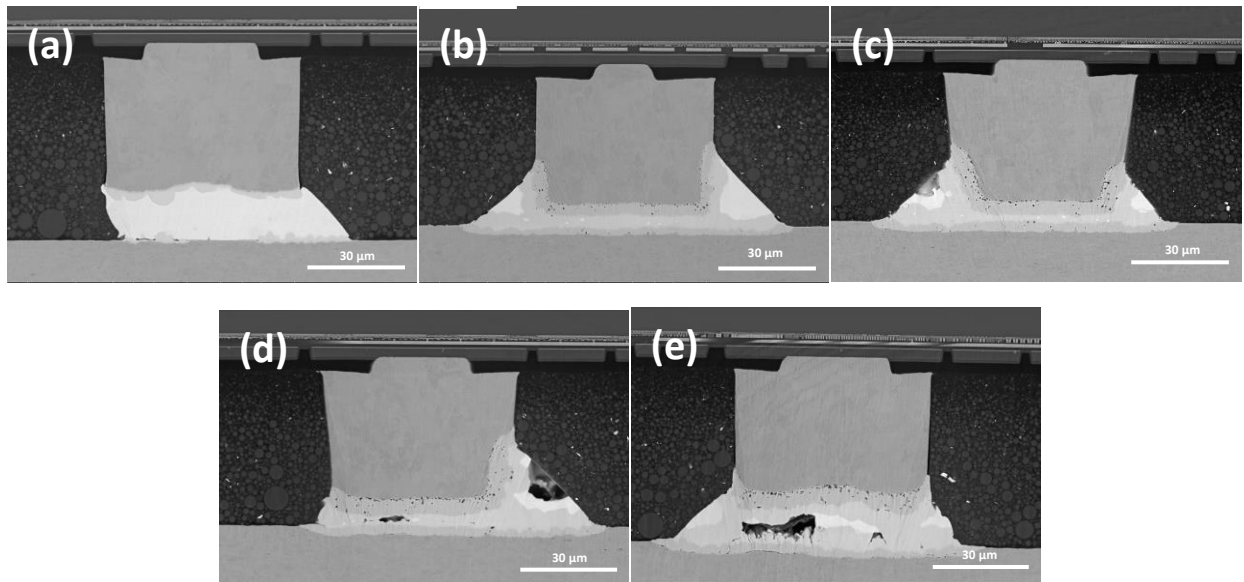


Figure 35 SEM micrographs of rolled Cu 5x reflow with underfill thermal aged for (a) non-aged (b) one week (c) two weeks (d) three weeks

#### 4.7. Effect of different additive level in bare die system

Figure 36 shows cross section images of shiny Cu (with the most additive level while plating among three variants) before and after one, two weeks thermal aging. The cross sections after aging were made by plasma focus ion beam (PFIB) due to weak connections bare dies have on this type of frame. When these samples were subjected to mechanical polishing, the severe Kirkendall voids at  $\text{Cu}_3\text{Sn}/\text{Cu}$  interfaces act as a disconnection layer between Cu substrates and bare dies resulting in peeling off failure. PFIB could minimize mechanical cracks and has shown an excellent outcome. Figure 37 shows images of matt Cu (with second highest additive level among three) and Figure 38 shows images of virgin Cu (with no additive added in the plating bath) before and after one, two weeks aging. Comparing three variants after one week thermal aging, apparently shiny Cu shows the most Kirkendall voids, followed by matt Cu and lastly virgin Cu, as can be seen in red circles in Figure 36b, Figure 37b and Figure 38b. The severity of Kirkendall voids in each variant is consistent with the additive level added during electroplating. Therefore, the impurities level on the surface of lead frames can indeed enhance the amount of Kirkendall voids. Increasing the aging time to two weeks, shiny Cu shows a large amount of voids leading to failure even with PFIB, as can be seen in Figure 36c. In Figure 37c, a delamination layer causes the Cu pillar fails apart from the IMC. This can be due to occurrence of stress after PFIB. In Figure 38c, there is still limited Kirkendall voids in virgin Cu after two weeks aging. However, the connection is too weak due to thick IMC layer (will be discussed in section 4-8) causing failure to occur. In principle, after electroplating, the plating can introduce an additional tensile stress to the Cu surface [28]. Once nucleated, voids can grow by local tensile stress, originating from residual stress in the film and the Kirkendall effect. Nevertheless, the fact that virgin Cu shows minimum Kirkendall voids suggest that not only does the tensile stress have enormous influence, but the impurities segregation can also be an essential factor. The impurities segregation can act as nucleus for heterogeneous nucleation at  $\text{Cu}_3\text{Sn}/\text{Cu}$  interface resulting in lowering activation energy of void nucleation. This lower activation energy makes void formation become easier;

as a result, more voids can be found in lead frames with more additives. In addition, the segregation of impurities can occupy the vacancy sinks such as grain boundaries, dislocations where vacancies tend to annihilate. This further assists the Kirkendall voids effect. The reason why impurities segregation occurred only to Cu/Cu<sub>3</sub>Sn interface and not to other boundaries, such as Cu<sub>3</sub>Sn/Cu<sub>6</sub>Sn<sub>5</sub> and Cu<sub>6</sub>Sn<sub>5</sub>/Sn, seems to be related to the incoherent structure of the Cu/Cu<sub>3</sub>Sn interface.

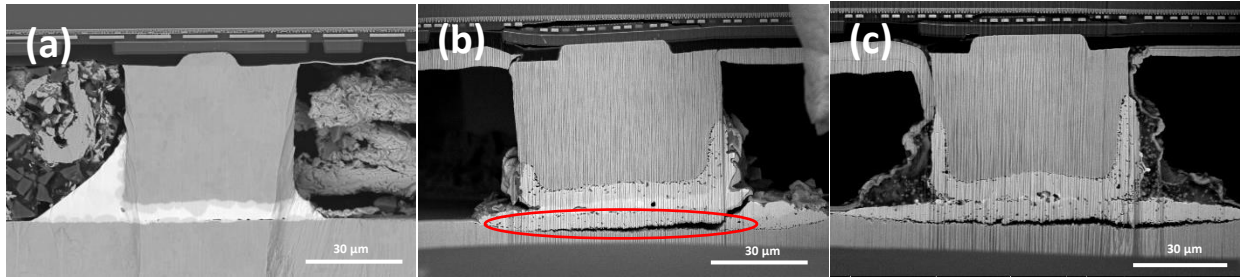


Figure 36 SEM micrographs of shiny Cu thermal aged for (a) non-aged (b) one week (c) two weeks

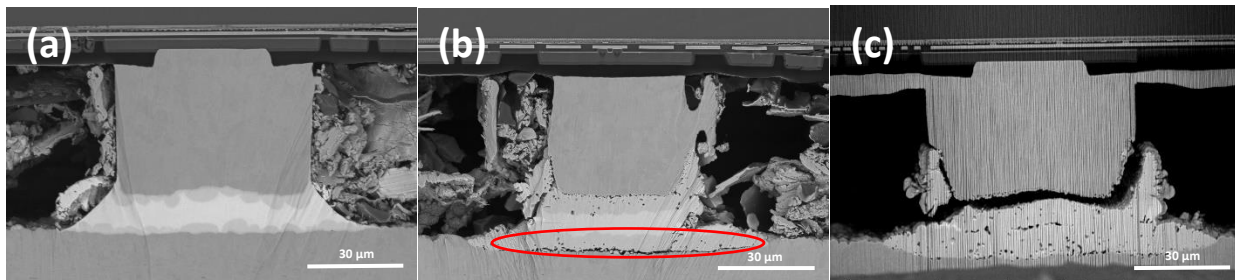


Figure 37 SEM micrographs of matt Cu thermal aged for (a) non-aged (b) one week (c) two weeks

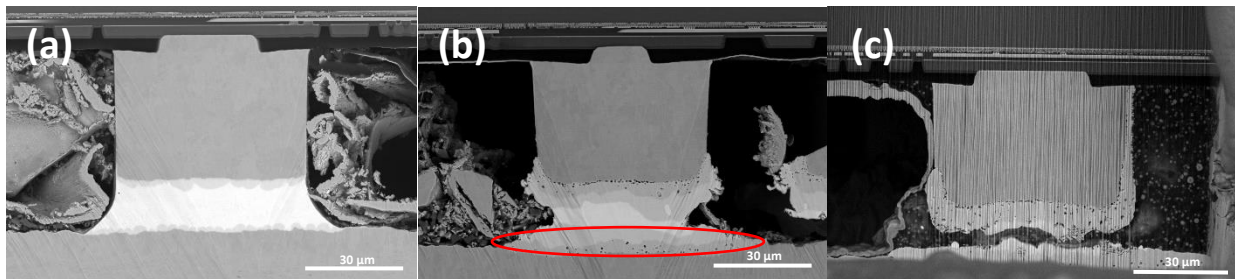


Figure 38 SEM micrographs of virgin Cu thermal aged for (a) non-aged (b) one week (c) two weeks

As we have confirmed higher impurities level during electroplating could increase Kirkendall voids. The next step is to suggest a potential element that might be the root cause of this severe Kirkendall voids. To study the surface composition of three plated lead frames, XPS was performed on them. Table 3 shows XPS surface analysis of rolled Cu lead frame (reference) and all three electroplated Cu lead frames: shiny Cu, matt Cu, virgin Cu. The data represents atomic concentration and has been normalized to 100% for each frame. In general, there are carbon, nitrogen, oxygen in all three electroplated lead frames. Tin was only found in matt and virgin Cu. On the contrary, tin was absent in shiny Cu which occurs to have the most Kirkendall void. Therefore, we can conclude that tin isn't responsible for the severe voids here. Nitrogen presented in all three coated lead frames was originated from flux residue as there wasn't nitrogen detected before flux application (See Appendix B for detail results on XPS analysis.) When reflowing, flux will be removed from the surface where IMC starts to form and thus will have no impact

on IMC formation. Consequently, nitrogen is not a possible candidate that helps voids to form. An XPS depth profile has been performed on lead frames to verify that these nitrogen atoms only exist in the very top layer of the surface. The result of matt Cu lead frames is demonstrated and shown in Figure 39. By far, only carbon and oxygen are left for discussion. The impurities intensity level of carbon and oxygen is confirmed to follow the order: shiny Cu > matt Cu > virgin Cu. This order is consistent with the level of Kirkendall voids in the frames. Therefore, carbon and oxygen seem to be elements that can contribute to Kirkendall voids in this case.

Table 3 *Surface elemental composition of rolled lead frame and three electroplated lead frames. In atomic concentration.*

<b>Lead Frame</b>	<b>C</b>	<b>N</b>	<b>O</b>	<b>Cu</b>	<b>Sn</b>	<b>Au</b>
Rolled Copper	59	2.6	24.1	10.7	-	2
Shiny Copper	58	3	28	12	-	-
Matt Copper	48	4	30	14	3	-
Virgin Copper	45	4	34	13	4	-

*Note. The composition value is an average value of several locations on lead frames. See Appendix B.*

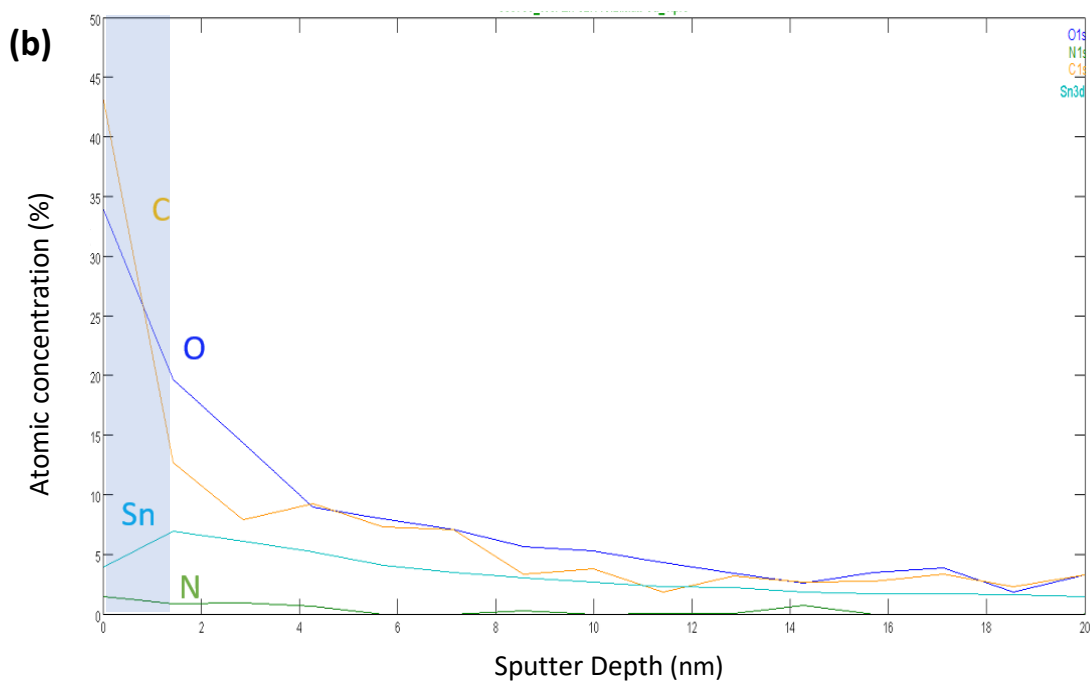
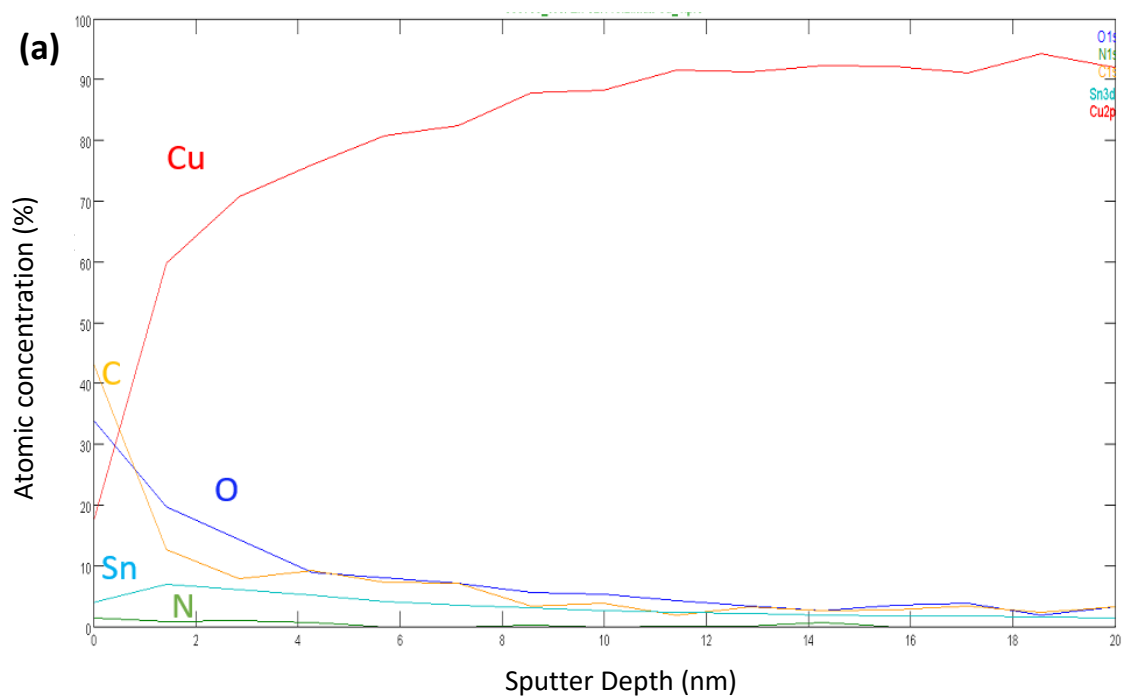


Figure 39 (a) XPS depth profile of matt Cu (b) Zoom in region of the depth profile without Cu. The shadow region is the oxidation layer which has a 1.8 nm thickness

#### 4.8. Cracks induced by voids

Failure tends to occur during mechanical polishing on samples with longer aging. Figure 40 show cracks that are generated during mechanical polishing. The interface between  $\text{Cu}_6\text{Sn}_5$  and  $\text{Cu}_3\text{Sn}$  serves as an easy path for brittle crack propagation because transmission of dislocations across the interface of IMC is a difficult process for  $\text{Cu}_6\text{Sn}_5$  and  $\text{Cu}_3\text{Sn}$  that have very few slip systems [49], see Figure 40a. The brittle nature of the IMC further assists cracks propagation through IMC especially when there are voids existing. Voids can act as stress concentrators amplifying the stress at a given point. Therefore, Figure 40 show the cracks propagating in IMC through the voids. Many researchers have pointed out when the IMC grows thicker, the fracture toughness of the solder joints will become lower [50, 51] leading to weaker connections. This conclusion can be qualitatively supported by mechanical polishing results of this thesis. Many units of bare dies couldn't be able to sustain the polishing stress resulting in peeling off from the frames when aging time increases.

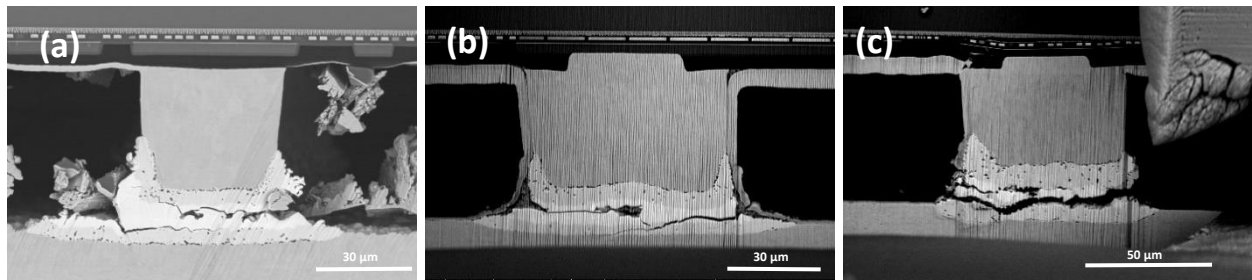


Figure 40 Crack propagate for (a) Matt Cu one-week aging (b) Rolled Cu two weeks aging (c) Rolled Cu four weeks aging

# 5

## Conclusions

This study set out to determine the influence of a variety of factors such as stress, underfill involvement, reflow times, additive level on void formation. Based on the set research objectives and following conclusions can be made:

*1. Understand the formation mechanism of voids in zero to four weeks of thermal aging and obtain the critical stress for either voids formation or self-healing.*

It was found that IMC formation is accompanied by volume shrinkage, which generates a high local stress. When this local tensile stress exceeds the critical stress of void formation, voids will start to form. The critical formation stress is 59 MPa for a 3  $\mu\text{m}$  void. In addition, voids can annihilate themselves when the local tensile stress at voids tips are suppressed by compressive stress that comes from outcurve solder ball volume shrinkage. This phenomenon is influenced by the geometry of solder joints so it might not appear in every solder joint. After all, a thorough self-healing mechanism is still lacking.

*2. Develop finite element model demonstrating the strain at interfaces with and without underfill.*

FEA model was successfully developed to simulate the shape shrinkage of the solder ball taking place after aging. Furthermore, the model successfully simulated strain deformation at the IMC interfaces due to volume shrinkage induced by IMC formation. For solder joints subjected to underfill, strain can be as high as 60 % while it can only be 25 % without underfill. The results of simulation were validated by the experimental result of voids formation. These suggest underfill application is crucial to solder reliability. However, aspects such as diffusion mechanism and grain orientation were not considered in this model. These can be very helpful to improve accuracy of the model.

*3. Develop a comprehensive model on void formation in Cu/Sn/Cu sandwich structure to understand the relation between the void formation, volume shrinkage and underfill involvement.*

A model was built to demonstrate the void formation in Cu/Sn/Cu sandwich structure, see Figure 32. In a Cu/Sn/Cu without underfill sandwich structure; the volume shrinkage induced stress can be compensated by height shrinkage. However, voids could occasionally form when the height shrinkage is not capable to fully release the IMC shrinkage stress. The stress will then cause voids to form in solder island positions where plastic deformation occurs. In contrast, in a structure where there is underfill sustaining and constraining height from decreasing, local tensile stress accumulates at the center faster than structures without underfill due to the absence of height

shrinkage. Therefore, voids can be found more easily when there is an underfill in the system. The result can be supported by simulated strain in FEA model. The limitation in this void formation sandwich model is that it is experimentally unfeasible to measure the height shrinkage of two IMC separately. Hence it is difficult to predict how much voids should form in order to relieve the total height shrinkage.

*4. Acquire knowledge on how to create void-free solder joints by controlling the impurities of Cu substrates.*

Higher additive level can accelerate Kirkendall void formation drastically. This phenomenon was proven in this study by examining three  $\text{Cu}_3\text{Sn}/\text{Cu}$  interfaces each with different electroplated additive level on Cu lead frames. Impurities can provide the system with more nucleation sites for voids nucleation and making the vacancies sink such as grain boundaries and dislocations inoperative at the same time. Several researchers have ascribed this phenomenon to various impurities such as Sulphur, Hydrogen etc. [26, 28]. However, in this study, C and O were found to be responsible for voids too. This implies that more than one specific element can give rise to serious Kirkendall voids. By eliminating these elements during electroplating, the voids can be largely reduced, and the reliability of solder joint would thus increase. Nevertheless, because of the resolution limitation of XPS, TOD-SIMS can be considered for a more sensitive surface analysis.

*5. Include effect of multiple reflow times to the tested samples and determine how to overcome the cracks induced by multiple reflow times.*

Higher reflow times enhances diffusion rate and reactions leading to more cracks in solder joints because of differences of coefficient of thermal expansion (CTE). Underfill can suppress these cracks from forming.

The terms described above leads to the following general conclusion:

Voids formation has a close relationship with volume shrinkage and stress. IMC formation induces volume shrinkage accompanied by a tensile stress causing large strain and voids in solder vicinity. Underfill involvement changes the stress field of the solder joints largely thus has huge impact on the formation of voids. Typically speaking, voids form more frequently when there is an underfill. This result is supported by a FEM simulation. The simulated strain induced by intermetallic compounds formation at the interfaces is much higher when the solder joints are subjected to underfill. In some cases, voids can annihilate themselves by the healing mechanism. However, it only happens when the geometry of the joints applies a compressive stress at the voids tips to compensate the formation of tensile stress. Electroplated Cu substrates increase Kirkendall voids at the interfaces. These voids can be reduced by eliminating carbon and organic additives during electroplating. Controlling the impurities on plated Cu surface and reduce the tensile stress in solder interface can thus enhance the reliability of the solder joints.



# 6

## Recommendations

The following can be suggested for further research:

1. In section, we discussed how FEA simulation were used to model plastic strain deformation in solder joints. However, there is one major restriction in the model. The formation of  $\text{Cu}_3\text{Sn}$  was only considered to grow toward the solder direction which isn't completely true in reality. Including this part can enhance the accuracy of the simulation. In addition, more delicate properties such as grain orientations, anisotropic behavior of IMC can be considered valuable for future FEA simulation. Different geometries of the solder shape should also be considered.
2. Self-healing of voids did not draw much attention yet. Nevertheless, from either academic or industrial point of views, this intriguing effect is worth further study. Current explanation provided in this thesis considers stress only. Including diffusion mechanism into the discussion could be a promising approach. The different diffusion rates of Cu and Sn in IMC and solder at various temperatures could be taken into account. Considering the difference of diffusivities and stress field concurrently should grant an interesting result.
3. Crack propagation can be studied by performing shear test on all the studied samples in this report.
4. Electroplating process will introduce a residual stress on the coated surface. The curvature of the frame can be measured by laser scanning and can be used for calculation of surface residual stress by Stoney's equation [28]. Another calculable stress that contributes to void formation is a type of stress which arises from the existence of nonequilibrium concentration of lattice vacancies. These two stresses combine with voids occurrence from experimental results could set a criterion for void formation. Hence, measuring and calculating those stress can be very helpful for further understanding the void formation. In addition, other condition during electroplating could also be added into designs of experiment as well. For instance, controlling the current density, coating thickness to have a different quality of surfaces could help addressing which parameter has the most impact on void formation. XPS depth profile could also be conducted in the future to target composition intensities at specific interfaces. For example, targeting and analyzing  $\text{Cu}_3\text{Sn}/\text{Cu}$  interface where Kirkendall voids form would give information on what element segregate at this interface. Moreover, etching and higher resolution examination exposing grain boundaries using TEM could be another appealing method to investigate where the elements segregate at.
5. A main restriction for the  $\text{Cu}/\text{Sn}/\text{Cu}$  sandwich structure cross sectional examination was the cracks generated during polishing. In spite of the fact that ion milling could minimize these cracks, FIB should be considered more often in order to obtain a less destructing cross section.
6. In section, the volume shrinkage contribution to void formation has been discussed. However, it seems like this shrinkage from IMC transformation needs to be compensated by height shrinkage



and voids in the solder joints. As a result, the sum of height shrinkage and voids ration in the solder should equal to the theoretical volume shrinkage the solder joints are supposed to experience. The height shrinkage of Cu/Sn/Cu sandwich structure could be performed by optical profilometer and the voids proportion could be measured by SEM image measurement.

7. The amount of solder has an extraordinary influence on IMC growth because it controls how thick  $\text{Cu}_6\text{Sn}_5$  is able to grow. The Cu/Sn/Cu sandwich structure in this report has limited amount of solder which makes the joints eventually contain only  $\text{Cu}_3\text{Sn}$  phase. Increasing the amount of solder in future studies creates joints with both  $\text{Cu}_6\text{Sn}_5$  and  $\text{Cu}_3\text{Sn}$  phases that would possibly show different behavior of void formation.
8. TOF-SIMS can be considered for a more sensitive surface analysis. Sulphur which is used during electroplating wasn't detected by XPS in this study. It is suggested that the Sulphur level is too low to be quantified because of the detecting limit of XPS. On the other hand, TOF-SIMS can overcome this barrier and is able to detect elements which are very scarce on the surface.

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# Appendix A

## A.1 EDX analysis results of packaged test chip

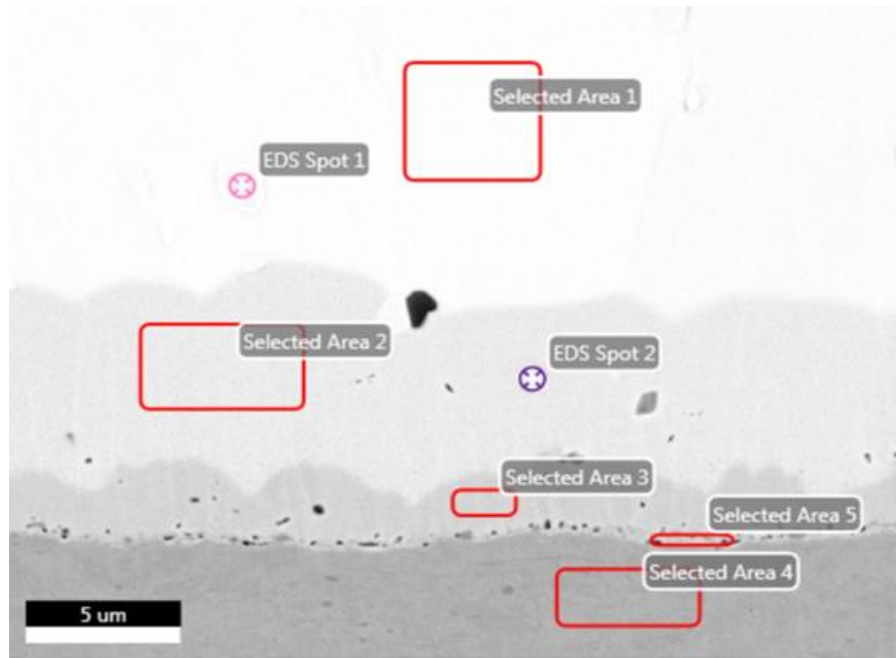
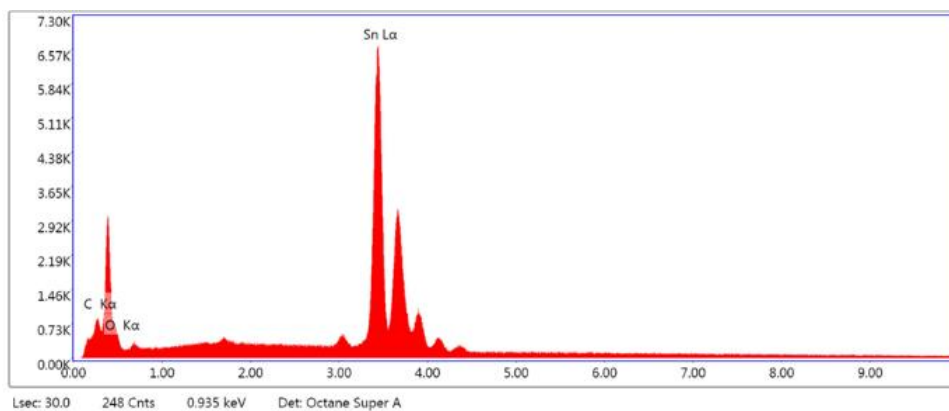
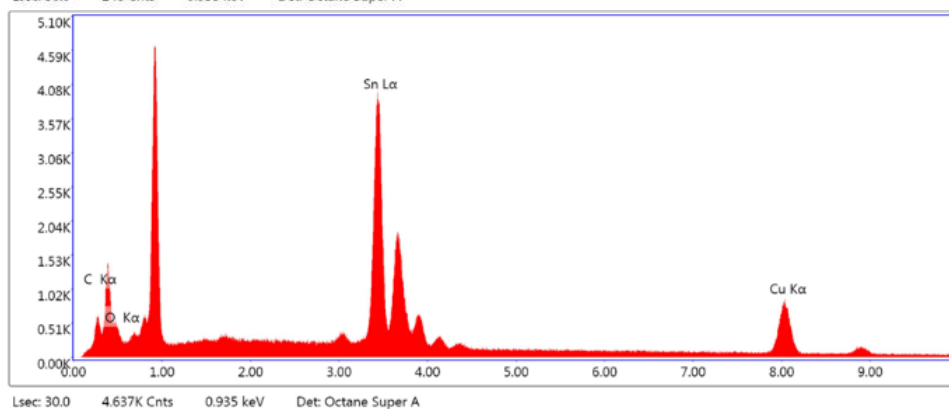


Figure A.1 The area taken for EDX analysis on the test chip

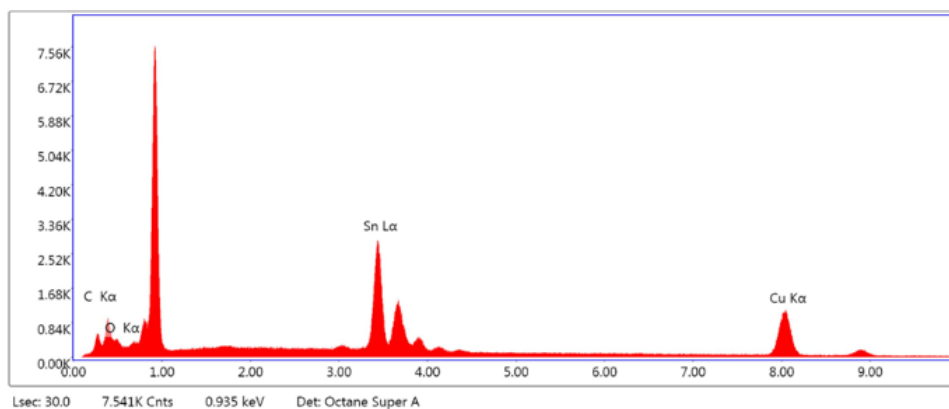
(a)



(b)



(c)



(d)

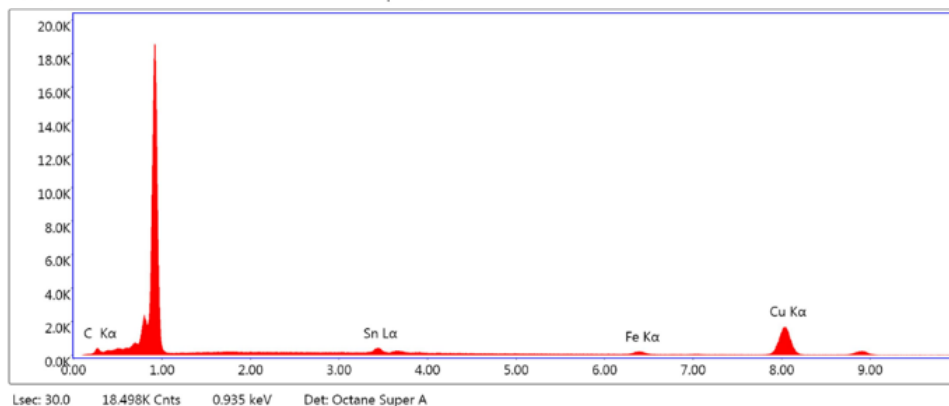
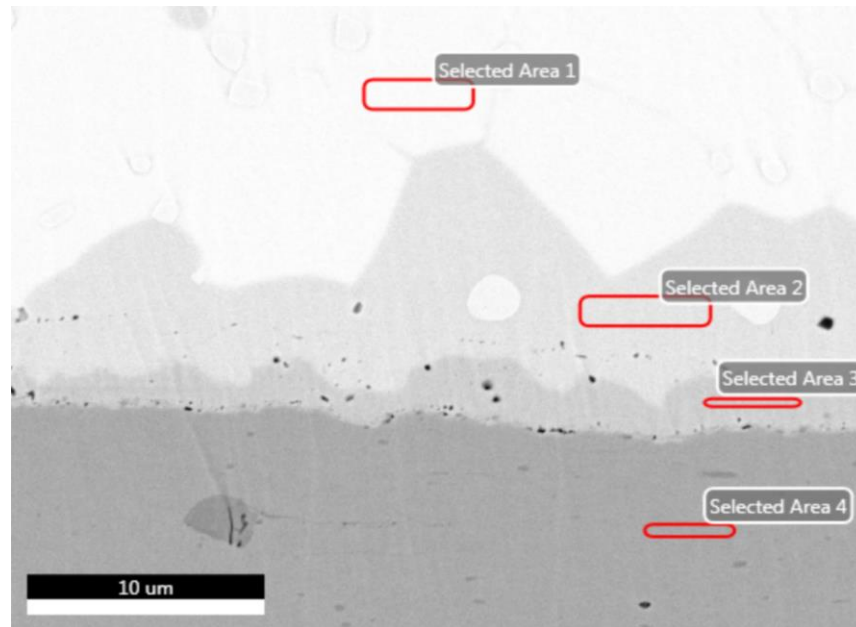


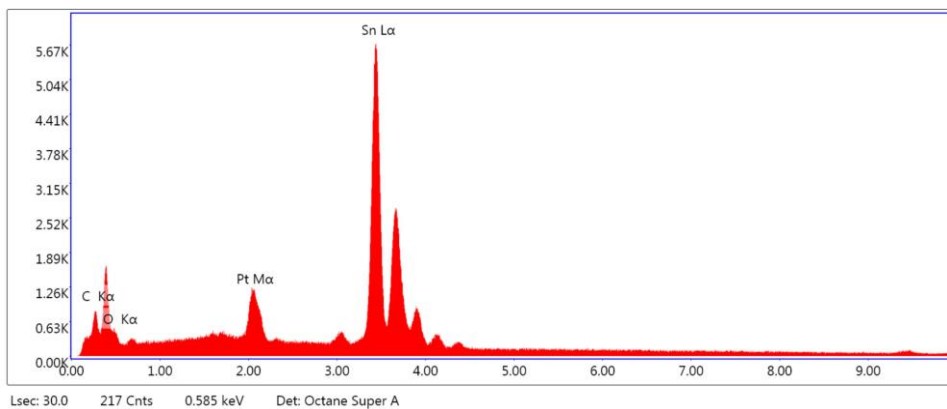
Figure A.2 Spectra of the points seen in Figure A.1 (a) Selected area 1 (b) Selected area 2 (c) Selected area 3 (d) Selected area 4

## A.2 EDX analysis results of bare dies system

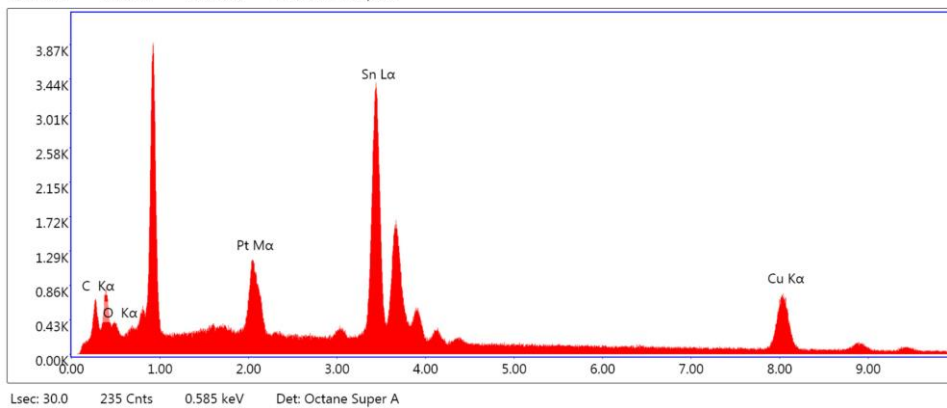


*Figure A.3 The area taken for EDX analysis on bare dies system*

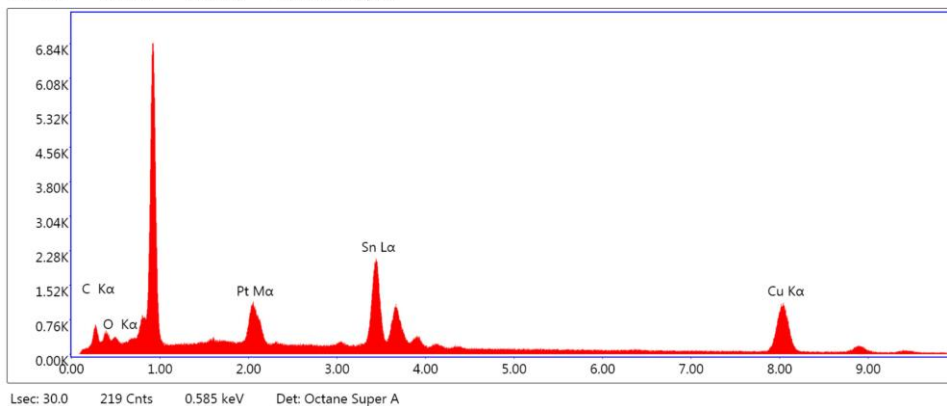
(a)



(b)



(c)



(d)

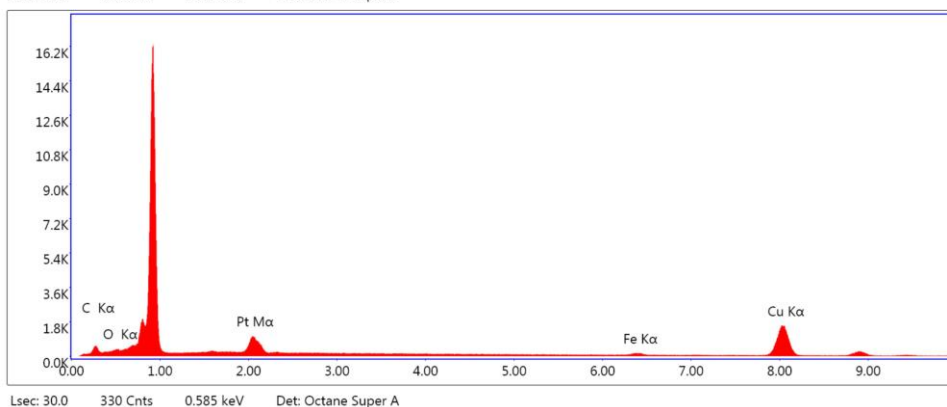


Figure A.4 Spectra of the points seen in Figure A.3 (a) Selected area 1 (b) Selected area 2 (c) Selected area 3 (d) Selected area 4



# Appendix B

## B.1 XPS results of rolled Cu lead frame

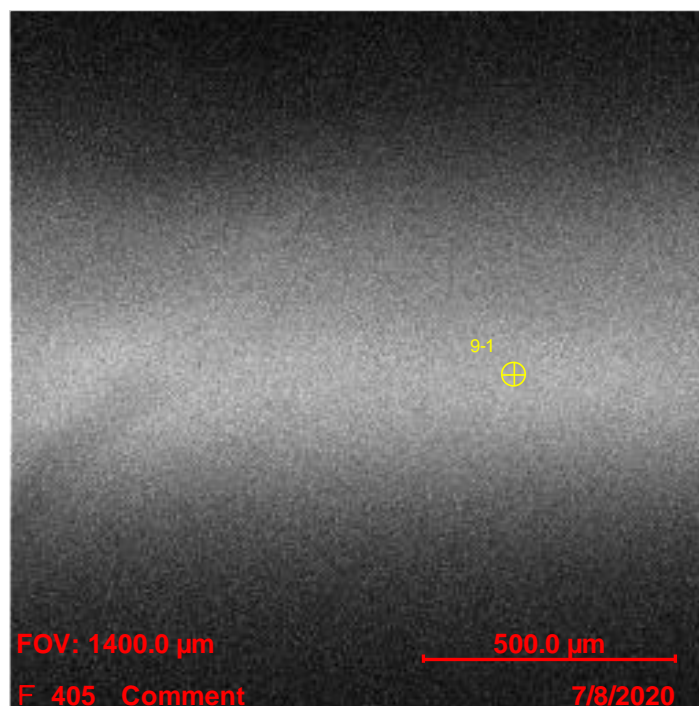


Figure B.1 The position taken for XPS analysis on rolled Cu

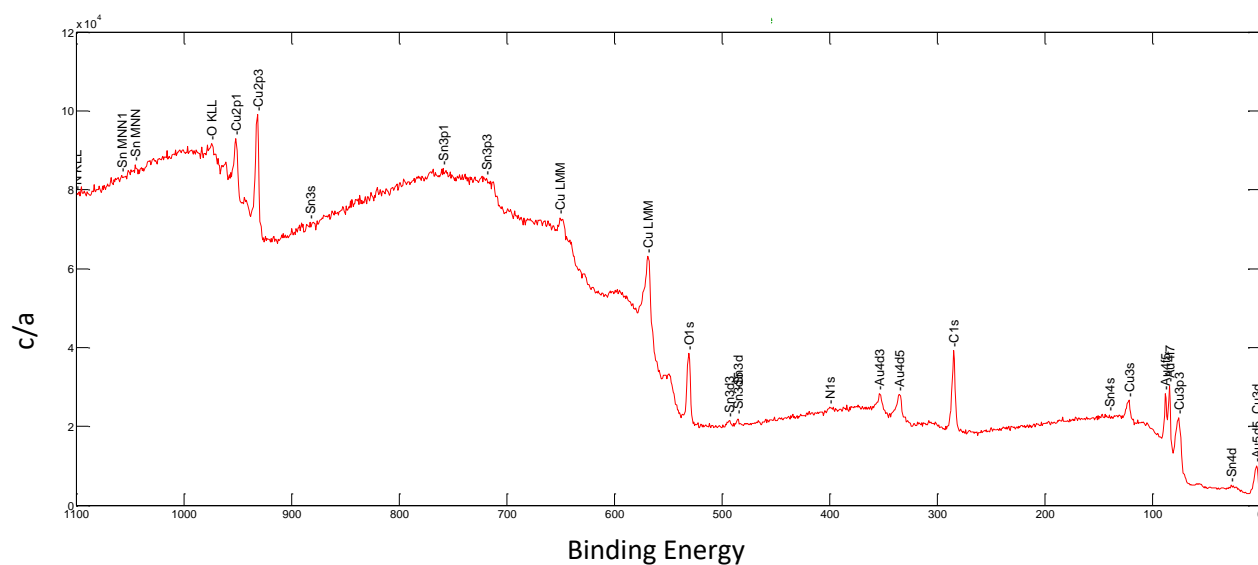


Figure B.2 XPS spectra of rolled Cu

## B.2 XPS results of electroplated virgin Cu lead frame

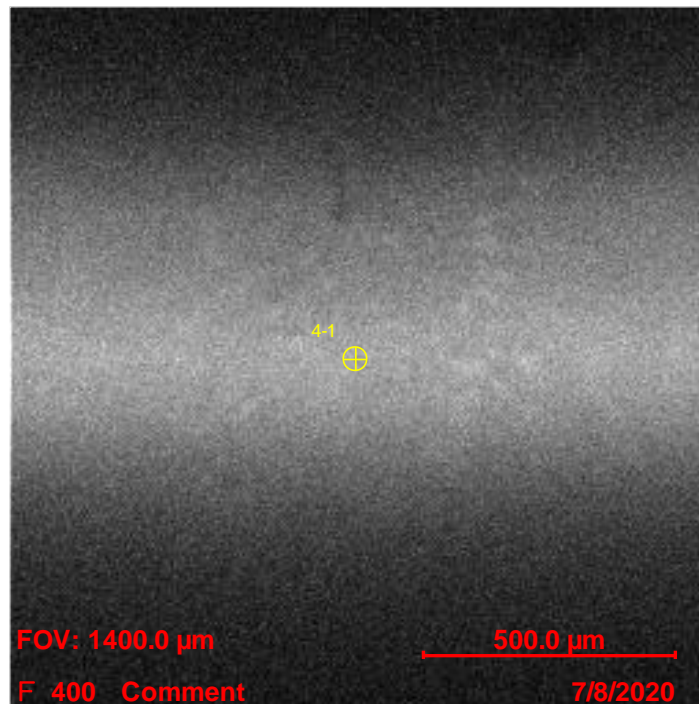


Figure B.3 The position taken for XPS analysis on virgin Cu

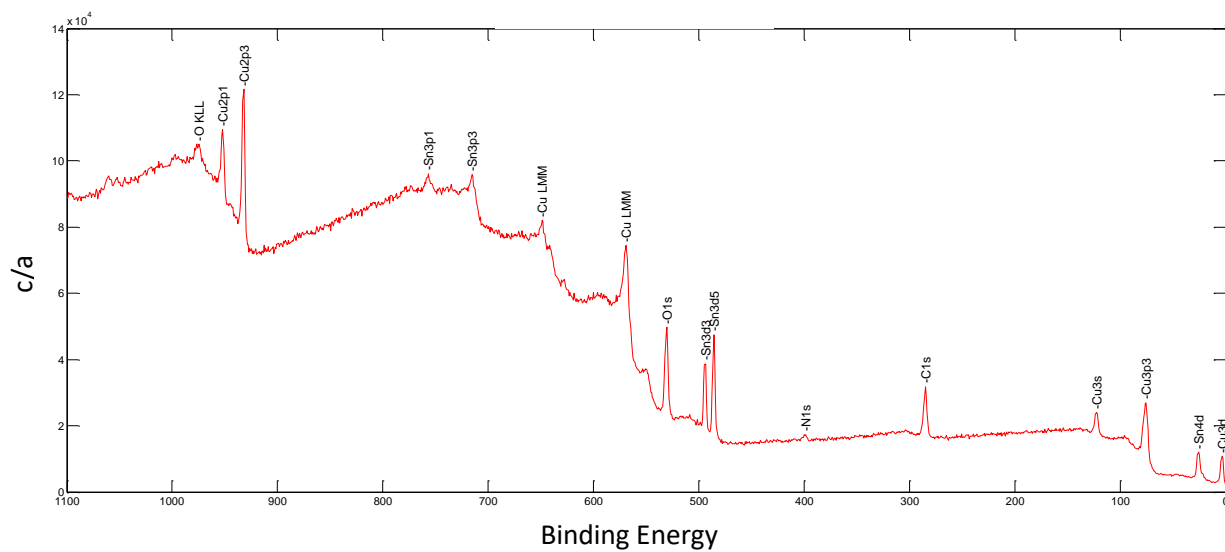


Figure B.4 XPS spectra of virgin Cu

### B.3 XPS results of electroplated shiny Cu lead frame

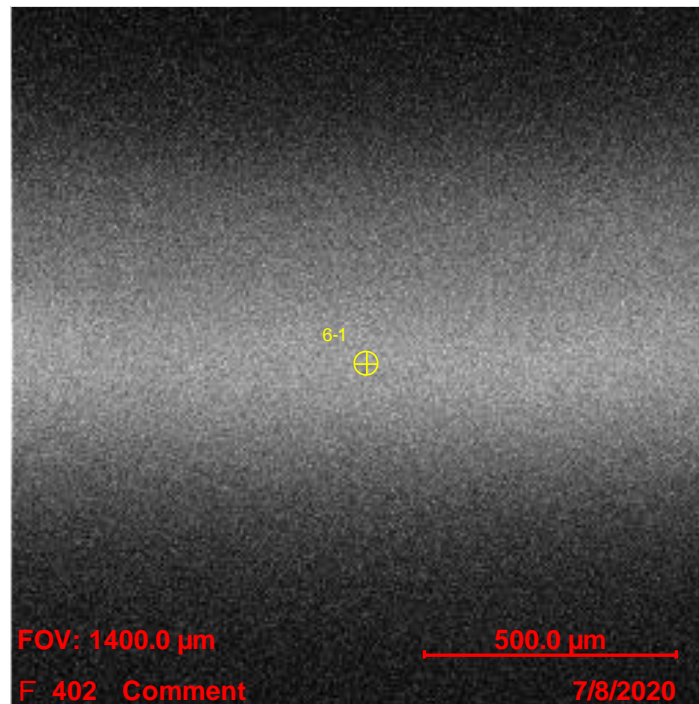


Figure B.5 The position taken for XPS analysis on shiny Cu

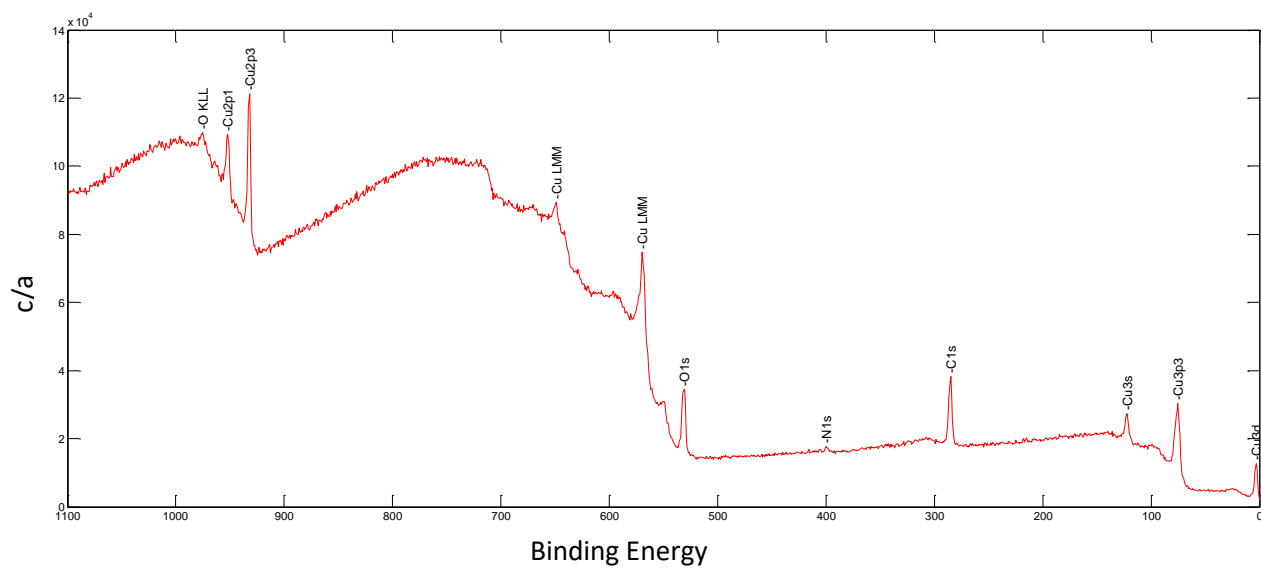


Figure B.6 XPS spectra of shiny Cu

## B.4 XPS results of electroplated matt Cu lead frame

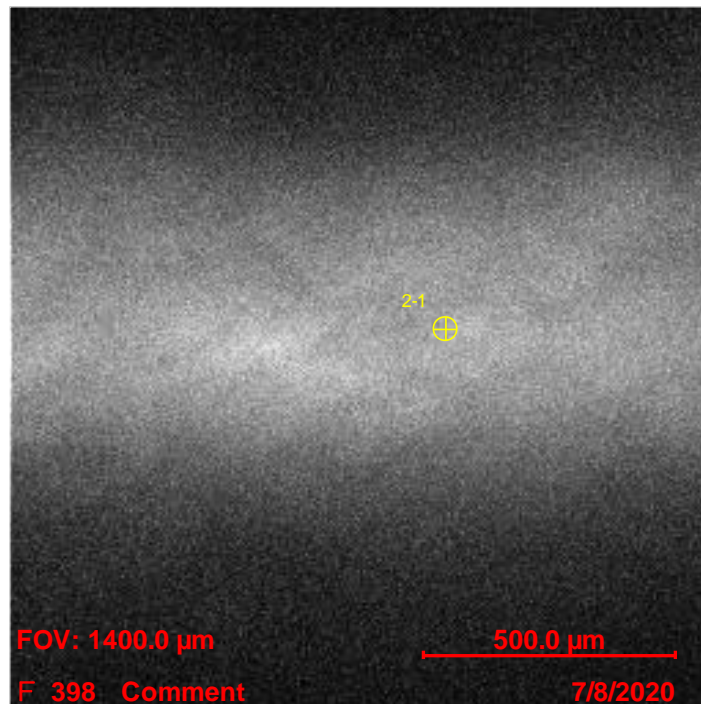


Figure B.7 The position taken for XPS analysis on matt Cu

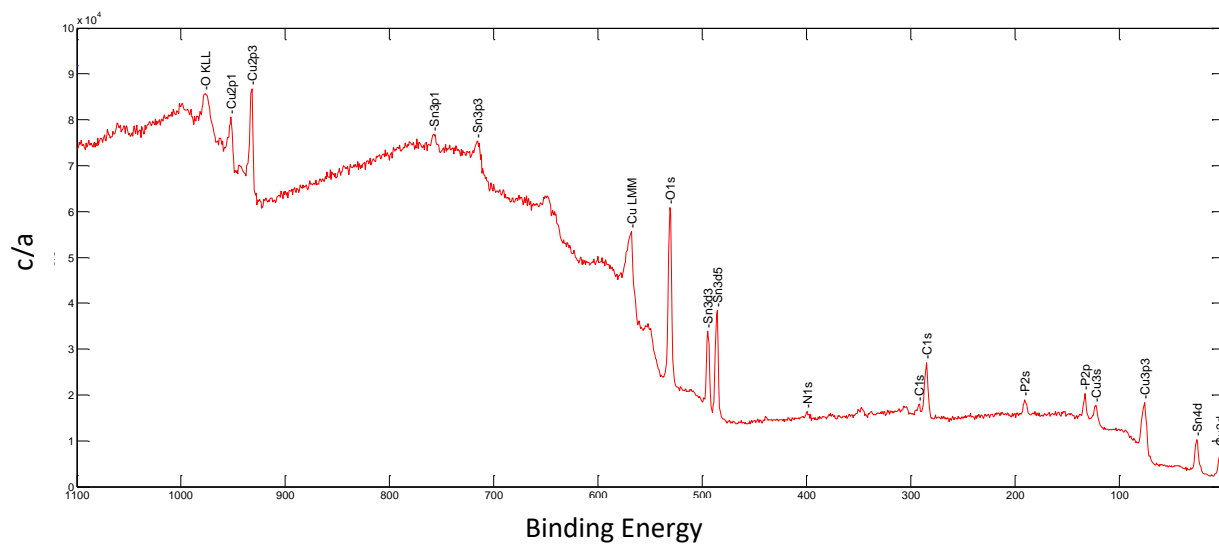


Figure B.8 XPS spectra of matt Cu

## B.5 XPS compositional analysis results of rolled Cu lead frame

Table B.1

*Compositional analysis results of rolled Cu. In atomic concentration.*

<i>Lead frame</i>	<i>Area</i>	<i>Comment</i>	<i>C1s</i>	<i>N1s</i>	<i>O1s</i>	<i>Cu2p3</i>	<i>Au4f</i>
<i>Rolled Cu</i>	1		55	3	28	12	2
<i>Rolled Cu</i>	2		61	3	23	10	2
<i>Rolled Cu</i>	3	Fine analysis	62.16	2.08	21.45	10.16	3.95
<i>Rolled Cu</i>	4	Analysis without flux	56.64	-	25.8	13.34	4.22

## B.6 XPS compositional analysis results of virgin Cu lead frame

Table B.2

*Compositional analysis results of virgin Cu. In atomic concentration.*

<i>Lead frame</i>	<i>Area</i>	<i>Comment</i>	<i>C1s</i>	<i>N1s</i>	<i>O1s</i>	<i>Cu2p3</i>	<i>Sn3d5</i>
<i>Virgin Cu</i>	1		45	4	34	13	2
<i>Virgin Cu</i>	2	Fine analysis	45.99	2.44	33.87	13.71	4
<i>Virgin Cu</i>	3	Analysis without flux	32.73	-	43.5	21.35	2.42

## B.7 XPS compositional analysis results of shiny Cu lead frame

Table B.3

*Compositional analysis results of shiny Cu. In atomic concentration.*

<i>Lead frame</i>	<i>Area</i>	<i>Comment</i>	<i>C1s</i>	<i>N1s</i>	<i>O1s</i>	<i>Cu2p3</i>
<i>Shiny Cu</i>	1		58	3	28	12
<i>Shiny Cu</i>	2	Fine analysis	58.63	2.1	26.64	12.64
<i>Shiny Cu</i>	3	Analysis without flux	53.36	-	31.42	15.22

## B.8 XPS compositional analysis results of matt Cu lead frame

Table B.4

*Compositional analysis results of matt Cu. In atomic concentration.*

<i>Lead frame</i>	<i>Area</i>	<i>Comment</i>	<i>C1s</i>	<i>N1s</i>	<i>O1s</i>	<i>Cu2p3</i>	<i>Sn3d5</i>
<i>Matt Cu</i>	1		48	4	30	14	3
<i>Matt Cu</i>	2	Fine analysis	48.45	4.23	29.34	14.68	3.3
<i>Matt Cu</i>	3	Analysis without flux	28.25	-	44.26	24.46	3.03



## B.9 XPS depth profile results of rolled Cu lead frame

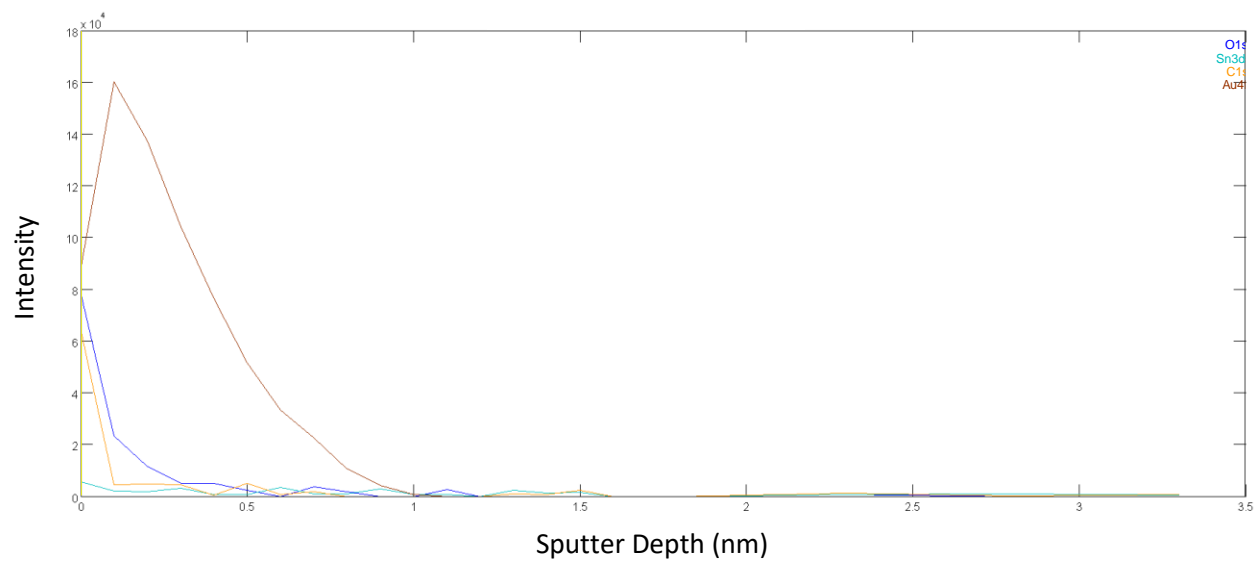


Figure B.9 XPS depth profile of rolled Cu

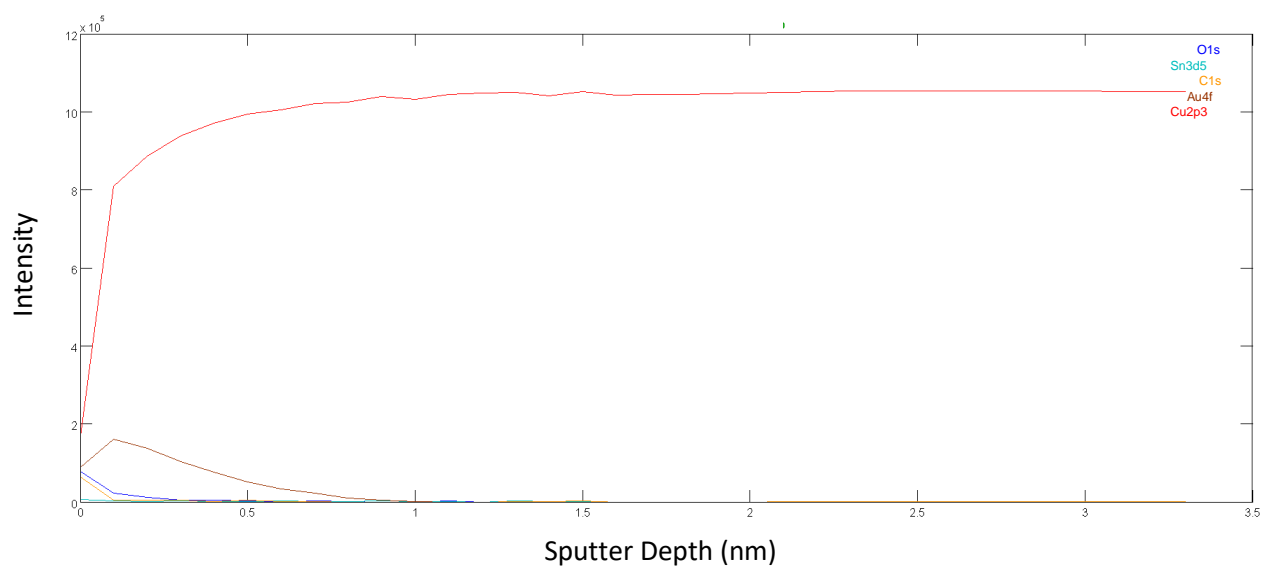


Figure B.10 zoom-in region of Figure B.9 without Cu

## B.10 XPS depth profile results of Virgin Cu lead frame

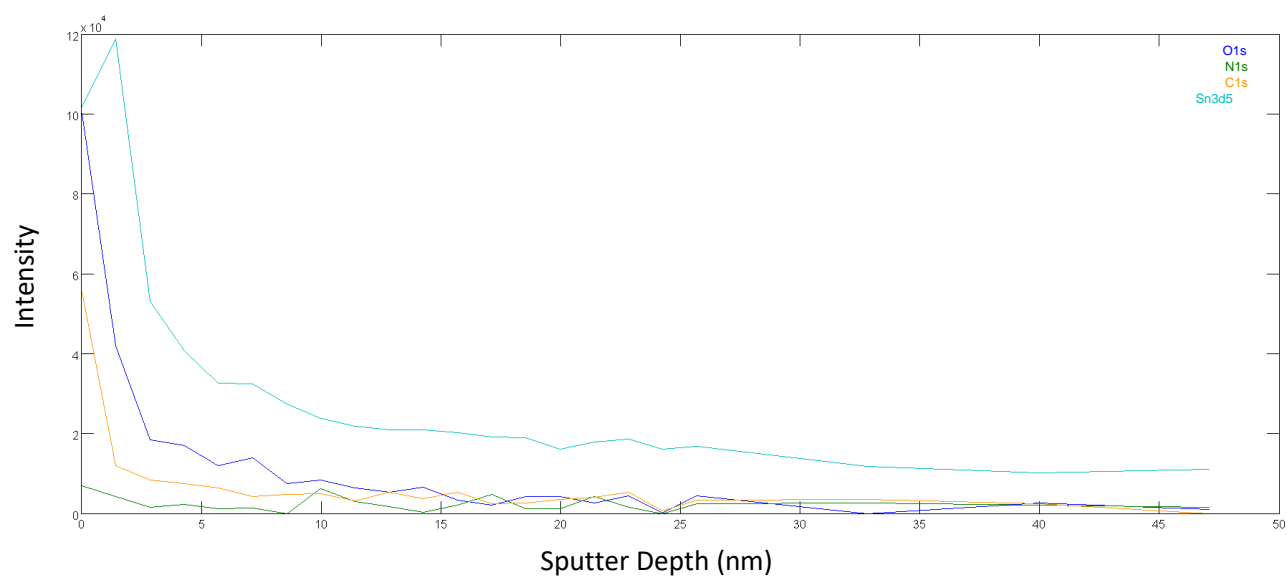


Figure B.11 XPS depth profile of virgin Cu

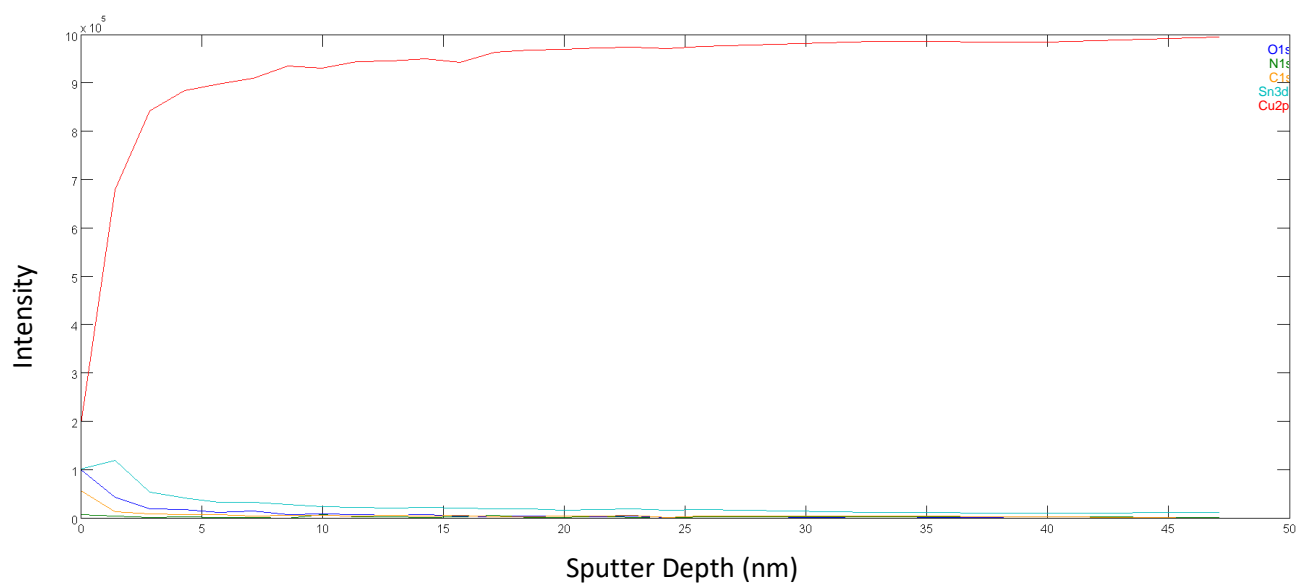


Figure B.12 Zoom-in region of Figure B.11 without Cu

## B.11 XPS depth profile results of shiny Cu lead frame

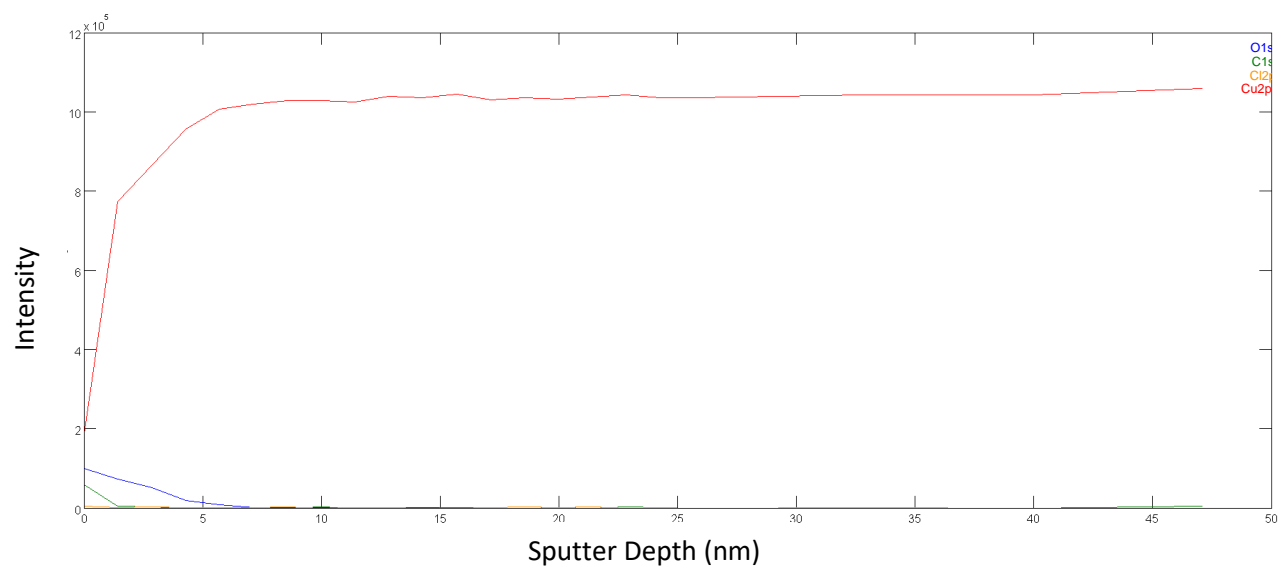


Figure B.13 XPS depth profile of shiny Cu

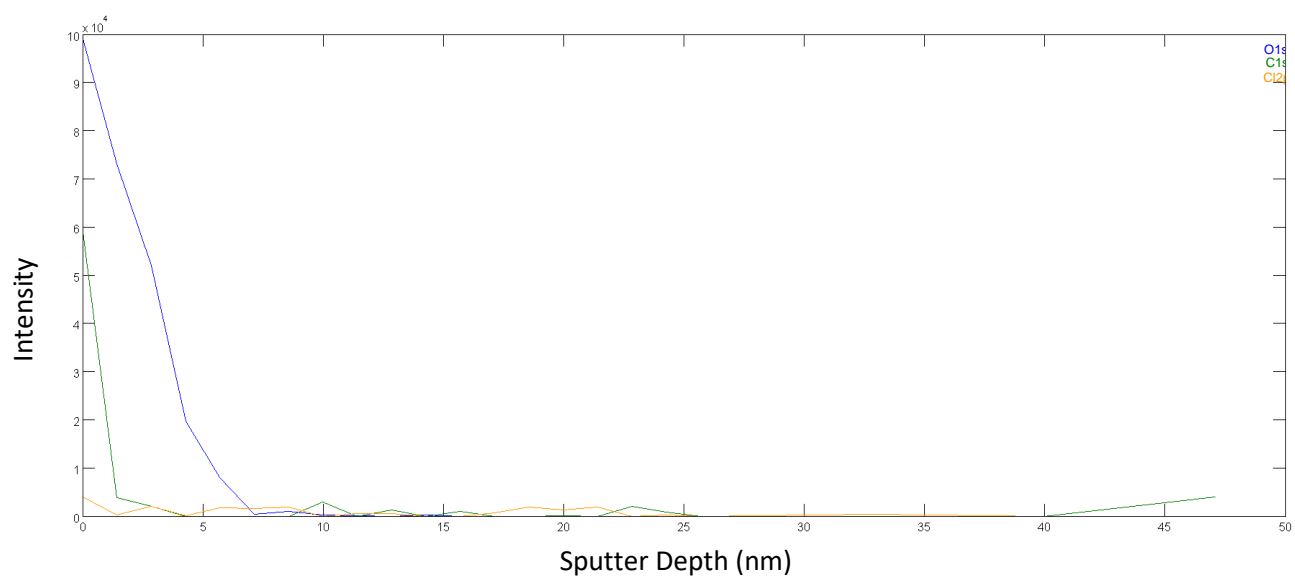


Figure B.14 Zoom-in region of Figure B.13 without Cu

## B.12 XPS depth profile results of matt Cu lead frame

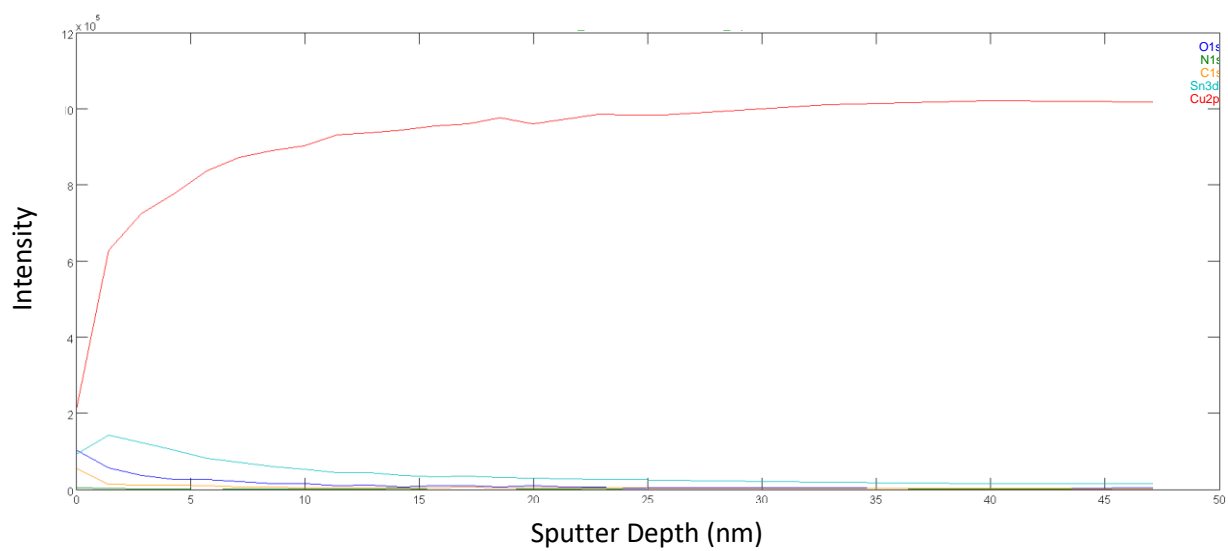


Figure B.15 XPS depth profile of matt Cu

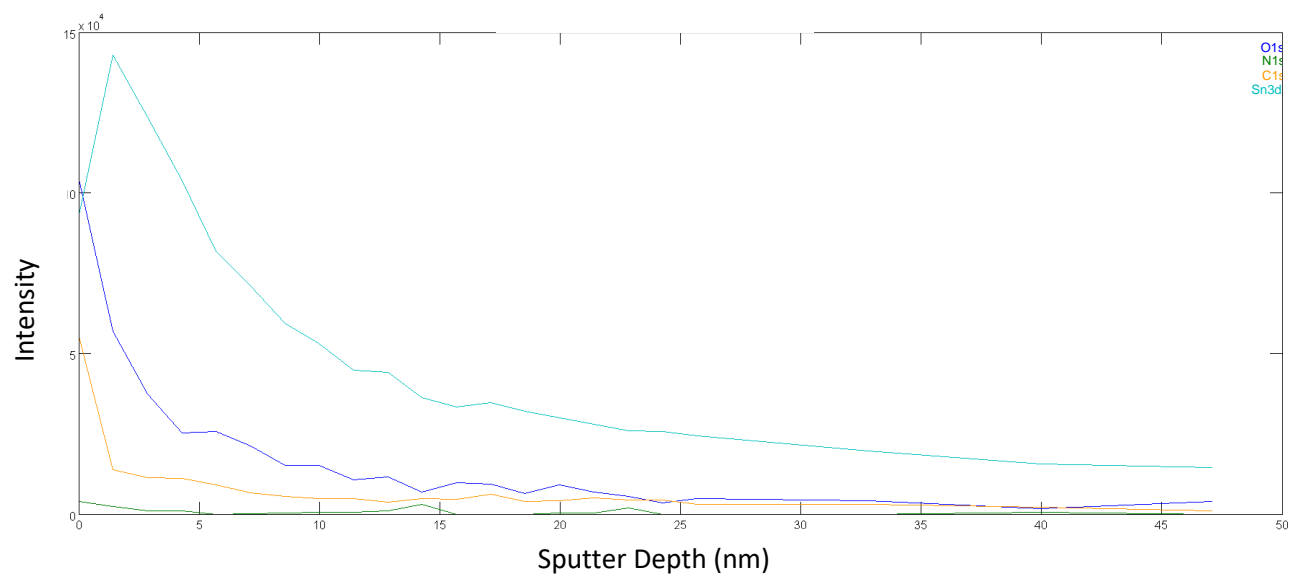


Figure B.16 Zoom-in region of Figure B.15 without Cu

